LINEAR
DATABOOK

NATIONAL
SEMICONDUCTOR
CORPORATION

LINEAR DATABOOK

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Introduction

This new 1982 edition of the National Semiconductor Linear Databook is the most comprehensive available. It presents approximately 2000 pages of specifications for our high technology linear products. Applications, descriptions, features and diagrams in this databook include detailed sections for Voltage Regulators, Op Amps, Voltage Comparators, A to D, D to A Converters, Industrial Blocks and Audio, Radio and TV Circuits.

The databook also features advanced telecommunication devices and speech synthesis (DIGITALKER™), plus other non-state-of-the-art linear products offering performance, economy, quality and reliability.

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Ordering Information

LM 101A F

- F — PACKAGE
- 101A — DEVICE NUMBER
- LM — DEVICE FAMILY

PACKAGE

D — Glass/Metal Dual-In-Line Package
F — Glass/Metal Flat Pack
H — TO-5 (TO-99, TO-100, TO-46)
J — Low Temperature Glass Dual-In-Line Package
K — TO-3 (Steel)
KC — TO-3 (Aluminum)
N — Plastic Dual-In-Line Package
P — TO-202 (D-40, Durawatt); also Single-In Line Package
S — "SGS" Type Power Dual-In-Line Package
T — TO-220
W — Low Temperature Glass Flat-Pack
Z — TO-92

DEVICE NUMBER

3, 4, or 5 Digit Number Suffix Indicators:
A — Improved Electrical Specification
C — Commercial Temperature Range

DEVICE FAMILY

AD — Analog to Digital
ADB — Analog to Digital Building Block
AH — Analog Hybrid
AM — Analog Monolithic
BLX — Board Level System
DAC — Digital to Analog Converter
DM — Digital Monolithic
DT — DIGITALKER™
HY — Hybrids
LF — Linear FET
LH — Linear Hybrid
LM — Linear Monolithic
MF — Monolithic Filter
MM — MOS Monolithic
TP — Telecommunications Product

Devices are listed in the table of contents alpha-numerically by device family (LH, LM, LX, etc.) and then by device number. **With most of National's proprietary linear circuits, a 1-2-3 numbering system is employed. The 1 denotes a Military temperature range device (−55°C to +125°C), the 2 denotes an Industrial temperature range device (−25°C to +85°C), and the 3 denotes a Commercial temperature range device (0°C to +70°C), i.e. LM101/LM201/LM301.**

Exceptions to this are the LM1800 series of consumer circuits which are specified for the commercial temperature range; some hybrid circuits which employ a "C" suffix to denote the commercial temperature range; and second-source products which follow the original manufacturers numbering system, i.e. LM741/LM741C or LM1414/LM1514.

Parts are generally listed in the table of contents by military part number first, i.e. LM139/LM239/LM339. Where a separate data sheet exists for a different temperature range, the device will be listed separately, i.e. LM119/LM219 and listed separately LM319. Where only one temperature range exists, the part will be listed in its proper order, i.e. LM340.

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Section 2—Voltage References

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† For additional information, see National Semiconductor's Hybrid Products Databook.

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Section 1

Voltage Regulators

1

Voltage Regulators†

Section Contents

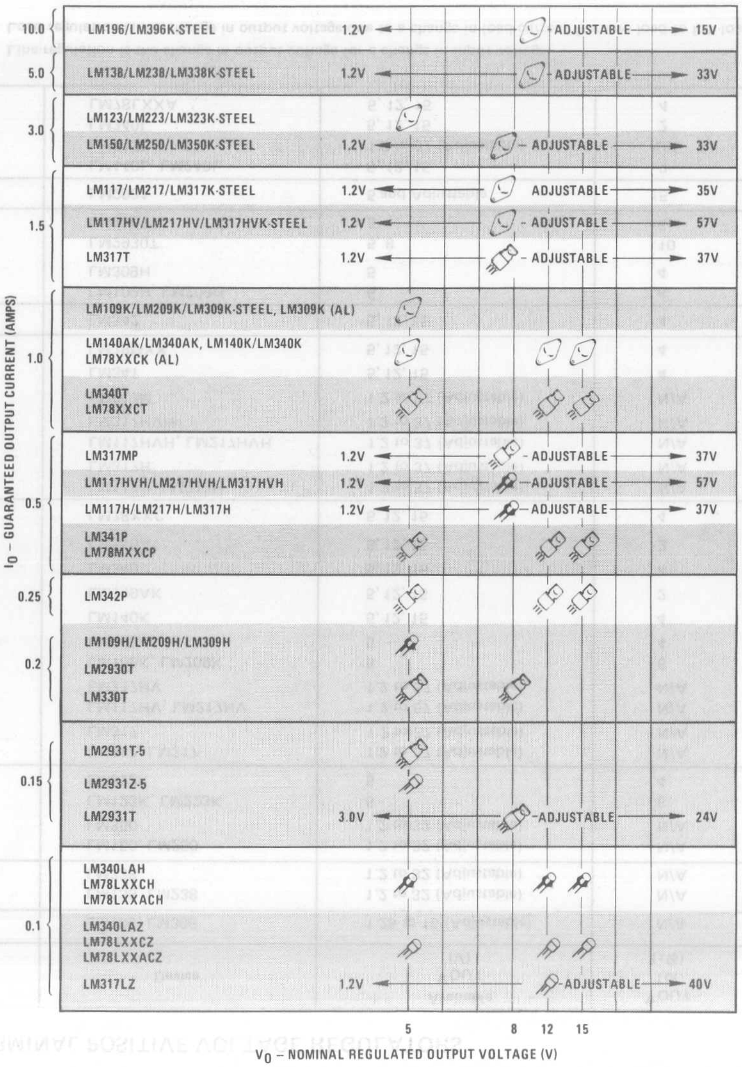
† For more information see National Semiconductor's Voltage Regulator Handbook.

3-TERMINAL POSITIVE VOLTAGE REGULATORS

Output Current (A)	Device	Available V_{OUT} (V)	V_{OUT} Tol. (±%)	Regulation: Line (Note 1) % V_{OUT}/V_{IN}	Regulation: Load (Note 2) % V_{OUT}/V_{IN}	V_{IN} (V) Max	Ripple Rejection (dB)
10	LM196, LM396	1.25 to 15 (Adjustable)	N/A	0.005	0.1	20	74
5	LM138, LM238	1.2 to 32 (Adjustable)	N/A	0.005	0.1	35	86
	LM338	1.2 to 32 (Adjustable)	N/A	0.005	0.1	35	86
3	LM150, LM250	1.2 to 32 (Adjustable)	N/A	0.005	0.1	35	86
	LM350	1.2 to 32 (Adjustable)	N/A	0.005	0.1	35	86
	LM123K, LM223K	5	6	0.01	0.5	20	75
	LM323K	5	4	0.01	0.5	20	75
1.5	LM117, LM217	1.2 to 37 (Adjustable)	N/A	0.01	0.1	40	80
	LM317	1.2 to 37 (Adjustable)	N/A	0.01	0.1	40	80
	LM117HV, LM217HV	1.2 to 57 (Adjustable)	N/A	0.01	0.1	60	80
	LM317HV	1.2 to 57 (Adjustable)	N/A	0.01	0.1	60	80
	LM109K, LM209K	5	6	0.004	1.0	35	80
	LM309K	5	4	0.004	1.0	35	80
	LM140K	5, 12, 15	4	0.02	0.5	35	66–80
	LM140AK	5, 12, 15	2	0.002	0.1	35	66–80
	LM340	5, 12, 15	4	0.02	0.5	35	66–80
	LM340A	5, 12, 15	2	0.002	0.1	35	66–80
	LM78XXC	5, 12, 15	4	0.03	0.5	35	66–80
0.5	LM117H, LM217H	1.2 to 37 (Adjustable)	N/A	0.01	0.1	40	80
	LM317H	1.2 to 37 (Adjustable)	N/A	0.01	0.1	40	80
	LM117HVH, LM217HVH	1.2 to 37 (Adjustable)	N/A	0.01	0.1	40	80
	LM317HVH	1.2 to 37 (Adjustable)	N/A	0.01	0.1	40	80
	LM317M	1.2 to 37 (Adjustable)	N/A	0.01	0.1	40	80
	LM341	5, 12, 15	4	0.02	0.5	35	
	LM78MXX	5, 12, 15	4	0.03	0.5	35	
0.25	LM342	5, 12, 15	4	0.03	0.5	35	53–64
0.20	LM109H, LM209H	5	6	0.004	0.4	35	80
	LM309H	5	4	0.004	0.4	35	80
	LM2930T	5, 8	±10			26V	56
	LM330T	5	±6			26V	56
0.15	LM2931	5 and Adjustable	±5	0.008	0.02	26	80
0.10	LM140L, LM240L	5, 12, 15	2	0.02	0.25	35	48–62
	LM317L	1.2 to 37 (Adjustable)	N/A	0.01	0.1	40V	65
	LM340L	5, 12, 15	2	0.02	0.25	35	48–62
	LM78LXXA	5, 12, 15	4	0.03	0.25	35	45–60

Note 1: Line regulation is the change in output voltage for a change in input voltage.

Note 2: Load regulation is the change in output voltage due to a change in load current from no load to full load.

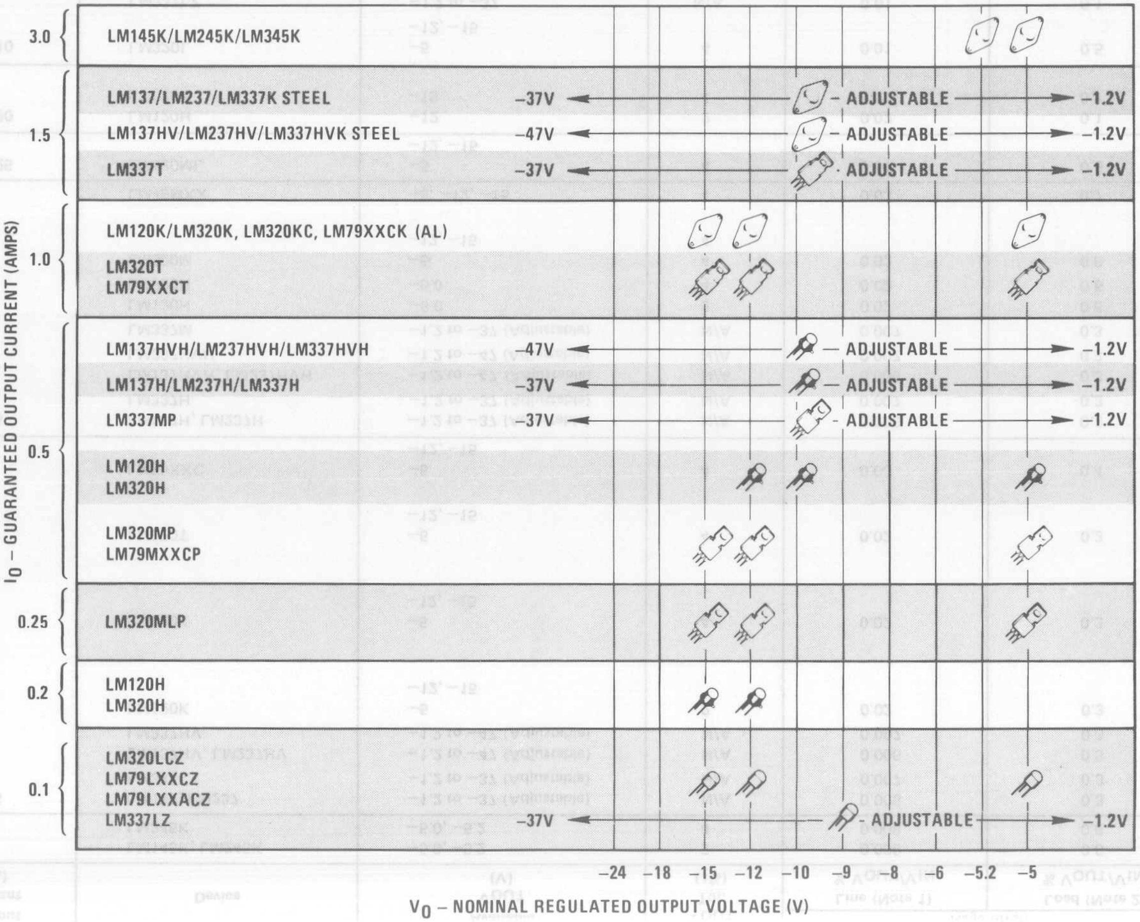


	PACKAGE DESIGNATOR	PACKAGE TYPE
	K KC K STEEL	TO-3* HERMETIC
	T	TO-220 PLASTIC
	P	TO-202 PLASTIC
	H	TO-5, TO-39 HERMETIC
	Z	TO-92 PLASTIC

*All devices with TO-3 package designators (K or K STEEL) are supplied in steel TO-3 packages unless otherwise designated as (AL) aluminum TO-3 package. All KC designated devices are supplied in aluminum TO-3.

3-TERMINAL NEGATIVE VOLTAGE REGULATORS

Output Current (A)	Device	Available V_{OUT} (V)	V_{OUT} Tol. (±%)	Regulation: Line (Note 1) % V_{OUT}/V_{IN}	Regulation: Load (Note 2) % V_{OUT}/V_{IN}	V_{IN} (V) Max	Ripple Rejection (dB)
3	LM145K, LM245K	−5.0, −5.2	2	0.008	0.6	20	68
	LM345K	−5.0, −5.2	4	0.008	0.6	20	68
1.5	LM137, LM237	−1.2 to −37 (Adjustable)	N/A	0.006	0.3	40	77
	LM337	−1.2 to −37 (Adjustable)	N/A	0.007	0.3	40	77
	LM137HV, LM237HV	−1.2 to −47 (Adjustable)	N/A	0.006	0.3	50	77
	LM337HV	−1.2 to −47 (Adjustable)	N/A	0.007	0.3	50	77
	LM120K	−5	2	0.02	0.3	25	64
		−12, −15				35 (12V)	80
						40 (15V)	75
							70
	LM320K	−5	4	0.02	0.3	25	64
		−12, −15				35 (12V)	80
						40 (15V)	75
							70
	LM320T	−5	4	0.02	0.3	25	64
		−12, −15				35 (12V, 15V)	75–80
							70
	LM79XXC	−5	4	0.03	0.4	35	66–70
		−12, −15					
0.5	LM137H, LM237H	−1.2 to −37 (Adjustable)	N/A	0.006	0.3	40	77
	LM337H	−1.2 to −37 (Adjustable)	N/A	0.007	0.3	40	77
	LM137HVH, LM237HVH	−1.2 to −47 (Adjustable)	N/A	0.006	0.3	50	77
	LM337HVH	−1.2 to −47 (Adjustable)	N/A	0.007	0.3	50	77
	LM337M	−1.2 to −37 (Adjustable)	N/A	0.007	0.3	40	77
	LM120H	−5.0	2	0.02	0.6	25	64
	LM320H	−5.0	4	0.02	0.6	25	64
	LM320M	−5	4	0.02	0.6	25	60–64
		−12, −15	4			35 (12V, 15V)	70–80
	LM79MXX	−5, −12, −15	4	0.03	0.7	35	58–60
0.25	LM320ML	−5	4	0.01	0.5	35	50–60
		−12, −15					
0.20	LM120H	−12	2	0.02	0.1	35 (12V)	70–80
	LM320H	−15	4	0.02	0.1	40 (15V)	
0.10	LM320L	−5	4	0.01	0.5	35	60–65
		−12, −15					
	LM337LZ	−1.2 to −37	N/A	0.01	0.1	40	65
	LM79LXXA	−5, −12, −15	4	0.02	0.6	35	50–55



	PACKAGE DESIGNATOR	PACK TY
	K KC K STEEL	TO- HERM
	T	TO-2 PLAS
	P	TO-2 PLAS
	H	TO-5, T HERM
	Z	TO- PLAS

*All devices with TO-3 package nators (K or K STEEL) are su in steel TO-3 packages unless oth designated as (AL) aluminum package. All KC designated c are supplied in aluminum TO-3.

Function	Features	Line Reg	Load Reg	I_{OUT} (mA)	V_{OUT} Toler. @25°C (Max)	Drift (Max)	Part Number −55°C to 125°C	Part Number −25°C to 85°C	Page Number *
Positive Programmable Voltage Regulator	Internal programming resistors, adjustable current limit, V_{OUT} = 5, 6, 8, 10, 12, 15, 18 V	0.008%	0.055%	0.1-200	0.5% 1%		LH0075	LH0075C	7-8
Negative Programmable Voltage Regulator	Internal programming resistors, adjustable current limit, V_{OUT} = 5, 6, 8, 10, 12, 15, 18 V	0.008%	0.055%	0.1-200	0.5% 1%		LH0076	LH0076C	7-13

*Refers to Hybrid Products Databook, 1982 edition

National Semiconductor

Definition of Terms

Current-Limit Sense Voltage: The voltage across the current limit terminals required to cause the regulator to current-limit with a short circuited output. This voltage is used to determine the value of the external current-limit resistor when external booster transistors are used.

Dropout Voltage: The input-output voltage differential at which the circuit ceases to regulate against further reductions in input voltage.

Feedback Sense Voltage: The voltage, referred to ground, on the feedback terminal of the regulator while it is operating in regulation.

Input Voltage Range: The range of dc input voltages over which the regulator will operate within specifications.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Long Term Stability: Output voltage stability under accelerated life-test conditions at 125°C with maximum rated voltages and power dissipation for 1000 hours.

Maximum Power Dissipation: The maximum total device dissipation for which the regulator will operate within specifications.

Output-Input Voltage Differential: The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate within specifications.

Output Noise Voltage: The RMS ac voltage at the output with constant load and no input ripple, measured over a specified frequency range.

Output Voltage Range: The range of regulated output voltages over which the specifications apply.

Output Voltage Scale Factor: The output voltage obtained for a unit value of resistance between the adjustment terminal and ground.

Quiescent Current: That part of input current to the regulator that is not delivered to the load.

Ripple Rejection: The line regulation for ac input signals at or above a given frequency with a specified value of bypass capacitor on the reference bypass terminal.

Standby Current Drain: That part of the operating current of the regulator which does not contribute to the load current.

Temperature Stability: The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

Thermal Regulation: Percentage change in output voltage for a given change in power dissipation over a specified time period.

National Semiconductor

Fixed or Adjustable Voltage Regulators

At National we see the trend moving toward the use of more adjustable regulators and we are broadening the adjustable line to satisfy this demand.

As you browse through this Voltage Regulator section you will notice many changes. We've expanded the adjustable regulator line and many voltage options on fixed regulators have been deleted.

The fixed voltage regulators, like the 7800 and 7900 series, resulted in customers having to stock and hold in inventory quantities of each voltage in order to always have on hand a specific device for a particular system. This proved to be very costly especially when production was stopped due to shortage of a particular voltage.

Adjustables combine versatility, performance and reliability, leading to increased popularity.

Versatility

- Satisfy output voltage requirements from 1.2V up to 47V
- Simplify inventory and purchasing since a single device satisfies many voltage requirements
- Allows precision application

Performance

- Improves system performance by having line and load regulation a factor of 10 better
- Has improved overload protection thus allowing greater output current over operating temperature range

Reliability

- Improves system reliability with each device being subjected to 100% thermal limit burn-in

As more and more applications use adjustable regulators, we believe that they will become the most popular regulators in the industry.

National Semiconductor

LM104/LM204/LM304 Negative Regulator

General Description

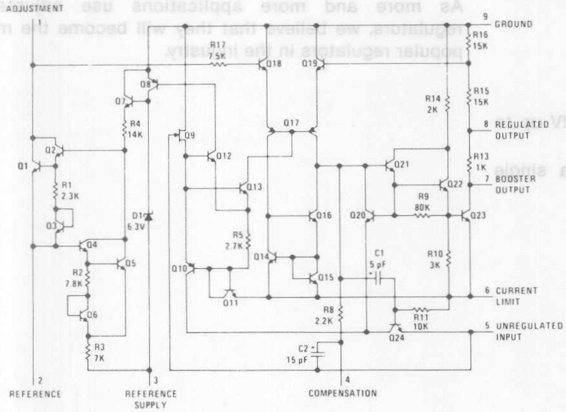
The LM104 series are precision voltage regulators which can be programmed by a single external resistor to supply any voltage from 40V down to zero while operating from a single unregulated supply. They can also provide 0.01-percent regulation in circuits using a separate, floating bias supply, where the output voltage is limited only by the breakdown of external pass transistors. Although designed primarily as linear, series regulators, the circuits can be used as switching regulators, current regulators or in a number of other control applications. Typical performance characteristics are:

- Subsurface zener reference
- 1 mV regulation no load to full load
- 0.01%/V line regulation
- 0.2 mV/V ripple rejection
- 0.3% temperature stability over military temperature range

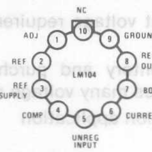
The LM104 series are complements of the LM100 and LM105 positive regulators, intended for systems requiring regulated negative voltages which have a common ground with the unregulated supply. By themselves, they can deliver output currents to 25 mA, but external transistors can be added to get any desired current. The output voltage is set by external resistors, and either constant or foldback current limiting is made available.

The LM104 is specified for operation over the −55°C to +125°C military temperature range. The LM204 is specified for operation over the −25°C to +85°C temperature range. The LM304 is specified for operation from 0°C to +70°C.

Schematic and Connection Diagrams



Metal Can Package



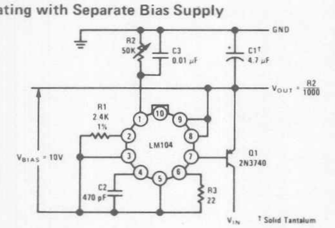
Note: Pin 5 connected to case.

TOP VIEW

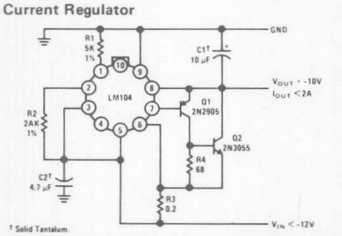
Order Number LM104H, LM204H or LM304H
See NS Package H10C

Typical Applications

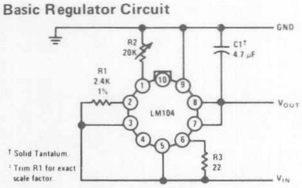
Operating with Separate Bias Supply



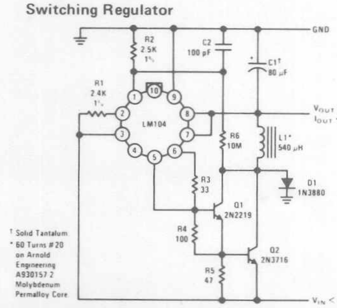
High Current Regulator



Basic Regulator Circuit



Switching Regulator



Absolute Maximum Ratings

	LM104/LM204	LM304
Input Voltage	50V	40V
Input-Output Voltage Differential	50V	40V
Power Dissipation (Note 1)	500 mW	500 mW
Operating Temperature Range		
LM104	−55°C to 125°C	
LM204	−25°C to 85°C	
LM304		0°C to +70°C
Storage Temperature Range	−65°C to 150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C	300°C

Electrical Characteristics

PARAMETER	CONDITIONS	LM104/LM204			LM304			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Voltage Range		−50		−8	−40		−8	V
Output Voltage Range		−40		−0.015	−30		−0.035	V
Output-Input Voltage Differential (Note 3)	I_O = 20 mA	2.0		50	2.0		40	V
	I_O = 5 mA	0.5		50	0.5		40	V
Load Regulation (Note 4)	$0 \leq I_O \leq 20$ mA, $R_{SC} = 15\Omega$		1	5		1	5	mV
Line Regulation (Note 5)	$V_{OUT} \leq -5V$, $\Delta V_{IN} = 0.1\ V_{IN}$		0.056	0.1		0.056	0.1	%
Ripple Rejection	$C_{19} = 10\ \mu F$, f = 120 Hz, $V_{IN} < -15V$		0.2	0.5		0.2	0.5	mV/V
	$-7V \geq V_{IN} \geq -15V$		0.5	1.0		0.5	1.0	mV/V
Output Voltage Scale Factor	R_{23} = 2.4k	1.8	2.0	2.2	1.8	2.0	2.2	V/kΩ
Temperature Stability	$V_O \leq -1V$		0.3	1.0		0.3	1.0	%
Output Noise Voltage	$10\ Hz \leq f \leq 10\ kHz$, $V_O \leq -5V$, $C_{19} = 0$		0.007			0.007		%
	$C_{19} = 10\ \mu F$		15			15		µV
Standby Current Drain	$I_L = 5$ mA, $V_O = 0$		1.7	2.5		1.7	2.5	mA
	$V_O = -30V$					3.6	5.0	mA
	$V_O = -40V$		3.6	5.0				mA
Long Term Stability	$V_O \leq -1V$		0.01	1.0		0.01	1.0	%

Note 1: The maximum junction temperature of the LM104 is 150°C, while that of the LM204 is 125°C and LM304 is 100°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case.

Note 2: These specifications apply for junction temperatures between −55°C and 150°C (between −25°C and 100°C for the LM204 and 0°C to +85°C for the LM304) and for input and output voltages within the ranges given, unless otherwise specified. The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.

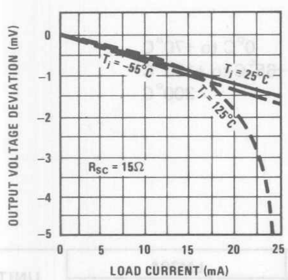
Note 3: When external booster transistors are used, the minimum output-input voltage differential is increased, in the worst case, by approximately 1V.

Note 4: The output currents given, as well as the load regulation, can be increased by the addition of external transistors. The improvement factor will be roughly equal to the composite current gain of the added transistors.

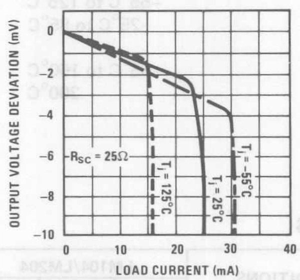
Note 5: With zero output, the dc line regulation is determined from the ripple rejection. Hence, with output voltages between 0V and −5V, a dc output variation, determined from the ripple rejection, must be added to find the worst-case line regulation.

Typical Performance Characteristics

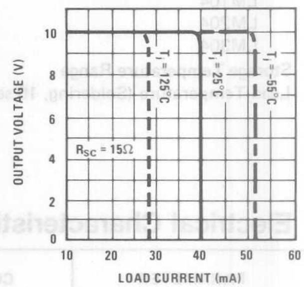
Load Regulation



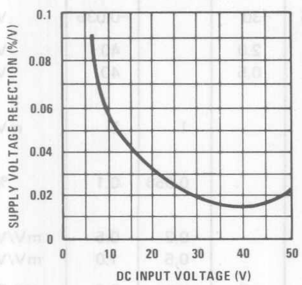
Load Regulation



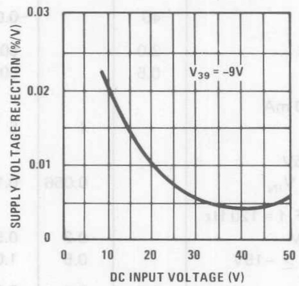
Current Limiting



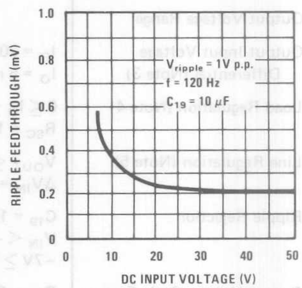
Supply Voltage Rejection



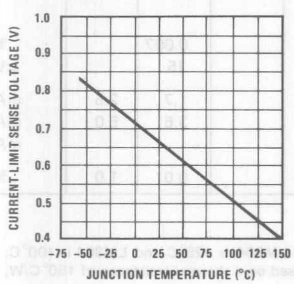
Supply Voltage Rejection With Preregulated Reference Supply



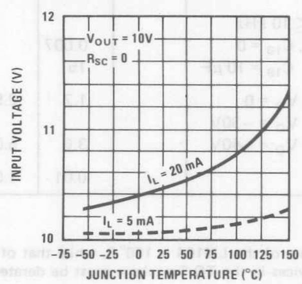
Ripple Rejection



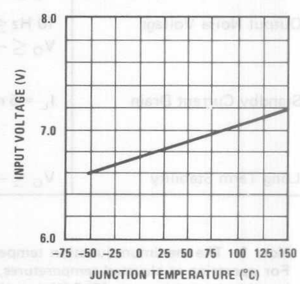
Current Limit Sense Voltage



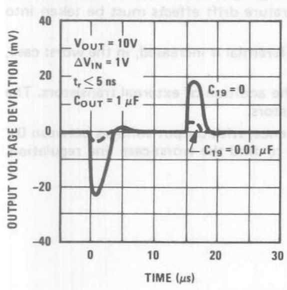
Regulator Dropout Voltage



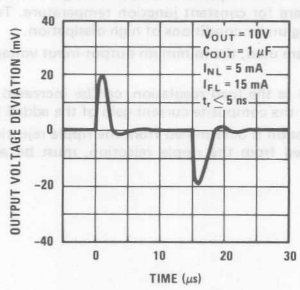
Minimum Input Voltage



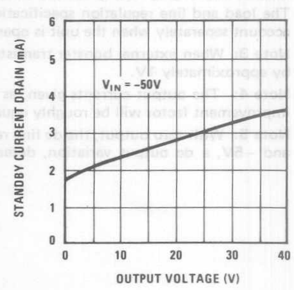
Line Transient Response



Load Transient Response



Standby Current Drain



National Semiconductor

Voltage Regulators

LM105/LM205/LM305/LM305A, LM376 Voltage Regulators

General Description

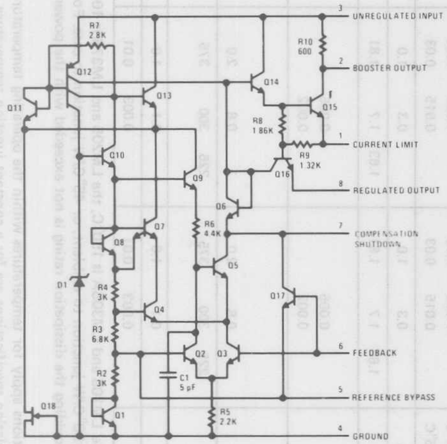
The LM105 series are positive voltage regulators similar to the LM100, except that an extra gain stage has been added for improved regulation. A redesign of the biasing circuitry removes any minimum load current requirement and at the same time reduces standby current drain, permitting higher voltage operation. They are direct, plug-in replacements for the LM100 in both linear and switching regulator circuits with output voltages greater than 4.5V. Important characteristics of the circuits are:

- Output voltage adjustable from 4.5V to 40V
- Output currents in excess of 10A possible by adding external transistors
- Load regulation better than 0.1%, full load with current limiting
- DC line regulation guaranteed at 0.03%/V
- Ripple rejection of 0.01%/V
- 45 mA output current without external pass transistor (LM305A)

Like the LM100, they also feature fast response to both load and line transients, freedom from oscillations with varying resistive and reactive loads and the ability to start reliably on any load within rating. The circuits are built on a single silicon chip and are supplied in either an 8-lead, TO-5 header or a 1/4" x 1/4" metal flat package.

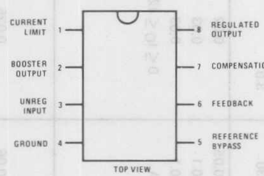
The LM105 is specified for operation for $-55^{\circ}C \leq T_A \leq +125^{\circ}C$, the LM205 is specified for $-25^{\circ}C \leq T_A \leq +85^{\circ}C$, and the LM305/LM305A, LM376 is specified for $0^{\circ}C \leq T_A \leq +70^{\circ}C$.

Schematic and Connection Diagrams



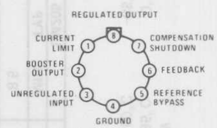
Pin connections shown are for metal can.

Dual-In-Line Package



Order Number LM376N
See NS Package N08B

Metal Can Package

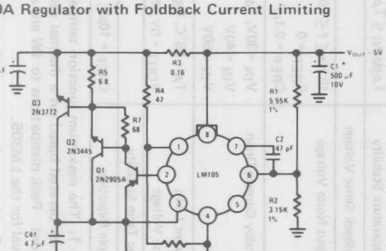


Note: Pin 4 connected to case.
TOP VIEW

Order Number LM105H, LM205H, LM305H or LM305AH
See NS Package H08C

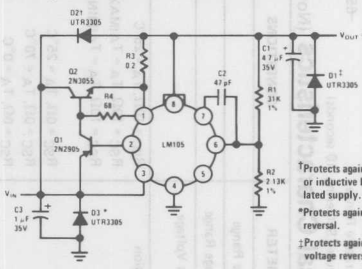
Typical Applications

10A Regulator with Foldback Current Limiting



†Solid tantalum.
*Electrolytic.

1.0A Regulator with Protective Diodes



†Protects against shorted input or inductive loads on unregulated supply.
*Protects against input voltage reversal.
‡Protects against output voltage reversal.

Absolute Maximum Ratings

	LM105	LM205	LM305	LM305A	LM376
Input Voltage	50V	50V	40V	50V	40V
Input-Output Differential	40V	40V	40V	40V	40V
Power Dissipation (Note 1)	800 mW	800 mW	800 mW	800 mW	400 mW
Operating Temperature Range	−55°C to +125°C	−25°C to +85°C	0°C to +70°C	0°C to +70°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	300°C	300°C	300°C

Electrical Characteristics (Note 2)

PARAMETER	CONDITIONS	LM105			LM205			LM305			LM305A			LM376		
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
Input Voltage Range		8.5		50	8.5		50	8.5		40	8.5		50	9.0		40
Output Voltage Range		4.5		40	4.5		40	4.5		30	4.5		40	5.0		37
Input-Output Voltage Differential		3.0		30	3.0		30	3.0		30	3.0		30	3.0		30
Load Regulation (Note 3)	$R_{SC} = 10\Omega$, $T_A = 25°C$		0.02	0.05		0.02	0.05		0.02	0.05						
	$R_{SC} = 10\Omega$, $T_A = T_{A(MAX)}$		0.03	0.1		0.03	0.1		0.03	0.1						
	$R_{SC} = 10\Omega$, $T_A = T_{A(MIN)}$		0.03	0.1		0.03	0.1		0.03	0.1						
		$0 \leq I_O \leq 12$ mA			$0 \leq I_O \leq 12$ mA			$0 \leq I_O \leq 12$ mA								
	$R_{SC} = 0\Omega$, $T_A = 25°C$											0.02	0.2			0.2
	$R_{SC} = 0\Omega$, $T_A = 70°C$											0.03	0.4			0.5
	$R_{SC} = 0\Omega$, $T_A = 0°C$											0.03	0.4			0.5
											$0 \leq I_O \leq 45$ mA			$0 \leq I_O \leq 25$ mA		
Line Regulation	$T_A = 25°C$															0.03
	$0°C \leq T_A \leq +70°C$															0.1
	$V_{IN} - V_{OUT} \leq 5V$, $T_A = 25°C$		0.025	0.06		0.025	0.06		0.025	0.06		0.025	0.06			
	$V_{IN} - V_{OUT} \geq 5V$, $T_A = 25°C$		0.015	0.03		0.015	0.03		0.015	0.03		0.015	0.03			
Temperature Stability	$T_{A(MIN)} \leq T_A \leq T_{A(MAX)}$		0.3	1.0		0.3	1.0		0.3	1.0		0.3	1.0			
Feedback Sense Voltage		1.63	1.7	1.81	1.63	1.7	1.81	1.63	1.7	1.81	1.55	1.7	1.85	1.60	1.72	1.80
Output Noise Voltage	$10\ Hz \leq f \leq 10\ kHz$															
	$C_{REF} = 0$		0.005			0.005			0.005			0.005				
	$C_{REF} = 0.1\mu F$		0.002			0.002			0.002			0.002				
Standby Current Drain	$V_{IN} = 30V$, $T_A = 25°C$															2.5
	$V_{IN} = 40V$								0.8	2.0						
	$V_{IN} = 50V$		0.8	2.0		0.8	2.0					0.8	2.0			
Current Limit Sense Voltage	$T_A = 25°C$, $R_{SC} = 10\Omega$, $V_{OUT} = 0V$, (Note 4)	225	300	375	225	300	375	225	300	375	225	300	375		300	
Long Term Stability			0.1	1.0		0.1	1.0		0.1	1.0		0.1	1.0			
Ripple Rejection	$C_{REF} = 10\mu F$, f = 120 Hz		0.003	0.01		0.003	0.01		0.003	0.01		0.003				0.1

Note 1: The maximum junction temperature of the LM105 and LM305A is 150°C, the LM205 and LM376 is 100°C, and the LM305 is 85°C. For operation at elevated temperatures, devices in the TC must be derated based on a thermal resistance of 150°C/W junction to ambient, or 45°C/W junction to case. For the epoxy dual-in-line package, derating is based on a thermal resistance of 187°C/W ambient. Peak dissipations to 1W are allowable providing the dissipation rating is not exceeded with the power averaged over a five second interval for the LM105 and LM205, and averaged over a t interval for the LM305.

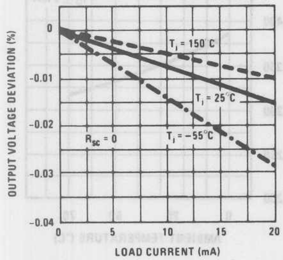
Note 2: Unless otherwise specified, these specifications apply for temperatures within the operating temperature range, for input and output voltages within the range given, and for a divider impedar the feedback terminal of 2 kΩ. Load and line regulation specifications are for a constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operа conditions of high dissipation.

Note 3: The output currents given, as well as the load regulation, can be increased by the addition of external transistors. The improvement factor will be roughly equal to the composite current g added transistors.

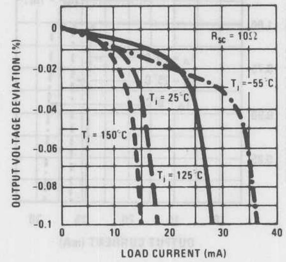
Note 4: With no external pass transistor.

Typical Performance Characteristics LM105/LM205/LM305/LM305A

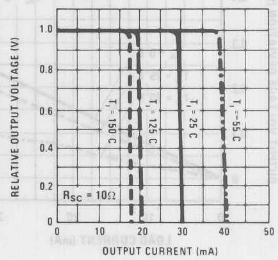
Load Regulation



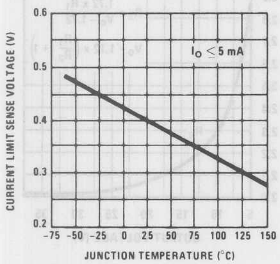
Load Regulation



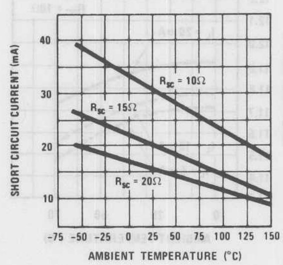
Current Limiting Characteristics



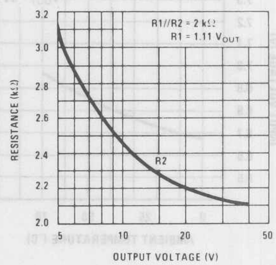
Current Limit Sense Voltage



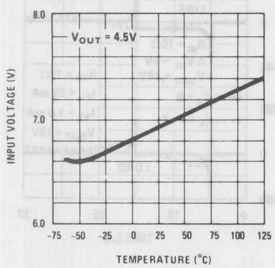
Short Circuit Current



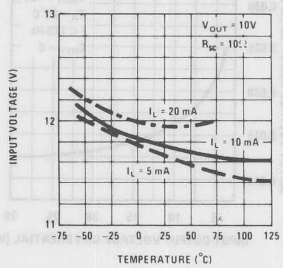
Optimum Divider Resistance Values



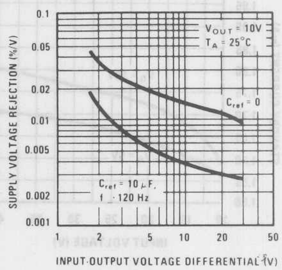
Minimum Input Voltage



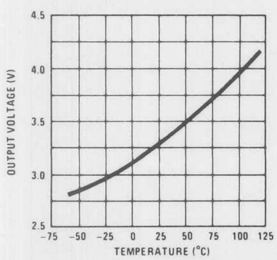
Regulator Dropout Voltage



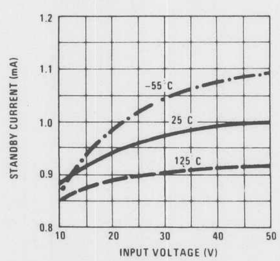
Supply Voltage Rejection



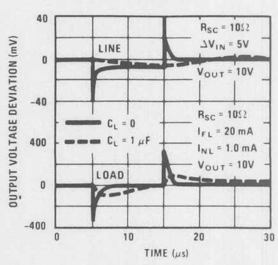
Minimum Output Voltage



Standby Current Drain

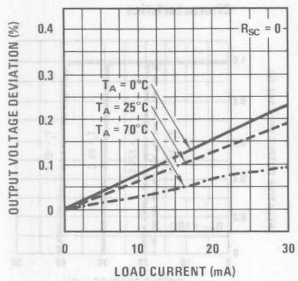


Transient Response

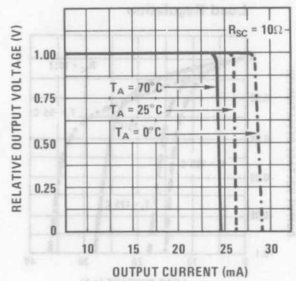


Typical Performance Characteristics LM376

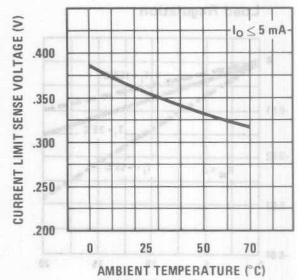
Load Regulation



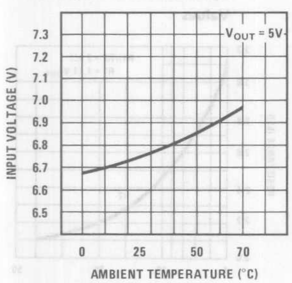
Current Limiting Characteristics



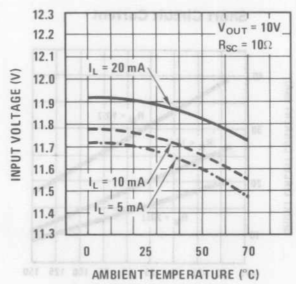
Current Limit Sense Voltage



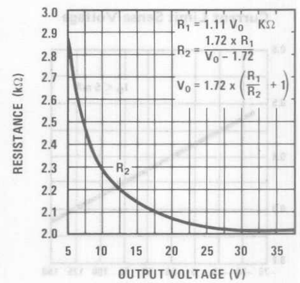
Minimum Input Voltage



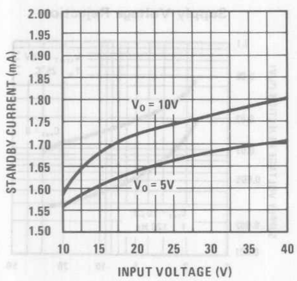
Regulator Dropout Voltage



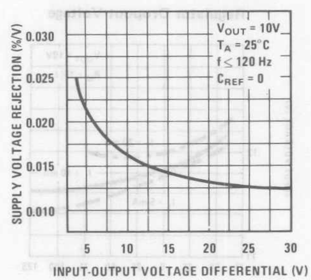
Optimum Divider Resistance



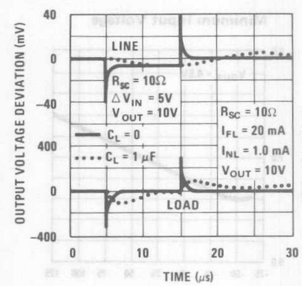
Standby Current Drain
T_A = 25°C



Supply Voltage Rejection

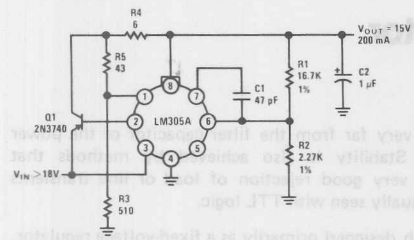


Transient Response

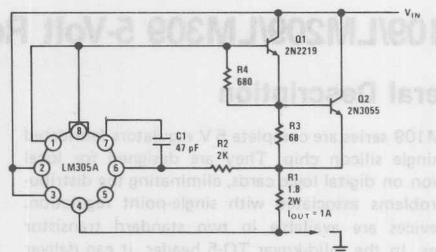


Typical Applications (Continued)

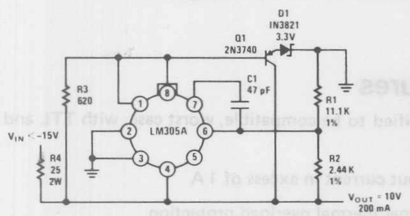
Linear Regulator with Foldback Current Limiting



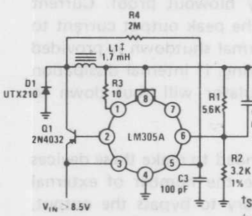
Current Regulator



Shunt Regulator



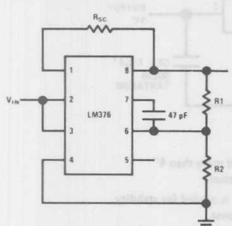
Switching Regulator



†Solid tantalum.

‡125 turns #22 on Arnold Engineering A262123-2 molybdenum permalloy core.

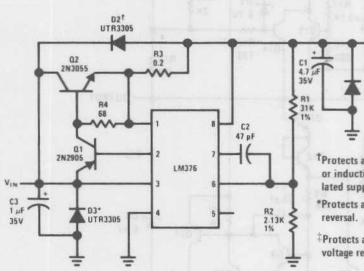
Basic Positive Regulator with Current Limiting



$$V_{OUT} \approx 1.72 \frac{R1 + R2}{R2} \text{ V}$$

$$I_{SC} \approx \frac{325}{R_{SC}} \text{ mA}$$

1.0A Regulator with Protective Diodes

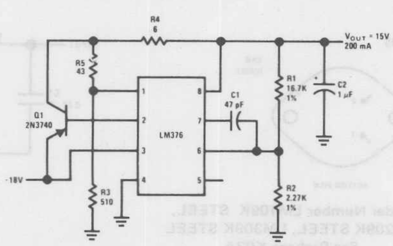


†Protects against shorted input or inductive loads on unregulated supply.

*Protects against input voltage reversal.

‡Protects against output voltage reversal.

Linear Regulator with Foldback Current Limiting



National Semiconductor

LM109/LM209/LM309 5-Volt Regulator

General Description

The LM109 series are complete 5 V regulators fabricated on a single silicon chip. They are designed for local regulation on digital logic cards, eliminating the distribution problems associated with single-point regulation. The devices are available in two standard transistor packages. In the solid-kovar TO-5 header, it can deliver output currents in excess of 200 mA, if adequate heat sinking is provided. With the TO-3 power package, the available output current is greater than 1 A.

The regulators are essentially blowout proof. Current limiting is included to limit the peak output current to a safe value. In addition, thermal shutdown is provided to keep the IC from overheating. If internal dissipation becomes too great, the regulator will shut down to prevent excessive heating.

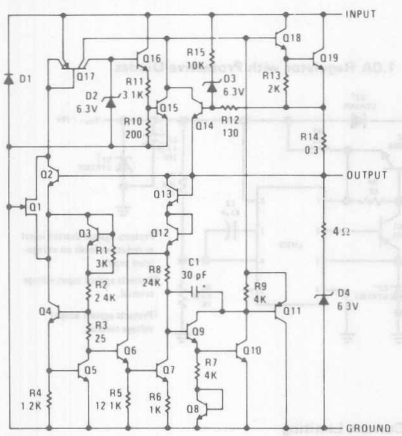
Considerable effort was expended to make these devices easy to use and to minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response somewhat. Input bypassing is needed, however, if the regulator is located very far from the filter capacitor of the power supply. Stability is also achieved by methods that provide very good rejection of load or line transients as are usually seen with TTL logic.

Although designed primarily as a fixed-voltage regulator, the output of the LM109 series can be set to voltages above 5 V, as shown below. It is also possible to use the circuits as the control element in precision regulators, taking advantage of the good current-handling capability and the thermal overload protection.

Features

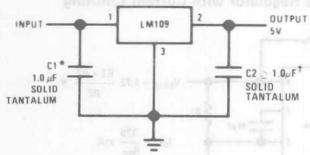
- Specified to be compatible, worst case, with TTL and DTL
- Output current in excess of 1 A
- Internal thermal overload protection
- No external components required

Schematic Diagram



Typical Application

Fixed 5V Regulator



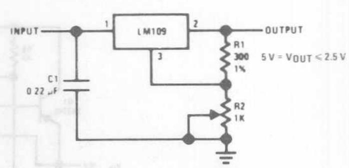
*Required if regulator is located more than 4" from power supply filter capacitor.

†Although no output capacitor is needed for stability, it does improve transient response.

C2 should be used whenever long wires are used to connect to the load, or when transient response is critical.

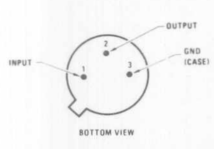
NOTE: Pin 3 electrically connected to case.

Adjustable Output Regulator

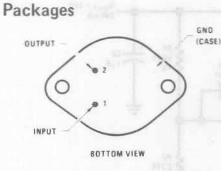


Connection Diagrams

Metal Can Packages



Order Number LM109H, LH209H or LM309H
See Package H03A



Order Number LM109K STEEL, LM209K STEEL, LM309K STEEL
See Package K02A

Order Number LM309K (ALUMINUM)
See Package KC02A

Power Dissipation	Internally Limited
Operating Junction Temperature Range	
LM109	−55°C to +150°C
LM209	−25°C to +150°C
LM309	0°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

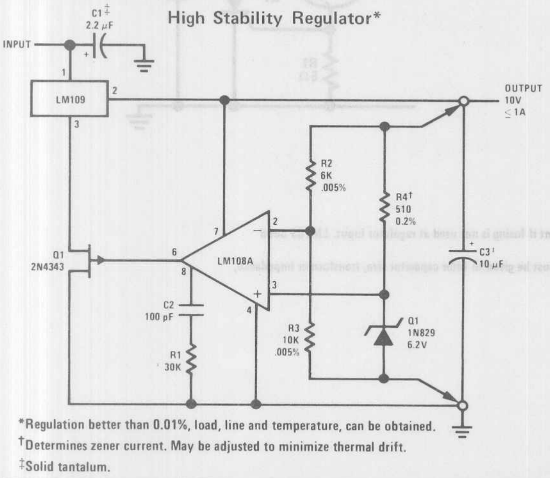
PARAMETER	CONDITIONS	LM109/LM209			LM309			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage	$T_j = 25°C$	4.7	5.05	5.3	4.8	5.05	5.2	V
Line Regulation	$T_j = 25°C$, $7V \leq V_{IN} \leq 25V$		4.0	50		4.0	50	mV
Load Regulation	$T_j = 25°C$							
TO-5 Package	$5mA \leq I_{OUT} \leq 0.5A$		15	50		15	50	mV
TO-3 Package	$5mA \leq I_{OUT} \leq 1.5A$		15	100		15	100	mV
Output Voltage	$7V \leq V_{IN} \leq 25V$, $5mA \leq I_{OUT} \leq I_{MAX}$, $P < P_{MAX}$	4.6		5.4	4.75		5.25	V
Quiescent Current	$7V \leq V_{IN} \leq 25V$		5.2	10		5.2	10	mA
Quiescent Current Change	$7V \leq V_{IN} \leq 25V$			0.5			0.5	mA
	$5mA \leq I_{OUT} \leq I_{MAX}$			0.8			0.8	mA
Output Noise Voltage	$T_A = 25°C$, $10Hz \leq f \leq 100kHz$		40			40		μV
Long Term Stability				10			20	mV
Ripple Rejection	$T_j = 25°C$	50			50			dB
Thermal Resistance, Junction to Case	(Note 2)							
TO-5 Package			15			15		°C/W
TO-3 Package			2.5			2.5		°C/W

Note 1: Unless otherwise specified, these specifications apply $-55°C \leq T_j \leq +150°C$ for the LM109, $-25°C \leq T_j \leq +150°C$ for the LM209, and $0°C \leq T_j \leq +125°C$ for the LM309; $V_{IN} = 10V$; and $I_{OUT} = 0.1A$ for the TO-39 package or $I_{OUT} = 0.5A$ for the TO-3 package. For the TO-39 package, $I_{MAX} = 0.2A$ and $P_{MAX} = 2.0W$. For the TO-3 package, $I_{MAX} = 1.0A$ and $P_{MAX} = 20W$.

Note 2: Without a heat sink, the thermal resistnace of the TO-39 package is about 150°C/W, while that of the TO-3 package is approximately 35°C/W. With a heat sink, the effective thermal resistance can only approach the values specified, depending on the efficiency of the sink.

Typical Applications (cont'd.)

High Stability Regulator*

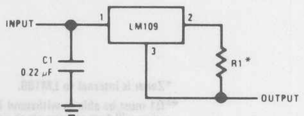


*Regulation better than 0.01%, load, line and temperature, can be obtained.

†Determines zener current. May be adjusted to minimize thermal drift.

‡Solid tantalum.

Current Regulator



*Determines output current. If wirewound resistor is used, bypass with 0.1 μF.

Application Hints

a. **Bypass the input** of the LM109 to ground with $\geqslant 0.2\ \mu F$ ceramic or solid tantalum capacitor if main filter capacitor is more than 4 inches away.

b. **Use steel package** instead of aluminum if more than 5,000 thermal cycles are expected. ($\Delta T \geqslant 50°C$)

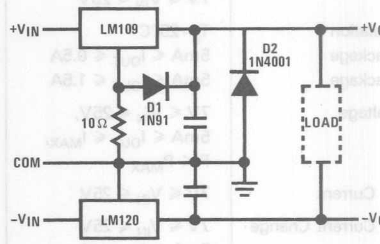
c. **Avoid insertion of regulator into "live" socket** if input voltage is greater than 10 V. The output will rise to within 2 V of the unregulated input if the ground pin does not make contact, possibly damaging the load. The LM109 may also be damaged if a large output capacitor is charged up, then discharged through the internal clamp zener when the ground pin makes contact.

d. **The output clamp zener** is designed to absorb transients only. It will not clamp the output effectively if a failure occurs in the internal power transistor structure. Zener dynamic impedance is $\approx 4\ \Omega$. Continuous RMS current into the zener should not exceed 0.5 A.

e. **Paralleling of LM109s** for higher output current is not recommended. Current sharing will be almost nonexistent, leading to a current limit mode operation for devices with the highest initial output voltage. The current limit devices may also heat up to the thermal shutdown point ($\approx$ 175°C). Long term reliability cannot be guaranteed under these conditions.

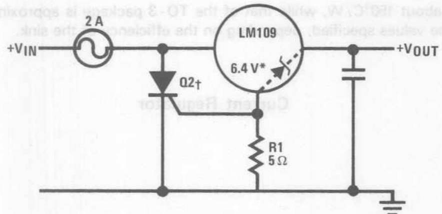
f. **Preventing latchoff** for loads connected to negative voltage:

If the output of the LM109 is pulled negative by a high current supply so that the output pin is more than 0.5 V negative with respect to the ground pin, the LM109 can latch off. This can be prevented by clamping the ground pin to the output pin with a germanium or Schottky diode as shown. A silicon diode (1N4001) at the output is also needed to keep the positive output from being pulled too far negative. The 10Ω resistor will raise $+V_{OUT}$ by ≈ 0.05 V.

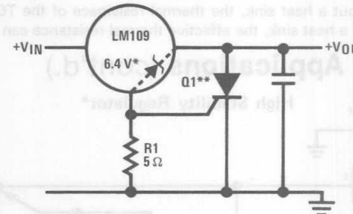


Crowbar Overvoltage Protection

INPUT CROWBAR



OUTPUT CROWBAR



*Zener is internal to LM109.

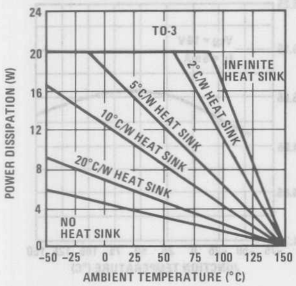
**Q1 must be able to withstand 7 A continuous current if fusing is not used at regulator input. LM109 bond wires will fuse at currents above 7 A.

†Q2 is selected for surge capability. Consideration must be given to filter capacitor size, transformer impedance, and fuse blowing time.

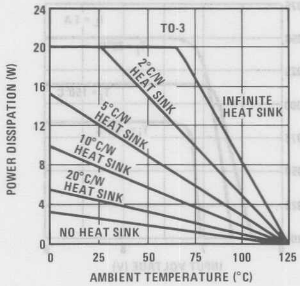
††Trip point is $\approx$ 7.5 V.

Typical Performance Characteristics

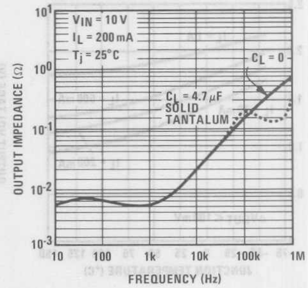
MAXIMUM AVERAGE POWER DISSIPATION (LM109K)



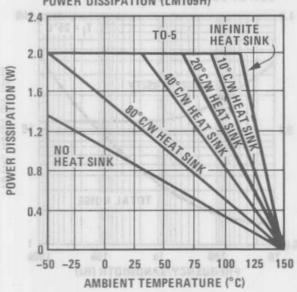
MAXIMUM AVERAGE POWER DISSIPATION (LM309K)



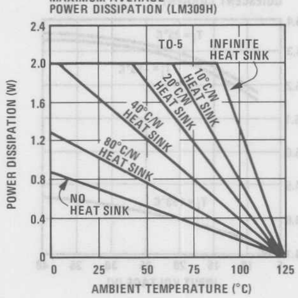
OUTPUT IMPEDANCE



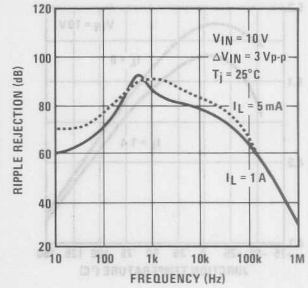
MAXIMUM AVERAGE POWER DISSIPATION (LM109H)



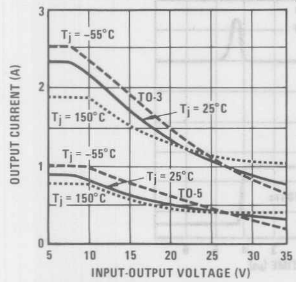
MAXIMUM AVERAGE POWER DISSIPATION (LM309H)



RIPPLE REJECTION

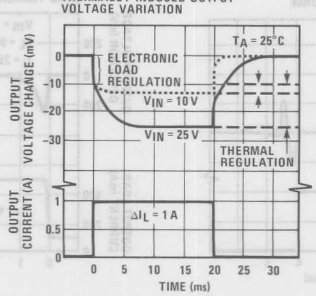


CURRENT LIMIT CHARACTERISTICS (NOTE 1)

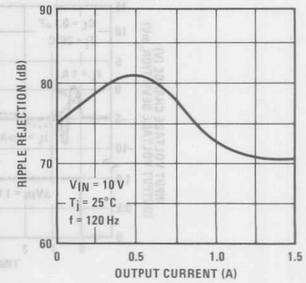


Note 1: Current limiting foldback characteristics are determined by input-output differential, not by output voltage.

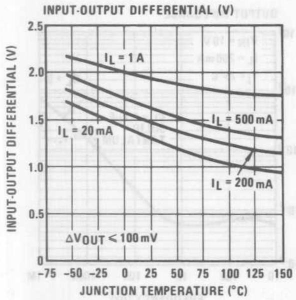
THERMALLY INDUCED OUTPUT VOLTAGE VARIATION

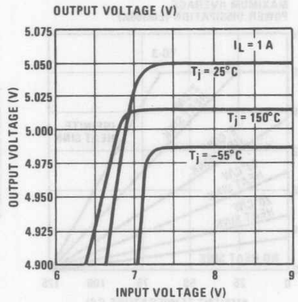


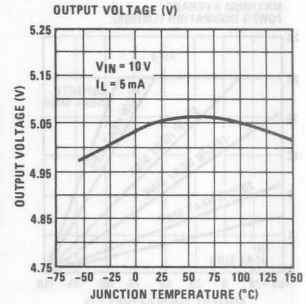
RIPPLE REJECTION

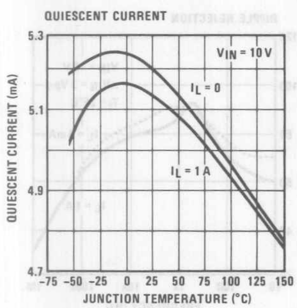


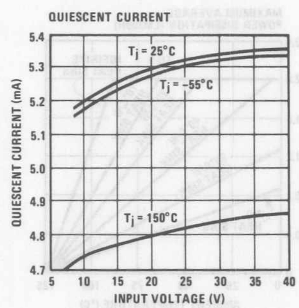
Typical Performance Characteristics (cont'd)

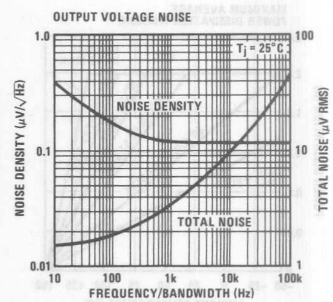


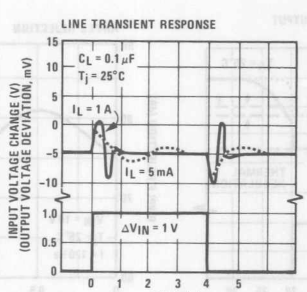


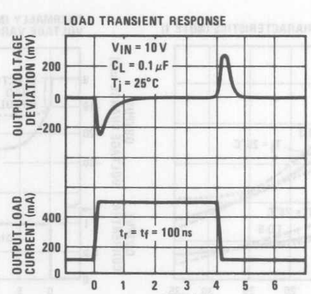












National Semiconductor

Voltage Regulators

LM117/LM217/LM317 3-Terminal Adjustable Regulator

General Description

The LM117/LM217/LM317 are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 1.5A over a 1.2V to 37V output range. They are exceptionally easy to use and require only two external resistors to set the output voltage. Further, both line and load regulation are better than standard fixed regulators. Also, the LM117 is packaged in standard transistor packages which are easily mounted and handled.

In addition to higher performance than fixed regulators, the LM117 series offers full overload protection available only in IC's. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

Features

- Adjustable output down to 1.2V
- Guaranteed 1.5A output current
- Line regulation typically 0.01%/V
- Load regulation typically 0.1%
- Current limit constant with temperature
- **100% electrical burn-in**
- Eliminates the need to stock many voltages
- Standard 3-lead transistor package
- 80 dB ripple rejection

Normally, no capacitors are needed unless the device is situated far from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejections ratios which are difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators, the LM117 is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input to output differential is not exceeded.

Also, it makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM117 can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2V where most loads draw little current.

The LM117K, LM217K and LM317K are packaged in standard TO-3 transistor packages while the LM117H, LM217H and LM317H are packaged in a solid Kovar base TO-39 transistor package. The LM117 is rated for operation from −55°C to +150°C, the LM217 from −25°C to +150°C and the LM317 from 0°C to +125°C. The LM317T and LM317MP, rated for operation over a 0°C to +125°C range, are available in a TO-220 plastic package and a TO-202 package, respectively.

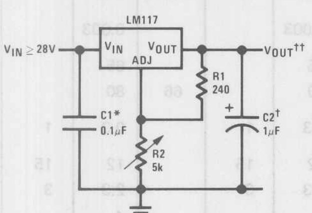
For applications requiring greater output current in excess of 3A and 5A, see LM150 series and LM138 series data sheets, respectively. For the negative complement, see LM137 series data sheet.

LM117 Series Packages and Power Capability

DEVICE	PACKAGE	RATED POWER DISSIPATION	DESIGN LOAD CURRENT
LM117 LM217 LM317	TO-3	20W	1.5A
	TO-39	2W	0.5A
LM317T	TO-220	15W	1.5A
LM317M	TO-202	7.5W	0.5A
LM317LZ	TO-92	0.6W	0.1A

Typical Applications

1.2V–25V Adjustable Regulator

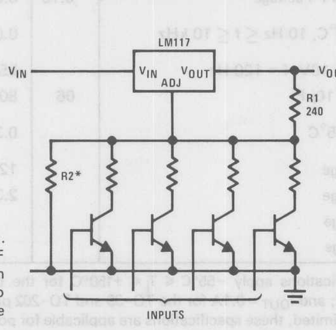


†Optional—improves transient response. Output capacitors in the range of 1 μF to 1000 μF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients.

*Needed if device is far from filter capacitors.

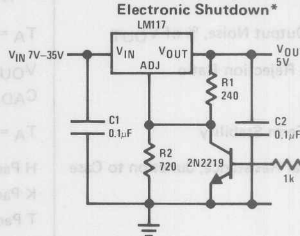
$$^{\dagger\dagger}V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right)$$

Digitally Selected Outputs



*Sets maximum V_{OUT}

5V Logic Regulator with Electronic Shutdown*



*Min output ≈ 1.2V

	−55°C to +150°C
LM217	−25°C to +150°C
LM317	0°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Preconditioning

Burn-In in Thermal Limit **100% All Devices**

Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	LM117/217 MIN	LM117/217 TYP	LM117/217 MAX	LM317 MIN	LM317 TYP	LM317 MAX	UNITS
Line Regulation	$T_A = 25°C$, $3V \leq V_{IN} - V_{OUT} \leq 40V$ (Note 2)		0.01	0.02		0.01	0.04	%/V
Load Regulation	$T_A = 25°C$, $10\ mA \leq I_{OUT} \leq I_{MAX}$							
	$V_{OUT} \leq 5V$, (Note 2)		5	15		5	25	mV
	$V_{OUT} \geq 5V$, (Note 2)		0.1	0.3		0.1	0.5	%
Thermal Regulation	$T_A = 25°C$, 20 ms Pulse		0.03	0.07		0.04	0.07	%/W
Adjustment Pin Current			50	100		50	100	μA
Adjustment Pin Current Change	$10\ mA \leq I_L \leq I_{MAX}$ $3V \leq (V_{IN} - V_{OUT}) \leq 40V$		0.2	5		0.2	5	μA
Reference Voltage	$3V \leq (V_{IN} - V_{OUT}) \leq 40V$, (Note 3) $10\ mA \leq I_{OUT} \leq I_{MAX}$, $P \leq P_{MAX}$	1.20	1.25	1.30	1.20	1.25	1.30	V
Line Regulation	$3V \leq V_{IN} - V_{OUT} \leq 40V$, (Note 2)		0.02	0.05		0.02	0.07	%/V
Load Regulation	$10\ mA \leq I_{OUT} \leq I_{MAX}$, (Note 2)							
	$V_{OUT} \leq 5V$		20	50		20	70	mV
	$V_{OUT} \geq 5V$		0.3	1		0.3	1.5	%
Temperature Stability	$T_{MIN} \leq T_j \leq T_{MAX}$		1			1		%
Minimum Load Current	$V_{IN} - V_{OUT} = 40V$		3.5	5		3.5	10	mA
Current Limit	$V_{IN} - V_{OUT} \leq 15V$							
	K and T Package	1.5	2.2		1.5	2.2		A
	H and P Package	0.5	0.8		0.5	0.8		A
	$V_{IN} - V_{OUT} = 40V$, $T_j = +25°C$							
	K and T Package	0.30	0.4		0.15	0.4		A
	H and P Package	0.15	0.07		0.075	0.07		A
RMS Output Noise, % of V_{OUT}	$T_A = 25°C$, $10\ Hz \leq f \leq 10\ kHz$		0.003			0.003		%
Ripple Rejection Ratio	$V_{OUT} = 10V$, f = 120 Hz		65			65		dB
	$C_{ADJ} = 10\mu F$	66	80		66	80		dB
Long-Term Stability	$T_A = 125°C$		0.3	1		0.3	1	%
Thermal Resistance, Junction to Case	H Package		12	15		12	15	°C/W
	K Package		2.3	3		2.3	3	°C/W
	T Package					4		°C/W
	P Package					12		°C/W

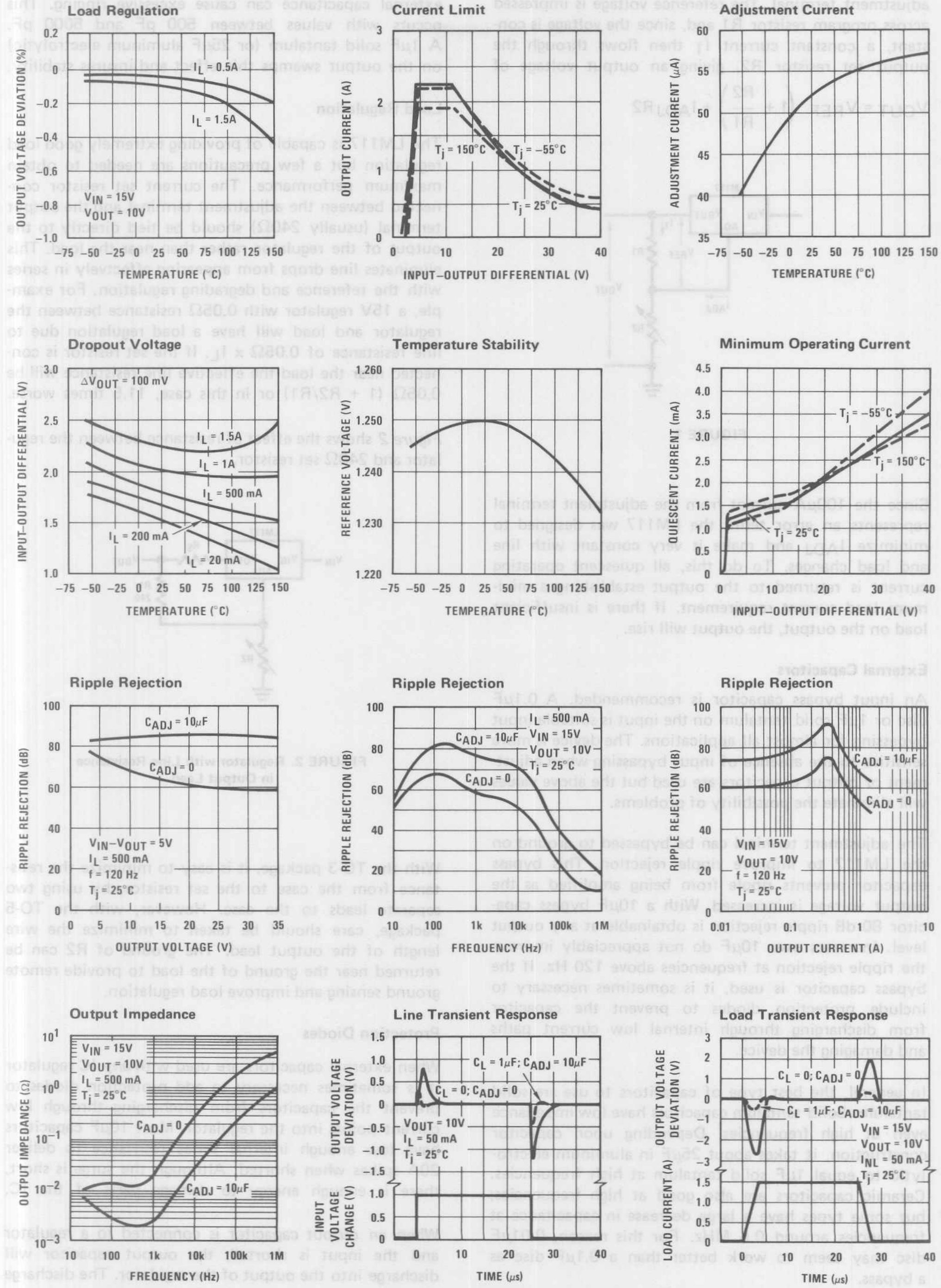
Note 1: Unless otherwise specified, these specifications apply $-55°C \leq T_j \leq +150°C$ for the LM117, $-25°C \leq T_j \leq +150°C$ for the LM217, and $0°C \leq T_j \leq +125°C$ for the LM317; $V_{IN} - V_{OUT} = 5V$; and $I_{OUT} = 0.1A$ for the TO-39 and TO-202 packages and $I_{OUT} = 0.5A$ for the TO-3 and TO-220 packages. Although power dissipation is internally limited, these specifications are applicable for power dissipations of 2W for the TO-39 and TO-202, and 20W for the TO-3 and TO-220. I_{MAX} is 1.5A for the TO-3 and TO-220 packages and 0.5A for the TO-39 and TO-202 packages.

Note 2: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.

Note 3: Selected devices with tightened tolerance reference voltage available.

Typical Performance Characteristics (K and T Packages)

Output Capacitor = 0 unless otherwise noted



Application Hints

In operation, the LM117 develops a nominal 1.25V reference voltage, V_{REF}, between the output and adjustment terminal. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R2, giving an output voltage of

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}R2$$

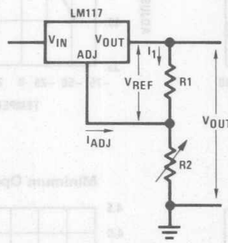


FIGURE 1.

Since the 100μA current from the adjustment terminal represents an error term, the LM117 was designed to minimize I_{ADJ} and make it very constant with line and load changes. To do this, all quiescent operating current is returned to the output establishing a minimum load current requirement. If there is insufficient load on the output, the output will rise.

External Capacitors

An input bypass capacitor is recommended. A 0.1μF disc or 1μF solid tantalum on the input is suitable input bypassing for almost all applications. The device is more sensitive to the absence of input bypassing when adjustment or output capacitors are used but the above values will eliminate the possibility of problems.

The adjustment terminal can be bypassed to ground on the LM117 to improve ripple rejection. This bypass capacitor prevents ripple from being amplified as the output voltage is increased. With a 10μF bypass capacitor 80 dB ripple rejection is obtainable at any output level. Increases over 10μF do not appreciably improve the ripple rejection at frequencies above 120 Hz. If the bypass capacitor is used, it is sometimes necessary to include protection diodes to prevent the capacitor from discharging through internal low current paths and damaging the device.

In general, the best type of capacitors to use are solid tantalum. Solid tantalum capacitors have low impedance even at high frequencies. Depending upon capacitor construction, it takes about 25μF in aluminum electrolytic to equal 1μF solid tantalum at high frequencies. Ceramic capacitors are also good at high frequencies; but some types have a large decrease in capacitance at frequencies around 0.5 MHz. For this reason, 0.01μF disc may seem to work better than a 0.1μF disc as a bypass.

Although the LM117 is stable with no output capacitors, like any feedback circuit, certain values of external capacitance can cause excessive ringing. This occurs with values between 500 pF and 5000 pF. A 1μF solid tantalum (or 25μF aluminum electrolytic) on the output swamps this effect and insures stability.

Load Regulation

The LM117 is capable of providing extremely good load regulation but a few precautions are needed to obtain maximum performance. The current set resistor connected between the adjustment terminal and the output terminal (usually 240Ω) should be tied directly to the output of the regulator rather than near the load. This eliminates line drops from appearing effectvely in series with the reference and degrading regulation. For example, a 15V regulator with 0.05Ω resistance between the regulator and load will have a load regulation due to line resistance of $0.05\Omega \times I_L$. If the set resistor is connected near the load the effective line resistance will be $0.05\Omega\ (1 + R2/R1)$ or in this case, 11.5 times worse.

Figure 2 shows the effect of resistance between the regulator and 240Ω set resistor.

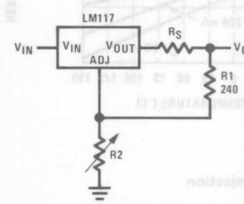


FIGURE 2. Regulator with Line Resistance in Output Lead

With the TO-3 package, it is easy to minimize the resistance from the case to the set resistor, by using two separate leads to the case. However, with the TO-5 package, care should be taken to minimize the wire length of the output lead. The ground of R2 can be returned near the ground of the load to provide remote ground sensing and improve load regulation.

Protection Diodes

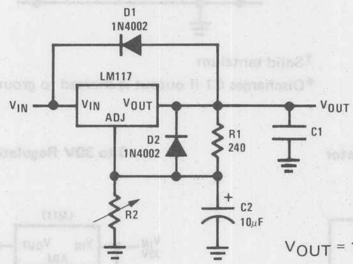
When external capacitors are used with *any* IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator. Most 10μF capacitors have low enough internal series resistance to deliver 20A spikes when shorted. Although the surge is short, there is enough energy to damage parts of the IC.

When an output capacitor is connected to a regulator and the input is shorted, the output capacitor will discharge into the output of the regulator. The discharge

Application Hints (cont'd.)

current depends on the value of the capacitor, the output voltage of the regulator, and the rate of decrease of V_{IN}. In the LM117, this discharge path is through a large junction that is able to sustain 15A surge with no problem. This is not true of other types of positive regulators. For output capacitors of 25μF or less, there is no need to use diodes.

The bypass capacitor on the adjustment terminal can discharge through a low current junction. Discharge occurs when *either* the input or output is shorted. Internal to the LM117 is a 50Ω resistor which limits the peak discharge current. No protection is needed for output voltages of 25V or less and 10μF capacitance. *Figure 3* shows an LM117 with protection diodes included for use with outputs greater than 25V and high values of output capacitance.



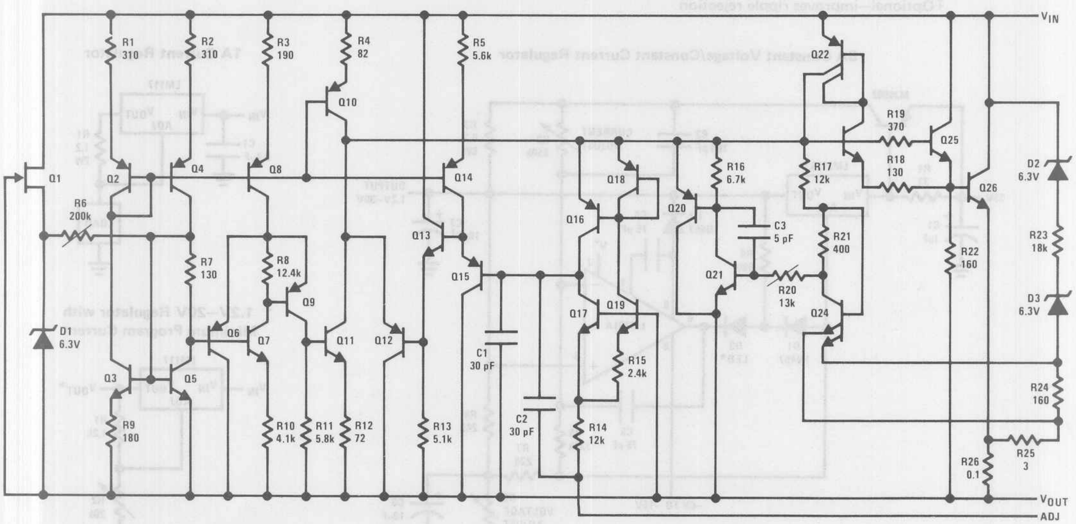
$$V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right) + R2I_{ADJ}$$

D1 protects against C1

D2 protects against C2

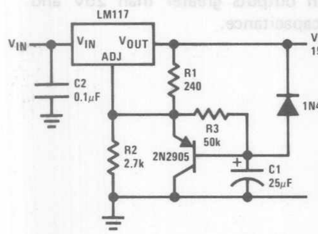
FIGURE 3. Regulator with Protection Diodes

Schematic Diagram

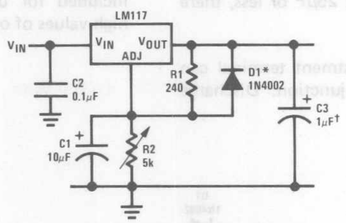


Typical Applications (cont'd.)

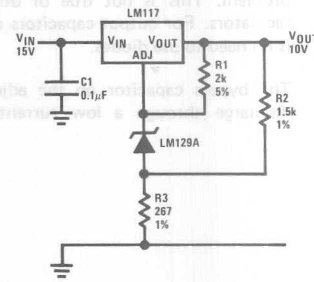
Slow Turn-On 15V Regulator



Adjustable Regulator with Improved Ripple Rejection



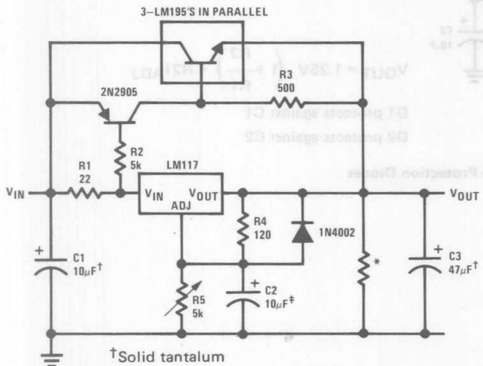
High Stability 10V Regulator



†Solid tantalum

*Discharges C1 if output is shorted to ground

High Current Adjustable Regulator

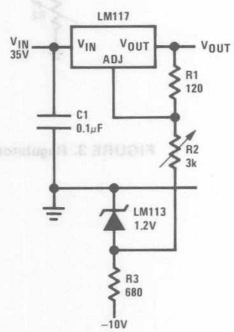


†Solid tantalum

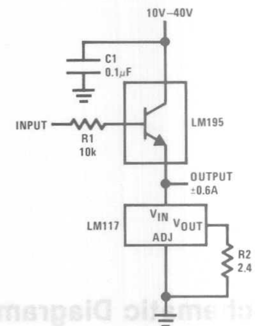
*Minimum load current = 30 mA

‡Optional—improves ripple rejection

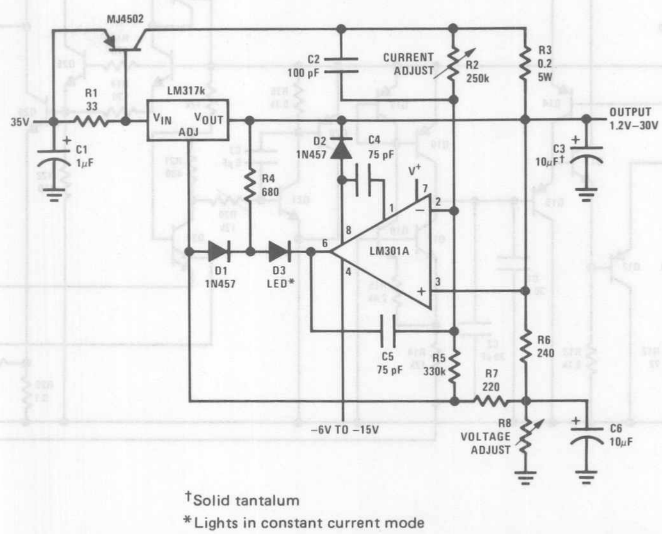
0 to 30V Regulator



Power Follower



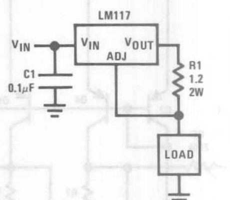
5A Constant Voltage/Constant Current Regulator



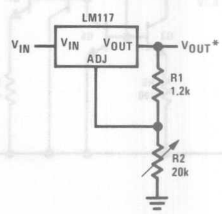
†Solid tantalum

*Lights in constant current mode

1A Current Regulator



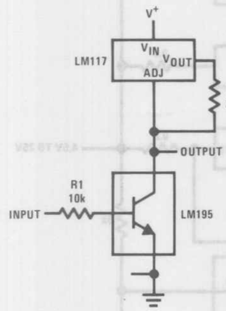
1.2V–20V Regulator with Minimum Program Current



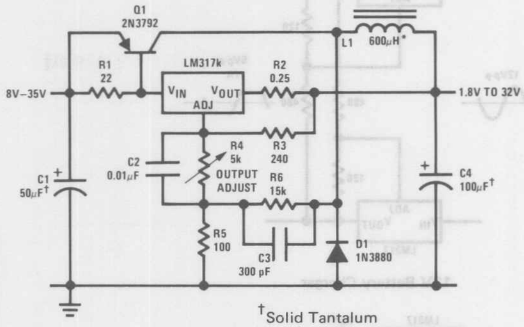
*Minimum load current ≈ 4 mA

Typical Applications (cont'd.)

High Gain Amplifier



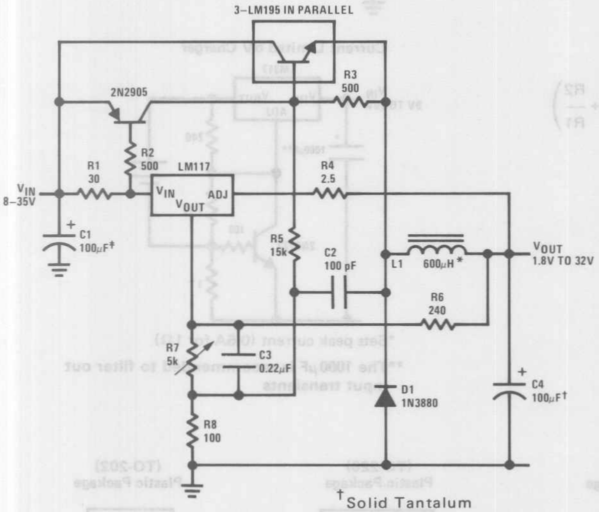
Low Cost 3A Switching Regulator



†Solid Tantalum

*Core—Arnold A-254168-2 60 turns

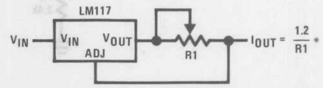
4A Switching Regulator with Overload Protection



†Solid Tantalum

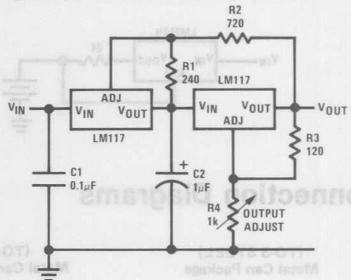
*Core Arnold A-254168-2 60 turns

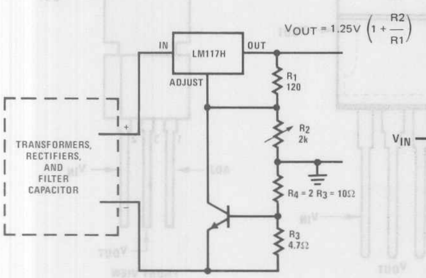
Precision Current Limiter



$*0.8\Omega \leq R1 \leq 120\Omega$

Tracking Preregulator



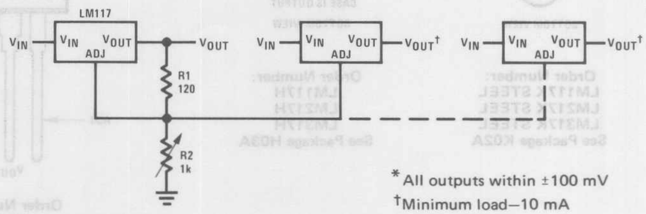


— Short circuit current is approximately $\frac{600\text{mV}}{R_3}$, or 120mA

(compared to LM117H's 1 ampere current limit)

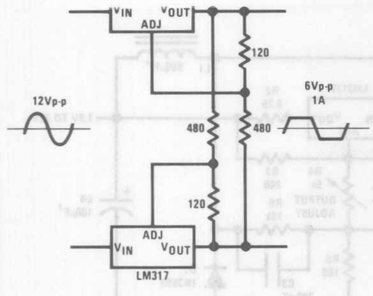
— (At 50mA output only ¾ volt of drop occurs in R_3 and R_4).

Adjusting Multiple On-Card Regulators with Single Control*

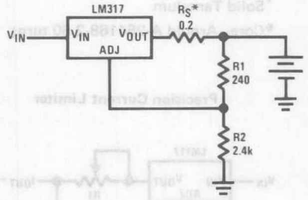


*All outputs within ±100 mV

†Minimum load—10 mA

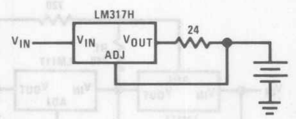


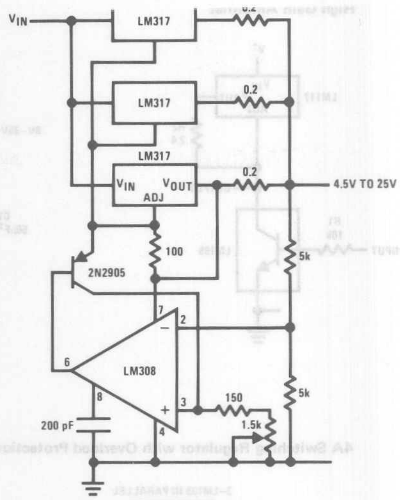
12V Battery Charger



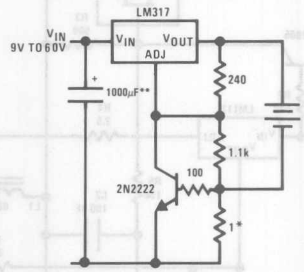
*R_S—sets output impedance of charger $Z_{OUT} = R_S\left(1+\frac{R2}{R1}\right)$
Use of R_S allows low charging rates with fully charged battery.

50 mA Constant Current Battery Charger





Current Limited 6V Charger

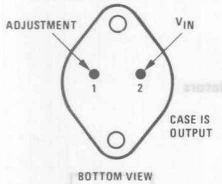


*Sets peak current (0.6A for 1Ω)

**The 1000 μF is recommended to filter out input transients

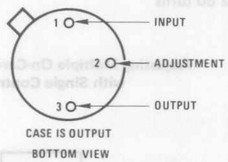
Connection Diagrams

(TO-3 STEEL)
Metal Can Package



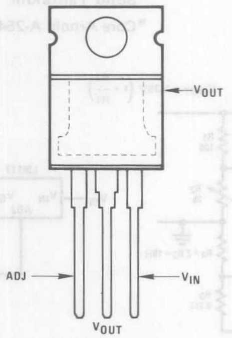
Order Number:
LM117K STEEL
LM217K STEEL
LM317K STEEL
See Package K02A

(TO-39)
Metal Can Package



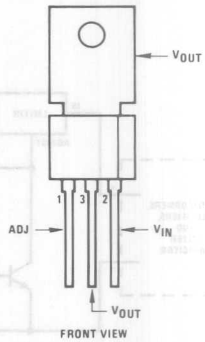
Order Number:
LM117H
LM217H
LM317H
See Package H03A

(TO-220)
Plastic Package



Order Number:
LM317T
See Package T03B

(TO-202)
Plastic Package



Order Number:
LM317MP
See Package P03A
Tab Formed Devices
LM317MP TB
See Package P03E

National Semiconductor

Voltage Regulators

LM117HV/LM217HV/LM317HV

1

LM117HV/LM217HV/LM317HV 3-Terminal Adjustable Regulator

General Description

The LM117HV/LM217HV/LM317HV are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 1.5A over a 1.2V to 57V output range. They are exceptionally easy to use and require only two external resistors to set the output voltage. Further, both line and load regulation are better than standard fixed regulators. Also, the LM117HV is packaged in standard transistor packages which are easily mounted and handled.

In addition to higher performance than fixed regulators, the LM117HV series offers full overload protection available only in IC's. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

Normally, no capacitors are needed unless the device is situated far from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejections ratios which are difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators, the LM117HV is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input to output differential is not exceeded.

Also, it makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM117HV can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2V where most loads draw little current.

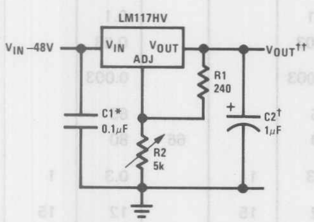
The LM117HVK STEEL, LM217HVK STEEL, and LM317HVK STEEL are packaged in standard TO-3 transistor packages while the LM117HVH, LM217HVH and LM317HVH are packaged in a solid Kovar base TO-39 transistor package. The LM117HV is rated for operation from −55°C to +150°C, the LM217HV from −25°C to +150°C and the LM317HV from 0°C to +125°C.

Features

- Adjustable output down to 1.2V
- Guaranteed 1.5A output current
- Line regulation typically 0.01%/V
- Load regulation typically 0.1%
- Current limit constant with temperature
- **100% electrical burn-in**
- Eliminates the need to stock many voltages
- Standard 3-lead transistor package
- 80 dB ripple rejection

Typical Applications

1.2V–45V Adjustable Regulator

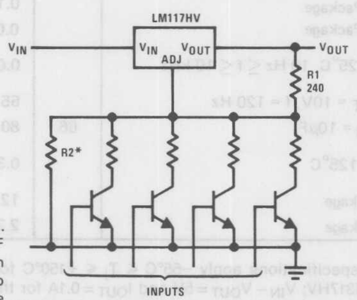


†Optional—improves transient response. Output capacitors in the range of 1 µF to 1000 µF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients.

*Needed if device is far from filter capacitors.

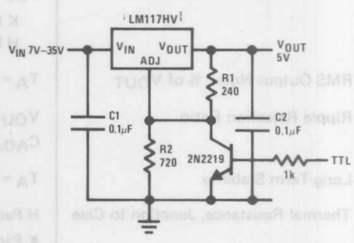
$$^{\dagger\dagger}V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right)$$

Digitally Selected Outputs



*Sets maximum V_{OUT}

5V Logic Regulator with Electronic Shutdown*



*Min output ≈ 1.2V

Absolute Maximum Ratings

Power Dissipation	Internally limited
Input–Output Voltage Differential	60V
Operating Junction Temperature Range	
LM117HV	−55°C to +150°C
LM217HV	−25°C to +150°C
LM317HV	0°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	LM117HV/LM217HV			LM317HV			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Line Regulation	$T_A = 25°C$, $3V \leq V_{IN} - V_{OUT} \leq 60V$ (Note 2)		0.01	0.02		0.01	0.04	%/V
Load Regulation	$T_A = 25°C$, $10\ mA \leq I_{OUT} \leq I_{MAX}$							
	$V_{OUT} \leq 5V$, (Note 2)		5	15		5	25	mV
	$V_{OUT} \geq 5V$, (Note 2)		0.1	0.3		0.1	0.5	%
Thermal Regulation	$T_A = 25°C$, 20ms Pulse		0.03	0.07		0.04	0.07	%/W
Adjustment Pin Current			50	100		50	100	μA
Adjustment Pin Current Change	$10\ mA \leq I_L \leq I_{MAX}$, $3.0V \leq (V_{IN} - V_{OUT}) \leq 60V$		0.2	5		0.2	5	μA
Reference Voltage	$3 \leq (V_{IN} - V_{OUT}) \leq 60V$, (Note 3) $10\ mA \leq I_{OUT} \leq I_{MAX}$, $P \leq P_{MAX}$	1.20	1.25	1.30	1.20	1.25	1.30	V
Line Regulation	$3V \leq V_{IN} - V_{OUT} \leq 60V$, (Note 2)		0.02	0.05		0.02	0.07	%/V
Load Regulation	$10\ mA \leq I_{OUT} \leq I_{MAX}$, (Note 2)							
	$V_{OUT} \leq 5V$		20	50		20	70	mV
	$V_{OUT} \geq 5V$		0.3	1		0.3	1.5	%
Temperature Stability	$T_{MIN} \leq T_j \leq T_{MAX}$		1			1		%
Minimum Load Current	$V_{IN} - V_{OUT} = 60V$		3.5	7		3.5	12	mA
Current Limit	$V_{IN} - V_{OUT} \leq 15V$							
	K Package	1.5	2.2		1.5	2.2		A
	H Package	0.5	0.8		0.5	0.8		A
	$V_{IN} - V_{OUT} = 60V$							
	K Package		0.1			0.1		A
	H Package		0.03			0.03		A
RMS Output Noise, % of V_{OUT}	$T_A = 25°C$, $10\ Hz \leq f \leq 10\ kHz$		0.003			0.003		%
Ripple Rejection Ratio	$V_{OUT} = 10V$, f = 120 Hz		65			65		dB
	$C_{ADJ} = 10\mu F$	66	80		66	80		dB
Long-Term Stability	$T_A = 125°C$		0.3	1		0.3	1	%
Thermal Resistance, Junction to Case	H Package		12	15		12	15	°C/W
	K Package		2.3	3		2.3	3	°C/W

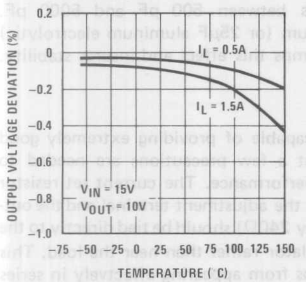
Note 1: Unless otherwise specified, these specifications apply −55°C ≤ T_j ≤ +150°C for the LM117HV, −25°C ≤ T_j ≤ +150°C for the LM217HV and 0°C ≤ T_j ≤ +125°C for the LM317HV; $V_{IN} - V_{OUT} = 5V$ and $I_{OUT} = 0.1A$ for the TO-39 package and $I_{OUT} = 0.5A$ for the TO-3 package. Although power dissipation is internally limited, these specifications are applicable for power dissipations of 2W for the TO-39 and 20W for the TO-3. I_{MAX} is 1.5A for the TO-3 and 0.5A for the TO-39 package.

Note 2: Regulation is measured at constant junction temperature. Changes in output voltage due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

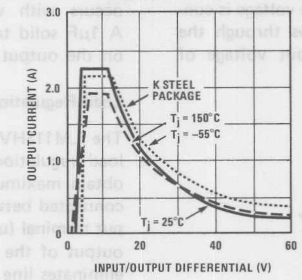
Note 3: Selected devices with tightened tolerance reference voltage available.

Typical Performance Characteristics (K and T Packages)

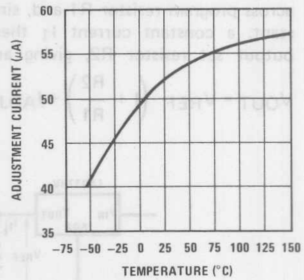
Load Regulation



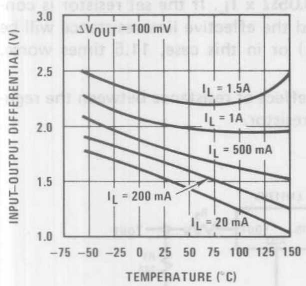
Current Limit



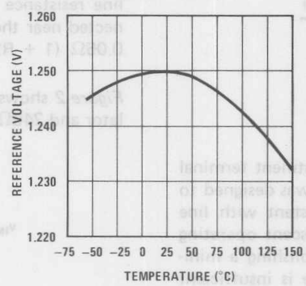
Adjustment Current



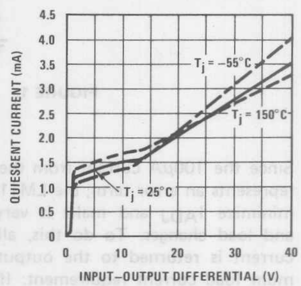
Dropout Voltage



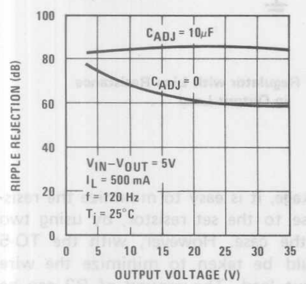
Temperature Stability



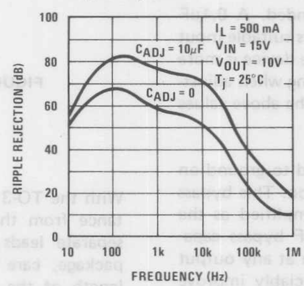
Minimum Operating Current



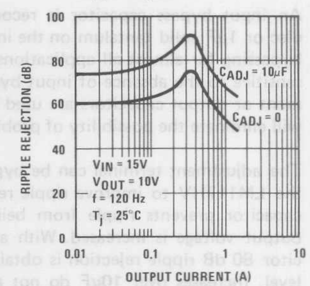
Ripple Rejection



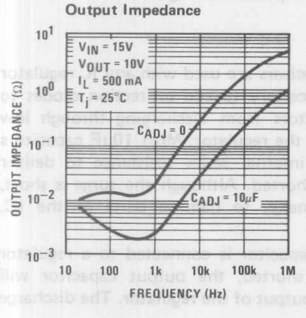
Ripple Rejection



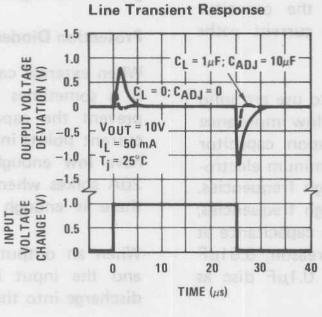
Ripple Rejection



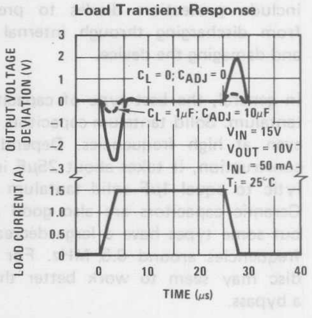
Output Impedance



Line Transient Response



Load Transient Response



In operation, the LM117HV develops a nominal 1.25V reference voltage, V_{REF}, between the output and adjustment terminal. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R2, giving an output voltage of

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}R2$$

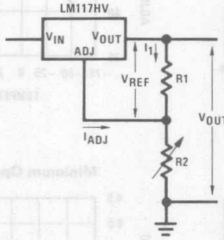


FIGURE 1.

Since the 100μA current from the adjustment terminal represents an error term, the LM117HV was designed to minimize I_{ADJ} and make it very constant with line and load changes. To do this, all quiescent operating current is returned to the output establishing a minimum load current requirement. If there is insufficient load on the output, the output will rise.

External Capacitors

An input bypass capacitor is recommended. A 0.1μF disc or 1μF solid tantalum on the input is suitable input bypassing for almost all applications. The device is more sensitive to the absence of input bypassing when adjustment or output capacitors are used but the above values will eliminate the possibility of problems.

The adjustment terminal can be bypassed to ground on the LM117HV to improve ripple rejection. This bypass capacitor prevents ripple from being amplified as the output voltage is increased. With a 10μF bypass capacitor 80 dB ripple rejection is obtainable at any output level. Increases over 10μF do not appreciably improve the ripple rejection at frequencies above 120 Hz. If the bypass capacitor is used, it is sometimes necessary to include protection diodes to prevent the capacitor from discharging through internal low current paths and damaging the device.

In general, the best type of capacitors to use are solid tantalum. Solid tantalum capacitors have low impedance even at high frequencies. Depending upon capacitor construction, it takes about 25μF in aluminum electrolytic to equal 1μF solid tantalum at high frequencies. Ceramic capacitors are also good at high frequencies; but some types have a large decrease in capacitance at frequencies around 0.5 MHz. For this reason, 0.01μF disc may seem to work better than a 0.1μF disc as a bypass.

Although the LM117HV is stable with no output capacitors, like any feedback circuit, certain values of external capacitance can cause excessive ringing. This occurs with values between 500 pF and 5000 pF. A 1μF solid tantalum (or 25μF aluminum electrolytic) on the output swamps this effect and insures stability.

Load Regulation

The LM117HV is capable of providing extremely good load regulation but a few precautions are needed to obtain maximum performance. The current set resistor connected between the adjustment terminal and the output terminal (usually 240Ω) should be tied directly to the output of the regulator rather than near the load. This eliminates line drops from appearing effectvely in series with the reference and degrading regulation. For example, a 15V regulator with 0.05Ω resistance between the regulator and load will have a load regulation due to line resistance of 0.05Ω x I_L. If the set resistor is connected near the load the effective line resistance will be 0.05Ω (1 + R2/R1) or in this case, 11.5 times worse.

Figure 2 shows the effect of resistance between the regulator and 240Ω set resistor.

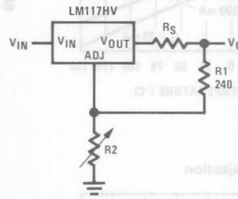


FIGURE 2. Regulator with Line Resistance in Output Lead

With the TO-3 package, it is easy to minimize the resistance from the case to the set resistor, by using two separate leads to the case. However, with the TO-5 package, care should be taken to minimize the wire length of the output lead. The ground of R2 can be returned near the ground of the load to provide remote ground sensing and improve load regulation.

Protection Diodes

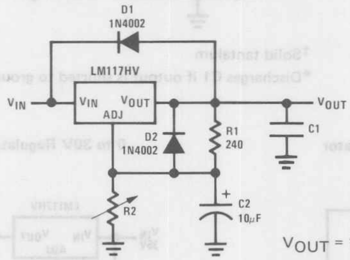
When external capacitors are used with *any* IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator. Most 10μF capacitors have low enough internal series resistance to deliver 20A spikes when shorted. Although the surge is short, there is enough energy to damage parts of the IC.

When an output capacitor is connected to a regulator and the input is shorted, the output capacitor will discharge into the output of the regulator. The discharge

Application Hints (cont'd.)

current depends on the value of the capacitor, the output voltage of the regulator, and the rate of decrease of V_{IN}. In the LM117HV, this discharge path is through a large junction that is able to sustain 15A surge with no problem. This is not true of other types of positive regulators. For output capacitors of 25µF or less, there is no need to use diodes.

The bypass capacitor on the adjustment terminal can discharge through a low current junction. Discharge occurs when *either* the input or output is shorted. Internal to the LM117HV is a 50Ω resistor which limits the peak discharge current. No protection is needed for output voltages of 25V or less and 10µF capacitance. *Figure 3* shows an LM117HV with protection diodes included for use with outputs greater than 25V and high values of output capacitance.



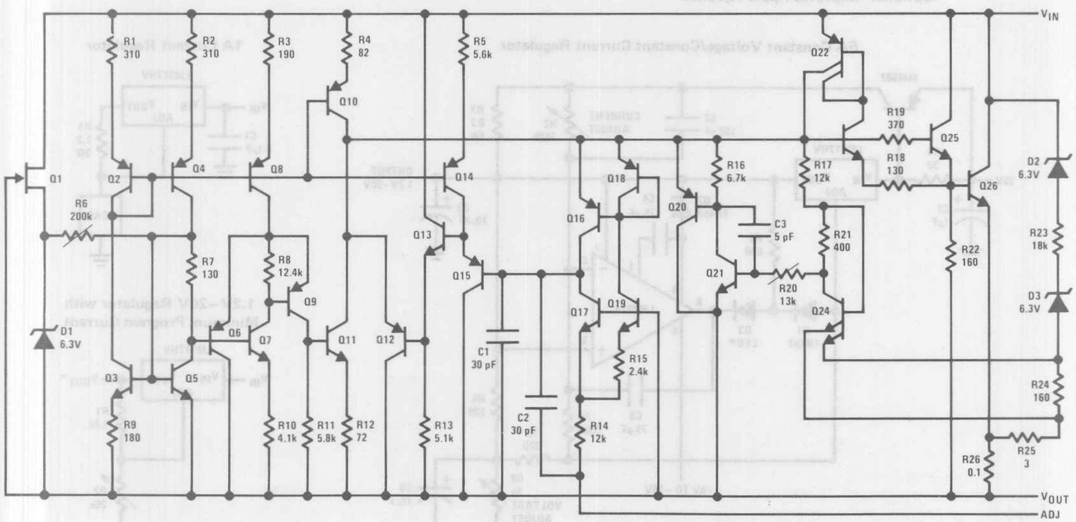
$$V_{OUT} = 1.25V \left(1 + \frac{R2}{R1}\right) + R2 I_{ADJ}$$

D1 protects against C1

D2 protects against C2

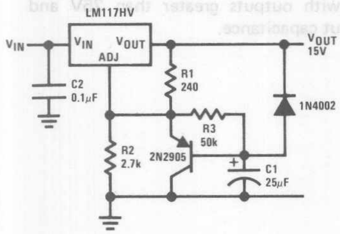
FIGURE 3. Regulator with Protection Diodes

Schematic Diagram

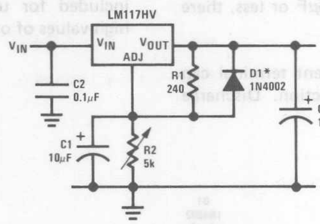


Typical Applications (cont'd.)

Slow Turn-On 15V Regulator



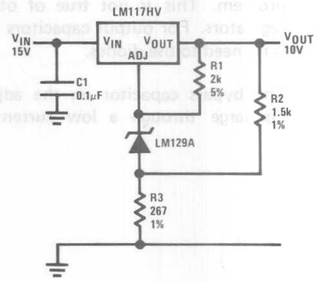
Adjustable Regulator with Improved Ripple Rejection



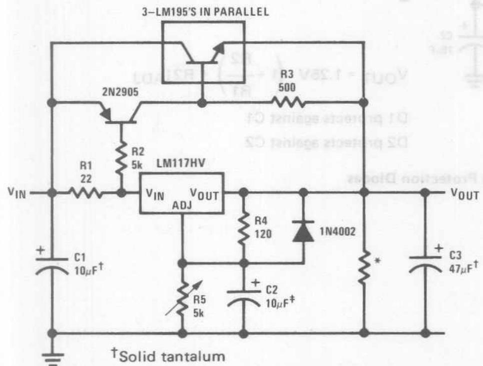
†Solid tantalum

*Discharges C1 if output is shorted to ground

High Stability 10V Regulator



High Current Adjustable Regulator

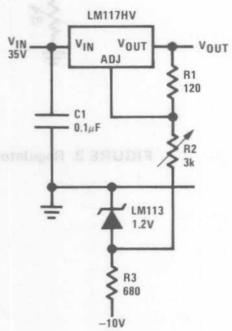


†Solid tantalum

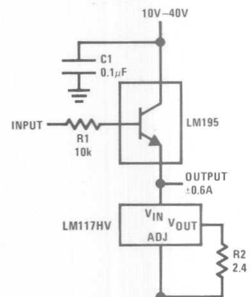
*Minimum load current = 30 mA

‡Optional—improves ripple rejection

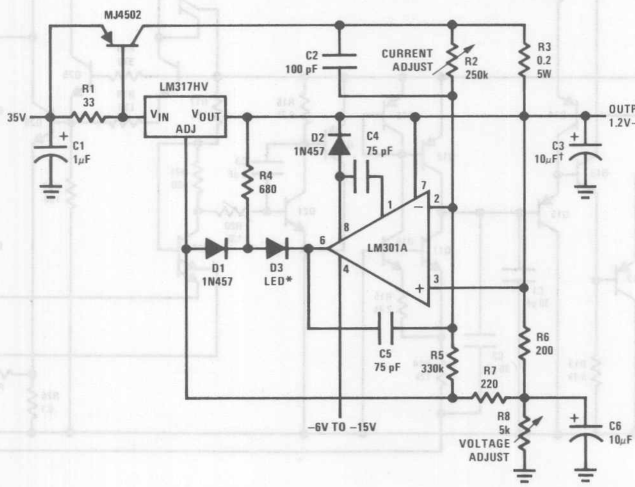
0 to 30V Regulator



Power Follower



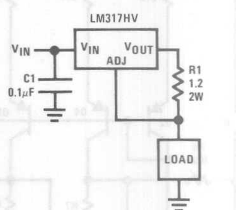
5A Constant Voltage/Constant Current Regulator



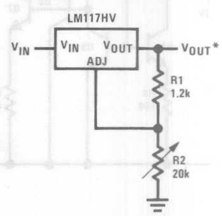
†Solid tantalum

*Lights in constant current mode

1A Current Regulator

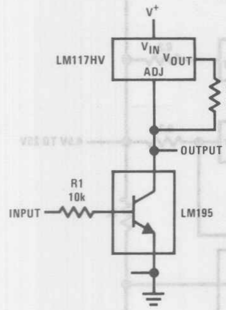


1.2V–20V Regulator with Minimum Program Current

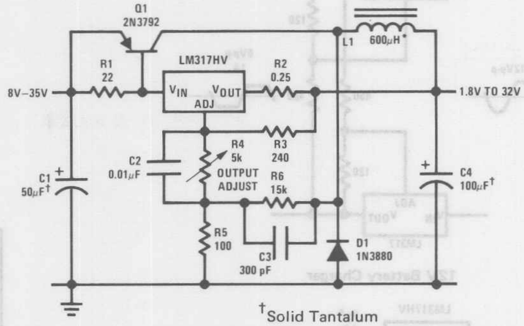


*Minimum load current ≈ 4 mA

High Gain Amplifier



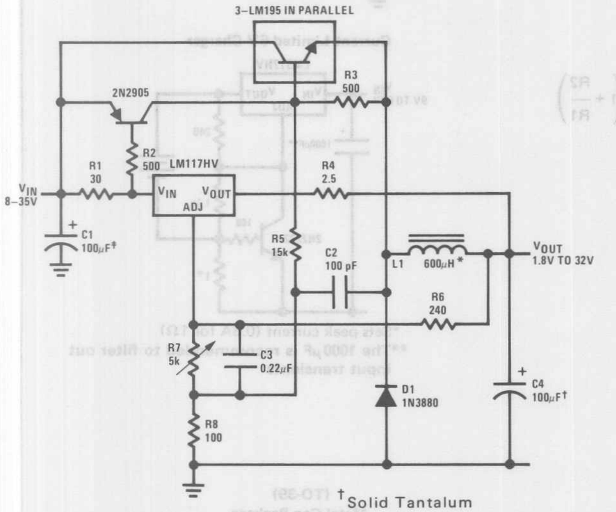
Low Cost 3A Switching Regulator



†Solid Tantalum

*Core–Arnold A-254168-2 60 turns

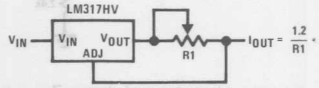
4A Switching Regulator with Overload Protection



†Solid Tantalum

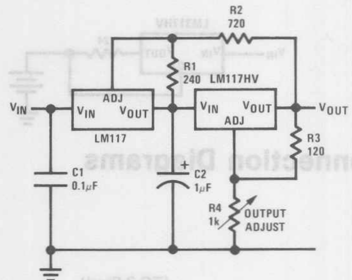
*Core Arnold A-254168-2 60 turns

Precision Current Limiter

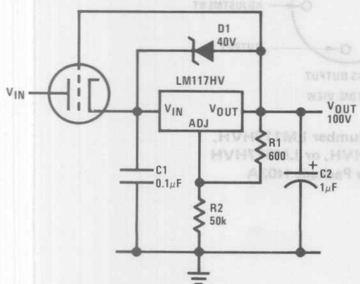


$*0.8\Omega \leq R1 \leq 120\Omega$

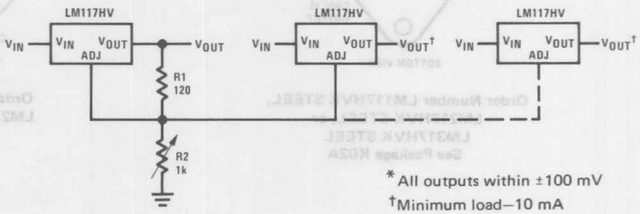
Tracking Preregulator



High Voltage Regulator

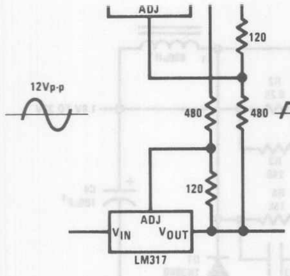


Adjusting Multiple On-Card Regulators with Single Control*

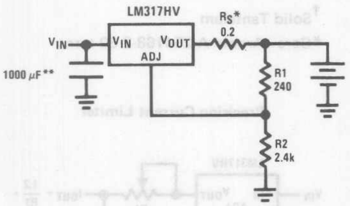


*All outputs within ±100 mV

†Minimum load—10 mA



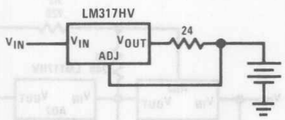
12V Battery Charger

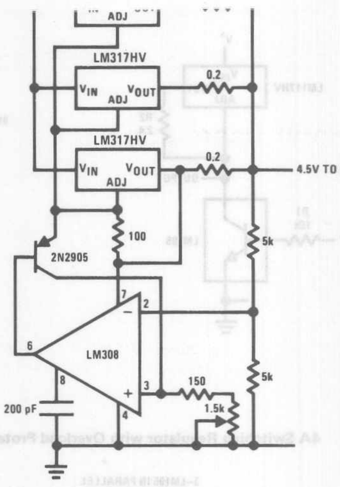


*R_S—sets output impedance of charger $Z_{OUT} = R_S \left(1 + \frac{R2}{R1}\right)$
Use of R_S allows low charging rates with fully charged battery.

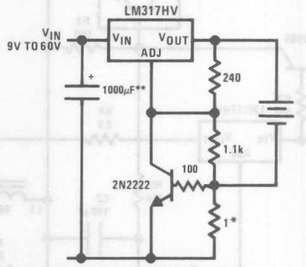
**The 1000 µF is recommended to filter out input transients

50 mA Constant Current Battery Charger





Current Limited 6V Charger

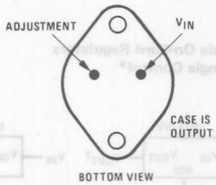


*Sets peak current (0.6A for 1Ω)

**The 1000µF is recommended to filter out input transients

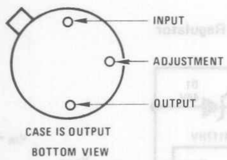
Connection Diagrams

(TO-3 Steel)
Metal Can Package



Order Number LM117HVK STEEL, LM217HVK STEEL, or LM317HVK STEEL
See Package K02A

(TO-39)
Metal Can Package



Order Number LM117HVH, LM217HVH, or LM317HVH
See Package H03A

National Semiconductor

LM120 Series 3-Terminal Negative Regulators

General Description

The LM120 series are three-terminal negative regulators with a fixed output voltage of -5V, -12V, and -15V, and up to 1.5A load current capability. Where other voltages are required, the LM137 series provides an output voltage range of -1.2V to -47V.

The LM120 need only one external component-a compensation capacitor at the output, making them easy to apply. Worst case guarantees on output voltage deviation due to any combination of line, load or temperature variation assure satisfactory system operation.

Exceptional effort has been made to make the LM120 Series immune to overload conditions. The regulators have current limiting which is independent of temperature, combined with thermal overload protection. Internal current limiting protects against momentary faults while thermal shutdown prevents junction temperatures from exceeding safe limits during prolonged overloads.

Although primarily intended for fixed output voltage applications, the LM120 Series may be programmed for higher output voltages with a simple resistive divider. The low quiescent drain current of the devices allows this technique to be used with good regulation.

Features

- Preset output voltage error less than ±3%
- Preset current limit
- Internal thermal shutdown
- Operates with input-output voltage differential down to 1V
- Excellent ripple rejection
- Low temperature drift
- Easily adjustable to higher output voltage

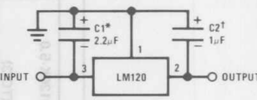
LM120 Series Packages and Power Capability

DEVICE	PACKAGE	RATED POWER DISSIPATION	DESIGN LOAD CURRENT
LM120	TO-3	20W	1.5A
LM320	TO-39	2W	0.5A
LM320T	TO-220	15W	1.5A
LM320M	TO-202	7.5W	0.5A
LM320ML*	TO-202	7.5W	0.25A
LM320L*	TO-92+	1.2W	0.1A

*Electrical specifications shown on separate data sheet

Typical Applications

Fixed Regulator

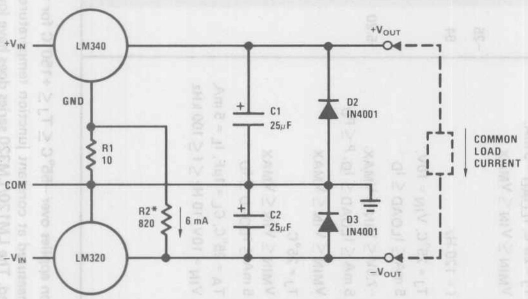


*Required if regulator is separated from filter capacitor by more than 3". For value given, capacitor must be solid tantalum. 25μF aluminum electrolytic may be substituted.

†Required for stability. For value given, capacitor must be solid tantalum. 25μF aluminum electrolytic may substituted. Values given may be increased without limit.

For output capacitance in excess of 100μF, a high current diode from input to output (1N4001, etc.) will protect the regulator from momentary input shorts.

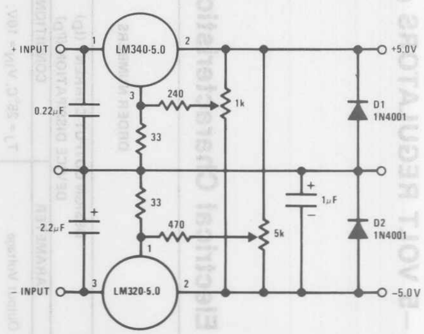
Preventing Positive Regulator Latch-Up



R1 & D1 allow the positive regulator to "start-up" when $^{+}V_{IN}$ is delayed relative to $^{-}V_{IN}$ and a heavy load is drawn between the outputs. Without R1 & D1, most three-terminal regulators will not start with heavy (0.1A–1A) load current flowing to the negative regulator, even though the positive output is clamped by D2.

*R2 is optional. Ground pin current from the positive regulator flowing through R1 will increase $+V_{OUT} \approx 60$ mV if R2 is omitted.

Dual Trimmed Supply



−5 VOLT REGULATORS (Note 3)

Absolute Maximum Ratings

Power Dissipation	Internally Limited
Input Voltage	−25V
Input-Output Voltage Differential	25V
Junction Temperatures	See Note 1
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

		METAL CAN PACKAGE												POWER PLASTIC PACKAGE						UNITS
ORDER NUMBERS		LM120K-5.0 (TO-3)			LM320K-5.0 (TO-3)			LM120H-5.0 (TO-39)			LM320H-5.0 (TO-39)			LM320T-5.0 (TO-220)			LM320MP-5.0 (TO-202)			
DESIGN OUTPUT CURRENT (I_D) DEVICE DISSIPATION (P_D)		1.5A 20W			1.5A 20W			0.5A 2W			0.5A 2W			1.5A 15W			0.5A 7.5W			
PARAMETER	CONDITIONS (NOTE 1)	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage	$T_J = 25°C$, $V_{IN} = 10V$, $I_{LOAD} = 5\ mA$	−5.1	−5	−4.9	−5.2	−5	−4.8	−5.1	−5.0	−4.9	−5.2	−5.0	−4.8	−5.2	−5.0	−4.8	−5.2	−5.0	−4.8	V
Line Regulation	$T_J = 25°C$, $I_{LOAD} = 5\ mA$, $V_{MIN} \leq V_{IN} \leq V_{MAX}$		10	25		10	40		10	25		10	40		10	40		10	40	mV
Input Voltage		−25		−7	−25		−7	−25		−7	−25		−7	−25		−7.5	−25		−7.5	V
Ripple Rejection	f = 120 Hz	54	64		54	64		54	64		54	64		54	64		54	64		dB
Load Regulation, (Note 2)	$T_J = 25°C$, $V_{IN} = 10V$, $5\ mA \leq I_{LOAD} \leq I_D$		50	75		50	100		30	50		30	50		50	100		40	100	mV
Output Voltage, (Note 1)	$-7.5V \leq V_{IN} \leq V_{MAX}$, $5\ mA \leq I_{LOAD} \leq I_D$, $P \leq P_D$	−5.20		−4.80	−5.25		−4.75	−5.20		−4.80	−5.25		−4.75	−5.25		−4.75	−5.25	−5.0	−4.75	V
Quiescent Current	$V_{MIN} \leq V_{IN} \leq V_{MAX}$		1	2		1	2		1	2		1	2		1	2		1	2	mA
Quiescent Current Change	$T_J = 25°C$																			
	$V_{MIN} \leq V_{IN} \leq V_{MAX}$		0.1	0.4		0.1	0.4		0.05	0.4		0.05	0.4		0.1	0.4		0.05	0.3	mA
	$5\ mA \leq I_{LOAD} \leq I_D$		0.1	0.4		0.1	0.4		0.04	0.4		0.04	0.4		0.1	0.4		0.04	0.25	mA
Output Noise Voltage	$T_A = 25°C$, $C_L = 1\mu F$, $I_L = 5\ mA$, $V_{IN} = 10V$, $10\ Hz \leq f \leq 100\ kHz$		150			150			150			150			150			150		μV
Long Term Stability			5	50		5	50		5	50		5	50		10			10		mV
Thermal Resistance																				
Junction to Case				3			3			15			15		4			12		°C/W
Junction to Ambient				35			35			150			150		50			70		°C/W

Note 1: This specification applies over $-55°C \leq T_J \leq +150°C$ for the LM120 and $0°C \leq T_J \leq +125°C$ for the LM320.

Note 2: Regulation is measured at constant junction temperature. Changes in output voltage due to heating effects must be taken into account separately. To ensure constant junction temperature, low duty cycle, pulse testing is used. The LM120/LM320 series does have low thermal feedback, improving line and load regulation. On all other tests, even though power dissipation is internally limited, electrical specifications apply only up to P_D.

Note 3: For −5V 3 amp regulators, see LM145 data sheet.

−12 VOLT REGULATORS

Absolute Maximum Ratings

Power Dissipation	Internall
Input Voltage	
Input-Output Voltage Differential	
Junction Temperatures	S
Storage Temperature Range	−65°C t
Lead Temperature (Soldering, 10 seconds)	

Electrical Characteristics

		METAL CAN PACKAGE												POWER PLASTIC PACKAGE					
	ORDER NUMBERS	LM120K-12 (TO-3)			LM320K-12 (TO-3)			LM120H-12 (TO-39)			LM320H-12 (TO-39)			LM320T-12 (TO-220)			LM320MP-12 (TO-202)		
DESIGN OUTPUT CURRENT (I_D) DEVICE DISSIPATION (P_D)		1A 20W			1A 20W			0.2A 2W			0.2A 2W			1A 15W			0.5A 7.5W		
PARAMETER	CONDITIONS (NOTE 1)	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
Output Voltage	$T_J = 25°C$, $V_{IN} = 17V$, $I_{LOAD} = 5\ mA$	−12.3	−12	−11.7	−12.4	−12	−11.6	−12.3	−12	−11.7	−12.4	−12	−11.6	−12.4	−12	−11.6	−12.5	−12	−11.5
Line Regulation	$T_J = 25°C$, $I_{LOAD} = 5\ mA$, $V_{MIN} \leq V_{IN} \leq V_{MAX}$		4	10		4	20		4	10		4	20		4	20		4	24
Input Voltage		−32		−14	−32		−14	−32		−14	−32		−14	−32		−14.5	−32		−14.5
Ripple Rejection	f = 120 Hz	56	80		56	80		56	80		56	80		56	80		56	80	
Load Regulation, (Note 2)	$T_J = 25°C$, $V_{IN} = 17V$, $5\ mA \leq I_{LOAD} \leq I_D$		30	80		30	80		10	25		10	40		30	80		40	100
Output Voltage, (Note 1)	$14.5V \leq V_{IN} \leq V_{MAX}$, $5\ mA \leq I_{LOAD} \leq I_D$, $P \leq P_D$	−12.5		−11.5	−12.6		−11.4	−12.5		−11.5	−12.6		−11.4	−12.6		−11.4	−12.6		−11.4
Quiescent Current	$V_{MIN} \leq V_{IN} \leq V_{MAX}$		2	4		2	4		2	4		2	4		2	4		2	4
Quiescent Current Change	$T_J = 25°C$																		
	$V_{MIN} \leq V_{IN} \leq V_{MAX}$		0.1	0.4		0.1	0.4		0.05	0.4		0.05	0.4		0.1	0.4		0.05	0.3
	$5\ mA \leq I_{LOAD} \leq I_D$		0.1	0.4		0.1	0.4		0.03	0.4		0.03	0.4		0.1	0.4		0.04	0.25
Output Noise Voltage	$T_A = 25°C$, $C_L = 1\mu F$, $I_L = 5\ mA$, $V_{IN} = 17V$, $10\ Hz \leq f \leq 100\ kHz$		400			400			400			400			400			400	
Long Term Stability			12	120		12	120		12	120		12	120		24			24	
Thermal Resistance																			
Junction to Case				3			3			15			15		4			12	
Junction to Ambient				35			35			150			150		50			70	

Note 1: This specification applies over $-55°C \leq T_J \leq +150°C$ for the LM120 and $0°C \leq T_J \leq +125°C$ for the LM320.

Note 2: Regulation is measured at constant junction temperature. Changes in output voltage due to heating effects must be taken into account separately. To ensure constant junction temperature, cycle, pulse testing is used. The LM120/LM320 series does have low thermal feedback, improving line and load regulation. On all other tests, even though power dissipation is internally limited, electrical tions apply only up to P_D.

–15 VOLT REGULATORS

Absolute Maximum Ratings

Power Dissipation	Internally Limited
Input Voltage	
LM120/LM320	–40V
LM320T/LM320MP	–35V
Input-Output Voltage Differential	30V
Junction Temperatures	See Note 1
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

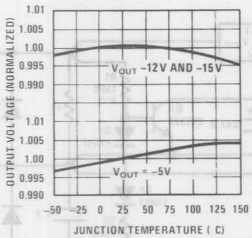
		METAL CAN PACKAGE												POWER PLASTIC PACKAGE						UNITS
	ORDER NUMBERS	LM120K-15 (TO-3)			LM320K-15 (TO-3)			LM120H-15 (TO-39)			LM320H-15 (TO-39)			LM320T-15 (TO-220)			LM320MP-15 (TO-202)			
DESIGN OUTPUT CURRENT (I_D) DEVICE DISSIPATION (P_D)		1A 20W			1A 20W			0.2A 2W			0.2A 2W			1A 15W			0.5A 7.5W			
PARAMETER	CONDITIONS (NOTE 1)	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage	$T_J = 25°C$, $V_{IN} = 20V$, $I_{LOAD} = 5\ mA$	–15.3	–15	–14.7	–15.4	–15	–14.6	–15.3	–15	–14.7	–15.4	–15	–14.6	–15.5	–15	–14.5	–15.6	–15	–14.4	V
Line Regulation	$T_J = 25°C$, $I_{LOAD} = 5\ mA$, $V_{MIN} \leq V_{IN} \leq V_{MAX}$		5	10		5	20		5	10		5	20		5	20		5	30	mV
Input Voltage		–35		–17	–35		–17	–35		–17	–35		–17	–35		–17.5	–35		–17.5	V
Ripple Rejection	f = 120 Hz	56	80		56	80		56	80		56	80		56	80		56	80		dB
Load Regulation, (Note 2)	$T_J = 25°C$, $V_{IN} = 20V$, $5\ mA \leq I_{LOAD} \leq I_D$		30	80		30	80		10	25		10	40		30	80		40	100	mV
Output Voltage, (Note 1)	$17.5V \leq V_{IN} \leq V_{MAX}$, $5\ mA \leq I_{LOAD} \leq I_D$, $P < P_D$	–15.5		–14.5	–15.6		–14.4	–15.5		–14.5	–15.6		–14.4	–15.7		–14.3	–15.7		–14.3	V
Quiescent Current	$V_{MIN} \leq V_{IN} \leq V_{MAX}$		2	4		2	4		2	4		2	4		2	4		2	4	mA
Quiescent Current Change	$T_J = 25°C$																			
	$V_{MIN} \leq V_{IN} \leq V_{MAX}$		0.1	0.4		0.1	0.4		0.05	0.4		0.05	0.4		0.1	0.4		0.05	0.3	mA
	$5\ mA \leq I_{LOAD} \leq I_D$		0.1	0.4		0.1	0.4		0.03	0.4		0.03	0.4		0.1	0.4		0.04	0.25	mA
Output Noise Voltage	$T_A = 25°C$, $C_L = 1\mu F$, $I_L = 5\ mA$, $V_{IN} = 20V$, $10\ Hz \leq f \leq 100\ kHz$		400			400			400			400			400			400		μV
Long Term Stability			15	150		15	150		15	150		15	150		30			30		mV
Thermal Resistance																				
Junction to Case				3			3			15			15		4			12		°C/W
Junction to Ambient				35			35			150			150		50			70		°C/W

Note 1: This specification applies over $-55°C \leq T_J \leq +150°C$ for the LM120 and $0°C \leq T_J \leq +125°C$ for the LM320.

Note 2: Regulation is measured at constant junction temperature. Changes in output voltage due to heating effects must be taken into account separately. To ensure constant junction temperature, low duty cycle, pulse testing is used. The LM120/LM320 series does have low thermal feedback, improving line and load regulation. On all other tests, even though power dissipation is internally limited, electrical specifications apply only up to P_D.

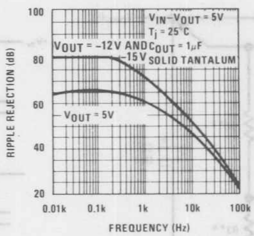
Typical Performance Characteristics

Output Voltage vs Temperature

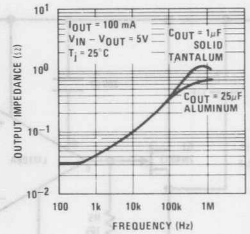


Note: Shaded portion refers to LM320 series regulators.

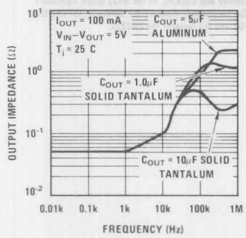
Ripple Rejection (All Types)



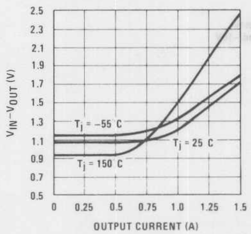
Output Impedance TO-3 and TO-220 Packages



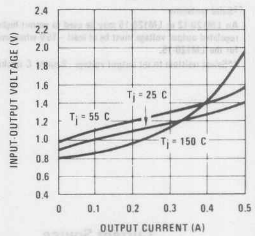
Output Impedance TO-5 and TO-202 Packages



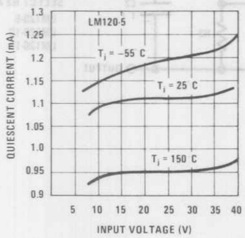
Minimum Input-Output Differential TO-3 and TO-220 Packages



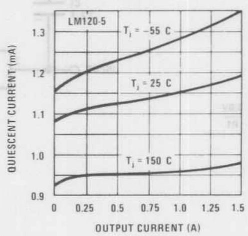
Minimum Input-Output Differential TO-5 and TO-202 Packages



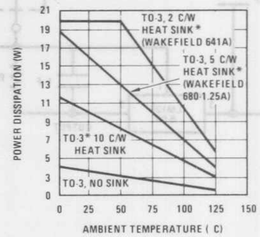
Quiescent Current vs Input Voltage



Quiescent Current vs Load Current



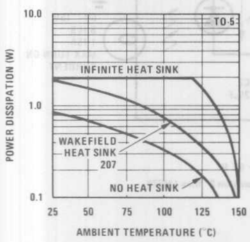
Maximum Average Power Dissipation (TO-3)



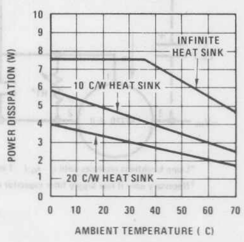
Note: Shaded area shows operating range of TO-5 and TO-202 packages.

*These curves for LM120 and LM220. Derate 25°C further for LM320.

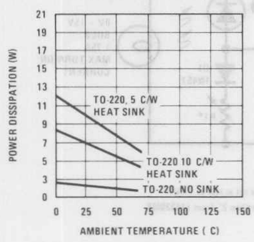
Maximum Average Power Dissipation (TO-5)



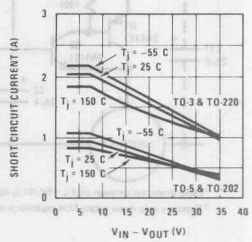
Maximum Average Power Dissipation (TO-202)



Maximum Average Power Dissipation (TO-220)

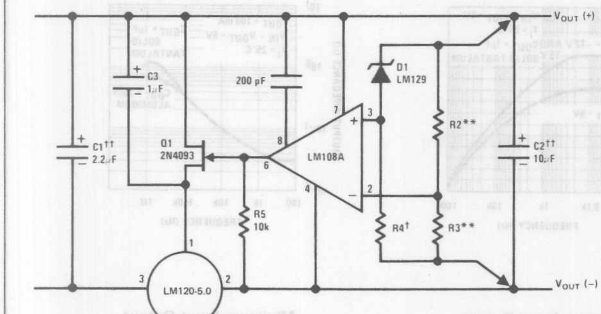


Short Circuit Current



Typical Applications (cont'd.)

High Stability 1 Amp Regulator



Load and line regulation 0.01% temperature stability 0.2%

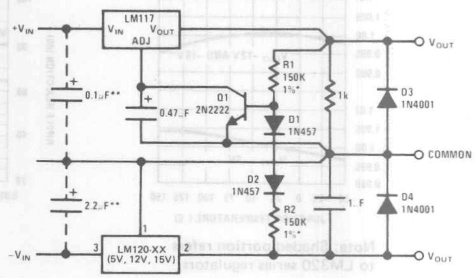
†Determines Zener current.

††Solid tantalum.

An LM120-12 or LM120-15 may be used to permit higher input voltages, but the regulated output voltage must be at least −15V when using the LM120-12 and −18V for the LM120-15.

**Select resistors to set output voltage. 2 ppm/°C tracking suggested.

Wide Range Tracking Regulator

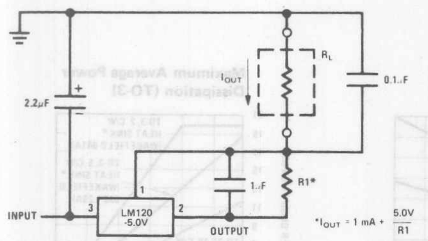


*Resistor tolerance of R1 and R2 determine matching of (+) and (−) inputs.

**Necessary only if raw supply capacitors are more than 3" from regulators

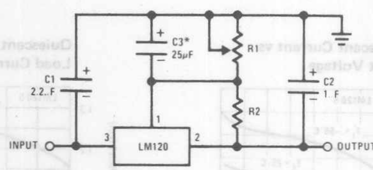
An LM3086N array may substitute for Q1, D1 and D2 for better stability and tracking. In the array diode transistors Q5 and Q4 (in parallel) make up D2, similarly, Q1 and Q2 become D1 and Q3 replaces the 2N2222.

Current Source



$^{*}I_{OUT} = 1\,mA + \frac{5.0V}{R1}$

Variable Output



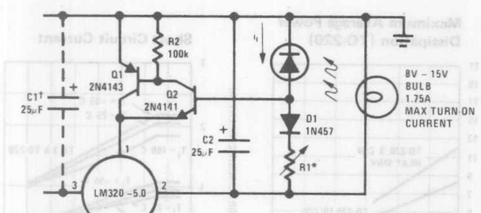
*Optional. Improves transient response and ripple rejection.

$V_{OUT} = V_{SET}\,\frac{R1 + R2}{R2}$

SELECT R2 AS FOLLOWS

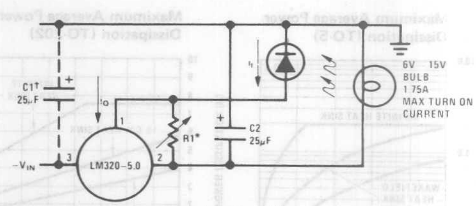
LM120-5	**−300Ω**
LM120-12	**−750Ω**
LM120-15	**−1K**

Light Controllers Using Silicon Photo Cells



*Lamp brightness increases until i_l = 5V/R1 (i_l can be set as low as 1μA).

†Necessary only if raw supply filter capacitor is more than 2" from LM320MP.

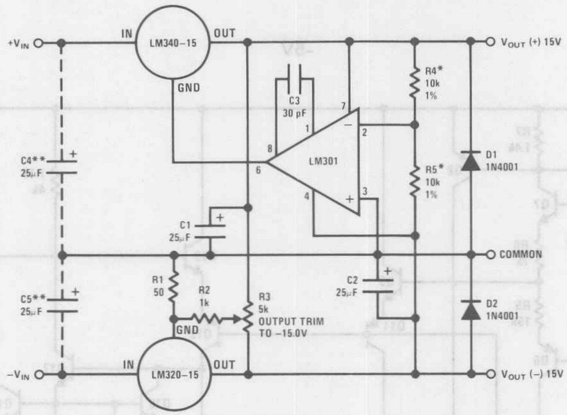


*Lamp brightness increases until i_l - i_Q (1 mA) · 5V R1.

†Necessary only if raw supply filter capacitor is more than 2" from LM320.

Typical Applications (cont'd.)

±15V, 1 Amp Tracking Regulators

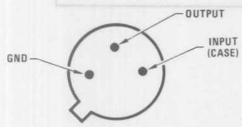


Performance (Typical)

Load Regulation at ΔI_L = 1A	10 mV	1 mV
Output Ripple, C_{IN} = 3000µF, I_L = 1A	100µVrms	100µVrms
Temperature Stability	+50 mV	+50 mV
Output Noise 10 Hz $\leq f \leq$ 10 kHz	150µVrms	150µVrms

*Resistor tolerance of R4 and R5 determine matching of (+) and (–) outputs.
**Necessary only if raw supply filter capacitors are more than 2" from regulators.

Connection Diagrams

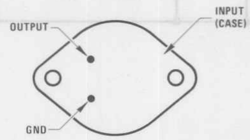


BOTTOM VIEW

Metal Can Package (TO-39) (H)
Order Numbers:

LM120H-5.0 LM120H-12 LM120H-15
LM320H-5.0 LM320H-12 LM320H-15

See Package H03A

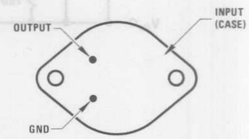


BOTTOM VIEW

Steel Metal Can Package TO-3 (K)
Order Numbers:

LM120K-5.0 LM120K-12 LM120K-15
LM320K-5.0 LM320K-12 LM320K-15

See Package K02A

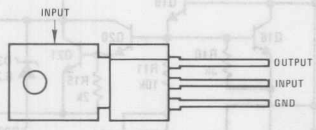


BOTTOM VIEW

Aluminum Metal Can Package TO-3 (KC)
Order Numbers:

LM320KC-5.0 LM320KC-12
LM320KC-15

See Package KC02A



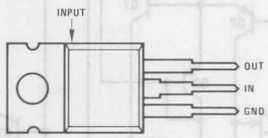
FRONT VIEW

Power Package TO-202 (P)
Order Numbers:

LM320MP-5.0
LM320MP-12
LM320MP-15

See Package P03A

For Tab Formed TO-202
Order Numbers:
LM320MP-5.0TB
LM320MP-12TB
LM320MP-15TB
See Package P03E



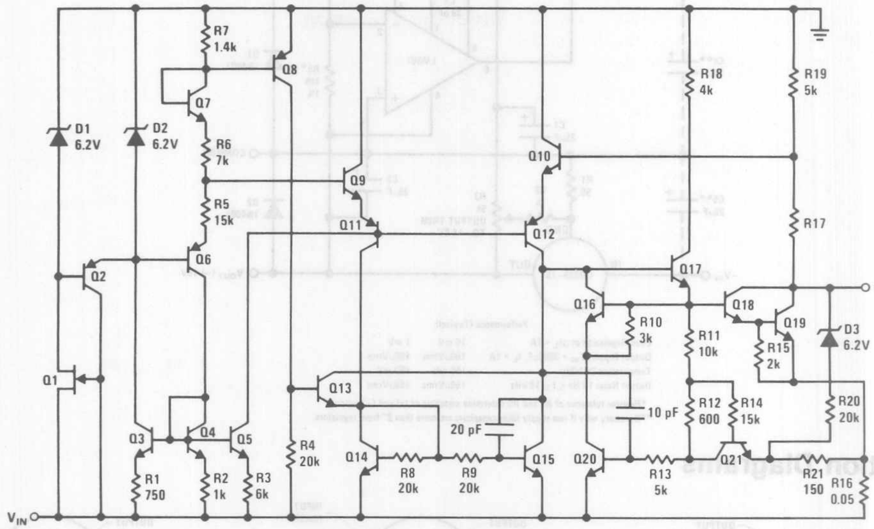
FRONT VIEW

Power Package TO-220 (T)
Order Numbers:

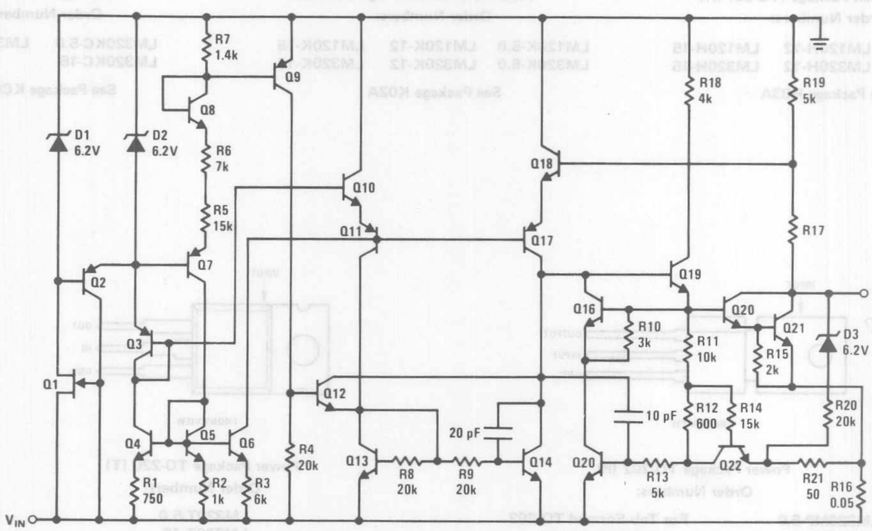
LM320T-5.0
LM320T-12
LM320T-15

See Package T03B

-5V



-12V and -15V



General Description

The LM123 is a three-terminal positive regulator with a preset 5V output and a load driving capability of 3 amps. New circuit design and processing techniques are used to provide the high output current without sacrificing the regulation characteristics of lower current devices.

The 3 amp regulator is virtually blowout proof. Current limiting, power limiting, and thermal shutdown provide the same high level of reliability obtained with these techniques in the LM109 1 amp regulator.

No external components are required for operation of the LM123. If the device is more than 4 inches from the filter capacitor, however, a 1μF solid tantalum capacitor should be used on the input. A 0.1μF or larger capacitor may be used on the output to reduce load transient spikes created by fast switching digital logic, or to swamp out stray load capacitance.

An overall worst case specification for the combined effects of input voltage, load currents, ambient temperature, and power dissipation ensure that the LM123 will perform satisfactorily as a system element.

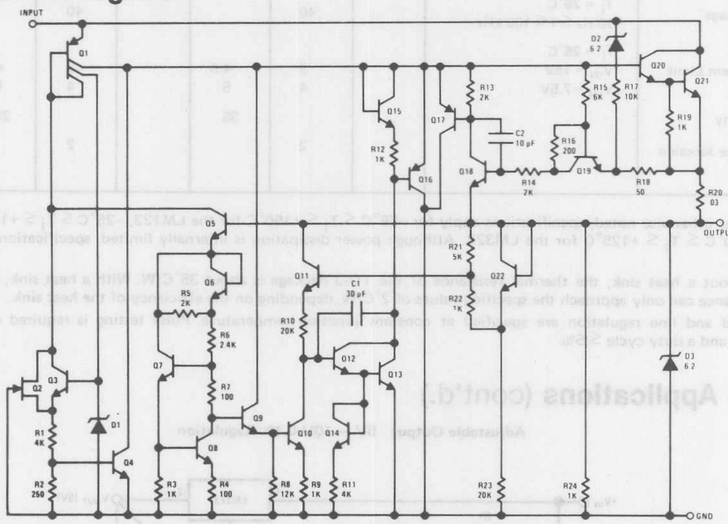
For applications requiring other voltages, see LM150 series data sheet.

Operation is guaranteed over the junction temperature range −55°C to +150°C. An electrically identical LM223 operates from −25°C to +150°C and the LM323 is specified from 0°C to +125°C junction temperature. A hermetic TO-3 package is used for high reliability and low thermal resistance.

Features

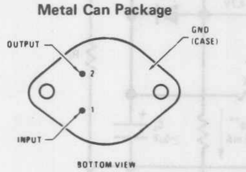
- 3 amp output current
- Internal current and thermal limiting
- 0.01Ω typical output impedance
- 7.5 minimum input voltage
- 30W power dissipation
- 100% electrical burn-in

Schematic Diagram



Connection Diagram

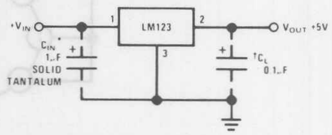
Metal Can Package



Order Number LM123K STEEL, LM223K STEEL or LM323K STEEL
See Package K02A

Typical Applications

Basic 3 Amp Regulator



*Required if LM123 is more than 4" from filter capacitor.
†Regulator is stable with no load capacitor into resistive loads.

Absolute Maximum Ratings

Input Voltage	20V
Power Dissipation	Internally Limited
Operating Junction Temperature Range	
LM123	$-55^\circ C$ to $+150^\circ C$
LM223	$-25^\circ C$ to $+150^\circ C$
LM323	$0^\circ C$ to $+125^\circ C$
Storage Temperature Range	$-65^\circ C$ to $+150^\circ C$
Lead Temperature (Soldering, 10 sec)	$300^\circ C$

Preconditioning

Burn-In in Thermal Limit **100% All Devices**

Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	LM123/LM223 MIN	LM123/LM223 TYP	LM123/LM223 MAX	LM323 MIN	LM323 TYP	LM323 MAX	UNITS
Output Voltage	$T_j = 25^\circ C$, $V_{IN} = 7.5V$, $I_{OUT} = 0$	4.7	5	5.3	4.8	5	5.2	V
Output Voltage	$7.5V \le V_{IN} \le 15V$, $0 \le I_{OUT} \le 3A$, $P \le 30W$	4.6		5.4	4.75		5.25	V
Line Regulation (Note 3)	$T_j = 25^\circ C$, $7.5V \le V_{IN} \le 15V$		5	25		5	25	mV
Load Regulation (Note 3)	$T_j = 25^\circ C$, $V_{IN} = 7.5V$, $0 \le I_{OUT} \le 3A$		25	100		25	100	mV
Quiescent Current	$7.5V \le V_{IN} \le 15V$, $0 \le I_{OUT} \le 3A$		12	20		12	20	mA
Output Noise Voltage	$T_j = 25^\circ C$, $10\ Hz \le f \le 100\ kHz$		40			40		μVrms
Short Circuit Current Limit	$T_j = 25^\circ C$, $V_{IN} = 15V$		3	4.5		3	4.5	A
	$V_{IN} = 7.5V$		4	5		4	5	A
Long Term Stability				35			35	mV
Thermal Resistance Junction to Case (Note 2)			2			2		$^\circ$C/W

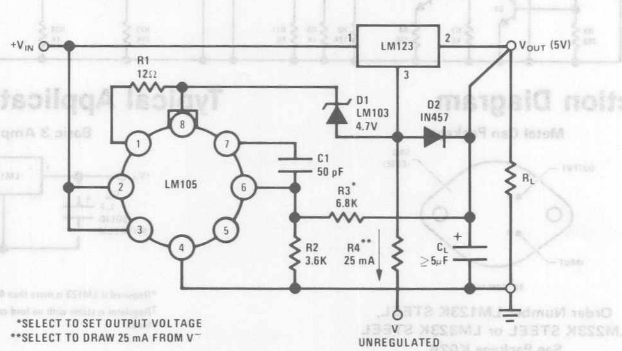
Note 1: Unless otherwise noted, specifications apply for $-55^\circ C \le T_j \le +150^\circ C$ for the LM123, $-25^\circ C \le T_j \le +150^\circ C$ for the LM223, and $0^\circ C \le T_j \le +125^\circ C$ for the LM323. Although power dissipation is internally limited, specifications apply only for $P \le 30W$.

Note 2: Without a heat sink, the thermal resistance of the TO-3 package is about 35°C/W. With a heat sink, the effective thermal resistance can only approach the specified values of 2°C/W, depending on the efficiency of the heat sink.

Note 3: Load and line regulation are specified at constant junction temperature. Pulse testing is required with a pulse width $\le$ 1 ms and a duty cycle $\le$ 5%.

Typical Applications (cont'd.)

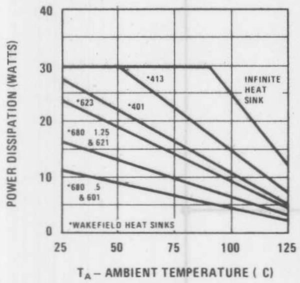
Adjustable Output 5V – 10V 0.1% Regulation



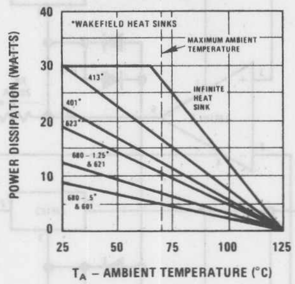
*SELECT TO SET OUTPUT VOLTAGE
**SELECT TO DRAW 25 mA FROM V⁻

Typical Performance Characteristics

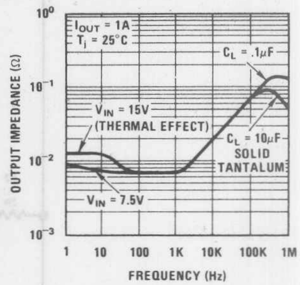
Maximum Average Power Dissipation For LM123; LM223



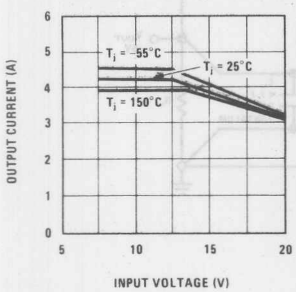
Maximum Average Power Dissipation For LM323



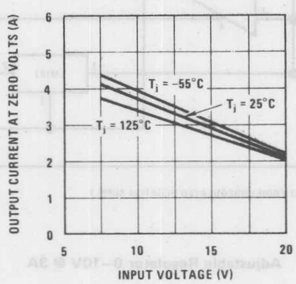
Output Impedance



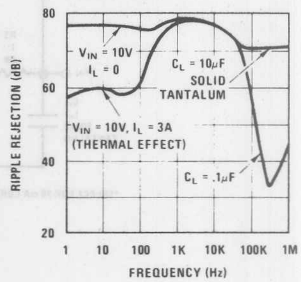
Peak Available Output Current



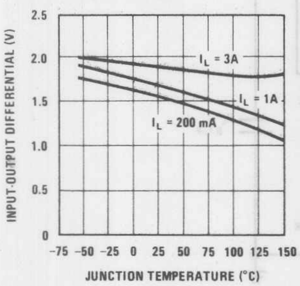
Short Circuit Current



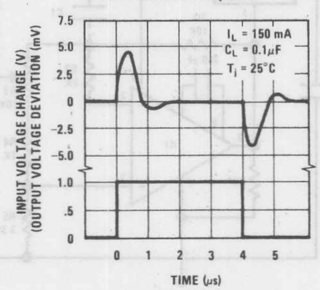
Ripple Rejection



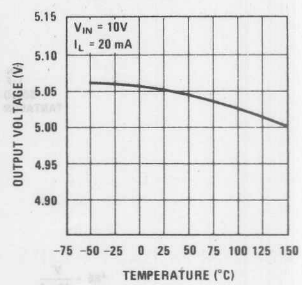
Dropout Voltage



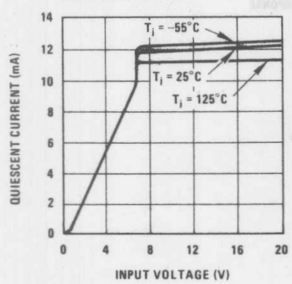
Line Transient Response



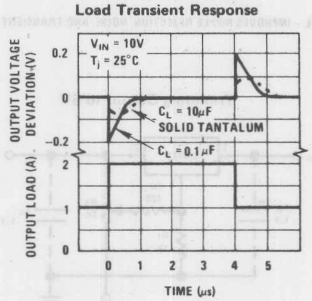
Output Voltage



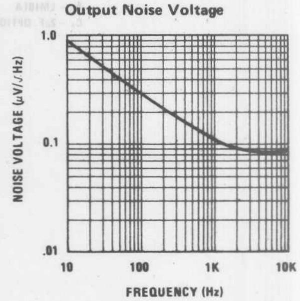
Quiescent Current



Load Transient Response

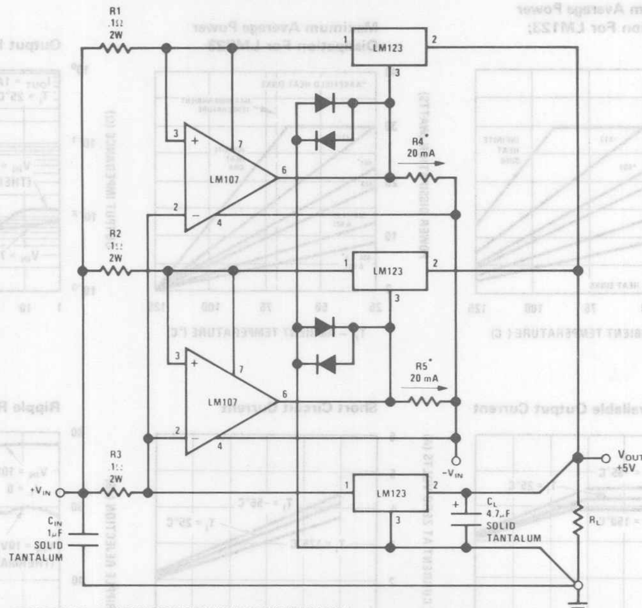


Output Noise Voltage



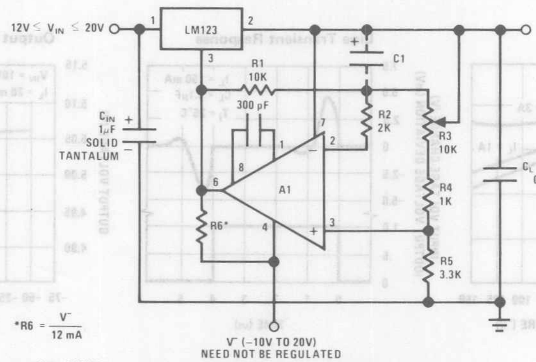
Typical Applications (cont'd.)

10 Amp Regulator With Complete Overload Protection



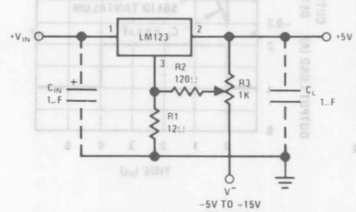
*SELECT FOR 20 mA CURRENT FROM UNREGULATED NEGATIVE SUPPLY

Adjustable Regulator 0–10V @ 3A



A1 – LM101A
C_1 – 2μF OPTIONAL – IMPROVES RIPPLE REJECTION, NOISE, AND TRANSIENT RESPONSE

Trimming Output to 5V



National Semiconductor

Voltage Regulators

LM125/LM325/LM325A, LM126/LM326 Voltage Regulators

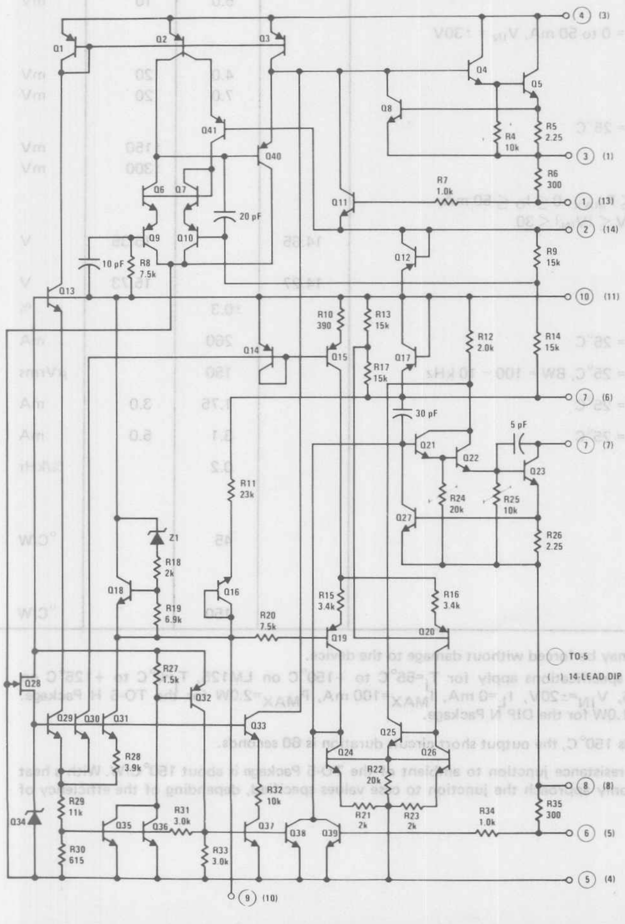
General Description

These are dual polarity tracking regulators designed to provide balanced positive and negative output voltages at current up to 100 mA, the devices are set for ±15 V and ±12 V outputs respectively. Input voltages up to ±30 V can be used and there is provision for adjustable current limiting. These devices are available in three package types to accomodate various power requirements and temperature ranges.

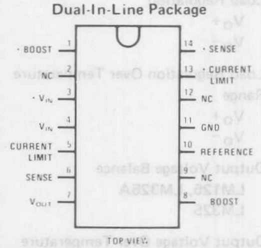
Features

- ±15V and ±12V tracking outputs
- Output current to 100 mA
- Output voltages balanced to within 1% (LM125, LM126, LM325A)
- Line and load regulation of 0.06%
- Internal thermal overload protection
- Standby current drain of 3 mA
- Externally adjustable current limit
- Internal current limit

Schematic and Connection Diagrams

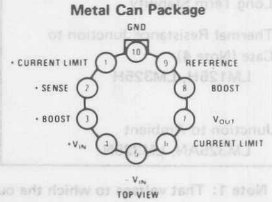


Dual-In-Line Package



Order Number LM325AN, LM325N, or LM326N
See Package N14A

Metal Can Package



Case connected to $-V_{IN}$
Order Number LM125H, LM325H, LM126H, or LM326H
See Package H10C

Forced V_O^+ (min) (Note 1)	−0.5V
Forced V_O^- (max) (Note 1)	+0.5V
Power Dissipation (Note 2)	P_{MAX}
Output Short-Circuit Duration (Note 3)	Indefinite
Operating Temperature Range	
LM125	−55°C to +125°C
LM325, LM325A	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics LM125/LM325/LM325A (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	$T_j = 25°C$				
LM125/LM325A		14.8	15	15.2	V
LM325		14.5	15	15.5	V
Input-Output Differential		2.0			V
Line Regulation	V_{IN} = 18V to 30V, I_L = 20 mA, $T_j = 25°C$		2.0	10	mV
Line Regulation Over Temperature Range	V_{IN} = 18V to 30V, I_L = 20 mA		2.0	20	mV
Load Regulation	I_L = 0 to 50 mA, $V_{IN} = \pm 30V$, $T_j = 25°C$				
V_O+			3.0	10	mV
V_O-			5.0	10	mV
Load Regulation Over Temperature Range	I_L = 0 to 50 mA, $V_{IN} = \pm 30V$				
V_O+			4.0	20	mV
V_O-			7.0	20	mV
Output Voltage Balance	$T_j = 25°C$				
LM125, LM325A				±150	mV
LM325				±300	mV
Output Voltage Over Temperature Range	$P \leq P_{MAX}$, $0 \leq I_O \leq 50$ mA, $18V \leq \lvert V_{IN} \rvert \leq 30$				
LM125/LM325A		14.65		15.35	V
LM325		14.27		15.73	V
Temperature Stability of V_O			±0.3		%
Short Circuit Current Limit	$T_j = 25°C$		260		mA
Output Noise Voltage	$T_j = 25°C$, BW = 100 − 10 kHz		150		μVrms
Positive Standby Current	$T_j = 25°C$		1.75	3.0	mA
Negative Standby Current	$T_j = 25°C$		3.1	5.0	mA
Long Term Stability			0.2		%/kHr
Thermal Resistance Junction to Case (Note 4)					
LM125H, LM325H			45		°C/W
Junction to Ambient					
LM325AN, LM325N			150		°C/W

Note 1: That voltage to which the output may be forced without damage to the device.

Note 2: Unless otherwise specified these specifications apply for T_j=55°C to +150°C on LM125, T_j=0°C to +125°C on LM325A, T_j=0°C to +125°C on LM325, V_{IN}=±20V, I_L=0 mA, I_{MAX}=100 mA, P_{MAX}=2.0W for the TO-5 H Package. I_{MAX}=100 mA. I_{MAX}=100 mA, P_{MAX}=1.0W for the DIP N Package.

Note 3: If the junction temperature exceeds 150°C, the output short circuit duration is 60 seconds.

Note 4: Without a heat sink, the thermal resistance junction to ambient of the TO-5 Package is about 150°C/W. With a heat sink, the effective thermal resistance can only approach the junction to case values specified, depending of the efficiency of the sink.

Absolute Maximum Ratings

Input Voltage	±30V
Forced V_O^+ (Min) (Note 1)	−0.5V
Forced V_O^- (Max) (Note 1)	+0.5V
Power Dissipation (Note 2)	Internally Limited
Output Short-Circuit Duration (Note 3)	Indefinite
Operating Temperature Range	
LM126	−55°C to +125°C
LM326	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics LM126/LM326 (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	$T_j = 25°C$				
LM126, LM326		11.8	12	12.2	V
		11.5		12.5	V
Input-Output Differential		2.0			V
Line Regulation	V_{IN} = 15V to 30V I_L = 20 mA, T_j = 25°C		2.0	10	mV
Line Regulation Over Temperature Range	V_{IN} = 15V to 30V, I_L = 20 mA		2.0	20	mV
Load Regulation	I_L = 0 to 50 mA, V_{IN} = ±30V, T_j = 25°C				
V_O^+			3.0	10	mV
V_O^-			5.0	10	mV
Load Regulation Over Temperature Range	I_L = 0 to 50 mA, V_{IN} = ±30V				
V_O^+			4.0	20	mV
V_O^-			7.0	20	mV
Output Voltage Balance	T_j = 25°C				
LM126, LM326				±125	mV
				±250	mV
Output Voltage Over Temperature Range	$P \leq P_{MAX}$, $0 \leq I_O \leq 50$ mA $15V \leq \|V_{IN}\| \leq 30V$				
LM126		11.68		12.32	V
LM326		11.32		12.68	V
Temperature Stability of V_O			±0.3		%
Short Circuit Current Limit	T_j = 25°C		260		mA
Output Noise Voltage	T_j = 25°C, BW = 100 − 10 kHz		100		μVrms
Positive Standby Current	T_j = 25°C, I_L = 0		1.75	3.0	mA
Negative Standby Current	T_j = 25°C, I_L = 0		3.1	5.0	mA
Long Term Stability			0.2		%/kHr
Thermal Resistance Junction to Case (Note 4) LM126/LM326H			45		°C/W
Junction to Ambient LM326N			150		°C/W

Note 1: That voltage to which the output may be forced without damage to the device.

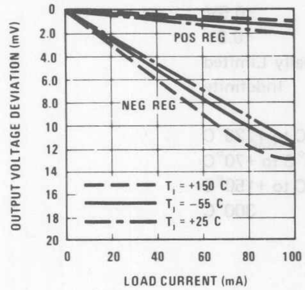
Note 2: Unless otherwise specified, these specifications apply for T_j=55°C to +150°C on LM126, T_j=0°C to +125°C on LM326, V_{IN}=±20V, I_L=0 mA, I_{MAX}=100 mA, P_{MAX}=2.0W for the TO-5 H Package I_{MAX}=100 mA. I_{MAX}=100 mA, P_{MAX}=1.0W for the DIP N Package.

Note 3: If the junction temperature exceeds 150°C the output short circuit duration is 60 seconds.

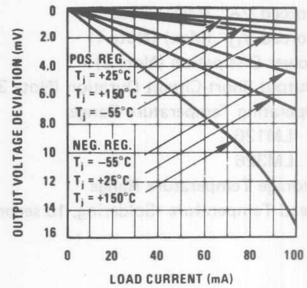
Note 4: Without a heat sink, the thermal resistance junction to ambient of the TO-5 Package is about 150° C/W. With a heat sink, the effective thermal resistance can only approach the junction to case values specified, depending on the efficiency of the sink.

Typical Performance Characteristics (V_{IN} = ±20V, I_L = 0 mA, T_j = 25°C, unless otherwise noted.)

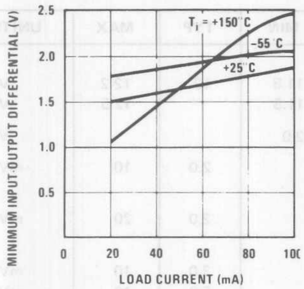
LM125 Load Regulation



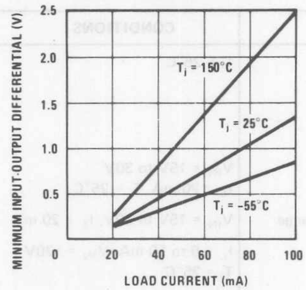
LM126 Load Regulation



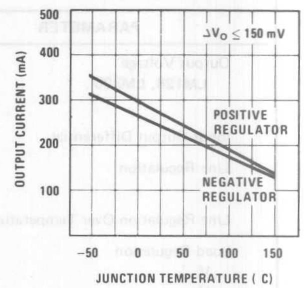
LM125/126 Regulator Dropout Voltage for Positive Regulator



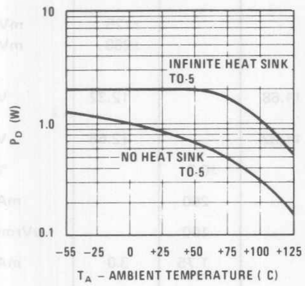
LM125/126 Regulator Dropout Voltage for Negative Regulator



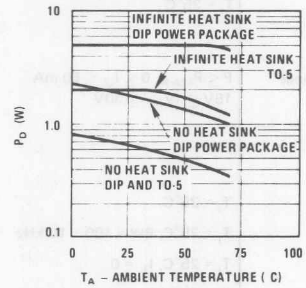
LM125/126 Peak Output Current vs Junction Temperature



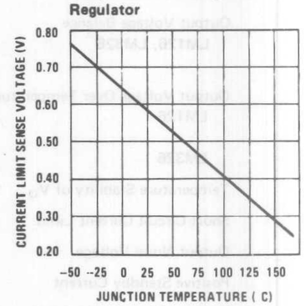
LM125/126 Maximum Average Power Dissipation vs Ambient Temperature



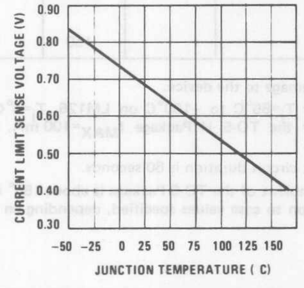
LM325/326 Maximum Average Power Dissipation vs Ambient Temperature



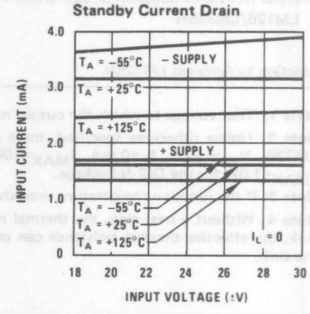
LM125/126 Current Limit Sense Voltage vs Temperature for Negative Regulator



LM125/126 Current Limit Sense Voltage vs Temperature for Positive Regulator

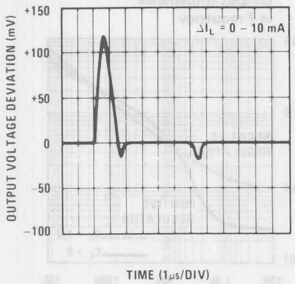


LM125/126 Standby Current Drain

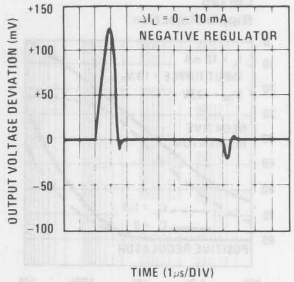


Typical Performance Characteristics (cont'd.)

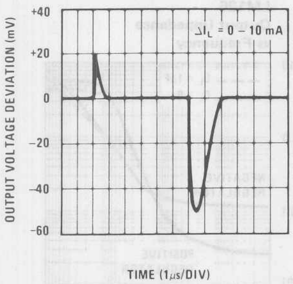
LM125
Load Transient Response
for Negative Regulator



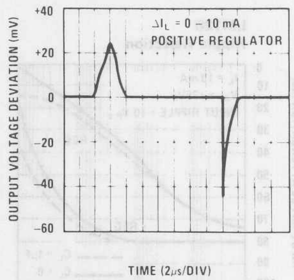
LM126
Load Transient Response



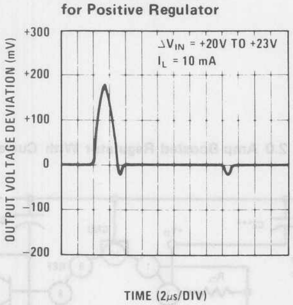
LM125
Load Transient Response
for Positive Regulator



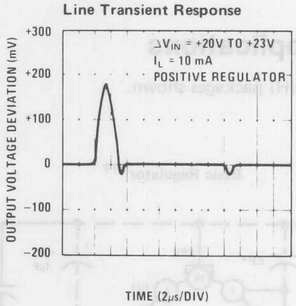
LM126
Load Transient Response



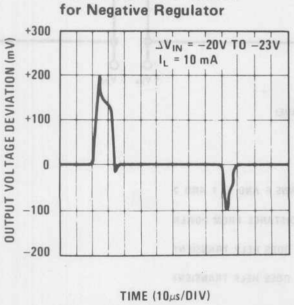
LM125
Line Transient Response
for Positive Regulator



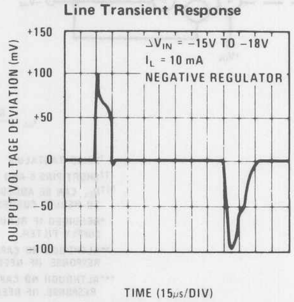
LM126
Line Transient Response



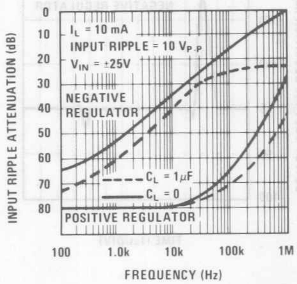
LM125
Line Transient Response
for Negative Regulator



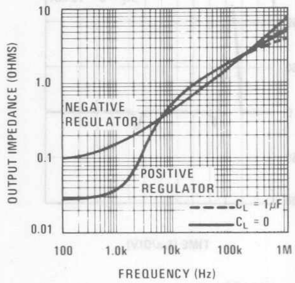
LM126
Line Transient Response



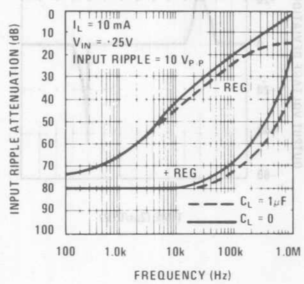
LM125
Ripple Rejection



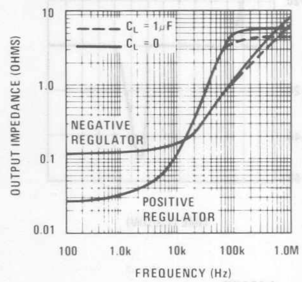
LM125
Output Impedance
vs Frequency



LM126
Ripple Rejection



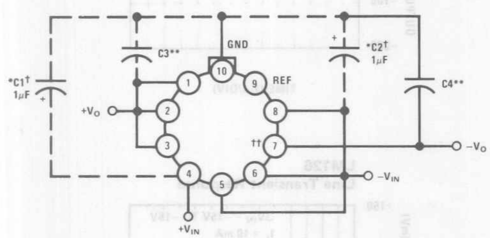
LM126
Output Impedance
vs Frequency



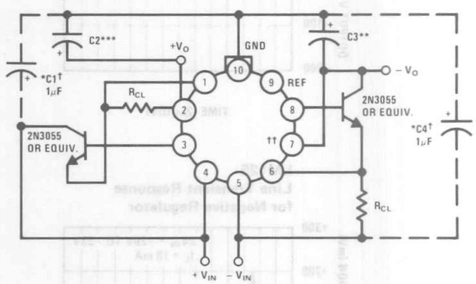
Typical Applications

Note. Metal can (H) packages shown.

Basic Regulator†††



2.0 Amp Boosted Regulator With Current Limit



$$I_{CL} = \frac{\text{CURRENT LIMIT SENSE VOLTAGE (SEE CURVE)}}{R_{CL}}$$

†SOLID TANTALUM

††SHORT PINS 6 AND 7 ON DIP

†††R_{CL} CAN BE ADDED TO THE BASIC REGULATOR BETWEEN PINS 6 AND 5, 1 AND 2 TO REDUCE CURRENT LIMIT.

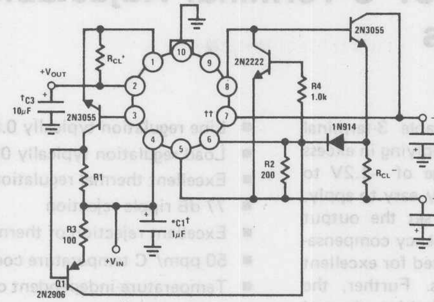
*REQUIRED IF REGULATOR IS LOCATED AN APPRECIABLE DISTANCE FROM POWER SUPPLY FILTER.

**ALTHOUGH NO CAPACITOR IS NEEDED FOR STABILITY, IT DOES HELP TRANSIENT RESPONSE. (IF NEEDED USE 1μF ELECTROLYTIC).

***ALTHOUGH NO CAPACITOR IS NEEDED FOR STABILITY, IT DOES HELP TRANSIENT RESPONSE. (IF NEEDED USE 10μF ELECTROLYTIC).

Typical Applications (cont'd.)

Positive Current Dependent Simultaneous Current Limiting

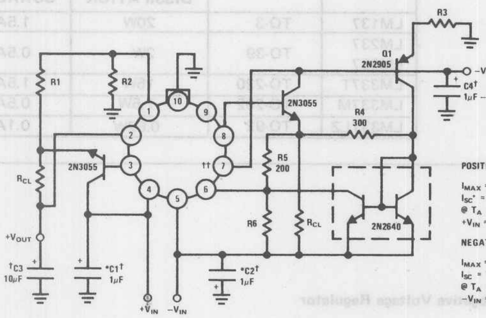


$$I_{CL}^+ = \frac{\frac{V_{SENSE\ NEG}}{2} + V_{BEQ1}}{R1} \qquad R_{CL}^+ = \frac{V_{SENSE}^+}{1.1\, I_{CL}^-}$$

$$I_{CL}^- = \frac{V_{SENSE\ NEG} + V_{DIODE}}{R_{CL}^-}$$

I_{CL}^+ CONTROLS BOTH SIDES OF THE REGULATOR.

Boosted Regulator With Foldback Current Limit



POSITIVE REG.

I_{MAX} = 2.0A
I_{SC} = 750 mA
@ T_A = 25°C
$+V_{IN}$ = +25V

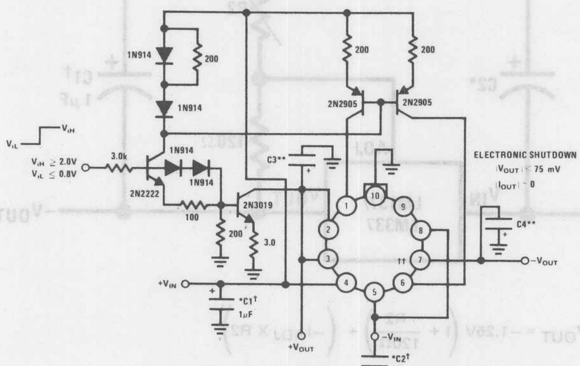
NEGATIVE REG.

I_{MAX} = 2.0A
I_{SC} = 750 mA
@ T_A = 25°C
$-V_{IN}$ = −25V

Resistor Values

	125	126
R1	18	20
R2	310	180
R3	2.4k	1.35k
R6	300	290
R_{CL}	0.7	0.9

Electric Shutdown



ELECTRONIC SHUTDOWN
$|V_{OUT}| \leq 75$ mV
$|I_{OUT}| \sim 0$

†SOLID TANTALUM
††SHORT PINS 6 AND 7 ON DIP
*REQUIRED IF REGULATOR IS LOCATED AN APPRECIABLE DISTANCE FROM POWER SUPPLY FILTER.
**ALTHOUGH NO CAPACITOR IS NEEDED FOR STABILITY, IT DOES HELP TRANSIENT RESPONSE. (IF NEEDED USE 1μF ELECTROLYTIC.)

National Semiconductor

LM137/LM237/LM337 3-Terminal Adjustable Negative Regulators

General Description

The LM137/LM237/LM337 are adjustable 3-terminal negative voltage regulators capable of supplying in excess of −1.5A over an output voltage range of −1.2V to −37V. These regulators are exceptionally easy to apply, requiring only 2 external resistors to set the output voltage and 1 output capacitor for frequency compensation. The circuit design has been optimized for excellent regulation and low thermal transients. Further, the LM137 series features internal current limiting, thermal shutdown and safe-area compensation, making them virtually blowout-proof against overloads.

The LM137/LM237/LM337 serve a wide variety of applications including local on-card regulation, programmable-output voltage regulation or precision current regulation. The LM137/LM237/LM337 are ideal complements to the LM117/LM217/LM317 adjustable positive regulators.

Features

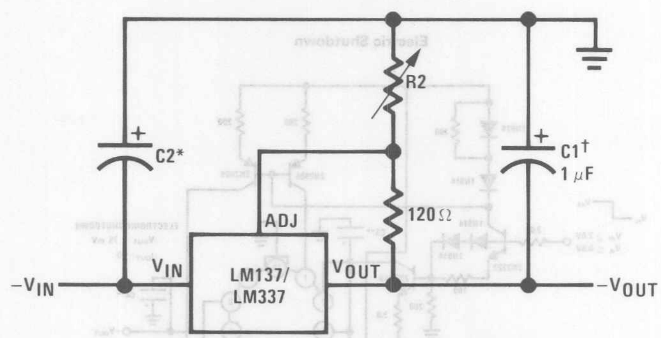
- Output voltage adjustable from −1.2V to −37V
- 1.5A output current guaranteed, −55°C to +150°C
- Line regulation typically 0.01%/V
- Load regulation typically 0.3%
- Excellent thermal regulation, 0.002%/W
- 77 dB ripple rejection
- Excellent rejection of thermal transients
- 50 ppm/°C temperature coefficient
- Temperature-independent current limit
- Internal thermal overload protection
- 100% electrical burn-in
- Standard 3-lead transistor package

LM137 Series Packages and Power Capability

DEVICE	PACKAGE	RATED POWER DISSIPATION	DESIGN LOAD CURRENT
LM137	TO-3	20W	1.5A
LM237 LM337	TO-39	2W	0.5A
LM337T	TO-220	15W	1.5A
LM337M	TO-202	7.5W	0.5A
LM337LZ	TO-92	0.62W	0.1A

Typical Applications

Adjustable Negative Voltage Regulator



$$-V_{OUT} = -1.25V\left(1 + \frac{R2}{120\Omega}\right) + \left(-I_{ADJ} \times R2\right)$$

†C1 = 1 µF solid tantalum or 10 µF aluminum electrolytic required for stability. Output capacitors in the range of 1 µF to 1000 µF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients.

*C2 = 1 µF solid tantalum is required only if regulator is more than 4″ from power-supply filter capacitor

Absolute Maximum Ratings

Power Dissipation	Internally limited
Input—Output Voltage Differential	40V
Operating Junction Temperature Range	
LM137	$-55^{\circ}C$ to $+150^{\circ}C$
LM237	$-25^{\circ}C$ to $+150^{\circ}C$
LM337	$0^{\circ}C$ to $+125^{\circ}C$
Storage Temperature	$-65^{\circ}C$ to $+150^{\circ}C$
Lead Temperature (Soldering, 10 seconds)	$300^{\circ}C$

Preconditioning

Burn-In in Thermal Limit	**100% All Devices**

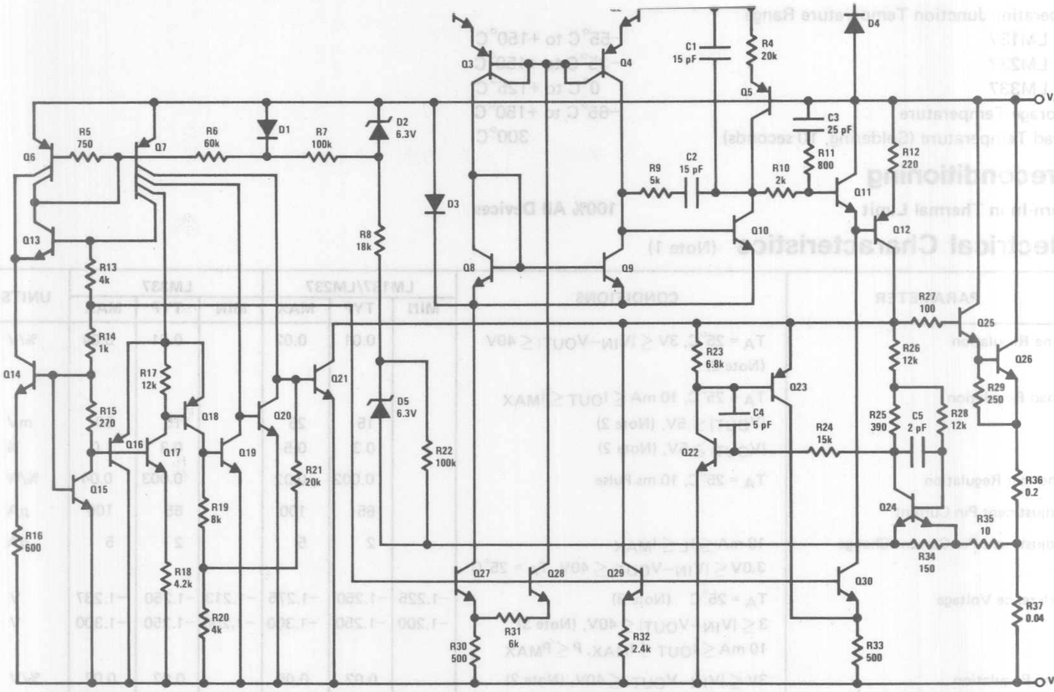
Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	LM137/LM237 MIN	LM137/LM237 TYP	LM137/LM237 MAX	LM337 MIN	LM337 TYP	LM337 MAX	UNITS
Line Regulation	$T_A = 25^{\circ}C$, $3V \leq \|V_{IN}-V_{OUT}\| \leq 40V$ (Note 2)		0.01	0.02		0.01	0.04	%/V
Load Regulation	$T_A = 25^{\circ}C$, $10\ mA \leq I_{OUT} \leq I_{MAX}$							
	$\|V_{OUT}\| \leq 5V$, (Note 2)		15	25		15	50	mV
	$\|V_{OUT}\| \geq 5V$, (Note 2)		0.3	0.5		0.3	1.0	%
Thermal Regulation	$T_A = 25^{\circ}C$, 10 ms Pulse		0.002	0.02		0.003	0.04	%/W
Adjustment Pin Current			65	100		65	100	μA
Adjustment Pin Current Change	$10\ mA \leq I_L \leq I_{MAX}$; $3.0V \leq \|V_{IN}-V_{OUT}\| \leq 40V$, $T_A = 25^{\circ}C$		2	5		2	5	μA
Reference Voltage	$T_A = 25^{\circ}C$ (Note 3)	−1.225	−1.250	−1.275	−1.213	−1.250	−1.287	V
	$3 \leq \|V_{IN}-V_{OUT}\| \leq 40V$, (Note 3); $10\ mA \leq I_{OUT} \leq I_{MAX}$, $P \leq P_{MAX}$	−1.200	−1.250	−1.300	−1.200	−1.250	−1.300	V
Line Regulation	$3V \leq \|V_{IN}-V_{OUT}\| \leq 40V$, (Note 2)		0.02	0.05		0.02	0.07	%/V
Load Regulation	$10\ mA \leq I_{OUT} \leq I_{MAX}$, (Note 2)							
	$\|V_{OUT}\| \leq 5V$		20	50		20	70	mV
	$\|V_{OUT}\| \geq 5V$		0.3	1		0.3	1.5	%
Temperature Stability	$T_{MIN} \leq T_j \leq T_{MAX}$		0.6			0.6		%
Minimum Load Current	$\|V_{IN}-V_{OUT}\| \leq 40V$		2.5	5		2.5	10	mA
	$\|V_{IN}-V_{OUT}\| \leq 10V$		1.2	3		1.5	6	mA
Current Limit	$\|V_{IN}-V_{OUT}\| \leq 15V$							
	K and T Package	1.5	2.2		1.5	2.2		A
	H and P Package	0.5	0.8		0.5	0.8		A
	$\|V_{IN}-V_{OUT}\| = 40V$, $T_j = 25^{\circ}C$							
	K and T Package	0.24	0.4		0.15	0.4		A
	H and P Package	0.15	0.17		0.10	0.17		A
RMS Output Noise, % of V_{OUT}	$T_A = 25^{\circ}C$, $10\ Hz \leq f \leq 10\ kHz$		0.003			0.003		%
Ripple Rejection Ratio	$V_{OUT} = -10V$, f = 120 Hz		60			60		dB
	$C_{ADJ} = 10\ \mu F$	66	77		66	77		dB
Long-Term Stability	$T_A = 125^{\circ}C$, 1000 Hours		0.3	1		0.3	1	%
Thermal Resistance, Junction to Case	H Package		12	15		12	15	°C/W
	K Package		2.3	3		2.3	3	°C/W
	T Package					4		°C/W
	P Package					12		°C/W

Note 1: Unless otherwise specified, these specifications apply $-55^{\circ}C \leq T_j \leq +150^{\circ}C$ for the LM137, $-25^{\circ}C \leq T_j \leq +150^{\circ}C$ for the LM237, $0^{\circ}C \leq T_j \leq +125^{\circ}C$ for the LM337; $V_{IN}-V_{OUT} = 5V$; and $I_{OUT} = 0.1A$ for the TO-39 and TO-202 packages and $I_{OUT} = 0.5A$ for the TO-3 and TO-220 packages. Although power dissipation is internally limited, these specifications are applicable for power dissipations of 2W for the TO-39 and TO-202 and 20W for the TO-3 and TO-220. I_{MAX} is 1.5A for the TO-3 and TO-220 packages, and 0.5A for the TO-202 package and 0.2A for the TO-39 package.

Note 2: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation. Load regulation is measured on the output pin at a point 1/8″ below the base of the TO-3 and TO-39 packages.

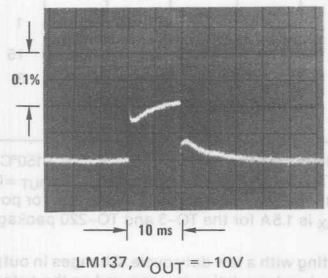
Note 3: Selected devices with tightened tolerance reference voltage available.



Thermal Regulation

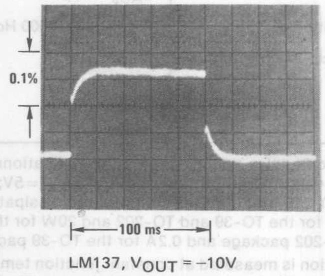
When power is dissipated in an IC, a temperature gradient occurs across the IC chip affecting the individual IC circuit components. With an IC regulator, this gradient can be especially severe since power dissipation is large. Thermal regulation is the effect of these temperature gradients on output voltage (in percentage output change) per Watt of power change in a specified time. Thermal regulation error is independent of electrical regulation or temperature coefficient, and occurs within 5 ms to 50 ms after a change in power dissipation. Thermal regulation depends on IC layout as well as electrical design. The thermal regulation of a voltage regulator is defined as the percentage change of V_{OUT}, per Watt, within the first 10 ms after a step of power is applied. The LM137's specification is 0.02%/W, max.

In *Figure 1*, a typical LM137's output drifts only 3 mV (or 0.03% of V_{OUT} = −10V) when a 10W pulse is applied for 10 ms. This performance is thus well inside the specification limit of 0.02%/W x 10W = 0.2% max. When the 10W pulse is ended, the thermal regulation again shows a 3 mV step as the LM137 chip cools off. Note that the load regulation error of about 8 mV (0.08%) is additional to the thermal regulation error. In *Figure 2*, when the 10W pulse is applied for 100 ms, the output drifts only slightly beyond the drift in the first 10 ms, and the thermal error stays well within 0.1% (10 mV).



LM137, V_{OUT} = −10V
$V_{IN}-V_{OUT}$ = −40V
I_L = 0A → 0.25A → 0A
Vertical sensitivity, 5 mV/div

FIGURE 1

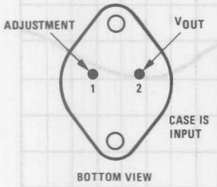


LM137, V_{OUT} = −10V
$V_{IN}-V_{OUT}$ = −40V
I_L = 0A → 0.25A → 0A
Horizontal sensitivity, 20 ms/div

FIGURE 2

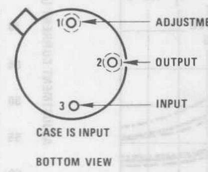
Connection Diagrams

TO-3
Metal Can Package



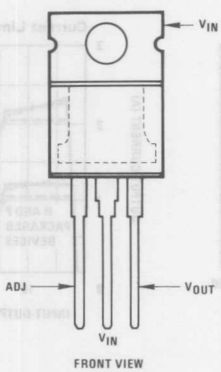
Order Number:
LM137K STEEL
LM237K STEEL
LM337K STEEL
See Package K02A

TO-39
Metal Can Package



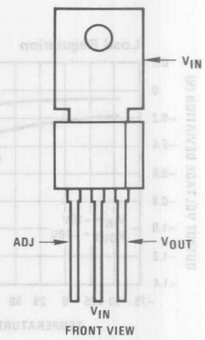
Order Number:
LM137H
LM237H
LM337H
See Package H03B

TO-220
Plastic Package



Order Number:
LM337T
See Package T03B

TO-202
Plastic Package

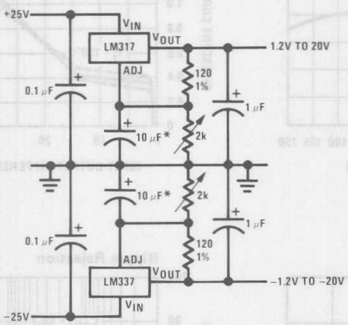


Order Number:
LM337MP
See Package P03A

For Tab Bend TO-202
Order Number:
LM337MP
See Package P03E

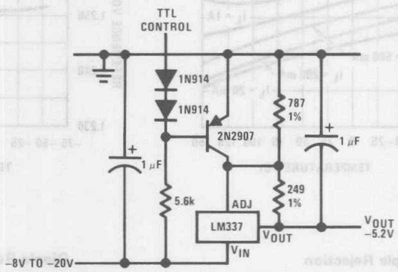
Typical Applications (Continued)

Adjustable Lab Voltage Regulator



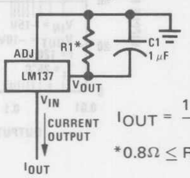
*The 10 μF capacitors are optional to improve ripple rejection

−5.2V Regulator with Electronic Shutdown*



*Minimum output ≅ −1.3V when control input is low

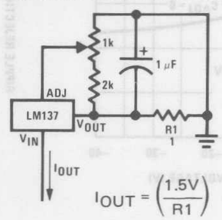
Current Regulator



$I_{OUT} = \dfrac{1.250V}{R1}$

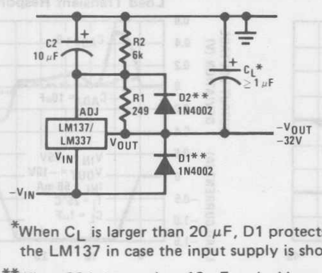
$*0.8\Omega \leq R1 \leq 120\Omega$

Adjustable Current Regulator



$I_{OUT} = \left(\dfrac{1.5V}{R1}\right)$ ±15% adjustable

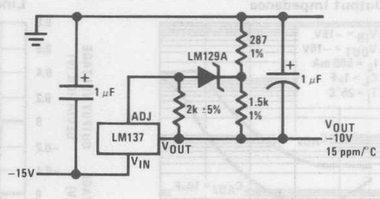
Negative Regulator with Protection Diodes



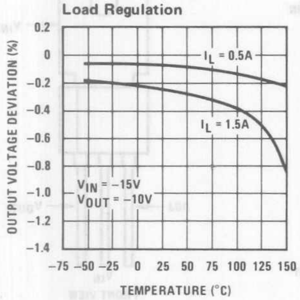
*When C_L is larger than 20 μF, D1 protects the LM137 in case the input supply is shorted

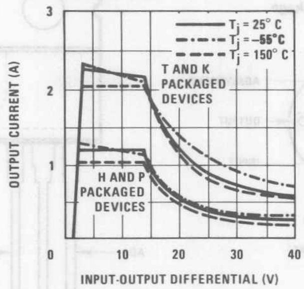
**When C2 is larger than 10 μF and $-V_{OUT}$ is larger than −25V, D2 protects the LM137 in case the output is shorted

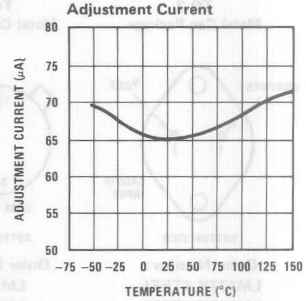
High Stability −10V Regulator

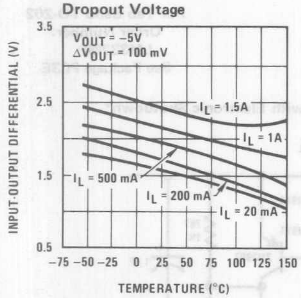


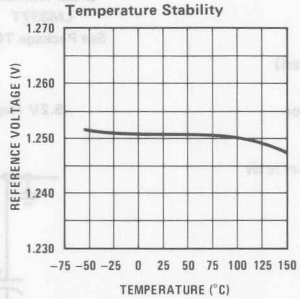
Typical Performance Characteristics (K Steel and T Packages)

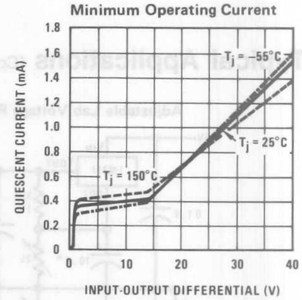
Load Regulation


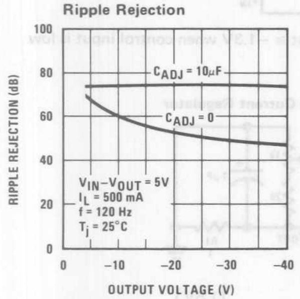
Current Limit


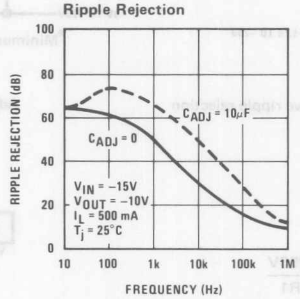
Adjustment Current


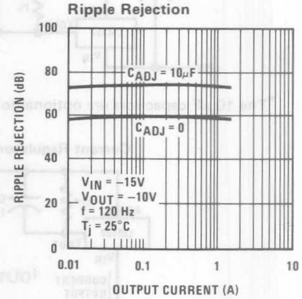
Dropout Voltage


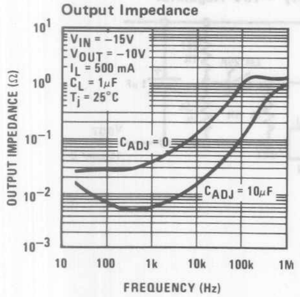
Temperature Stability


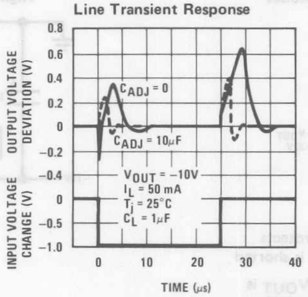
Minimum Operating Current


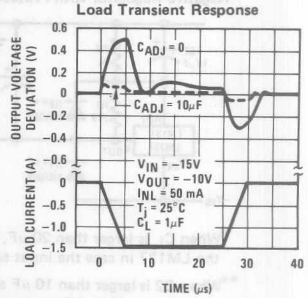
Ripple Rejection


Ripple Rejection


Ripple Rejection


Output Impedance


Line Transient Response


Load Transient Response


National Semiconductor

Voltage Regulators

LM137HV/LM237HV/LM337HV 3-Terminal Adjustable Negative Regulators (High Voltage)

General Description

The LM137HV/LM237HV/LM337HV are adjustable 3-terminal negative voltage regulators capable of supplying in excess of −1.5A over an output voltage range of −1.2V to −47V. These regulators are exceptionally easy to apply, requiring only 2 external resistors to set the output voltage and 1 output capacitor for frequency compensation. The circuit design has been optimized for excellent regulation and low thermal transients. Further, the LM137HV series features internal current limiting, thermal shutdown and safe-area compensation, making them virtually blowout-proof against overloads.

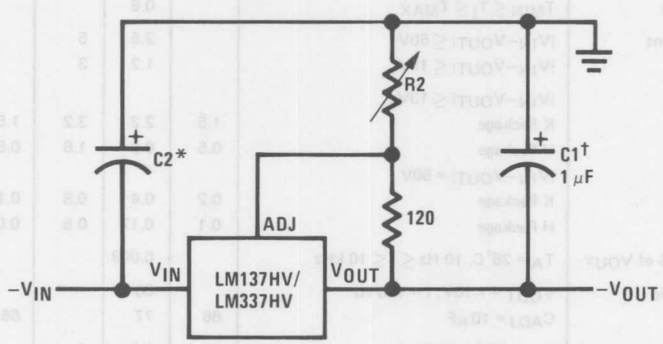
The LM137HV/LM237HV/LM337HV serve a wide variety of applications including local on-card regulation, programmable-output voltage regulation or precision current regulation. The LM137HV/LM237HV/LM337HV are ideal complements to the LM117HV/LM217HV/LM317HV adjustable positive regulators.

Features

- Output voltage adjustable from −1.2V to −47V
- 1.5A output current guaranteed, −55°C to +150°C
- Line regulation typically 0.01%/V
- Load regulation typically 0.3%
- Excellent thermal regulation, 0.002%/W
- 77 dB ripple rejection
- Excellent rejection of thermal transients
- 50 ppm/°C temperature coefficient
- Temperature-independent current limit
- Internal thermal overload protection
- 100% electrical burn-in
- Standard 3-lead transistor package

Typical Applications

Adjustable Negative Voltage Regulator



$$-V_{OUT} = -1.25V\left(1 + \frac{R2}{120\Omega}\right)$$

†C1 = 1 μF solid tantalum or 10 μF aluminum electrolytic required for stability. Output capacitors in the range of 1 μF to 1000 μF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients.

*C2 = 1 μF solid tantalum is required only if regulator is more than 4" from power-supply filter capacitor

Operating Junction Temperature Range	
LM137HV	−55°C to +150°C
LM237HV	−25°C to +150°C
LM337HV	0°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Preconditioning

Burn-In in Thermal Limit **100% All Devices**

Electrical Characteristics (Note 1)

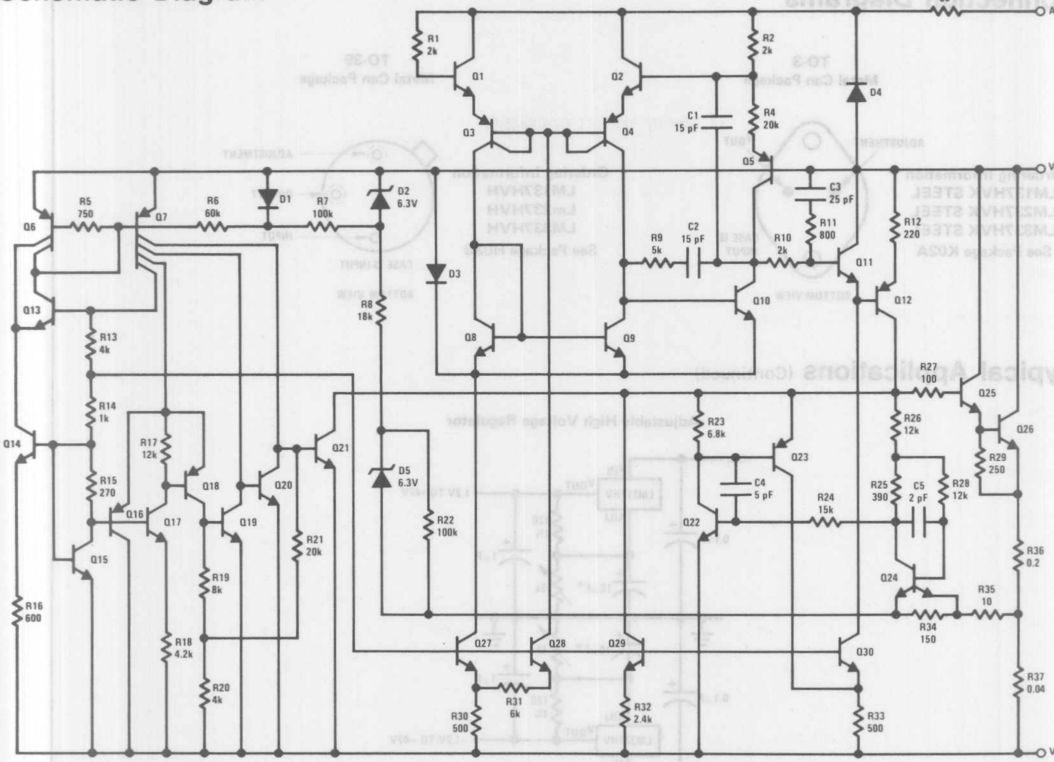
PARAMETER	CONDITIONS	LM137HV/LM237HV MIN	TYP	MAX	LM337HV MIN	TYP	MAX	UNITS
Line Regulation	$T_A = 25°C$, $3V \le \lvert V_{IN} - V_{OUT} \rvert \le 50V$, (Note 2)		0.01	0.02		0.01	0.04	%/V
Load Regulation	$T_A = 25°C$, $10\ mA \le I_{OUT} \le I_{MAX}$							
	$\lvert V_{OUT} \rvert \le 5V$, (Note 2)		15	25		15	50	mV
	$\lvert V_{OUT} \rvert \ge 5V$, (Note 2)		0.3	0.5		0.3	1.0	%
Thermal Regulation	$T_A = 25°C$, 10 ms Pulse		0.002	0.02		0.003	0.04	%/W
Adjustment Pin Current			65	100		65	100	μA
Adjustment Pin Current Change	$10\ mA \le I_L \le I_{MAX}$		2	5		2	5	μA
	$2.5V \le \lvert V_{IN} - V_{OUT} \rvert \le 50V$, $T_A = 25°C$		3	6		3	6	μA
Reference Voltage	$T_A = 25°C$, (Note 3)	−1.225	−1.250	−1.275	−1.213	−1.250	−1.287	V
	$3 \le \lvert V_{IN} - V_{OUT} \rvert \le 50V$, (Note 3) $10\ mA \le I_{OUT} \le I_{MAX}$, $P \le P_{MAX}$	−1.200	−1.250	−1.300	−1.200	−1.250	−1.300	V
Line Regulation	$3V \le \lvert V_{IN} - V_{OUT} \rvert \le 50V$, (Note 2)		0.02	0.05		0.02	0.07	%/V
Load Regulation	$10\ mA \le I_{OUT} \le I_{MAX}$, (Note 2)							
	$\lvert V_{OUT} \rvert \le 5V$		20	50		20	70	mV
	$\lvert V_{OUT} \rvert \ge 5V$		0.3	1		0.3	1.5	%
Temperature Stability	$T_{MIN} \le T_j \le T_{MAX}$		0.6			0.6		%
Minimum Load Current	$\lvert V_{IN} - V_{OUT} \rvert \le 50V$		2.5	5		2.5	10	mA
	$\lvert V_{IN} - V_{OUT} \rvert \le 10V$		1.2	3		1.5	6	mA
Current Limit	$\lvert V_{IN} - V_{OUT} \rvert \le 13V$							
	K Package	1.5	2.2	3.2	1.5	2.2	3.5	A
	H Package	0.5	0.8	1.6	0.5	0.8	1.8	A
	$\lvert V_{IN} - V_{OUT} \rvert = 50V$							
	K Package	0.2	0.4	0.8	0.1	0.4	0.8	A
	H Package	0.1	0.17	0.5	0.050	0.17	0.5	A
RMS Output Noise, % of V_{OUT}	$T_A = 25°C$, $10\ Hz \le f \le 10\ kHz$		0.003			0.003		%
Ripple Rejection Ratio	$V_{OUT} = -10V$, f = 120 Hz		60			60		dB
	$C_{ADJ} = 10\ \mu F$	66	77		66	77		dB
Long-Term Stability	$T_A = 125°C$, 1000 Hours		0.3	1		0.3	1	%
Thermal Resistance, Junction	H Package		12	15		12	15	°C/W
to Case	K Package		2.3	3		2.3	3	°C/W

Note 1: Unless otherwise specified, these specifications apply $-55°C \le T_j \le +150°C$ for the LM137HV, $-25°C \le T_j \le +150°C$ for the LM237HV, $0°C \le T_j \le +125°C$ for the LM337HV; $V_{IN} - V_{OUT} = 5V$; and $I_{OUT} = 0.1A$ for the TO-39 package and $I_{OUT} = 0.5A$ for the TO-3 package. Although power dissipation is internally limited, these specifications are applicable for power dissipations of 2W for the TO-39 and 20W for the TO-3. I_{MAX} is 1.5A for the TO-3 package and 0.2A for the TO-39 package.

Note 2: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation. Load regulation is measured on the output pin at a point 1/8″ below the base of the TO-3 and TO-39 packages.

Note 3: Selected devices with tightened tolerance reference voltage available.

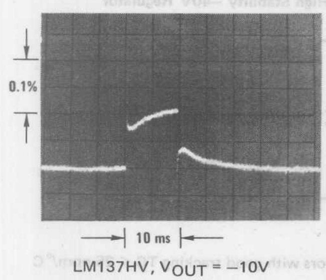
Schematic Diagram



Thermal Regulation

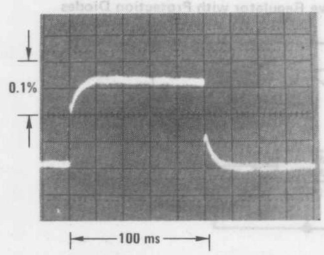
When power is dissipated in an IC, a temperature gradient occurs across the IC chip affecting the individual IC circuit components. With an IC regulator, this gradient can be especially severe since power dissipation is large. Thermal regulation is the effect of these temperature gradients on output voltage (in percentage output change) per Watt of power change in a specified time. Thermal regulation error is independent of electrical regulation or temperature coefficient, and occurs within 5 ms to 50 ms after a change in power dissipation. Thermal regulation depends on IC layout as well as electrical design. The thermal regulation of a voltage regulator is defined as the percentage change of V_{OUT}, per Watt, within the first 10 ms after a step of power is applied. The LM137HV's specification is 0.02%/W, max.

In *Figure 1*, a typical LM137HV's output drifts only 3 mV (or 0.03% of $V_{OUT} = -10V$) when a 10W pulse is applied for 10 ms. This performance is thus well inside the specification limit of 0.02%/W x 10W = 0.2% max. When the 10W pulse is ended, the thermal regulation again shows a 3 mV step as the LM137HV chip cools off. Note that the load regulation error of about 8 mV (0.08%) is additional to the thermal regulation error. In *Figure 2*, when the 10W pulse is applied for 100 ms, the output drifts only slightly beyond the drift in the first 10 ms, and the thermal error stays well within 0.1% (10 mV).



LM137HV, $V_{OUT} = -10V$
$V_{IN}-V_{OUT} = -40V$
$I_L = 0A \rightarrow 0.25A \rightarrow 0A$
Vertical sensitivity, 5 mV/div

FIGURE 1

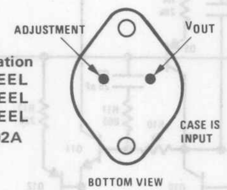


LM137HV, $V_{OUT} = -10V$
$V_{IN}-V_{OUT} = -40V$
$I_L = 0A \rightarrow 0.25A \rightarrow 0A$
Horizontal sensitivity, 20 ms/div

FIGURE 2

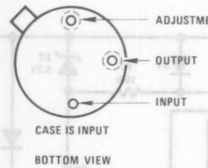
Connection Diagrams

TO-3 Metal Can Package



Ordering Information
LM137HVK STEEL
LM237HVK STEEL
LM337HVK STEEL
See Package K02A

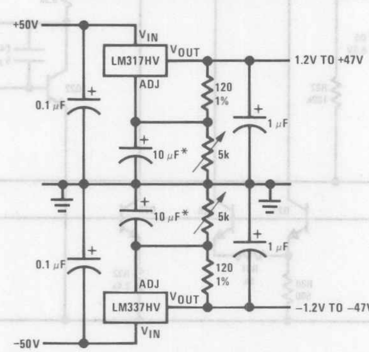
TO-39 Metal Can Package



Ordering Information
LM137HVH
Lm237HVH
LM337HVH
See Package H03B

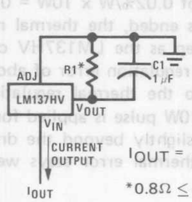
Typical Applications (Continued)

Adjustable High Voltage Regulator



*The 10 μF capacitors are optional to improve ripple rejection

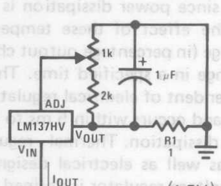
Current Regulator



$$I_{OUT} = \frac{1.250V}{R1}$$

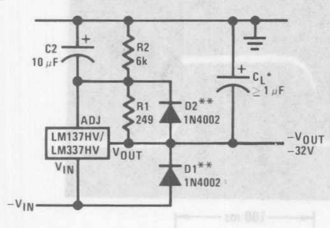
$*0.8\Omega \leq R1 \leq 120\Omega$

Adjustable Current Regulator



$$I_{OUT} = \left(\frac{1.5V}{R1}\right) \pm 15\% \text{ adjustable}$$

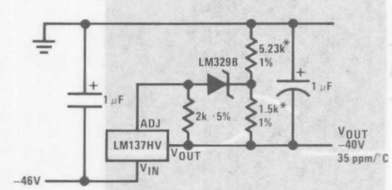
Negative Regulator with Protection Diodes



*When C_L is larger than 20 μF, D1 protects the LM137HV is case the input supply is shorted

**When C2 is larger than 10 μF and $-V_{OUT}$ is larger than −25V, D2 protects the LM137HV in case the output is shorted

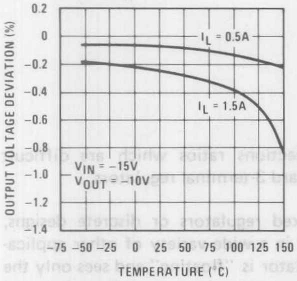
High Stability −40V Regulator



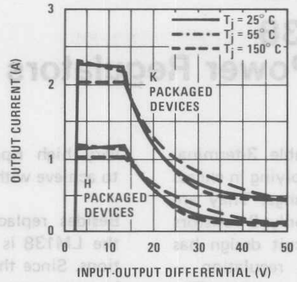
*Use resistors with good tracking TC < 25 ppm/°C

Typical Performance Characteristics (H and K-STEEL Package)

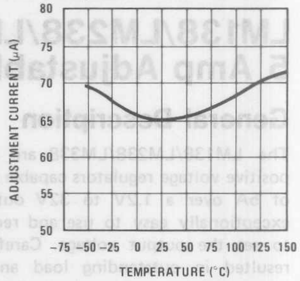
Load Regulation



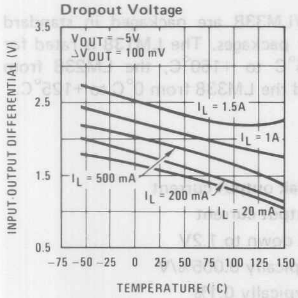
Current Limit



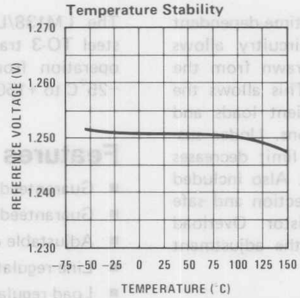
Adjustment Current



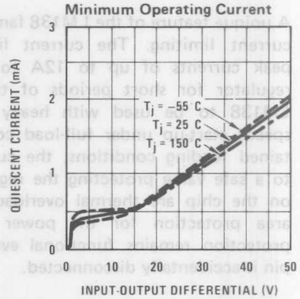
Dropout Voltage



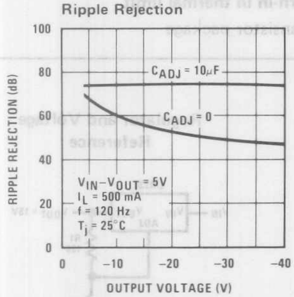
Temperature Stability



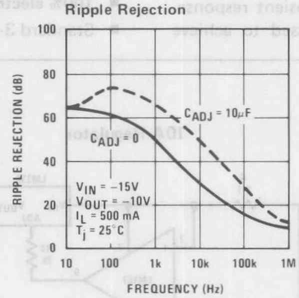
Minimum Operating Current



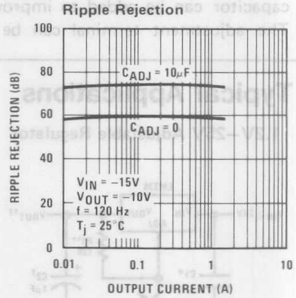
Ripple Rejection



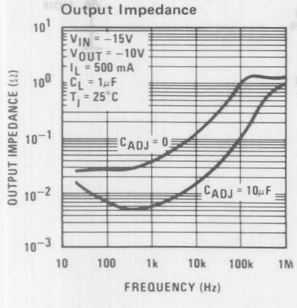
Ripple Rejection



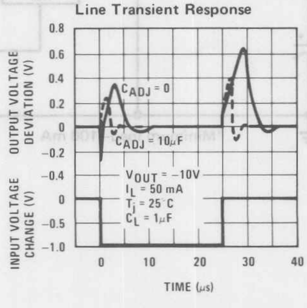
Ripple Rejection



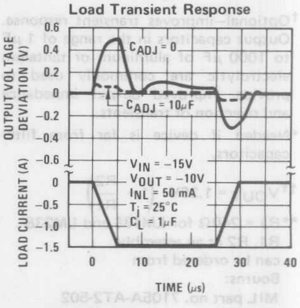
Output Impedance



Line Transient Response



Load Transient Response



LM138/LM238/LM338 5 Amp Adjustable Power Regulators

General Description

The LM138/LM238/LM338 are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 5A over a 1.2V to 32V output range. They are exceptionally easy to use and require only 2 resistors to set the output voltage. Careful circuit design has resulted in outstanding load and line regulation — comparable to many commercial power supplies. The LM138 family is supplied in a standard 3-lead transistor package.

A unique feature of the LM138 family is time-dependent current limiting. The current limit circuitry allows peak currents of up to 12A to be drawn from the regulator for short periods of time. This allows the LM138 to be used with heavy transient loads and speeds start-up under full-load conditions. Under sustained loading conditions, the current limit decreases to a safe value protecting the regulator. Also included on the chip are thermal overload protection and safe area protection for the power transistor. Overload protection remains functional even if the adjustment pin is accidentally disconnected.

Normally, no capacitors are needed unless the device is situated far from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejections ratios which are difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators or discrete designs, the LM138 is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input to output differential is not exceeded.

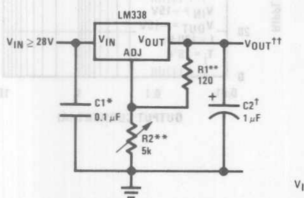
The LM138/LM238/LM338 are packaged in standard steel TO-3 transistor packages. The LM138 is rated for operation from −55°C to +150°C, the LM238 from −25°C to +150°C and the LM338 from 0°C to +125°C.

Features

- Guaranteed 7A peak output current
- Guaranteed 5A output current
- Adjustable output down to 1.2V
- Line regulation typically 0.005%/V
- Load regulation typically 0.1%
- Guaranteed thermal regulation
- Current limit constant with temperature
- **100% electrical burn-in in thermal limit**
- Standard 3-lead transistor package

Typical Applications

1.2V–25V Adjustable Regulator



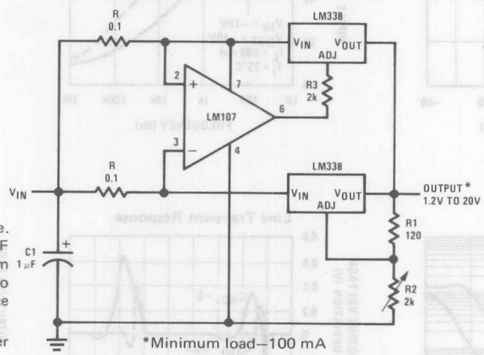
†Optional—improves transient response. Output capacitors in the range of 1 μF to 1000 μF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients.

*Needed if device is far from filter capacitors.

$$^{\dagger\dagger}V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right)$$

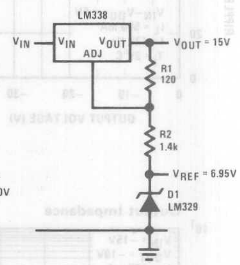
**R1 = 240Ω for LM138 and LM238
R1, R2 as an assembly can be ordered from Bourns:
MIL part no. 7105A-AT2-502
COMM part no. 7105A-AT7-502

10A Regulator



*Minimum load—100 mA

Regulator and Voltage Reference



Absolute Maximum Ratings

Power Dissipation	Internally limited
Input–Output Voltage Differential	35V
Operating Junction Temperature Range	
LM138	−55°C to +150°C
LM238	−25°C to +150°C
LM338	0°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Preconditioning

Burn-In in Thermal Limit **All Devices 100%**

Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	LM138/LM238			LM338			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Line Regulation	$T_A = 25°C$, $3V \leq V_{IN} - V_{OUT} \leq 35V$, (Note 2)		0.005	0.01		0.005	0.03	%/V
Load Regulation	$T_A = 25°C$, $10\ mA \leq I_{OUT} \leq 5A$							
	$V_{OUT} \leq 5V$, (Note 2)		5	15		5	25	mV
	$V_{OUT} \geq 5V$, (Note 2)		0.1	0.3		0.1	0.5	%
Thermal Regulation	Pulse = 20 ms		0.002	0.01		0.002	0.02	%/W
Adjustment Pin Current			45	100		45	100	μA
Adjustment Pin Current Change	$10\ mA \leq I_L \leq 5A$ $3V \leq (V_{IN} - V_{OUT}) \leq 35V$		0.2	5		0.2	5	μA
Reference Voltage	$3 \leq (V_{IN} - V_{OUT}) \leq 35V$, (Note 3) $10\ mA \leq I_{OUT} \leq 5A$, $P \leq 50W$	1.19	1.24	1.29	1.19	1.24	1.29	V
Line Regulation	$3V \leq V_{IN} - V_{OUT} \leq 35V$, (Note 2)		0.02	0.04		0.02	0.06	%/V
Load Regulation	$10\ mA \leq I_{OUT} \leq 5A$, (Note 2)							
	$V_{OUT} \leq 5V$		20	30		20	50	mV
	$V_{OUT} \geq 5V$		0.3	0.6		0.3	1.0	%
Temperature Stability	$T_{MIN} \leq T_j \leq T_{MAX}$		1			1		%
Minimum Load Current	$V_{IN} - V_{OUT} = 35V$		3.5	5		3.5	10	mA
Current Limit	$V_{IN} - V_{OUT} \leq 10V$							
	DC	5.0	8		5.0	8		A
	0.5 ms Peak	7	12		7	12		A
	$V_{IN} - V_{OUT} = 30V$		1			1		A
RMS Output Noise, % of V_{OUT}	$T_A = 25°C$, $10\ Hz \leq f \leq 10\ kHz$		0.003			0.003		%
Ripple Rejection Ratio	$V_{OUT} = 10V$, f = 120 Hz		60			60		dB
	$C_{ADJ} = 10\ \mu F$	60	75		60	75		dB
Long Term Stability	$T_A = 125°C$		0.3	1		0.3	1	%
Thermal Resistance, Junction to Case	K Package			1.0			1.0	°C/W

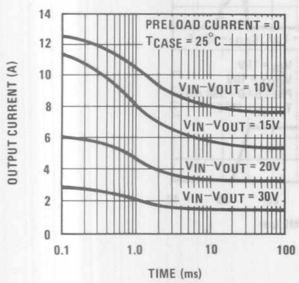
Note 1: Unless otherwise specified, these specifications apply $-55°C \leq T_j \leq +150°C$ for the LM138, $-25°C \leq T_j \leq +150°C$ for the LM238 and $0°C \leq T_j \leq +125°C$ for the LM338, $V_{IN} - V_{OUT} = 5V$ and $I_{OUT} = 2.5A$. Although power dissipation is internally limited, these specifications are applicable for power dissipations up to 50W.

Note 2: Regulation is measured at constant junction temperature. Changes in output voltage due to heating effects are taken into account separately by thermal regulation.

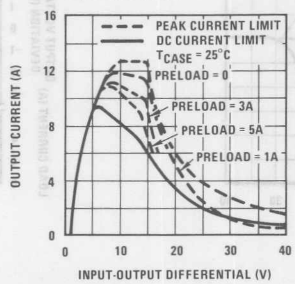
Note 3: Selected devices with tightened tolerance reference voltage available.

Typical Performance Characteristics

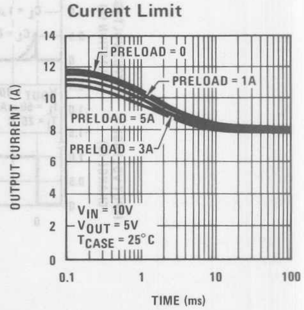
Current Limit



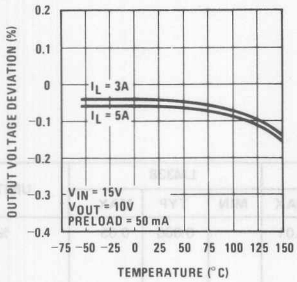
Current Limit

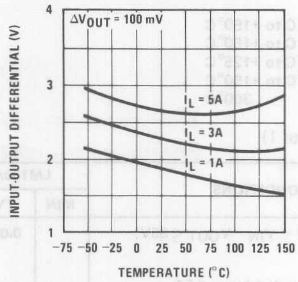


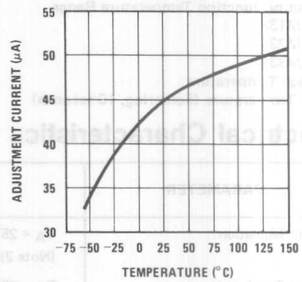
Current Limit

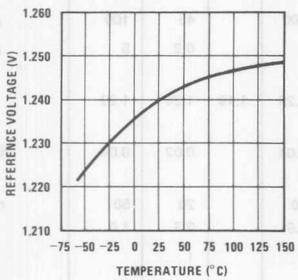


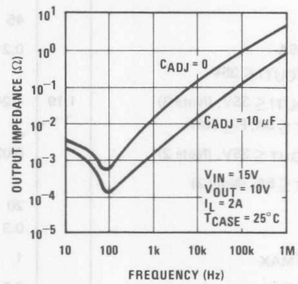
Typical Performance Characteristics (Continued)

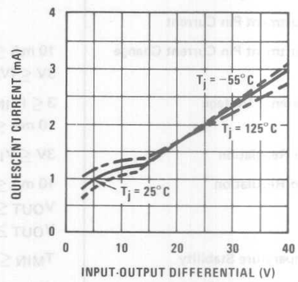
Load Regulation


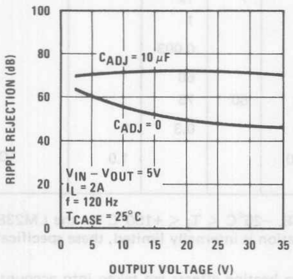
Dropout Voltage


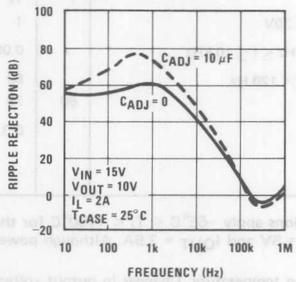
Adjustment Current


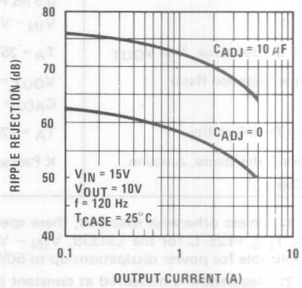
Temperature Stability


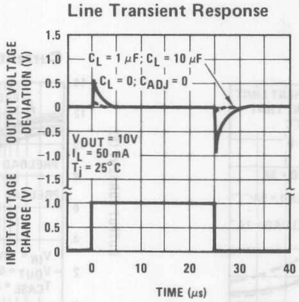
Output Impedance


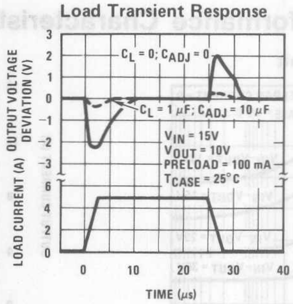
Minimum Operating Current


Ripple Rejection


Ripple Rejection


Ripple Rejection


Line Transient Response


Load Transient Response


Application Hints

In operation, the LM138 develops a nominal 1.25V reference voltage, V_{REF}, between the output and adjustment terminal. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R2, giving an output voltage of

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}R2.$$

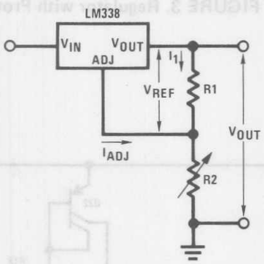


FIGURE 1

Since the 50 μA current from the adjustment terminal represents an error term, the LM138 was designed to minimize I_{ADJ} and make it very constant with line and load changes. To do this, all quiescent operating current is returned to the output establishing a minimum load current requirement. If there is insufficient load on the output, the output will rise.

External Capacitors

An input bypass capacitor is recommended. A 0.1 μF disc or 1 μF solid tantalum on the input is suitable input bypassing for almost all applications. The device is more sensitive to the absence of input bypassing when adjustment or output capacitors are used but the above values will eliminate the possibility of problems.

The adjustment terminal can be bypassed to ground on the LM138 to improve ripple rejection. This bypass capacitor prevents ripple from being amplified as the output voltage is increased. With a 10 μF bypass capacitor 75 dB ripple rejection is obtainable at any output level. Increases over 20 μF do not appreciably improve the ripple rejection at frequencies above 120 Hz. If the bypass capacitor is used, it is sometimes necessary to include protection diodes to prevent the capacitor from discharging through internal low current paths and damaging the device.

In general, the best type of capacitors to use are solid tantalum. Solid tantalum capacitors have low impedance even at high frequencies. Depending upon capacitor construction, it takes about 25 μF in aluminum electrolytic to equal 1 μF solid tantalum at high frequencies. Ceramic capacitors are also good at high frequencies, but some types have a large decrease in capacitance at frequencies around 0.5 MHz. For this reason, 0.01 μF disc may seem to work better than a 0.1 μF disc as a bypass.

Although the LM138 is stable with no outout capacitors, like any feedback circuit, certain values of external capacitance can cause excessive ringing. This occurs with values between 500 pF and 5000 pF. A 1 μF solid tantalum (or 25 μF aluminum electrolytic) on the output swamps this effect and insures stability.

Load Regulation

The LM138 is capable of providing extremely good load regulation but a few precautions are needed to obtain maximum performance. The current set resistor connected between the adjustment terminal and the output terminal (usually 240Ω) should be tied directly to the output of the regulator rather than near the load. This eliminates line drops from appearing effectively in series with the reference and degrading regulation. For example, a 15V regulator with 0.05Ω resistance between the regulator and load will have a load regulation due to line resistance of 0.05Ω x I_L. If the set resistor is connected near the load the effective line resistance will be 0.05Ω (1 + R2/R1) or in this case, 11.5 times worse.

Figure 2 shows the effect of resistance between the regulator and 240Ω set resistor.

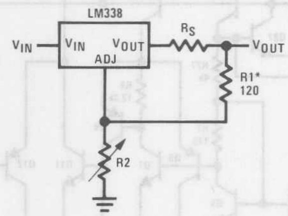


FIGURE 2. Regulator with Line Resistance in Output Lead

With the TO-3 package, it is easy to minimize the resistance from the case to the set resistor, by using 2 separate leads to the case. The ground of R2 can be returned near the ground of the load to provide remote ground sensing and improve load regulation.

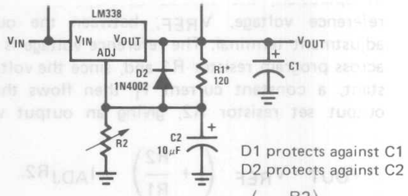
Protection Diodes

When external capacitors are used with *any* IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator. Most 20 μF capacitors have low enough internal series resistance to deliver 20A spikes when shorted. Although the surge is short, there is enough energy to damage parts of the IC.

When an output capacitor is connected to a regulator and the input is shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage of the regulator, and the rate of decrease of V_{IN}. In the LM138 this discharge path is through a large junction that is able to sustain 25A surge with no problem. This is not true of other types of positive

regulators. For output capacitors of 100 μF or less at output of 15V or less, there is no need to use diodes.

The bypass capacitor on the adjustment terminal can discharge through a low current junction. Discharge occurs when *either* the input or output is shorted. Internal to the LM138 is a 50Ω resistor which limits the peak discharge current. No protection is needed for output voltages of 25V or less and 10 μF capacitance. *Figure 3* shows an LM138 with protection diodes included for use with outputs greater than 25V and high values of output capacitance.

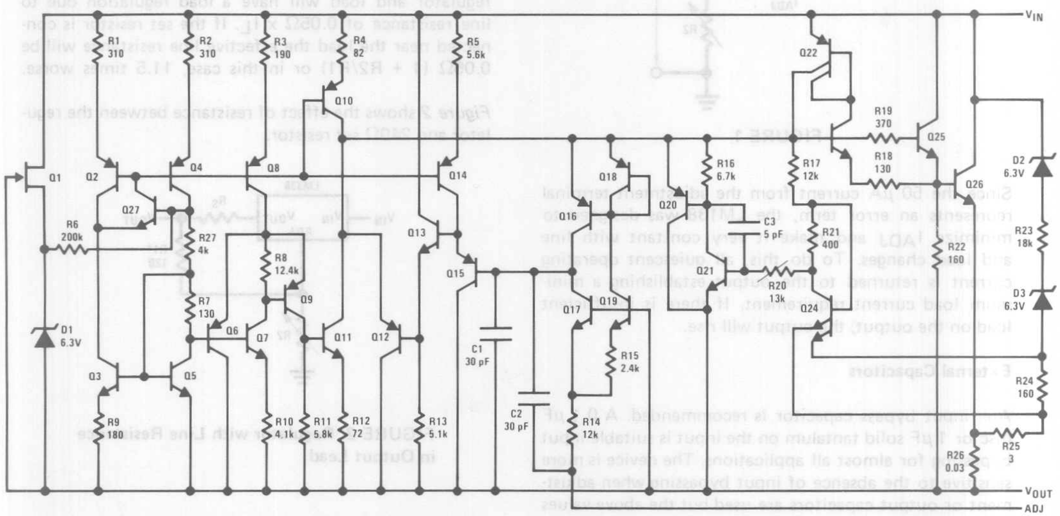


$$V_{OUT} = 1.25V \left(1 + \frac{R2}{R1}\right) + R2I_{ADJ}$$

*R1 = 240Ω for LM138 and LM238

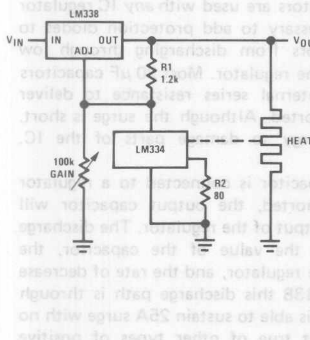
FIGURE 3. Regulator with Protection Diodes

Schematic Diagram

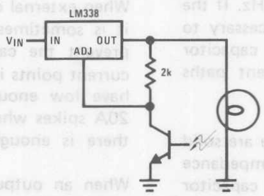


Typical Applications (Continued)

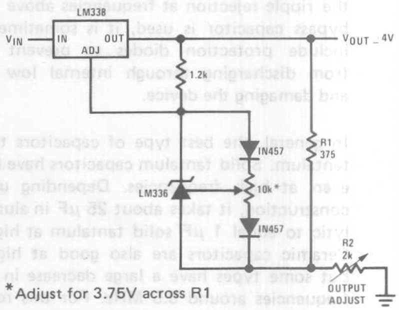
Temperature Controller



Light Controller



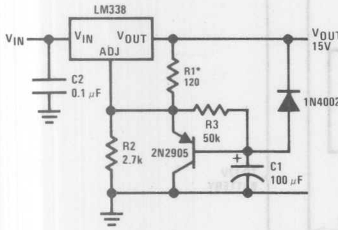
Precision Power Regulator with Low Temperature Coefficient



*Adjust for 3.75V across R1

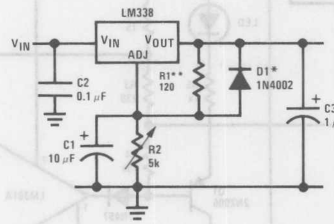
Typical Applications (Continued)

Slow Turn-ON 15V Regulator



*R1 = 240Ω for LM138 and LM238

Adjustable Regulator with Improved Ripple Rejection

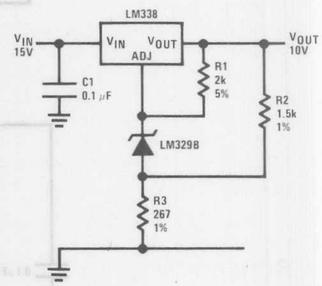


†Solid tantalum

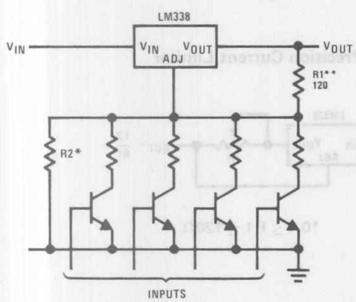
*Discharges C1 if output is shorted to ground

**R1 = 240Ω for LM138 and LM238

High Stability 10V Regulator



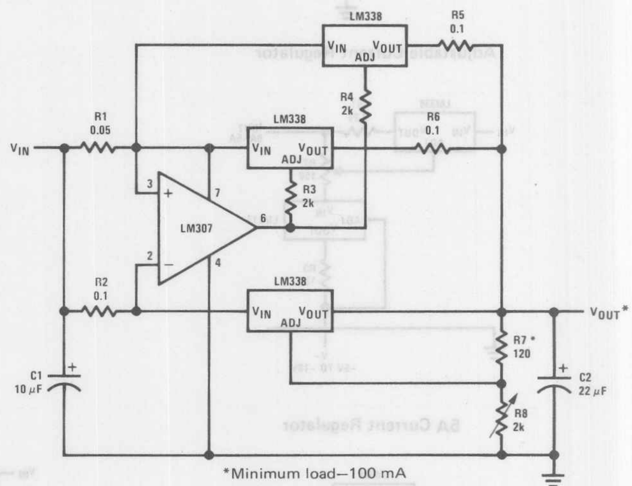
Digitally Selected Outputs



*Sets maximum V_{OUT}

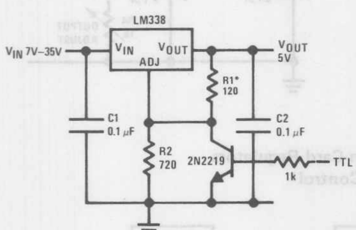
**R1 = 240Ω for LM138 and LM238

15A Regulator



*Minimum load—100 mA

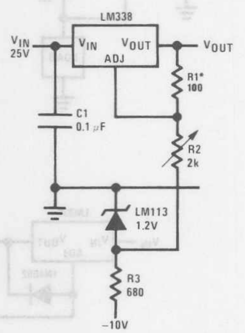
5V Logic Regulator with Electronic Shutdown**



*R1 = 240Ω for LM138 or LM238

**Minimum output ≈ 1.2V

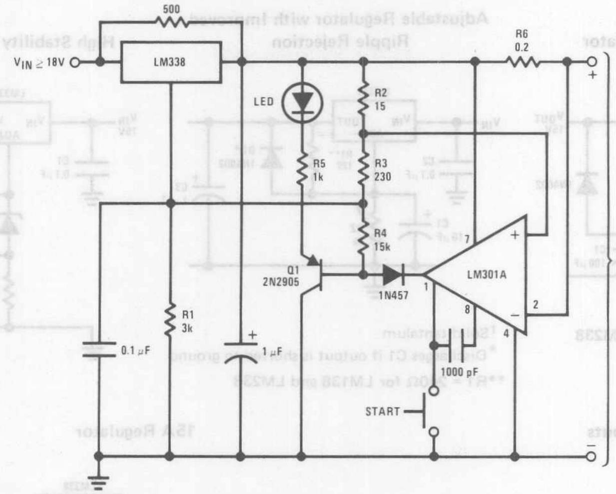
0 to 22V Regulator



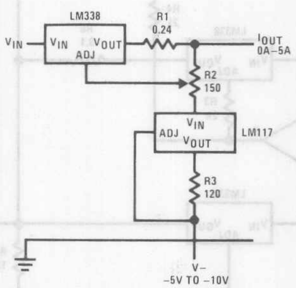
*R1=240Ω, R2 = 5k for LM138 and LM238

Typical Applications (Continued)

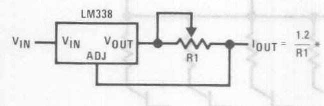
12V Battery Charger



Adjustable Current Regulator

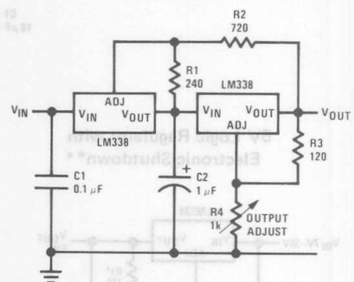


Precision Current Limiter

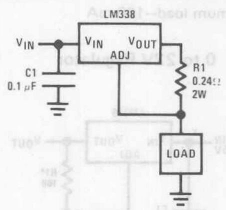


$^*0.4 \leq R1 \leq 120\Omega$

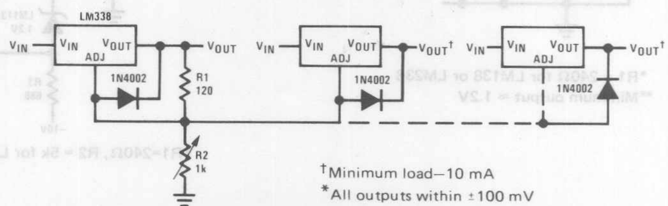
Tracking Preregulator



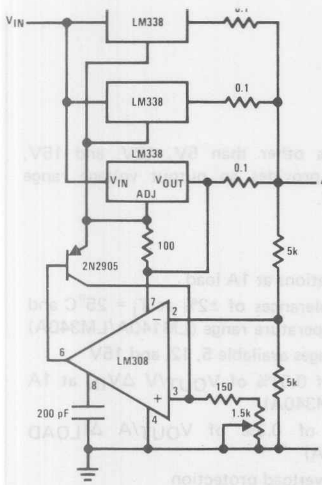
5A Current Regulator

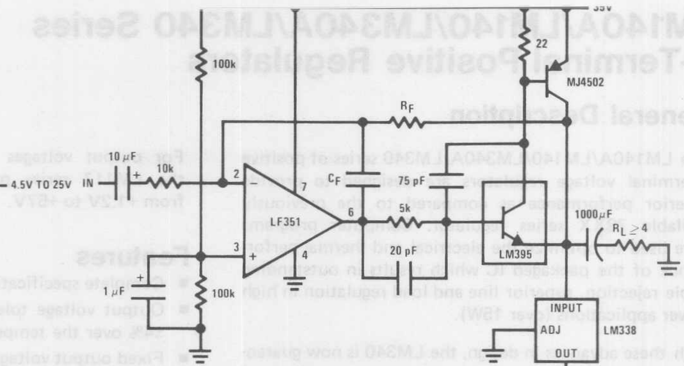


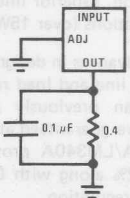
Adjusting Multiple On-Card Regulators with Single Control*



†Minimum load—10 mA
*All outputs within ±100 mV

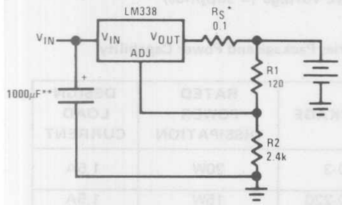






$A_V = 1$, $R_F = 10k$, $C_F = 100\ pF$
$A_V = 10$, $R_F = 100k$, $C_F = 10\ pF$
Bandwidth $\geq 100\ kHz$
Distortion $\leq 0.1\%$

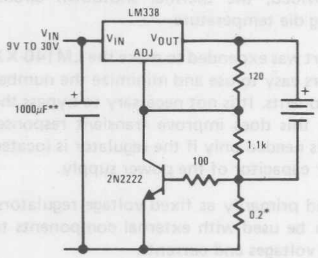
Simple 12V Battery Charger



*R_S—sets output impedance of charger $Z_{OUT} = R_S \left(1 + \frac{R2}{R1}\right)$ Use of R_S allows low charging rates with fully charged battery.

**The 1000 µF is recommended to filter out input transients

Current Limited 6V Charger

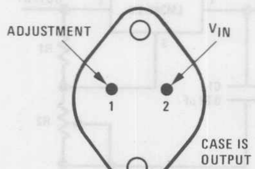


*Sets max charge current to 3A

**The 1000 µF is recommended to filter out input transients

Connection Diagram

Metal Can Package



BOTTOM VIEW

Order Number
LM138K STEEL
LM238K STEEL
LM338K STEEL
See NS Package K02A

National Semiconductor

LM140A/LM140/LM340A/LM340 Series 3-Terminal Positive Regulators

General Description

The LM140A/LM140/LM340A/LM340 series of positive 3-terminal voltage regulators are designed to provide superior performance as compared to the previously available 78XX series regulator. Computer programs were used to optimize the electrical and thermal performance of the packaged IC which results in outstanding ripple rejection, superior line and load regulation in high power applications (over 15W).

With these advances in design, the LM340 is now guaranteed to have line and load regulation that is a factor of 2 better than previously available devices. Also, all parameters are guaranteed at 1A vs 0.5A output current. The LM140A/LM340A provide tighter output voltage tolerance, ±2% along with 0.01%/V line regulation and 0.3%/A load regulation.

Current limiting is included to limit peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over limiting die temperature.

Considerable effort was expended to make the LM140-XX series of regulators easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

The entire LM140A/LM140/LM340A/LM340 series of regulators is available in the metal TO-3 power package and the LM340A/LM340 series is also available in the TO-220 plastic power package.

For output voltages other than 5V, 12V, and 15V, the LM117 series provides an output voltage range from +1.2V to +57V.

Features

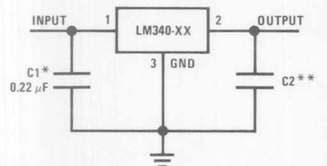
- Complete specifications at 1A load
- Output voltage tolerances of ±2% at $T_j = 25°C$ and ±4% over the temperature range (LM140A/LM340A)
- Fixed output voltages available 5, 12, and 15V
- Line regulation of 0.01% of $V_{OUT}/V\ \Delta V_{IN}$ at 1A load (LM140A/LM340A)
- Load regulation of 0.3% of $V_{OUT}/A\ \Delta I_{LOAD}$ (LM140A/LM340A)
- Internal thermal overload protection
- Internal short-circuit current limit
- Output transistor safe area protection
- 100% thermal limit burn-in
- Special circuitry allows start-up even if output is pulled to negative voltage (± supplies)

LM140 Series Package and Power Capability

DEVICE	PACKAGE	RATED POWER DISSIPATION	DESIGN LOAD CURRENT
LM140 LM340	TO-3	20W	1.5A
LM340T	TO-220	15W	1.5A
LM341	TO-202	7.5W	0.5A
LM342	TO-202	7.5W	0.25A
LM140L LM340L	TO-39	2W	0.1A
LM340L	TO-92	1.2W	0.1A

Typical Applications

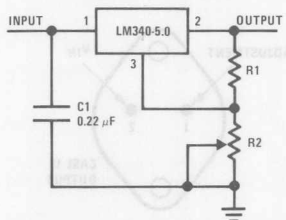
Fixed Output Regulator



*Required if the regulator is located far from the power supply filter

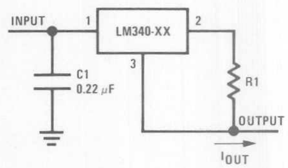
**Although no output capacitor is needed for stability, it does help transient response. (If needed, use 0.1 μF, ceramic disc)

Adjustable Output Regulator



$V_{OUT} = 5V + (5V/R1 + I_Q)\ R2$
$5V/R1 > 3\ I_Q$, load regulation $(L_r) \approx [(R1 + R2)/R1]\ (L_r$ of LM340-5)

Current Regulator



$$I_{OUT} = \frac{V2\text{-}3}{R1} + I_Q$$

ΔI_Q = 1.3 mA over line and load changes

Absolute Maximum Ratings

Input Voltage (V_O = 5V, 12V, 15V)	35V
Internal Power Dissipation (Note 1)	Internally Limited
Operating Temperature Range (T_A)	
LM140A/LM140	−55°C to +125°C
LM340A/LM340	0°C to +70°C
Maximum Junction Temperature	
(TO-3 Package K, KC)	150°C
(TO-220 Package T)	125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 Seconds)	
TO-3 Package K, KC	300°C
TO-220 Package T	230°C

Electrical Characteristics LM140A/LM340A (Note 2)

I_{OUT} = 1A, −55°C ≤ Tj ≤ +150°C (LM140A), or 0°C ≤ Tj ≤ +125°C (LM340A) unless otherwise specified.

OUTPUT VOLTAGE			5V			12V			15V			UNITS
INPUT VOLTAGE (unless otherwise noted)			10V			19V			23V			
	PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_O	Output Voltage	Tj = 25°C	4.9	5	5.1	11.75	12	12.25	14.7	15	15.3	V
		P_D ≤ 15W, 5 mA ≤ I_O ≤ 1A	4.8		5.2	11.5		12.5	14.4		15.6	V
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}		(7.5 ≤ V_{IN} ≤ 20)			(14.8 ≤ V_{IN} ≤ 27)			(17.9 ≤ V_{IN} ≤ 30)		V
ΔV_O	Line Regulation	I_O = 500 mA			10			18			22	mV
		ΔV_{IN}		(7.5 ≤ V_{IN} ≤ 20)			(14.8 ≤ V_{IN} ≤ 27)			(17.9 ≤ V_{IN} ≤ 30)		V
		Tj = 25°C		3	10		4	18		4	22	mV
		ΔV_{IN}		(7.3 ≤ V_{IN} ≤ 20)			(14.5 ≤ V_{IN} ≤ 27)			(17.5 ≤ V_{IN} ≤ 30)		V
		Tj = 25°C			4			9			10	mV
		Over Temperature			12			30			30	mV
		ΔV_{IN}		(8 ≤ V_{IN} ≤ 12)			(16 ≤ V_{IN} ≤ 22)			(20 ≤ V_{IN} ≤26)		V
ΔV_O	Load Regulation	Tj = 25°C, 5 mA ≤ I_O ≤ 1.5A		10	25		12	32		12	35	mV
		Tj = 25°C, 250 mA ≤ I_O ≤ 750 mA			15			19			21	mV
		Over Temperature, 5 mA ≤ I_O ≤ 1A			25			60			75	mV
I_Q	Quiescent Current	Tj = 25°C			6			6			6	mA
		Over Temperature			6.5			6.5			6.5	mA
ΔI_Q	Quiescent Current Change	5mA ≤ I_O ≤ 1A			0.5			0.5			0.5	mA
		Tj = 25°C, I_O = 1A			0.8			0.8			0.8	mA
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}		(7.5 ≤ V_{IN} ≤ 20)			(14.8 ≤ V_{IN} ≤ 27)			(17.9 ≤ V_{IN} ≤ 30)		V
		I_O = 500 mA			0.8			0.8			0.8	mA
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}		(8 ≤ V_{IN} ≤ 25)			(15 ≤ V_{IN} ≤ 30)			(17.9 ≤ V_{IN} ≤ 30)		V
V_N	Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz		40			75			90		μV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	Tj = 25°C, f = 120 Hz, I_O = 1A or	68	80		61	72		60	70		dB
		f = 120 Hz, I_O = 500 mA, Over Temperature,	68			61			60			dB
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}		(8 ≤ V_{IN} ≤ 18)			(15 ≤ V_{IN} ≤ 25)			(18.5 ≤ V_{IN} ≤ 28.5)		V
R_O	Dropout Voltage	Tj = 25°C, I_O = 1A		2.0			2.0			2.0		V
	Output Resistance	f = 1 kHz		8			18			19		mΩ
	Short-Circuit Current	Tj = 25°C		2.1			1.5			1.2		A
	Peak Output Current	Tj = 25°C		2.4			2.4			2.4		A
	Average TC of V_O	Min, Tj = 0°C, I_O = 5mA		−0.6			−1.5			−1.8		mV/°C
V_{IN}	Input Voltage Required to Maintain Line Regulation	Tj = 25°C	7.3			14.5			17.5			v

Note 1: Thermal resistance of the TO-3 package (K, KC) is typically 4°C/W junction to case and 35°C/W case to ambient. Thermal resistance of the TO-220 package (T) is typically 4°C/W junction to case and 50°C/W case to ambient.

Note 2: All characteristics are measured with a capacitor across the input of 0.22 μF and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (t_W ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

				5V			12V			15V			
INPUT VOLTAGE (unless otherwise noted)				10V			19V			23V			UNITS
	PARAMETER	CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_O	Output Voltage	$Tj = 25°C$, $5\ mA \leq I_O \leq 1A$		4.8	5	5.2	11.5	12	12.5	14.4	15	15.6	V
		$P_D \leq 15W$, $5\ mA \leq I_O \leq 1A$		4.75		5.25	11.4		12.6	14.25		15.75	V
		$V_{MIN} \leq V_{IN} \leq V_{MAX}$		$(8 \leq V_{IN} \leq 20)$			$(15.5 \leq V_{IN} \leq 27)$			$(18.5 \leq V_{IN} \leq 30)$			V
ΔV_O	Line Regulation	$I_O = 500\ mA$	$Tj = 25°C$		3	50		4	120		4	150	mV
			ΔV_{IN}	$(7 \leq V_{IN} \leq 25)$			$(14.5 \leq V_{IN} \leq 30)$			$(17.5 \leq V_{IN} \leq 30)$			V
			$-55°C \leq Tj \leq +150°C$			50			120			150	mV
			ΔV_{IN}	$(8 \leq V_{IN} \leq 20)$			$(15 \leq V_{IN} \leq 27)$			$(18.5 \leq V_{IN} \leq 30)$			V
		$I_O \leq 1A$	$Tj = 25°C$			50			120			150	mV
			ΔV_{IN}	$(7.3 \leq V_{IN} \leq 20)$			$(14.6 \leq V_{IN} \leq 27)$			$(17.7 \leq V_{IN} \leq 30)$			V
			$-55°C \leq Tj \leq +150°C$			25			60			75	mV
			ΔV_{IN}	$(8 \leq V_{IN} \leq 12)$			$(16 \leq V_{IN} \leq 22)$			$(20 \leq V_{IN} \leq 26)$			V
ΔV_O	Load Regulation	$Tj = 25°C$	$5\ mA \leq I_O \leq 1.5A$		10	50		12	120		12	150	mV
			$250\ mA \leq I_P \leq 750\ mA$			25			60			75	mV
		$-55°C \leq Tj \leq +150°C$, $5\ mA \leq I_O \leq 1A$				50			120			150	mV
I_Q	Quiescent Current	$I_O \leq 1A$	$Tj = 25°C$			6			6			6	mA
			$-55°C \leq Tj \leq +150°C$			7			7			7	mA
ΔI_Q	Quiescent Current Change	$5\ mA \leq I_O \leq 1A$				0.5			0.5			0.5	mA
		$Tj = 25°C$, $I_O \leq 1A$				0.8			0.8			0.8	mA
		$V_{MIN} \leq V_{IN} \leq V_{MAX}$		$(8 \leq V_{IN} \leq 20)$			$(15 \leq V_{IN} \leq 27)$			$(18.5 \leq V_{IN} \leq 30$			V
		$I_O \leq 500\ mA$, $-55°C \leq Tj \leq +150°C$				0.8			0.8			0.8	mA
		$V_{MIN} \leq V_{IN} \leq V_{MAX}$		$(8 \leq V_{IN} \leq 25)$			$(15 \leq V_{IN} \leq 30)$			$(18.5 \leq V_{IN} \leq 30)$			V
V_N	Output Noise Voltage	$T_A = 25°C$, $10\ Hz \leq f \leq 100\ kHz$			40			75			90		μV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	$f = 120\ Hz$	$I_O \leq 1A$, $Tj = 25°C$ or	68	80		61	72		60	70		dB
			$I_O \leq 500\ mA$, $-55° \leq Tj \leq +150°C$	68			61			60			dB
		$V_{MIN} \leq V_{IN} \leq V_{MAX}$		$(8 \leq V_{IN} \leq 18)$			$(15 \leq V_{IN} \leq 25)$			$(18.5 \leq V_{IN} \leq 28.5)$			V
	Dropout Voltage	$Tj = 25°C$, $I_{OUT} = 1A$			2.0			2.0			2.0		V
R_O	Output Resistance	$f = 1\ kHz$			8			18			19		mΩ
	Short-Circuit Current	$Tj = 25°C$			2.1			1.5			1.2		A
	Peak Output Current	$Tj = 25°C$			2.4			2.4			2.4		A
	Average TC of V_{OUT}	$0°C \leq Tj \leq +150°C$, $I_O = 5\ mA$			−0.6			−1.5			−1.8		mV/°C
V_{IN}	Input Voltage Required to Maintain Line Regulation	$Tj = 25°C$, $I_O \leq 1A$		7.3			14.6			17.7			V

Note 2: All characteristics are measured with a capacitor across the input of 0.22 μF and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

Electrical Characteristics LM340

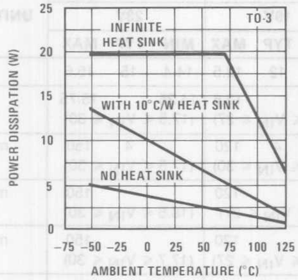
(Note 2) 0 °C ≤ Tj ≤ +125 °C unless otherwise noted.

OUTPUT VOLTAGE				5V			12V			15V			UNITS
INPUT VOLTAGE (unless otherwise noted)				10V			19V			23V			
PARAMETER		CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_O	Output Voltage	$T_j = 25°C$, $5\ mA \le I_O \le 1A$		4.8	5	5.2	11.5	12	12.5	14.4	15	15.6	V
		$P_D \le 15W$, $5\ mA \le I_O \le 1A$		4.75		5.25	11.4		12.6	14.25		15.75	V
		$V_{MIN} \le V_{IN} \le V_{MAX}$			$(7 \le V_{IN} \le 20)$			$(14.5 \le V_{IN} \le 27)$			$(17.5 \le V_{IN} \le 30)$		V
ΔV_O	Line Regulation	$I_O = 500\ mA$	$T_j = 25°C$		3	50		4	120		4	150	mV
			ΔV_{IN}		$(7 \le V_{IN} \le 25)$			$(14.5 \le V_{IN} \le 30)$			$(17.5 \le V_{IN} \le 30)$		V
			$0°C \le T_j \le +125°C$			50			120			150	mV
			ΔV_{IN}		$(8 \le V_{IN} \le 20)$			$(15 \le V_{IN} \le 27)$			$(18.5 \le V_{IN} \le 30)$		V
		$I_O \le 1A$	$T_j = 25°C$			50			120			150	mV
			ΔV_{IN}		$(7.3 \le V_{IN} \le 20)$			$(14.6 \le V_{IN} \le 27)$			$(17.7 \le V_{IN} \le 30)$		V
			$0°C \le T_j \le +125°C$			25			60			75	mV
			ΔV_{IN}		$(8 \le V_{IN} \le 12)$			$(16 \le V_{IN} \le 22)$			$(20 \le V_{IN} \le 26)$		V
ΔV_O	Load Regulation	$T_j = 25°C$	$5\ mA \le I_O \le 1.5\ A$		10	50		12	120		12	150	mV
			$250\ mA \le I_O \le 750\ mA$			25			60			75	mV
		$5\ mA \le I_O \le 1A$, $0°C \le T_j \le +125°C$				50			120			150	mV
I_Q	Quiescent Current	$I_O \le 1A$	$T_j = 25°C$			8			8			8	mA
			$0°C \le T_j \le +125°C$			8.5			8.5			8.5	mA
ΔI_Q	Quiescent Current Change	$5\ mA \le I_O \le 1A$				0.5			0.5			0.5	mA
		$T_j = 25°C$, $I_O \le 1A$				1.0			1.0			1.0	mA
		$V_{MIN} \le V_{IN} \le V_{MAX}$			$(7.5 \le V_{IN} \le 20)$			$(14.8 \le V_{IN} \le 27)$			$(17.9 \le V_{IN} \le 30)$		V
		$I_O \le 500\ mA$, $0°C \le T_j \le +125°C$				1.0			1.0			1.0	mA
		$V_{MIN} \le V_{IN} \le V_{MAX}$			$(7 \le V_{IN} \le 25)$			$(14.5 \le V_{IN} \le 30)$			$(17.5 \le V_{IN} \le 30)$		V
V_N	Output Noise Voltage	$T_A = 25°C$, $10\ Hz \le f \le 100\ kHz$			40			75			90		μV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	$f = 120\ Hz$	$I_O \le 1A$, $T_j = 25°C$ or	62	80		55	72		54	70		dB
			$I_O \le 500\ mA$, $0°C \le T_j \le +125°C$	62			55			54			dB
		$V_{MIN} \le V_{IN} \le V_{MAX}$			$(8 \le V_{IN} \le 18)$			$(15 \le V_{IN} \le 25)$			$(18.5 \le V_{IN} \le 28.5)$		V
R_O	Dropout Voltage	$T_j = 25°C$, $I_{OUT} = 1A$			2.0			2.0			2.0		V
	Output Resistance	$f = 1\ kHz$			8			18			19		mΩ
	Short-Circuit Current	$T_j = 25°C$			2.1			1.5			1.2		A
	Peak Output Current	$T_j = 25°C$			2.4			2.4			2.4		A
	Average TC of V_{OUT}	$0°C \le T_j \le +125°C$, $I_O = 5\ mA$			−0.6			−1.5			−1.8		mV/°C
V_{IN}	Input Voltage Required to Maintain Line Regulation	$T_j = 25°C$, $I_O \le 1A$		7.3			14.6			17.7			V

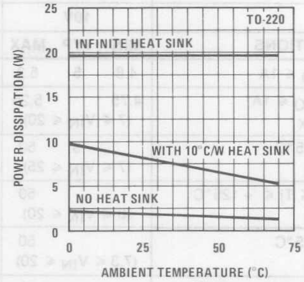
Note 2: All characteristics are measured with a capacitor across the input of 0.22 μF and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_W \le 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

Typical Performance Characteristics

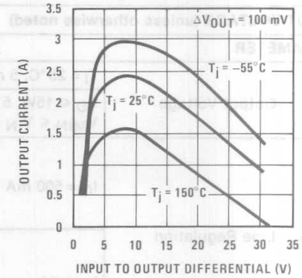
Maximum Average Power Dissipation



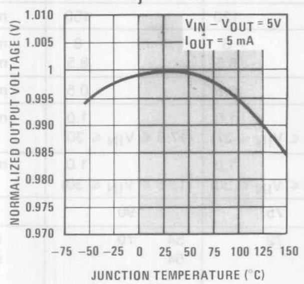
Maximum Average Power Dissipation



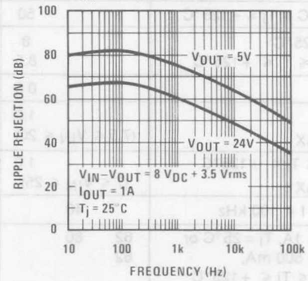
Peak Output Current



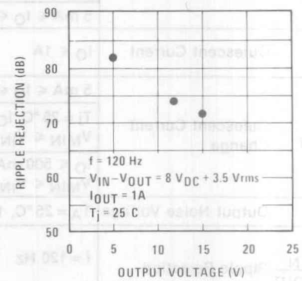
Output Voltage (Normalized to 1V at $T_j = 25°C$)



Ripple Rejection

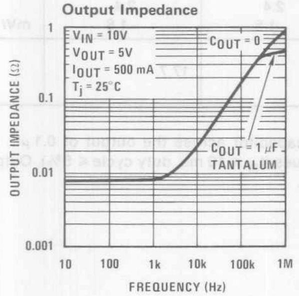


Ripple Rejection

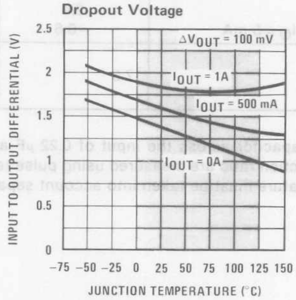


Note. Shaded area refers to LM340A/LM340

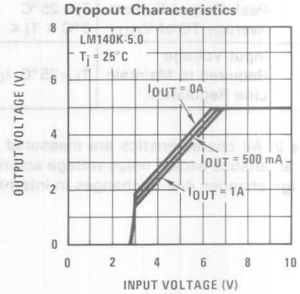
Output Impedance



Dropout Voltage

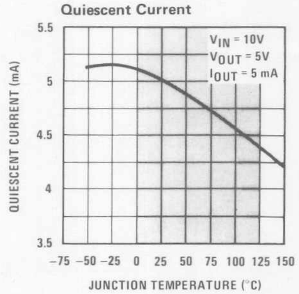


Dropout Characteristics

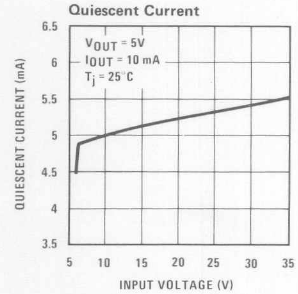


Note. Shaded area refers to LM340A/LM340

Quiescent Current



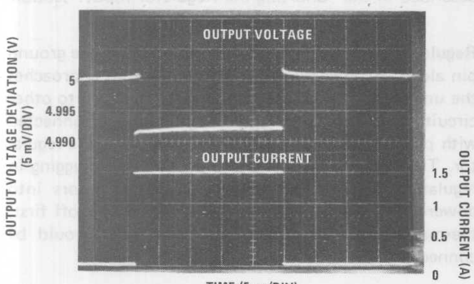
Quiescent Current



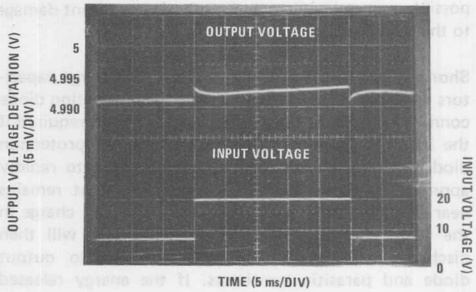
Note. Shaded area refers to LM340A/LM340

Typical Performance Characteristics (Continued)

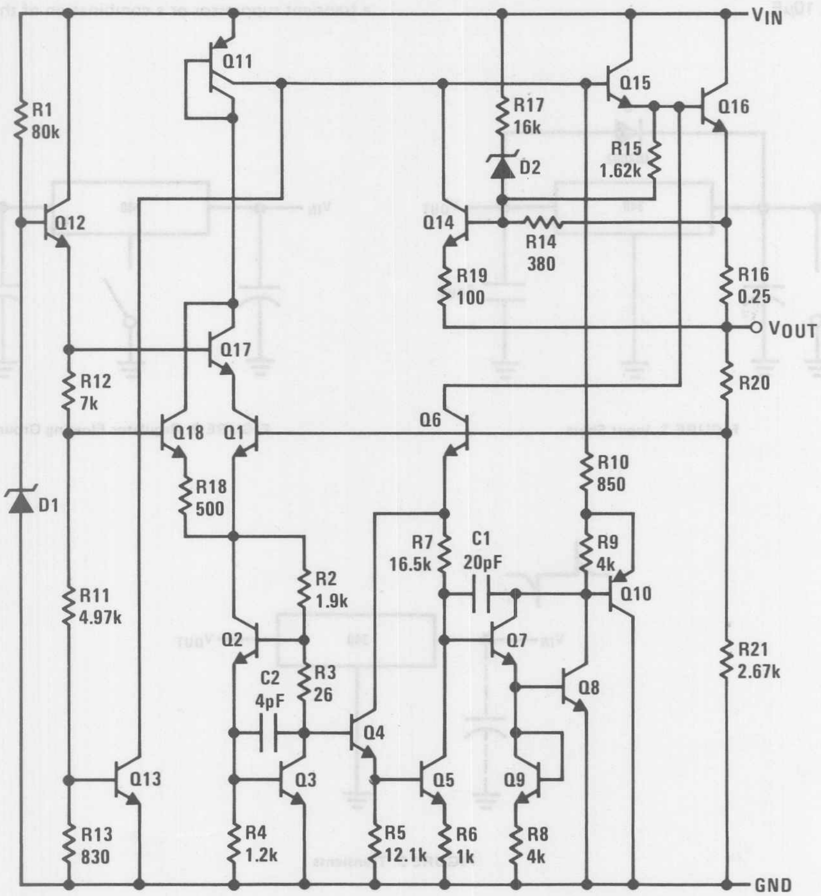
Load Regulation
140AK-5.0, $V_{IN} = 10V$, $T_A = 25^\circ C$



Line Regulation
140AK-5.0, $I_{OUT} = 1A$, $T_A = 25^\circ C$



Equivalent Schematic



Application Hints

The LM340 is designed with thermal protection, output short-circuit protection and output transistor safe area protection. However, as with *any* IC regulator, it becomes necessary to take precautions to assure that the regulator is not inadvertently damaged. The following describes possible misapplications and methods to prevent damage to the regulator.

Shorting the Regulator Input: When using large capacitors at the output of these regulators, a protection diode connected input to output (*Figure 1*) may be required if the input is shorted to ground. Without the protection diode, an input short will cause the input to rapidly approach ground potential, while the output remains near the initial V_{OUT} because of the stored charge in the large output capacitor. The capacitor will then discharge through a large internal input to output diode and parasitic transistors. If the energy released by the capacitor is large enough, this diode, low current metal and the regulator will be destroyed. The fast diode in *Figure 1* will shunt most of the capacitor's discharge current around the regulator. Generally no protection diode is required for values of output capacitance $\leq 10\mu F$.

Raising the Output Voltage above the Input Voltage: Since the output of the LM340 does not sink current, forcing the output high can cause damage to internal low current paths in a manner similar to that just described in the "Shorting the Regulator Input" section.

Regulator Floating Ground *(Figure 2)*: When the ground pin alone becomes disconnected, the output approaches the unregulated input, causing possible damage to other circuits connected to V_{OUT}. If ground is reconnected with power "ON", damage may also occur to the regulator. This fault is most likely to occur when plugging in regulators or modules with on card regulators into powered up sockets. Power should be turned off first, thermal limit ceases operating, or ground should be connected first if power must be left on.

Transient Voltages: If transients exceed the maximum rated input voltage of the 340, or reach more than 0.8V below ground and have sufficient energy, they will damage the regulator. The solution is to use a large input capacitor, a series input breakdown diode, a choke, a transient suppressor or a combination of these.

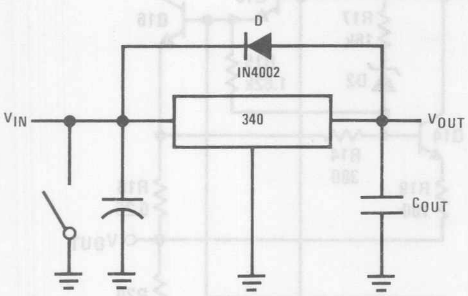


FIGURE 1. Input Short

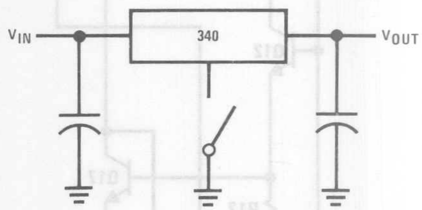


FIGURE 2. Regulator Floating Ground

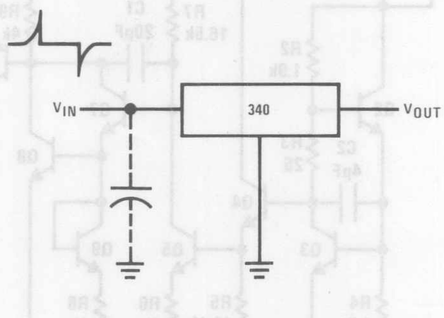
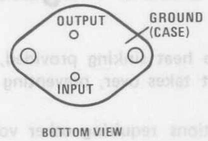


FIGURE 3. Transients

Connection Diagrams

TO-3 Metal Can Package (K and KC)



BOTTOM VIEW

Steel Package Order Numbers:

LM140AK-5.0	LM140K-5.0	LM340AK-5.0	LM340K-5.0
LM140AK-12	LM140K-12	LM340AK-12	LM340K-12
LM140AK-15	LM140K-15	LM340AK-15	LM340K-15

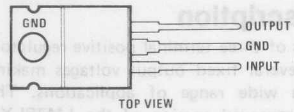
See Package K02A

Aluminum Package Order Numbers:

LM340KC-5.0
LM340KC-12
LM340KC-15

See Package KC02A

TO-220 Power Package (T)



TOP VIEW

Plastic Package Order Numbers:

LM340AT-5.0	LM340T-5.0
LM340AT-12	LM340T-12
LM340AT-15	LM340T-15

See Package T03B

National Semiconductor

Voltage Regulators

LM140L/LM340L Series 3-Terminal Positive Regulators

General Description

The LM140L series of three terminal positive regulators is available with several fixed output voltages making them useful in a wide range of applications. The LM140LA is an improved version of the LM78LXX series with a tighter output voltage tolerance (specified over the full military temperature range), higher ripple rejection, better regulation and lower quiescent current. The LM140LA regulators have ±2% V_{OUT} specification, 0.04%/V line regulation, and 0.01%/mA load regulation. When used as a zener diode/resistor combination replacement, the LM140LA usually results in an effective output impedance improvement of two orders of magnitude, and lower quiescent current. These regulators can provide local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow the LM140LA to be used in logic systems, instrumentation, Hi-Fi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

The LM140LA/LM340LA are available in the low profile metal three lead TO-39 (H) and the LM340LA are also available in the plastic TO-92 (Z). With adequate heat sinking the regulator can deliver 100 mA output current. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over, preventing the IC from overheating.

For applications requiring other voltages, see LM117 Data Sheet.

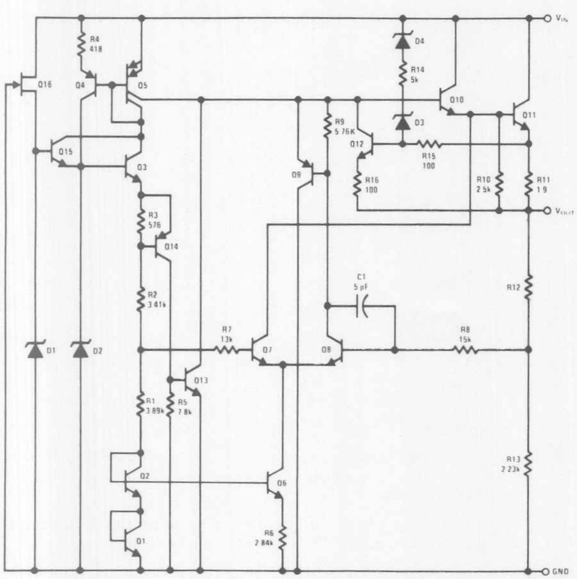
Features

- Line regulation of 0.04%/V
- Load regulation of 0.01%/mA
- Output voltage tolerances of ±2% at T_J = 25°C and ±4% over the temperature range (LM140LA) ±3% over the temperature range (LM340LA)
- Output current of 100 mA
- Internal thermal overload protection
- Output transistor safe area protection
- Internal short circuit current limit
- Available in metal TO-39 low profile package (LM140LA/LM340LA) and plastic TO-92 (LM340LA)

Output Voltage Options

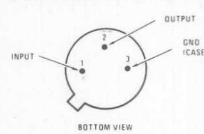
LM140LA-5.0	5V	LM340LA-5.0	5V
LM140LA-12	12V	LM340LA-12	12V
LM140LA-15	15V	LM340LA-15	15V

Equivalent Circuit



Connection Diagrams

TO-39 Metal Can Package (H)

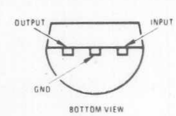


Order Number:

LM140LAH-5.0	LM340LAH-5.0
LM140LAH-12	LM340LAH-12
LM140LAH-15	LM340LAH-15

See Package H03A

TO-92 Plastic Package (Z)



Order Number:
LM340LAZ-5.0
LM340LAZ-12
LM340LAZ-15
See Package Z03A

5.0V, 12V, 15V Output Voltage Options	35V
Internal Power Dissipation (Note 1)	Internally Limited
Operating Temperature Range	
LM140LA	−55°C to +125°C
LM340LA	0°C to 70°C
Maximum Junction Temperature	+150°C
Storage Temperature Range	
Metal Can (H package)	−65°C to +150°C
Molded TO-92	−55° to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Electrical Characteristics (Note 2)

Test conditions unless otherwise specified
$T_A = -55°C$ to $+125°C$ (LM140LA)
$T_A = 0°C$ to $+70°C$ (LM340LA)
$I_O = 40$ mA
$C_{IN} = 0.33\mu F$, $C_O = 0.01\mu F$

OUTPUT VOLTAGE OPTION					**5.0V**			**12V**			**15V**		**UNITS**
INPUT VOLTAGE (unless otherwise noted)					**10V**			**19V**			**23V**		
	PARAMETER	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	
V_O	Output Voltage	Tj = 25°C		4.9	5	5.1	11.75	12	12.25	14.7	15	15.3	V
	Output Voltage Over Temp. (Note 4)	LM140LA LM240LA	I_O = 1-100 mA	4.8		5.2	11.5		12.5	14.4		15.6	
			I_O = 1-40 mA and V_{IN} = ( )V		(7.2-20)			(14.5-27)			(17.6-30)		
		LM340LA	I_O = 1-100 mA or	4.85		5.15	11.65		12.35	14.55		15.45	
			I_O = 1-40 mA and V_{IN} = ( )V		(7-20)			(14.3-27)			(17.5-30)		
ΔV_O	Line Regulation	Tj = 25°C	I_O = 40 mA		18	30		30	65		37	70	mV
			V_{IN} = ( ) V		(7-25)			(14.2-30)			(17.3-30)		
			I_O = 100 mA		18	30		30	65		37	70	
			V_{IN} = ( )V		(7.5-25)			(14.5-30)			(17.5-30)		
	Load Regulation	Tj = 25°C	I_O = 1-40 mA		5	20		10	40		12	50	
			I_O = 1-100 mA		20	40		30	80		35	100	
	Long Term Stability				12			24			30		mV 1000 hrs
I_O	Quiescent Current	Tj = 25°C			3	4.5		3	4.5		3.1	4.5	mA
		Tj = 125°C				4.2			4.2			4.2	
ΔI_Q	Quiescent Current Change	Tj = 25°C	ΔLoad I_O = 1-40mA			0.1			0.1			0.1	mA
			ΔLine			0.5			0.5			0.5	
			V_{IN} = ( ) V		(7.5-25)			(14.3-30)			(17.5-30)		
V_N	Output Noise Voltage	Tj = 25°C (Note 3) f = 10 Hz-10 kHz			40			80			90		μV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	f = 120 Hz, V_{IN} = ( ) V		55	62		47	54		45	52		dB
					(7.5-18)			(14.5-25)			(17.5-28.5)		
	Input Voltage Required to Maintain Line Regulation	Tj = 25°C, I_O = 40 mA		7			14.2			17.3			V

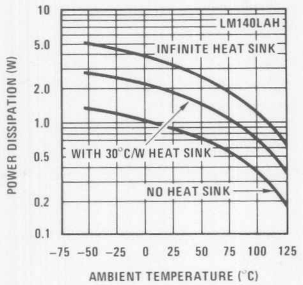
Note 1: Thermal resistance of the Metal Can Package (H) without a heat sink is 40°C/W junction to case and 140°C/W junction to ambient. Thermal resistance of the TO-92 package is 180°C/W junction to ambient with 0.4 inch leads from PC board and 160°C/W junction to ambient with 0.125 inch lead length to a PC board.

Note 2: The maximum steady state usable output current and input voltage are very dependent on the heat sinking and/or lead length of the package. The data above represent pulse test conditions with junction temperatures as indicated at the initiation of tests.

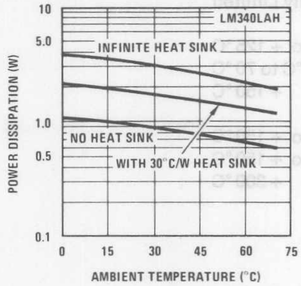
Note 3: It is recommended that a minimum load capacitor of 0.01μF be used to limit the high frequency noise bandwidth.

Note 4: The temperature coefficient of V_{OUT} is typically within 0.01% V_O/°C.

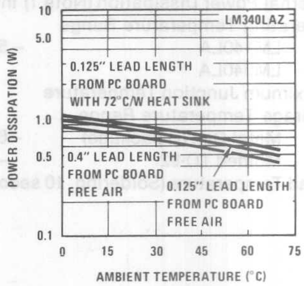
Maximum Average Power Dissipation



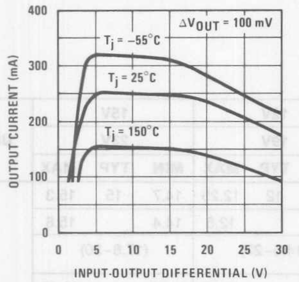
Maximum Average Power Dissipation (Metal Can Package)



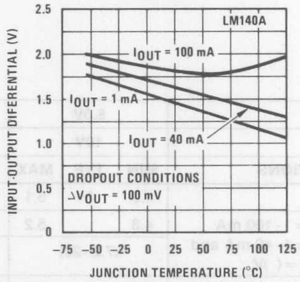
Maximum Average Power Dissipation (Plastic Package)



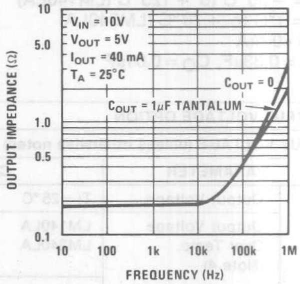
Peak Output Current



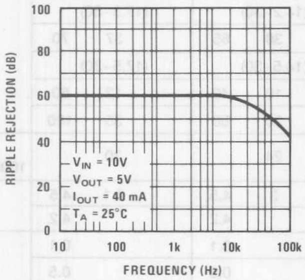
Dropout Voltage



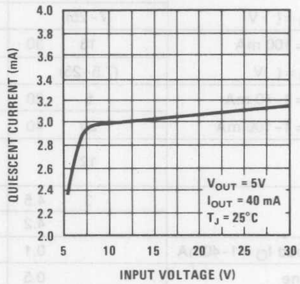
Output Impedance



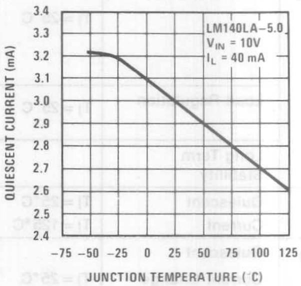
Ripple Rejection



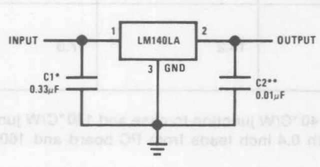
Quiescent Current



Quiescent Current



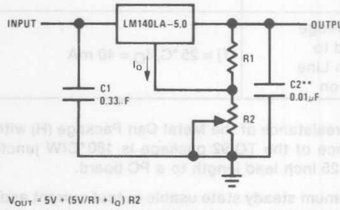
Typical Applications



*Required if the regulator is located far from the power supply filter.

**See note 3 in the electrical characteristics table.

Fixed Output Regulator



$V_{OUT} = 5V + (5V/R1 + I_Q)\,R2$

5V/R1 3 I_Q load regulation (L_r) [(R1 + R2)/R1] (L_r of LM140LA−5.0)

Adjustable Output Regulator

National Semiconductor

LM145/LM345 Negative Three Amp Regulator

General Description

The LM145 is a three-terminal negative regulator with a fixed output voltage of −5V or −5.2V, and up to 3A load current capability. This device needs only one external component—a compensation capacitor at the output, making it easy to apply. Worst case guarantees on output voltage deviation due to any combination of line, load or temperature variation assure satisfactory system operation.

Exceptional effort has been made to make the LM145 immune to overload conditions. The regulator has current limiting which is independent of temperature, combined with thermal overload protection. Internal current limiting protects against momentary faults while thermal shutdown prevents junction temperatures from exceeding safe limits during prolonged overloads.

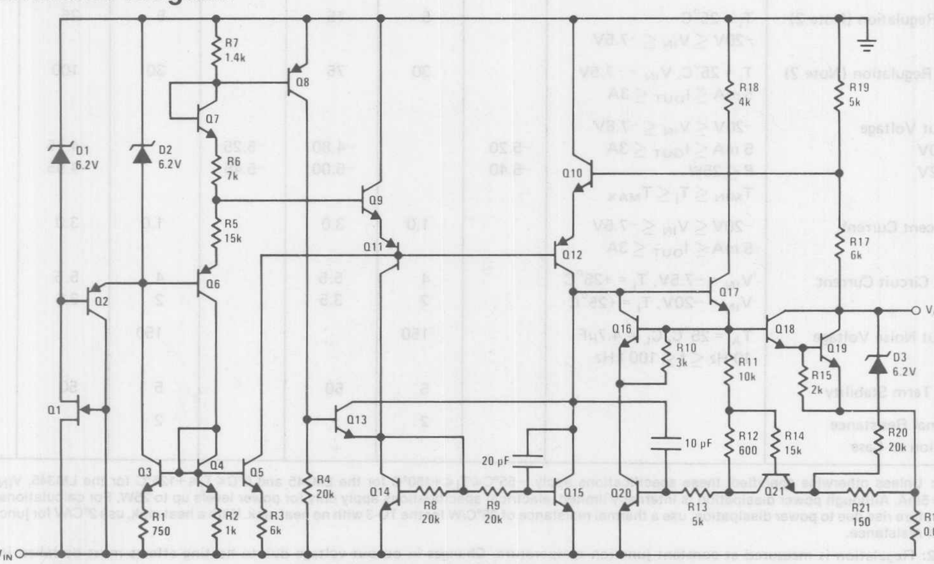
Although primarily intended for fixed output voltage applications, the LM145 may be programmed for higher output voltages with a simple resistive divider. The low quiescent drain current of the device allows this technique to be used with good regulation.

The LM145 comes in a hermetic TO-3 package rated at 25W. A reduced temperature range part LM345 is also available.

Features

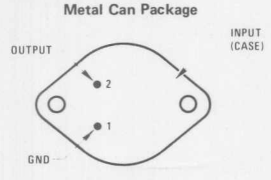
- Output voltage accurate to better than ±2%
- Current limit constant with temperature
- Internal thermal shutdown protection
- Operates with input-output voltage differential of 2.8V at full rated load over full temperature range
- Regulation guaranteed with 25W power dissipation
- 3A output current guaranteed
- Only one external component needed
- 100% electrical burn-in

Schematic Diagram



Connection Diagram

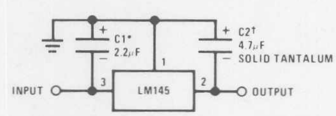
Metal Can Package



BOTTOM VIEW

Order Number LM145K-5.0, LM345K-5.0, LM145K-5.2, or LM345K-5.2
See NS Package K02A

Typical Applications



†Required for stability. For value given, capacitor must be solid tantalum. 50μF aluminum electrolytic may be substituted. Values given may be increased without limit.

*Required if regulator is separated from filter capacitor. For value given, capacitor must be solid tantalum. 50μF aluminum electrolytic may be substituted.

Fixed Regulator

Absolute Maximum Ratings

Input Voltage	20V
Input-Output Differential	20V
Power Dissipation	Internally Limited
Operating Junction Temperature Range	
LM145	$-55^{\circ}C$ to $+150^{\circ}C$
LM345	$0^{\circ}C$ to $+125^{\circ}C$
Storage Temperature Range	$-65^{\circ}C$ to $+150^{\circ}C$
Lead Temperature (Soldering, 10 seconds)	$300^{\circ}C$

Electrical Characteristics (−5V & −5.2V) (Note 1)

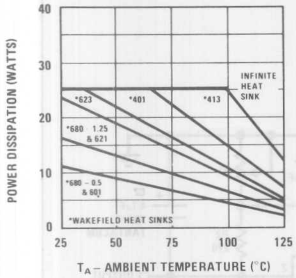
PARAMETER	CONDITIONS	LIMITS LM145 MIN	LM145 TYP	LM145 MAX	LM345 MIN	LM345 TYP	LM345 MAX	UNITS
Output Voltage	$T_j = 25^{\circ}C$, $I_{OUT} = 5$ mA,							
5.0V	$V_{IN} = -7.5$	−5.1	−5.0	−4.9	−5.2	−5.0	−4.8	V
5.2V		−5.3	−5.2	−5.1	−5.4	−5.2	−5.0	V
Line Regulation (Note 2)	$T_j = 25^{\circ}C$ $-20V \leq V_{IN} \leq -7.5V$		5	15		5	25	mV
Load Regulation (Note 2)	$T_j = 25^{\circ}C$, $V_{IN} = -7.5V$ $5\text{ mA} \leq I_{OUT} \leq 3A$		30	75		30	100	mV
Output Voltage	$-20V \leq V_{IN} \leq -7.8V$							
5.0V	$5\text{ mA} \leq I_{OUT} \leq 3A$	−5.20		−4.80	−5.25		−4.75	V
5.2V	$P \leq 25W$ $T_{MIN} \leq T_j \leq T_{MAX}$	−5.40		−5.00	−5.45		−4.95	V
Quiescent Current	$-20V \leq V_{IN} \leq -7.5V$ $5\text{ mA} \leq I_{OUT} \leq 3A$		1.0	3.0		1.0	3.0	mA
Short Circuit Current	$V_{IN} = -7.5V$, $T_j = +25^{\circ}C$		4	5.5		4	5.5	A
	$V_{IN} = -20V$, $T_j = +25^{\circ}C$		2	3.5		2	3.5	A
Output Noise Voltage	$T_A = 25^{\circ}C$, $C_L = 4.7\mu F$ $10\text{ Hz} \leq f \leq 100\text{ kHz}$		150			150		μV
Long Term Stability			5	50		5	50	mV
Thermal Resistance Junction to Case			2			2		°C/W

Note 1: Unless otherwise specified, these specifications apply: $-55^{\circ}C \leq T_j \leq +150^{\circ}C$ for the LM145 and $0^{\circ}C \leq T_j \leq +125^{\circ}C$ for the LM345. $V_{IN} = 7.5V$ and $I_{OUT} = 5mA$. Although power dissipation is internally limited, electrical specifications apply only for power levels up to 25W. For calculations of junction temperature rise due to power dissipation, use a thermal resistance of 35°C/W for the TO-3 with no heat sink. With a heat sink, use 2°C/W for junction to case thermal resistance.

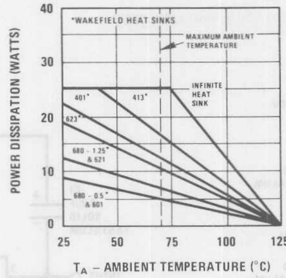
Note 2: Regulation is measured at constant junction temperature. Changes in output voltage due to heating effects must be taken into account separately. To ensure constant junction temperature, pulse testing with a low duty cycle is used.

Typical Performance Characteristics

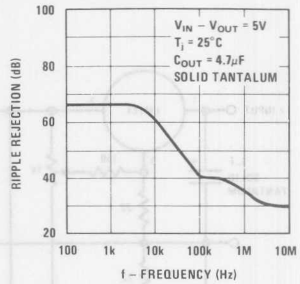
Maximum Average Power Dissipation for LM145,



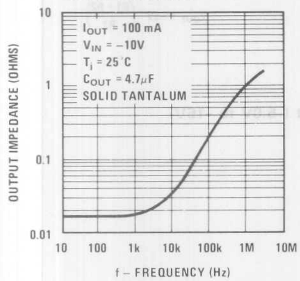
Maximum Average Power Dissipation for LM345



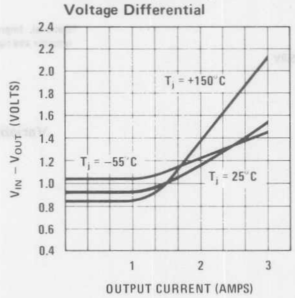
Ripple Rejection



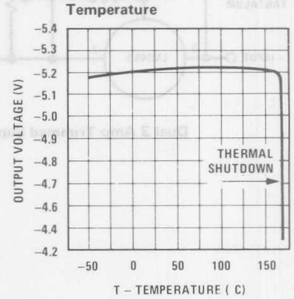
Output Impedance



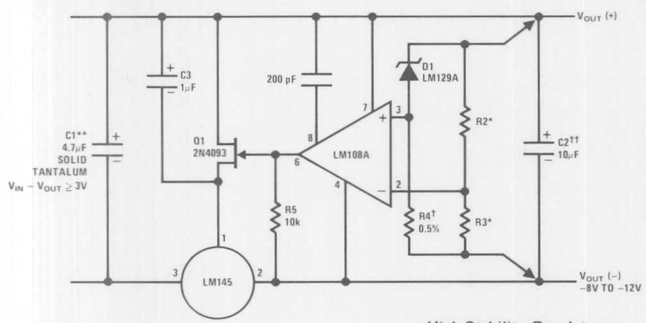
Minimum Input-Output Voltage Differential



Output Voltage vs Temperature



Typical Applications (Continued)



*Select resistors to set output voltage. 1 ppm/°C tracking suggested.

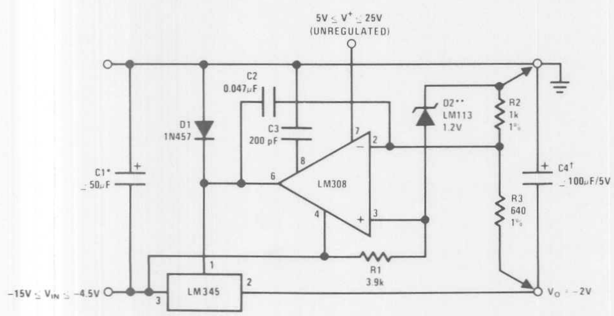
**C1 is not needed if power supply filter capacitor is within 3" of regulator.

†Determines zener current. May be adjusted to minimize temperature drift.

††Solid tantalum.

Load and line regulation < 0.01%
Temperature drift < 0.001%/°C

High Stability Regulator

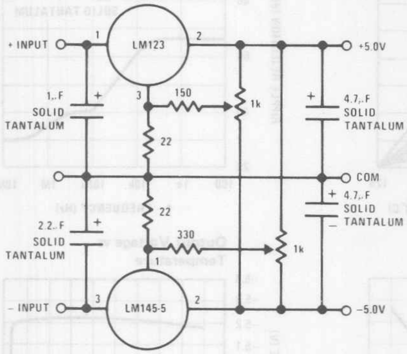


**C1 is not needed if power supply filter capacitor is within 3" of regulator.

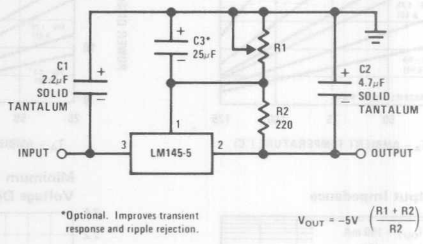
†Keep C4 within 2" of LM345.

**D2 sets initial output voltage accuracy. The LM113 is available in ±5, ±2, and ±1% tolerance.

–2V ECL Termination Regulator



Dual 3 Amp Trimmed Supply



*Optional. Improves transient response and ripple rejection.

$V_{OUT} = -5V \left(\frac{R1 + R2}{R2}\right)$

Variable Output (-5.0V to -15V)

National Semiconductor

LM150/LM250/LM350 3 Amp Adjustable Power Regulators

General Description

The LM150/LM250/LM350 are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 3A over a 1.2V to 33V output range. They are exceptionally easy to use and require only 2 external resistors to set the output voltage. Further, both line and load regulation are comparable to discrete designs. Also, the LM150 is packaged in standard transistor packages which are easily mounted and handled.

In addition to higher performance than fixed regulators, the LM150 series offers full overload protection available only in IC's. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is accidentally disconnected.

Normally, no capacitors are needed unless the device is situated far from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejections ratios which are difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators or discrete designs, the LM150 is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input to output differential is not exceeded.

Also, it makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM150 can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2V where most loads draw little current.

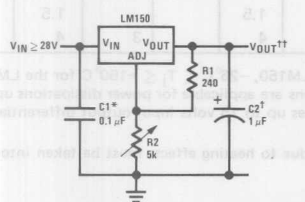
The LM150K/LM250K/LM350K are packaged in standard steel TO-3 transistor packages. The LM350T is packaged in a TO-220 plastic package. The LM150 is rated for operation from −55°C to +150°C, the LM250 from −25°C to +150°C and the LM350 from 0°C to +125°C.

Features

- Adjustable output down to 1.2V
- Guaranteed 3A output current
- Line regulation typically 0.005%/V
- Load regulation typically 0.1%
- Guaranteed thermal regulation
- Current limit constant with temperature
- **100% electrical burn-in in thermal limit**
- Eliminates the need to stock many voltages
- Standard 3-lead transistor package
- 86 dB ripple rejection

Typical Applications

1.2V–25V Adjustable Regulator



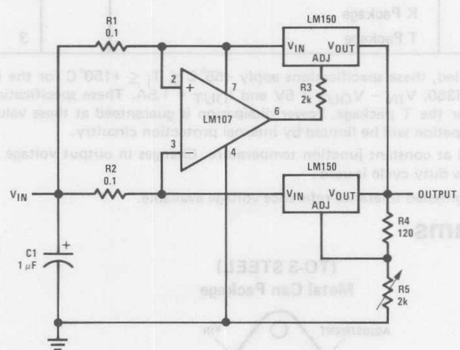
†Optional—improves transient response. Output capacitors in the range of 1 µF to 1000 µF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients.

*Needed if device is far from filter capacitors.

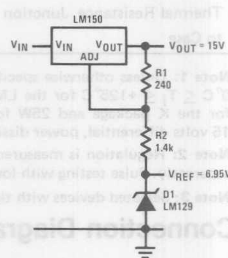
$$^{\dagger\dagger}V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right)$$

Note. Usually R1 = 240Ω for LM150 and LM250 and R1 = 120Ω for LM350.

6A Regulator



Regulator and Voltage Reference



Absolute Maximum Ratings

Power Dissipation	Internally limited
Input–Output Voltage Differential	35V
Operating Junction Temperature Range	
LM150	−55°C to +150°C
LM250	−25°C to +150°C
LM350	0°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Preconditioning

Burn-In in Thermal Limit **All Devices 100%**

Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	LM150/LM250 MIN	LM150/LM250 TYP	LM150/LM250 MAX	LM350 MIN	LM350 TYP	LM350 MAX	UNITS
Line Regulation	$T_A = 25°C$, $3V \leq V_{IN} - V_{OUT} \leq 35V$, (Note 2)		0.005	0.01		0.005	0.03	%/V
Load Regulation	$T_A = 25°C$, $10\ mA \leq I_{OUT} \leq 3A$							
	$V_{OUT} \leq 5V$, (Note 2)		5	15		5	25	mV
	$V_{OUT} \geq 5V$, (Note 2)		0.1	0.3		0.1	0.5	%
Thermal Regulation	Pulse = 20 ms		0.002	0.01		0.002	0.03	%/W
Adjustment Pin Current			50	100		50	100	μA
Adjustment Pin Current Change	$10\ mA \leq I_L \leq 3A$, $3V \leq (V_{IN} - V_{OUT}) \leq 35V$		0.2	5		0.2	5	μA
Reference Voltage	$3 \leq (V_{IN} - V_{OUT}) \leq 35V$, (Note 3) $10\ mA \leq I_{OUT} \leq 3A$, $P \leq 30W$	1.20	1.25	1.30	1.20	1.25	1.30	V
Line Regulation	$3V \leq V_{IN} - V_{OUT} \leq 35V$, (Note 2)		0.02	0.05		0.02	0.07	%/V
Load Regulation	$10\ mA \leq I_{OUT} \leq 3A$, (Note 2)							
	$V_{OUT} \leq 5V$		20	50		20	70	mV
	$V_{OUT} \geq 5V$		0.3	1		0.3	1.5	%
Temperature Stability	$T_{MIN} \leq T_j \leq T_{MAX}$		1			1		%
Minimum Load Current	$V_{IN} - V_{OUT} = 35V$		3.5	5		3.5	10	mA
Current Limit	$V_{IN} - V_{OUT} \leq 10V$	3.0	4.5		3.0	4.5		A
	$V_{IN} - V_{OUT} = 30V$, $T_j = +25°C$	0.3	1		0.25	1		A
RMS Output Noise, % of V_{OUT}	$T_A = 25°C$, $10\ Hz \leq f \leq 10\ kHz$		0.001			0.001		%
Ripple Rejection Ratio	$V_{OUT} = 10V$, f = 120 Hz		65			65		dB
	$C_{ADJ} = 10\ \mu F$	66	86		66	86		dB
Long Term Stability	$T_A = 125°C$		0.3	1		0.3	1	%
Thermal Resistance, Junction to Case	K Package			1.5			1.5	°C/W
	T Package		3	4		3	4	°C/W

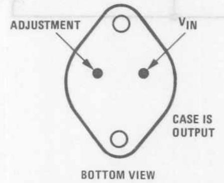
Note 1: Unless otherwise specified, these specifications apply $-55°C \leq T_j \leq +150°C$ for the LM150, $-25°C \leq T_j \leq +150°C$ for the LM250 and $0°C \leq T_j \leq +125°C$ for the LM350. $V_{IN} - V_{OUT} = 5V$ and $I_{OUT} = 1.5A$. These specifications are applicable for power dissipations up to 30W for the K package and 25W for the T package. Power dissipation is guaranteed at these values up to 15 volts input-output differential. Above 15 volts differential, power dissipation will be limited by internal protection circuitry.

Note 2: Regulation is measured at constant junction temperature. Changes in output voltage due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

Note 3: Selected devices with tightened tolerance reference voltage available.

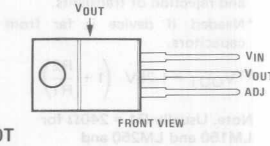
Connection Diagrams

(TO-3 STEEL)
Metal Can Package



Order Number LM150K Steel, LM250K Steel or LM350K Steel
See NS Package K02A

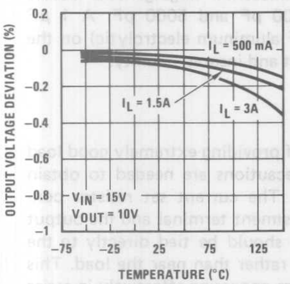
(TO-220)
Plastic Package



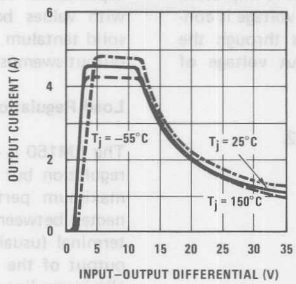
Order Number LM350T
See NS Package T03B

Typical Performance Characteristics

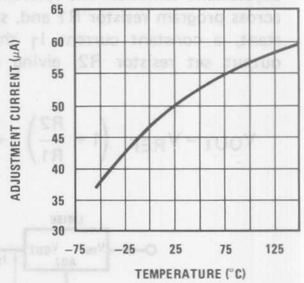
Load Regulation



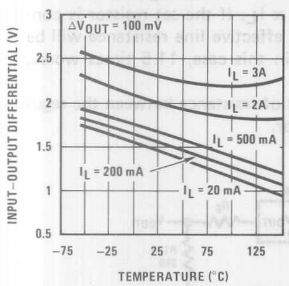
Current Limit



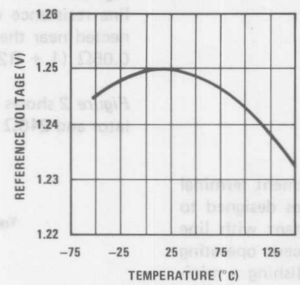
Adjustment Current



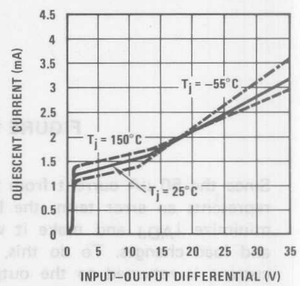
Dropout Voltage



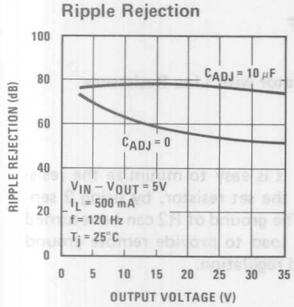
Temperature Stability



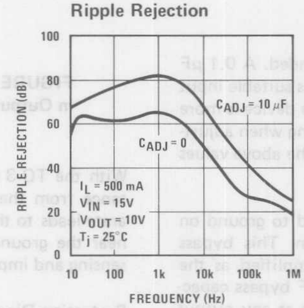
Minimum Operating Current



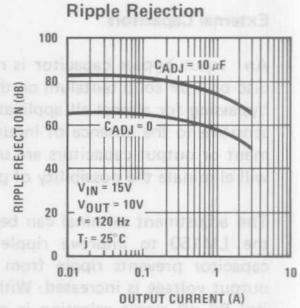
Ripple Rejection



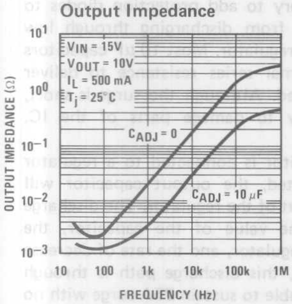
Ripple Rejection



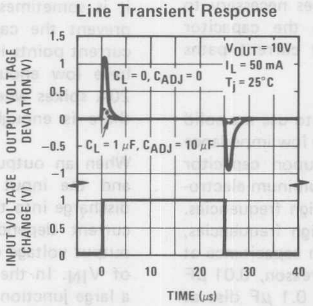
Ripple Rejection



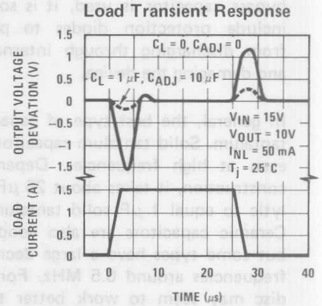
Output Impedance



Line Transient Response



Load Transient Response



reference voltage, V_{REF}, between the output and adjustment terminal. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R2, giving an output voltage of

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}R2.$$

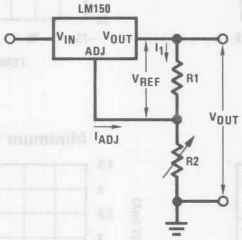


FIGURE 1

Since the 50 μA current from the adjustment terminal represents an error term, the LM150 was designed to minimize I_{ADJ} and make it very constant with line and load changes. To do this, all quiescent operating current is returned to the output establishing a minimum load current requirement. If there is insufficient load on the output, the output will rise.

External Capacitors

An input bypass capacitor is recommended. A 0.1 μF disc or 1 μF solid tantalum on the input is suitable input bypassing for almost all applications. The device is more sensitive to the absence of input bypassing when adjustment or output capacitors are used but the above values will eliminate the possibility of problems.

The adjustment terminal can be bypassed to ground on the LM150 to improve ripple rejection. This bypass capacitor prevents ripple from being amplified as the output voltage is increased. With a 10 μF bypass capacitor 86 dB ripple rejection is obtainable at any output level. Increases over 10 μF do not appreciably improve the ripple rejection at frequencies above 120 Hz. If the bypass capacitor is used, it is sometimes necessary to include protection diodes to prevent the capacitor from discharging through internal low current paths and damaging the device.

In general, the best type of capacitors to use are solid tantalum. Solid tantalum capacitors have low impedance even at high frequencies. Depending upon capacitor construction, it takes about 25 μF in aluminum electrolytic to equal 1 μF solid tantalum at high frequencies. Ceramic capacitors are also good at high frequencies, but some types have a large decrease in capacitance at frequencies around 0.5 MHz. For this reason, 0.01 μF disc may seem to work better than a 0.1 μF disc as a bypass.

Although the LM150 is stable with no output capacitors, like any feedback circuit, certain values of external capacitance can cause excessive ringing. This occurs with values between 500 pF and 5000 pF. A 1 μF solid tantalum (or 25 μF aluminum electrolytic) on the output swamps this effect and insures stability.

Load Regulation

The LM150 is capable of providing extremely good load regulation but a few precautions are needed to obtain maximum performance. The current set resistor connected between the adjustment terminal and the output terminal (usually 240Ω) should be tied directly to the output of the regulator rather than near the load. This eliminates line drops from appearing effectively in series with the reference and degrading regulation. For example, a 15V regulator with 0.05Ω resistance between the regulator and load will have a load regulation due to line resistance of 0.05Ω x I_L. If the set resistor is connected near the load the effective line resistance will be 0.05Ω (1 + R2/R1) or in this case, 11.5 times worse.

Figure 2 shows the effect of resistance between the regulator and 240Ω set resistor.

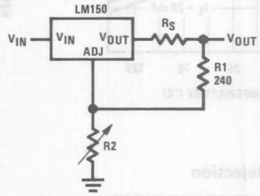


FIGURE 2. Regulator with Line Resistance in Output Lead

With the TO-3 package, it is easy to minimize the resistance from the case to the set resistor, by using 2 separate leads to the case. The ground of R2 can be returned near the ground of the load to provide remote ground sensing and improve load regulation.

Protection Diodes

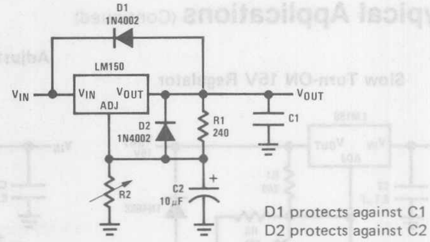
When external capacitors are used with *any* IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator. Most 10 μF capacitors have low enough internal series resistance to deliver 20A spikes when shorted. Although the surge is short, there is enough energy to damage parts of the IC.

When an output capacitor is connected to a regulator and the input is shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage of the regulator, and the rate of decrease of V_{IN}. In the LM150, this discharge path is through a large junction that is able to sustain 25A surge with no problem. This is not true of other types of positive

Application Hints (Continued)

regulators. For output capacitors of 25 µF or less, there is no need to use diodes.

The bypass capacitor on the adjustment terminal can discharge through a low current junction. Discharge occurs when *either* the input or output is shorted. Internal to the LM150 is a 50Ω resistor which limits the peak discharge current. No protection is needed for output voltages of 25V or less and 10 µF capacitance. *Figure 3* shows an LM150 with protection diodes included for use with outputs greater than 25V and high values of output capacitance.

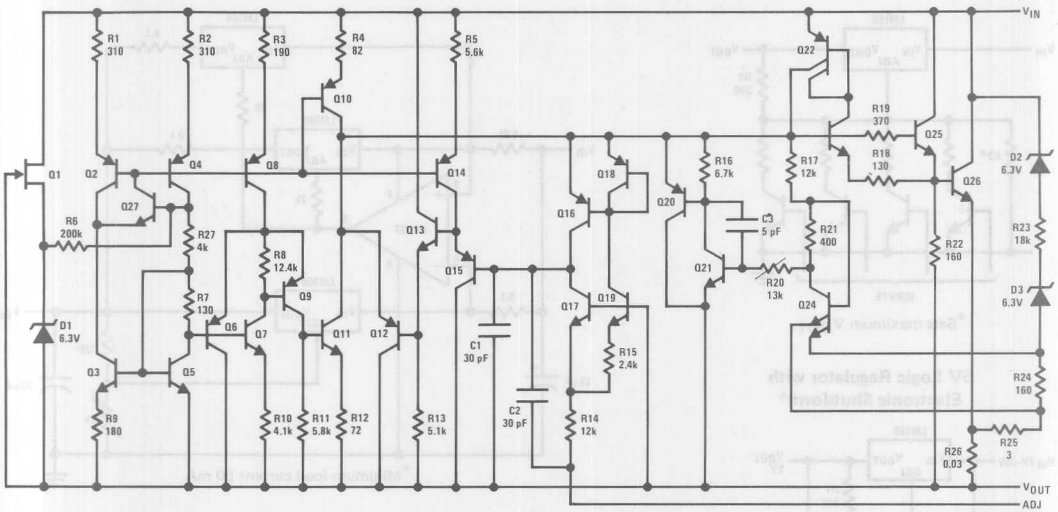


D1 protects against C1
D2 protects against C2

$$V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right) + R2I_{ADJ}$$

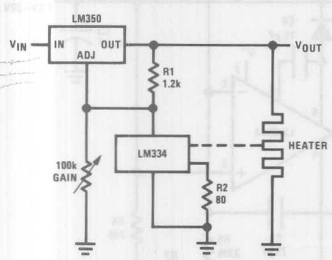
FIGURE 3. Regulator with Protection Diodes

Schematic Diagram

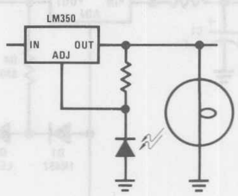


Typical Applications (Continued)

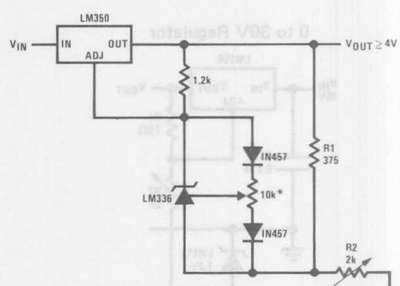
Temperature Controller



Light Controller



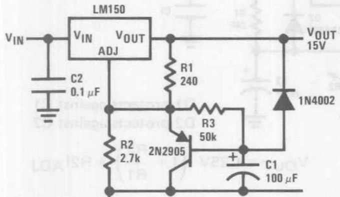
Precision Power Regulator with Low Temperature Coefficient



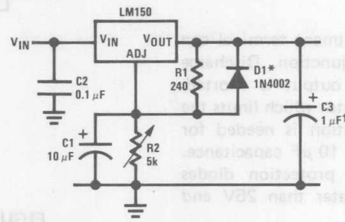
*Adjust for 3.75V across R1

Typical Applications (Continued)

Slow Turn-ON 15V Regulator



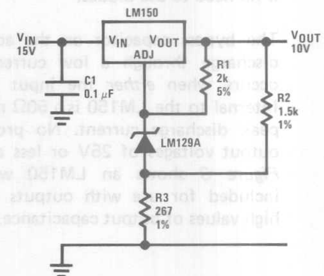
Adjustable Regulator with Improved Ripple Rejection



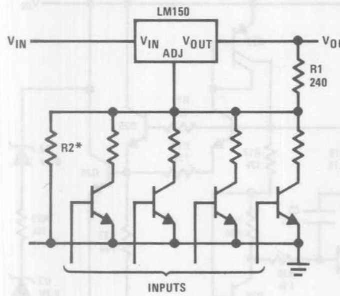
†Solid tantalum

*Discharges C1 if output is shorted to ground

High Stability 10V Regulator

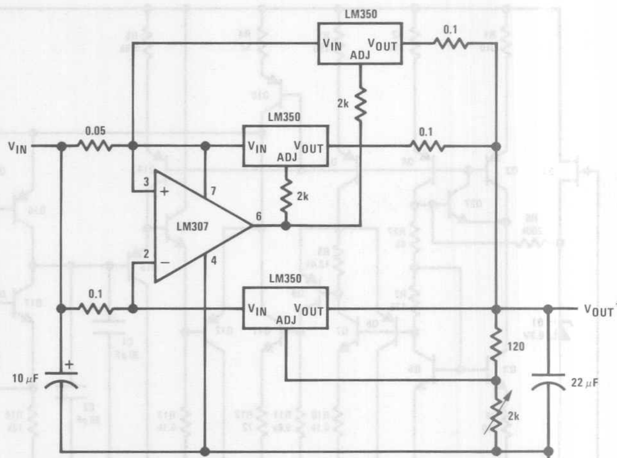


Digitally Selected Outputs



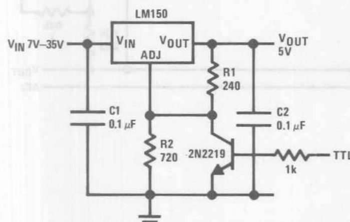
*Sets maximum V_{OUT}

10A Regulator



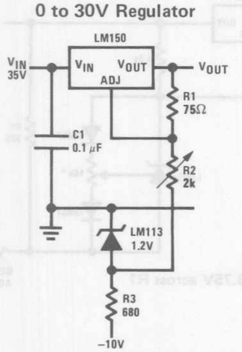
*Minimum load current 50 mA

5V Logic Regulator with Electronic Shutdown*

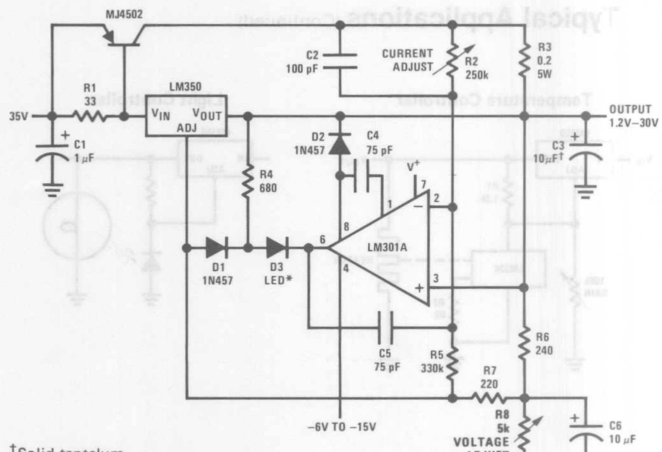


*Min output ≈ 1.2V

0 to 30V Regulator



5A Constant Voltage/Constant Current Regulator

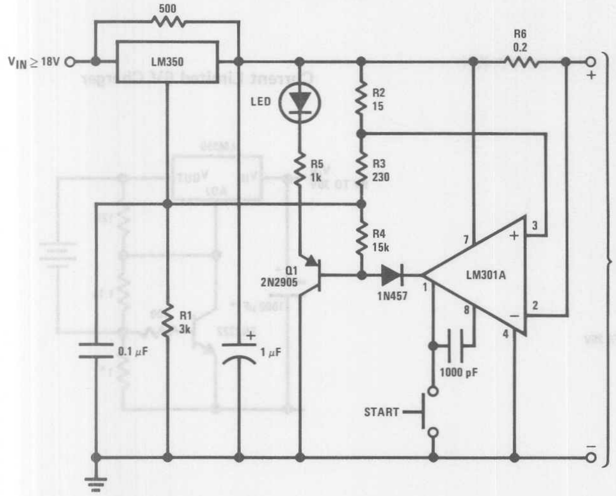


†Solid tantalum

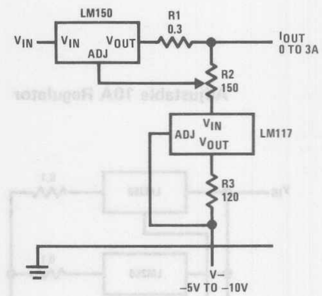
*Lights in constant current mode

Typical Applications (Continued)

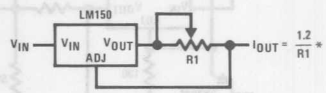
12V Battery Charger



Adjustable Current Regulator

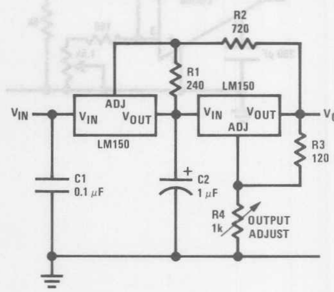


Precision Current Limiter

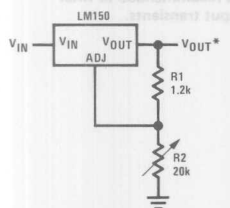


*$0.4 \leq R1 \leq 120\Omega$

Tracking Preregulator

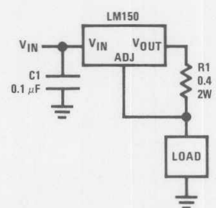


1.2V – 20V Regulator with Minimum Program Current

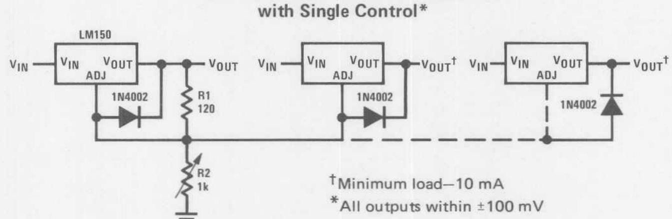


*Minimum load current ≈ 4 mA

3A Current Regulator



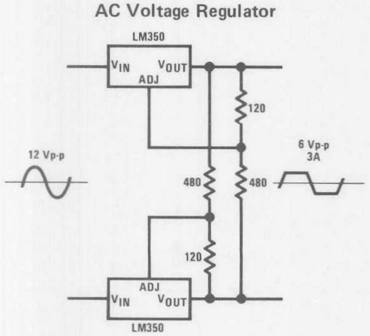
Adjusting Multiple On-Card Regulators with Single Control*



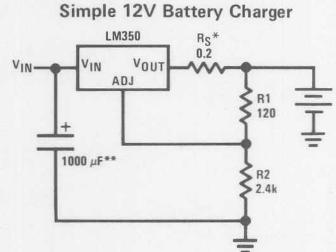
†Minimum load—10 mA

*All outputs within ±100 mV

AC Voltage Regulator



Simple 12V Battery Charger

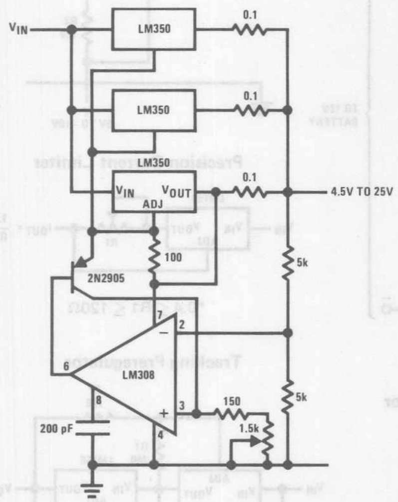


*R_S—sets output impedance of charger $Z_{OUT} = R_S \left(1 + \frac{R2}{R1}\right)$ Use of R_S allows low charging rates with fully charged battery.

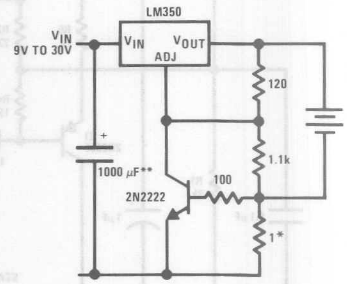
**1000 µF is recommended to filter out any input transients.

Typical Applications (Continued)

Adjustable 10A Regulator



Current Limited 6V Charger



*Sets peak current (2A for 0.3Ω)

**1000 μF is recommended to filter out any input transients.

National Semiconductor

Voltage Regulators

PRELIMINARY

LM196/LM396 10 Amp Adjustable Voltage Regulator

General Description

The LM196 is a 10 amp regulator, adjustable from 1.25V to 15V, which uses a revolutionary new IC fabrication structure to combine high power discrete transistor technology with modern monolithic linear IC processing. This combination yields a high-performance single-chip regulator capable of supplying in excess of 10 amps and operating at power levels up to 70 watts. The LM196 features on-chip trimming of reference voltage to ±0.8% and simultaneous trimming of reference temperature drift to 30 ppm/°C typical. Thermal interaction between control circuitry and the pass transistor which affects the output voltage has been reduced to extremely low levels by strict attention to isothermal layout. This interaction, called thermal regulation, is 100% tested.

This new regulator has all the protection features of popular lower power adjustable regulators such as LM117 and LM138, including current limiting and thermal limiting. The combination of these features makes the LM196 immune to blowout from output overloads or shorts, even if the adjustment pin is accidentally disconnected. All devices are "burned-in" in thermal shutdown to guarantee proper operation of these protective features under actual overload conditions.

Output voltage is continuously adjustable from 1.25V to 15V. Higher output voltages are possible if the maximum input/output voltage differential specification is not exceeded. Full load current of 10A is available at all output voltages, subject only to the maximum power limit of 70W and of course, maximum junction temperature.

The LM196 is exceptionally easy to use. Only two external resistors are used to set output voltage. On-chip adjustment of the reference voltage allows a much tighter specification of output voltage, eliminating any need for trimming in most cases. The regulator will tolerate an extremely wide range of reactive loads, and does not depend on external capacitors for frequency stabilization. Heat sink requirements are much less stringent, because overload situations do not have to be accounted for—only worst-case full load conditions.

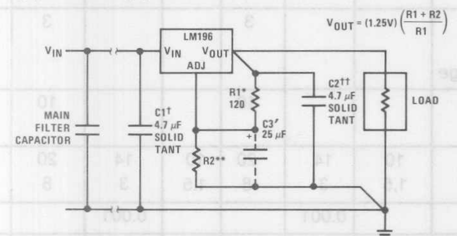
The LM196 is in a TO-3 package with oversized (0.060") leads to provide best possible load regulation. Operating junction temperature range is −55°C to +150°C. The LM396 is specified for a 0°C to +125°C junction temperature range.

Available in 1982—a 5-terminal version of the LM196. The LM196-5 will be able to operate at input-output voltage differentials as low as 1V at full load current in addition to having output sense capability. This device will also be in a TO-3 package.

Features

- Output pre-trimmed to ±0.8%
- 10A guaranteed output current
- **100% burn-in in thermal limit**
- 70W maximum power dissipation
- Adjustable output—1.25V to 15V
- Internal current and power limiting
- Guaranteed thermal resistance
- Output voltage guaranteed under worst-case conditions

Typical Applications



* For best TC of V_{OUT}, R1 should be wirewound or metal film, 1% or better.

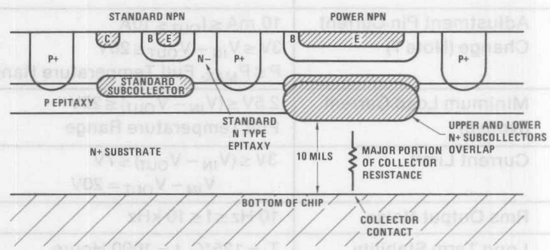
** R2 should be same type as R1, with TC tracking of 30 ppm/°C or better.

† C1 is necessary only if main filter capacitor is more than 6" away, assuming #18 or larger leads.

†† C2 is not absolutely necessary, but is suggested to lower high frequency output impedance.

′ C3 improves ripple rejection, output impedance, and noise. C2 should be 1 µF or larger close to the regulator if C3 is used.

FIGURE 1. Basic 1.25V to 15V Regulator



Power NPNs have low collector resistance, and do not require collector bond wires. Collectors are all common to substrate. Standard NPNs are still isolated.

FIGURE 2. 10 Amp Process

Absolute Maximum Ratings

Power Dissipation	Internally Limited
Input-Output Voltage Differential	20V
Operating Junction Temperature Range	
LM196 Control Section	−55°C to +150°C
Power Transistor	−55°C to +200°C
LM396 Control Section	0°C to +125°C
Power Transistor	0°C to +175°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Pre-Conditioning

100% Burn-In in Thermal Limit

Electrical Characteristics (Note 1)

Parameter	Conditions	LM196 Min	LM196 Typ	LM196 Max	LM396 Min	LM396 Typ	LM396 Max	Units
Reference Voltage	$I_{OUT}=10$ mA	1.24	1.25	1.26	1.23	1.25	1.27	V
Reference Voltage (Note 2)	$3V \le (V_{IN}-V_{OUT}) \le 20V$ 10 mA $\le I_{OUT}$ 10A, $P \le P_{MAX}$ Full Temperature Range	1.22	1.25	1.28	1.21	1.25	1.29	V
Line Regulation (Note 3)	$2.5V \le (V_{IN}-V_{OUT}) \le 20V$ Full Temperature Range		0.005	0.01 0.05		0.005	0.02 0.05	%/V %/V
Load Regulation (Note 4)	10 mA $\le I_{OUT} \le$ 10A $3V \le V_{IN}-V_{OUT} \le 10V$, $P \le P_{MAX}$ Full Temperature Range			0.1 0.15			0.1 0.15	%/A %/A
Ripple Rejection (Note 5)	$C_{ADJ}=25$ µF, f = 120 Hz Full Temperature Range	60 54	74		66 54	74		dB dB
Thermal Regulation (Note 6)	$V_{IN}-V_{OUT}=5V$, $I_{OUT}=10A$		0.003	0.005		0.003	0.015	%/W
Average Output Voltage Temperature Coefficient	$T_{jMIN} \le T_j \le T_{jMAX}$ (See Curves for Limits)		0.003			0.003		%/°C
Adjustment Pin Current			50	100		50	100	µA
Adjustment Pin Current Change (Note 7)	10 mA $\le I_{OUT} \le$ 10A $3V \le V_{IN}-V_{OUT} \le 20V$ $P \le P_{MAX}$, Full Temperature Range			3			3	µA
Minimum Load Current (Note 9)	$2.5V \le (V_{IN}-V_{OUT}) \le 20V$ Full Temperature Range			10			10	mA
Current Limit	$3V \le (V_{IN}-V_{OUT}) \le 7V$ $V_{IN}-V_{OUT}=20V$	10 1.5	14 3	20 8	10 1.5	14 3	20 8	A A
Rms Output Noise	10 Hz $\le$ f $\le$ 10 kHz		0.001			0.001		$\%V_{OUT}$
Long Term Stability	$T_j=125°C$, t = 1000 Hours		0.3	1.0		0.3	1.0	%
Thermal Resistance Junction to Case (Note 10)	Control Circuitry Power Transistor		0.3 1.0	0.5 1.2		0.3 1.0	0.5 1.2	°C/W °C/W
Power Dissipation (P_{MAX}) (Note 11)	$7.0V \le V_{IN}-V_{OUT} \le 12V$ $V_{IN}-V_{OUT}=15V$ $V_{IN}-V_{OUT}=18V$	70 50 36	100		70 50 36	100		W W W
Drop-Out Voltage (Note 12)	$I_{OUT}=10A$		2.1	2.5		2.1	2.75	V

Note 1: Unless otherwise stated, these specifications apply for $T_j = 25°C$, $V_{IN} - V_{OUT} = 5V$, $I_{OUT} = 10$ mA to 10A.

Note 2: This is a worst-case specification which includes all effects due to input voltage, output current, temperature, and power dissipation. Maximum power (P_{MAX}) is specified under Electrical Characteristics.

Note 3: Line regulation is measured on a short-pulse, low-duty-cycle basis to maintain constant junction temperature. Changes in output voltage due to thermal gradients or temperature changes must be taken into account separately. See discussion of line regulation under Application Hints.

Note 4: Load regulation on the 2-pin package is determined primarily by the voltage drop along the output pin. Specifications apply for an external Kelvin sense connection at a point on the output pin 1/4" from the bottom of the package. Testing is done on a short-pulse-width, low-duty-cycle basis to maintain constant junction temperature. Changes in output voltage due to thermal gradients or temperature changes must be taken into account separately. See discussion of load regulation under Application Hints.

Note 5: Ripple rejection is measured with the adjustment pin bypassed with a 25 μF capacitor, and is therefore independent of output voltage. With no load or bypass capacitor, ripple rejection is determined by line regulation and may be calculated from; $RR = 20 \log_{10} [100/(K \times V_{OUT})]$ where K is line regulation expressed in %/V. At frequencies below 100 Hz, ripple rejection may be limited by thermal effects, if load current is above 1A.

Note 6: Thermal regulation is defined as the change in output voltage during the time period of 0.2 ms to 20 ms after a change in power dissipation in the regulator, due to either a change in input voltage or output current. See graphs and discussion of thermal effects under Application Hints.

Note 7: Adjustment pin current change is specified for the worst-case combination of input voltage, output current, and power dissipation. Changes due to temperature must be taken into account separately. See graph of adjustment pin current vs temperature.

Note 8: Current limit is measured 10 ms after a short is applied to the output. DC measurements may differ slightly due to the rapidly changing junction temperature, tending to drop slightly as temperature increases. A minimum available load current of 10A is guaranteed over the full temperature range as long as power dissipation does not exceed 70W, and $V_{IN} - V_{OUT}$ is less than 7.0V.

Note 9: Minimum load current of 10 mA is normally satisfied by the resistor divider which sets up output voltage.

Note 10: Total thermal resistance, junction to ambient, will include junction to case thermal resistance plus interface resistance and heat sink resistance. See discussion of heat sinking under Application Hints.

Note 11: Although power dissipation is internally limited, electrical specifications apply only for power dissipation up to the limits shown. Derating with temperature is a function of both power transistor temperature and control area temperature, which are specified differently. See discussion of heat sinking under Application Hints. For $V_{IN} - V_{OUT}$ less than 7V, power dissipation is limited by current limit of 10A.

Note 12: Dropout voltage is input-output voltage differential measured at a forced reference voltage of 1.15V, with a 10A load, and is a measurement of the minimum input/output differential at full load.

Application Hints

Heat Sinking

Because of its extremely high power dissipation capability, the *major limitation* in the load driving capability of the LM196 is *heat sinking*. Previous regulators such as LM109, LM340, LM117, etc., had internal power limiting circuitry which limited power dissipation to about 30W. The LM196 is guaranteed to dissipate up to 70W continuously, as long as the maximum junction temperature limit is not exceeded. This requires careful attention to all sources of thermal resistance from junction-to-ambient, including junction-to-case resistance, case-to-heat-sink interface resistance (0.1–1.0°C/W), and heat sink resistance itself. A good thermal joint compound such as Wakefield type 120 or Thermalloy Thermacote must be used when mounting the LM196, especially if an electrical insulator is used to isolate the regulator from the heat sink. Interface resistance without this compound will be no better than 0.5°C/W, and probably much worse. With the compound, and no insulator, interface resistance will be 0.2°C/W or less, assuming 0.005" or less combined flatness run-out of TO-3 and heat sink. Proper torquing of the mounting bolts is important to achieve minimum thermal resistance. Four to six inch pounds is recommended. Keep in mind that good electrical, as well as thermal, contact must be made to the case.

The actual heat sink chosen for the LM196 will be determined by the worst-case continuous full load current, input voltage and maximum ambient temperature. Overload or short circuit output conditions do not normally have to be considered when selecting a heat sink because the thermal shutdown built into the LM196 will protect it under these conditions. An exception to this is in situations where the regulator must recover very quickly from overload. The LM196 may take some time to recover to within specified output tolerance following an extended overload, if the regulator is cooling from thermal shutdown temperature (approximately 175°) to specified operating temperature (125°C or 150°C). The procedure for heat sink selection is as follows:

Calculate worst-case *continuous* average power dissipation in the regulator from $P = (V_{IN} - V_{OUT}) \times (I_{OUT})$. To do this, you must know the raw power supply voltage/current characteristics fairly accurately. For example, consider a 10V output with 15V nominal input voltage. At full load of 10A, the regulator will dissipate $P = (15 - 10) \times (10) = 50W$. If input voltage rises by 10%, power dissipation will increase to $(16.5 - 10) \times (10) = 65W$, *a 30% increase*. It is strongly suggested that a raw supply be assembled and tested to determine its average DC output voltage *under full load with maximum line voltage*. Do not over-design by using unloaded voltage as a worst-case, since the regulator will not be dissipating any power under no load conditions. Worst-case regulator dissipation normally occurs under full load conditions except when the effective DC resistance of the raw supply ($\Delta V/\Delta I$) is larger than $(V_{IN}{}^* - V_{OUT})/2I_{fL}$, where $V_{IN}{}^*$ is the lightly-loaded raw supply voltage and I_{fL} is full load current. For $(V_{IN}{}^* - V_{OUT}) = 5V - 8V$, and $I_{fL} = 5A–10A$, this gives a resistance of 0.25Ω to 0.8Ω. If raw supply resistance is higher than this, the regulator power dissipation may be *less* at full load current, than at some intermediate current, due to the large drop in input voltage. Fortunately, most well designed raw supplies have low enough output resistance that regulator dissipation does maximize at full load current, or very close to it, so tedious testing is not usually required to find worst-case power dissipation.

Application Hints (Continued)

A very important consideration is the size of the filter capacitor in the raw supply. At these high current levels, capacitor size is usually dictated by ripple current ratings rather than just obtaining a certain ripple voltage. Capacitor ripple current (rms) is 2–3 times the DC output current of the filter. If the capacitor has just 0.05Ω DC resistance, this can cause 30W internal power dissipation at 10A output current. Capacitor life is very sensitive to operating temperature, decreasing by a factor of two for each 15°C rise in internal temperature. Since capacitor life is not all that great to start with, it is obvious that a small capacitor with a large internal temperature rise is inviting very short mean-time-to-failure. A second consideration is the loss of usable input voltage to the regulator. The LM196 requires 2V–2.5V minimum input/output voltage differential to maintain regulation. If the capacitor is small, the large dips in the input voltage may cause the LM196 to drop out of regulation. 2000 μF per ampere of load current is the *minimum* recommended value, yielding about 2 Vp-p ripple of 120 Hz. Larger values will have longer life and the reduced ripple will allow lower DC input voltage to the regulator, with subsequent cost savings in the transformer and heat sink. Sometimes several capacitors in parallel are better to decrease series resistance and increase heat dissipating area.

After the raw supply characteristics have been determined, and worst-case power dissipation in the LM196 is known, the heat sink thermal resistance can be found from the graphs titled Maximum Heat Sink Thermal Resistance (page 7). These curves indicate the minimum size heat sink required as a function of ambient temperature. They are derived from a case-to-control-area thermal resistance of 0.5°C/W and a case-to-power transistor thermal resistance of 1.2°C/W. 0.2°C/W is assumed for interface resistance. A maximum control area temperature of 150°C is used for the LM196 and 125°C for the LM396. Maximum power transistor temperature is 200°C for the LM196 and 175°C for the LM396. For conservative designs, it is suggested that when using these curves, you assume an ambient temperature 25°C–50°C higher than is actually anticipated, to avoid running the regulator right at its design limits of operating temperature.

A quick look at the curves shows that heat sink resistance (θ_{SA}) will normally fall into the range of 0.2°C/W – 1.5°C/W. These are *not* small heat sinks. A model 441, for instance, which is sold by several manufacturers, has a θ_{SA} of 0.6°C/W with natural convection and is about five inches on a side. Smaller sinks are more volumetrically efficient, and larger sinks, less so. A rough formula for estimating the volume of heat sink required is: $V = 50/\theta_{SA}^{1.5}$ CU IN. This holds for natural convection only. If the heat sink is inside a small sealed enclosure, θ_{SA} will increase substantially because the air is not free to form natural convection currents. Fan-forced convection can reduce θ_{SA} by a factor of two at 200 FPM air velocity, and by four at 1000 FPM.

Ripple Rejection

Ripple rejection at the normal ripple frequency of 120 Hz is a function of both electrical and thermal effects in the LM196. If the adjustment pin is not bypassed with a capacitor, it is also dependent on output voltage. A 25 μF capacitor from the adjustment pin to ground will make ripple rejection independent of output voltage for frequencies above 100 Hz. If lower ripple frequencies are encountered, the capacitor should be increased proportionally.

Keep in mind that the bypass capacitor on the adjustment pin will limit the turn-on time of the regulator. A 25 μF capacitor, combined with the output divider resistance, will give an extended output voltage settling time following the application of input power.

Load Regulation

Because the LM196 is a three-terminal device, it is not possible to provide true remote load sensing. Load regulation will be limited by the resistance of the output pin and the wire connecting the regulator to the load. For the data sheet specification, regulation is measured 1/4" from the bottom of the package on the output pin. Negative side sensing is a true Kelvin connection, with the bottom of the output divider returned to the negative side of the load. Although it may not be immediately obvious, best load regulation is obtained when the top of the divider is connected *directly* to the output pin, *not to the load*. This is illustrated in *Figure 3*. If R1 were connected to the load, the effective resistance between the regulator and the load would be

$$(Rw) \times \left(\frac{R2 + R1}{R1}\right)$$

Rw = Line Resistance

Connected as shown, Rw is not multiplied by the divider ratio. Rw is about 0.004Ω per foot using 16 gauge wire. This translates to 40 mV/ft at 10A load current, so it is important to keep the positive lead between regulator and load as short as possible.

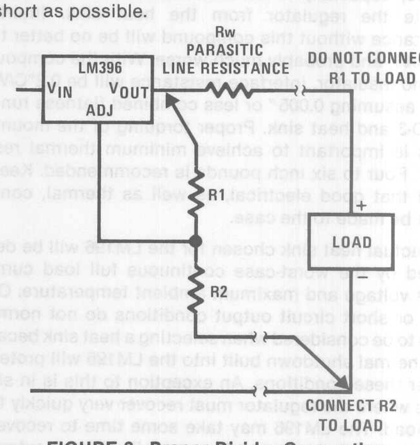


FIGURE 3. Proper Divider Connection

Application Hints (Continued)

Thermal, as well as electrical, load regulation must be considered with IC regulators. Electrical load regulation occurs in microseconds, thermal regulation due to die thermal gradients occurs in the 0.2 ms–20 ms time frame, and regulation due to overall temperature changes in the die occurs over a 20 ms to 20 minute period, depending on the time constant of the heat sink used. Gradient induced load regulation is calculated from

$$\Delta V_{OUT} = (V_{IN} - V_{OUT}) \times (\Delta I_{OUT}) \times (\beta)$$

β = Thermal regulation specified on data sheet.

For $V_{IN} = 9V$, $V_{OUT} = 5V$, $\Delta I_{OUT} = 10A$, and $\beta = 0.005\%/W$, this yields a 0.2% change in output voltage. Changes in output voltage due to overall temperature rise are calculated from

$$V_{OUT} = (V_{IN} - V_{OUT}) \times (\Delta I_{OUT}) \times (TC) \times (\theta_{jA})$$

TC = Temperature coefficient of output voltage.

θ_{jA} = Thermal resistance from junction to ambient. θ_{jA} is approximately $0.5°C/W + \theta$ of heat sink.

For the same conditions as before, with $TC = 0.003\%/°C$, and $\theta_{jA} = 1.5°C/W$, the change in output voltage will be 0.18%. Because these two thermal terms can have either polarity, they may subtract from, or add to, electrical load regulation. For worst-case analysis, they must be assumed to add. If the output of the regulator is trimmed under load, only that portion of the load that changes need be used in the previous calculations, significantly improving output accuracy.

Line Regulation

Electrical line regulation is very good on the LM196—typically less than 0.005% change in output voltage for a 1V change in input. This level of regulation is achieved only for very low load currents, however, because of thermal effects. Even with a thermal regulation of 0.002%/W, and a temperature coefficient of 0.003%/°C, DC line regulation will be dominated by thermal effects as shown by the following example:

Assume $V_{OUT} = 5V$, $V_{IN} = 9V$, $I_{OUT} = 8A$

Following a 10% change in input voltage (0.9V), the output will change quickly ($\leq 100\ \mu s$), due to electrical effects, by $(0.005\%/V) \times (0.9V) = 0.0045\%$. In the next 20 ms, the output will change an additional $(0.002\%/W) \times (8A) \times (0.9V) = 0.0144\%$ due to thermal gradients across the die. After a much longer time, determined by the time constant of the heat sink, the output will change an additional $(0.003\%/°C) \times (8A) \times (0.9V) \times (2°C/W) = 0.043\%$ due to the temperature coefficient of output voltage and the thermal resistance from die to ambient. (2°C/W was chosen for this calculation). The sign of these last two terms varies from part to part, so no assumptions can be made about any cancelling effects. All three terms must be added for a proper analysis. This yields $0.0045 + 0.0144 + 0.043 = 0.062\%$ using *typical* values for thermal regulation and temperature coefficient. For worst-case analysis, the maximum data sheet specifications for thermal regulation and temperature coefficient should be used, along with the *actual* thermal resistance of the heat sink being used.

Paralleling Regulators

Paralleling regulators is not normally recommended because they do not share currents equally. The regulator with the highest reference voltage will supply all the current to the load until it current limits. With an 18A load, for instance, one regulator might be operating in current limit at 16A while the second device is only carrying 2A. Power dissipation in the high current regulator is extremely high with attendant high junction temperatures. Long term reliability cannot be guaranteed under these conditions.

Quasi-paralleling may be accomplished if load regulation is not critical. The connection shown in *Figure 6* will typically share to within 1A, with a worst-case of about 3A. Load regulation is degraded by 150 mV at 20A loads. An external op amp may be used as in *Figure 8* to improve load regulation.

Input and Output Capacitors

The LM196 will tolerate a wide range of input and output capacitance, but long wire runs or small values of output capacitance can sometimes cause problems. If an output capacitor is used, it should be 1 μF or larger. We suggest 10 μF solid tantalum if significant improvements in high frequency output impedance are needed (see output impedance graph). This capacitor should be as close to the regulator as possible, with short leads, to reduce the effects of lead inductance. No input capacitor is needed if the regulator is within 6 inches of the power supply filter capacitor, using 18 gauge stranded wire. For longer wire runs, the LM196 input should be bypassed locally with a 4.7 μF (or larger) solid tantalum capacitor, or a 100 μF (or larger) aluminum electrolytic capacitor.

Correcting for Line Losses

Three-terminal regulators can only provide partial Kelvin load sensing (see Load Regulation). Full remote sensing can be added by using an external op amp to cancel the effect of voltage drops in the unsensed positive output lead. In *Figure 8*, the LM301A op amp forces the voltage loss across the unsensed output lead to appear across R3. The current through R3 then flows out the V^- pin of the op amp through R4. The voltage drop across R4 will raise the output voltage by an amount equal to the line loss, just cancelling the line loss itself. A small ($\simeq$ 40 mV) initial output voltage error is created by the quiescent current of the op amp. Cancellation range is limited by the maximum output current of the op amp, about 300 mV as shown. This can be raised by increasing R3 or R4 at the expense of more initial output error.

Transformers and Diodes

Proper transformer ratings are very important in a high current supply because of the conflicting requirements of efficiency and tolerance to low-line conditions. A transformer with a high secondary voltage will waste power and cause unnecessary heating in the regulator.

1

used to calculate the required secondary voltage and current ratings using a full-wave center tap:

$$V_{rms} = \left(\frac{V_{OUT} + V_{REG} + V_{RECT} + V_{RIPPLE}}{\sqrt{2}}\right)\left(\frac{V_{NOM}}{V_{LOW}}\right)\left(1.1^{*}\right)$$

$I_{rms} = (I_{OUT})\,(1.2)$ (Full-wave center tap)

where:

V_{OUT} = DC regulated output voltage

V_{REG} = Minimum input-output voltage of regulator

V_{RECT} = Rectifier forward voltage drop at three times DC output current

V_{RIPPLE} = 1/2 peak-to-peak capacitor ripple voltage $= \dfrac{(5.3 \times 10^{-3})\,(I_{OUT})}{2C}$

V_{NOM} = Nominal line voltage AC rms

V_{LOW} = Low line voltage AC rms

I_{OUT} = DC output current

Example: $I_{OUT} = 10A$, $V_{OUT} = 5V$

Assume: $V_{REG} = 2.2V$, $V_{RECT} = 1.2V$

$V_{RIPPLE} = 2$ Vp-p, $V_{NOM} = 115V$,

$V_{LOW} = 105V$

$$V_{rms} = \left(\frac{5 + 2.2 + 1.2 + 1}{\sqrt{2}}\right)\left(\frac{115}{105}\right)1.1$$

$$= 8.01\ V_{rms}$$

$$\text{Capacitor C} = \frac{(5.3 \times 10^{-3})\,(I_{OUT})}{2 \bullet V_{RIPPLE}}$$

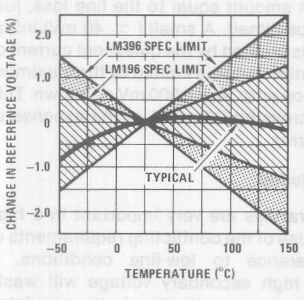
$$= \frac{(5.3 \times 10^{-3})(10)}{2} = 26{,}500\ \mu F$$

*The factor of 1.1 is only an approximate factor accounting for load regulation of the transformer.

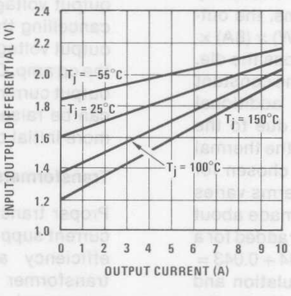
than the average current flowing through them. In a 10A supply, for instance, the average current through each diode is only 5A, but the diodes should have a rating of 10A–15A. There are many reasons for this, both thermal and electrical. The diodes conduct current in pulses about 3.5 ms wide with a peak value of 5–8 times the average value, and an rms value 1.5–2.0 times the average value. This results in long term diode heating roughly equivalent to 10A DC current. The most demanding condition however, may be the one cycle surge through the diode during power turn on. The peak value of the surge is about 10–20 times the DC output current of the supply, or 100A–200A for a 10A supply. The diodes must have a one cycle non-repetitive surge rating of 200A or more, and this is usually not found in a diode with less than 10A average current rating. Keep in mind that even though the LM196 may be used at current levels below 10A, the diodes may still have to survive shorted output conditions where average current could rise to 12A–15A. Smaller transformers and filter capacitors used in lower current supplies will reduce surge currents, but unless specific information is available on worst-case surges, it is best not to economize on diodes. Stud-mounted devices in a DO-4 package are recommended. Cathode-to-case types may be bolted directly to the same heat sink as the LM196 because the case of the regulator is its power input. Part numbers to consider are the 1N1200 series rated at 12A average current in a DO-4 stud package. Additional types include common cathode duals in a TO-3 package, both standard and Schottky, and various duals in plastic filled assemblies. Schottky diodes will improve efficiency, especially in low voltage applications. In a 5V supply for instance, Schottky diodes will decrease wasted power by up to 6W, or alternatively provide an additional 5% "drop out" margin for low-line conditions. Several manufacturers are producing "high efficiency" diodes with a forward voltage drop nearly as good as Schottkys at high current levels. These devices do not have the low breakdown voltages of Schottkys, so are much less prone to reverse breakdown induced failures.

Typical Performance Characteristics

Reference Drift

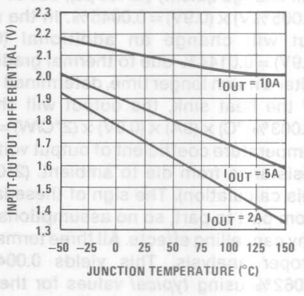


Minimum Input-Output Differential*



*V_{IN} is reduced until output drops 2%

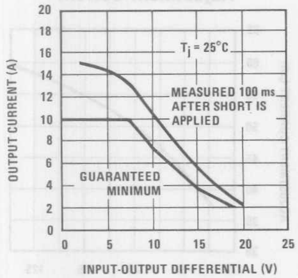
Minimum Input-Output Differential*



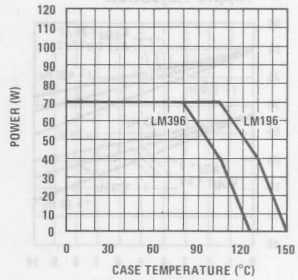
*V_{IN} is reduced until output drops 2%

Typical Performance Characteristics (Continued)

Current Limit

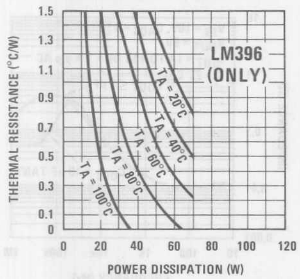


Maximum Power Dissipation*



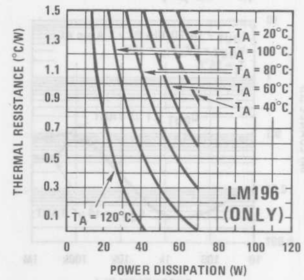
*As limited by maximum junction temperature

Maximum Heat Sink Thermal Resistance



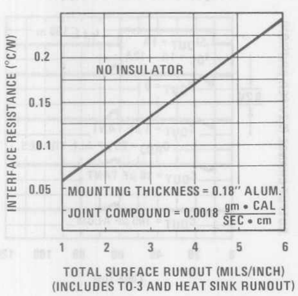
* See "Heat Sinking" under Application Hints.

Maximum Heat Sink Thermal Resistance*

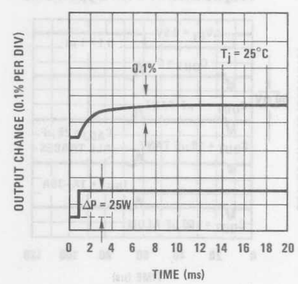


*See "Heat Sinking" under Application Hints.

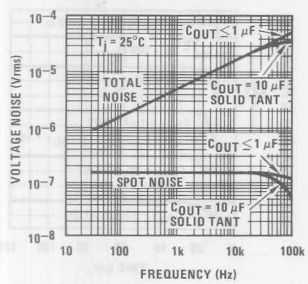
TO-3 Interface Thermal Resistance using Thermal Joint Compound



Thermal Regulation

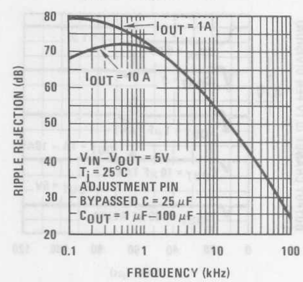


Reference Voltage Noise*



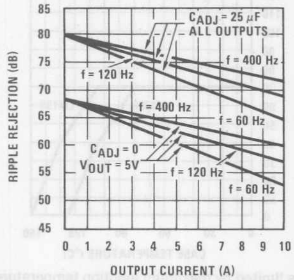
*To obtain output noise, multiply by $V_{OUT}/1.25$ if adjustment pin is not bypassed.

Ripple Rejection

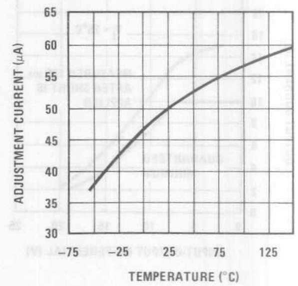


Typical Performance Characteristics (Continued)

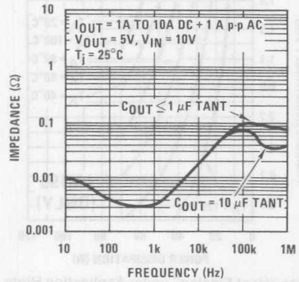
Ripple Rejection



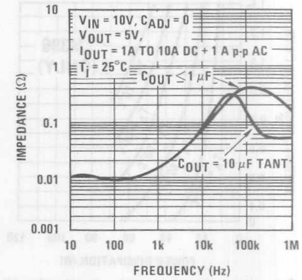
Adjustment Current



Output Impedance Adjustment Pin Bypassed (C = 25 μF)

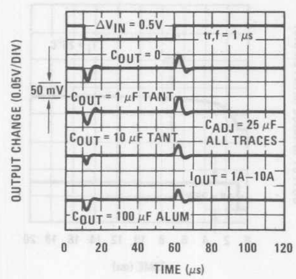


Output Impedance*

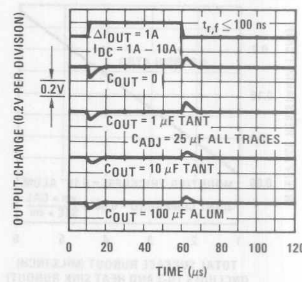


*For output voltages other than 5V, multiply vertical scale readings by $V_{OUT}/5$.

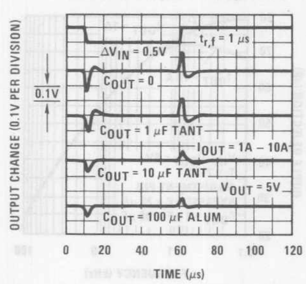
Line Transient Response Adjustment Pin Bypassed



Load Transient Response Adjustment Pin Bypassed

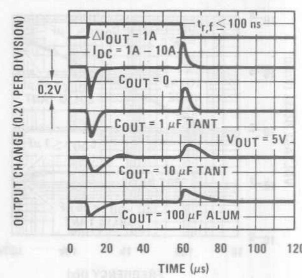


Line Transient Response*

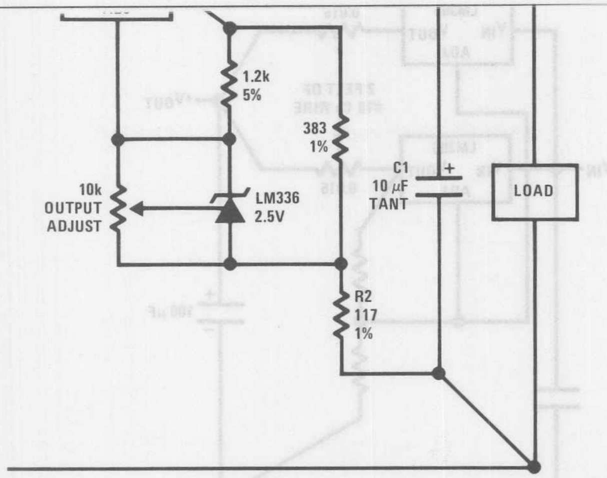


*With no adjustment pin bypass. For output voltages other than 5V, multiply vertical scale by $V_{OUT}/5$.

Load Transient Response*

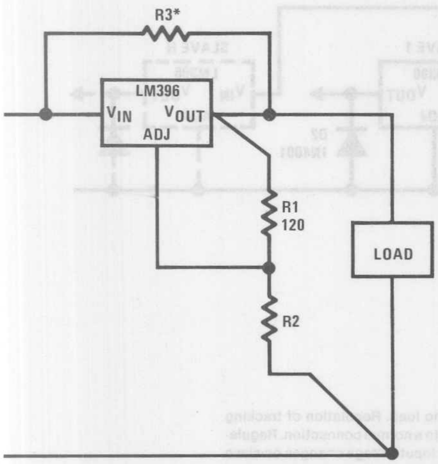


*With no adjustment pin bypass. For output voltages other than 5V, multiply vertical scale by $V_{OUT}/5$.



*Regulation can be improved by adding an LM336 reference diode to increase the effective reference voltage to 3.75V. Load and line regulation are improved by 3:1, including thermal effects.

FIGURE 4. Improving Regulation*



*R3 is selected to supply partial load current. Therefore, a minimum load must always be maintained to prevent the regulated output from rising uncontrolled. R3 must be greater than $(V_{MAX} - V_{OUT})/I_{MIN}$, where V_{MAX} is worst-case high input voltage, and I_{MIN} is the minimum load current. R3 must be rated for at least $(V_{IN} - V_{OUT})^2/R3$ watts. Regulator power dissipation will be reduced by a factor of 2 – 3 in a typical situation where minimum load current is 1/2 full load current. Regulator dissipation will peak at:

$$V_{IN} = \frac{(R3)(I_{OUT})}{2} + V_{OUT}$$

and will be equal to:

$$P_{MAX} = \frac{(R3)(I_{OUT})^2}{4} \text{ Assuming: } (R3)(I_{OUT}) \le V_{MAX} - V_{OUT}$$

A few words of caution; (1) R3 power rating must be increased to $(V_{MAX})^2/R3$ if continuous output shorts are possible. (2) Under normal load conditions, system power dissipation is not changed, but under short circuit conditions *system* power dissipation increases by $(V_{IN})^2/R3$ watts over the already high power of a shorted regulator. The LM196 will not be harmed and neither will R3 if it is rated properly, but the raw supply components must be able to withstand the overload also. Thermal shutdown of the LM196 will probably occur for sustained shorts, somewhat alleviating the problem.

FIGURE 5. Reducing Regulator Power Dissipation

Typical Applications (Continued)

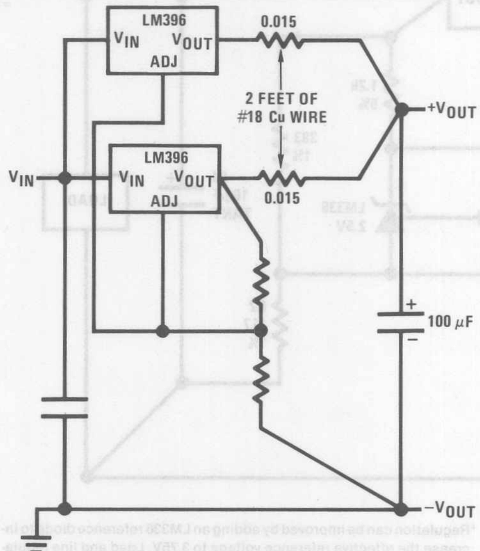
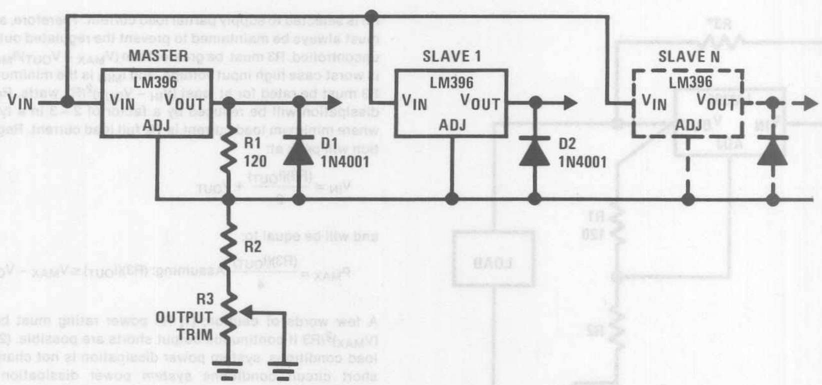


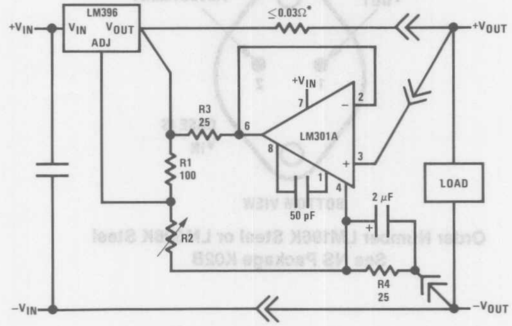
FIGURE 6. Paralleling Regulators



Output will be within ±20 mV at 25°C, no load. Regulation of tracking units is improved by $V_{OUT}/1.25$ compared to a normal connection. Regulation of master unit is unchanged. Load or input voltage changes on slave units do not affect other units, but all units will be affected by changes on master. A short on any output will cause all other outputs to drop to approximately 2V.

FIGURE 7. Tracking Regulators

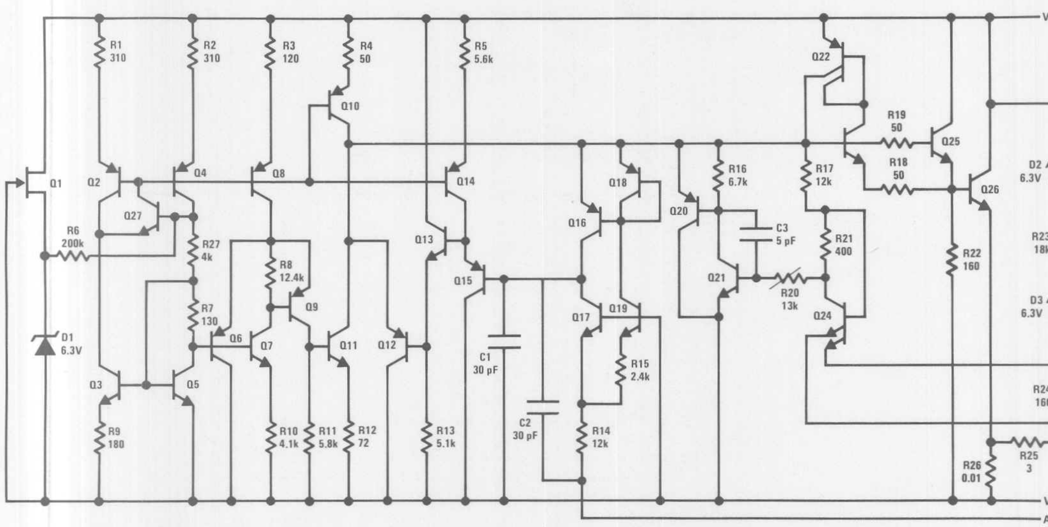
Typical Applications (Continued)



*Parasitic line resistance created by wiring, connectors, or parallel ballasting.

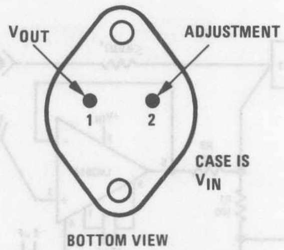
FIGURE 8. Correcting for Line Losses

LM196 Schematic Diagram



Connection Diagram

Metal Can Package



Order Number LM196K Steel or LM396K Steel
See NS Package K02B

National Semiconductor

Voltage Regulators

LM317L 3-Terminal Adjustable Regulator

General Description

The LM317L is an adjustable 3-terminal positive voltage regulator capable of supplying 100 mA over a 1.2V to 37V output range. It is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, both line and load regulation are better than standard fixed regulators. Also, the LM317L is packaged in a standard TO-92 transistor package which is easy to use.

In addition to higher performance than fixed regulators, the LM317L offers full overload protection. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

Besides replacing fixed regulators, the LM317L is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input-to-output differential is not exceeded.

Also, it makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM317L can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2V where most loads draw little current.

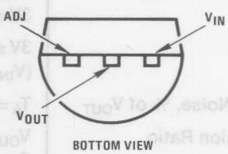
The LM317L is packaged in a standard TO-92 transistor package. The LM317L is rated for operation over a −25°C to 125°C range.

Features

- Adjustable output down to 1.2V
- Guaranteed 100 mA output current
- Line regulation typically 0.01%/V
- Load regulation typically 0.1%
- Current limit constant with temperature
- Eliminates the need to stock many voltages
- Standard 3-lead transistor package
- 80 dB ripple rejection

Normally, no capacitors are needed unless the device is situated far from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejection ratios which are difficult to achieve with standard 3-terminal regulators.

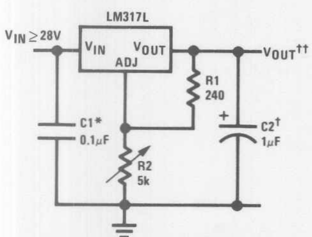
Connection Diagram



Order Number LM317LZ
See NS Package Z03A

Typical Applications

1.2V–25V Adjustable Regulator

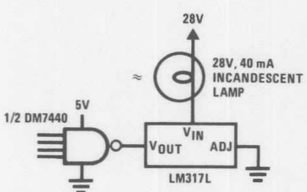


† Optional—improves transient response

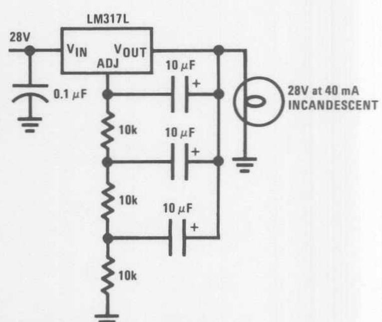
* Needed if device is far from filter capacitors

$$††V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right)$$

Fully Protected (Bulletproof) Lamp Driver



Lamp Flasher



Output rate — 4 flashes per second at 10% duty cycle

Operating Junction Temperature Range −40°C to +125°C
Storage Temperature −55°C to +150°C
Lead Temperature (Soldering, 10 seconds) 300°C

Electrical Characteristics (Note 1)

Parameter	Conditions	Min	Typ	Max	Units
Line Regulation	$T_A = 25°C$, $3V \le (V_{IN}-V_{OUT}) \le 40V$, (Note 2)		0.01	0.04	%/V
Load Regulation	$T_A = 25°C$, $5\ mA \le I_{OUT} \le I_{MAX}$, (Note 2)		0.1	0.5	%
Thermal Regulation	$T_A = 25°C$, 10 ms Pulse		0.04	0.2	%/W
Adjustment Pin Current			50	100	μA
Adjustment Pin Current Change	$5\ mA \le I_L \le 100\ mA$ $3V \le (V_{IN}-V_{OUT}) \le 40V$, $P \le 625\ mW$		0.2	5	μA
Reference Voltage	$3V \le (V_{IN}-V_{OUT}) \le 40V$, (Note 3) $5\ mA \le I_{OUT} \le 100\ mA$, $P \le 625\ mW$	1.20	1.25	1.30	V
Line Regulation	$3V \le (V_{IN}-V_{OUT}) \le 40V$, (Note 2)		0.02	0.07	%/V
Load Regulation	$5\ mA \le I_{OUT} \le 100\ mA$, (Note 2)		0.3	1.5	%
Temperature Stability	$T_{MIN} \le T_j \le T_{MAX}$		0.65		%
Minimum Load Current	$(V_{IN}-V_{OUT}) \le 40V$ $3V \le (V_{IN}-V_{OUT}) \le 15V$		3.5 1.5	5 2.5	mA mA
Current Limit	$3V \le (V_{IN}-V_{OUT}) \le 13V$ $(V_{IN}-V_{OUT}) = 40V$	100 25	200 50	300 150	mA mA
Rms Output Noise, % of V_{OUT}	$T_A = 25°C$, $10\ Hz \le f \le 10\ kHz$		0.003		%
Ripple Rejection Ratio	$V_{OUT} = 10V$, $f = 120\ Hz$, $C_{ADJ} = 0$ $C_{ADJ} = 10\ \mu F$	 66	65 80		dB dB
Long-Term Stability	$T_j = 125°C$, 1000 Hours		0.3	1	%

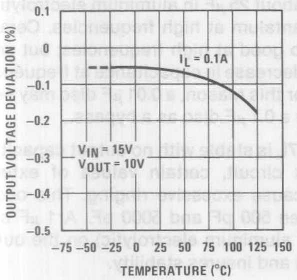
Note 1: Unless otherwise specified, these specifications apply $-25°C \le T_j \le 125°C$ for the LM317L; $V_{IN}-V_{OUT} = 5V$ and $I_{OUT} = 40$ mA. Although power dissipation is internally limited, these specifications are applicable for power dissipations up to 625 mW. I_{MAX} is 100 mA.

Note 2: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.

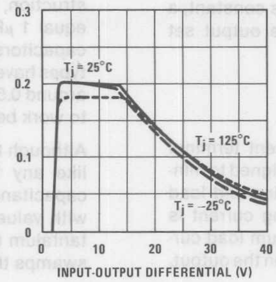
Note 3: Thermal resistance of the TO-92 package is 180°C/W junction to ambient with 0.4″ leads from a PC board and 160°C/W junction to ambient with 0.125″ lead length to PC board.

Typical Performance Characteristics (Output capacitor = 0 μF unless otherwise noted.)

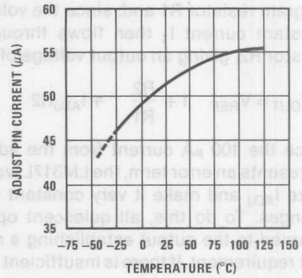
Load Regulation



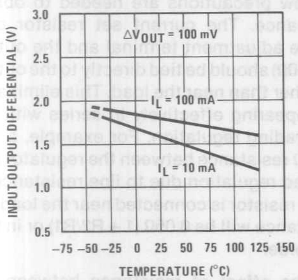
Current Limit



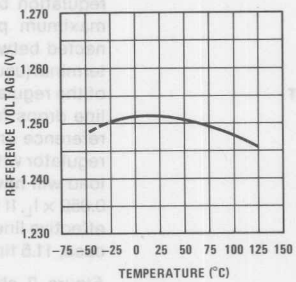
Adjustment Current



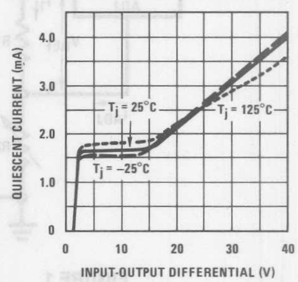
Dropout Voltage



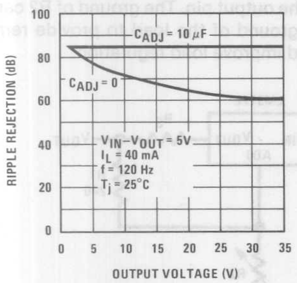
Reference Voltage Temperature Stability



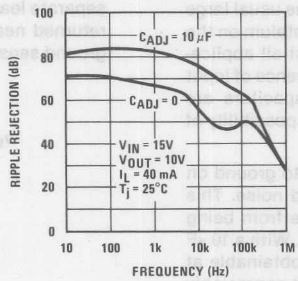
Minimum Operating Current



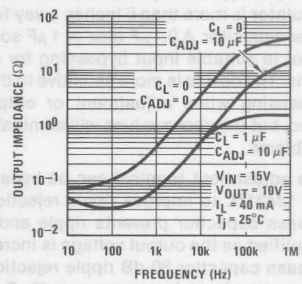
Ripple Rejection



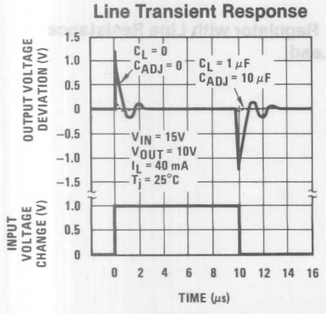
Ripple Rejection



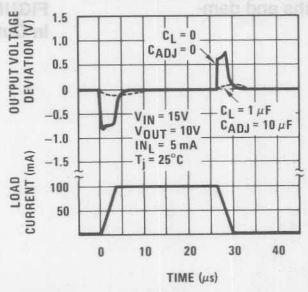
Output Impedance



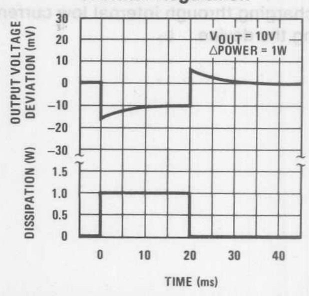
Line Transient Response



Load Transient Response



Thermal Regulation



Application Hints

In operation, the LM317L develops a nominal 1.25V reference voltage, V_{REF}, between the output and adjustment terminal. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R2, giving an output voltage of

$$V_{OUT} = V_{REF} \left(1 + \frac{R2}{R1}\right) + I_{ADJ}R2$$

Since the 100 μA current from the adjustment terminal represents an error term, the LM317L was designed to minimize I_{ADJ} and make it very constant with line and load changes. To do this, all quiescent operating current is returned to the output establishing a minimum load current requirement. If there is insufficient load on the output, the output will rise.

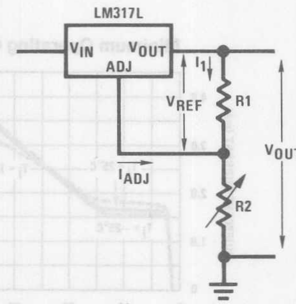


FIGURE 1

External Capacitors

An input bypass capacitor is recommended in case the regulator is more than 6 inches away from the usual large filter capacitor. A 0.1 μF disc or 1 μF solid tantalum on the input is suitable input bypassing for almost all applications. The device is more sensitive to the absence of input bypassing when adjustment or output capacitors are used, but the above values will eliminate the possibility of problems.

The adjustment terminal can be bypassed to ground on the LM317L to improve ripple rejection and noise. This bypass capacitor prevents ripple and noise from being amplified as the output voltage is increased. With a 10 μF bypass capacitor 80 dB ripple rejection is obtainable at any output level. Increases over 10 μF do not appreciably improve the ripple rejection at frequencies above 120 Hz. If the bypass capacitor is used, it is sometimes necessary to include protection diodes to prevent the capacitor from discharging through internal low current paths and damaging the device.

In general, the best type of capacitors to use is solid tantalum. Solid tantalum capacitors have low impedance even at high frequencies. Depending upon capacitor construction, it takes about 25 μF in aluminum electrolytic to equal 1 μF solid tantalum at high frequencies. Ceramic capacitors are also good at high frequencies; but some types have a large decrease in capacitance at frequencies around 0.5 MHz. For this reason, a 0.01 μF disc may seem to work better than a 0.1 μF disc as a bypass.

Although the LM317L is stable with no output capacitors, like any feedback circuit, certain values of external capacitance can cause excessive ringing. This occurs with values between 500 pF and 5000 pF. A 1 μF solid tantalum (or 25 μF aluminum electrolytic) on the output swamps this effect and insures stability.

Load Regulation

The LM317L is capable of providing extremely good load regulation but a few precautions are needed to obtain maximum performance. The current set resistor connected between the adjustment terminal and the output terminal (usually 240Ω) should be tied directly to the output of the regulator rather than near the load. This eliminates line drops from appearing effectively in series with the reference and degrading regulation. For example, a 15V regulator with 0.05Ω resistance between the regulator and load will have a load regulation due to line resistance of $0.05\Omega \times I_L$. If the set resistor is connected near the load the effective line resistance will be 0.05Ω (1 + R2/R1) or in this case, 11.5 times worse.

Figure 2 shows the effect of resistance between the regulator and 240Ω set resistor.

With the TO-92 package, it is easy to minimize the resistance from the case to the set resistor, by using two separate leads to the output pin. The ground of R2 can be returned near the ground of the load to provide remote ground sensing and improve load regulation.

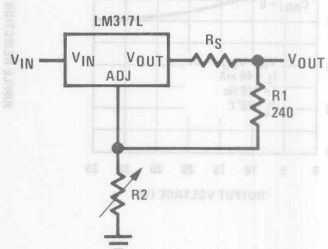


FIGURE 2. Regulator with Line Resistance in Output Lead

Application Hints (Continued)

Thermal Regulation

When power is dissipated in an IC, a temperature gradient occurs across the IC chip affecting the individual IC circuit components. With an IC regulator, this gradient can be especially severe since power dissipation is large. Thermal regulation is the effect of these temperature gradients on output voltage (in percentage output change) per watt of power change in a specified time. Thermal regulation error is independent of electrical regulation or temperature coefficient, and occurs within 5 ms to 50 ms after a change in power dissipation. Thermal regulation depends on IC layout as well as electrical design. The thermal regulation of a voltage regulator is defined as the percentage change of V_{OUT}, per watt, within the first 10 ms after a step of power is applied. The LM317L specification is 0.2%/W, maximum.

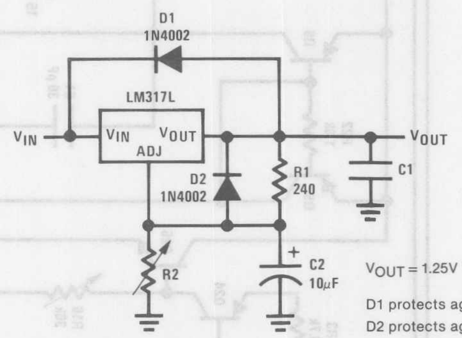
In the Thermal Regulation curve at the bottom of page 3, a typical LM317L's output changes only 7 mV (or 0.07% of $V_{OUT} = -10V$) when a 1W pulse is applied for 10 ms. This performance is thus well inside the specification limit of $0.2\%/W \times 1W = 0.2\%$ maximum. When the 1W pulse is ended, the thermal regulation again shows a 7 mV change as the gradients across the LM317L chip die out. Note that the load regulation error of about 14 mV (0.14%) is additional to the thermal regulation error.

Protection Diodes

When external capacitors are used with *any* IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator. Most 10 μF capacitors have low enough internal series resistance to deliver 20A spikes when shorted. Although the surge is short, there is enough energy to damage parts of the IC.

When an output capacitor is connected to a regulator and the input is shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage of the regulator, and the rate of decrease of V_{IN}. In the LM317L, this discharge path is through a large junction that is able to sustain a 2A surge with no problem. This is not true of other types of positive regulators. For output capacitors of 25 μF or less, the LM317L's ballast resistors and output structure limit the peak current to a low enough level so that there is no need to use a protection diode.

The bypass capacitor on the adjustment terminal can discharge through a low current junction. Discharge occurs when *either* the input or output is shorted. Internal to the LM317L is a 50Ω resistor which limits the peak discharge current. No protection is needed for output voltages of 25V or less and 10 μF capacitance. *Figure 3* shows an LM317L with protection diodes included for use with outputs greater than 25V and high values of output capacitance.

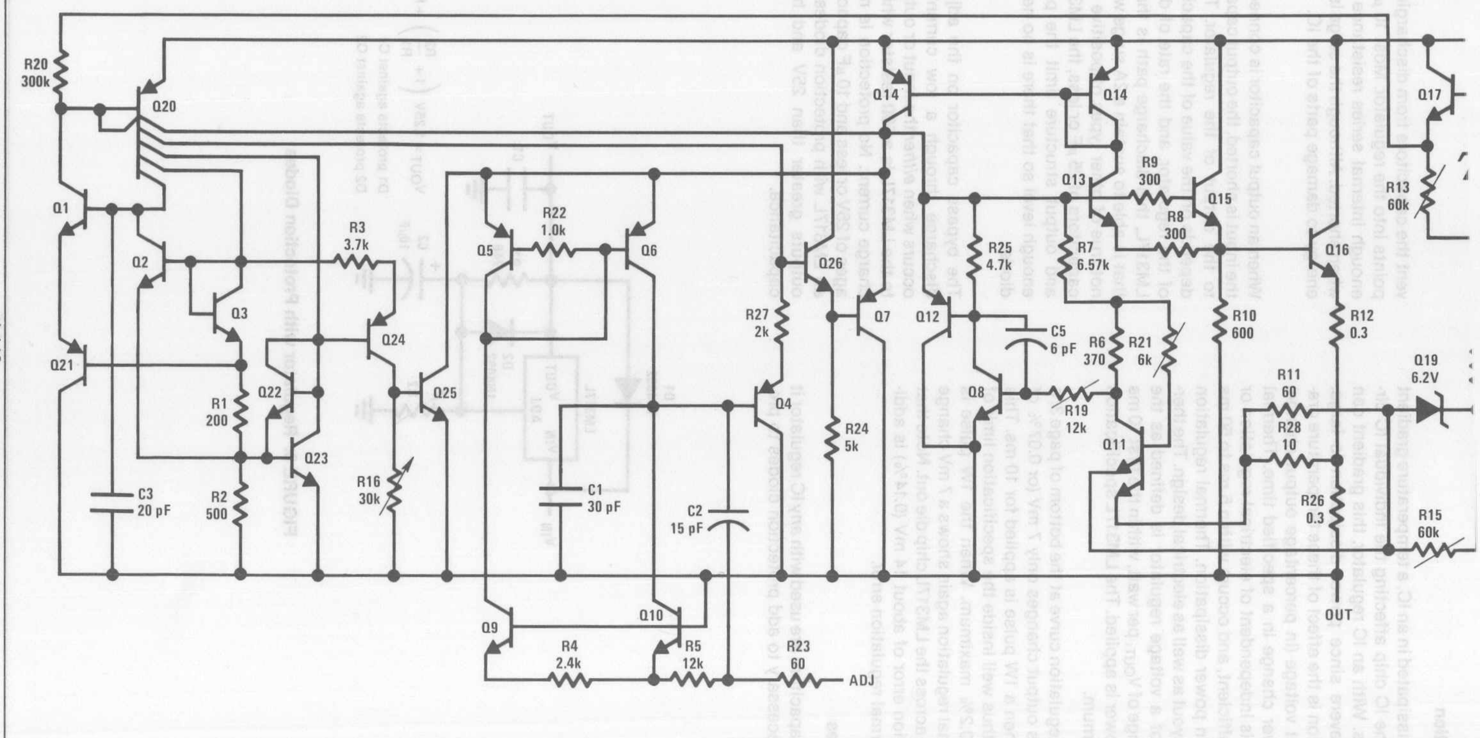


$$V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right) + R2\,I_{ADJ}$$

D1 protects against C1

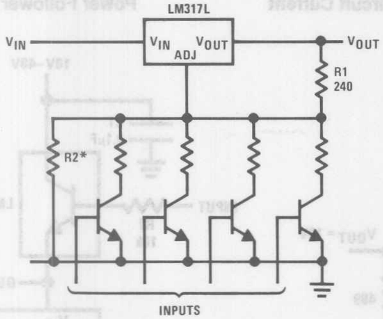
D2 protects against C2

FIGURE 3. Regulator with Protection Diodes


R20
300k
Q20
Q1
Q2
Q21
Q3
R3
3.7k
Q24
Q22
R1
200
Q23
R2
500
C3
20 pF
R16
30k
Q25
Q5
R22
1.0k
Q6
C1
30 pF
Q9
R4
2.4k
Q10
R5
12k
C2
15 pF
R23
60
ADJ
Q4
R27
2k
Q26
Q7
R24
5k
Q14
Q14
R25
4.7k
Q13
R9
300
R8
300
R7
6.57k
Q12
C5
6 pF
R6
370
R21
6k
Q8
R19
12k
Q11
Q15
R10
600
Q16
R12
0.3
R11
60
R28
10
R26
0.3
OUT
Q17
R13
60k
Q19
6.2V
R15
60k

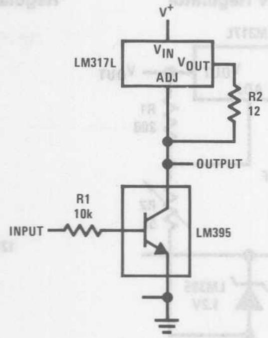
Typical Applications (Continued)

Digitally Selected Outputs

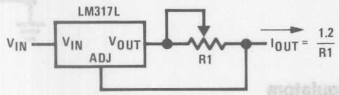


* Sets maximum V_{OUT}

High Gain Amplifier

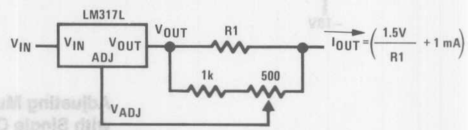


Adjustable Current Limiter

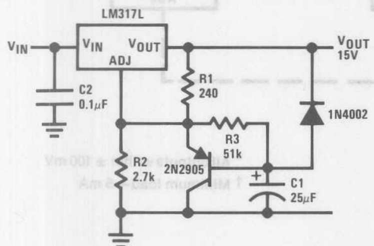


$12 \leq R1 \leq 240$

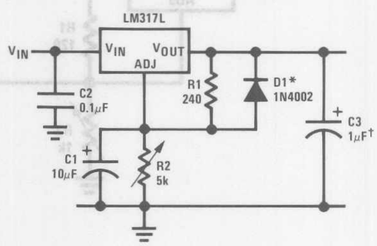
Precision Current Limiter



Slow Turn-On 15V Regulator



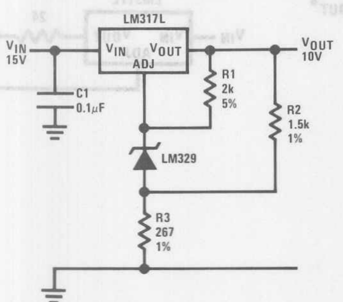
Adjustable Regulator with Improved Ripple Rejection



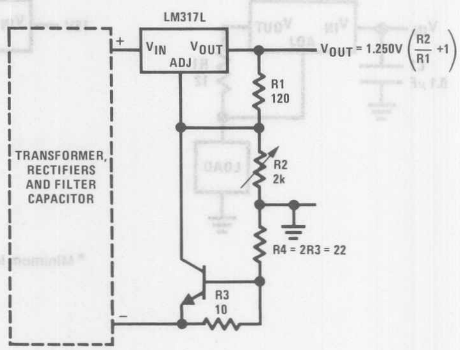
† Solid tantalum

* Discharges C1 if output is shorted to ground

High Stability 10V Regulator



Adjustable Regulator with Current Limiter

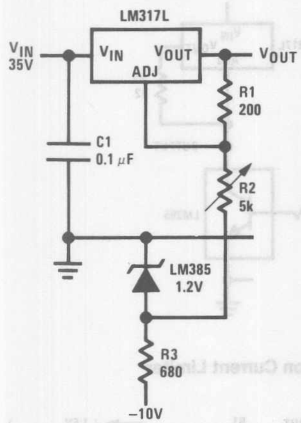


Short circuit current is approximately 600 mV/R3, or 60 mA (compared to LM317LZ's 200 mA current limit).

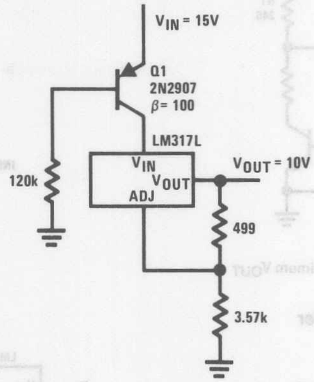
At 25 mA output only 3/4V of drop occurs in R3 and R4.

Typical Applications (Continued)

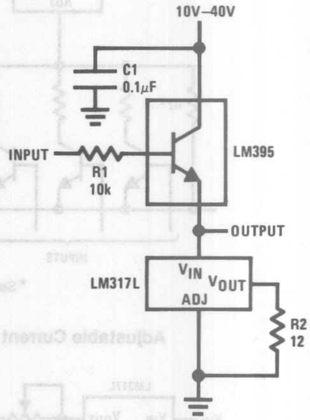
0V–30V Regulator



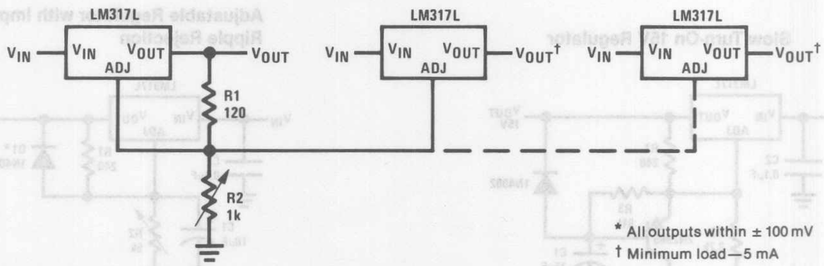
Regulator With 15 mA Short Circuit Current



Power Follower

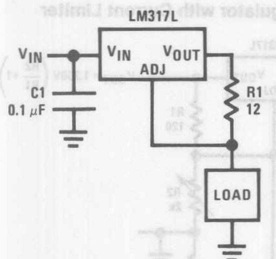


Adjusting Multiple On-Card Regulators with Single Control*

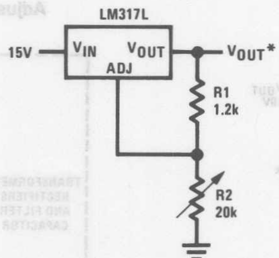


* All outputs within ± 100 mV
† Minimum load—5 mA

100 mA Current Regulator

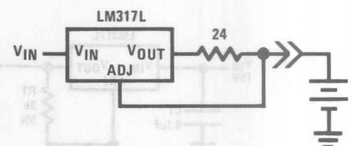


1.2V–12V Regulator with Minimum Program Current



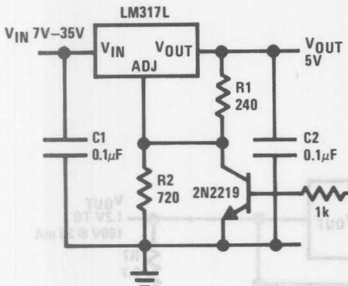
* Minimum load current ≈ 2 mA

50 mA Constant Current Battery Charger for Nickel-Cadmium Batteries



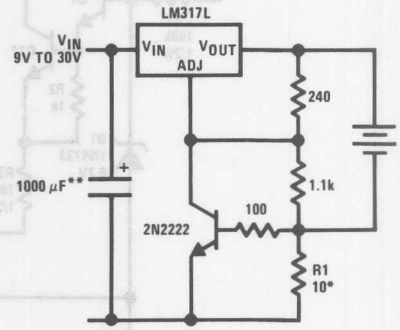
Typical Applications (Continued)

5V Logic Regulator with Electronic Shutdown*



*Minimum output ≈ 1.2V

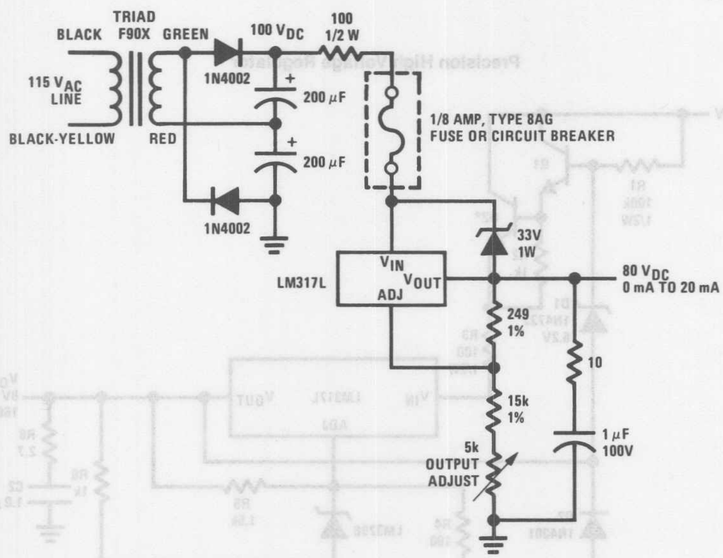
Current Limited 6V Charger



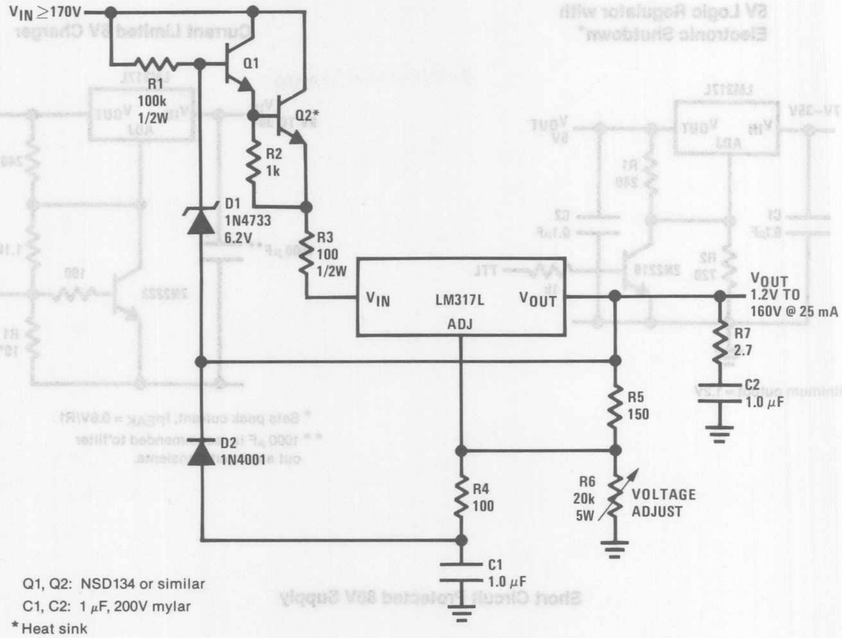
* Sets peak current, $I_{PEAK} = 0.6V/R1$

** 1000 µF is recommended to filter out any input transients.

Short Circuit Protected 80V Supply

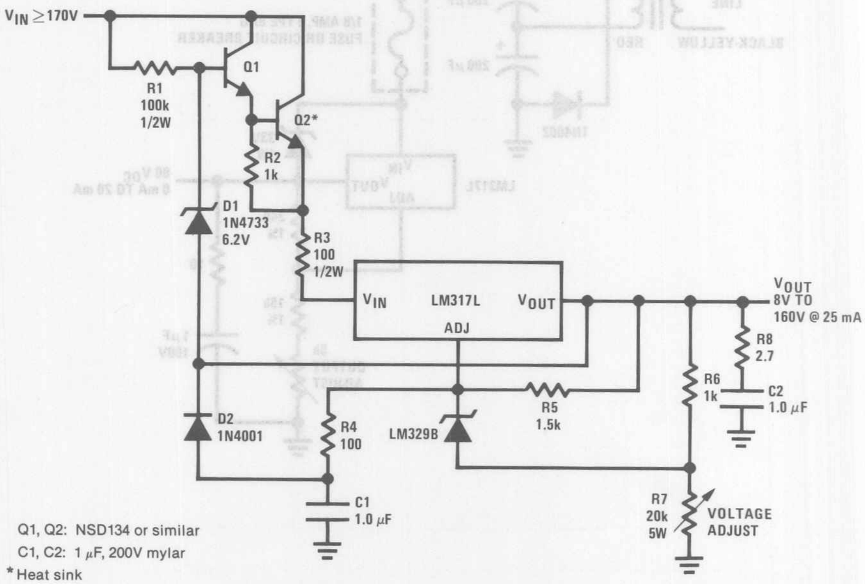


Basic High Voltage Regulator



Q1, Q2: NSD134 or similar
C1, C2: 1 µF, 200V mylar
*Heat sink

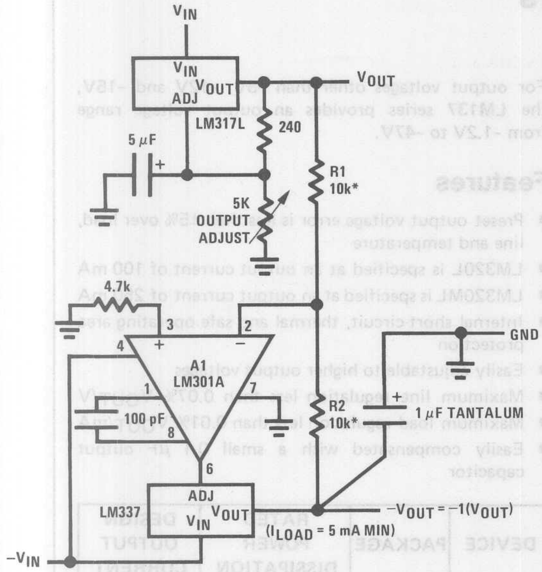
Precision High Voltage Regulator



Q1, Q2: NSD134 or similar
C1, C2: 1 µF, 200V mylar
*Heat sink

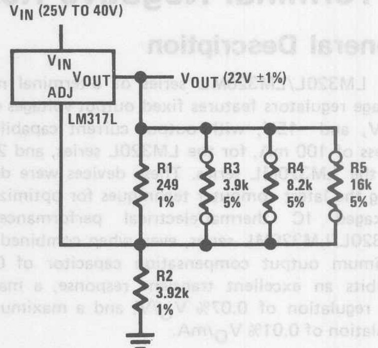
Typical Applications (Continued)

Tracking Regulator



A1 = LM301A, LM307, or LF13741 only
R1, R2—matched resistors with good TC tracking

Regulator with Trimmable Output Voltage



Trim Procedure:

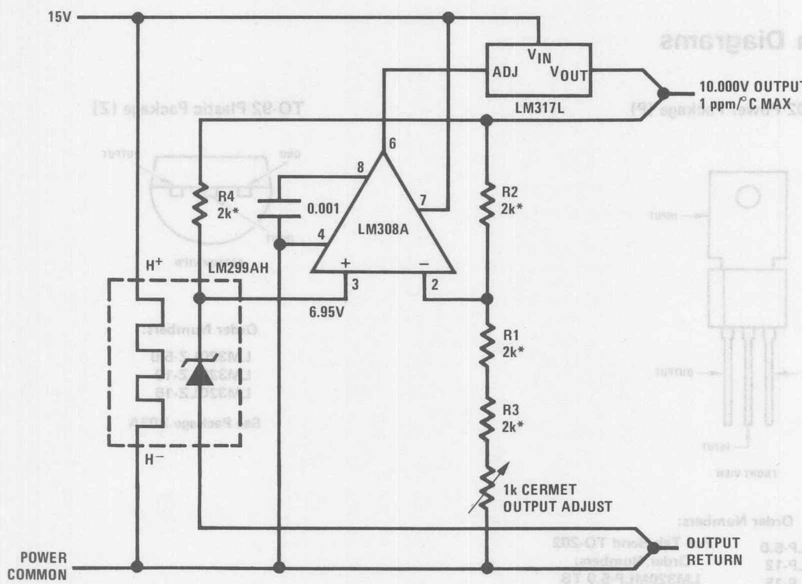
—If V_{OUT} is 23.08V or higher, cut out R3 (if lower, don't cut it out).

—Then if V_{OUT} is 22.47V or higher, cut out R4 (if lower, don't).

—Then if V_{OUT} is 22.16V or higher, cut out R5 (if lower, don't).

This will trim the output to well within ±1% of 22.00 V_{DC}, without any of the expense or uncertainty of a trim pot (see LB-46). Of course, this technique can be used at any output voltage level.

Precision Reference with Short-Circuit-Proof Output



*R1–R4 from thin-film network, Beckman 694-3-R2K-D or similar

National Semiconductor

LM320L/LM320ML Series 3-Terminal Negative Regulators

General Description

The LM320L/LM320ML series of 3-terminal negative voltage regulators features fixed output voltages of -5V, -12V, and -15V, with output current capabilities in excess of 100 mA, for the LM320L series, and 250 mA for the LM320ML series. These devices were designed using the latest computer techniques for optimizing the packaged IC thermal/electrical performance. The LM320L/LM320ML series, even when combined with a minimum output compensation capacitor of 0.1 μF, exhibits an excellent transient response, a maximum line regulation of 0.07% V_O/V, and a maximum load regulation of 0.01% V_O/mA.

The LM320L/LM320ML series also includes, as self-protection circuitry: safe operating area circuitry for output transistor power dissipation limiting, a temperature independent short circuit current limit for peak output current limiting, and a thermal shutdown circuit to prevent excessive junction temperature. Although designed primarily as fixed voltage regulators, these devices may be combined with simple external circuitry for boosted and/or adjustable voltages and currents. The LM320L series is available in the 3-lead TO-92 package, and the LM320ML series is available in the 3-lead TO-202 package.

For output voltages other than -5V, -12V and -15V, the LM137 series provides an output voltage range from -1.2V to -47V.

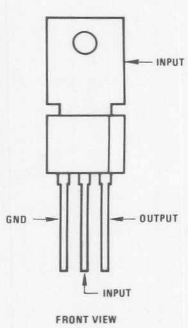
Features

- Preset output voltage error is less than ±5% over load, line and temperature
- LM320L is specified at an output current of 100 mA
- LM320ML is specified at an output current of 250 mA
- Internal short-circuit, thermal and safe operating area protection
- Easily adjustable to higher output voltages
- Maximum line regulation less than 0.07% V_{OUT}/V
- Maximum load regulation less than 0.01% V_{OUT}/mA
- Easily compensated with a small 0.1 μF output capacitor

DEVICE	PACKAGE	RATED POWER DISSIPATION	DESIGN OUTPUT CURRENT
LM320ML	TO-202	7.5W	0.25A
LM320L	TO-92	0.6W	0.1A

Connection Diagrams

TO-202 Power Package (P)



Order Numbers:

LM320MLP-5.0
LM320MLP-12
LM320MLP-15

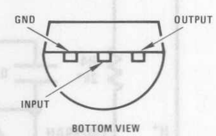
See Package P03A

For Tab Bend TO-202 Order Numbers:

LM320MLP-5.0 TB
LM320MLP-12 TB
LM320MLP-15 TB

See Package P03E

TO-92 Plastic Package (Z)



Order Numbers:

LM320LZ-5.0
LM320LZ-12
LM320LZ-15

See Package Z03A

Input Voltage
$V_{OUT} = -5V$ 12V and 15V — −35V
Internal Power Dissipation (Notes 1 and 3) — Internally Limited
Operating Temperature Range — 0°C to +70°C
Maximum Junction Temperature — +125°C
Storage Temperature Range
Molded TO-92 — −55°C to +150°C
Molded TO-202 — −65°C to +150°C
Lead Temperature (Soldering, 10 seconds) — 300°C

Electrical Characteristics LM320ML (Note 2) $T_A = 0°C$ to +70°C unless otherwise noted.

OUTPUT VOLTAGE				−5V			−12V			−15V		UNITS
INPUT VOLTAGE (unless otherwise noted)				−10V			−17V			−20V		
	PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_O	Output Voltage	$T_j = 25°C$, $I_O = 250$ mA	−5.2	−5	−4.8	−12.5	−12	−11.5	−15.6	−15	−14.4	
		1 mA ≤ I_O ≤ 250 mA ($V_{MIN} \leq V_{IN} \leq V_{MAX}$)	−5.25 (−20 ≤ V_{IN} ≤ −7.5)		−4.75	−12.6 (−27 ≤ V_{IN} ≤ −14.8)		−11.4	−15.75 (−30 ≤ V_{IN} ≤ −18)		−14.25	V
ΔV_O	Line Regulation	$T_j = 25°C$, $I_O = 250$ mA ($V_{MIN} \leq V_{IN} \leq V_{MAX}$)	(−25 ≤ V_{IN} ≤ −7.3)		50	(−30 ≤ V_{IN} ≤ 14.6)		40	(−30 ≤ V_{IN} ≤ 17.7)		40	mV V
ΔV_O	Load Regulation	$T_j = 25°C$ 1 mA ≤ I_O ≤ 250 mA			50			120			150	mV
ΔV_O	Long Term Stability	$I_O = 250$ mA		20			48			60		mV/khr
I_Q	Quiescent Current	$I_O = 250$ mA		2	6		2	6		2	6	mA
ΔI_Q	Quiescent Current Change	1 mA ≤ I_O ≤ 250 mA			0.3		0.3		0.3			mA
		$I_O = 250$ mA ($V_{MIN} \leq V_{IN} \leq V_{MAX}$)	(−20 ≤ V_{IN} ≤ −7.5)		0.25	(−27 ≤ V_{IN} ≤ −14.8)		0.25	(−30 ≤ V_{IN} ≤ −18)		0.25	V
V_n	Output Noise Voltage	$T_j = 25°C$, $I_O = 250$ mA f = 10 Hz-10 kHz		40			100			120		µV
$\frac{\Delta V_{IN}}{\Delta V_O}$	Ripple Rejection	$T_j = 25°C$, $I_O = 250$ mA f = 120 Hz	54			56			54			dB
	Input Voltage Required to Maintain Line Regulation	$T_j = 25°C$ $I_O = 250$ mA			−7.3			−14.6			−17.7	V

Note 1: Thermal resistance of the TO-202 Package (P) without a heat sink is 12°C/W junction to case and 70°C/W case to ambient.

Note 2: To ensure constant junction temperature, low duty cycle pulse testing is used.

Note 3: Thermal resistance, junction to ambient, of the TO-92 (Z) Package is 180°C/W when mounted with 0.40 inch leads on a PC board, and 160°C/W when mounted with 0.25 inch leads on a PC board.

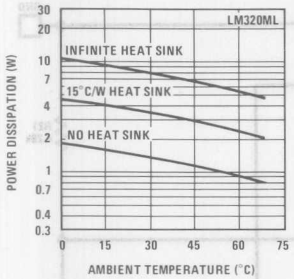
Electrical Characteristics LM320L (Note 4) $T_A = 0°C$ to $+70°C$ unless otherwise noted.

OUTPUT VOLTAGE				−5V			−12V			−15V		
INPUT VOLTAGE (unless otherwise noted)				−10V			−17V			−20V		UNITS
PARAMETER		CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_O	Output Voltage	$Tj = 25°C$, $I_O = 100$ mA	−5.2	−5	−4.8	−12.5	−12	−11.5	−15.6	−15	−14.4	
		1mA $\leq I_O \leq$ 100 mA $V_{MIN} \leq V_{IN} \leq V_{MAX}$	−5.25	$(-20 \leq V_{IN} \leq -7.5)$	−4.75	−12.6	$(-27 \leq V_{IN} \leq -14.8)$	−11.4	−15.75	$(-30 \leq V_{IN} \leq -18)$	−14.25	V
		1 mA $\leq I_O \leq$ 40 mA $V_{MIN} \leq V_{IN} \leq V_{MAX}$	−5.25	$(-20 \leq V_{IN} \leq -7)$	−4.75	−12.6	$(-27 \leq V_{IN} \leq -14.5)$	−11.4	−15.75	$(-30 \leq V_{IN} \leq -17.5)$	−14.25	
ΔV_O	Line Regulation	$Tj = 25°C$, $I_O = 100$ mA $V_{MIN} \leq V_{IN} \leq V_{MAX}$		$(-20 \leq V_{IN} \leq -7.3)$	60		$(-27 \leq V_{IN} \leq -14.6)$	45		$(-30 \leq V_{IN} \leq -17.7)$	45	mV V
		$Tj = 25°C$, $I_O = 40$ mA $V_{MIN} \leq V_{IN} \leq V_{MAX}$		$(-20 \leq V_{IN} \leq -7)$	60		$(-27 \leq V_{IN} \leq -14.5)$	45		$(-30 \leq V_{IN} \leq -17.5)$	45	mV V
ΔV_O	Load Regulation	$Tj = 25°C$ 1 mA $\leq I_O \leq$ 100 mA			50			100			125	mV
ΔV_O	Long Term Stability	$I_O = 100$ mA		20			48			60		mV/khr
I_Q	Quiescent Current	$I_O = 100$ mA		2	6		2	6		2	6	mA
ΔI_Q	Quiescent Current Change	1 mA $\leq I_O \leq$ 100 mA			0.3			0.3			0.3	mA
		1 mA $\leq I_O \leq$ 40 mA			0.1			0.1			0.1	
		$I_O = 100$ mA $V_{MIN} \leq V_{IN} \leq V_{MAX}$		$(-20 \leq V_{IN} \leq -7.5)$	0.25		$(-27 \leq V_{IN} \leq -14.8)$	0.25		$(-30 \leq V_{IN} \leq -18)$	0.25	mA V
V_n	Output Noise Voltage	$Tj = 25°$, $I_O = 100$ mA f = 10 Hz–10 kHz		40			96			120		µV
$\frac{\Delta V_{IN}}{\Delta V_O}$	Ripple Rejection	$Tj = 25°C$, $I_O = 100$ mA f = 120 Hz	50			52			50			dB
	Input Voltage Required to Maintain Line Regulation	$Tj = 25°$ $I_O = 100$ mA $I_O = 40$ mA			 −7.3 −7.0			 −14.6 −14.5			 −17.7 −17.5	V

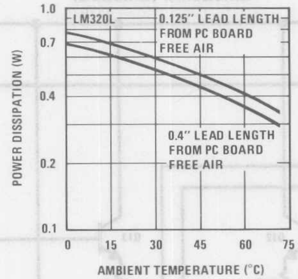
Note 4: To ensure constant junction temperature, low duty cycle pulse testing is used.

Typical Performance Characteristics

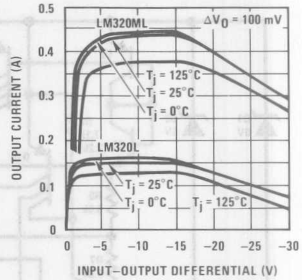
Maximum Average Power Dissipation (TO-202)



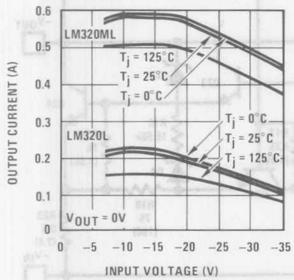
Maximum Average Power Dissipation (TO-92)



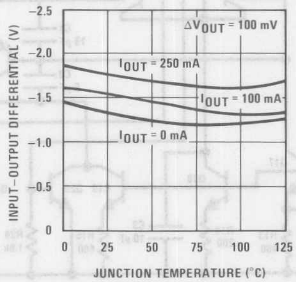
Peak Output Current



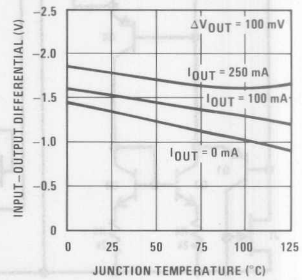
Short-Circuit Output Current



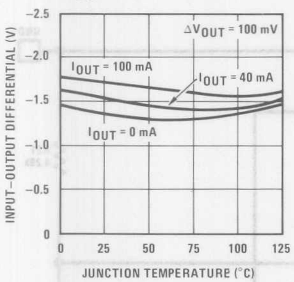
Dropout Voltage, LM320ML, –5V



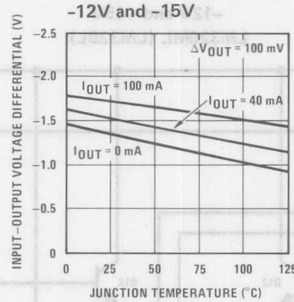
Dropout Voltage, LM320ML, -12V and -15V



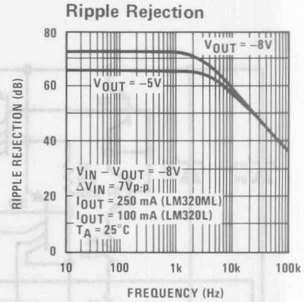
Dropout Voltage, LM320L –5V



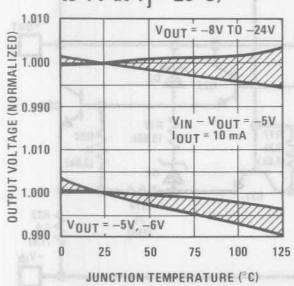
Dropout Voltage, LM320L -12V and -15V



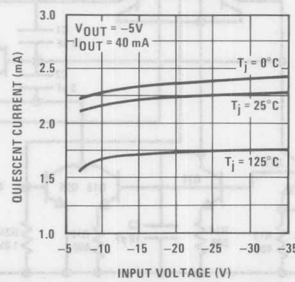
Ripple Rejection



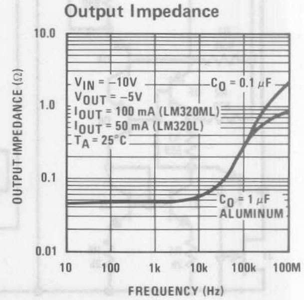
Output Voltage vs. Temperature (Normalized to 1V at $T_j = 25°C$)



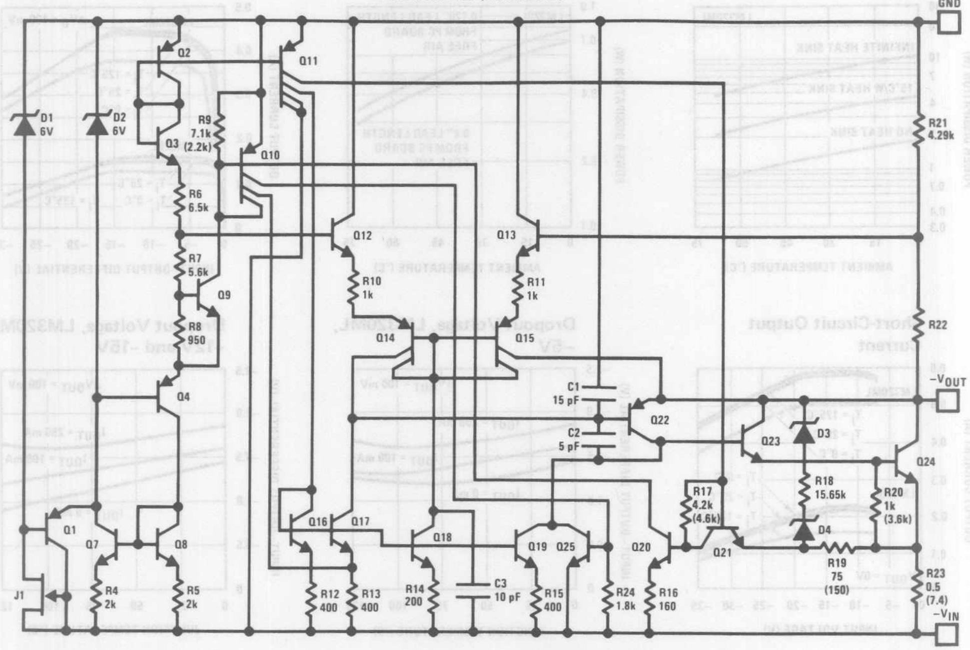
Quiescent Current



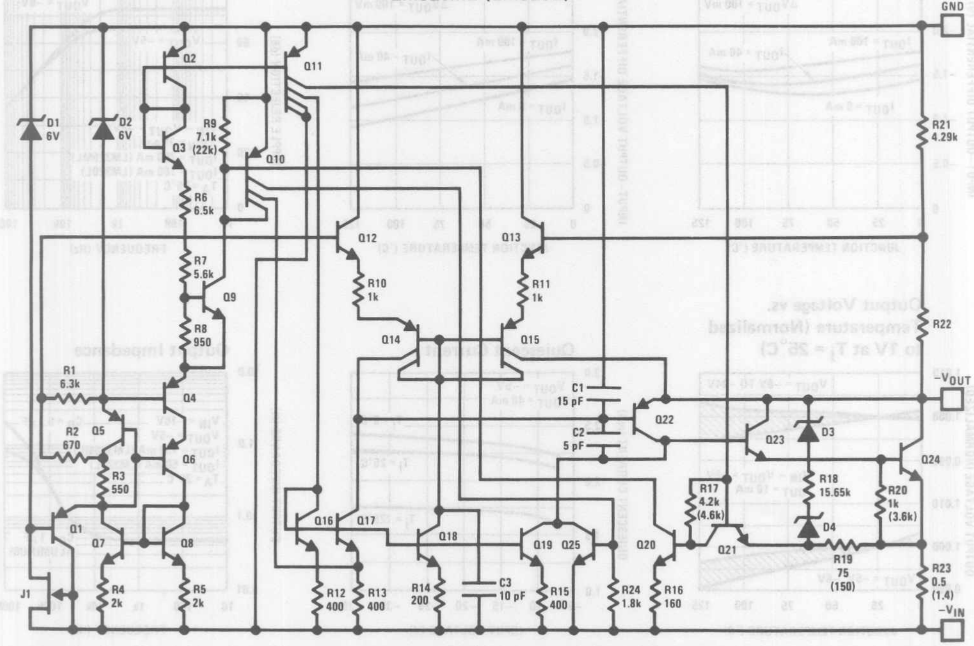
Output Impedance



LM320ML (LM320L)

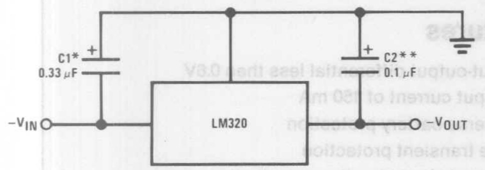


−12V and −15V
LM320ML (LM320L)



Typical Applications

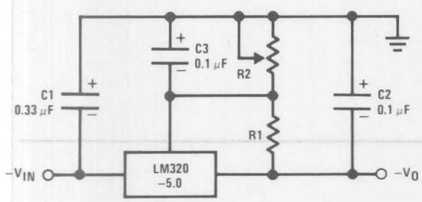
Fixed Output Regulator



*Required if the regulator is located far from the power supply filter. A 1 μF aluminum electrolytic may be substituted.

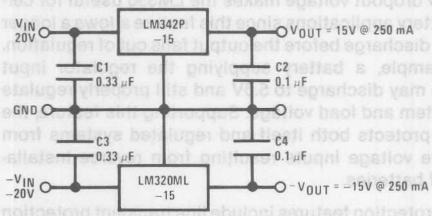
**Required for stability. A 1 μF aluminum electrolytic may be substituted.

Adjustable Output Regulator



$-V_O = -5V - (5V/R1 + I_Q) \cdot R2,$
$5V/R1 > 3\ I_Q$

±15V, 250 mA Dual Power Supply



National Semiconductor

Voltage Regulators

LM330 3-Terminal Positive Regulator

General Description

The LM330 5V 3-terminal positive voltage regulator features an ability to source 150 mA of output current with an input-output differential of 0.6V or less. Familiar regulator features such as current limit and thermal overload protection are also provided.

The low dropout voltage makes the LM330 useful for certain battery applications since this feature allows a longer battery discharge before the output falls out of regulation. For example, a battery supplying the regulator input voltage may discharge to 5.6V and still properly regulate the system and load voltage. Supporting this feature, the LM330 protects both itself and regulated systems from negative voltage inputs resulting from reverse installations of batteries.

Other protection features include line transient protection up to 26V, when the output actually shuts down to avoid damaging internal and external circuits. Also, the LM330 regulator cannot be harmed by a temporary mirror-image insertion.

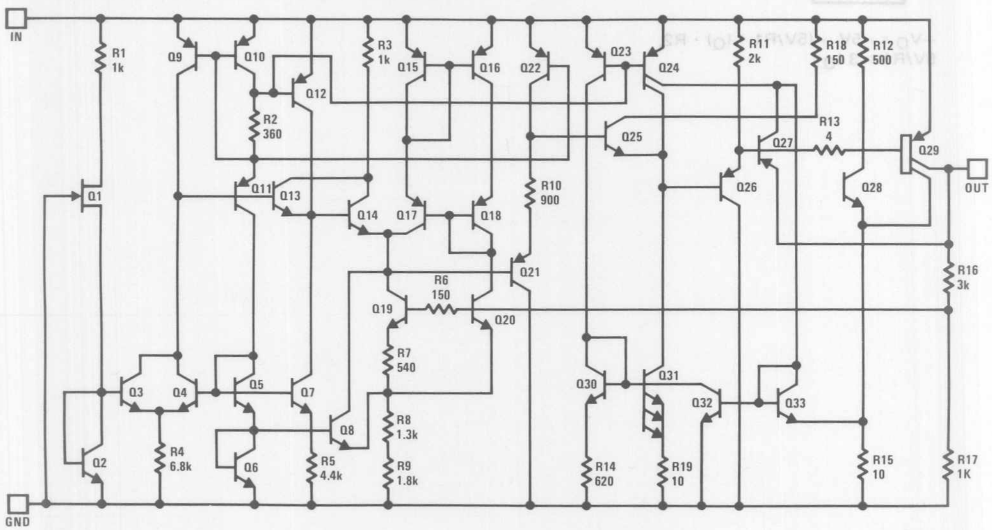
Features

- Input-output differential less than 0.6V
- Output current of 150 mA
- Reverse battery protection
- Line transient protection
- Internal short circuit current limit
- Internal thermal overload protection
- Mirror-image insertion protection
- 100% electrical burn-in in the thermal limit

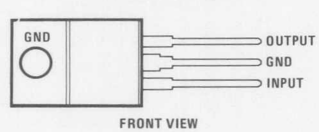
Voltage Range

LM330T-5.0 5V

Schematic and Connection Diagrams



(TO-220)
Plastic Package



Order Number LM330T-5.0
See NS Package T03B

Absolute Maximum Ratings

Input Voltage	
Operating Range	26V
Line Transient Protection (1000 ms)	40V
Internal Power Dissipation	Internally Limited
Operating Temperature Range	0°C to +70°C
Maximum Junction Temperature	+125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

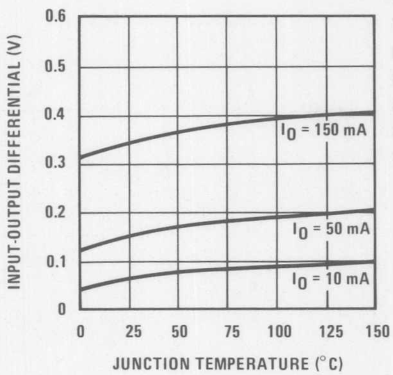
Electrical Characteristics (Note 1)

	Parameter	Conditions	Min	Typ	Max	Units
V_o	Output Voltage	$T_j = 25°C$	4.8	5	5.2	V
	Output Voltage Over Temp	$5 < I_o < 150$ mA $6 < V_{IN} < 26V$; $0°C \le T_j \le 100°C$	4.75		5.25	V
ΔV_o	Line Regulation	$9 < V_{IN} < 16V$, $I_o = 5$ mA $6 < V_{IN} < 26V$, $I_o = 5$ mA		7 30	25 60	mV
	Load Regulation	$5 < I_o < 150$ mA		14	50	mV
	Long Term Stability			20		mV/1000 hrs
I_Q	Quiescent Current	$I_o = 10$ mA $I_o = 50$ mA $I_o = 150$ mA		3.5 5 18	7 11 40	mA
	Line Transient Reverse Polarity	$V_{IN} = 40V$, $R_L = 100\Omega$, 1 sec $V_{IN} = -6V$, $R_L = 100\Omega$		14 −80		mA
ΔI_Q	Quiescent Current Change	$6 < V_{IN} < 26V$		10		%
V_{IN}	Overvoltage Shutdown Voltage		26	30		V
	Max Line Transient	100 ms $V_o \le 5.5V$ 1 sec $V_o \le 5.5V$		60 50		V
	Reverse Polarity Input Voltage	100 ms $V_o > -0.3V$ $R_L = 100\Omega$ DC $V_o > -0.3V$ $R_L = 100\Omega$		−30 −12		V
	Output Noise Voltage	10 Hz–100 kHz		50		μV
	Output Impedance	$I_o = 100$ mADC + 10 mArms		200		mΩ
	Ripple Rejection			56		dB
	Current Limit		150	400	700	mA
	Dropout Voltage	$I_o = 150$ mA		0.32	0.6	V
	Thermal Resistance	Junction to Case Junction to Ambient		4 50		°C/W

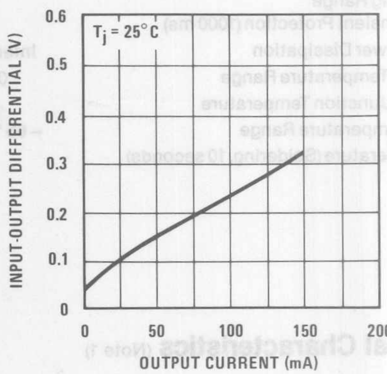
Note 1: Unless otherwise specified: $V_{IN} = 14V$, $I_O = 150$ mA, $T_j = 25°C$, C1 = 0.1 μF, C2 = 10 μF. All characteristics except noise voltage and ripple rejection are measured using pulse techniques ($t_w \le 10$ ms, duty cycle $\le 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately.

Typical Performance Characteristics

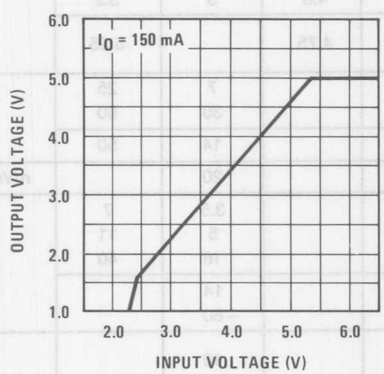
Dropout Voltage



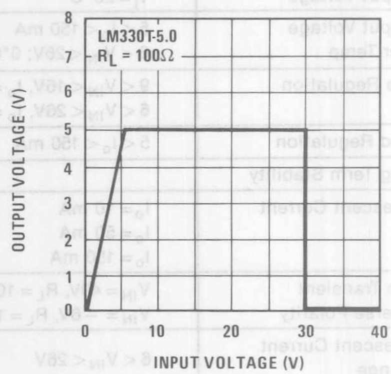
Dropout Voltage



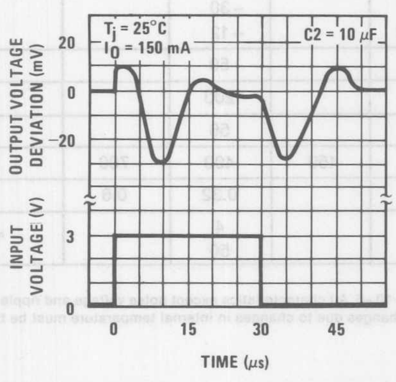
Low Voltage Behavior



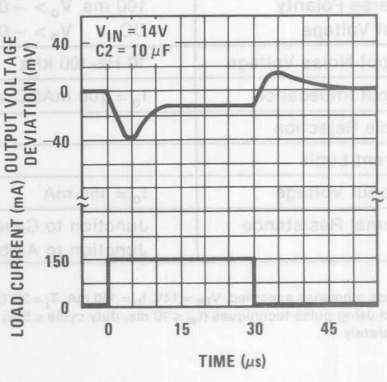
High Voltage Behavior



Line Transient Response

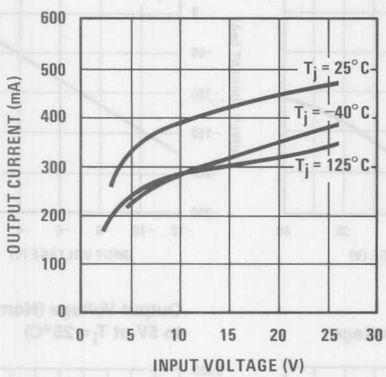


Load Transient Response

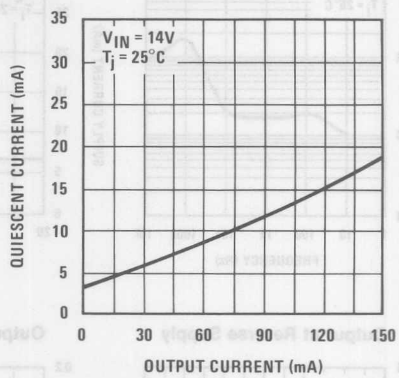


Typical Performance Characteristics (Continued)

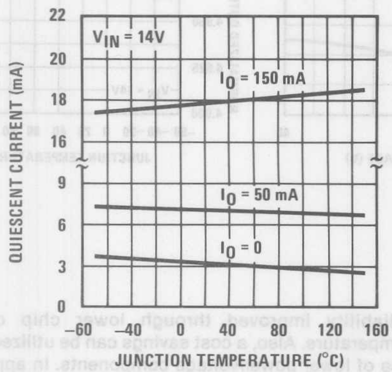
Peak Output Current



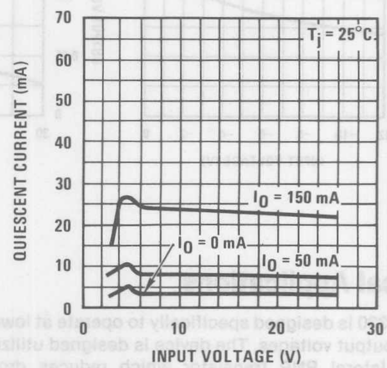
Quiescent Current



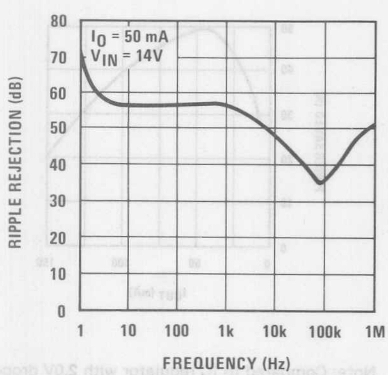
Quiescent Current



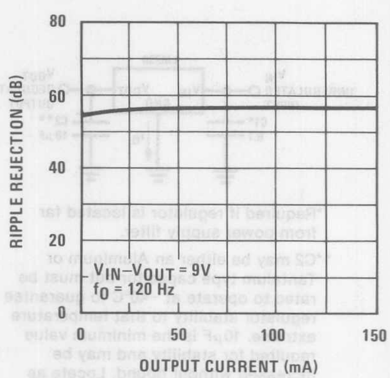
Quiescent Current



Ripple Rejection



Ripple Rejection



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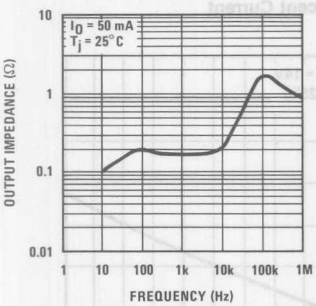
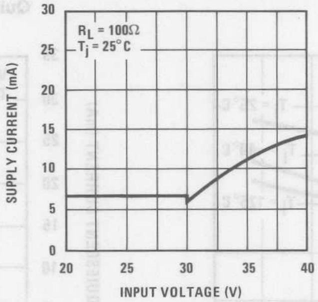
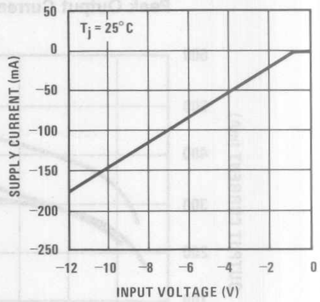
Output Impedance



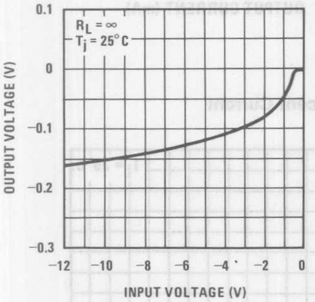
Overvoltage Supply Current



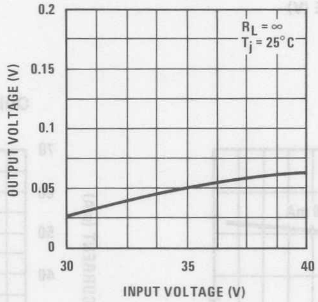
Reverse Supply Current



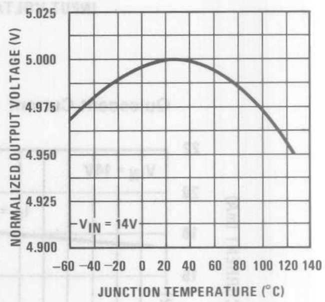
Output at Reverse Supply



Output at Overvoltage

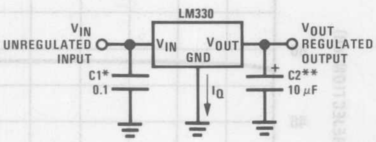


Output Voltage (Normalized to 5V at T_j = 25°C)



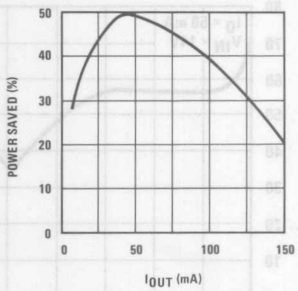
Typical Applications

The LM330 is designed specifically to operate at lower input to output voltages. The device is designed utilizing a power lateral PNP transistor which reduces dropout voltage from 2.0V to 0.3V when compared to IC regulators using NPN pass transistors. Since the LM330 can operate at a much lower input voltage, the device power dissipation is reduced, heat sinking can be simpler and device reliability improved through lower chip operating temperature. Also, a cost savings can be utilized through use of lower power/voltage components. In applications utilizing battery power, the LM330 allows the battery voltage to drop to within 0.3V of output voltage prior to the voltage regulator dropping out of regulation.



*Required if regulator is located far from power supply filter.

**C2 may be either an Aluminum or Tantalum type capacitor but must be rated to operate at −40°C to guarantee regulator stability to that temperature extreme. 10 μF is the minimum value required for stability and may be increased without bound. Locate as close as possible to the regulation.



Note: Compared to IC regulator with 2.0V dropout voltage and $I_{Qmax.}$ = 6.0 mA.

Definition of Terms

Dropout Voltage: The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14V input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Input-Output Differential: The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Long Term Stability: Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

Output Noise Voltage: The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Quiescent Current: That part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

Ripple Rejection: The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

Temperature Stability of V_O: The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

National Semiconductor

Voltage Regulators

PRELIMINARY

LM337L 3-Terminal Adjustable Regulator

General Description

The LM337L is an adjustable 3-terminal negative voltage regulator capable of supplying 100 mA over a 1.2V to 37V output range. It is exceptionally easy to use and requires only two external resistors to set the output voltage. Furthermore, both line and load regulation are better than standard fixed regulators. Also, the LM337L is packaged in a standard TO-92 transistor package which is easy to use.

In addition to higher performance than fixed regulators, the LM337L offers full overload protection. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

Features

- Adjustable output down to 1.2V
- Guaranteed 100 mA output current
- Line regulation typically 0.01%/V
- Load regulation typically 0.1%
- Current limit constant with temperature
- Eliminates the need to stock many voltages
- Standard 3-lead transistor package
- 80 dB ripple rejection

Normally, only a single 1 μF solid tantalum output capacitor is needed unless the device is situated far from the input filter capacitors, in which case an input bypass is needed. A larger output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejection ratios which are difficult to achieve with standard 3-terminal regulators.

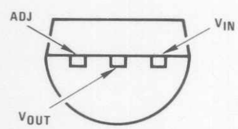
Besides replacing fixed regulators, the LM337L is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input-to-output differential is not exceeded.

Also, it makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM337L can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2V where most loads draw little current.

The LM337L is packaged in a standard TO-92 transistor package. The LM337L is rated for operation over a −25°C to +125°C range.

For applications requiring greater output current in excess of 0.5A and 1.5A, see LM137 series data sheets. For the positive complement, see series LM117 and LM317L data sheets.

Connection Diagram

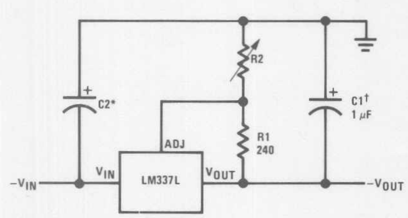


BOTTOM VIEW

Order Number LM337LZ
See NS Package Z03A

Typical Applications

1.2V–25V Adjustable Regulator

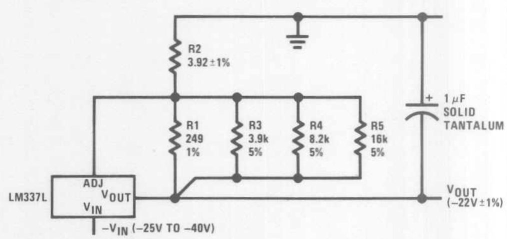


$$-V_{OUT} = -1.25V \left(1 + \frac{R2}{240\Omega}\right)$$

†C1 = 1 μF solid tantalum or 10 μF aluminum electrolytic required for stability

*C2 = 1 μF solid tantalum is required only if regulator is more than 4" from power supply filter capacitor

Regulator with Trimmable Output Voltage



Trim Procedure:

—If V_{OUT} is −23.08V or bigger, cut out R3 (if smaller, don't cut it out).

—Then if V_{OUT} is −22.47V or bigger, cut out R4 (if smaller, don't).

—Then if V_{OUT} is −22.16V or bigger, cut out R5 (if smaller, don't).

This will trim the output to well within 1% of −22.00 V_{DC}, without any of the expense or trouble of a trim pot (see LB-46). Of course, this technique can be used at any output voltage level.

Absolute Maximum Ratings

Power Dissipation	Internally Limited
Input-Output Voltage Differential	40V
Operating Junction Temperature Range	$-25°C$ to $+125°C$
Storage Temperature	$-55°C$ to $+150°C$
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 1)

Parameter	Conditions	Min	Typ	Max	Units
Line Regulation	$T_A = 25°C$, $3V \le \lvert V_{IN}-V_{OUT} \rvert \le 40V$, (Note 2)		0.01	0.04	%/V
Load Regulation	$T_A = 25°C$, $5\ mA \le I_{OUT} \le I_{MAX}$, (Note 2)		0.1	0.5	%
Thermal Regulation	$T_A = 25°C$, 10 ms Pulse		0.04	0.2	%/W
Adjustment Pin Current			50	100	μA
Adjustment Pin Current Change	$5\ mA \le I_L \le 100\ mA$ $3V \le \lvert V_{IN}-V_{OUT} \rvert \le 40V$		0.2	5	μA
Reference Voltage	$3V \le \lvert V_{IN}-V_{OUT} \rvert \le 40V$, (Note 3) $10\ mA \le I_{OUT} \le 100\ mA$, $P \le 625\ mW$	1.20	1.25	1.30	V
Line Regulation	$3V \le \lvert V_{IN}-V_{OUT} \rvert \le 40V$, (Note 2)		0.02	0.07	%/V
Load Regulation	$5\ mA \le I_{OUT} \le 100\ mA$, (Note 2)		0.3	1.5	%
Temperature Stability	$T_{MIN} \le T_j \le T_{MAX}$		0.65		%
Minimum Load Current	$\lvert V_{IN}-V_{OUT} \rvert \le 40V$		3.5	5	mA
	$3V \le \lvert V_{IN}-V_{OUT} \rvert \le 15V$		2.2	3.5	mA
Current Limit	$3V \le \lvert V_{IN}-V_{OUT} \rvert \le 13V$	100	200	320	mA
	$\lvert V_{IN}-V_{OUT} \rvert = 40V$	25	50	120	mA
Rms Output Noise, % of V_{OUT}	$T_A = 25°C$, $10\ Hz \le f \le 10\ kHz$		0.003		%
Ripple Rejection Ratio	$V_{OUT} = -10V$, $f = 120\ Hz$, $C_{ADJ} = 0$		65		dB
	$C_{ADJ} = 10\ \mu F$	66	80		dB
Long-Term Stability	$T_A = 125°C$		0.3	1	%

Note 1: Unless otherwise specified, these specifications apply $-25°C \le T_j \le +125°C$ for the LM337L; $\lvert V_{IN}-V_{OUT} \rvert = 5V$ and $I_{OUT} = 40$ mA. Although power dissipation is internally limited, these specifications are applicable for power dissipations up to 625 mW. I_{MAX} is 100 mA.

Note 2: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.

Note 3: Thermal resistance of the TO-92 package is 180°C/W junction to ambient with 0.4″ leads from a PC board and 160°C/W junction to ambient with 0.125″ lead length to PC board.

LM341 Series 3-Terminal Positive Regulators

General Description

The LM341-XX series of three terminal regulators is available with several fixed output voltages making them useful in a wide range of applications. One of these is local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents.

The LM341-XX series is available in the plastic TO-202 package. This package allows these regulators to deliver over 0.5A if adequate heat sinking is provided. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

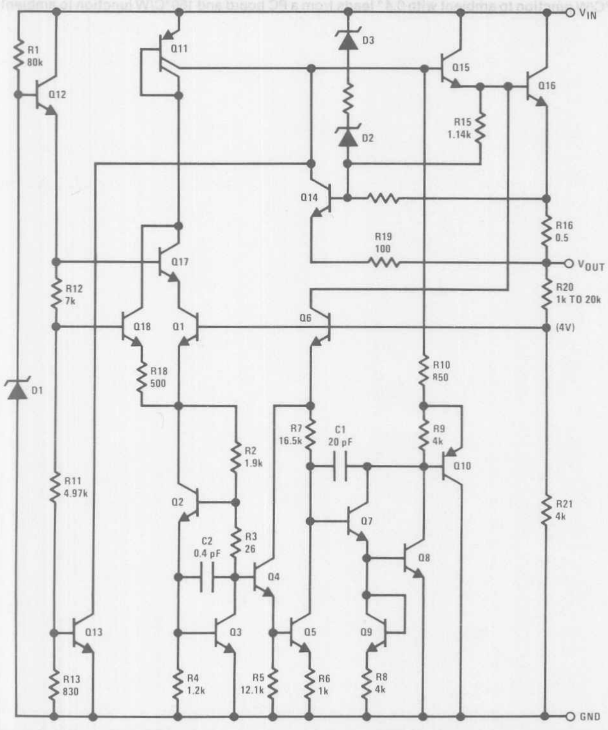
Considerable effort was expended to make the LM341-XX series of regulators easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

For output voltage other than 5V, 12V and 15V the LM117 series provides an output voltage range from 1.2V to 57V.

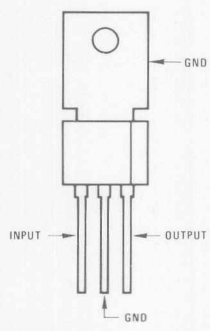
Features

- Output current in excess of 0.5A
- Internal thermal overload protection
- No external components required
- Output transistor safe area protection
- Internal short circuit current limit
- Available in plastic TO-202 package
- Special circuitry allows start-up even if output is pulled to negative voltage (± supplies)

Schematic and Connection Diagrams



Plastic Package



FRONT VIEW

Order Numbers
LM341P-5.0
LM341P-12
LM341P-15
See Package P03A

For Tab Bend TO-202
Order Numbers
LM341P-5.0 TB
LM341P-12 TB
LM341P-15 TB
See Package P03E

Internal Power Dissipation (Note 1)	Internally Limited
Operating Temperature Range	0 °C to + 70 °C
Maximum Junction Temperature	+ 125 °C
Storage Temperature Range	− 65 °C to + 150 °C
Lead Temperature (Soldering, 10 seconds)	+ 230 °C

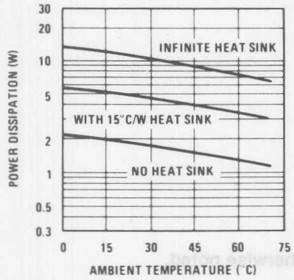
Electrical Characteristics $T_A = 0°C$ to $70°C$, $I_O = 500$ mA, unless otherwise noted.

OUTPUT VOLTAGE			5V			12V			15V			
INPUT VOLTAGE (unless otherwise noted)			10V			19V			23V			UNITS
	PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_O	Output Voltage	Tj = 25 °C	4.8	5	5.2	11.5	12	12.5	14.4	15	15.6	V
		$P_D \leq 7.5W$, $5mA \leq I_O \leq 500mA$ and $V_{MIN} \leq V_{IN} \leq V_{MAX}$	4.75		5.25	11.4		12.6	14.25		15.75	V
			$(7.5 \leq V_{IN} \leq 20)$			$(14.8 \leq V_{IN} \leq 27)$			$(18 \leq V_{IN} \leq 30)$			V
ΔV_O	Line Regulation	Tj = 25 °C, I_O = 100 mA			50			120			150	mV
		Tj = 25 °C, I_O = 500 mA			100			240			300	mV
			$(7.2 \leq V_{IN} \leq 25)$			$(14.5 \leq V_{IN} \leq 30)$			$(17.6 \leq V_{IN} \leq 30)$			V
ΔV_O	Load Regulation	Tj = 25 °C, $5mA \leq I_O \leq 500mA$			100			240			300	mV
ΔV_O	Long Term Stability				20			48			60	mV/khrs
I_Q	Quiescent Current	Tj = 25 °C		4	10		4	10		4	10	mA
ΔI_Q	Quiescent Current Change	Tj = 25 °C, $5mA \leq I_O \leq 500mA$			0.5			0.5			0.5	mA
		Tj = 25 °C, $V_{MIN} \leq V_{IN} \leq V_{MAX}$			1			1			1	mA
			$(7.5 \leq V_{IN} \leq 25)$			$(14.8 \leq V_{IN} \leq 30)$			$(18 \leq V_{IN} \leq 30)$			V
V_n	Output Noise Voltage	Tj = 25 °C, f = 10 Hz – 100kHz		40			75			90		µV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	f = 120 Hz		78			71			69		dB
	Input Voltage Required to Maintain Line Regulation	Tj = 25 °C, I_O = 500 mA	7.2			14.5			17.6			V

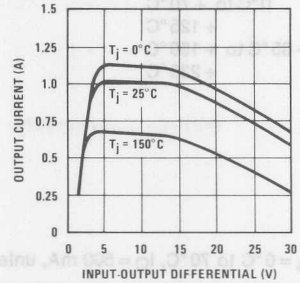
Note 1: Thermal resistance without a heat sink for junction to case temperature is 12 °C/W for the TO-202 package. Thermal resistance for case to ambient temperature is 70 °C/W for the TO-202 package.

Typical Performance Characteristics

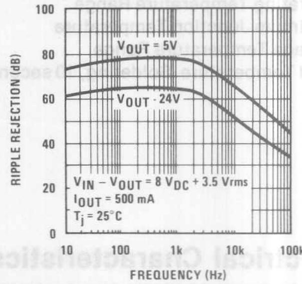
Maximum Average Power Dissipation



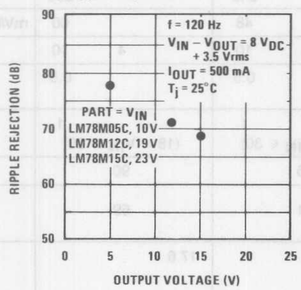
Peak Output Current



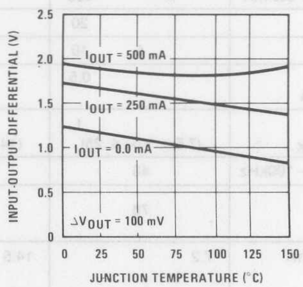
Ripple Rejection



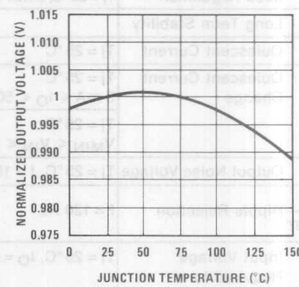
Ripple Rejection



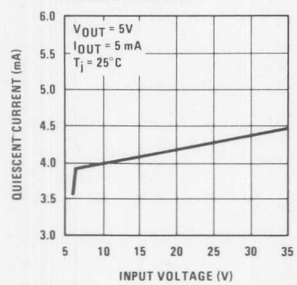
Dropout Voltage



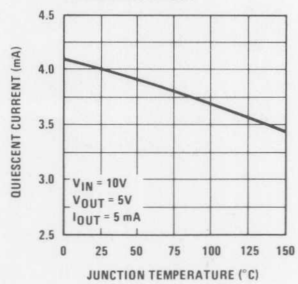
Output Voltage (Normalized to 1V at $T_J = 25°$ C)



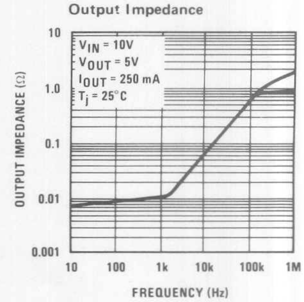
Quiescent Current



Quiescent Current



Output Impedance



National Semiconductor

Voltage Regulators

LM342 Series 3-Terminal Positive Regulators

General Description

The LM342-XX series of three terminal regulators is available with several fixed output voltages making them useful in a wide range of applications. One of these is local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents.

The LM342-XX series is available in the plastic TO-202 package. This package allows these regulators to deliver over 0.25A if adequate heat sinking is provided. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

Considerable effort was expended to make the LM342-XX series of regulators easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

For output voltage other than 5V, 12V and 15V the LM117 series provides an output voltage range from 1.2V to 57V.

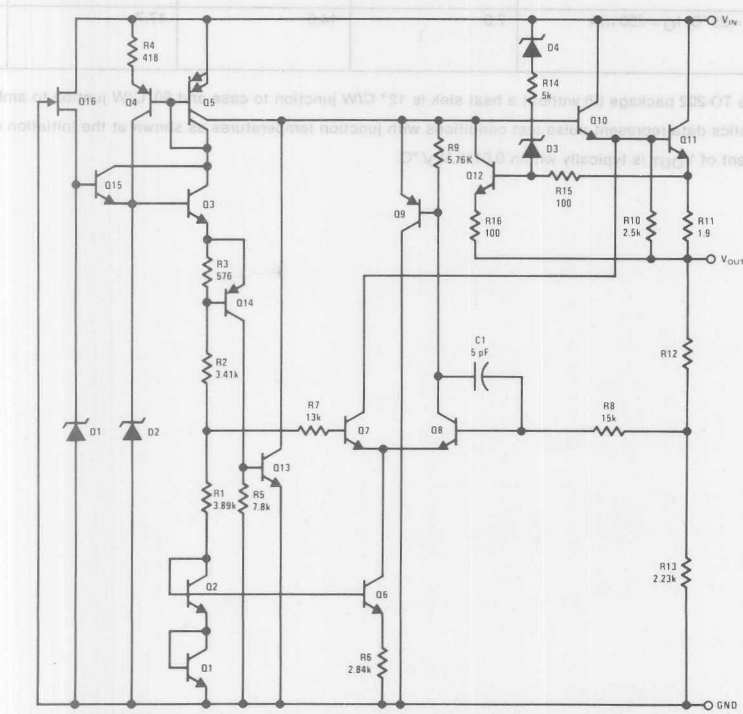
Features

- Output current in excess of 0.25A
- Internal thermal overload protection
- No external components required
- Output transistor safe area protection
- Internal short circuit current limit
- Available in plastic TO-202 package
- Special circuitry allows start-up even if output is pulled to negative voltage (± supplies)

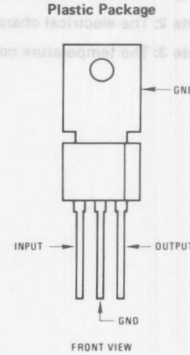
Voltage Range

LM342-5.0	5V
LM342-12	12V
LM342-15	15V

Schematic and Connection Diagrams



Plastic Package



Order Numbers:

LM342P-5.0
LM342P-12
LM342P-15

See Package P03A

For Tab Bend TO-202
Order Numbers:
LM342P-5.0 TB
LM342P-12 TB
LM342P-15 TB
See Package P03E

$V_O = 12V$ and $15V$	35V
Internal Power Dissipation (Note 1)	Internally Limited
Operating Temperature Range	0°C to +70°C
Maximum Junction Temperature	125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 Seconds)	300°C

Electrical Characteristics $T_A = 0°C$ to $+70°C$, $I_O = 250$ mA (Note 2) unless noted.

OUTPUT VOLTAGE			5V			12V			15V			
INPUT VOLTAGE (unless otherwise noted)			10V			19V			23V			UNITS
	PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_O	Output Voltage	$T_j = 25°C$	4.8	5	5.2	11.5	12	12.5	14.4	15	15.6	V
	(Note 3)	1 mA ≤ I_O ≤ 250 mA and	4.75		5.25	11.4		12.6	14.25		15.75	V
		$V_{MIN} \leq V_{IN} \leq V_{MAX}$	(7.5 ≤ V_{IN} ≤ 20)			(14.8 ≤ V_{IN} ≤ 27)			(18 ≤ V_{IN} ≤ 30)			V
ΔV_O	Line Regulation	$T_j = 25°C$, $I_O = 250$ mA			55			100			100	mV
			(7.3 ≤ V_{IN} ≤ 25)			(14.6 ≤ V_{IN} ≤ 30)			(17.7 ≤ V_{IN} ≤ 30)			V
ΔV_O	Load Regulation	$T_j = 25°C$, 1 mA ≤ I_O ≤ 250 mA			50			120			150	mV
ΔV_O	Long Term Stability			20			48			60		mV/khrs
I_Q	Quiescent Current	$T_j = 25°C$			6			6			6	mA
ΔI_Q	Quiescent Current	$T_j = 25°C$, 1 mA ≤ I_O ≤ 250 mA			0.5			0.5			0.5	mA
	Change	$T_j = 25°C$, $V_{MIN} \leq V_{IN} \leq V_{MAX}$			1.5			1.5			1.5	mA
			(7.3 ≤ V_{IN} ≤ 25)			(14.6 ≤ V_{IN} ≤ 30)			(17.7 ≤ V_{IN} ≤ 30)			V
V_n	Output Noise Voltage	$T_j = 25°C$, f = 10 Hz − 10 kHz		40			96			120		µV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	f = 120 Hz	50	64		44	58		42	56		dB
	Input Voltage Required to Maintain Line Regulation	$T_j = 25°C$, $I_O = 250$ mA	7.3			14.6			17.7			V

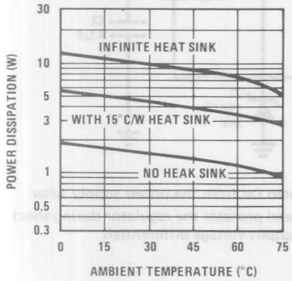
Note 1: Thermal resistance of the TO-202 package (P) without a heat sink is 12° C/W junction to case and 80°C/W juntion to ambient.

Note 2: The electrical characteristics data represent pulse test conditions with junction temperatures as shown at the initiation of tests.

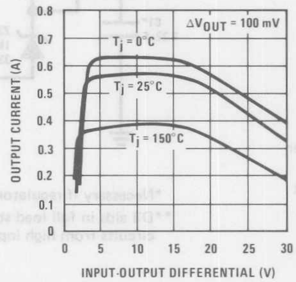
Note 3: The temperature coefficient of V_{OUT} is typically within 0.01% V_O/°C.

Typical Performance Characteristics

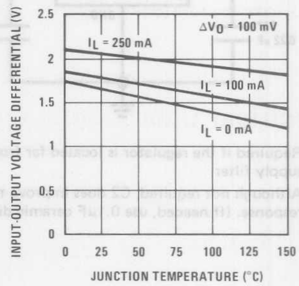
Maximum Average Power Dissipation (TO-202 Package)



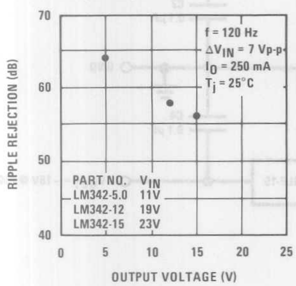
Peak Output Current



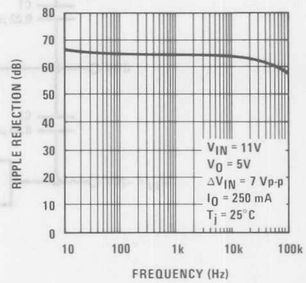
Dropout Voltage



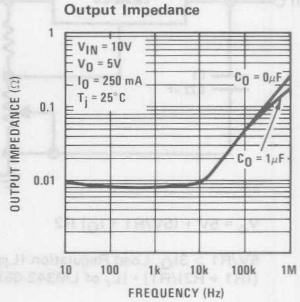
Ripple Rejection



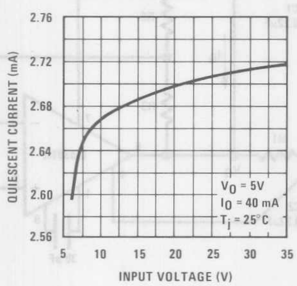
Ripple Rejection



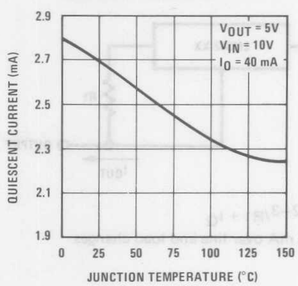
Output Impedance



Quiescent Current

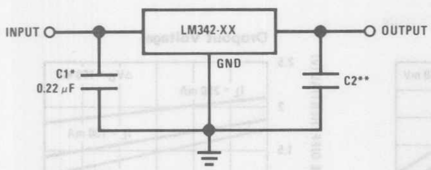


Quiescent Current



Typical Applications

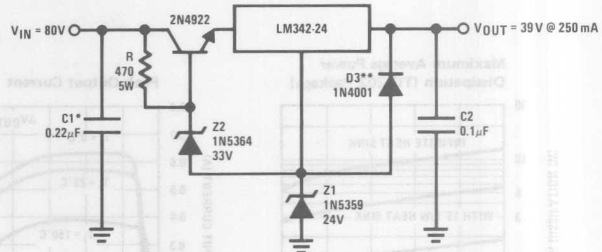
Fixed Output Regulator



*Required if the regulator is located far from power supply filter

**Although not required, C2 does improve transient response. (If needed, use 0.1µF ceramic disc.)

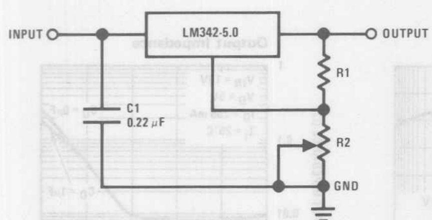
High Output Voltage Regulator



*Necessary if regulator is located far from the power supply filter

**D3 aids in full load start-up and protects the regulator during short circuits from high input to output voltage differentials

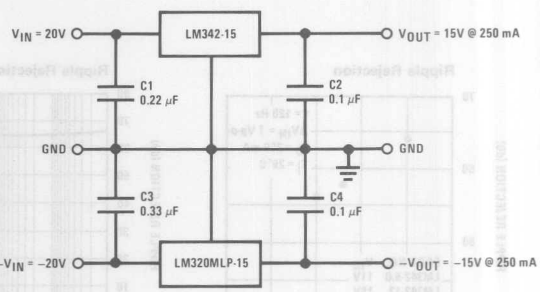
Adjustable Output Regulator



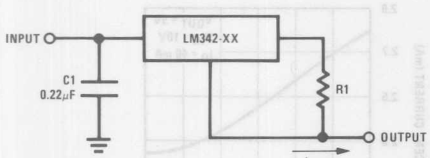
$V_o = 5V + (5V/R1 + I_Q)\ R2$

$5V/R1 > 3I_Q$, Load Regulation (L_R) = $[(R1 + R2)/R1] \cdot$ (L_r of LM342-05)

±15V, 250 mA Dual Power Supply



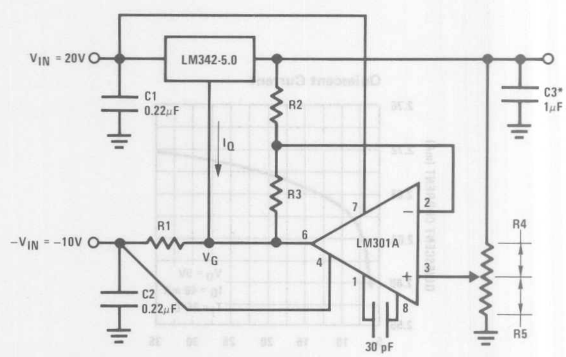
Current Regulator



$I_{OUT} = V^{2-3}/R1 + I_Q$

$\Delta I_Q \leq 1.5$ mA over line and load changes

Variable Output Regulator 0.5V – 18V



$V_{OUT} = V_G + 5V$, $R1 = (-V_{IN}/I_Q$ LM342)

$V_{OUT} = 5V(R2/R4)$ for $(R2 + R3) = (R4 + R5)$

A 0.5V output will correspond to $(R2/R4) = 0.1$, $(R3/R4) = 0.9$

*Solid tantalum

National Semiconductor

Voltage Regulators

LM723/LM723C Voltage Regulator

General Description

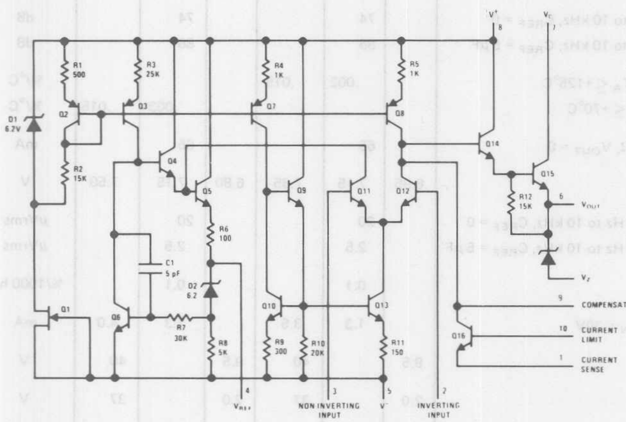
The LM723/LM723C is a voltage regulator designed primarily for series regulator applications. By itself, it will supply output currents up to 150 mA; but external transistors can be added to provide any desired load current. The circuit features extremely low standby current drain, and provision is made for either linear or foldback current limiting. Important characteristics are:

- 150 mA output current without external pass transistor
- Output currents in excess of 10A possible by adding external transistors
- Input voltage 40V max
- Output voltage adjustable from 2V to 37V
- Can be used as either a linear or a switching regulator.

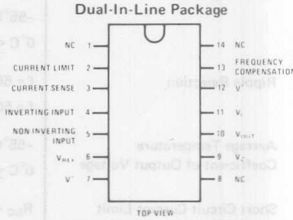
The LM723/LM723C is also useful in a wide range of other applications such as a shunt regulator, a current regulator or a temperature controller.

The LM723C is identical to the LM723 except that the LM723C has its performance guaranteed over a 0°C to 70°C temperature range, instead of −55°C to +125°C.

Schematic and Connection Diagrams*

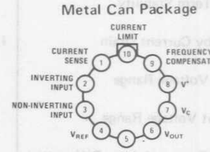


Dual-In-Line Package



Order Number LM723CN
See NS Package N14A
Order Number LM723J or LM723CJ
See NS Package J14A

Metal Can Package

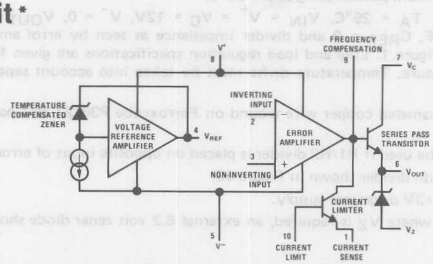


Note: Pin 5 connected to case.

TOP VIEW

Order Number LM723H or LM723CH
See NS Package H10C

Equivalent Circuit*



*Pin numbers refer to metal can package.

Absolute Maximum Ratings

Pulse Voltage from V^+ to V^- (50 ms)	50V
Continuous Voltage from V^+ to V^-	40V
Input-Output Voltage Differential	40V
Maximum Amplifier Input Voltage (Either Input)	7.5V
Maximum Amplifier Input Voltage (Differential)	5V
Current from V_Z	25 mA
Current from V_{REF}	15 mA
Internal Power Dissipation Metal Can (Note 1)	800 mW
Cavity DIP (Note 1)	900 mW
Molded DIP (Note 1)	660 mW
Operating Temperature Range LM723	$-55^\circ C$ to $+125^\circ C$
LM723C	$0^\circ C$ to $+70^\circ C$
Storage Temperature Range Metal Can	$-65^\circ C$ to $+150^\circ C$
DIP	$-55^\circ C$ to $+125^\circ C$
Lead Temperature (Soldering, 10 sec)	$300^\circ C$

Electrical Characteristics (Note 2)

PARAMETER	CONDITIONS	LM723			LM723C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Line Regulation	V_{IN} = 12V to V_{IN} = 15V		.01	0.1		.01	0.1	% V_{OUT}
	$-55^\circ C \le T_A \le +125^\circ C$			0.3				% V_{OUT}
	$0^\circ C \le T_A \le +70^\circ C$						0.3	% V_{OUT}
	V_{IN} = 12V to V_{IN} = 40V		.02	0.2		0.1	0.5	% V_{OUT}
Load Regulation	I_L = 1 mA to I_L = 50 mA		.03	0.15		.03	0.2	% V_{OUT}
	$-55^\circ C \le T_A \le +125^\circ C$			0.6				%V_{OUT}
	$0^\circ C \le T_A \le +70^\circ C$						0.6	%V_{OUT}
Ripple Rejection	f = 50 Hz to 10 kHz, C_{REF} = 0		74			74		dB
	f = 50 Hz to 10 kHz, C_{REF} = 5 μF		86			86		dB
Average Temperature Coefficient of Output Voltage	$-55^\circ C \le T_A \le +125^\circ C$		.002	.015				%/°C
	$0^\circ C \le T_A \le +70^\circ C$					.003	.015	%/°C
Short Circuit Current Limit	R_{SC} = 10Ω, V_{OUT} = 0		65			65		mA
Reference Voltage		6.95	7.15	7.35	6.80	7.15	7.50	V
Output Noise Voltage	BW = 100 Hz to 10 kHz, C_{REF} = 0		20			20		μVrms
	BW = 100 Hz to 10 kHz, C_{REF} = 5 μF		2.5			2.5		μVrms
Long Term Stability			0.1			0.1		%/1000 hrs
Standby Current Drain	I_L = 0, V_{IN} = 30V		1.3	3.5		1.3	4.0	mA
Input Voltage Range		9.5		40	9.5		40	V
Output Voltage Range		2.0		37	2.0		37	V
Input-Output Voltage Differential		3.0		38	3.0		38	V

Note 1: See derating curves for maximum power rating above 25°C.

Note 2: Unless otherwise specified, T_A = 25°C, $V_{IN} = V^+ = V_C$ = 12V, V^- = 0, V_{OUT} = 5V, I_L = 1 mA, R_{SC} = 0, C_1 = 100 pF, C_{REF} = 0 and divider impedance as seen by error amplifier $\le$ 10 kΩ connected as shown in Figure 1. Line and load regulation specifications are given for the condition of constant chip temperature. Temperature drifts must be taken into account separately for high dissipation conditions.

Note 3: L_1 is 40 turns of No. 20 enameled copper wire wound on Ferroxcube P36/22-3B7 pot core or equivalent with 0.009 in. air gap.

Note 4: Figures in parentheses may be used if R1/R2 divider is placed on opposite input of error amp.

Note 5: Replace R1/R2 in figures with divider shown in Figure 13.

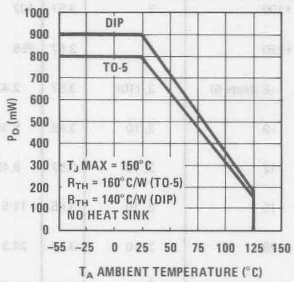
Note 6: V^+ must be connected to a +3V or greater supply.

Note 7: For metal can applications where V_Z is required, an external 6.2 volt zener diode should be connected in series with V_{OUT}.

Maximum Power Ratings

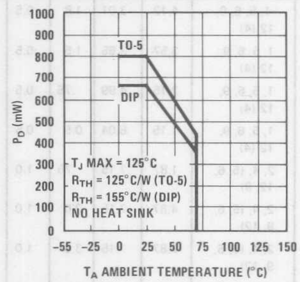
LM723

Power Dissipation vs Ambient Temperature



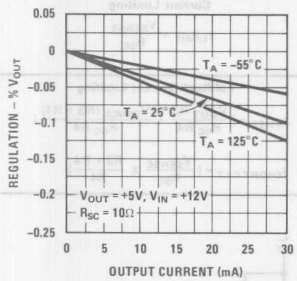
LM723C

Power Dissipation vs Ambient Temperature

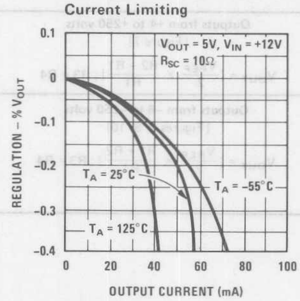


Typical Performance Characteristics

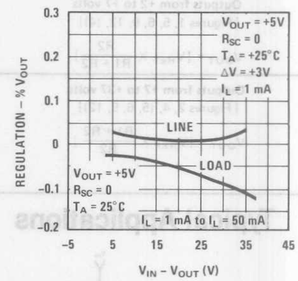
Load Regulation Characteristics with Current Limiting



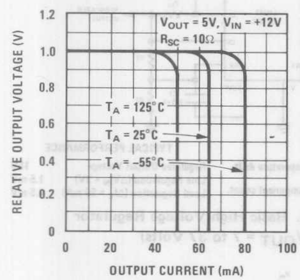
Load Regulation Characteristics with Current Limiting



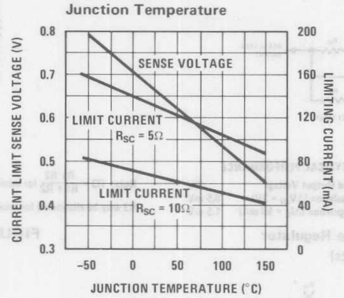
Load & Line Regulation vs Input-Output Voltage Differential



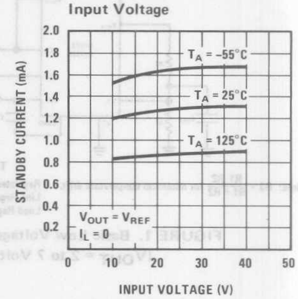
Current Limiting Characteristics



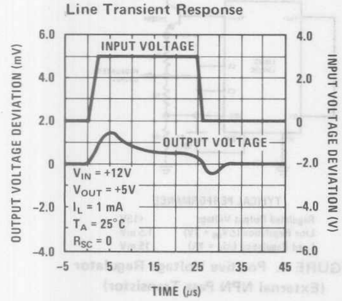
Current Limiting Characteristics vs Junction Temperature



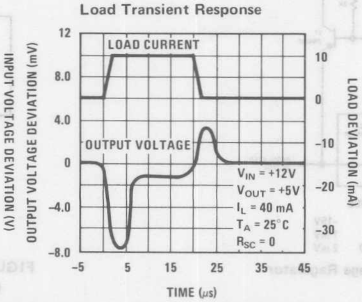
Standby Current Drain vs Input Voltage



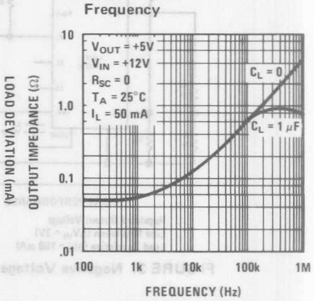
Line Transient Response



Load Transient Response



Output Impedance vs Frequency



		R1	R2	R1	P1	R2
+3.0	1, 5, 6, 9, 12 (4)	4.12	3.01	1.8	0.5	1.2
+3.6	1, 5, 6, 9, 12 (4)	3.57	3.65	1.5	0.5	1.5
+5.0	1, 5, 6, 9, 12 (4)	2.15	4.99	.75	0.5	2.2
+6.0	1, 5, 6, 9, 12 (4)	1.15	6.04	0.5	0.5	2.7
+9.0	2, 4, (5, 6, 12, 9)	1.87	7.15	.75	1.0	2.7
+12	2, 4, (5, 6, 9, 12)	4.87	7.15	2.0	1.0	3.0
+15	2, 4, (5, 6, 9, 12)	7.87	7.15	3.3	1.0	3.0
+28	2, 4, (5, 6, 9, 12)	21.0	7.15	5.6	1.0	2.0
+45	7	3.57	48.7	2.2	10	39
+75	7	3.57	78.7	2.2	10	68

		R1	R2	R1	P1	R2
+100	7	3.57	102	2.2	10	91
+250	7	3.57	255	2.2	10	240
−6 (Note 6)	3, (10)	3.57	2.43	1.2	0.5	.75
−9	3, 10	3.48	5.36	1.2	0.5	2.0
−12	3, 10	3.57	8.45	1.2	0.5	3.3
−15	3, 10	3.65	11.5	1.2	0.5	4.3
−28	3, 10	3.57	24.3	1.2	0.5	10
−45	8	3.57	41.2	2.2	10	33
−100	8	3.57	97.6	2.2	10	91
−250	8	3.57	249	2.2	10	240

TABLE II FORMULAE FOR INTERMEDIATE OUTPUT VOLTAGES

Outputs from +2 to +7 volts
[Figures 1, 5, 6, 9, 12, (4)]

$$V_{OUT} = \left[V_{REF} \times \frac{R2}{R1 + R2}\right]$$

Outputs from +4 to +250 volts
[Figure 7]

$$V_{OUT} = \left[\frac{V_{REF}}{2} \times \frac{R2 - R1}{R1}\right];\ R3 = R4$$

Current Limiting

$$I_{LIMIT} = \frac{V_{SENSE}}{R_{SC}}$$

Outputs from +7 to +37 volts
[Figures 2, 4, (5, 6, 9, 12)]

$$V_{OUT} = \left[V_{REF} \times \frac{R1 + R2}{R2}\right]$$

Outputs from −6 to −250 volts
[Figures 3, 8, 10]

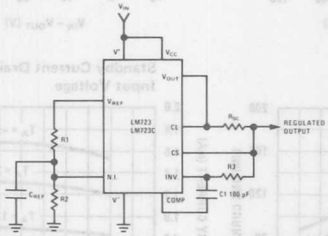
$$V_{OUT} = \left[\frac{V_{REF}}{2} \times \frac{R1 + R2}{R1}\right];\ R3 = R4$$

Foldback Current Limiting

$$I_{KNEE} = \left[\frac{V_{OUT}\,R3}{R_{SC}\,R4} + \frac{V_{SENSE}\,(R3 + R4)}{R_{SC}\,R4}\right]$$

$$I_{SHORT\,CKT} = \left[\frac{V_{SENSE}}{R_{SC}} \times \frac{R3 + R4}{R4}\right]$$

Typical Applications

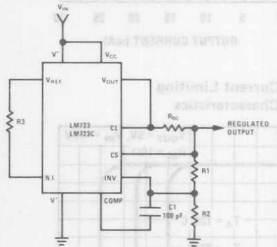


Note: $R3 = \frac{R1\,R2}{R1 + R2}$ for minimum temperature drift.

TYPICAL PERFORMANCE

Regulated Output Voltage	5V
Line Regulation (ΔV_{IN} = 3V)	0.5 mV
Load Regulation (ΔI_L = 50 mA)	1.5 mV

FIGURE 1. Basic Low Voltage Regulator (V_{OUT} = 2 to 7 Volts)



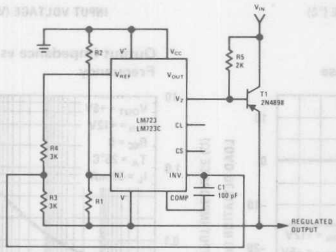
Note: $R3 = \frac{R1\,R2}{R1 + R2}$ for minimum temperature drift.

R3 may be eliminated for minimum component count.

TYPICAL PERFORMANCE

Regulated Output Voltage	15V
Line Regulation (ΔV_{IN} = 3V)	1.5 mV
Load Regulation (ΔI_L = 50 mA)	4.5 mV

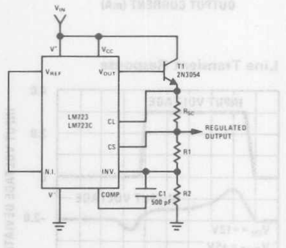
FIGURE 2. Basic High Voltage Regulator (V_{OUT} = 7 to 37 Volts)



TYPICAL PERFORMANCE

Regulated Output Voltage	−15V
Line Regulation (ΔV_{IN} = 3V)	1 mV
Load Regulation (ΔI_L = 100 mA)	2 mV

FIGURE 3. Negative Voltage Regulator

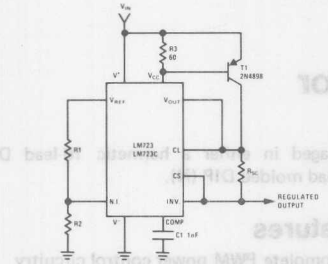


TYPICAL PERFORMANCE

Regulated Output Voltage	+15V
Line Regulation (ΔV_{IN} = 3V)	1.5 mV
Load Regulation (ΔI_L = 1A)	15 mV

FIGURE 4. Positive Voltage Regulator (External NPN Pass Transistor)

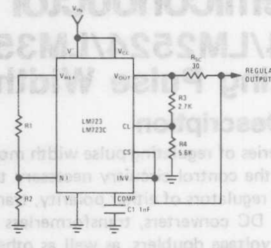
Typical Applications (Continued)



TYPICAL PERFORMANCE

Regulated Output Voltage	+5V
Line Regulation (ΔV_{IN} = 3V)	0.5 mV
Load Regulation (ΔI_L = 1A)	5 mV

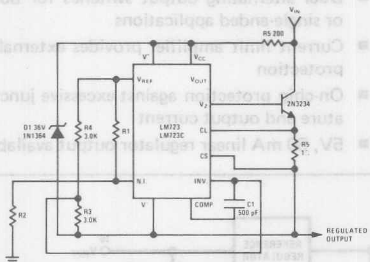
FIGURE 5. Positive Voltage Regulator (External PNP Pass Transistor)



TYPICAL PERFORMANCE

Regulated Output Voltage	+5V
Line Regulation (ΔV_{IN} = 3V)	0.5 mV
Load Regulation (ΔI_L = 10 mA)	1 mV
Short Circuit Current	20 mA

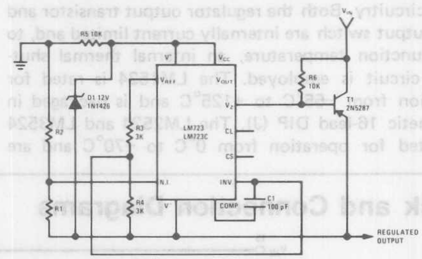
FIGURE 6. Foldback Current Limiting



TYPICAL PERFORMANCE

Regulated Output Voltage	+50V
Line Regulation (ΔV_{IN} = 20V)	15 mV
Load Regulation (ΔI_L = 50 mA)	20 mV

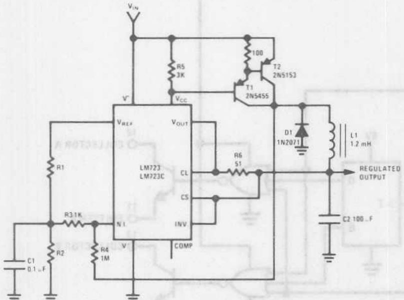
FIGURE 7. Positive Floating Regulator



TYPICAL PERFORMANCE

Regulated Output Voltage	−100V
Line Regulation (ΔV_{IN} = 20V)	30 mV
Load Regulation (ΔI_L = 100 mA)	20 mV

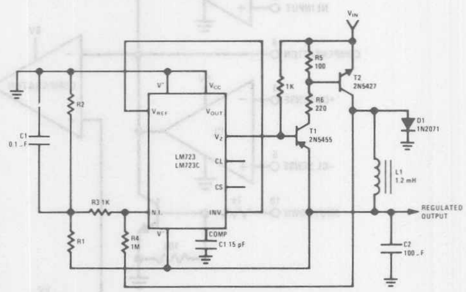
FIGURE 8. Negative Floating Regulator



TYPICAL PERFORMANCE

Regulated Output Voltage	+5V
Line Regulation (ΔV_{IN} = 30V)	10 mV
Load Regulation (ΔI_L = 2A)	80 mV

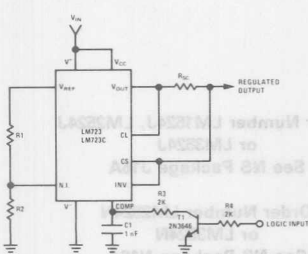
FIGURE 9. Positive Switching Regulator



TYPICAL PERFORMANCE

Regulated Output Voltage	−15V
Line Regulation (ΔV_{IN} = 20V)	8 mV
Load Regulation (ΔI_L = 2A)	6 mV

FIGURE 10. Negative Switching Regulator

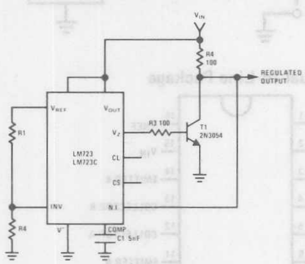


Note: Current limit transistor may be used for shutdown if current limiting is not required.

TYPICAL PERFORMANCE

Regulated Output Voltage	+5V
Line Regulation (ΔV_{IN} = 3V)	0.5 mV
Load Regulation (ΔI_L = 50 mA)	1.5 mV

FIGURE 11. Remote Shutdown Regulator with Current Limiting



TYPICAL PERFORMANCE

Regulated Output Voltage	+5V
Line Regulation (ΔV_{IN} = 10V)	0.5 mV
Load Regulation (ΔI_L = 100 mA)	1.5 mV

FIGURE 12. Shunt Regulator

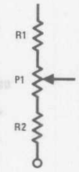


FIGURE 13. Output Voltage Adjust (See Note 5)

National Semiconductor

LM1524/LM2524/LM3524 Regulating Pulse Width Modulator

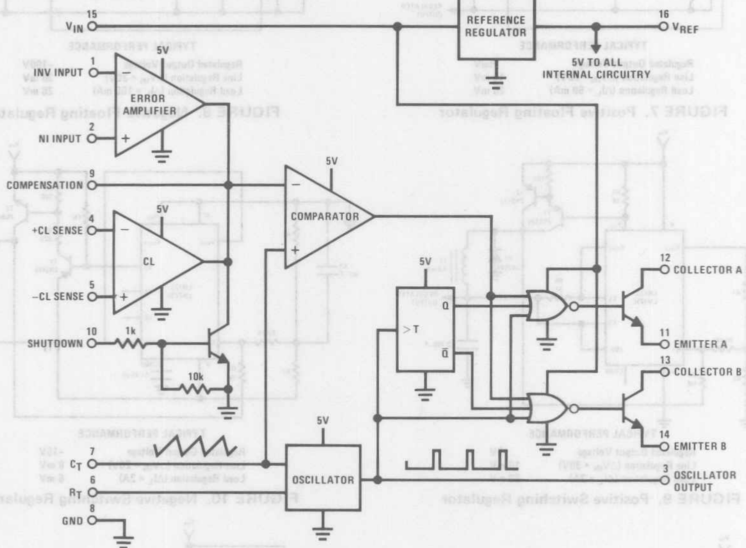
General Description

The LM1524 series of regulating pulse width modulators contains all of the control circuitry necessary to implement switching regulators of either polarity, transformer coupled DC to DC converters, transformerless polarity converters and voltage doublers, as well as other power control applications. This device includes a 5V voltage regulator capable of supplying up to 50 mA to external circuitry, a control amplifier, an oscillator, a pulse width modulator, a phase splitting flip-flop, dual alternating output switch transistors, and current limiting and shutdown circuitry. Both the regulator output transistor and each output switch are internally current limited and, to limit junction temperature, an internal thermal shutdown circuit is employed. The LM1524 is rated for operation from −55°C to +125°C and is packaged in a hermetic 16-lead DIP (J). The LM2524 and LM3524 are rated for operation from 0°C to +70°C and are packaged in either a hermetic 16-lead DIP (J) or a 16-lead molded DIP (N).

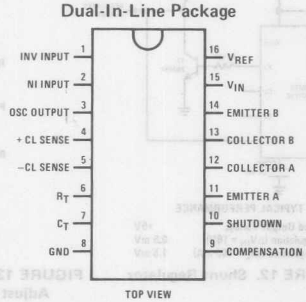
Features

- Complete PWM power control circuitry
- Frequency adjustable to greater than 100 kHz
- 2% frequency stability with temperature
- Total quiescent current less than 10 mA
- Dual alternating output switches for both push-pull or single-ended applications
- Current limit amplifier provides external component protection
- On-chip protection against excessive junction temperature and output current
- 5V, 50 mA linear regulator output available to user

Block and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number LM1524J, LM2524J or LM3524J
See NS Package J16A

Order Number LM2524N or LM3524N
See NS Package N16A

Absolute Maximum Ratings

Input Voltage	40V
Reference Voltage, Forced	6V
Reference Output Current	50 mA
Output Current (Each Output)	100 mA
Oscillator Charging Current (Pin 6 or 7)	5 mA
Internal Power Dissipation (Note 1)	1W
Operating Temperature Range	
LM1524	−55°C to +125°C
LM2524/LM3524	0°C to +70°C
Maximum Junction Temperature	
(J Package)	150°C
(N Package)	125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

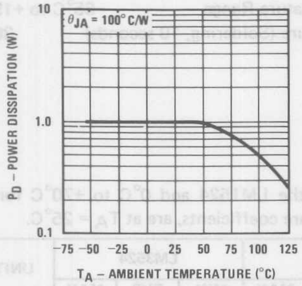
Unless otherwise stated, these specifications apply for T_A = −55°C to +125°C for the LM1524 and 0°C to +70°C for the LM2524 and LM3524, V_{IN} = 20V, and f = 20 kHz. Typical values other than temperature coefficients, are at T_A = 25°C.

PARAMETER	CONDITIONS	LM1524/LM2524 MIN	LM1524/LM2524 TYP	LM1524/LM2524 MAX	LM3524 MIN	LM3524 TYP	LM3524 MAX	UNITS
Reference Section								
Output Voltage		4.8	5.0	5.2	4.6	5.0	5.4	V
Line Regulation	V_{IN} = 8–40V		10	20		10	30	mV
Load Regulation	I_L = 0–20 mA		20	50		20	50	mV
Ripple Rejection	f = 120 Hz, T_A = 25°C		66			66		dB
Short-Circuit Output Current	V_{REF} = 0, T_A = 25°C		100			100		mA
Temperature Stability	Over Operating Temperature Range		0.3	1		0.3	1	%
Long Term Stability	T_A = 25°C		20			20		mV/khr
Oscillator Section								
Maximum Frequency	C_T = 0.001 μF, R_T = 2 kΩ		350			350		kHz
Initial Accuracy	R_T and C_T constant		5			5		%
Frequency Change with Voltage	V_{IN} = 8–40V, T_A = 25°C			1			1	%
Frequency Change with Temperature	Over Operating Temperature Range			2			2	%
Output Amplitude (Pin 3)	T_A = 25°C		3.5			3.5		V
Output Pulse Width (Pin 3)	C_T = 0.01 μF, T_A = 25°C		0.5			0.5		μs
Error Amplifier Section								
Input Offset Voltage	V_{CM} = 2.5V		0.5	5		2	10	mV
Input Bias Current	V_{CM} = 2.5V		2	10		2	10	μA
Open Loop Voltage Gain		72	80		60	80		dB
Common-Mode Input Voltage Range	T_A = 25°C	1.8		3.4	1.8		3.4	V
Common-Mode Rejection Ratio	T_A = 25°C		70			70		dB
Small Signal Bandwidth	A_V = 0 dB, T_A = 25°C		3			3		MHz
Output Voltage Swing	T_A = 25°C	0.5		3.8	0.5		3.8	V
Comparator Section								
Maximum Duty Cycle	% Each Output ON	45			45			%
Input Threshold (Pin 9)	Zero Duty Cycle		1			1		V
Input Threshold (Pin 9)	Maximum Duty Cycle		3.5			3.5		V
Input Bias Current			−1			−1		μA
Current Limiting Section								
Sense Voltage	$V_{(Pin\ 2)} - V_{(Pin\ 1)} \geq 50$ mV, Pin 9 = 2V, T_A = 25°C	190	200	210	180	200	220	mV
Sense Voltage T.C.			0.2			0.2		mV/°C
Common-Mode Voltage		−0.7		1	−0.7		1	V
Output Section (Each Output)								
Collector-Emitter Voltage		40			40			V
Collector Leakage Current	V_{CE} = 40V		0.1	50		0.1	50	μA
Saturation Voltage	I_C = 50 mA		1	2		1	2	V
Emitter Output Voltage	V_{IN} = 20V, I_E = −250 μA	17	18		17	18		V
Rise Time (10% to 90%)	R_C = 2 kΩ, T_A = 25°C		0.2			0.2		μs
Fall Time (90% to 10%)	R_C = 2 kΩ, T_A = 25°C		0.1			0.1		μs
Total Standby Current	V_{IN} = 40V, Pins 1, 4, 7, 8, 11, and 14 are grounded, Pin 2 = 2V, All Other Inputs and Outputs Open		5	10		5	10	mA

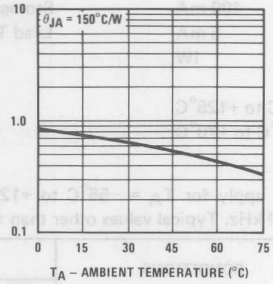
Note 1: For operation at elevated temperatures, devices in the J package must be derated based on a thermal resistance of 100°C/W, junction to ambient, and devices in the N package must be derated based on a thermal resistance of 150°C/W, junction to ambient.

Typical Performance Characteristics

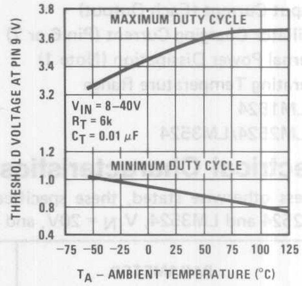
Maximum Average Power Dissipation (J Package)



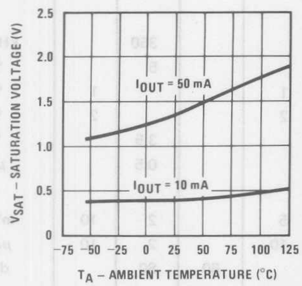
Maximum Average Power Dissipation (N Package)



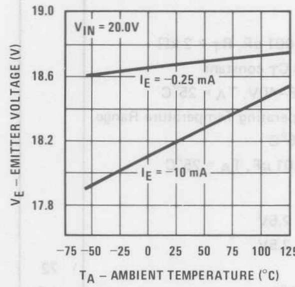
Maximum and Minimum Duty Cycle Threshold Voltage



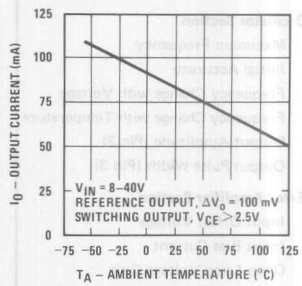
Output Transistor Saturation Voltage



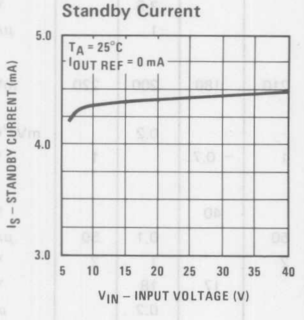
Output Transistor Emitter Voltage



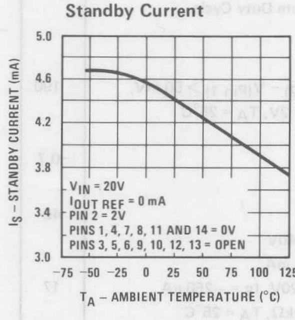
Reference and Switching Transistor Peak Output Current



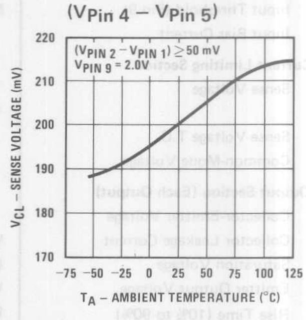
Standby Current



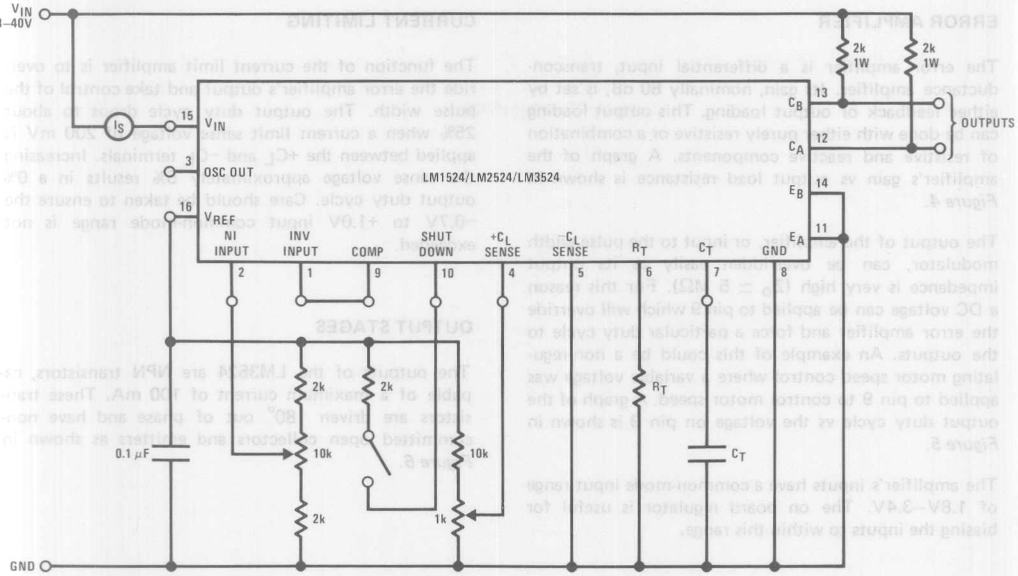
Standby Current



Current Limit Sense Voltage ($V_{Pin\ 4} - V_{Pin\ 5}$)



Test Circuit

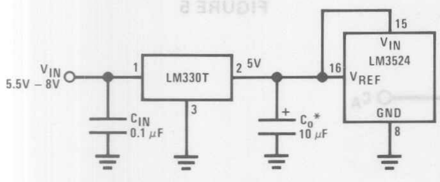


Functional Description

INTERNAL VOLTAGE REGULATOR

The LM3524 has on chip a 5V, 50 mA, short circuit protected voltage regulator. This voltage regulator provides a supply for all internal circuitry of the device and can be used as an external reference.

For input voltages of less than 8V the 5V output should be shorted to pin 15, V_{IN}, which disables the 5V regulator. With these pins shorted the input voltage must be limited to a maximum of 6V. If input voltages of 6–8V are to be used, a pre-regulator, as shown in *Figure 1*, must be added.



*Minimum C_o of 10 μF required for stability.

FIGURE 1

OSCILLATOR

The LM3524 provides a stable on-board oscillator. Its frequency is set by an external resistor, R_T and capacitor, C_T. A graph of R_T, C_T vs oscillator frequency is shown in *Figure 2*. The oscillator's output provides the signals for triggering an internal flip-flop, which directs the PWM information to the outputs, and a blanking pulse to turn off both outputs during transitions to ensure that cross conduction does not occur. The width of the blanking pulse, or dead time, is controlled by the value of C_T, as shown in *Figure 3*. The recommended values of R_T are 1.8 kΩ to 100 kΩ, and for C_T, 0.001 μF to 0.1 μF.

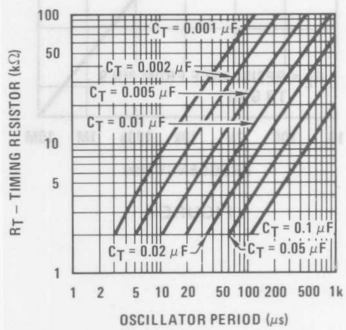


FIGURE 2

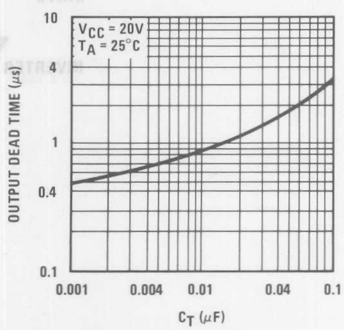


FIGURE 3

The error amplifier is a differential input, transconductance amplifier. Its gain, nominally 80 dB, is set by either feedback or output loading. This output loading can be done with either purely resistive or a combination of resistive and reactive components. A graph of the amplifier's gain vs output load resistance is shown in *Figure 4*.

The output of the amplifier, or input to the pulse width modulator, can be overridden easily as its output impedance is very high ($Z_O \simeq 5\ M\Omega$). For this reason a DC voltage can be applied to pin 9 which will override the error amplifier and force a particular duty cycle to the outputs. An example of this could be a non-regulating motor speed control where a variable voltage was applied to pin 9 to control motor speed. A graph of the output duty cycle vs the voltage on pin 9 is shown in *Figure 5*.

The amplifier's inputs have a common-mode input range of 1.8V–3.4V. The on board regulator is useful for biasing the inputs to within this range.

The function of the current limit amplifier is to override the error amplifier's output and take control of the pulse width. The output duty cycle drops to about 25% when a current limit sense voltage of 200 mV is applied between the $+C_L$ and $-C_L$ terminals. Increasing the sense voltage approximately 5% results in a 0% output duty cycle. Care should be taken to ensure the −0.7V to +1.0V input common-mode range is not exceeded.

OUTPUT STAGES

The outputs of the LM3524 are NPN transistors, capable of a maximum current of 100 mA. These transistors are driven 180° out of phase and have non-committed open collectors and emitters as shown in *Figure 6*.

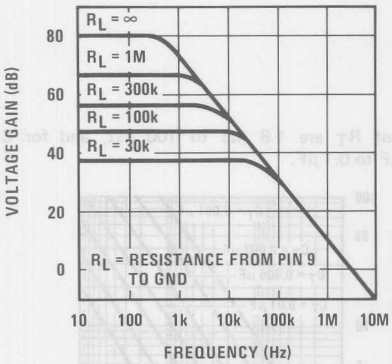


FIGURE 4

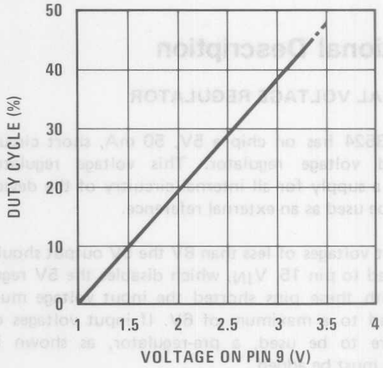


FIGURE 5

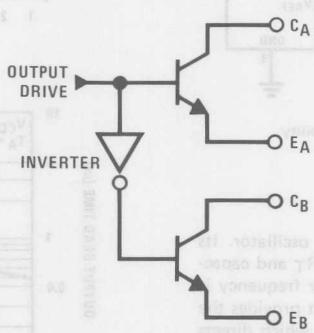
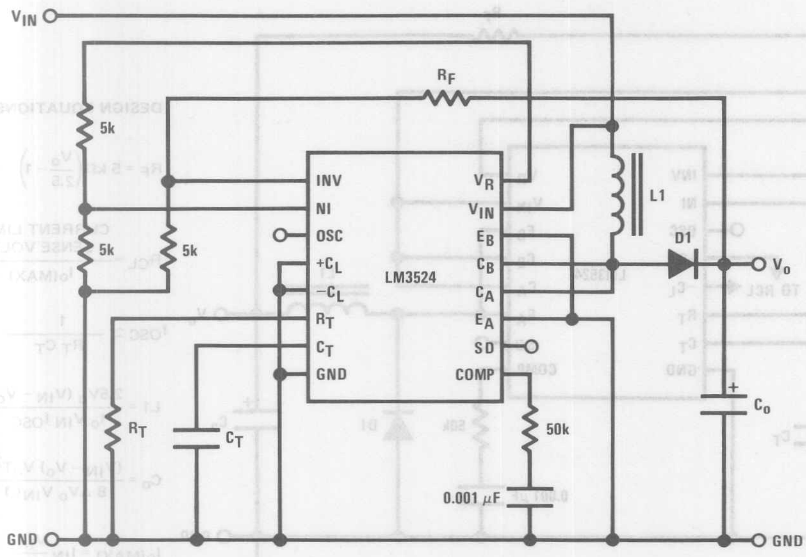


FIGURE 6

Typical Applications



DESIGN EQUATIONS

$$R_F = 5k\left(\frac{V_o}{2.5} - 1\right)$$

$$f_{OSC} \simeq \frac{1}{R_T C_T}$$

$$L1 = \frac{2.5V_{IN}^2\,(V_o - V_{IN})}{f_{OSC} I_o V_o^2}$$

$$C_o = \frac{I_o\,(V_o - V_{IN})}{f_{OSC}\,\Delta V_o\,V_o}$$

$$I_{o(MAX)} = I_{IN}\,\frac{V_{IN}}{V_o}$$

FIGURE 7. Positive Regulator, Step-Up Basic Configuration ($I_{IN(MAX)}$ = 80 mA)

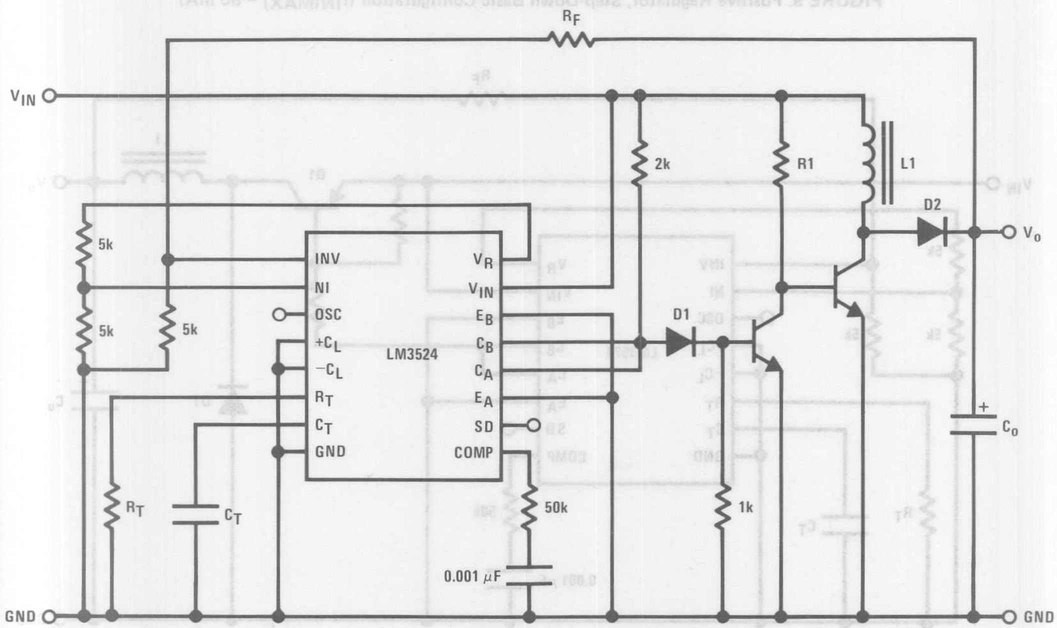
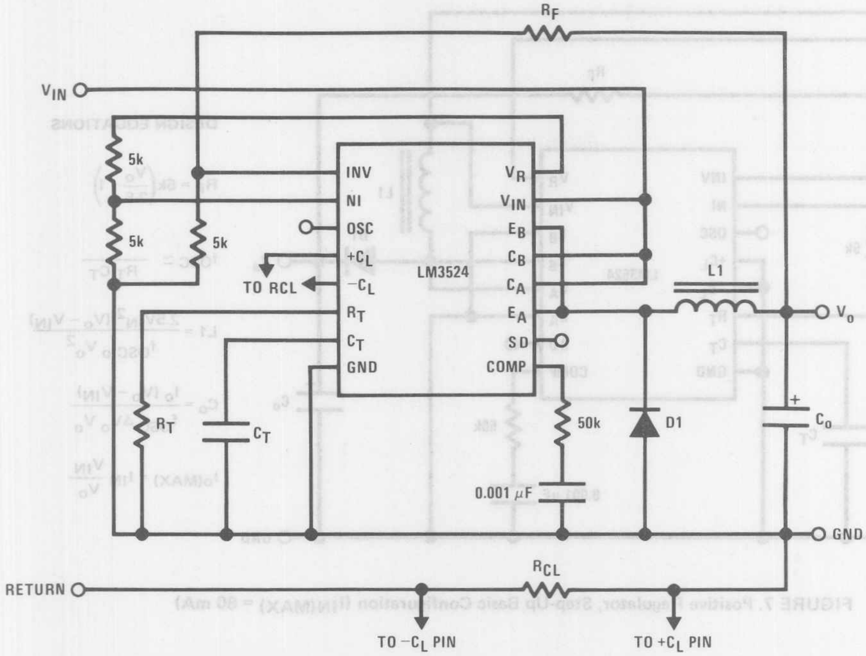


FIGURE 8. Positive Regulator, Step-Up Boosted Current Configuration

Typical Applications (Continued)



DESIGN EQUATIONS

$$R_F = 5\ k\Omega\left(\frac{V_o}{2.5} - 1\right)$$

$$R_{CL} = \frac{\text{CURRENT LIMIT SENSE VOLT}}{I_{o(MAX)}}$$

$$f_{OSC} \simeq \frac{1}{R_T\, C_T}$$

$$L1 = \frac{2.5V_o\,(V_{IN} - V_o)}{I_o\, V_{IN}\, f_{OSC}}$$

$$C_o = \frac{(V_{IN} - V_o)\, V_o T^2}{8\, \Delta V_o\, V_{IN} L1}$$

$$I_{o(MAX)} = I_{IN}\frac{V_{IN}}{V_o}$$

FIGURE 9. Positive Regulator, Step-Down Basic Configuration ($I_{IN(MAX)}$ = 80 mA)

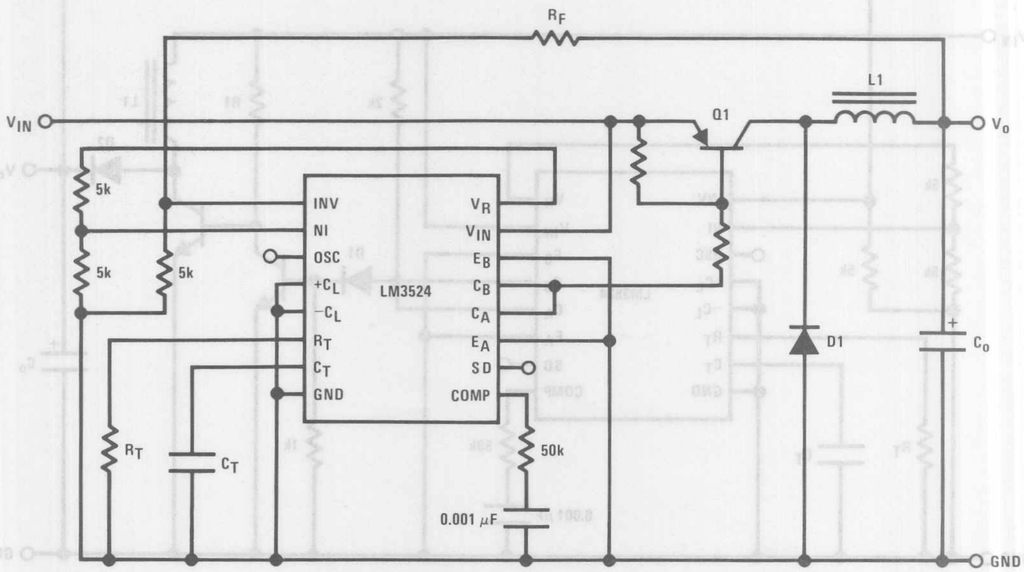
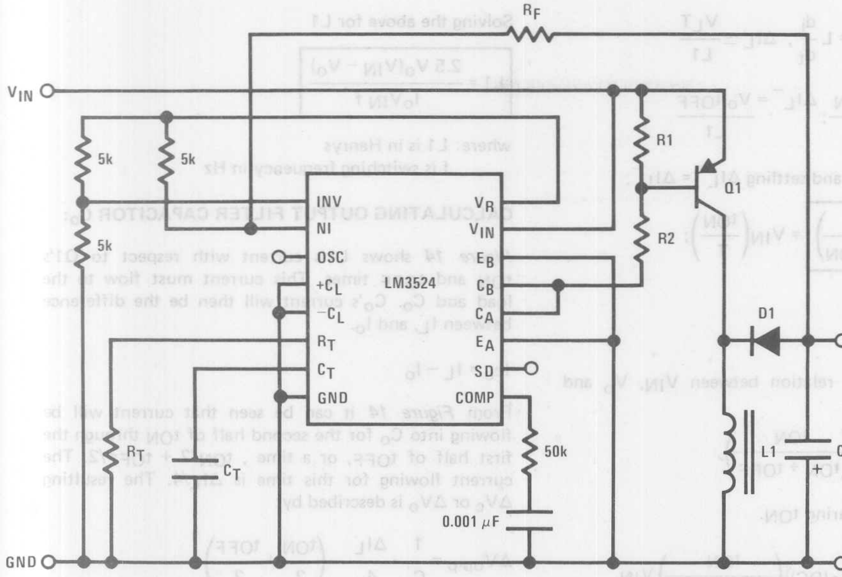


FIGURE 10. Positive Regulator, Step-Down Boosted Current Configuration

Typical Applications (Continued)



DESIGN EQUATIONS

$$R_F = 5k\left(1 - \frac{V_o}{2.5}\right)$$

$$f_{OSC} \simeq \frac{1}{R_T C_T}$$

$$L1 = \frac{2.5 V_{IN} V_o}{f_{OSC} (V_o + V_{IN}) I_o}$$

$$C_o = \frac{I_o V_o}{\Delta V_o f_{OSC} (V_o + V_{IN})}$$

FIGURE 11. Boosted Current Polarity Inverter

BASIC SWITCHING REGULATOR THEORY AND APPLICATIONS

The basic circuit of a step-down switching regulator circuit is shown in *Figure 12*, along with a practical circuit design using the LM3524 in *Figure 15*.

The circuit works as follows: Q1 is used as a switch, which has ON and OFF times controlled by the pulse width modulator. When Q1 is ON, power is drawn from V_{IN} and supplied to the load through L1; V_A is at approximately V_{IN}, D1 is reverse biased, and C_o is charging. When Q1 turns OFF the inductor L1 will force V_A negative to keep the current flowing in it, D1 will start conducting and the load current will flow through D1 and L1. The voltage at V_A is smoothed by the L1, C_o filter giving a clean DC output. The current flowing through L1 is equal to the nominal DC load current plus some ΔI_L which is due to the changing voltage across it. *A good rule of thumb is to set* $\Delta I_{Lp\text{-}p} \simeq 40\% \cdot I_o$.

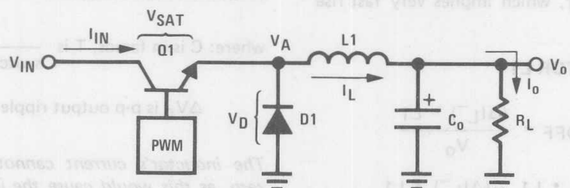


FIGURE 12. Basic Step-Down Switching Regulator

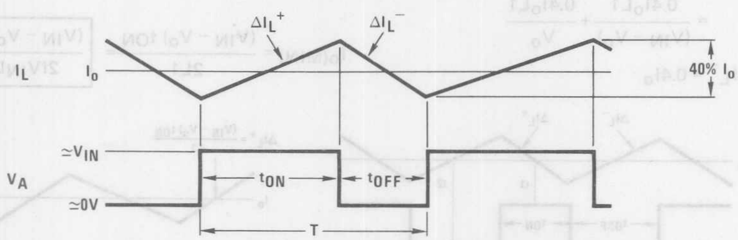


FIGURE 13

$$\Delta I_L^+ = \frac{(V_{IN} - V_o)\ t_{ON}}{L1}; \quad \Delta I_L^- = \frac{V_o\ t_{OFF}}{L1}$$

Neglecting V_{SAT}, V_D, and settling $\Delta I_L^+ = \Delta I_L^-$;

$$\boxed{V_o \simeq V_{IN}\left(\frac{t_{ON}}{t_{OFF} + t_{ON}}\right)} = V_{IN}\left(\frac{t_{ON}}{T}\right);$$

where T = Total Period

The above shows the relation between V_{IN}, V_o and duty cycle.

$$I_{IN(DC)} = I_{OUT(DC)}\left(\frac{t_{ON}}{t_{ON} + t_{OFF}}\right),$$

as Q1 only conducts during t_{ON}.

$$P_{IN} = I_{IN(DC)}V_{IN} = (I_{o(DC)})\left(\frac{t_{ON}}{t_{ON} + t_{OFF}}\right)V_{IN}$$

$$P_o = I_oV_o$$

The efficiency, η, of the circuit is:

$$\eta MAX = \frac{P_o}{P_{IN}} = \frac{I_oV_o}{I_o\frac{(t_{ON})}{T}V_{IN} + (V_{SAT}\ \frac{t_{ON}}{T} + V_{D1}\frac{t_{OFF}}{T})\ I_o}$$

$$= \boxed{\frac{V_o}{V_o + 1}} \text{ for } V_{SAT} = V_{D1} = 1V.$$

ηMAX will be further decreased due to switching losses in Q1. For this reason Q1 should be selected to have the maximum possible f_T, which implies very fast rise and fall times.

CALCULATING INDUCTOR L1

$$t_{ON} \simeq \frac{(\Delta I_L^+) \bullet L1}{(V_{IN} - V_o)}, \quad t_{OFF} = \frac{(\Delta I_L^-) \bullet L1}{V_o}$$

$$t_{ON} + t_{OFF} = T = \frac{(\Delta I_L^+) \bullet L1}{(V_{IN} - V_o)} + \frac{(\Delta I_L^-) \bullet L1}{V_o}$$

$$= \frac{0.4I_oL1}{(V_{IN} - V_o)} + \frac{0.4I_oL1}{V_o}$$

Since $\Delta I_L^+ = \Delta I_L^- = 0.4I_o$

$$\boxed{L1 = \frac{\ldots}{I_oV_{IN}\ f}}$$

where: L1 is in Henrys
f is switching frequency in Hz

CALCULATING OUTPUT FILTER CAPACITOR C_o:

Figure 14 shows L1's current with respect to Q1's t_{ON} and t_{OFF} times. This current must flow to the load and C_o. C_o's current will then be the difference between I_L, and I_o.

$$I_{C_o} = I_L - I_o$$

From *Figure 14* it can be seen that current will be flowing into C_o for the second half of t_{ON} through the first half of t_{OFF}, or a time, $t_{ON}/2 + t_{OFF}/2$. The current flowing for this time is $\Delta I_L/4$. The resulting ΔV_c or ΔV_o is described by:

$$\Delta V_{op\text{-}p} = \frac{1}{C} \bullet \frac{\Delta I_L}{4} \bullet \left(\frac{t_{ON}}{2} + \frac{t_{OFF}}{2}\right)$$

$$= \frac{\Delta I_L}{4C}\left(\frac{t_{ON} + t_{OFF}}{2}\right)$$

$$\text{Since } \Delta I_L = \frac{V_o(T - t_{ON})}{L1} \quad \text{and} \quad t_{ON} = \frac{V_oT}{V_{IN}}$$

$$\Delta V_{op\text{-}p} = \frac{V_o\left(T - \frac{V_oT}{V_{IN}}\right)}{4C\ L1}\left(\frac{T}{2}\right) = \frac{(V_{IN} - V_o)\ V_oT^2}{8V_{IN}C_oL1} \quad \text{or}$$

$$\boxed{C_o = \frac{(V_{IN} - V_o)V_o\ T^2}{8\Delta V_oV_{IN}L1}}$$

where: C is in farads, T is $\frac{1}{\text{switching frequency}}$,

ΔV_o is p-p output ripple

The inductor's current cannot be allowed to fall to zero, as this would cause the inductor to saturate. For this reason some minimum I_o is required as shown below:

$$I_{o(MIN)} = \frac{(V_{IN} - V_o)\ t_{ON}}{2L1} = \boxed{\frac{(V_{IN} - V_o)\ V_o}{2fV_{IN}L1}}$$

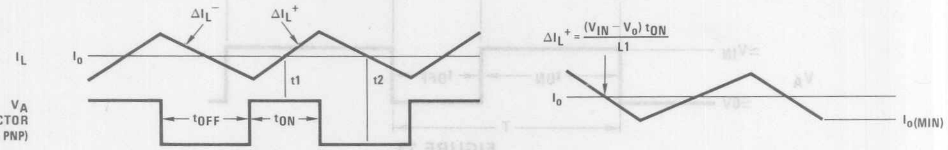


FIGURE 14

Typical Applications (Continued)

A complete step-down switching regulator schematic, using the LM3524, is illustrated in *Figure 15*. Transistors Q1 and Q2 have been added to boost the output to 1A. The 5V regulator of the LM3524 has been divided in half to bias the error amplifier's non-inverting input to within its common-mode range. Since each output transistor is on for half the period, actually 45%, they have been paralleled to allow longer possible duty cycles, up to 90%. This makes a lower possible input voltage. The output voltage is set by:

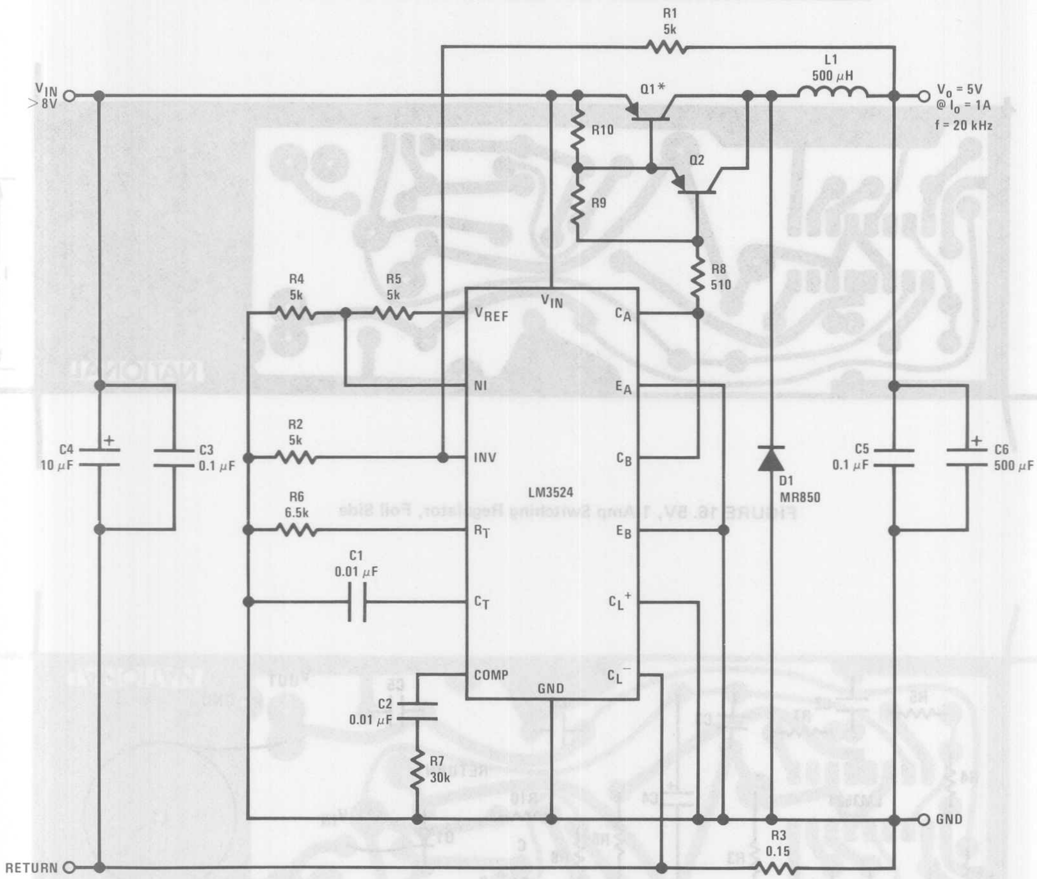
$$V_O = V_{NI}\left(1 + \frac{R1}{R2}\right),$$

where V_{NI} is the voltage at the error amplifier's non-inverting input.

Resistor R3 sets the current limit to:

$$\frac{200\text{ mV}}{R3} = \frac{200\text{ mV}}{0.15} = 1.3\text{A}.$$

Figure 16 and *17* show a PC board layout and stuffing diagram for the 5V, 1A regulator of *Figure 15*. The regulator's performance is listed in Table I.



*Mounted to Staver Heatsink No. V5-1.
Q1 = BD344
Q2 = 2N5023
L1 = > 40 turns No. 22 wire on Ferroxcube No. K300502 Torroid core.

FIGURE 15. 5V, 1 Amp Step-Down Switching Regulator

Typical Applications (Continued)

TABLE I

PARAMETER	CONDITIONS	TYPICAL CHARACTERISTICS
Output Voltage	$V_{IN} = 10V, I_o = 1A$	5V
Switching Frequency	$V_{IN} = 10V, I_o = 1A$	20 kHz
Short Circuit Current Limit	$V_{IN} = 10V$	1.3A
Load Regulation	$V_{IN} = 10V, I_o = 0.2 - 1A$	3 mV
Line Regulation	$\Delta V_{IN} = 10 - 20V, I_o = 1A$	6 mV
Efficiency	$V_{IN} = 10V, I_o = 1A$	80%
Output Ripple	$V_{IN} = 10V, I_o = 1A$	10 mVp-p

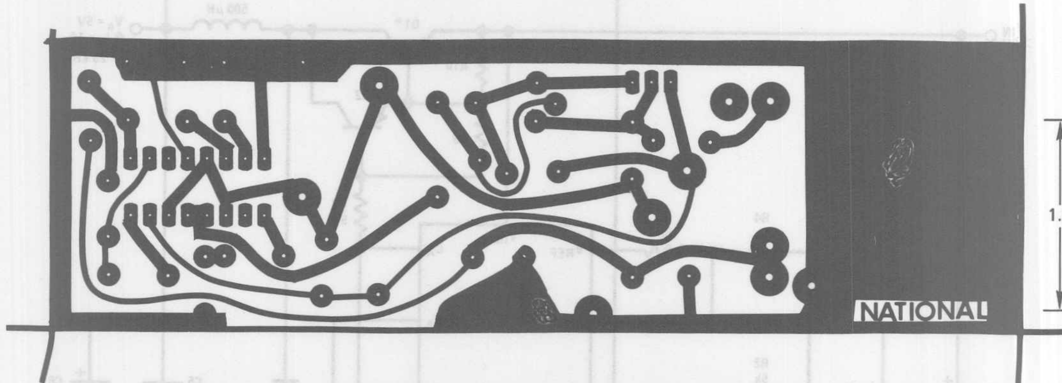


FIGURE 16. 5V, 1 Amp Switching Regulator, Foil Side

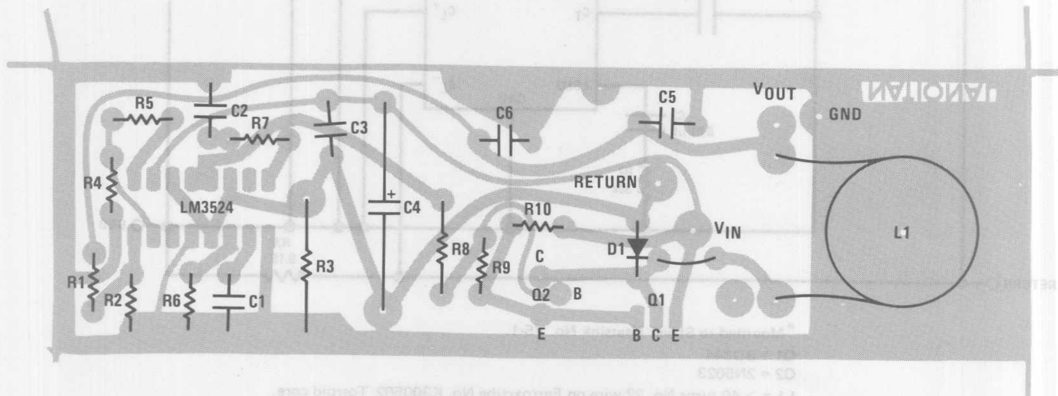


FIGURE 17. Stuffing Diagram, Component Side.

Typical Applications (Continued)

THE STEP-UP SWITCHING REGULATOR

Figure 18 shows the basic circuit for a step-up switching regulator. In this circuit Q1 is used as a switch to alternately apply V_{IN} across inductor L1. During the time, t_{ON}, Q1 is ON and energy is drawn from V_{IN} and stored in L1; D1 is reverse biased and I_o is supplied from the charge stored in C_o. When Q1 opens, t_{OFF}, voltage V1 will rise positively to the point where D1 turns ON. The output current is now supplied through L1,D1 to the load and any charge lost from C_o during t_{ON} is replenished. Here also, as in the step-down regulator, the current through L1 has a DC component plus some ΔI_L. ΔI_L is again selected to be approximately 40% of I_L. *Figure 19* shows the inductor's current in relation to Q1's ON and OFF times.

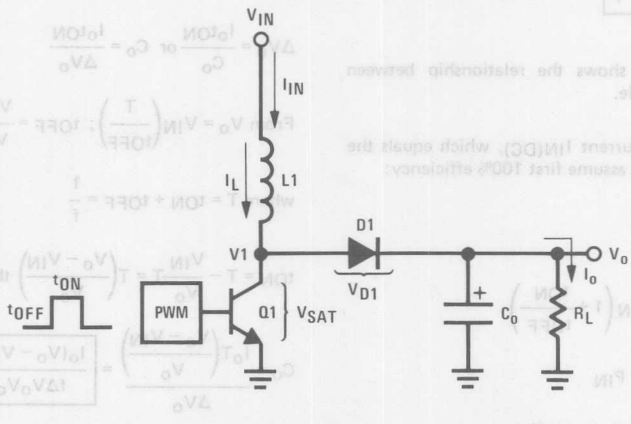


FIGURE 18. Basic Step-Up Switching Regulator

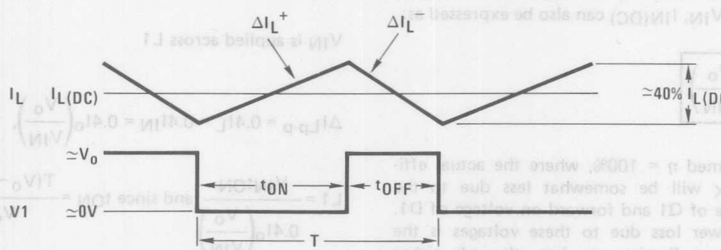


FIGURE 19

and $\Delta I_L^- \simeq \frac{(V_o - V_{IN})t_{OFF}}{L1}$

Since $\Delta I_L^+ = \Delta I_L^-$, $V_{IN}t_{ON} = V_o t_{OFF} - V_{IN}t_{OFF}$,

and neglecting V_{SAT} and V_{D1}

$$\boxed{V_o \simeq V_{IN}\left(1 + \frac{t_{ON}}{t_{OFF}}\right)}$$

The above equation shows the relationship between V_{IN}, V_o and duty cycle.

In calculating input current $I_{IN(DC)}$, which equals the inductor's DC current, assume first 100% efficiency:

$$P_{IN} = I_{IN(DC)}V_{IN}$$

$$P_{OUT} = I_oV_o = I_o\ V_{IN}\left(1 + \frac{t_{ON}}{t_{OFF}}\right)$$

for η = 100%, $P_{OUT} = P_{IN}$

$$I_o\ V_{IN}\left(1 + \frac{t_{ON}}{t_{OFF}}\right) = I_{IN(DC)}\ V_{IN}$$

$$I_{IN(DC)} = I_o\left(1 + \frac{t_{ON}}{t_{OFF}}\right)$$

This equation shows that the input, or inductor, current is larger than the output current by the factor $(1 + t_{ON}/t_{OFF})$. Since this factor is the same as the relation between V_o and V_{IN}, $I_{IN(DC)}$ can also be expressed as:

$$\boxed{I_{IN(DC)} = I_o\left(\frac{V_o}{V_{IN}}\right)}$$

So far it is assumed η = 100%, where the actual efficiency or η_{MAX} will be somewhat less due to the saturation voltage of Q1 and forward on voltage of D1. The internal power loss due to these voltages is the average I_L current flowing, or I_{IN}, through either V_{SAT} or V_{D1}. For $V_{SAT} = V_{D1}$ = 1V this power loss becomes $I_{IN(DC)}$ (1V). η_{MAX} is then:

$$\eta_{MAX} = \frac{P_o}{P_{IN}} = \frac{V_oI_o}{V_oI_o + I_{IN}\,(1V)} = \frac{V_oI_o}{V_oI_o + I_o\left(1 + \frac{t_{ON}}{t_{OFF}}\right)}$$

$\left. t_{OFF} \right)$

$$\boxed{\eta_{max} = \frac{V_{IN}}{V_{IN} + 1}}$$

This equation assumes only DC losses, however η_{MAX} is further decreased because of the switching time of Q1 and D1.

In calculating the output capacitor C_o it can be seen that C_o supplies I_o during t_{ON}. The voltage change on C_o during this time will be some $\Delta V_c = \Delta V_o$ or the output ripple of the regulator. Calculation of C_o is:

$$\Delta V_o = \frac{I_ot_{ON}}{C_o} \text{ or } C_o = \frac{I_ot_{ON}}{\Delta V_o}$$

From $V_o = V_{IN}\left(\frac{T}{t_{OFF}}\right)$; $t_{OFF} = \frac{V_{IN}}{V_o}T$

where $T = t_{ON} + t_{OFF} = \frac{1}{f}$

$$t_{ON} = T - \frac{V_{IN}}{V_o}T = T\left(\frac{V_o - V_{IN}}{V_o}\right) \text{ therefore:}$$

$$C_o = \frac{I_oT\left(\frac{V_o - V_{IN}}{V_o}\right)}{\Delta V_o} = \boxed{\frac{I_o(V_o - V_{IN})}{f\Delta V_oV_o}}$$

where: C_o is in farads, f is the switching frequency, ΔV_o is the p-p output ripple

Calculation of inductor L1 is as follows:

$$L1 = \frac{V_{IN}t_{ON}}{\Delta I_L^+}, \text{ since during } t_{ON},$$

V_{IN} is applied across L1

$$\Delta I_{Lp\text{-}p} = 0.4I_L = 0.4I_{IN} = 0.4I_o\left(\frac{V_o}{V_{IN}}\right), \text{ therefore:}$$

$$L1 = \frac{V_{IN}t_{ON}}{0.4I_o\left(\frac{V_o}{V_{IN}}\right)} \text{ and since } t_{ON} = \frac{T(V_o - V_{IN})}{V_o}$$

$$\boxed{L1 = \frac{2.5\ V_{IN}^2(V_o - V_{IN})}{f\ I_oV_o^2}}$$

where : L1 is in henrys, f is the switching frequency in Hz

Typical Applications (Continued)

To apply the above theory, a complete step-up switching regulator is shown in *Figure 20*. Since V_{IN} is 5V, V_{REF} is tied to V_{IN}. The input voltage is divided by 2 to bias the error amplifier's inverting input. The output voltage is:

$$V_{OUT} = \left(1 + \frac{R2}{R1}\right) \bullet V_{INV} = 2.5 \bullet \left(1 + \frac{R2}{R1}\right)$$

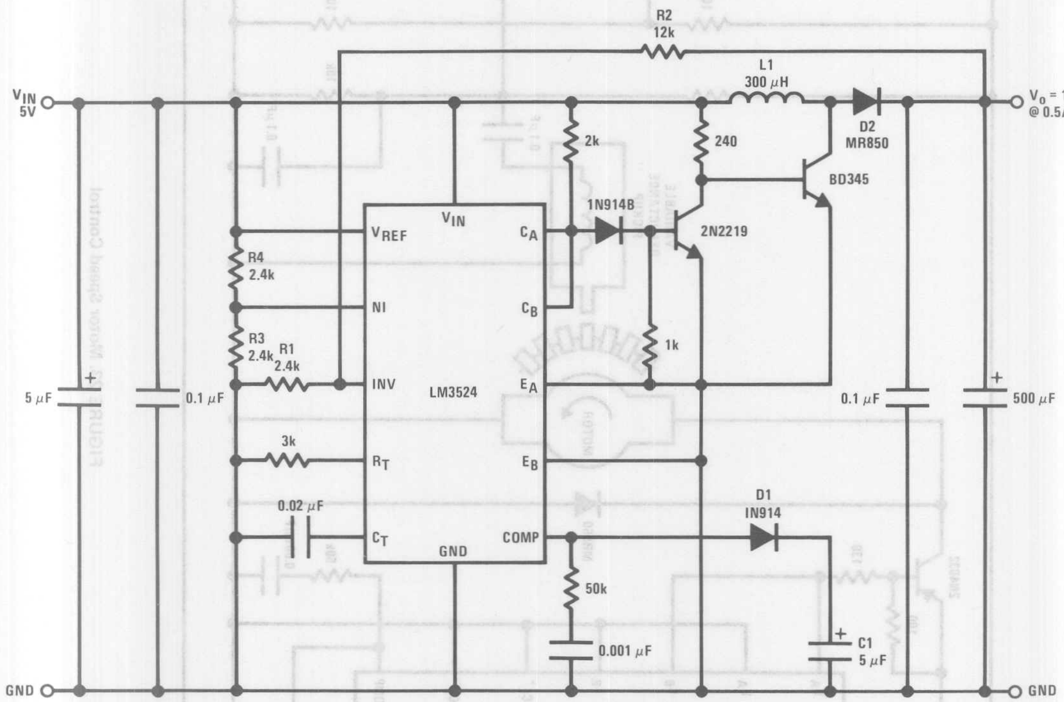
The network D1, C1 forms a slow start circuit.

This holds the output of the error amplifier initially low thus reducing the duty-cycle to a minimum. Without the slow start circuit the inductor may saturate at turn-on because it has to supply high peak currents to charge the output capacitor from 0V. It should also be noted that this circuit has no supply rejection. By adding a reference voltage at the non-inverting input to the error amplifier, see *Figure 21*, the input voltage variations are rejected.

The LM3524 can also be used in inductorless switching regulators. *Figure 22* shows a polarity inverter which if connected to *Figure 20* provides a −15V unregulated output.

MOTOR SPEED CONTROL

Figure 23 shows a regulating series DC motor speed control circuit using the LM3524 for the control and drive for the motor and the LM2907 as a speed sensor for the feedback network.



L1 = > 25 turns No. 24 wire on Ferroxcube No. K300502 Torroid core.

FIGURE 20. 15V, 0.5A Step-Up Switching Regulator

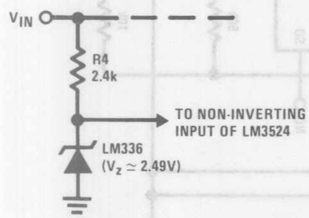


FIGURE 21

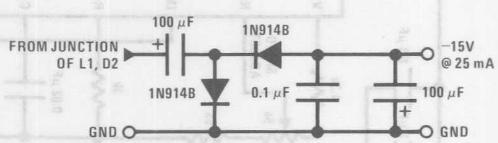


FIGURE 22

Typical Applications (Continued)

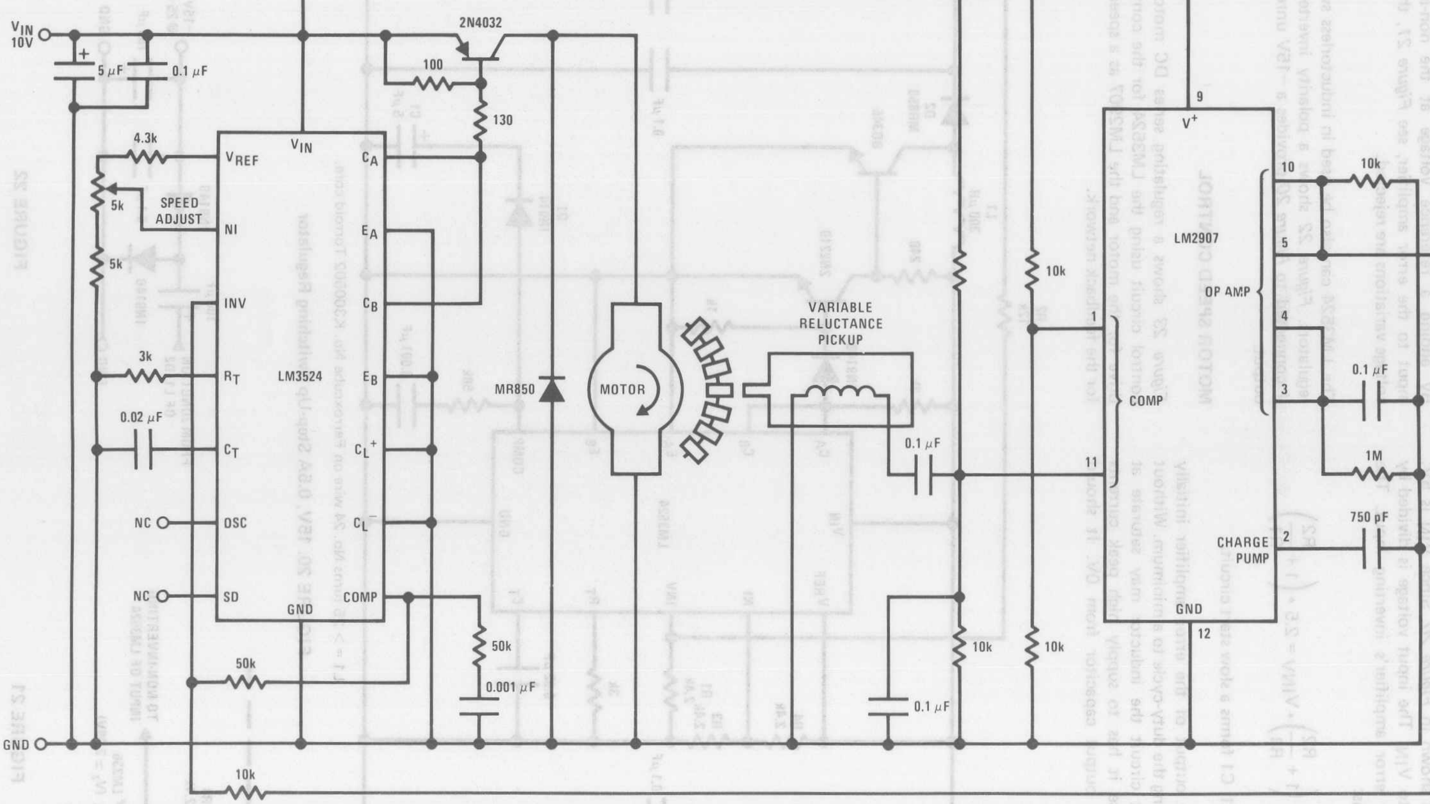


FIGURE 23. Motor Speed Control

National Semiconductor

LH1605/LH1605C
5 Amp, High Efficiency Switching Regulator

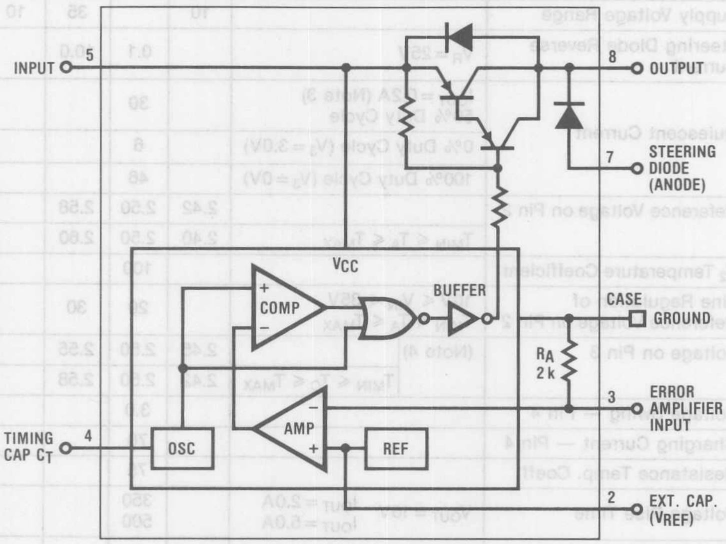
General Description

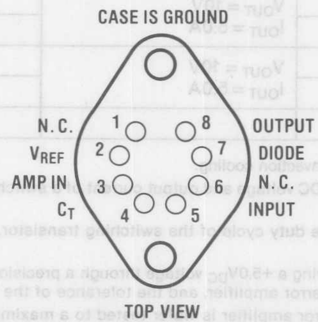
The LH1605 is a hybrid switching regulator with high output current capability. It incorporates a temperature-compensated voltage reference, a duty cycle modulator with the oscillator frequency programmable, error amplifier, high current-high voltage output switch, and a power diode. The LH1605 can supply up to 5 A of output current over a wide range of regulated output voltages.

Features

- Step down switching regulator
- Output adjustable from 3.0 to 30 V
- 5 A output current
- High efficiency
- Frequency adjustable to 100 kHz
- Standard 8-pin TO-3 package

Block Diagram and Connection Diagram





Order Number LH1605K or LH1605CK
See NS Package K08A

I_{OUT}	Output Current	6A
T_J	Operating Temperature	150°C
P_D	Internal Power Dissipation	20W
T_A	Operating Temperature Range	
	LH1605C	−25°C to +85°C
	LH1605	−55°C to +125°C
T_{STG}	Storage Temperature Range	−65°C to +150°C
V_R (V_{8-7})	Steering Diode Reverse Voltage	60V
I_D (I_{7-8})	Steering Diode Forward Current	6A

Electrical Characteristics $T_C = 25°C$, $V_{IN} = 15V$ unless otherwise specified.

Symbol	Characteristics	Conditions	LH1605 Min.	LH1605 Typ.	LH1605 Max.	LH1605C Min.	LH1605C Typ.	LH1605C Max.	Units
V_{OUT}	Output Voltage Range	$V_{IN} \geq V_{OUT} + 5V$ $I_{OUT} = 2A$ (Note 2)	3.0		30	3.0		30	V
V_S	Switch Saturation Voltage	$I_C = 5.0A$ $I_C = 2.0A$		1.5 1.0	2.0 1.2		1.5 1.0	2.0 1.2	V
V_F	Steering Diode On Voltage	$I_D = 5.0A$ $I_D = 2.0A$		2.0 1.6	2.8 2.0		2.0 1.6	2.8 2.0	V
V_{IN}	Supply Voltage Range		10		35	10		35	V
I_R	Steering Diode Reverse Current	$V_R = 25V$		0.1	10.0		0.1	10.0	μA
I_Q	Quiescent Current	$I_{OUT} = 0.2A$ (Note 3) 50% Duty Cycle		30			30		mA
		0% Duty Cycle ($V_3 = 3.0V$)		6			6		mA
		100% Duty Cycle ($V_3 = 0V$)		46			46		mA
V_2	Reference Voltage on Pin 2		2.42	2.50	2.58		2.50		V
		$T_{MIN} \leq T_A \leq T_{MAX}$	2.40	2.50	2.60		2.50		V
$\Delta V_2/\Delta T$	V_2 Temperature Coefficient			100			100		ppm/°C
ΔV_2	Line Regulation of Reference Voltage on Pin 2	$10V \leq V_{IN} \leq 35V$ $T_{MIN} \leq T_A \leq T_{MAX}$		20	30		20		mV
V_3	Voltage on Pin 3	(Note 4)	2.45	2.50	2.55		2.50		V
		(Note 4) $T_{MIN} \leq T_C \leq T_{MAX}$	2.42	2.50	2.58		2.50		V
V_4	Voltage Swing — Pin 4			3.0			3.0		V
I_4	Charging Current — Pin 4			70			70		μA
$\Delta R_A/\Delta T$	Resistance Temp. Coeff.			75			75		ppm/°C
t_r	Voltage Rise Time	$V_{OUT} = 10V$ $I_{OUT} = 2.0A$ $I_{OUT} = 5.0A$		350 500			350 500		ns
t_f	Voltage Fall Time	$V_{OUT} = 10V$ $I_{OUT} = 2.0A$ $I_{OUT} = 5.0A$		300 400			300 400		ns
t_s	Storage Time	$V_{OUT} = 10V$ $I_{OUT} = 5.0A$		1.5			1.5		μs
t_d	Delay Time	$V_{OUT} = 10V$ $I_{OUT} = 5.0A$		100			100		ns
P_D	Power Dissipation	$V_{OUT} = 10V$ $I_{OUT} = 5.0A$		16			16		W
η	Efficiency	$V_{OUT} = 10V$ $I_{OUT} = 5.0A$		75			75		%
θ_{JC}	Thermal Resistance			5.0			5.0		°C/W

Note 1: θ_{JA} is typically 30°C/W for natural convection cooling.

Note 2: V_{OUT} and I_{OUT} refer to the output DC voltage and output current of a switching supply after the output LC filter as shown in the Typical Application circuit.

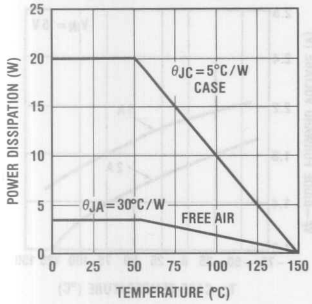
Note 3: Quiescent current depends on the duty cycle of the switching transistor. The average quiescent current may be calculated from known operating parameters.

Note 4: Voltage on pin 3 is tested by applying a $+5.0V_{DC}$ voltage through a precision 2.0kΩ resistor to pin 3. This method combines the error due to the input bias current of the error amplifier, and the tolerance of the 2kΩ resistor from pin 3 to ground.

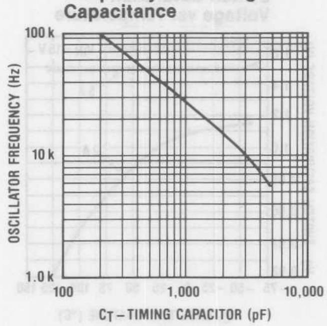
Note 5: The input offset voltage of the error amplifier is wafer tested to a maximum of 10mV.

Typical Performance Characteristics

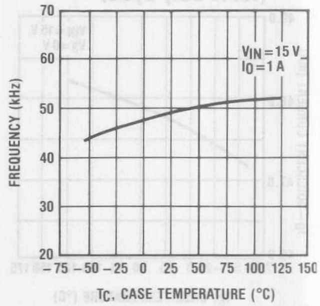
Power Derating Curve



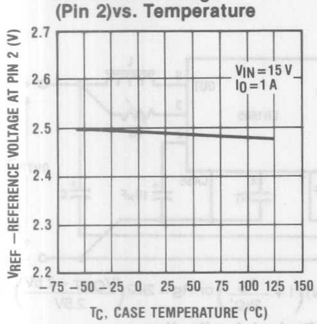
Frequency vs. Timing Capacitance



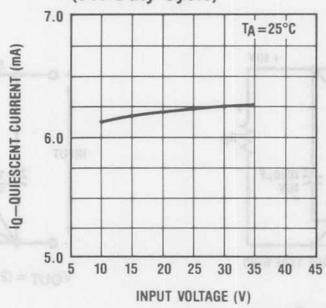
Frequency vs. Temperature



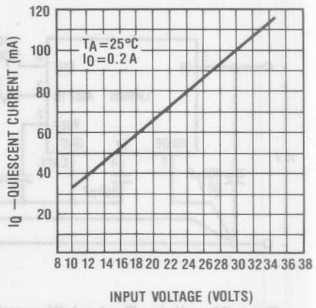
Reference Voltage (Pin 2)vs. Temperature



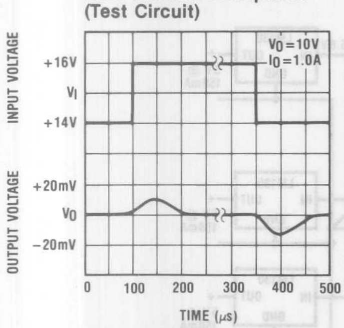
Quiescent Current vs. Input Voltage (0% Duty Cycle)



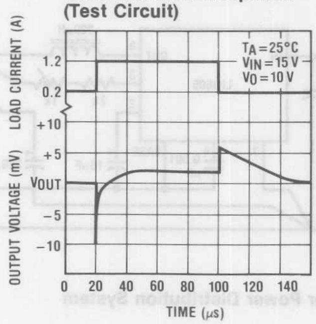
Quiescent Current vs. Input Voltage (100% Duty Cycle)



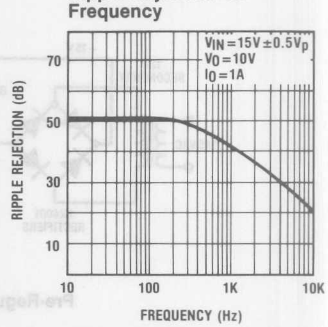
Line Transient Response (Test Circuit)



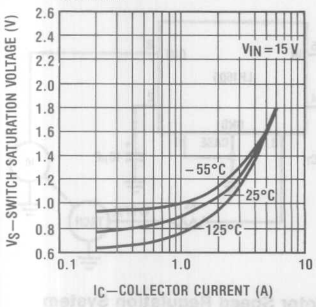
Load Transient Response (Test Circuit)



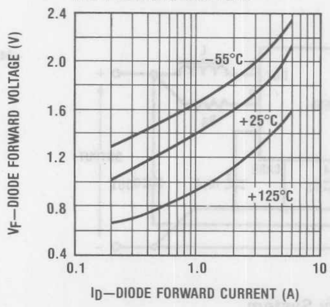
Ripple Rejection vs. Frequency



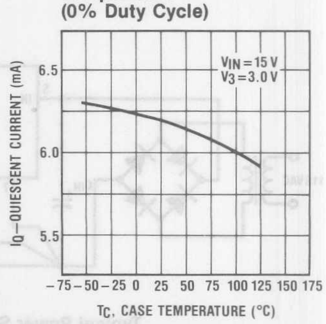
Switch Saturation Voltage vs. Collector Current



Diode Forward Voltage vs. Forward Current

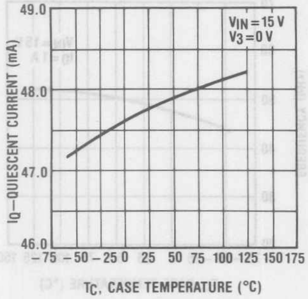


Quiescent Current vs. Temperature (0% Duty Cycle)

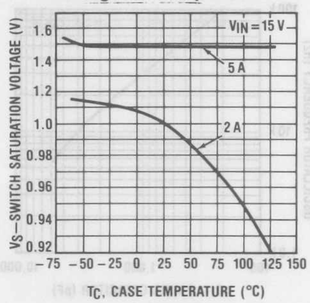


Typical Performance Characteristics (continued)

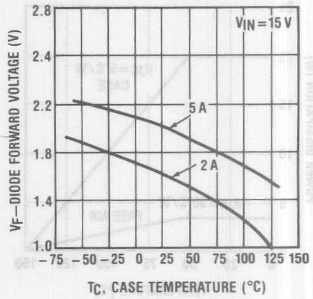
Quiescent Current vs. Temperature (100% Duty Cycle)

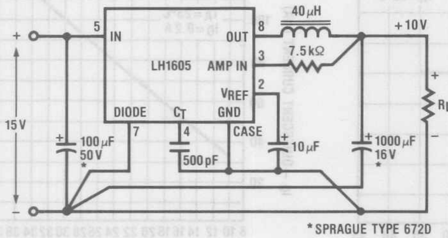


Switch Saturation Voltage vs. Temperature

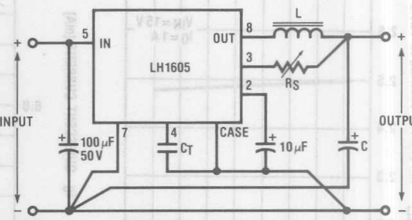


Diode Forward Saturation Voltage vs. Temperature



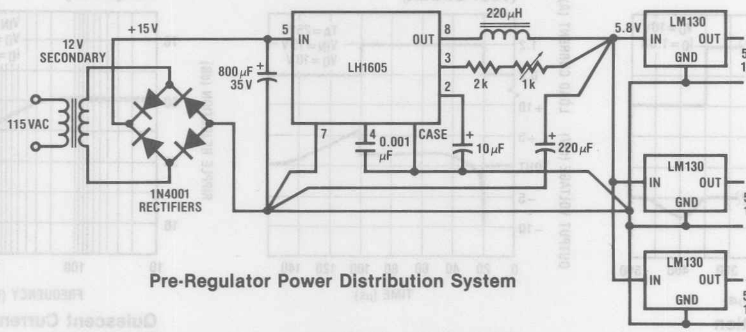


Test Circuit for Typical Characteristic Curves

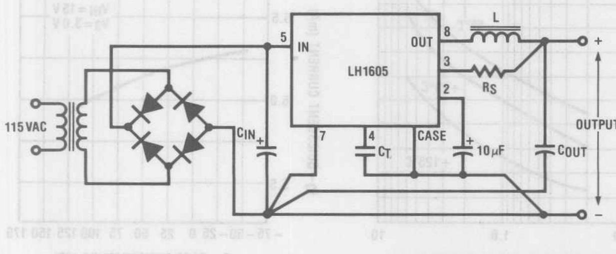


$$V_{OUT} = (2.50V)\left(1 + \frac{R_S}{2k\Omega}\right) \text{ or } R_S = 2k\Omega\left(\frac{V_{OUT} - 2.5V}{2.5V}\right)$$

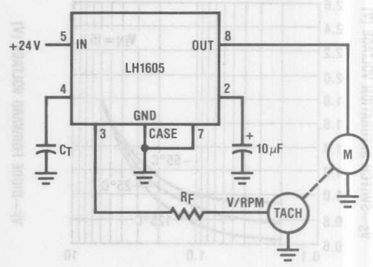
Typical Application



Pre-Regulator Power Distribution System



Typical Power Supply System



Motor Speed Regulation System

Applications Information

Output Voltage Programming

A single resistor is required to set the supply output voltage. The value may be computed using the following relationship:

$$R_S = 2\,k\Omega\,\frac{V_{OUT} - 2.5V}{2.5V}$$

The internal $2\,k\Omega$ resistor connected between pin 3 and ground has a typical tolerance of $\pm 1\%$ and a typical temperature coefficient of $\pm 75\,ppm/^\circ C$. Thus the overall supply tolerance may be computed given the tolerance of the reference voltage at pin 2.

Short Circuit Protection

Permanent damage to the device will result under prolonged ($>10\,ms$) short circuit condition. Current limit protection may be added using the circuit shown in the following figure:

Heat Sink Considerations

Even at moderate output power, there will be significant self-heating due to internal power dissipation. The junction temperature rise must be kept below 150°C under all operating conditions. A useful expression for steady-state thermal design is given below:

$$P_{DISS} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JC} + \theta_{CS} + \theta_{SA}}$$

where:

$T_{J(MAX)}$ = Maximum allowable junction temperature, °C.

$T_{A(MAX)}$ = Maximum ambient operating temperature, °C.

θ_{JC} = Device junction-to-case thermal resistance, typically 4.5°C/W.

θ_{CS} = Case-to-heatsink thermal resistance in °C/W.

θ_{SA} = Heatsink-to-ambient thermal resistance in °C/W.

Typically, the case-to-heatsink thermal resistance depends on the interface materials used. The following list gives the expected values for various materials:

0.002″ thick insulating Mica,	
without thermal grease	1.20°C/W
with thermal grease	0.35°C/W
0.003″ thick insulating Mica,	
without thermal grease	1.30°C/W
with thermal grease	0.38°C/W
Bare joint,	
without thermal grease	0.50°C/W
with thermal grease	0.15°C/W

Most heatsink manufacturers do provide the heatsink-to-ambient thermal resistance, under convection as well as forced-air cooling. A partial list of the hardware is included in the back of the data sheet.

Reference Voltage Bypass

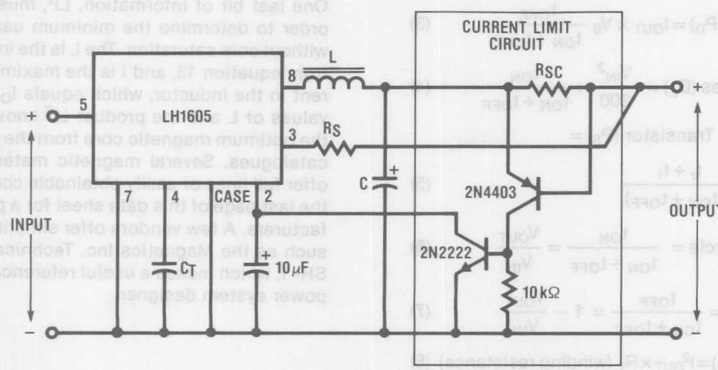
Because of the inherent high current switching nature of the device, switching spikes can find their way into the linear amplifier circuit. Output noise and ripple voltage can be improved drastically by bypassing the reference voltage pin with a $10\,\mu F$ solid tantalum capacitor connected from pin 2 to ground.

Minimization of Output Voltage Spikes

The best solution to minimize switching spike noise can be found in laying out the circuit. An input single-point ground and an output single-point ground should be used. The schematic is shown in the typical application circuit. Where high current flows, conductor trace should be as wide as possible.

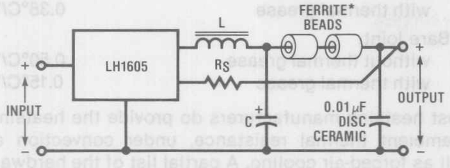
The ripple current frequency is usually in the order of tens of kilohertz, therefore the input and output filter capacitors should be of low ESR (Equivalent Series Resistance) type over extended frequency range in order to minimize noise generation. They should be of high quality construction with ratings sufficient to withstand current and voltage surges. Generally, selecting a capacitor with a working voltage rating that is a minimum of 10V above the worst-case operating voltage is recommended.

The output can be filtered further by means of a very high frequency π-filter network using inexpensive ferrite beads. An example is shown in the figure below. Because the fre-



$$R_{SC} = \frac{0.6V}{I_{SC}}$$

dance peak in that region. One or more beads may be strung in series on the wire to increase the peak impedance as well as to increase the absorption loss to the higher frequencies. This would also minimize parasitic oscillation.



*FERRONICS TYPE J CORE MATERIAL
FERROXCUBE TYPE 4A6 CORE MATERIAL

RFI/EMI Suppression

High frequency radiation can be an important system consideration, particularly if the surrounding circuitry is sensitive to it. Metallic shielding around the switching circuitry is an effective means of suppression. A perforated metal cover works well both to contain radiation and to allow unrestricted convection cooling. Grounded conductor plane on the PC board also helps fully enclose the critical circuits.

Metallic shield is generally adequate in shielding the magnetic field radiated around the magnetic components. A more effective design is the use of the self-shielding property of ferrite pot core, which acts as EMI shield around the coil winding. Magnetic flux leakage of this type is minimal.

Design Guide

Efficiency Calculation

The design of a complete voltage regulator with the LH1605 is relatively straightforward. The efficiency of a regulator can be calculated with the following equations:

$$\text{Efficiency } (\eta) = \frac{P_{OUT} \times 100}{P_{IN}} \quad (1)$$

$$\text{Transistor DC Losses } (P_T) = I_{OUT} \times V_S \frac{t_{ON}}{t_{ON} + t_{OFF}} \quad (2)$$

$$\text{Diode DC Losses } (P_D) = I_{OUT} \times V_S \frac{t_{OFF}}{t_{ON} + t_{OFF}} \quad (3)$$

$$\text{Drive Circuit Losses } (D_L) = \frac{V_{IN}^2}{300} \times \frac{t_{ON}}{t_{ON} + t_{OFF}} \quad (4)$$

Switching Losses Transistor (P_S) =

$$V_{IN} \times I_{OUT} \frac{t_r + t_f}{2(t_{ON} + t_{OFF})} \quad (5)$$

$$\text{Transistor Duty Cycle} = \frac{t_{ON}}{t_{ON} + t_{OFF}} = \frac{V_{OUT}}{V_{IN}} \quad (6)$$

$$\text{Diode Duty Cycle} = \frac{t_{OFF}}{t_{ON} + t_{OFF}} = 1 - \frac{V_{OUT}}{V_{IN}} \quad (7)$$

$$\text{Power Inductor } (P_L) = I^2_{OUT} \times R_L \text{ (winding resistance)} \quad (8)$$

$$\text{Efficiency } (\eta) = \frac{V_{OUT} I_{OUT}}{V_{OUT} I_{OUT} + P_T + P_D + D_L + P_S + P_L} \times 100 \quad (9)$$

1. Maximum and minimum input voltage.
2. Required output voltage.
3. Maximum and minimum load current.
4. Maximum allowable ripple voltage.
5. Desired switching frequency.

The values of the output LC filter can be computed. First, the off-time of the switching transistor is calculated.

$$t_{OFF} = \frac{1 - \dfrac{V_{OUT}}{V_{IN(MAX)}}}{f} \quad (10)$$

The minimum equivalent frequency of the switching transistor at minimum input voltage is:

$$f_{MIN} = \frac{1 - \dfrac{V_{OUT}}{V_{IN(MIN)}}}{t_{OFF}} \quad (11)$$

The allowable peak-to-peak ripple current (Δi) through the inductor is:

$$\Delta i = 2 \times I_{O(MIN)} \quad (12)$$

The inductance can now be calculated by:

$$L = \frac{V_{OUT}\, t_{OFF}}{\Delta i} \quad (13)$$

The value calculated for Δi is somewhat arbitrary. However, equation 12 is a good rule of thumb. Thus Δi may be adjusted to obtain a practical value for the inductance.

The minimum output filter capacitance is given by:

$$C = \frac{\Delta i}{8 \times f_{MIN} \times \Delta e_O} \quad (14)$$

where Δe_O is the allowable ripple voltage.

Finally, the maximum ESR of the capacitor is:

$$ESR_{MAX} = \frac{\Delta e_O}{\Delta i} \quad (15)$$

Inductor Design

One last bit of information, LI^2, must be calculated in order to determine the minimum usable inductor core without core saturation. The L is the inductance obtained from equation 13, and I is the maximum DC output current in the inductor, which equals $I_{O(MAX)} + \Delta i$. With the values of L and the product LI^2 known, one can select the optimum magnetic core from the core manufacturer catalogues. Several magnetic material manufacturers offer full lines of easily obtainable components. Refer to the last page of this data sheet for a partial list of manufacturers. A few vendors offer simplified design guides, such as the Magnetics Inc. Technical Bulletin Number SR-1, which makes a useful reference for any switching power system designer.

At this point, the designer must choose the core material type. There are two popular types — molypermalloy powder and ferrite cores. Both offer advantages depending on cost, space limitations, winding capabilities, and size for a given operating frequency.

Ferrite pot cores have the advantages of ease of winding and inherent magnetic self-shielding, whereas molypermalloy powder cores are made of insulated embrittled alloy powder which provides a uniformly distributed air gap. The effect is that the latter is capable of higher flux density for a given core size than ferrite core.

Once the core is selected, the number of winding turns N can be determined to obtain the required inductance:

$$N = 1000\sqrt{L/L_{1000}} \tag{16}$$

where:

N = number of turns needed.

L = inductance desired.

L_{1000} = nominal inductance (mH/1000 turns) for a given core specifed by the manufacturers.

Design Example

Design requirements:

$V_{IN(MAX)} = 15V$

$V_{IN(MIN)} = 10V$

$V_{OUT} = 5V$

$I_{O(MAX)} = 3A$

$I_{O(MIN)} = 1A$

Output Ripple $(\Delta e_O) = 20\,mV$

Operating Frequency (f) = 25 kHz

Using equations 10 through 15:

$$t_{OFF} = \frac{1 - \frac{5V}{15V}}{25\,kHz} = 26.7\,\mu s$$

$$f_{MIN} = \frac{1 - \frac{5V}{10V}}{26.7\,\mu s} = 18.7\,kHz$$

$$\Delta i = 2 \times 1A = 2A$$

$$L = \frac{5V \times 26.7\,\mu s}{2A} = 67\,\mu H$$

$$C = \frac{2A}{8 \times 18.7\,kHz \times 20\,mV} = 668\,\mu F \text{ Minimum}$$

$$ESR_{MAX} = \frac{20 \times 10^{-3}}{2} = 10\,m\Omega$$

The power handling capability of the inductor is calculated:

$$E_L = LI^2$$

where:

L = Inductor

I = Peak current in the inductor

$= I_{O(MAX)} + \Delta i$

$$LI^2 = (67\,\mu H)\,(3A + 2A)^2 = 1.68 \text{ millijoules}$$

Assuming molypermalloy powder core is chosen for the design, and using the Core Selection Table in the Magnetic, Inc. Technical Bulletin Number SR-1, the minimum core size usable with minimum winding is Part Number 55894, which is a 60 perm core. Since the 125 perm of the same core size family is very popular and consequently of lower cost, the 55930 part is selected for the design. The specified nominal inductance is 157 mH per 1000 turns. The numer of turns is calculated from equation 16:

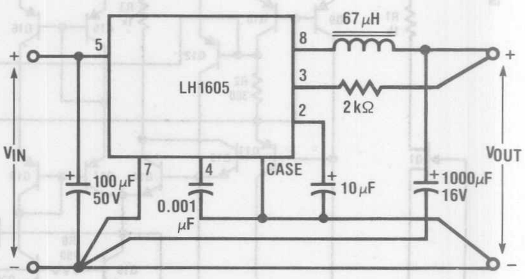
$$N = 1000\sqrt{\frac{67\,\mu H}{157\,mH}} = 21 \text{ turns}$$

Using the Frequency vs. Timing Capacitor Plot, a 0.001 µF capacitor is used in order to obtain the 25 kHz operating frequency.

Finally, the output of 5V is programmed by computing the output voltage-set resistor:

$$R_S = 2\,k\Omega\,\frac{V_{OUT} - 2.5V}{2.5V} = 2\,k\Omega$$

The complete design is shown in the schematic below:



$V_{IN} = 12V$ Output Ripple (@ $I_O = 1A$) = $50\,mV_{P\text{-}P}$

$V_{OUT} = 5V$ (@ $I_O = 3A$) = $100\,mV_{P\text{-}P}$

Load Regulation (1A to 3A) = 30mV

Line Regulation (10V to 20V) = 10mV

National Semiconductor

Voltage Regulators

LM2930 3-Terminal Positive Regulator

General Description

The LM2930 3-terminal positive voltage regulator features an ability to source 150 mA of output current with an input-output differential of 0.6V or less. Efficient use of low input voltages obtained, for example, from an automotive battery during cold crank conditions, allows 5V circuitry to be properly powered with supply voltages as low as 5.6V. Familiar regulator features such as current limit and thermal overload protection are also provided.

Designed primarily for automotive applications, the LM2930 and all regulated circuitry are protected from reverse battery installations or 2 battery jumps. During line transients, such as a load dump (40V) when the input voltage to the regulator can momentarily exceed the specified maximum operating voltage, the regulator will automatically shut down to protect both internal circuits and the load. The LM2930 cannot be harmed by temporary mirror-image insertion.

Fixed outputs of 5V and 8V are available in the plastic TO-220 power package.

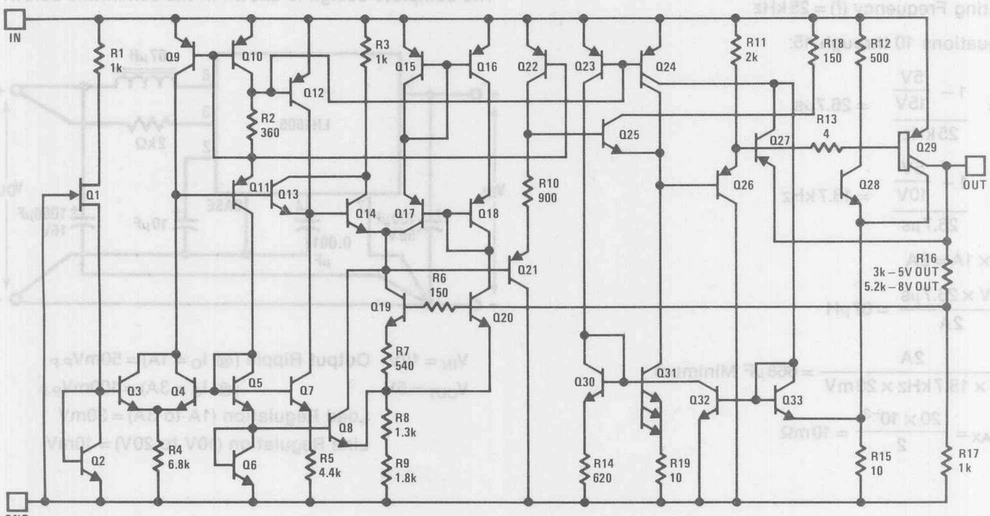
Features

- Input-output differential less than 0.6V
- Output current in excess of 150 mA
- Reverse battery protection
- 40V load dump protection
- Internal short circuit current limit
- Internal thermal overload protection
- Mirror-image insertion protection
- 100% electrical burn-in in thermal limit

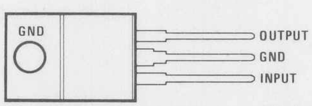
Voltage Range

LM2930T-5.0	5V
LM2930T-8.0	8V

Schematic and Connection Diagrams



(TO-220)
Plastic Package



FRONT VIEW

Order Number LM2930T-5.0 or LM2930T-8.0
See NS Package T03B

Absolute Maximum Ratings

Input Voltage	
Operating Range	26V
Overvoltage Protection	40V
Reverse Voltage (100 ms)	−12V
Reverse Voltage (DC)	−6V
Internal Power Dissipation (Note 1)	Internally Limited
Operating Temperature Range	−40°C to +85°C
Maximum Junction Temperature	125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	230°C

Electrical Characteristics (Note 2)

LM2930T-5.0 (V_{IN} = 14V, I_O = 150 mA, T_j = 25°C, C2 = 10 μF, unless otherwise specified)

Parameter	Conditions	Min	Typ	Max	Units
Output Voltage	$6V \le V_{IN} \le 26V$, $5\ mA \le I_O \le 150\ mA$, $-40°C \le T_j \le +125°C$	4.5	5	5.5	V
Line Regulation	$9V \le V_{IN} \le 16V$, $I_O = 5\ mA$ $6V \le V_{IN} \le 26V$, $I_O = 5\ mA$		7 30	25 80	mV mV
Load Regulation	$5\ mA \le I_O \le 150\ mA$		14	50	mV
Output Impedance	100 mA_{DC} & 10 mArms, 100 Hz-10 kHz		200		mΩ
Quiescent Current	I_O = 10 mA I_O = 150 mA		4 18	7 40	mA mA
Output Noise Voltage	10 Hz-100 kHz		140		μVrms
Long Term Stability			20		mV/1000 hr
Ripple Rejection	f_O = 120 Hz		56		dB
Current Limit		150	400	700	mA
Dropout Voltage	I_O = 150 mA		0.32	0.6	V
Output Voltage Under Transient Conditions	$-12V \le V_{IN} \le 40V$, $R_L = 100Ω$	−0.3		5.5	V

Electrical Characteristics (Note 2)

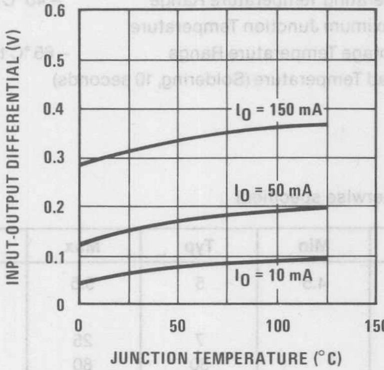
LM2930T-8.0 (V_{IN} = 14V, I_O = 150 mA, T_j = 25°C, C2 = 10 μF, unless otherwise specified)

Parameter	Conditions	Min	Typ	Max	Units
Output Voltage	$9.4V \le V_{IN} \le 26V$, $5\ mA \le I_O \le 150\ mA$, $-40°C \le T_j \le +125°C$	7.2	8	8.8	V
Line Regulation	$9.4V \le V_{IN} \le 16V$, $I_O = 5\ mA$ $9.4V \le V_{IN} \le 26V$, $I_O = 5\ mA$		12 50	50 100	mV mV
Load Regulation	$5\ mA \le I_O \le 150\ mA$		25	50	mV
Output Impedance	100 mA_{DC} & 10 mArms, 100 Hz-10 kHz		300		mΩ
Quiescent Current	I_O = 10 mA I_O = 150 mA		4 18	7 40	mA mA
Output Noise Voltage	10 Hz-100 kHz		170		μVrms
Long Term Stability			30		mV/1000 hr
Ripple Rejection	f_O = 120 Hz		52		dB
Current Limit		150	400	700	mA
Dropout Voltage	I_O = 150 mA		0.32	0.6	V
Output Voltage Under Transient Conditions	$-12V \le V_{IN} \le 40V$, $R_L = 100Ω$	−0.3		8.8	V

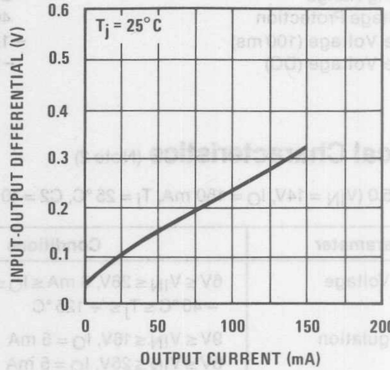
Note 1: Thermal resistance without a heat sink for junction to case temperature is 4°C/W and for case to ambient temperature is 50°C/W.

Note 2: All characteristics are measured with a capacitor across the input of 0.1 μF and a capacitor across the output of 10 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \le 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

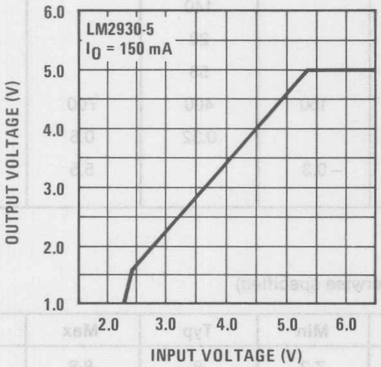
Dropout Voltage



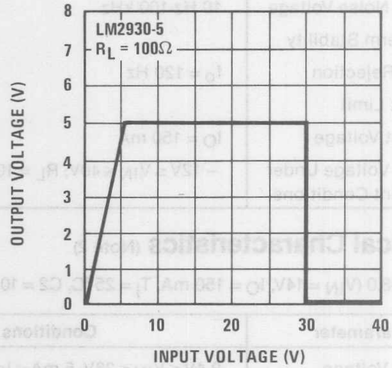
Dropout Voltage



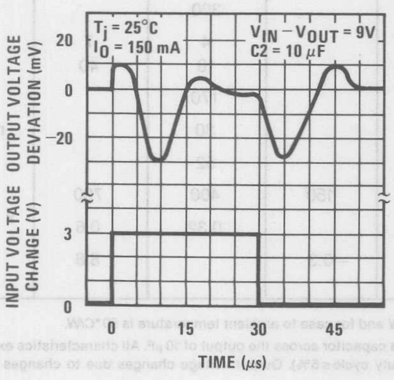
Low Voltage Behavior



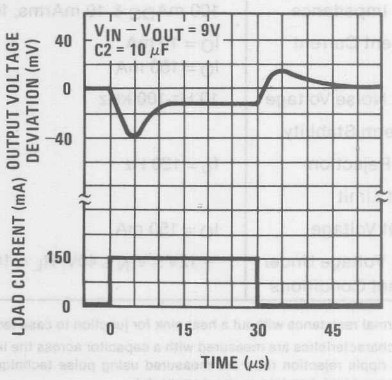
High Voltage Behavior



Line Transient Response

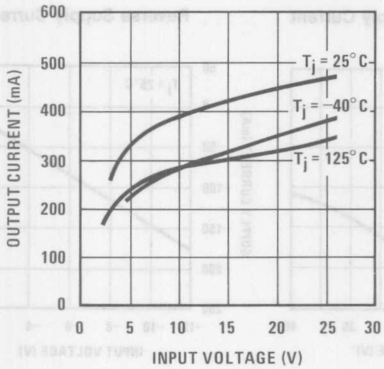


Load Transient Response

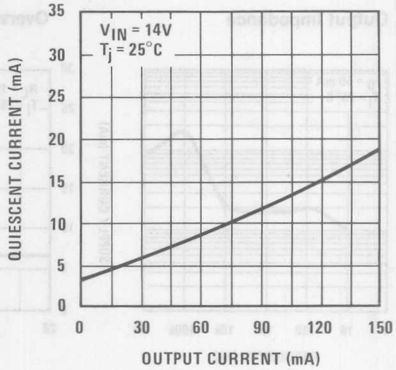


Typical Performance Characteristics (Continued)

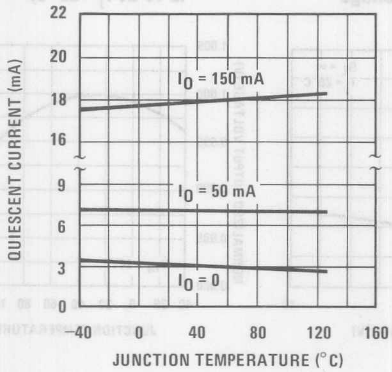
Peak Output Current



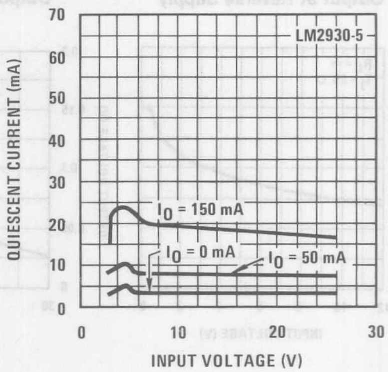
Quiescent Current



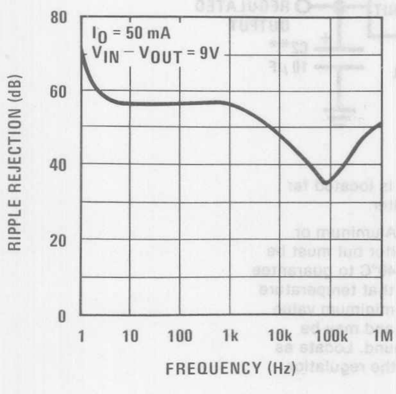
Quiescent Current



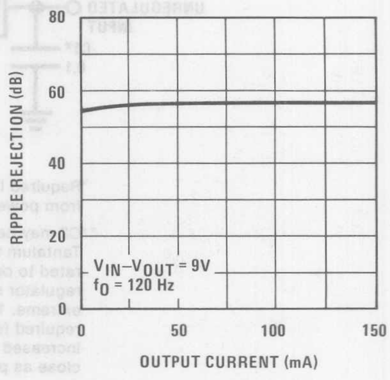
Quiescent Current



Ripple Rejection

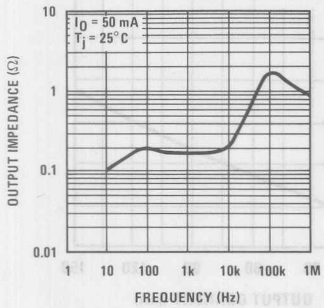


Ripple Rejection

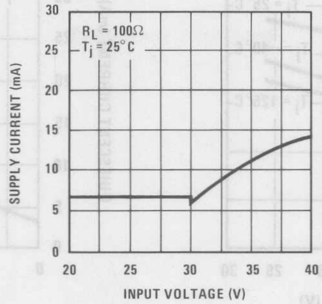


Typical Performance Characteristics (Continued)

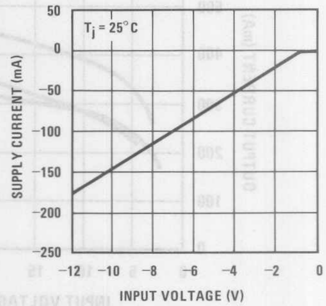
Output Impedance



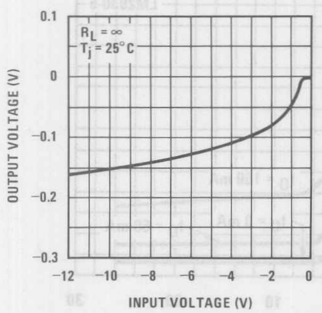
Overvoltage Supply Current



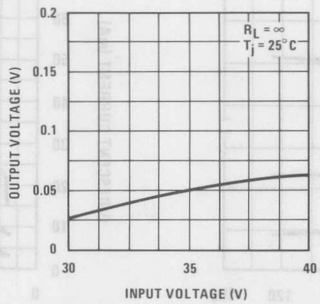
Reverse Supply Current



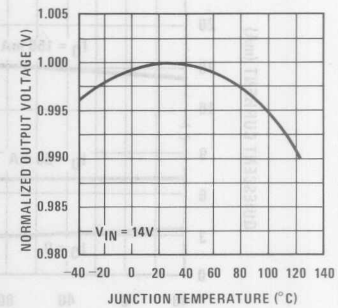
Output at Reverse Supply



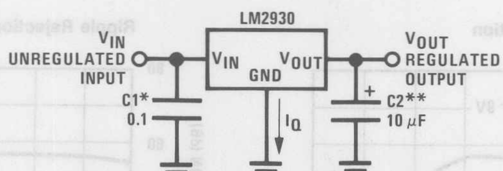
Output at Overvoltage



Output Voltage (Normalized to 1V at $T_j = 25°C$)



Typical Application



*Required if regulator is located far from power supply filter.

**C2 may be either an Aluminum or Tantalum type capacitor but must be rated to operate at −40°C to guarantee regulator stability to that temperature extreme. 10μF is the minimum value required for stability and may be increased without bound. Locate as close as possible to the regulation.

Definition of Terms

Dropout Voltage: The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14V input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Input-Output Differential: The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Long Term Stability: Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

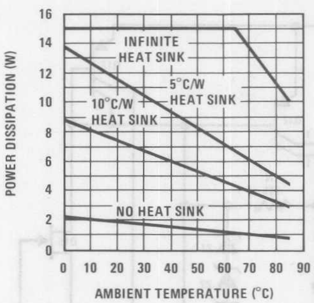
Output Noise Voltage: The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Quiescent Current: That part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

Ripple Rejection: The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

Temperature Stability of V_O: The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

Maximum Average Power Dissipation



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LM2931 Series Low Dropout Regulators

General Description

The LM2931 positive voltage regulator features a very low quiescent current of 1 mA or less when supplying 10 mA loads. This unique characteristic and the extremely low input-output differential required for proper regulation (0.2V for output currents of 10 mA) make the LM2931 the ideal regulator for standby power systems. Applications include memory standby circuits, CMOS and other low power processor power supplies as well as systems demanding as much as 150 mA of output current.

Designed primarily for automotive applications, the LM2931 and all regulated circuitry are protected from reverse battery installations or 2 battery jumps. During line transients, such as a load dump (60V) when the input voltage to the regulator can momentarily exceed the specified maximum operating voltage, the regulator will automatically shut down to protect both internal circuits and the load. The LM2931 cannot be harmed by temporary mirror-image insertion. Familiar regulator features such as short circuit and thermal overload protection are also provided.

Fixed output of 5V is available in the plastic TO-220 power package or the popular TO-92 package. An adjustable output version, with on/off switch, is available in a 5-lead TO-220 package.

Features

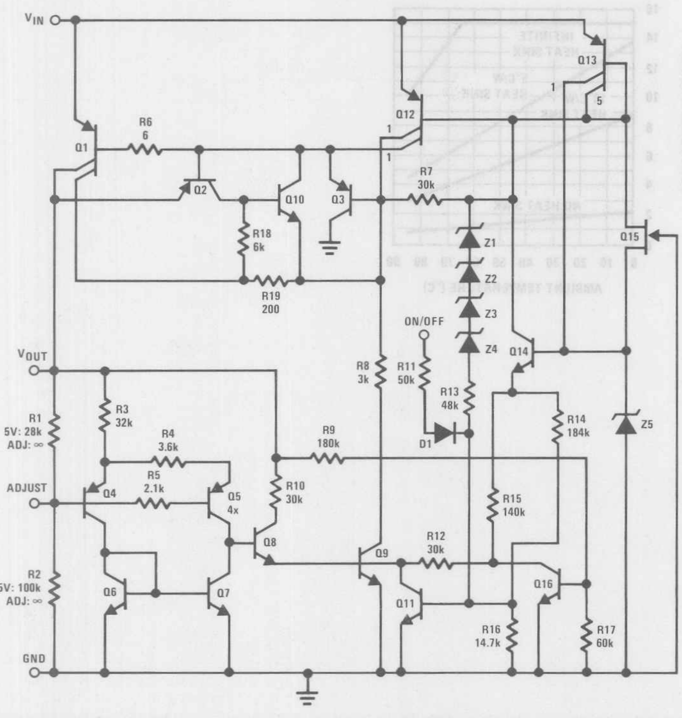
- Very low quiescent current
- Output current in excess of 150 mA
- Input-output differential less than 0.6V
- Reverse battery protection
- 60V load dump protection
- −50V reverse transient protection
- Short circuit protection
- Internal thermal overload protection
- Mirror-image insertion protection
- Available in plastic TO-220 or TO-92
- Available as adjustable with TTL compatible switch

Output Voltage Options

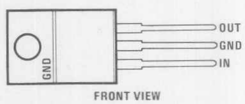
LM2931AT-5.0	5V	LM2931AZ-5.0	5V
LM2931T	Adjustable		

(Contact factory for other fixed output options.)

Schematic and Connection Diagrams

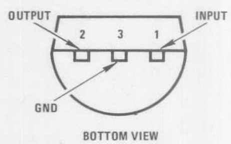


TO-220 3-Lead



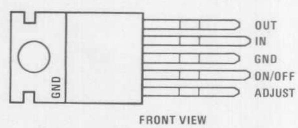
Order Number LM2931AT-5.0
See NS Package T03B

TO-92



Order Number LM2931AZ-5.0
See NS Package Z03A

TO-220 5-Lead



Order Number LM2931T
See NS Package T05A

Absolute Maximum Ratings

Input Voltage	
Operating Range	26V
Overvoltage Protection	
LM2931A, LM2931 Adjustable	60V
Internal Power Dissipation (Note 1)	Internally Limited
Operating Temperature Range	−40°C to +85°C
Maximum Junction Temperature	125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	230°C

Electrical Characteristics for 5V

($V_{IN}=14V$, $I_O=10$ mA, $T_j=25°C$ unless otherwise specified)

Parameter	Conditions	LM2931A-5.0 Min	LM2931A-5.0 Typ	LM2931A-5.0 Max	Units
Output Voltage	$6.0V \le V_{IN} \le 26V$, $I_O \le 150$ mA, $-40°C \le T_j \le +125°C$	4.75	5	5.25	V
Line Regulation	$9V \le V_{IN} \le 16V$ $6V \le V_{IN} \le 26V$		2 4	10 30	mV mV
Load Regulation	$5\text{ mA} \le I_O \le 150$ mA		14	50	mV
Output Impedance	100 mA_{DC} and 10 mArms, 100 Hz-10 kHz		200		mΩ
Quiescent Current	$I_O \le 10$ mA, $6V \le V_{IN} \le 26V$, $-40°C \le T_j \le +125°C$ $I_O=150$ mA, $V_{IN}=14V$, $T_j=25°C$		0.4 15	1	mA mA
Output Noise Voltage	10 Hz-100 kHz		500		μVrms
Long Term Stability			20		mV/1000 hr
Ripple Rejection	$f_o=120$ Hz		80		dB
Dropout Voltage	$I_O=10$ mA $I_O=150$ mA		0.05 0.3	0.2 0.6	V V
Maximum Operational Input Voltage		26	33		V
Maximum Line Transient	$R_L=500\Omega$, $V_O \le 5.5V$	60	70		V
Reverse Polarity Input Voltage, DC	$V_O \ge -0.3V$	−15	−30		V
Reverse Polarity Input Voltage, Transient	1% Duty Cycle, $\mathcal{T} \le 100$ ms	−50	−80		V

Electrical Characteristics for Adjustable

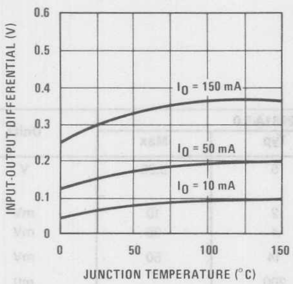
($V_{IN} \ge V_{OUT}+0.6V$, $I_O=10$ mA, $T_j=25°C$ unless otherwise specified)

Parameter	Conditions	LM2931T Min	LM2931T Typ	LM2931T Max	Units
Reference Voltage	$I_O \le 150$ mA, $-40°C \le T_j \le +125°C$, R1 = 27k Measured from V_{OUT} to Adjust Pin	1.12	1.20	1.28	V
Output Voltage Range	R1 = 27k	3		24	V
Line Regulation	$V_{OUT}+0.6V \le V_{IN} \le 26V$		0.2	1.5	mV/V
Load Regulation	$5\text{ mA} \le I_O \le 150$ mA		0.3	1	%
Output Impedance	100 mA_{DC} and 10 mArms, 100 Hz-10 kHz		40		mΩ/V
Quiescent Current	$I_O=10$ mA, $-40°C \le T_j \le +125°C$ $I_O=150$ mA During Shutdown $R_L=500\Omega$		0.4 15 0.8	1 1	mA mA mA
Output Noise Voltage	10 Hz-100 kHz		100		μVrms/V
Long Term Stability			0.4		%/1000 hr
Ripple Rejection	$f_o=120$ Hz		0.002		%/V
Dropout Voltage	$I_O \le 10$ mA $I_O=150$ mA		0.05 0.3	0.2 0.6	V V
Maximum Operational Input Voltage		26	33		V
Maximum Line Transient	$I_O=10$ mA, Reference Voltage $\le 1.5V$	60	70		V
Reverse Polarity Input Voltage, DC	$V_O \ge -0.3V$	−15	−30		V
Reverse Polarity Input Voltage, Transient	1% Duty Cycle, $\mathcal{T} \le 100$ ms	−50	−80		V
On/Off Threshold Voltage On Off	$-40°C \le T_j \le +125°C$	 3.0	 2.0 2.2	 1.2	 V V
On/Off Threshold Current			20	50	μA

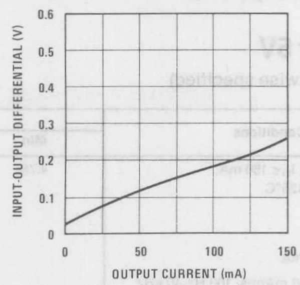
Note 1: Thermal resistance without a heat sink for junction to case temperature is 4°C/W (TO-220) and 55°C/W (TO-92). Thermal resistance for TO-220 case to ambient temperature is 50°C/W. Thermal resistance for TO-92 case to ambient with 0.125″ lead length to PC board is 105°C/W and with 0.4″ lead is 125°C/W.

Typical Performance Characteristics

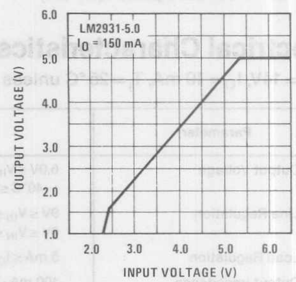
Dropout Voltage



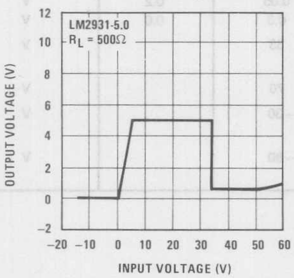
Dropout Voltage



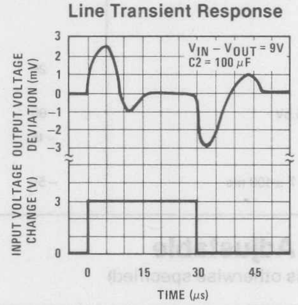
Low Voltage Behavior



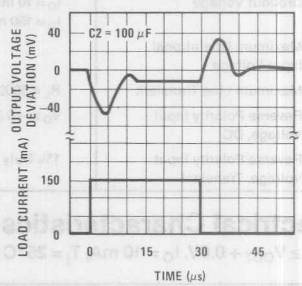
Output at Voltage Extremes



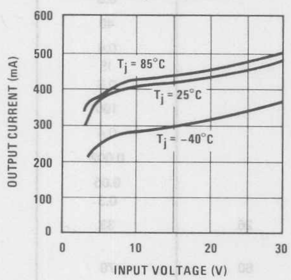
Line Transient Response



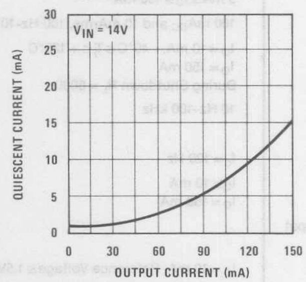
Load Transient Response



Peak Output Current



Quiescent Current



Series

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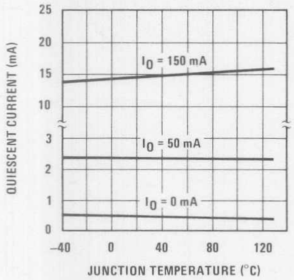
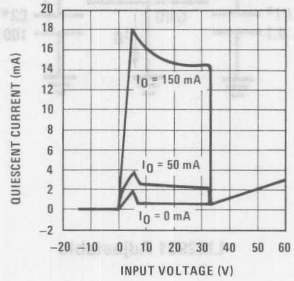
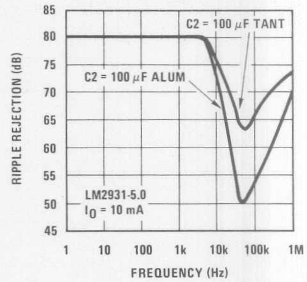
Quiescent Current



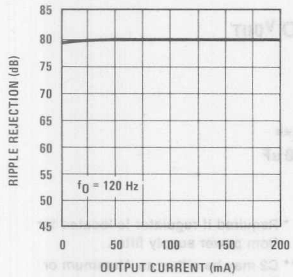
Quiescent Current



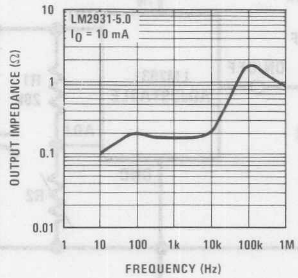
Ripple Rejection



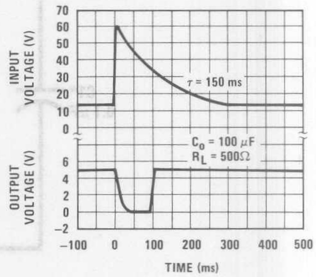
Ripple Rejection



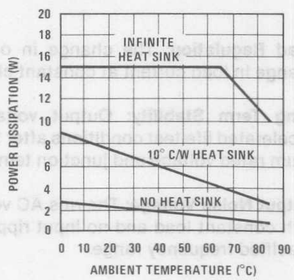
Output Impedance



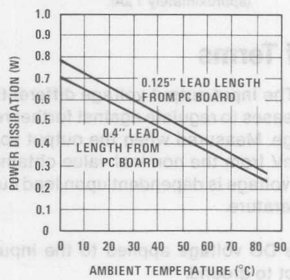
Operation During Load Dump

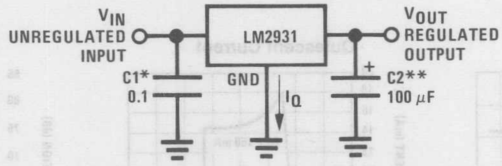


Maximum Power Dissipation (TO-220)

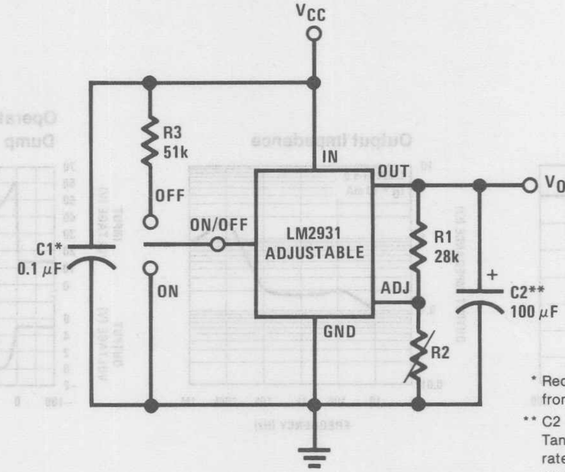


Maximum Power Dissipation (TO-92)





LM2931 Adjustable



$$V_{OUT} = \text{Reference Voltage} \times \frac{R1 + R2}{R1}$$

Note: Using 28k for R1 will automatically compensate for errors in V_{OUT} due to the input bias current of the ADJ pin (approximately 1 μA).

* Required if regulator is located far from power supply filter.

** C2 may be either an Aluminum or Tantalum type capacitor but must be rated to operate at −40°C to guarantee regulator stability to that temperature extreme. 100μF is the minimum value required for stability and may be increased without bound. Locate as close as possible to the regulator.

Definition of Terms

Dropout Voltage: The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14V input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Input-Output Differential: The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Long Term Stability: Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

Output Noise Voltage: The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Quiescent Current: That part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

Ripple Rejection: The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

Temperature Stability of V_O: The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

National Semiconductor

Voltage Regulators

LM78XX Series Voltage Regulators

General Description

The LM78XX series of three terminal regulators is available with several fixed output voltages making them useful in a wide range of applications. One of these is local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents.

The LM78XX series is available in an aluminum TO-3 package which will allow over 1.0A load current if adequate heat sinking is provided. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

Considerable effort was expended to make the LM78XX series of regulators easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

For output voltage other than 5V, 12V and 15V the LM117 series provides an output voltage range from 1.2V to 57V.

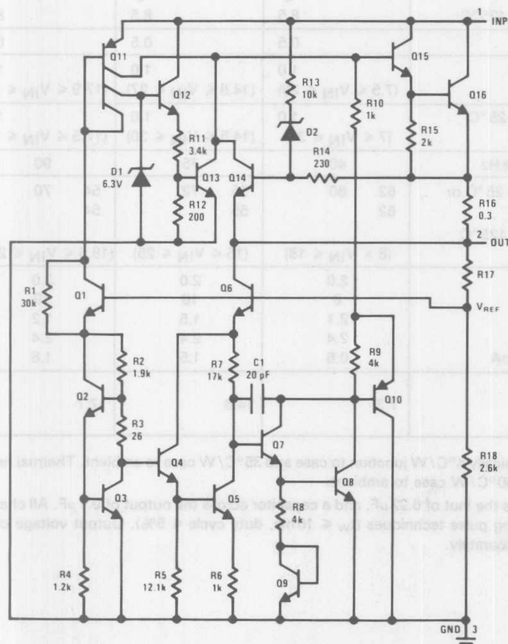
Features

- Output current in excess of 1A
- Internal thermal overload protection
- No external components required
- Output transistor safe area protection
- Internal short circuit current limit
- Available in the aluminum TO-3 package

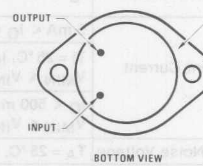
Voltage Range

LM7805C	5V
LM7812C	12V
LM7815C	15V

Schematic and Connection Diagrams



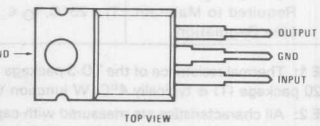
Metal Can Package
TO-3 (K)
Aluminum



BOTTOM VIEW

Order Numbers
LM7805CK
LM7812CK
LM7815CK
See Package KC02A

Plastic Package
TO-220 (T)



TOP VIEW

Order Numbers:
LM7805CT
LM7812CT
LM7815CT
See Package T03B

Absolute Maximum Ratings

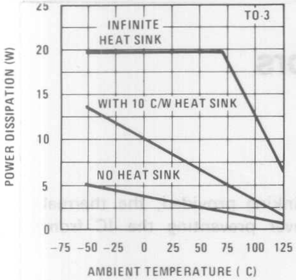
Input Voltage (V_O = 5V, 12V and 15V)	35V
Internal Power Dissipation (Note 1)	Internally Limited
Operating Temperature Range (T_A)	0 °C to +70 °C
Maximum Junction Temperature	
(K Package)	150 °C
(T Package)	125 °C
Storage Temperature Range	−65 °C to +150 °C
Lead Temperature (Soldering, 10 seconds)	
TO-3 Package K	300 °C
TO-220 Package T	230 °C

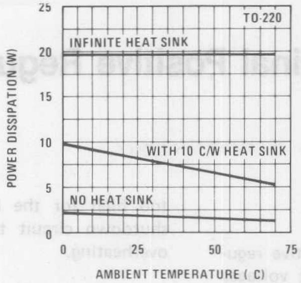
Electrical Characteristics LM78XXC (Note 2) 0 °C ≤ Tj ≤ 125 °C unless otherwise noted.

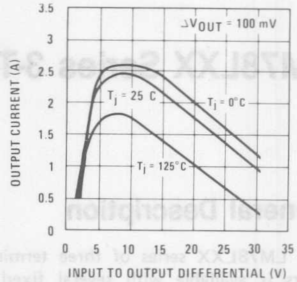
OUTPUT VOLTAGE					5V			12V			15V		
INPUT VOLTAGE (unless otherwise noted)					10V			19V			23V		UNITS
	PARAMETER	CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_O	Output Voltage	$Tj = 25°C$, $5 mA \leq I_O \leq 1A$		4.8	5	5.2	11.5	12	12.5	14.4	15	15.6	V
		$P_D \leq 15W$, $5 mA \leq I_O \leq 1A$		4.75		5.25	11.4		12.6	14.25		15.75	V
		$V_{MIN} \leq V_{IN} \leq V_{MAX}$			$(7 \leq V_{IN} \leq 20)$			$(14.5 \leq V_{IN} \leq 27)$			$(17.5 \leq V_{IN} \leq 30)$		V
ΔV_O	Line Regulation	$I_O = 500 mA$	$Tj = 25°C$		3	50		4	120		4	150	mV
			ΔV_{IN}		$(7 \leq V_{IN} \leq 25)$			$(14.5 \leq V_{IN} \leq 30)$			$(17.5 \leq V_{IN} \leq 30)$		V
			$0°C \leq Tj \leq +125°C$			50			120			150	mV
			ΔV_{IN}		$(8 \leq V_{IN} \leq 20)$			$(15 \leq V_{IN} \leq 27)$			$(18.5 \leq V_{IN} \leq 30)$		V
		$I_O \leq 1A$	$Tj = 25°C$			50			120			150	mV
			ΔV_{IN}		$(7.3 \leq V_{IN} \leq 20)$			$(14.6 \leq V_{IN} \leq 27)$			$(17.7 \leq V_{IN} \leq 30)$		V
			$0° \leq Tj \leq +125°C$			25			60			75	mV
			ΔV_{IN}		$(8 \leq IN \leq 12)$			$(16 \leq V_{IN} \leq 22)$			$(20 \leq V_{IN} \leq 26)$		V
ΔV_O	Load Regulation	$Tj = 25°C$	$5 mA \leq I_O \leq 1.5A$		10	50		12	120		12	150	mV
			$250 mA \leq I_O \leq 750 mA$			25			60			75	mV
		$5 mA \leq I_O \leq 1A$, $0°C \leq Tj \leq +125°C$				50			120			150	mV
I_Q	Quiescent Current	$I_O \leq 1A$	$Tj = 25°C$			8			8			8	mA
			$0°C \leq Tj \leq +125°C$			8.5			8.5			8.5	mA
ΔI_Q	Quiescent Current Change	$5 mA \leq I_O \leq 1A$				0.5			0.5			0.5	mA
		$Tj = 25°C$, $I_O \leq 1A$				1.0			1.0			1.0	mA
		$V_{MIN} \leq V_{IN} \leq V_{MAX}$			$(7.5 \leq V_{IN} \leq 20)$			$(14.8 \leq V_{IN} \leq 27)$			$(17.9 \leq V_{IN} \leq 30)$		V
		$I_O \leq 500 mA$, $0°C \leq Tj \leq +125°C$				1.0			1.0			1.0	mA
		$V_{MIN} \leq V_{IN} \leq V_{MAX}$			$(7 \leq V_{IN} \leq 25)$			$(14.5 \leq V_{IN} \leq 30)$			$(17.5 \leq V_{IN} \leq 30)$		V
V_N	Output Noise Voltage	$T_A = 25°C$, $10 Hz \leq f \leq 100 kHz$			40			75			90		μV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	f = 120 Hz	$I_O \leq 1A$, $Tj = 25°C$ or	62	80		55	72		54	70		dB
			$I_O \leq 500 mA$, $0°C \leq Tj \leq +125°C$	62			55			54			dB
		$V_{MIN} \leq V_{IN} \leq V_{MAX}$			$(8 \leq V_{IN} \leq 18)$			$(15 \leq V_{IN} \leq 25)$			$(18.5 \leq V_{IN} \leq 28.5)$		V
R_O	Dropout Voltage	$Tj = 25°C$, $I_{OUT} = 1A$			2.0			2.0			2.0		V
	Output Resistance	f = 1 kHz			8			18			19		mΩ
	Short-Circuit Current	$Tj = 25°C$			2.1			1.5			1.2		A
	Peak Output Current	$Tj = 25°C$			2.4			2.4			2.4		A
	Average TC of V_{OUT}	$0°C \leq Tj \leq +125°C$, $I_O = 5 mA$			0.6			1.5			1.8		mV/°C
V_{IN}	Input Voltage Required to Maintain Line Regulation	$Tj = 25°C$, $I_O \leq 1A$		7.3			14.6			17.7			V

NOTE 1: Thermal resistance of the TO-3 package (K, KC) is typically 4°C/W junction to case and 35°C/W case to ambient. Thermal resistance of the TO-220 package (T) is typically 4°C/W junction to case and 50°C/W case to ambient.

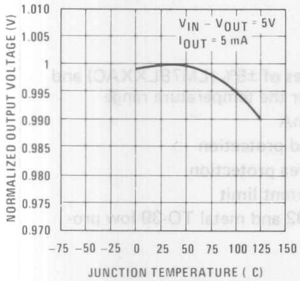
NOTE 2: All characteristics are measured with capacitor across the inut of 0.22 μF, and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_W \leq$ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.



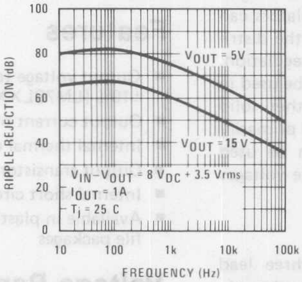




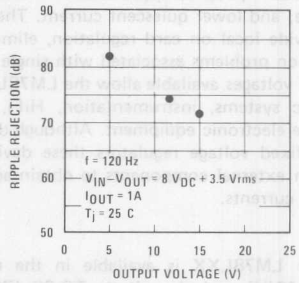
Output Voltage (Normalized to 1V at $T_j = 25°C$)



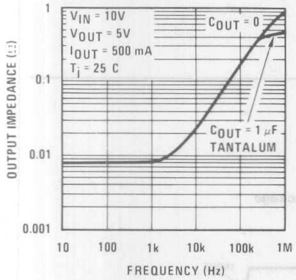
Ripple Rejection



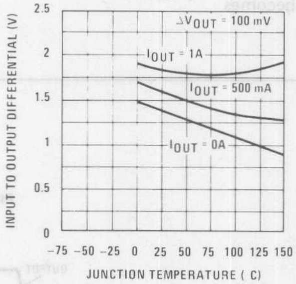
Ripple Rejection



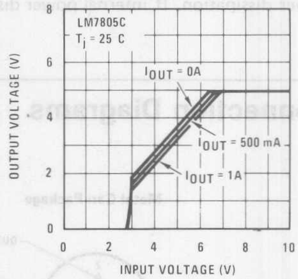
Output Impedance



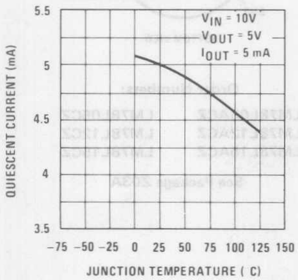
Dropout Voltage



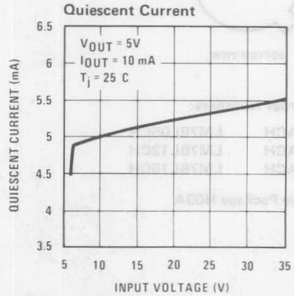
Dropout Characteristics



Quiescent Current



Quiescent Current



National Semiconductor

Voltage Regulators

LM78LXX Series 3-Terminal Positive Regulators

General Description

The LM78LXX series of three terminal positive regulators is available with several fixed output voltages making them useful in a wide range of applications. When used as a zener diode/resistor combination replacement, the LM78LXX usually results in an effective output impedance improvement of two orders of magnitude, and lower quiescent current. These regulators can provide local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow the LM78LXX to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents.

The LM78LXX is available in the metal three lead TO-39(H) and the plastic TO-92 (Z). With adequate heat sinking the regulator can deliver 100 mA output current. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

For output voltage other than 5V, 12V and 15V the LM117 series provides an output voltage range from 1.2V to 57V.

Features

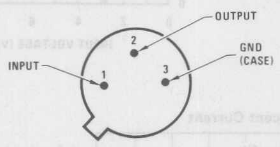
- Output voltage tolerances of ±5% (LM78LXXAC) and ±10% (LM78LXXC) over the temperature range
- Output current of 100 mA
- Internal thermal overload protection
- Output transistor safe area protection
- Internal short circuit current limit
- Available in plastic TO-92 and metal TO-39 low profile packages

Voltage Range

LM78L05	5V
LM78L12	12V
LM78L15	15V

Connection Diagrams

Metal Can Package



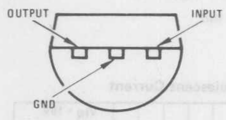
BOTTOM VIEW

Order Numbers:

LM78L05ACH	LM78L05CH
LM78L12ACH	LM78L12CH
LM78L15ACH	LM78L15CH

See Package H03A

Plastic Package



BOTTOM VIEW

Order Numbers:

LM78L05ACZ	LM78L05CZ
LM78L12ACZ	LM78L12CZ
LM78L15ACZ	LM78L15CZ

See Package Z03A

Absolute Maximum Ratings

Input Voltage	
$V_O = 5V$	30V
$V_O = 12V$ to 15V	35V
Internal Power Dissipation (Note 1)	Internally Limited
Operating Temperature Range	0°C to +70°C
Maximum Junction Temperature	125°C
Storage Temperature Range	
Metal Can (H Package)	−65°C to +150°C
Molded TO-92 (Z Package)	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

LM78LXXAC Electrical Characteristics

(Note 2) $T_j = 0°C$ to 125°C, $I_O = 40mA$, $C_{IN} = 0.33\mu F$, $C_O = 0.1\mu F$ (unless noted)

LM78LXXAC OUTPUT VOLTAGE			5V			12V			15V			
INPUT VOLTAGE (unless otherwise noted)			10V			19V			23V			UNITS
	PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_O	Output Voltage	$Tj = 25°C$	4.8	5	5.2	11.5	12	12.5	14.4	15	15.6	V
	(Note 4)	$1 mA \leq I_O \leq 70 mA$	4.75		5.25	11.4		12.6	14.25		15.75	V
		$1 mA \leq I_O \leq 40 mA$ and	4.75		5.25	11.4		12.6	14.25		15.75	V
		$V_{MIN} \leq V_{IN} \leq V_{MAX}$		$(7 \leq V_{IN} \leq 20)$			$(14.5 \leq V_{IN} \leq 27)$			$(17.5 \leq V_{IN} \leq 30)$		V
ΔV_O	Line Regulation	$Tj = 25°C$		10	54		20	110		25	140	mV
				$(8 \leq V_{IN} \leq 20)$			$(16 \leq V_{IN} \leq 27)$			$(20 \leq V_{IN} \leq 30)$		V
				18	75		30	180		37	250	mV
				$(7 \leq V_{IN} \leq 20)$			$(14.5 \leq V_{IN} \leq 27)$			$(17.5 \leq V_{IN} \leq 30)$		V
ΔV_O	Load Regulation	$Tj = 25°C$, $1 mA \leq I_O \leq 40 mA$		5	30		10	50		12	75	mV
		$Tj = 25°C$, $1 mA \leq I_O \leq 100 mA$		20	60		30	100		35	150	mV
ΔV_O	Long Term Stability			12			24			30		mV/1000 hrs
I_Q	Quiescent Current	$Tj = 25°C$		3	5		3	5		3.1	5	mA
		$Tj = 125°C$			4.7			4.7			4.7	
ΔI_Q	Quiescent Current	$1 mA \leq I_O \leq 40 mA$			0.1			0.1			0.1	mA
	Change	$V_{MIN} \leq V_{IN} \leq V_{MAX}$			1.0			1.0			1.0	mA
				$(8 \leq V_{IN} \leq 20)$			$(16 \leq V_{IN} \leq 27)$			$(20 \leq V_{IN} \leq 30)$		V
V_n	Output Noise Voltage	$Tj = 25°C$, (Note 3) f = 10 Hz – 10 kHz		40			80			90		μV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	f = 120 Hz	47	62		40	54		37	51		dB
				$(8 \leq V_{IN} \leq 16)$			$(15 \leq V_{IN} \leq 25)$			$(18.5 \leq V_{IN} \leq 28.5)$		V
	Input Voltage Required to Maintain Line Regulation	$Tj = 25°C$	7			14.5			17.5			V

Note 1: Thermal resistance of the Metal Can Package (H) without a heat sink is 15°C/W junction to case and 140°C/W junction to ambient. Thermal resistance of the TO-92 package is 180°C/W junction to ambient with 0.4" leads from a PC board and 160°C/W junction to ambient with 0.125" lead length to a PC board.

Note 2: The maximum steady state usable output current and input voltage are very dependent on the heat sinking and/or lead length of the package. The data above represent pulse test conditions with junction temperatures as indicated at the initiation of test.

Note 3: Recommended minimum load capacitance of $0.01\mu F$ to limit high frequency noise bandwidth.

Note 4: The temperature coefficient of V_{OUT} is typically within $\pm 0.01\%$ $V_O/°C$.

Absolute Maximum Ratings

Input Voltage	
$V_O = 5V$	30V
$V_O = 12V$ to 15V	35V
Internal Power Dissipation (Note 1)	Internally Limited
Operating Temperature Range	0°C to +70°C
Maximum Junction Temperature	125°C
Storage Temperature Range	
Metal Can (H Package)	−65°C to +150°C
Molded TO-92	−55° to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

LM78LXXC Electrical Characteristics

(Note 2) $T_j = 0°C$ to 125°C, $I_O = 40mA$, $C_{IN} = 0.33\mu F$, $C_O = 0.1\mu F$ (unless noted)

LM78LXXC OUTPUT VOLTAGE			5V			12V			15V			
INPUT VOLTAGE (unless otherwise noted)			10V			19V			23V			**UNITS**
	PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	
V_O	Output Voltage	$T_j = 25°C$	4.6	5	5.4	11.1	12	12.9	13.8	15	16.2	V
	(Note 4)	1 mA ≤ I_O ≤ 70 mA or	4.5		5.5	10.8		13.2	13.5		16.5	V
		1 mA ≤ I_O ≤ 40 mA and ΔV_{IN}		(7 ≤ V_{IN} ≤ 20)			(14.5 ≤ V_{IN} ≤ 27)			(18 ≤ V_{IN} ≤ 30)		V
ΔV_O	Line Regulation	$T_j = 25°C$		10	150		20	200		25	250	mV
				(8 ≤ V_{IN} ≤ 20)			(16 ≤ V_{IN} ≤ 27)			(20 ≤ V_{IN} ≤ 30)		V
				18	200		30	250		30	300	mV
				(7 ≤ V_{IN} ≤ 20)			(14.5 ≤ V_{IN} ≤ 27)			(18 ≤ V_{IN} ≤ 30)		V
ΔV_O	Load Regulation	$T_j = 25°C$, 1 mA ≤ I_O ≤ 40 mA		5	30		10	50		12	75	mV
		$T_j = 25°C$, 1 mA ≤ I_O ≤ 100 mA		20	60		30	100		35	150	mV
ΔV_O	Long Term Stability			12			24			30		mV/1000 hrs
I_Q	Quiescent Current	$T_j = 25°C$		3	6		3	6.5		3.1	6.5	mA
		$T_j = 125°C$			5.5			6			6	
ΔI_Q	Quiescent Current	$T_j = 25°C$, 1 mA ≤ I_O ≤ 40 mA			0.2			0.2			0.2	mA
	Change				1.5			1.5			1.5	mA
		$T_j = 25°C$		(8 ≤ V_{IN} ≤ 20)			(16 ≤ V_{IN} ≤ 27)			(20 ≤ V_{IN} ≤ 30)		V
V_n	Output Noise Voltage	$T_j = 25°C$, (Note 3) f = 10 Hz − 10 kHz		40			80			90		µV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	f = 125 Hz	40	60		36	52		33	49		dB
				(8 ≤ V_{IN} ≤ 18)			(15 ≤ V_{IN} ≤ 25)			(18.5 ≤ V_{IN} ≤ 28.5)		V
	Input Voltage Required to Maintain Line Regulation	$T_j = 25°C$		7			14.5			18		V

Note 1: Thermal resistance of the Metal Can Package (H) without a heat sink is 15°C/W junction to case and 140°C/W junction to ambient. Thermal resistance of the TO-92 package is 180°C/W junction to ambient with 0.4" leads from a PC board and 160°C/W junction to ambient with 0.125" lead length to a PC board.

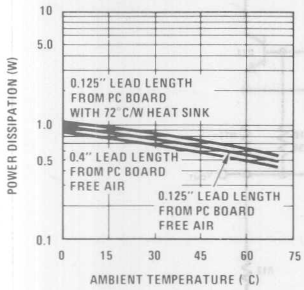
Note 2: The maximum steady state usable output current and input voltage are very dependent on the heat sinking and/or lead length of the package. The data above represent pulse test conditions with junction temperatures as indicated at the initiation of test.

Note 3: Recommended minimum load capacitance of 0.01µF to limit high frequency noise bandwidth.

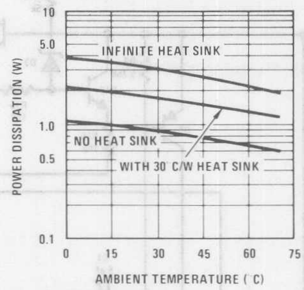
Note 4: The temperature coefficient of V_{OUT} is typically within ±0.01% V_O/°C.

Typical Performance Characteristics

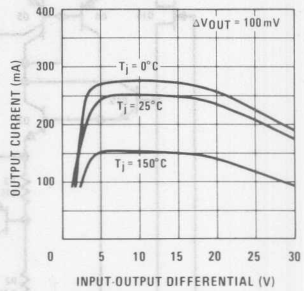
Maximum Average Power Dissipation (Plastic Package)



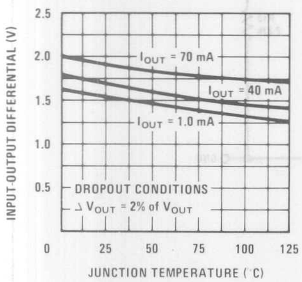
Maximum Average Power Dissipation (Metal Can Package)



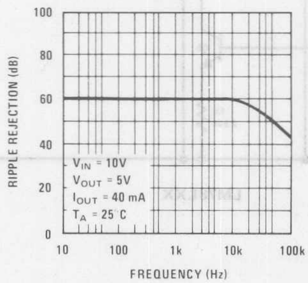
Peak Output Current



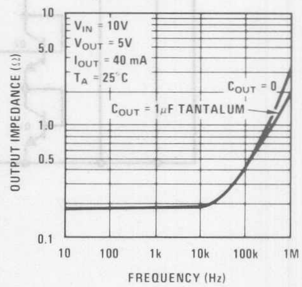
Dropout Voltage



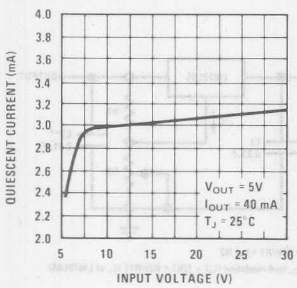
Ripple Rejection



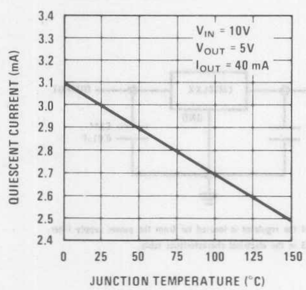
Output Impedance

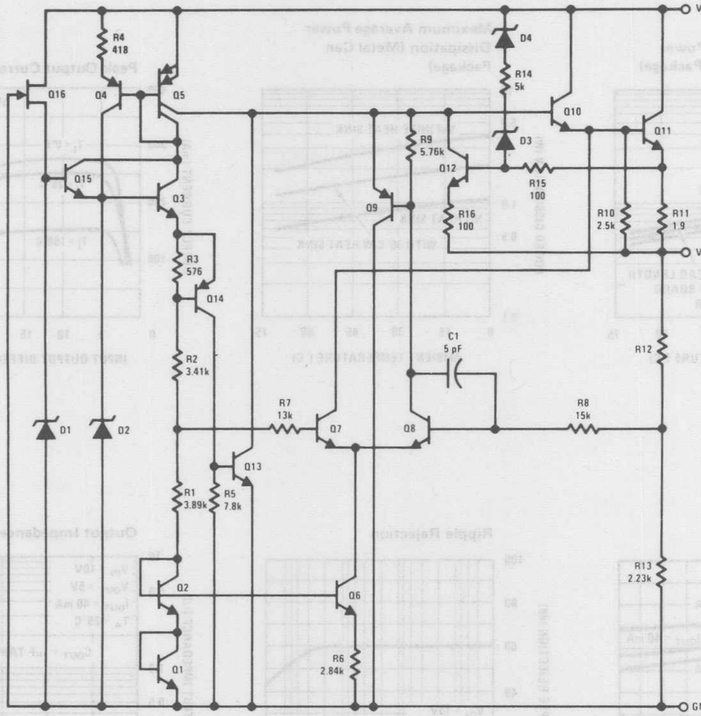


Quiescent Current



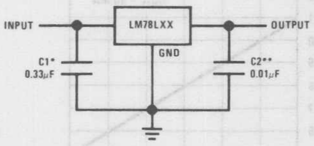
Quiescent Current





LM78LXX

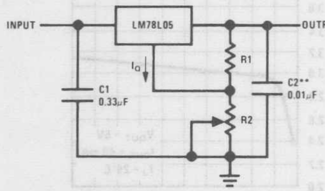
Typical Applications



*Required if the regulator is located far from the power supply filter.

**See Note 3 in the electrical characteristics table.

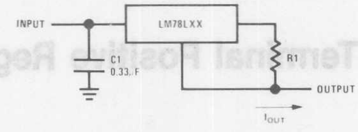
Fixed Output Regulator



$V_{OUT} = 5V + (5V/R1 + I_Q)\ R2$

$5V/R1 > 3\ I_Q$, load regulation $(L_r) \approx [(R1 + R2)/R1]\ (L_r$ of LM78L05)

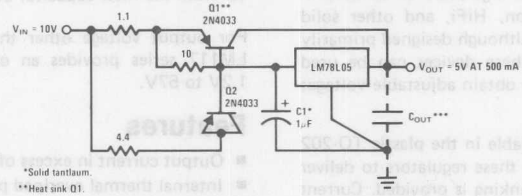
Adjustable Output Regulator



$I_{OUT} = (V_{23}/R1) + I_Q$

$\Delta I_Q = 1.5$ mA over line and load changes

Current Regulator



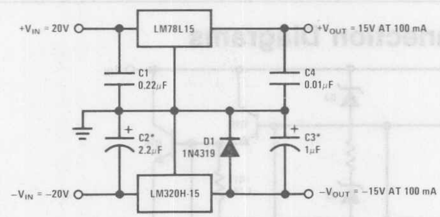
*Solid tantlaum.

**Heat sink Q1.

***Optional: Improves ripple rejection and transient response.

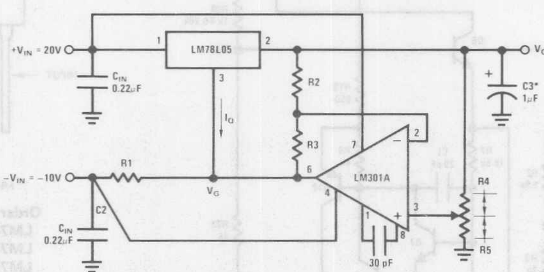
Load Regulation: 0.6% $0 \le I_L \le 250$ mA pulsed with $t_{ON} = 50$ ms.

5V, 500 mA Regulator with Short Circuit Protection



*Solid tantalum.

±15V, 100 mA Dual Power Supply



*Solid tantalum.

$V_{OUT} = V_G + 5V$, $R1 = (-V_{IN}/I_{Q\,LM78L05})$

$V_{OUT} = 5V\,(R2/R4)$ for $(R2 + R3) = (R4 + R5)$

A 0.5V output will correspond to $(R2/R4) = 0.1$, $(R3/R4) = 0.9$

Variable Output Regulator 0.5V – 18V

National Semiconductor

LM78MXX Series 3-Terminal Positive Regulators

General Description

The LM78MXX series of three terminal regulators is available with several fixed output voltages making them useful in a wide range of applications. One of these is local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents.

The LM78MXX series is available in the plastic TO-202 package. This package allows these regulators to deliver over 0.5A if adequate heat sinking is provided. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

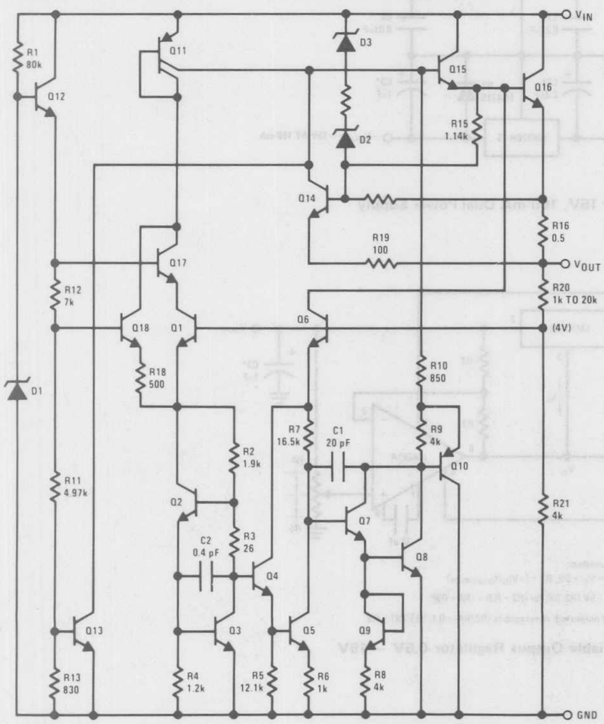
Considerable effort was expended to make the LM78MXX series of regulators easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

For output voltage other than 5V, 12V and 15V the LM117 series provides an output voltage range from 1.2V to 57V.

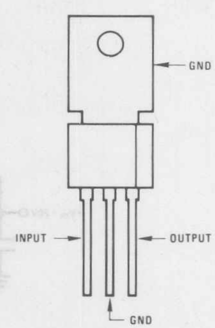
Features

- Output current in excess of 0.5A
- Internal thermal overload protection
- No external components required
- Output transistor safe area protection
- Internal short circuit current limit
- Available in plastic TO-202 package
- Special circuitry allows start-up even if output is pulled to negative voltage (± supplies)

Schematic and Connection Diagrams



Plastic Package



FRONT VIEW

Order Numbers
LM78M05CP
LM78M12CP
LM78M15CP
See Package P03A

For Tab Bend TO-202
Order Numbers
LM78M05CP TB
LM78M12CP TB
LM78M15CP TB
See Package P03E

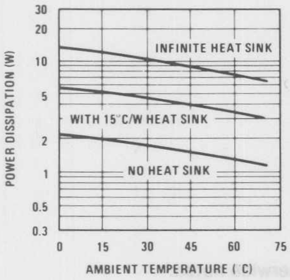
Absolute Maximum Ratings

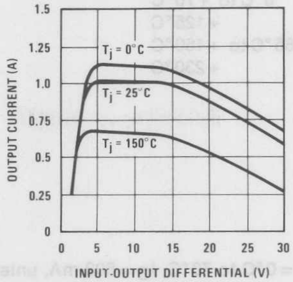
Input Voltage	
($V_O = 5V, 12V, 15V$)	35V
Internal Power Dissipation (Note 1)	Internally Limited
Operating Temperature Range	0°C to +70°C
Maximum Junction Temperature	+125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+230°C

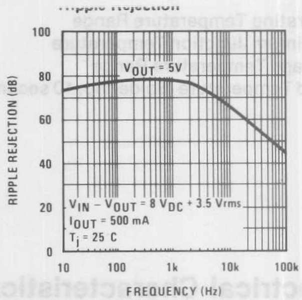
Electrical Characteristics $T_A = 0°C$ to $70°C$, $I_O = 500$ mA, unless otherwise noted.

OUTPUT VOLTAGE			5V			12V			15V			UNITS
INPUT VOLTAGE (unless otherwise noted)			10V			19V			23V			
	PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	
V_O	Output Voltage	$Tj = 25°C$	4.8	5	5.2	11.5	12	12.5	14.4	15	15.6	V
		$P_D \leq 7.5W$, $5\ mA \leq I_O \leq 500\ mA$ and $V_{MIN} \leq V_{IN} \leq V_{MAX}$	4.75 $(7.5 \leq V_{IN} \leq 20)$		5.25	11.4 $(14.8 \leq V_{IN} \leq 27)$		12.6	14.25 $(18 \leq V_{IN} \leq 30)$		15.75	V V
ΔV_O	Line Regulation	$Tj = 25°C$, $I_O = 100$ mA $Tj = 25°C$, $I_O = 500$ mA	$(7.2 \leq V_{IN} \leq 25)$		50 100	$(14.5 \leq V_{IN} \leq 30)$		120 240	$(17.6 \leq V_{IN} \leq 30)$		150 300	mV mV V
ΔV_O	Load Regulation	$Tj = 25°C$, $5\ mA \leq I_O \leq 500\ mA$			100			240			300	mV
ΔV_O	Long Term Stability				20			48			60	mV/1000 hrs
I_Q	Quiescent Current	$Tj = 25°C$		4	10		4	10		4	10	mA
ΔI_Q	Quiescent Current Change	$Tj = 25°C$ $5\ mA \leq I_O \leq 500\ mA$			0.5			0.5			0.5	mA
		$Tj = 25°C$ $V_{MIN} \leq V_{IN} \leq V_{MAX}$	$(7.5 \leq V_{IN} \leq 25)$		1	$(14.8 \leq V_{IN} \leq 30)$		1	$(18 \leq V_{IN} \leq 30)$		1	mA V
V_n	Output Noise Voltage	$Tj = 25°C$, $f = 10\ Hz - 100\ kHz$		40			75			90		µV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	$f = 120$ Hz		78			71			69		V
	Input Voltage Required to Maintain Line Regulation	$Tj = 25°C$, $I_O = 500$ mA	7.2			14.5			17.6			V

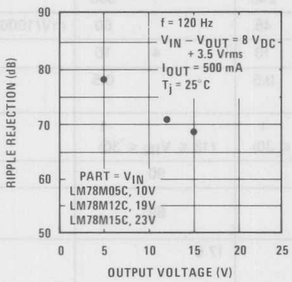
Note 1: Thermal resistance without a heat sink for junction to case temperature is 12°C/W for the TO-202 package. Thermal resistance for case to ambient temperature is 70°C/W for the TO-202 package.



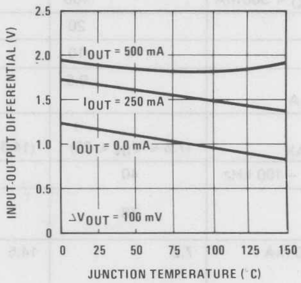




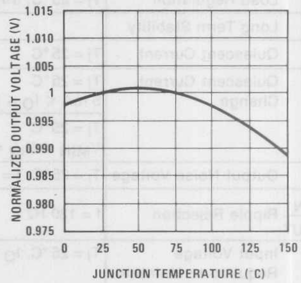
Ripple Rejection



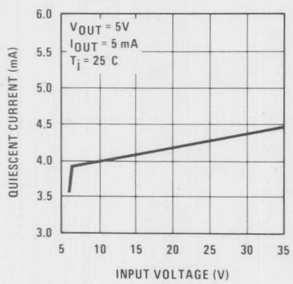
Dropout Voltage



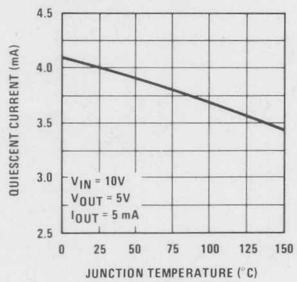
Output Voltage (Normalized to 1V at T_J = 25° C)



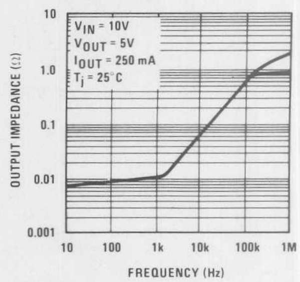
Quiescent Current



Quiescent Current



Output Impedance



National Semiconductor

Voltage Regulators

LM79XX Series 3-Terminal Negative Regulators

General Description

The LM79XX series of 3-terminal regulators is available with fixed output voltages of −5V, −12V, and −15V. These devices need only one external component—a compensation capacitor at the output. The LM79XX series is packaged in the TO-220 power package and is capable of supplying 1.5A of output current.

These regulators employ internal current limiting safe area protection and thermal shutdown for protection against virtually all overload conditions.

Low ground pin current of the LM79XX series allows output voltage to be easily boosted above the preset value with a resistor divider. The low quiescent current drain of these devices with a specified maximum change with line and load ensures good regulation in the voltage boosted mode.

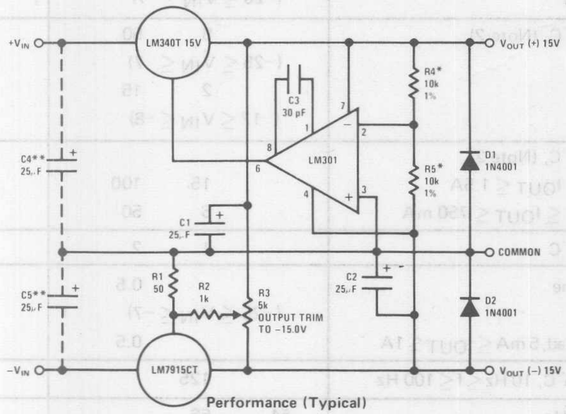
For applications requiring other voltages, see LM137 data sheet.

Features

- Thermal, short circuit and safe area protection
- High ripple rejection
- 1.5A output current
- 4% preset output voltage

Typical Applications

±15V, 1 Amp Tracking Regulators



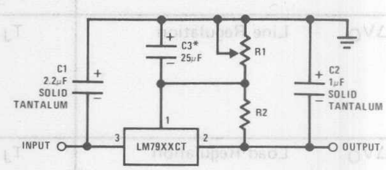
Performance (Typical)

	(−15)	(+15)
Load Regulation at $\Delta I_L = 1A$	40 mV	2 mV
Output Ripple, $C_{IN} = 3000\mu F$, $I_L = 1A$	100μVrms	100μVrms
Temperature Stability	50 mV	50 mV
Output Noise 10 Hz $\leq f \leq$ 10 kHz	150μVrms	150μVrms

*Resistor tolerance of R4 and R5 determine matching of (+) and (−) outputs

**Necessary only if raw supply filter capacitors are more than 3" from regulators

Variable Output



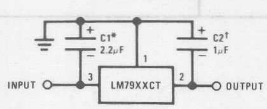
*Improves transient response and ripple rejection. Do not increase beyond 50μF.

$$V_{OUT} = V_{SET}\left(\frac{R1 + R2}{R2}\right)$$

Select R2 as follows

LM7905CT	300Ω
LM7912CT	750Ω
LM7915CT	1k

Fixed Regulator

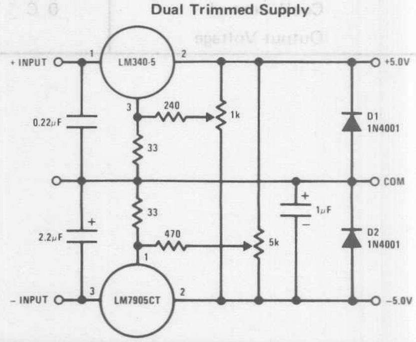


*Required if regulator is separated from filter capacitor by more than 3". For value given, capacitor must be solid tantalum. 25μF aluminum electrolytic may be substituted.

†Required for stability. For value given, capacitor must be solid tantalum. 25μF aluminum electrolytic may be substituted. Values given may be increased without limit.

For output capacitance in excess of 100μF, a high current diode from input to output (1N4001, etc.) will protect the regulator from momentary input shorts.

Dual Trimmed Supply



Absolute Maximum Ratings

Input Voltage	
(V_O = 5V)	−35V
(V_O = 12V and 15V)	−40V
Input-Output Differential	
(V_O = 5V)	25V
(V_O = 12V and 15V)	30V
Power Dissipation	Internally Limited
Operating Junction Temperature Range	0°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	230°C

Electrical Characteristics

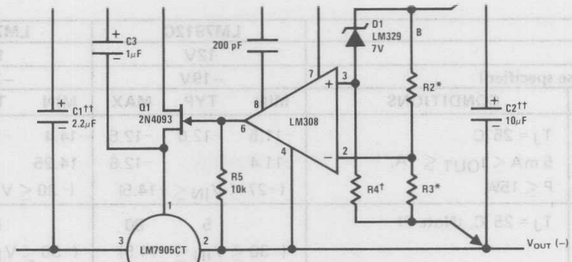
Conditions unless otherwise noted: I_{OUT} = 500 mA, C_{IN} = 2.2μF, C_{OUT} = 1μF, 0°C ≤ T_J ≤ +125°C, Power Dissipation ≤ 15W.

PART NUMBER			LM7905C			UNITS
OUTPUT VOLTAGE			5V			
INPUT VOLTAGE (unless otherwise specified)			−10V			
PARAMETER		CONDITIONS	MIN	TYP	MAX	
V_O	Output Voltage	T_J = 25°C	−4.8	−5.0	−5.2	V
		5 mA ≤ I_{OUT} ≤ 1A, P ≤ 15W	−4.75		−5.25	V
			(−20 ≤ V_{IN} ≤ −7)			V
ΔV_O	Line Regulation	T_J = 25°C, (Note 2)		8	50	mV
			(−25 ≤ V_{IN} ≤ −7)			V
				2	15	mV
			(−12 ≤ V_{IN} ≤ −8)			V
ΔV_O	Load Regulation	T_J = 25°C, (Note 2)				mV
		5 mA ≤ I_{OUT} ≤ 1.5A		15	100	mV
		250 mA ≤ I_{OUT} ≤ 750 mA		5	50	mV
I_Q	Quiescent Current	T_J = 25°C		1	2	mA
ΔI_Q	Quiescent Current Change	With Line			0.5	mA
			(−25 ≤ V_{IN} ≤ −7)			V
		With Load, 5 mA ≤ I_{OUT} ≤ 1A			0.5	mA
V_n	Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 Hz		125		μV
	Ripple Rejection	f = 120 Hz	54	66		dB
			(−18 ≤ V_{IN} ≤ −8)			V
	Dropout Voltage	T_J = 25°C, I_{OUT} = 1A		1.1		V
I_{OMAX}	Peak Output Current	T_J = 25°C		2.2		A
	Average Temperature Coefficient of Output Voltage	I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 100°C		0.4		mV/°C

			LM7912C			LM7915C			
OUTPUT VOLTAGE			12V			15V			UNITS
INPUT VOLTAGE (unless otherwise specified)			−19V			−23V			
	PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	
V_O	Output Voltage	$T_J = 25°C$	−11.5	−12.0	−12.5	−14.4	−15.0	−15.6	V
		$5\ mA \leq I_{OUT} \leq 1A$,	−11.4		−12.6	−14.25		−15.75	V
		$P \leq 15W$	$(-27 \leq V_{IN} \leq -14.5)$			$(-30 \leq V_{IN} \leq -17.5)$			V
ΔV_O	Line Regulation	$T_J = 25°C$, (Note 2)		5	80		5	100	mV
			$(-30 \leq V_{IN} \leq -14.5)$			$(-30 \leq V_{IN} \leq -17.5)$			V
				3	30		3	50	mV
			$(-22 \leq V_{IN} \leq -16)$			$(-26 \leq V_{IN} \leq -20)$			V
ΔV_O	Load Regulation	$T_J = 25°C$, (Note 2)		15	200		15	200	mV
		$5\ mA \leq I_{OUT} \leq 1.5A$		15	200		15	200	mV
		$250\ mA \leq I_{OUT} \leq 750\ mA$		5	75		5	75	mV
I_Q	Quiescent Current	$T_J = 25°C$		1.5	3		1.5	3	mA
ΔI_Q	Quiescent Current Change	With Line			0.5			0.5	mA
			$(-30 \leq V_{IN} \leq -14.5)$			$(-30 \leq V_{IN} \leq -17.5)$			V
		With Load, $5\ mA \leq I_{OUT} \leq 1A$			0.5			0.5	mA
V_n	Output Noise Voltage	$T_A = 25°C$, $10\ Hz \leq f \leq 100\ Hz$		300			375		μV
	Ripple Rejection	f = 120 Hz	54	70		54	70		dB
			$(-25 \leq V_{IN} \leq -15)$			$(-30 \leq V_{IN} \leq -17.5)$			V
	Dropout Voltage	$T_J = 25°C$, $I_{OUT} = 1A$		1.1			1.1		V
I_{OMAX}	Peak Output Current	$T_J = 25°C$		2.2			2.2		A
	Average Temperature Coefficient of Output Voltage	$I_{OUT} = 5\ mA$, $0°C \leq T_J \leq 100°C$		−0.8			−1.0		mV/°C

Note 1: For calculations of junction temperature rise due to power dissipation, thermal resistance junction to ambient (θ_{JA}) is 50°C/W (no heat sink) and 5°C/W (infinite heat sink).

Note 2: Regulation is measured at a constant junction temperature by pulse testing with a low duty cycle. Changes in output voltage due to heating effects must be taken into account.



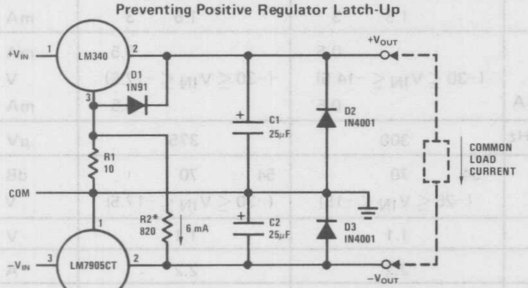
Load and line regulation < 0.01% temperature stability ≤ 0.2%

† Determines Zener current

†† Solid tantalum

* Select resistors to set output voltage. 2 ppm/°C tracking suggested

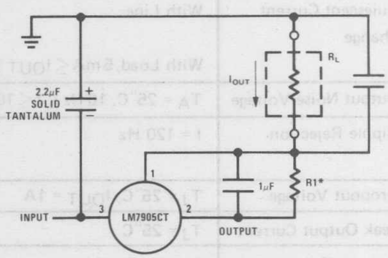
Preventing Positive Regulator Latch-Up



R1 and D1 allow the positive regulator to "start-up" when $+V_{IN}$ is delayed relative to $-V_{IN}$ and a heavy load is drawn between the outputs. Without R1 and D1, most three-terminal regulators will not start with heavy (0.1A–1A) load current flowing to the negative regulator, even though the positive output is clamped by D2.

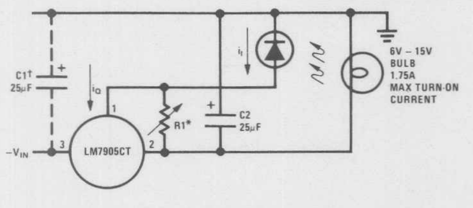
* R2 is optional. Ground pin current from the positive regulator flowing through R1 will increase $+V_{OUT} \approx 60$ mV if R2 is omitted.

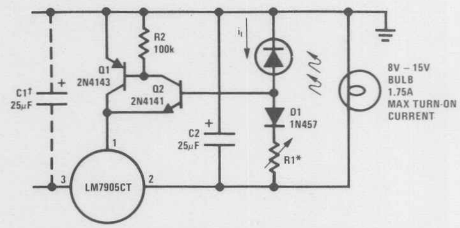
Current Source



$$*I_{OUT} = 1\text{ mA} + \frac{5V}{R1}$$

Light Controllers Using Silicon Photo Cells





* Lamp brightness increases until $i_l = i_Q$ (≈ 1 mA) + 5V/R1.

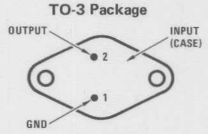
† Necessary only if raw supply filter capacitor is more than 2" from LM7905CT

* Lamp brightness increases until i_l = 5V/R1 (i_l can be set as low as 1µA)

† Necessary only if raw supply filter capacitor is more than 2" from LM7905CT

Connection Diagrams

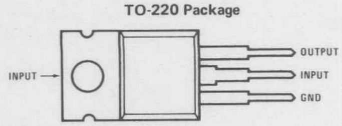
TO-3 Package



BOTTOM VIEW

Order Numbers:
LM7905CK
LM7912CK
LM7915CK
See NS Package KC02A

TO-220 Package

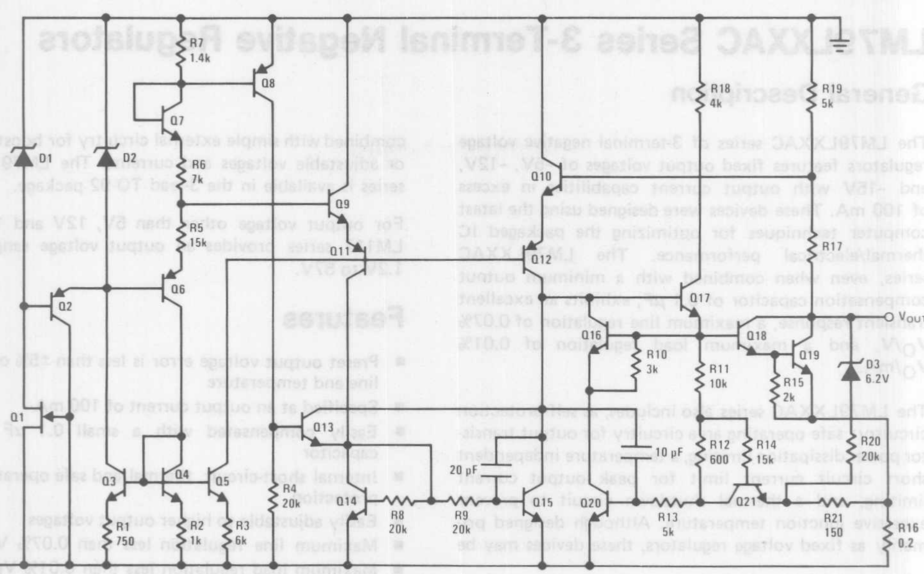


TOP VIEW

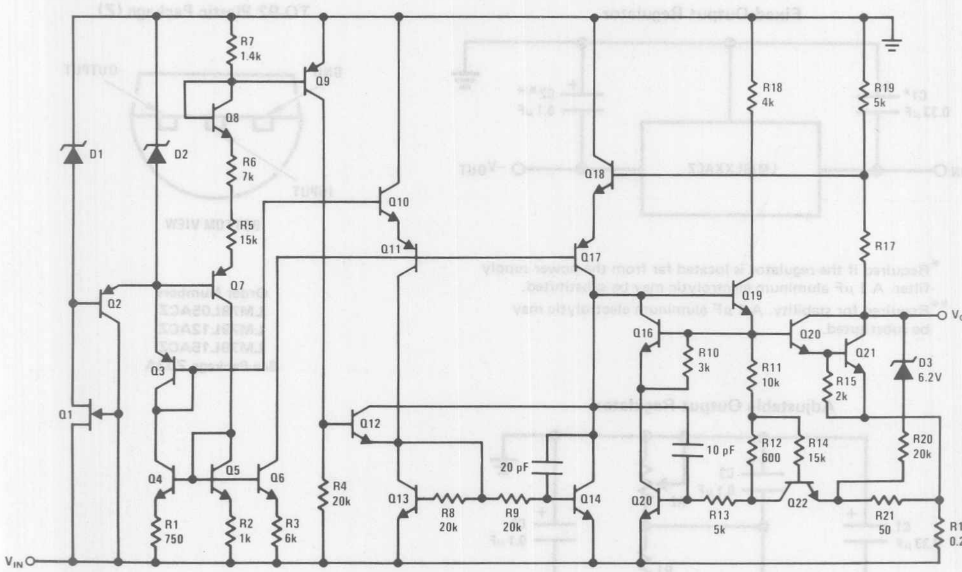
Order Numbers:
LM7905CT
LM7912CT
LM7915CT
See NS Package T03B

Schematic Diagrams

−5V



−12V and −15V



National Semiconductor

Voltage Regulators

LM79LXXAC Series 3-Terminal Negative Regulators

General Description

The LM79LXXAC series of 3-terminal negative voltage regulators features fixed output voltages of -5V, -12V, and -15V with output current capabilities in excess of 100 mA. These devices were designed using the latest computer techniques for optimizing the packaged IC thermal/electrical performance. The LM79LXXAC series, even when combined with a minimum output compensation capacitor of 0.1 μF, exhibits an excellent transient response, a maximum line regulation of 0.07% V_O/V, and a maximum load regulation of 0.01% V_O/mA.

The LM79LXXAC series also includes, as self-protection circuitry: safe operating area circuitry for output transistor power dissipation limiting, a temperature independent short circuit current limit for peak output current limiting, and a thermal shutdown circuit to prevent excessive junction temperature. Although designed primarily as fixed voltage regulators, these devices may be combined with simple external circuitry for boosted and/or adjustable voltages and currents. The LM79LXXAC series is available in the 3-lead TO-92 package.

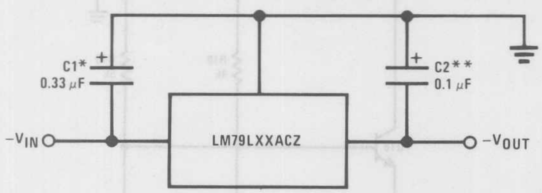
For output voltage other than 5V, 12V and 15V the LM117 series provides an output voltage range from 1.2V to 57V.

Features

- Preset output voltage error is less than ±5% overload, line and temperature
- Specified at an output current of 100 mA
- Easily compensated with a small 0.1 μF output capacitor
- Internal short-circuit, thermal and safe operating area protection
- Easily adjustable to higher output voltages
- Maximum line regulation less than 0.07% V_{OUT}/V
- Maximum load regulation less than 0.01% V_{OUT}mA
- TO-92 package

Typical Applications

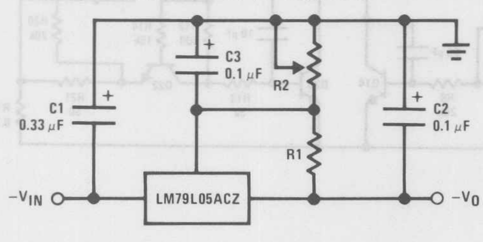
Fixed Output Regulator



*Required if the regulator is located far from the power supply filter. A 1 μF aluminum electrolytic may be substituted.

**Required for stability. A 1 μF aluminum electrolytic may be substituted.

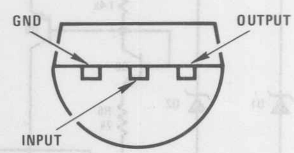
Adjustable Output Regulator



$-V_O = -5V - (5V/R1 + I_Q) \cdot R2,$
$5V/R1 > 3\, I_Q$

Connection Diagram

TO-92 Plastic Package (Z)



BOTTOM VIEW

Order Numbers
LM79L05ACZ
LM79L12ACZ
LM79L15ACZ
See Package Z03A

Absolute Maximum Ratings

Input Voltage	
$V_O = -5V, -12V, -15V$	$-35V$
Internal Power Dissipation (Note 1)	Internally Limited
Operating Temperature Range	0 °C to +70 °C
Maximum Junction Temperature	+125 °C
Storage Temperature Range	−55 °C to +150 °C
Lead Temperature (Soldering, 10 seconds)	300 °C

Electrical Characteristics

(Note 2) $T_A = 0°C$ to $+70°$ unless otherwise noted.

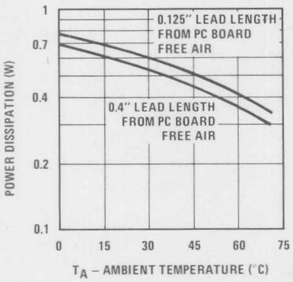
OUTPUT VOLTAGE			−5V			−12V			−15V			UNITS
INPUT VOLTAGE (unless otherwise noted)			−10V			−17V			−20V			
	PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_O	Output Voltage	$T_j = 25°C$, $I_O = 100$ mA	−5.2	−5	−4.8	−12.5	−12	−11.5	−15.6	−15	−14.4	
		1 mA $\leq I_O \leq$ 100 mA	−5.25		−4.75	−12.6		−11.4	−15.75		−14.25	
		$V_{MIN} \leq V_{IN} \leq V_{MAX}$	$(-20 \leq V_{IN} \leq -7.5)$			$(-27 \leq V_{IN} \leq -14.8)$			$(-30 \leq V_{IN} \leq -18)$			V
		1 mA $\leq I_O \leq$ 40 mA	−5.25		−4.75	−12.6		−11.4	−15.75		−14.25	
		$V_{MIN} \leq V_{IN} \leq V_{MAX}$	$(-20 \leq V_{IN} \leq -7)$			$(-27 \leq V_{IN} \leq -14.5)$			$(-30 \leq V_{IN} \leq -17.5)$			
ΔV_O	Line Regulation	$T_j = 25°C$, $I_O = 100$ mA			60			45			45	mV
		$V_{MIN} \leq V_{IN} \leq V_{MAX}$	$(-20 \leq V_{IN} \leq -7.3)$			$(-27 \leq V_{IN} \leq -14.6)$			$(-30 \leq V_{IN} \leq -17.7)$			V
		$T_j = 25°C$, $I_O = 40$ mA			60			45			45	mV
		$V_{MIN} \leq V_{IN} \leq V_{MAX}$	$(-20 \leq V_{IN} \leq -7)$			$(-27 \leq V_{IN} \leq -14.5)$			$(-30 \leq V_{IN} \leq -17.5)$			V
Δ	Load Regulation	$T_j = 25°C$, 1 mA $\leq I_O \leq$ 100 mA			50			100			125	mV
ΔV_O	Long Term Stability	$I_O = 100$ mA		20			48			60		mV/khrs
I_Q	Quiescent Current	$I_O = 100$ mA		2	6		2	6		2	6	mA
ΔI_Q	Quiescent Current Change	1 mA $\leq I_O \leq$ 100 mA			0.3			0.3			0.3	mA
		1 mA $\leq I_O \leq$ 40 mA			0.1			0.1			0.1	
		$I_O = 100$ mA			0.25			0.25			0.25	mA
		$V_{MIN} \leq V_{IN} \leq V_{MAX}$	$(-20 \leq V_{IN} \leq -7.5)$			$(-27 \leq V_{IN} \leq -14.8)$			$(-30 \leq V_{IN} \leq -18)$			V
V_n	Output Noise Voltage	$T_j = 25°C$, $I_O = 100$ mA, f = 10 Hz – 10 kHz		40			96			120		µV
$\frac{\Delta V_{IN}}{\Delta V_O}$	Ripple Rejection	$T_j = 25°C$, $I_O = 100$ mA, f = 120 Hz	50			52			50			dB
	Input Voltage Required to Maintain Line Regulation	$T_j = 25°C$										
		$I_O = 100$ mA			−7.3			−14.6			−17.7	V
		$I_O = 40$ mA			−7.0			−14.5			−17.5	

Note 1: Thermal resistance, junction to ambient, of the TO-92 (Z) package is 180 °C/W when mounted with 0.40 inch leads on a PC board, and 160 °C/W when mounted with 0.25 inch leads on a PC board.

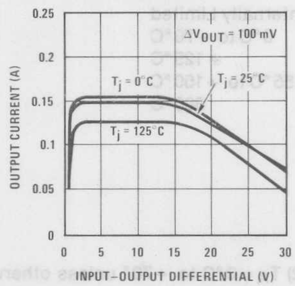
Note 2: To ensure constant junction temperature, low duty cycle pulse testing is used.

Typical Performance Characteristics

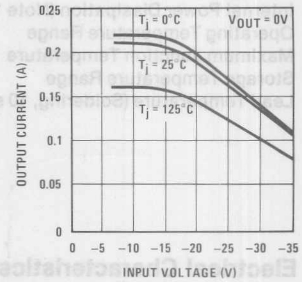
Maximum Average Power Dissipation (TO-92)



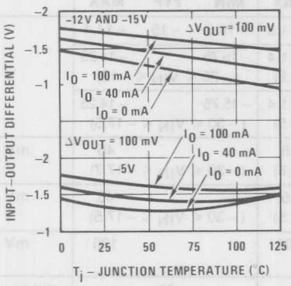
Peak Output Current



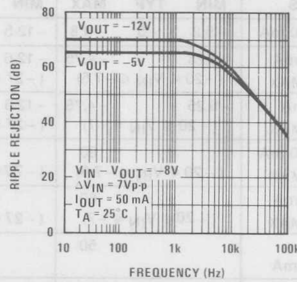
Short Circuit Output Current



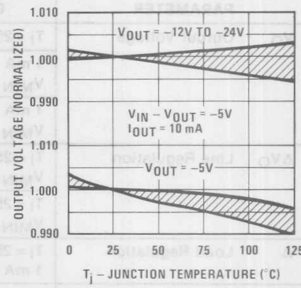
Dropout Voltage



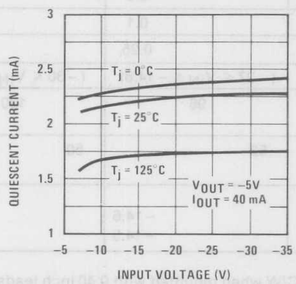
Ripple Rejection



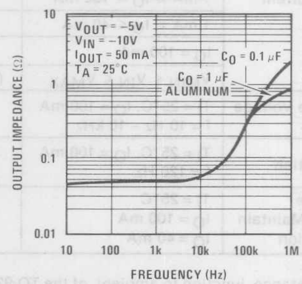
Output Voltage vs. Temperature (Normalized to 1V @ 25°C)



Quiescent Current

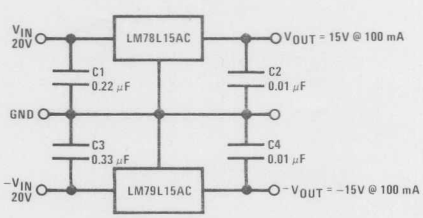


Output Impedance



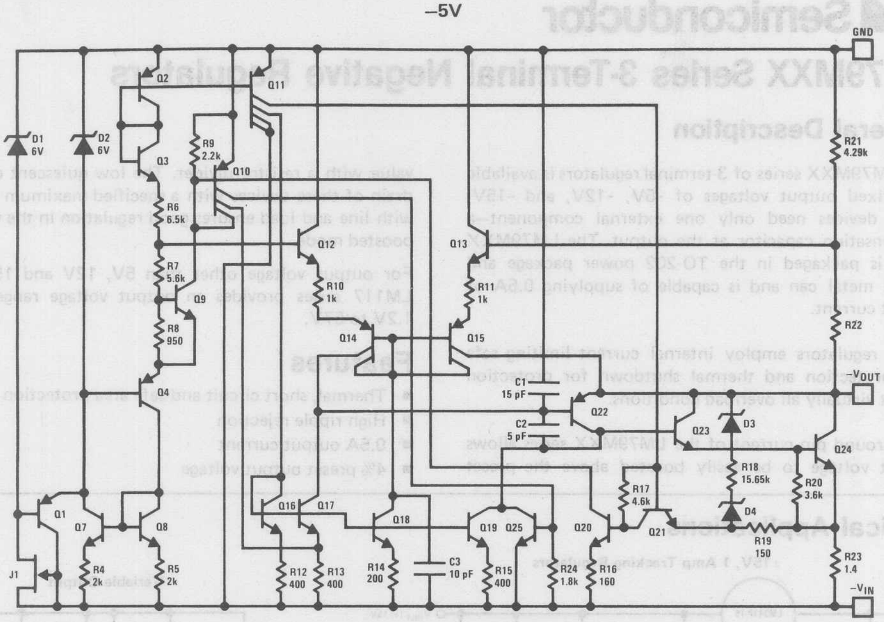
Typical Applications (Continued)

±15V, 100 mA Dual Power Supply

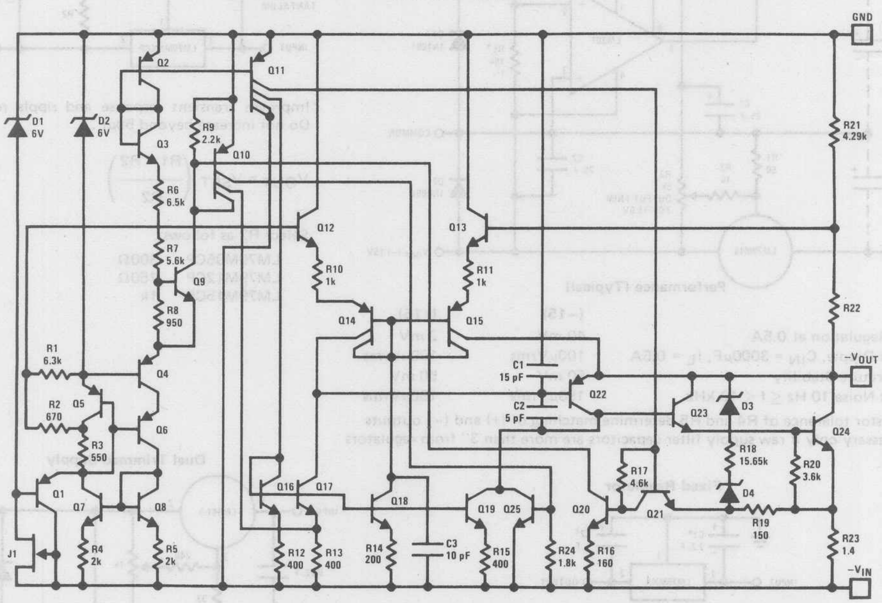


Schematic Diagrams

-5V



-12V and -15V



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National Semiconductor

Voltage Regulators

LM79MXX Series 3-Terminal Negative Regulators

General Description

The LM79MXX series of 3-terminal regulators is available with fixed output voltages of -5V, -12V, and -15V. These devices need only one external component—a compensation capacitor at the output. The LM79MXX series is packaged in the TO-202 power package and TO-39 metal can and is capable of supplying 0.5A of output current.

These regulators employ internal current limiting safe area protection and thermal shutdown for protection against virtually all overload conditions.

Low ground pin current of the LM79MXX series allows output voltage to be easily boosted above the preset value with a resistor divider. The low quiescent current drain of these devices with a specified maximum change with line and load ensures good regulation in the voltage boosted mode.

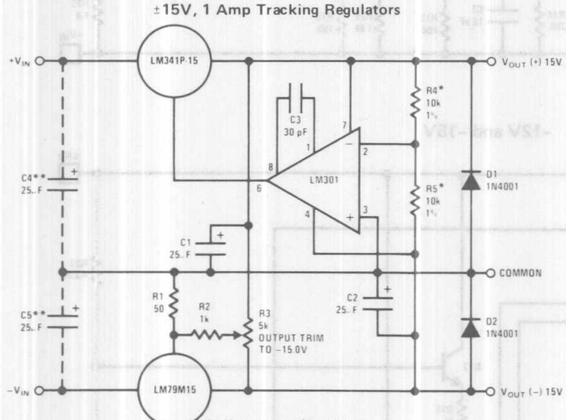
For output voltage other than 5V, 12V and 15V the LM117 series provides an output voltage range from 1.2V to 57V.

Features

- Thermal, short circuit and safe area protection
- High ripple rejection
- 0.5A output current
- 4% preset output voltage

Typical Applications

±15V, 1 Amp Tracking Regulators



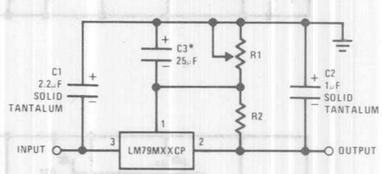
Performance (Typical)

	(−15)	(+15)
Load Regulation at 0.5A	40 mV	2 mV
Output Ripple, C_{IN} = 3000μF, I_L = 0.5A	100μVrms	100μVrms
Temperature Stability	50 mV	50 mV
Output Noise 10 Hz ≤ f ≤ 10 kHz	150μVrms	150μVrms

*Resistor tolerance of R4 and R5 determine matching of (+) and (−) outputs

**Necessary only if raw supply filter capacitors are more than 3" from regulators

Variable Output



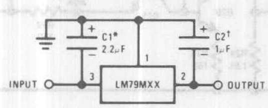
*Improves transient response and ripple rejection. Do not increase beyond 50μF.

$$V_{OUT} = V_{SET}\left(\frac{R1 + R2}{R2}\right)$$

Select R2 as follows:

LM79M05CP	300Ω
LM79M12CP	750Ω
LM79M15CP	1k

Fixed Regulator

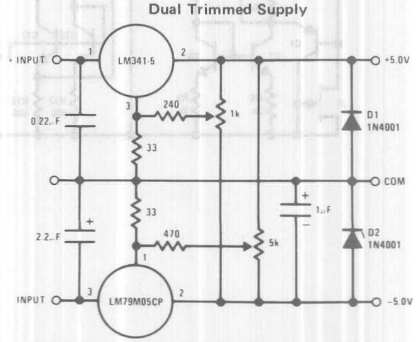


*Required if regulator is separated from filter capacitor by more than 3". For value given, capacitor must be solid tantalum. 25μF aluminum electrolytic may be substituted.

†Required for stability. For value given, capacitor must be solid tantalum. 25μF aluminum electrolytic may be substituted. Values given may be increased without limit.

For output capacitance in excess of 100μF, a high current diode from input to output (1N4001, etc.) will protect the regulator from momentary input shorts.

Dual Trimmed Supply



Absolute Maximum Ratings

Input Voltage	
($V_O = 5V$)	25V
($V_O = 12V$ and 15V)	−35V
Input/Output Differential	
($V_O = 5V$)	25V
($V_O = 12V$ and 15V)	30V
Power Dissipation	Internally Limited
Operating Junction Temperature Range	0°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	230°C

Electrical Characteristics

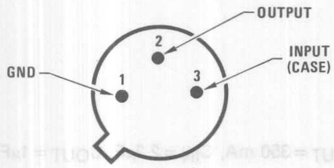
Conditions unless otherwise noted: $I_{OUT} = 350$ mA, $C_{IN} = 2.2\mu F$, $C_{OUT} = 1\mu F$, $0°C \leq T_j \leq +125°C$

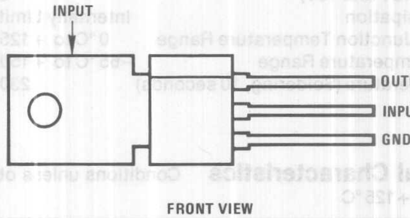
PART NUMBER			LM79M05C			LM79M12C			LM79M15C			UNITS
OUTPUT VOLTAGE			−5V			−12V			−15V			
INPUT VOLTAGE (unless otherwise specified)			−10V			−19V			−23V			
	PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_O	Output Voltage	$T_j = 25°C$	−4.8	−5.0	−5.2	−11.5	−12.0	−12.5	−14.4	−15.0	−15.6	V
		$5 mA \leq I_{OUT} \leq 350 mA$	−4.75		−5.25	−11.4		−12.6	−14.25		−15.75	V
				$(-25 \leq V_{IN} \leq -7)$			$(-27 \leq V_{IN} \leq -14.5)$			$(-30 \leq V_{IN} \leq -17.5)$		V
ΔV_O	Line Regulation	$T_j = 25°C$, (Note 2)		8	50		5	80		5	80	mV
				$(-25 \leq V_{IN} \leq -7)$			$(-30 \leq V_{IN} \leq -14.5)$			$(- \leq V_{IN} \leq -17.5)$		V
				2	30		3	30		3	50	mV
				$(-18 \leq V_{IN} \leq -8)$			$(-25 \leq V_{IN} \leq -15)$			$(-28 \leq V_{IN} \leq -18)$		V
ΔV_O	Load Regulation	$T_j = 25°C$, (Note 2) $5 mA \leq I_{OUT} \leq 0.5A$		30	100		30	240		30	240	mV
I_Q	Quiescent Current	$T_j = 25°C$		1	2		1.5	3		1.5	3	mA
ΔI_Q	Quiescent Current Change	With Line			0.4			0.4			0.4	mA
				$(-25 \leq V_{IN} \leq -8)$			$(-30 \leq V_{IN} \leq -14.5)$			$(-30 \leq V_{IN} \leq -27)$		V
		With Load, $5 mA \leq I_{OUT} \leq 350 mA$			0.4			0.4			0.4	mA
V_n	Output Noise Voltage	$T_A = 25°C$, $10 Hz \leq f \leq 100 Hz$		750			400			400		μV
	Ripple Rejection	f = 120 Hz	54	66		54	70		54	70		dB
				$(-18 \leq V_{IN} \leq -8)$			$(-25 \leq V_{IN} \leq -15)$			$(-30 \leq V_{IN} \leq -17.5)$		V
	Dropout Voltage	$T_j = 25°C$, $I_{OUT} = 0.5A$		1.1			1.1			1.1		V
I_{OMAX}	Peak Output Current	$T_j = 25°C$		800			800			800		A
	Average Temperature Coefficient of Output Voltage	$I_{OUT} = 5 mA$, $0°C \leq T_j \leq 100°C$		0.4			−0.8			−1.0		mV/°C

Note 1: For calculations of junction temperature rise due to power dissipation, thermal resistance junction to ambient (θ_{JA}) is 70°C/W (no heat sink) and 12°C/W (infinite heat sink).

Note 2: Regulation is measured at a constant junction temperature by pulse testing with a low duty cycle. Changes in output voltage due to heating effects must be taken into account.

Connection Diagrams





Metal Can Package TO-39 (H)
Order Number:
LM79M05CH
LM79M12CH
LM79M15CH

See Package H03A

Power Package TO-202 (P)
Order Number:
LM79M05CP
LM79M12CP
LM79M15CP

See Package P03A

For Tab Bend TO-202
Order Number:
LM79M05CP TB
LM79M12CP TB
LM79M15CP TB
See Package P03E

Section 2

Voltage References

2

Section Contents

Reverse Breakdown Voltage V_R at I_R	Device	Voltage Tolerance Max, $T_A = 25°C$	Voltage Temperature Drift-ppm/°C Max or mV Max Change Over Temperature Range		Current Range, I_R	Output Dynamic Impedance (Max)
			Drift (Max)	Temperature Range		
1.22	LM113	±5%	100 ppm typ	−55°C to +125°C	500 μA to 20 mA	0.8Ω
1.22	LM313	±5%	100 ppm typ	0°C to 70°C	500 μA to 20 mA	0.8Ω
1.22	LM113-1	±1%	50 ppm typ	−55°C to +125°C	500 μA to 20 mA	0.8Ω
1.22	LM113-2	±2%	50 ppm typ	−55°C to +125°C	500 μA to 20 mA	0.8Ω
1.235	LM185	±1%	20 ppm typ	−55°C to +125°C	1 mA to 20 mA	0.6Ω
1.235	LM285	±1%	20 ppm typ	−25°C to +85°C	1 mA to 20 mA	0.6Ω
1.235	LM385B	±1%	20 ppm typ	0°C to +70°C	1 mA to 20 mA	1Ω
1.235	LM385	−2.5, +2	20 ppm typ	0°C to +70°C	1 mA to 20 mA	1Ω
2.49	LM136	±2%	18 mV	−55°C to +125°C	400 μA to 10 mA	0.6Ω
2.49	LM136A	±1%	18 mV	−55°C to +125°C	400 μA to 10 mA	0.6Ω
2.49	LM236	±2%	9 mV	−25°C to +85°C	400 μA to 10 mA	0.6Ω
2.49	LM236A	±1%	9 mV	−25°C to +85°C	400 μA to 10 mA	0.6Ω
2.49	LM336	±4%	6 mV	0°C to +70°C	400 μA to 10 mA	1Ω
2.49	LM336B	±2%	6 mV	0°C to +70°C	400 μA to 10 mA	1Ω
2.5	LM185-2.5	±1.5%	20 ppm typ	−55°C to +125°C	20 μA to 20 mA	0.6Ω
2.5	LM285-2.5	±1.5%	20 ppm typ	−25°C to +85°C	20 μA to 20 mA	0.6Ω
2.5	LM385-2.5	±3%	20 ppm typ	0°C to +70°C	20 μA to 20 mA	1Ω
2.5	LM385B-2.5	±1.5%	20 ppm typ	0°C to +70°C	20 μA to 20 mA	1Ω
5.0	LM136-5.0	±2%	36 mV	−55°C to +125°C	400 μA to 10 mA	0.6Ω
5.0	LM136A-5.0	±1%	36 mV	−55°C to +125°C	400 μA to 10 mA	0.6Ω
5.0	LM236-5.0	±2%	18 mV	−25°C to +85°C	400 μA to 10 mA	0.6Ω
5.0	LM236A-5.0	±1%	18 mV	−25°C to +85°C	400 μA to 10 mA	0.6Ω
5.0	LM336-5.0	±4%	12 mV	0°C to +70°C	400 μA to 10 mA	1Ω
5.0	LM336B-5.0	±2%	12 mV	0°C to +70°C	400 μA to 10 mA	1Ω
6.90	LM129A	+3%, −2%	10 ppm	−55°C to +125°C	0.6 mA to 15 mA	1Ω
6.90	LM129B	+3%, −2%	20 ppm	−55°C to +125°C	0.6 mA to 15 mA	1Ω
6.90	LM129C	+3%, −2%	50 ppm	−55°C to +125°C	0.6 mA to 15 mA	1Ω
6.90	LM329B	±5%	50 ppm	0°C to +70°C	0.6 mA to 15 mA	2Ω
6.90	LM329C	±5%	20 ppm	0°C to +70°C	0.6 mA to 15 mA	2Ω
6.90	LM329D	±5%	100 ppm	0°C to +70°C	0.6 mA to 15 mA	2Ω
6.95	LM199A	+1%, −2%	0.5 ppm	−55°C to +125°C	0.5 mA to 10 mA	1Ω
6.95	LM199A	+1%, −2%	10 ppm	85°C to +125°C	0.5 mA to 10 mA	1Ω
6.95	LM199	+1%, −2%	1 ppm	−55°C to +85°C	0.5 mA to 10 mA	1Ω
6.95	LM199	+1%, −2%	15 ppm	85°C to +125°C	0.5 mA to 10 mA	1Ω
6.95	LM299A	+1%, −2%	0.5 ppm	−25°C to +85°C	0.5 mA to 10 mA	1Ω
6.95	LM299	+1%, −2%	1 ppm	−25°C to +85°C	0.5 mA to 10 mA	1Ω
6.95	LM399A	±5%	1 ppm	0°C to +70°C	0.5 mA to 10 mA	1.5Ω
6.95	LM399	±5%	2 ppm	0°C to +70°C	0.5 mA to 10 mA	1.5Ω
6.95	LM3999	±5%	5 ppm	0°C to +70°C	0.6 mA to 10 mA	2.2Ω
10.00	LH0070-0	0.1%	20 mV	−25°C to +85°C	0 mA to 20 mA	1Ω
10.00	LH0070-1	0.1%	10 mV	−25°C to +85°C	0 mA to 20 mA	1Ω
10.00	LH0070-2	0.05%	4 mV	−25°C to +85°C	0 mA to 20 mA	1Ω
10.24	LH0071-0	0.1%	20 mV	−25°C to +85°C	0 mA to 20 mA	1Ω
10.24	LH0071-1	0.1%	10 mV	−25°C to +85°C	0 mA to 20 mA	1Ω
10.24	LH0071-2	0.05%	4 mV	−25°C to +85°C	0 mA to 20 mA	1Ω
Adjustable— 5V, 6V, 10V, 12V, 15V	LH0075	±0.5%	0.003%/°C typ	−55°C to +125°C	1 mA to 200 mA	1Ω
Adjustable— 5V, 6V, 10V, 12V, 15V	LH0075C	±1%	0.003%/°C typ	0°C to +70°C	1 mA to 200 mA	1Ω
Adjustable— −5V, −6V, −10V, −12V, −15V	LH0076	±0.5%	0.003%/°C typ	−55°C to +125°C	1 mA to 200 mA	1Ω
Adjustable— −5V, −6V, −10V, −12V, −15V	LH0076C	±1%	0.003%/°C typ	0°C to +70°C	1 mA to 200 mA	1Ω

Reverse Breakdown Voltage V_R at I_R	Device	Voltage Tolerance Max, $T_A = 25°C$	Voltage Temperature Drift-ppm/°C Max or mV Max Change Over Temperature Range		Current Range, I_R	Output Dynamic Impedance (Max)
			Drift (Max)	Temperature Range		
LOW CURRENT ZENER DIODES						
1.8	LM103	± 10%	− 5 mV/°C typ	− 55°C to + 125°C	10 μA to 10 mA	25Ω
2.0	LM103	± 10%	− 5 mV/°C typ	− 55°C to + 125°C	10 μA to 10 mA	25Ω
2.2	LM103	± 10%	− 5 mV/°C typ	− 55°C to + 125°C	10 μA to 10 mA	25Ω
2.4	LM103	± 10%	− 5 mV/°C typ	− 55°C to + 125°C	10 μA to 10 mA	25Ω
2.7	LM103	± 10%	− 5 mV/°C typ	− 55°C to + 125°C	10 μA to 10 mA	25Ω
3.0	LM103	± 10%	− 5 mV/°C typ	− 55°C to + 125°C	10 μA to 10 mA	25Ω
3.3	LM103	± 10%	− 5 mV/°C typ	− 55°C to + 125°C	10 μA to 10 mA	25Ω
3.6	LM103	± 10%	− 5 mV/°C typ	− 55°C to + 125°C	10 μA to 10 mA	25Ω
3.9	LM103	± 10%	− 5 mV/°C typ	− 55°C to + 125°C	10 μA to 10 mA	25Ω
4.3	LM103	± 10%	− 5 mV/°C typ	− 55°C to + 125°C	10 μA to 10 mA	25Ω
4.7	LM103	± 10%	− 5 mV/°C typ	− 55°C to + 125°C	10 μA to 10 mA	25Ω
5.1	LM103	± 10%	− 5 mV/°C typ	− 55°C to + 125°C	10 μA to 10 mA	25Ω
5.6	LM103	± 10%	− 5 mV/°C typ	− 55°C to + 125°C	10 μA to 10 mA	25Ω

National Semiconductor

Voltage References

LH0070 Series Precision BCD Buffered Reference
LH0071 Series Precision Binary Buffered Reference

General Description

The LH0070 and LH0071 are precision, three terminal, voltage references consisting of a temperature compensated zener diode driven by a current regulator and a buffer amplifier. The devices provide an accurate reference that is virtually independent of input voltage, load current, temperature and time. The LH0070 has a 10.000V nominal output to provide equal step sizes in BCD applications. The LH0071 has a 10.240V nominal output to provide equal step sizes in binary applications.

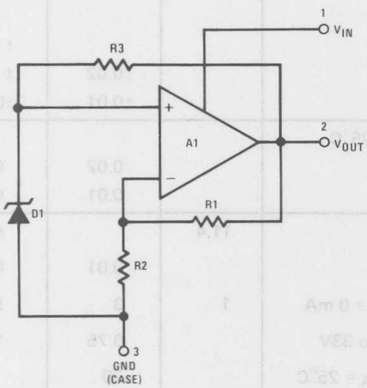
The output voltage is established by trimming ultra-stable, low temperature drift, thin film resistors under actual operating circuit conditions. The devices are short-circuit proof in both the current sourcing and sinking directions.

The LH0070 and LH0071 series combine excellent long term stability, ease of application, and low cost, making them ideal choices as reference voltages in precision D to A and A to D systems.

Features

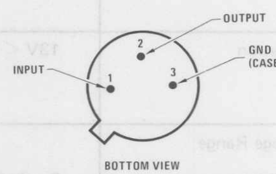
- Accurate output voltage
  - LH0070 — 10V ±0.02%
  - LH0071 — 10.24V ±0.02%
- Single supply operation — 11.4V to 40V
- Low output impedance — 0.2Ω
- Excellent line regulation — 0.1 mV/V
- Low zener noise — 20 μVp-p
- 3-lead TO-5 (pin compatible with the LM109)
- Short circuit proof
- Low standby current — 3 mA

Equivalent Schematic



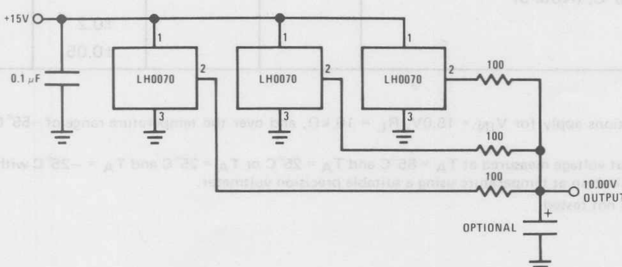
Connection Diagram

TO-5 Metal Can Package

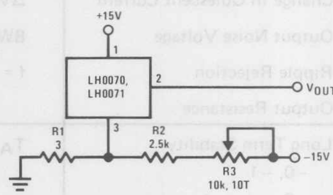


Order Number LH0070-0H, LH0071-0H, LH0070-1H, LH0071-1H, LH0070-2H or LH0071-2H
See NS Package H03B

Typical Applications



Statistical Voltage Standard



*Note. The output of the LH0070 and LH0071 may be adjusted to a precise voltage by using the above circuit since the supply current of the devices is relatively small and constant with temperature and input voltage. For the circuit shown, supply sensitivities are degraded slightly to 0.01%/V change in V_{OUT} for changes in V_{IN} and V−.

An additional temperature drift of 0.0001%/°C is added due to the variation of supply current with temperature of the LH0070 and LH0071. Sensitivity to the value of R1, R2 and R3 is less than 0.001%/%.

***Output Voltage Fine Adjustment**

Power Dissipation (See Curve)	600 mW
Short Circuit Duration	Continuous
Output Current	±20 mA
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	$T_A = 25°C$				
LH0070			10.000		V
LH0071			10.240		V
Output Accuracy	$T_A = 25°C$				
−0, −1			±0.03	±0.1	%
−2			±0.02	±0.05	%
Output Accuracy	$T_A = -55°C, 125°C$				
−0, −1				±0.3	%
−2				±0.2	%
Output Voltage Change With Temperature	(Note 2)				
−0				± 0.2	%
−1			±0.02	± 0.1	%
−2			±0.01	±0.04	%
Line Regulation	$13V \leq V_{IN} \leq 33V$, $T_C = 25°C$				
−0, −1			0.02	0.1	%
−2			0.01	0.03	%
Input Voltage Range		11.4		40	V
Load Regulation	$0 mA \leq I_{OUT} \leq 5 mA$		0.01	0.03	%
Quiescent Current	$13V \leq V_{IN} \leq 33V$, $I_{OUT} = 0 mA$	1	3	5	mA
Change In Quiescent Current	$\Delta V_{IN} = 20V$ From 13V To 33V		0.75	1.5	mA
Output Noise Voltage	BW = 0.1 Hz To 10 Hz, $T_A = 25°C$		20		μVp-p
Ripple Rejection	f = 120 Hz		0.01		%/Vp-p
Output Resistance			0.2	0.6	Ω
Long Term Stability	$T_A = 25°C$, (Note 3)				
−0, −1				±0.2	%/yr.
−2				±0.05	%/yr.

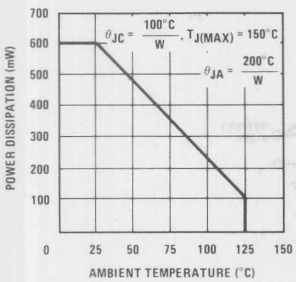
Note 1: Unless otherwise specified, these specifications apply for $V_{IN} = 15.0V$, $R_L = 10\ k\Omega$, and over the temperature range of $-55°C \leq T_A \leq +125°C$.

Note 2: This specification is the difference in output voltage measured at $T_A = 85°C$ and $T_A = 25°C$ or $T_A = 25°C$ and $T_A = -25°C$ with readings taken after test chamber and device-under-test stabilization at temperature using a suitable precision voltmeter.

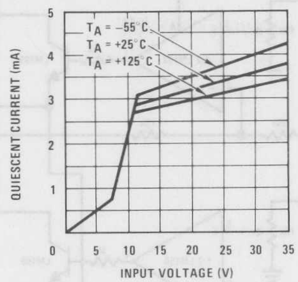
Note 3: This parameter is guaranteed by design and not tested.

Typical Performance Characteristics

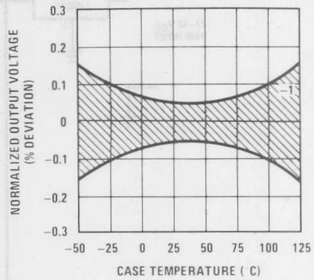
Maximum Power Dissipation



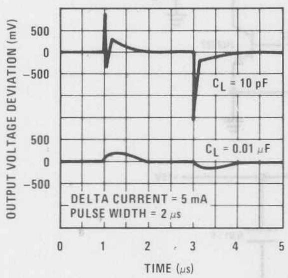
Quiescent Current vs Input Voltage



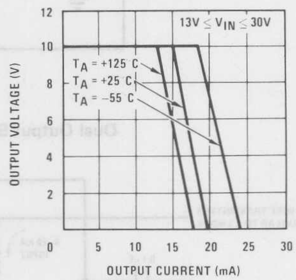
Normalized Output Voltage vs Temperature



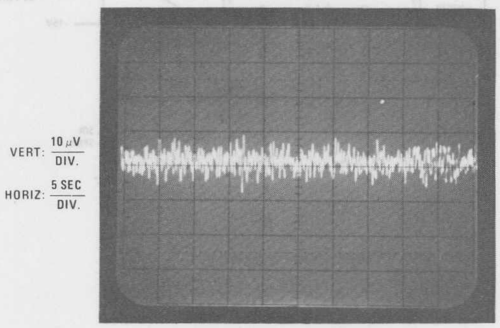
Step Load Response



Output Short Circuit Characteristics

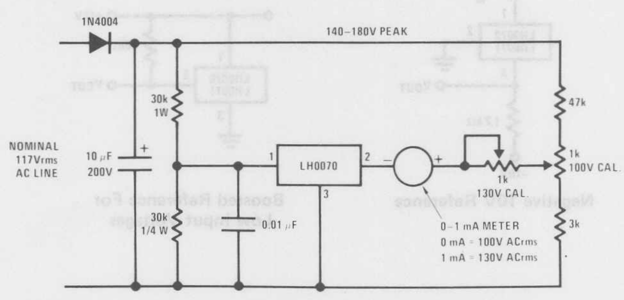


Noise Voltage



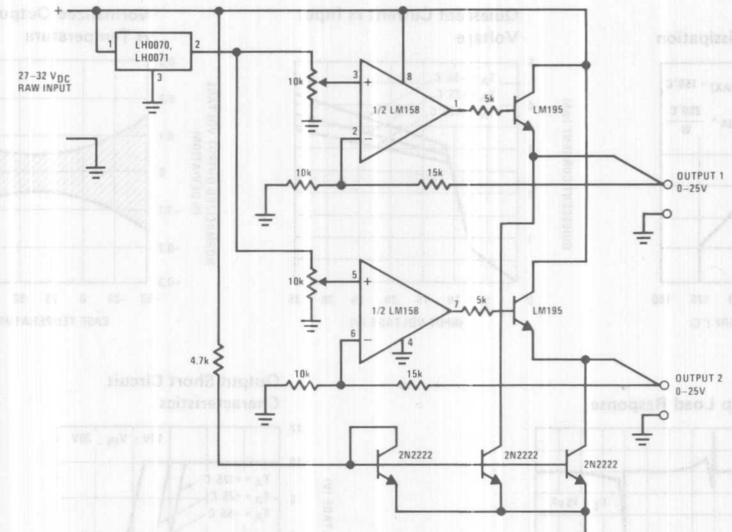
BW = 0.1 Hz TO 10 Hz

Typical Applications (Continued)

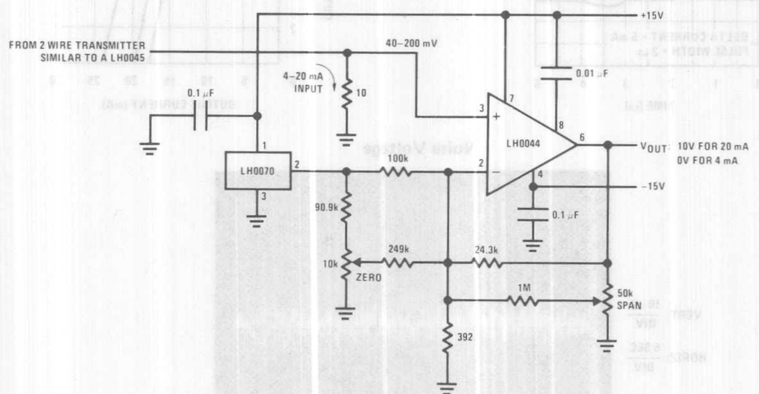


Expanded Scale AC Voltmeter

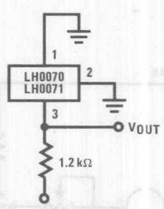
Typical Applications (Continued)



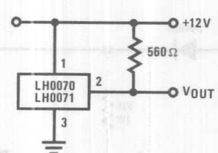
Dual Output Bench Power Supply



Precision Process Control Interface



Negative 10V Reference



Boosted Reference For Low Input Voltages

National Semiconductor

Voltage References

LH0075 Positive Precision Programmable Regulator

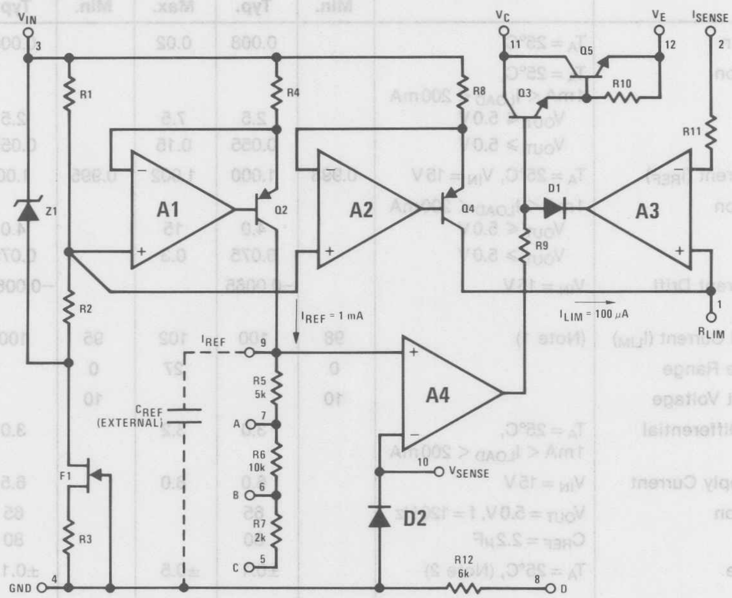
General Description

The LH0075 is a precision programmable regulator for positive voltages. Regulated output voltages from 0 to 27V may be obtained using one external resistor. Also available without any external components are several fixed regulated voltages with accuracies to 0.1% (5V, 6V, 10V, 12V and 15V). The output current limit is adjustable from 0 to 200 mA using two external resistors. These features provide an inventory of precision regulated values in one package.

Features

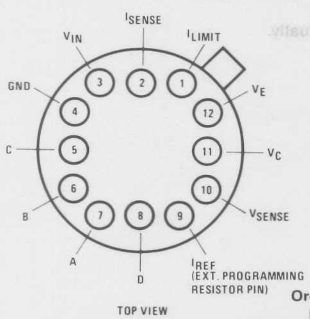
- Output adjustable to 0V
- Line regulation typically 0.008%/V
- Load regulation typically 0.075%
- Remote voltage sensing
- Ripple rejection of 80 dB
- Adjustable precision current limit
- Output currents to 200 mA
- Popular voltages available without external resistors

Schematic Diagram



Connection Diagram

TO-8 Metal Can Package



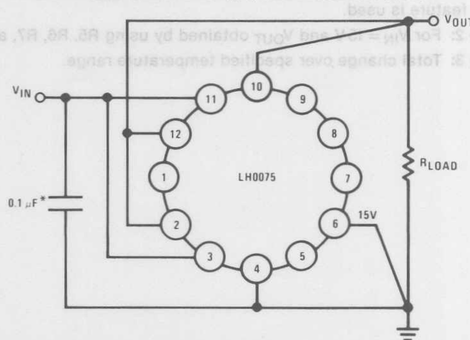
TOP VIEW

Case is electrically isolated

Order Number LH0075G LH0075CG See Package H12B

Typical Applications

Precision 15V Reference Supply without Current Limit



*Needed if device is far from filter capacitors

Output Current		200 mA
Power Dissipation		See Curve
Operating Temperature Range	T_{MIN}	T_{MAX}
LH0075		−55°C to +125°C
LH0075C		0° to +70°C
Storage Temperature		−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)		300°C

Electrical Characteristics Conditions for $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise noted

Parameter	Conditions	LH0075			LH0075C			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Line Regulation	$T_A = 25°C$		0.008	0.02		0.008	0.04	%/V
Load Regulation	$T_A = 25°C$, $1\,mA < I_{LOAD} < 200\,mA$							
	$V_{OUT} \leq 5.0\,V$		2.5	7.5		2.5	15	mV
	$V_{OUT} \geq 5.0\,V$		0.055	0.15		0.055	0.3	%
Reference Current (I_{REF})	$T_A = 25°C$, $V_{IN} = 15\,V$	0.998	1.000	1.002	0.995	1.00	1.005	mA
Load Regulation	$1\,mA < I_{LOAD} < 200\,mA$							
	$V_{OUT} \leq 5.0\,V$		4.0	15		4.0	25	mV
	$V_{OUT} \geq 5.0\,V$		0.075	0.3		0.075	0.5	%
Reference Current Drift ($\Delta I_{REF}/\Delta Temp.$)	$V_{IN} = 15\,V$		−0.0065			−0.0065		%/°C
Minimum Load Current (I_{LIM})	(Note 1)	98	100	102	95	100	105	μA
Output Voltage Range		0		27	0		27	V
Minimum Input Voltage		10			10			V
Input-Output Differential Voltage	$T_A = 25°C$, $1\,mA < I_{LOAD} < 200\,mA$		3.0	3.2		3.0	3.5	V
Quiescent Supply Current	$V_{IN} = 15\,V$		6.0	8.0		6.5	10	mA
Ripple Rejection	$V_{OUT} = 5.0\,V$, $f = 120\,Hz$		65			65		dB
	$C_{REF} = 2.2\,\mu F$		80			80		dB
Output Voltage Tolerance	$T_A = 25°C$, (Note 2)		±0.1	±0.5		±0.1	±1.0	%
Output Voltage Change with Temperature ($\Delta V_{OUT}/\Delta Temp.$)	(Note 3)		0.003			0.003		%/°C

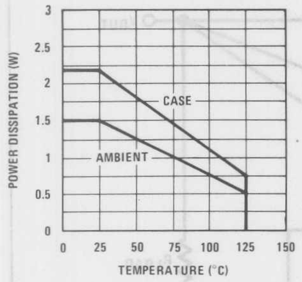
Note 1: Minimum load current is established by I_{LIM}, the current from Q4 (see schematic). I_{LIM} goes directly to the output if the current limit feature is used.

Note 2: For $V_{IN} = 15\,V$ and V_{OUT} obtained by using R5, R6, R7, and R12 individually.

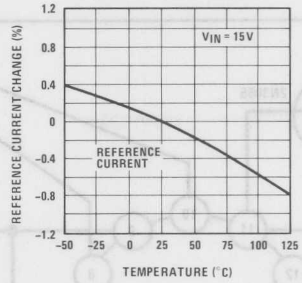
Note 3: Total change over specified temperature range.

Typical Performance Characteristics

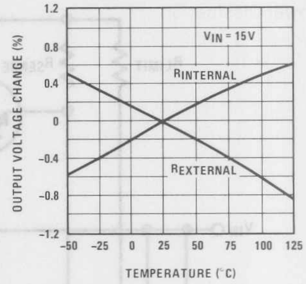
Maximum Power Dissipation



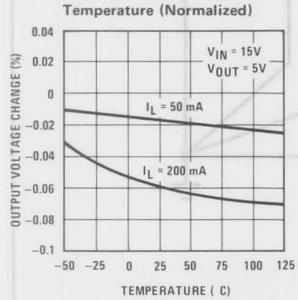
Reference Current Change with Temperature (Normalized)



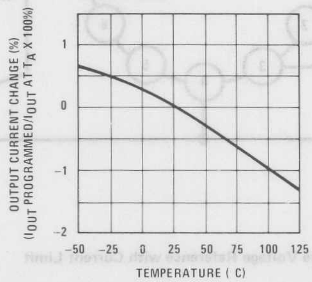
Temperature Stability



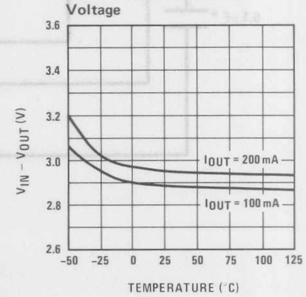
Output Voltage Change with Temperature (Normalized)



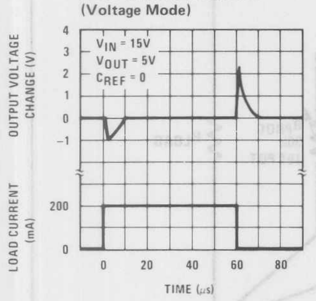
Current Limit



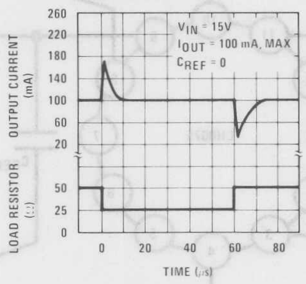
Input–Output Differential Voltage



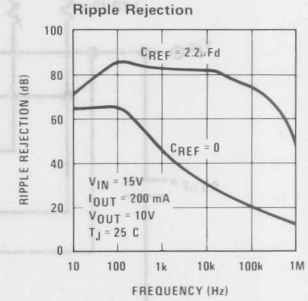
Load Transient Response (Voltage Mode)



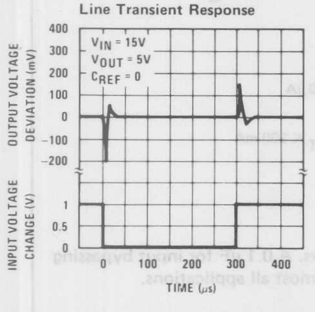
Load Transient Response (Current Mode)



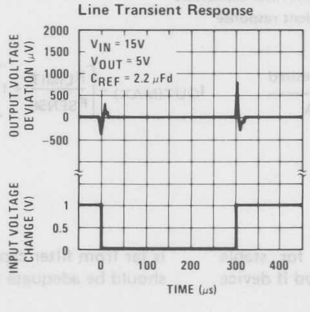
Ripple Rejection



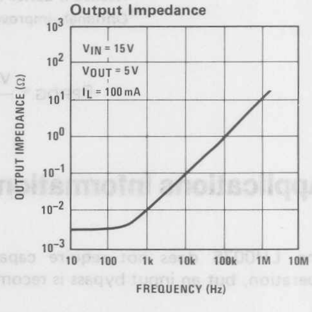
Line Transient Response



Line Transient Response

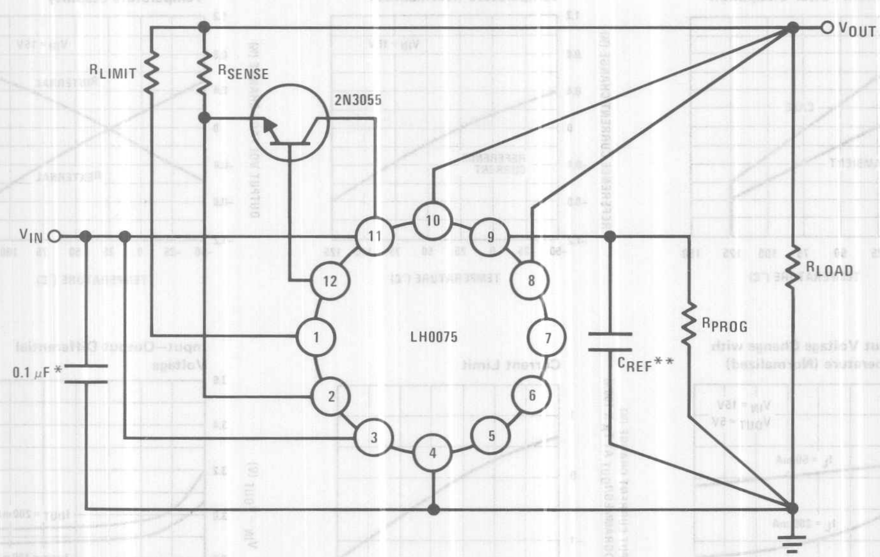


Output Impedance

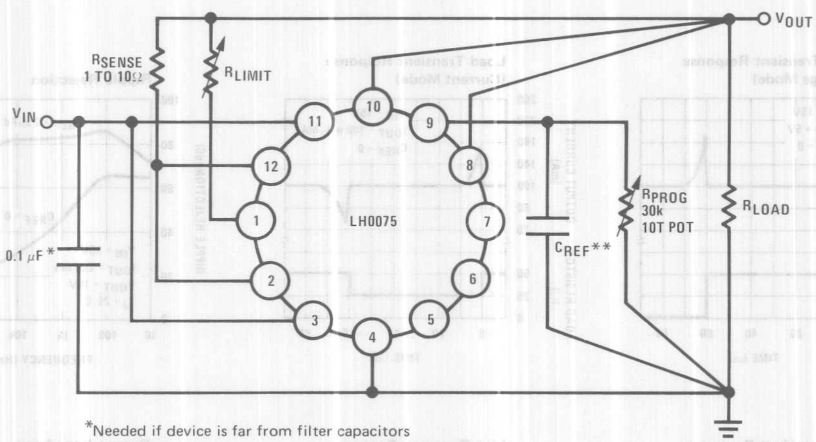


Typical Applications (Cont'd)

2A Regulator with Current Limit



Variable Voltage Reference with Current Limit



*Needed if device is far from filter capacitors

**Optional—improves transient response

$$R_{PROG} = \frac{V_{OUT}\ \text{Desired}}{1\ \text{mA}} \qquad I_{OUT(MAX)} = \left[\frac{R_{LIMIT}}{R_{SENSE}} + 1\right] \times 100\ \mu A$$

$$I_{OUT} \leq 200\ \text{mA}$$

Applications Information

The LH0075 does not require capacitors for stable operation, but an input bypass is recommended if device is far from filter capacitors. A 0.1 μF for input bypassing should be adequate for almost all applications.

jection Typically to 80 dB)

The ripple rejection may be improved by connecting an external capacitor between pin 9 and ground. (The typical performance curves show the rejection with a capacitance of 2.2 μFd.)

Internal Voltage Programming

The LH0075 provides various precision output voltages simply by using one or more of the internal resistors. A particular voltage may be obtained by external connections as shown in Table I.

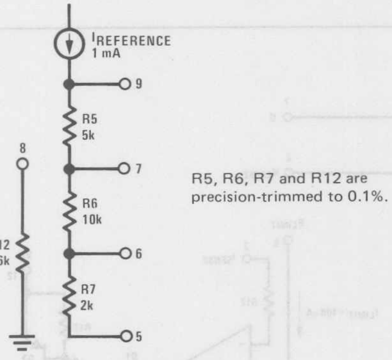


FIGURE 1

External Voltage Programming

An external resistance can be connected between pin 9 and ground to obtain any voltage from 0 to 27V using the following equation:

$$R_{EXT} = \frac{V_{OUT}\ \text{Desired}}{1\ \text{mA}}$$

The reference current (I_{REF}) has a typical temperature coefficient of −65 ppm/°C. Choosing a resistive material with a temperature coefficient of 65 ppm/°C will compensate the negative temperature coefficient, resulting in an output voltage with minimal change over the operating temperature range. Example of a good resistive material is Nichrome, which has a typical temperature coefficient of 80 ppm/°C.

Current Limit Programming

The maximum current output of the device may be limited by adding two external resistors as shown below. The resistor values are easily calculated with the following equation:

$$I_{OUT(MAX)} = \left[\frac{R_{LIMIT}}{R_{SENSE}} + 1\right] \times 100\,\mu A$$

where $R_{SENSE} = 1$ to 10Ω

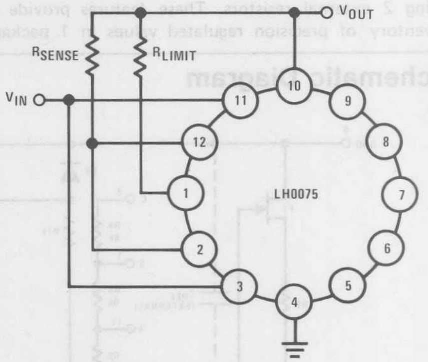


FIGURE 2. Current Limit Programming

This programmable current limit feature can be extended to make the LH0075 a programmable constant current source. This can be done by leaving pin 9 open and setting R_{LIMIT} and R_{SENSE} as desired.

For applications where the current limit is used, a minimum load current of 100 μA is established at the output. This arises from the fact that the constant current used in setting maximum output current is 100 μA, and it goes directly to the output of the LH0075. If the total current drawn from the output is less than the minimum, the output will rise.

As in the remote voltage adjustment application, remote current sensing can be applied similarly. R_{SENSE} must be placed as close to the output of the LH0075 as possible, but R_{LIMIT} can be a fixed resistor or potentiometer located remotely from the device.

TABLE I. Connection Scheme for Internal Available Output Voltages

OUTPUT VOLTAGE (V)	PIN 5	PIN 6	PIN 7	PIN 8	PIN 9
5			Gnd		
6				•	•
8	•	•		•	•
10		Gnd	•		•
12	Gnd		•		•
15		Gnd			
18	•		•	•	•

LH0076 Negative Precision Programmable Regulator

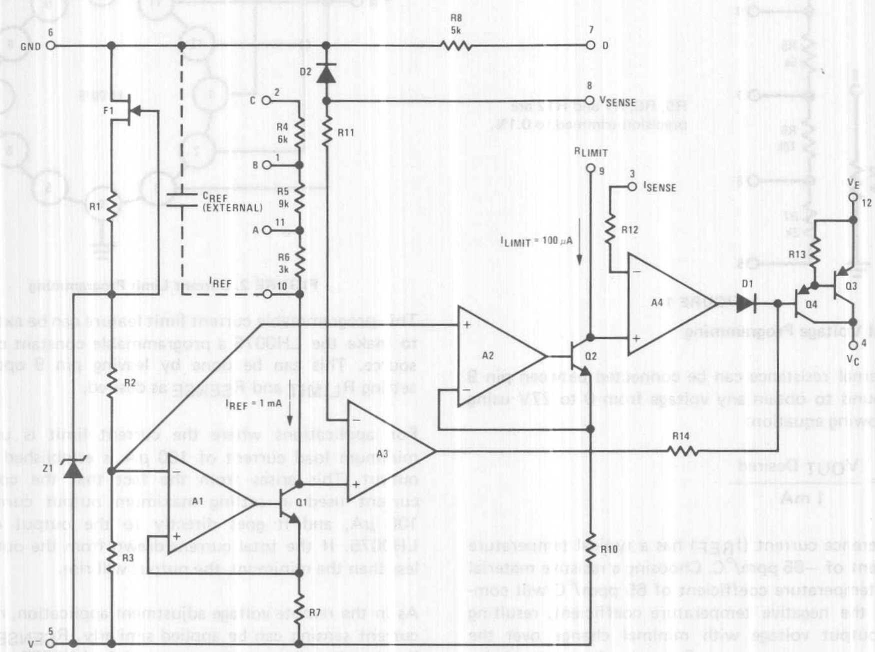
General Description

The LH0076 is a precision programmable regulator for negative voltages. Regulated output voltages from 0 to −27V may be obtained by using 1 external resistor. Also available without any external components are several fixed regulated voltages with accuracies to 0.1% (−3V, −5V, −6V, −8V, −9V, −12V, −15V and −18V). The output current limit is adjustable from 0 to 200 mA using 2 external resistors. These features provide an inventory of precision regulated values in 1 package.

Features

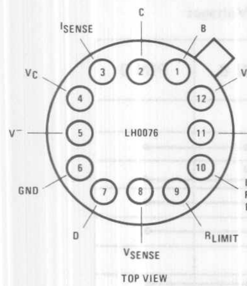
- Line regulation typically 0.005%/V
- Load regulation typically 0.02%
- Remote voltage sensing
- Ripple rejection−70 dB
- Output Adjustable to 0V
- Adjustable precision current limit
- Output current to 200 mA

Schematic Diagram



Connection Diagram

Metal Can Package



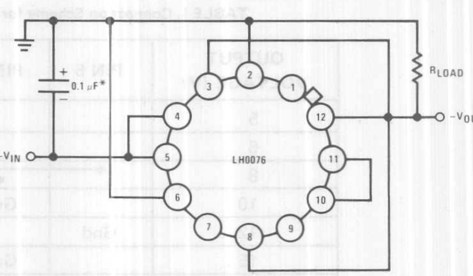
TOP VIEW

Case is electrically isolated

Order Number
LH0076G
LH0076CG
See Package H12B

Typical Application

Precision − 15V Reference Supply without Current Limit



*Recommended if device is far from filter capacitors

Absolute Maximum Ratings

Input Voltage	−32 V
Output Voltage	−27 V
Output Current	200 mA
Power Dissipation	See Curve
Operating Temperature Range	
LH0076	−55°C to +125°C
LH0076C	−25°C to +85°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

Conditions are for $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise noted

Parameter	Conditions	LH0076 Min.	LH0076 Typ.	LH0076 Max.	LH0076C Min.	LH0076C Typ.	LH0076C Max.	Units
Line Regulation	$T_A = 25°C$		0.005	0.02		0.005	0.04	%/V
Load Regulation	$T_A = 25°C$, $1\,mA < I_{LOAD} < 200\,mA$							
	$V_{OUT} \geq -5.0\,V$			7.5			15	mV
	$V_{OUT} \leq -5.0\,V$		0.02	0.15		0.02	0.3	%
Reference Current (I_{REF})	$T_A = 25°C$, $V_{IN} = -15\,V$	0.998	1.000	1.002	0.995	1.000	1.005	mA
Reference Current Drift ($\Delta I_{REF}/\Delta Temp.$)	$V_{IN} = -15\,V$		−0.0065			−0.0065		%/°C
Minimum Load Current (I_{LIM})	(Note 1)	98	100	102	95	100	105	μA
Output Voltage Range		0		−27	0		−27	V
Minimum Input Voltage		−10			−10			V
Input-Output Differential Voltage	$T_A = 25°C$, $1\,mA < I_{LOAD} < 200\,mA$		2.7	3.2		2.7	3.5	V
Quiescent Supply Current	$V_{IN} = -15\,V$		11	15		11	15	mA
Ripple Rejection	$V_{OUT} = -5.0\,V$, f = 120 Hz		70			70		dB
Output Voltage Tolerance	$T_A = 25°C$, (Note 2)		±0.1	±0.5		±0.1	±1.0	%
Output Voltage Change with Temperature ($\Delta V_{OUT}/\Delta Temp.$)	(Note 3)		0.003			0.003		%/°C

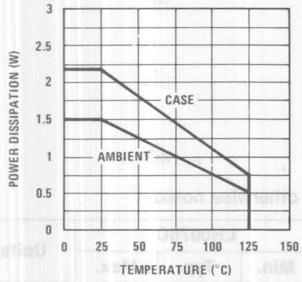
Note 1: Minimum load current is established by I_{LIM}, the current to Q2 (see schematic). I_{LIM} draws directly from the output if the current limit feature is used.

Note 2: For $V_{IN} = -15\,V$ and V_{OUT} obtained by using R4, R5, R6, and R8 individually.

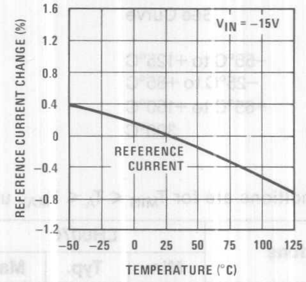
Note 3: Total change over specified temperature range.

Typical Performance Characteristics

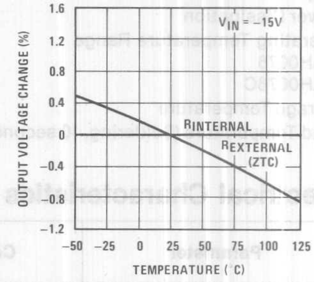
Maximum Power Dissipation



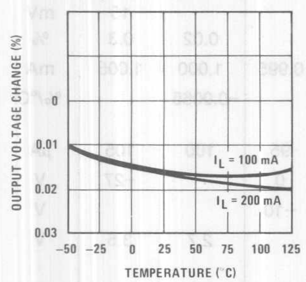
Reference Current Change with Temperature (Normalized)



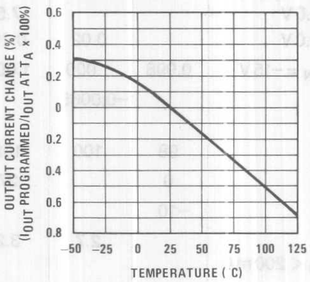
Temperature Stability



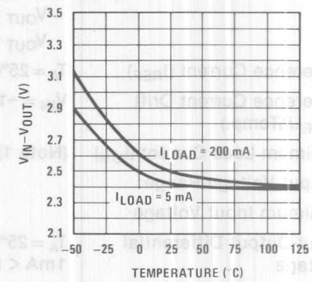
Output Voltage Change with Temperature (Normalized)



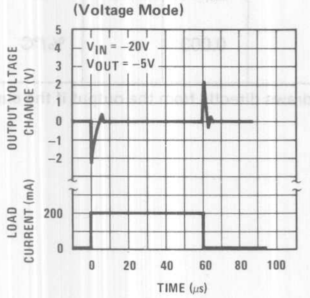
Current Limit



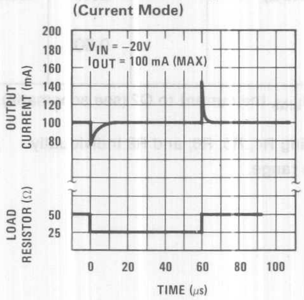
Input-Output Differential Voltage



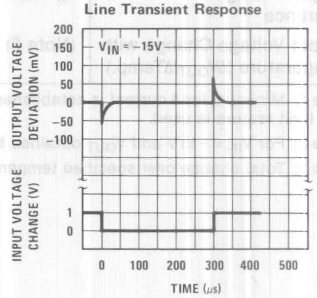
Load Transient Response (Voltage Mode)



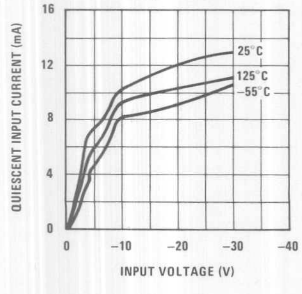
Load Transient Response (Current Mode)



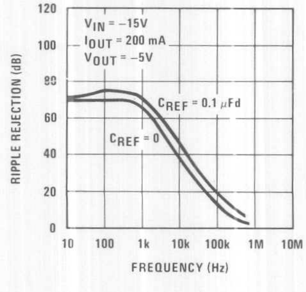
Line Transient Response



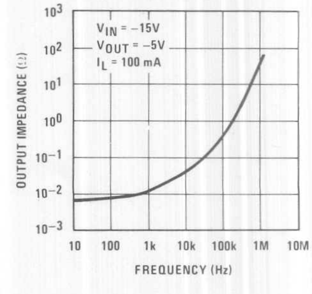
Quiescent Input Current



Ripple Rejection

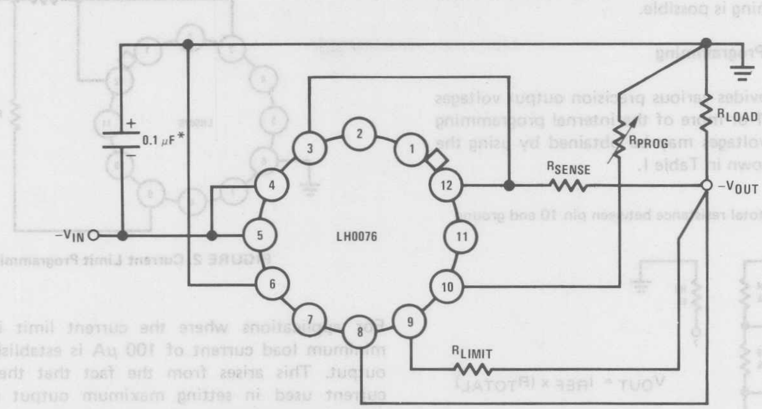


Output Impedance

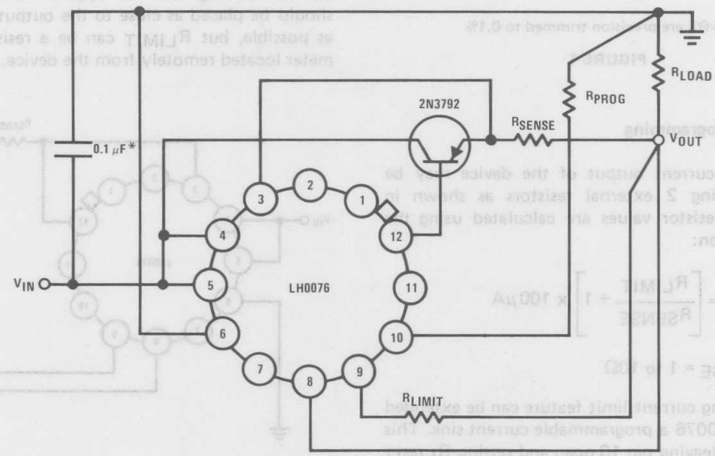


Typical Application (Continued)

Variable Voltage Reference with Current Limit



2-Amp Regulator with Current Limit



*Recommended if device is far from filter capacitors

Application Information

The LH0076 does not require external capacitors for stable operation. However, an input bypass is recommended if the device is far from filter capacitors. A 0.1 μF for input bypassing should be adequate for most applications.

DESCRIPTION OF OPTIONS

External Voltage Programming

An external resistance can be connected between pin 10 and ground to obtain any voltage from 0 to −27V using the following equation:

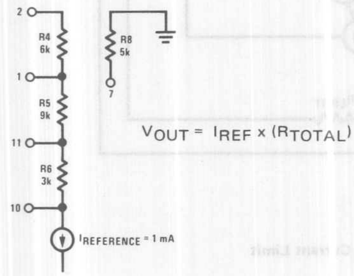
$$R_{EXT} = \frac{V_{OUT} \text{ desired}}{-1 \text{ mA}}$$

The reference current (I_{REF}) has a typical temperature coefficient of −60 ppm/°C. Choosing a resistive material with a temperature coefficient of 60 ppm/°C will compensate the negative tempco of the reference current, resulting in an output voltage with minimal change over the operating temperature range. Example of a good resistive material is nichrome, which has a typical tempco of 80 ppm/°C. Nichrome is the resistive material used in the LH0076, resulting in output voltage drift of 20 ppm/°C typically.

Internal Voltage Programming

The LH0076 provides various precision output voltages simply by using 1 or more of the internal programming resistors. These voltages may be obtained by using the connections as shown in Table I.

R_{TOTAL} is the total resistance between pin 10 and ground



R4, R5, R6 and R8 are precision trimmed to 0.1%

FIGURE 1

Current Limit Programming

The maximum current output of the device may be limited by adding 2 external resistors as shown in *Figure 2*. The resistor values are calculated using the following equation:

$$I_{OUT(MAX)} = \left[\frac{R_{LIMIT}}{R_{SENSE}} + 1\right] \times 100\,\mu A$$

where $R_{SENSE} = 1$ to 10Ω

This programming current limit feature can be extended to make the LH0076 a programmable current sink. This can be done by leaving pin 10 open and setting R_{LIMIT} and R_{SENSE} as desired. (See *Figure 3*).

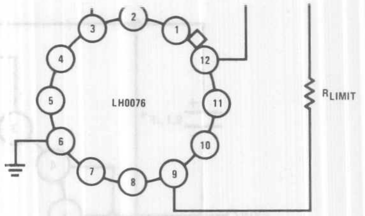


FIGURE 2. Current Limit Programming

For applications where the current limit is used, a minimum load current of 100 μA is established at the output. This arises from the fact that the constant current used in setting maximum output current is 100 μA, and it comes directly from the output of the LH0076. If the total load current is less than this minimum current, the output will drop.

As in the remote voltage adjustment application, remote current sensing can be applied similarly. R_{SENSE} should be placed as close to the output of the LH0076 as possible, but R_{LIMIT} can be a resistor or potentiometer located remotely from the device.

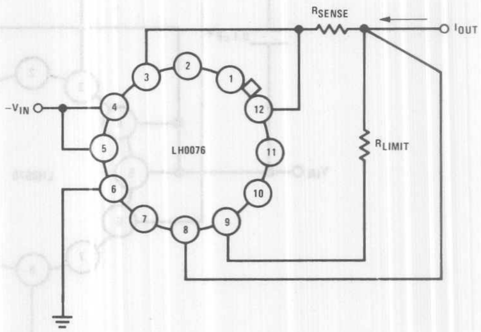


FIGURE 3. Precision Current Sink

TABLE I. Connection Scheme for Internally Available Output Voltages

OUTPUT VOLTAGE (V)	PIN 1	PIN 2	PIN 7	PIN 10	PIN 11
−3					Gnd
−5					
−6		Gnd			
−8					
−9	Gnd				
−12	Gnd				
−15		Gnd			
−18		Gnd			

LM103 Reference Diode**

General Description

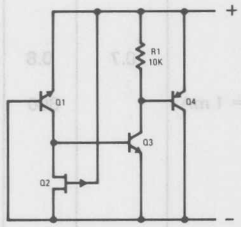
The LM103 is a two-terminal monolithic reference diode electrically equivalent to a breakdown diode. The device makes use of the reverse punch-through of double-diffused transistors, combined with active circuitry, to produce a breakdown characteristic which is ten times sharper than single-junction zener diodes at low voltages. Breakdown voltages from 1.8V to 5.6V are available; and, although the design is optimized for operation between 100 μA and 1 mA, it is completely specified from 10 μA to 10 mA. Noteworthy features of the device are:

- Exceptionally sharp breakdown
- Low dynamic impedance from 10 μA to 10 mA
- Performance guaranteed over full military temperature range
- Planar, passivated junctions for stable operation
- Low capacitance.

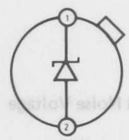
The LM103, packaged in a hermetically sealed, modified TO-46 header is useful in a wide range of circuit applications from level shifting to simple voltage regulation. It can also be employed with operational amplifiers in producing breakpoints to generate nonlinear transfer functions. Finally, its unique characteristics recommend it as a reference element in low voltage power supplies with input voltages down to 4V.

2

Schematic and Connection Diagrams



Metal Can Package



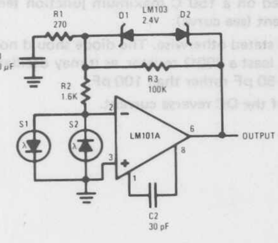
Note: Pin 2 connected to case.

TOP VIEW

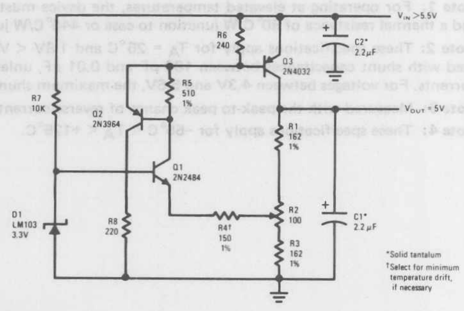
Order Number LM103H
See NS Package H02A

Typical Applications

Saturating Servo Preamplifier with Rate Feedback



200 mA Positive Regulator



**Covered by U.S. Patent Number 3,571,630

Absolute Maximum Ratings

Power Dissipation (note 1)	250 mW
Reverse Current	20 mA
Forward Current	100 mA
Operating Temperature Range	−55°C to 125°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (soldering, 60 sec)	300°C

Electrical Characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Reverse Breakdown Voltage Change	$10\ \mu A \leq I_R \leq 100\ \mu A$		60	120	mV
	$100\ \mu A \leq I_R \leq 1\ mA$		15	50	mV
	$1\ mA \leq I_R \leq 10\ mA$		50	150	mV
Reverse Dynamic Impedance (Note 3)	$I_R = 3\ mA$		5	25	Ω
	$I_R = 0.3\ mA$		15	60	Ω
Reverse Leakage Current	$V_R = V_Z - 0.2V$		2	5	μA
Forward Voltage Drop	$I_F = 10\ mA$	0.7	0.8	1.0	V
Peak-to-Peak Broadband Noise Voltage	$10\ Hz \leq f \leq 100\ kHz$, $I_R = 1\ mA$		300		μV
Reverse Breakdown Voltage Change with Current (Note 4)	$10\ \mu A \leq I_R \leq 100\ \mu A$			200	mV
	$100\ \mu A \leq I_R \leq 1\ mA$			60	mV
	$1\ mA \leq I_R \leq 10\ mA$			200	mV
Breakdown Voltage Temperature Coefficient (Note 4)	$100\ \mu A \leq I_R \leq 1\ mA$		−5.0		mV/°C

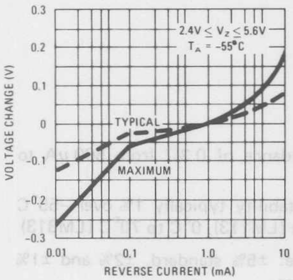
Note 1: For operating at elevated temperatures, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 80°C/W junction to case or 440°C/W junction to ambient (see curve).

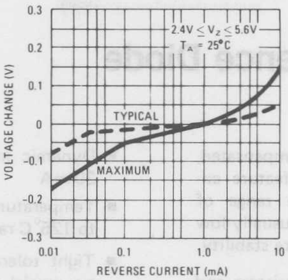
Note 2: These specifications apply for $T_A = 25°C$ and $1.8V < V_Z < 5.6V$ unless stated otherwise. The diode should not be operated with shunt capacitances between 100 pF and 0.01 μF, unless isolated by at least a 300Ω resistor, as it may oscillate at some currents. For voltages between 4.3V and 5.6V, the maximum shunt capacitance is 50 pF rather than 100 pF.

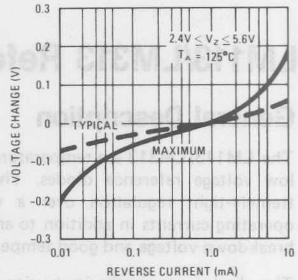
Note 3: Measured with the peak-to peak change of reverse current equal to 10% of the DC reverse current.

Note 4: These specifications apply for $-55°C < T_A < +125°C$.

Guaranteed Reverse Characteristics

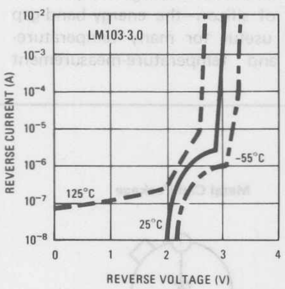




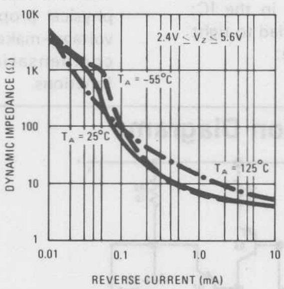


Typical Performance Characteristics

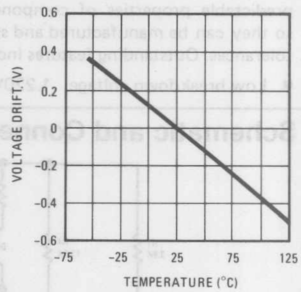
Reverse Characteristics



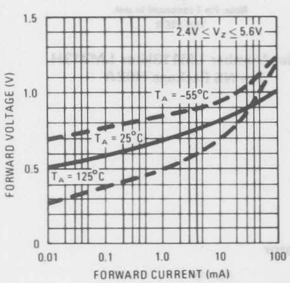
Reverse Dynamic Impedance



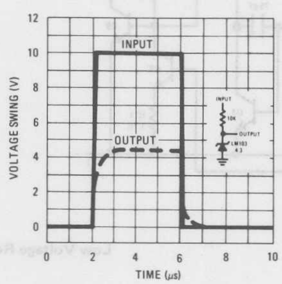
Temperature Drift



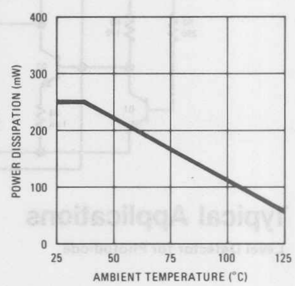
Forward Characteristics



Response Time



Maximum Power Dissipation



BREAKDOWN VOLTAGE*	PART NUMBER
1.8	LM103H-1.8
2.0	LM103H-2.0
2.2	LM103H-2.2
2.4	LM103H-2.4
2.7	LM103H-2.7
3.0	LM103H-3.0
3.3	LM103H-3.3
3.6	LM103H-3.6
3.9	LM103H-3.9
4.3	LM103H-4.3
4.7	LM103H-4.7
5.1	LM103H-5.1
5.6	LM103H-5.6

*Measured at I_R = 1 mA.

Standard tolerance is ±10%.

LM113/LM313 Reference Diode

General Description

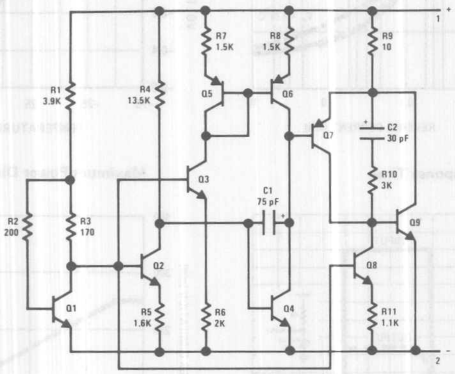
The LM113/LM313 are temperature compensated, low voltage reference diodes. They feature extremely-tight regulation over a wide range of operating currents in addition to an unusually-low breakdown voltage and good temperature stability.

The diodes are synthesized using transistors and resistors in a monolithic integrated circuit. As such, they have the same low noise and long term stability as modern IC op amps. Further, output voltage of the reference depends only on highly-predictable properties of components in the IC; so they can be manufactured and supplied to tight tolerances. Outstanding features include:

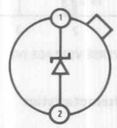
- Low breakdown voltage: 1.220V
- Dynamic impedance of 0.3Ω from 500 μA to 20 mA
- Temperature stability typically 1% over −55°C to 125°C range (LM113), 0°C to 70°C (LM313)
- Tight tolerance: ±5% standard, ±2% and ±1% on special order.

The characteristics of this reference recommend it for use in bias-regulation circuitry, in low-voltage power supplies or in battery powered equipment. The fact that the breakdown voltage is equal to a physical property of silicon—the energy-band-gap voltage—makes it useful for many temperature-compensation and temperature-measurement functions.

Schematic and Connection Diagrams



Metal Can Package

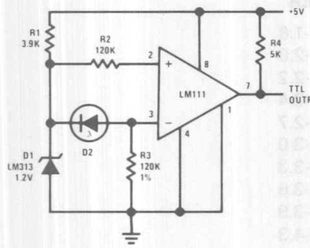


Note: Pin 2 connected to case.
TOP VIEW

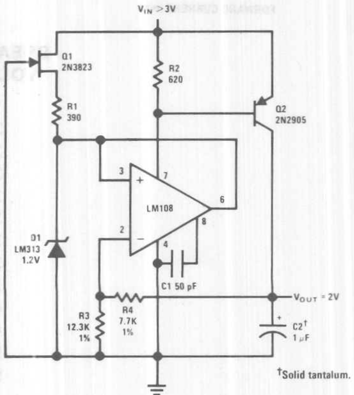
Order Number LM113H or LM313H
See NS Package H02A

Typical Applications

Level Detector for Photodiode



Low Voltage Regulator



†Solid tantalum.

Power Dissipation (Note 1)	100 mW	Temperature (T_A)			
Reverse Current	50 mA	LM113	−55	+125	°C
Forward Current	50 mA	LM313	0	70	°C
Storage Temperature Range	−65°C to +150°C				
Lead Temperature (Soldering, 10 seconds)	300°C				

Electrical Characteristics (Note 2)

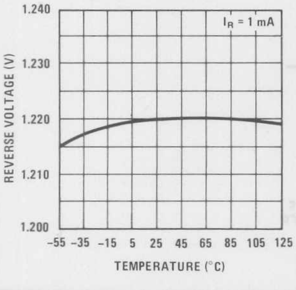
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reverse Breakdown Voltage					
LM113/LM313	$I_R = 1$ mA	1.160	1.220	1.280	V
LM113-1		1.210	1.22	1.232	V
LM113-2		1.195	1.22	1.245	V
Reverse Breakdown Voltage Change	$0.5\text{ mA} \leq I_R \leq 20\text{ mA}$		6.0	15	mV
Reverse Dynamic Impedance	$I_R = 1$ mA		0.2	1.0	Ω
	$I_R = 10$ mA		0.25	0.8	Ω
Forward Voltage Drop	$I_F = 1.0$ mA		0.67	1.0	V
RMS Noise Voltage	$10\text{ Hz} \leq f \leq 10\text{ kHz}$ $I_R = 1$ mA		5		μV
Reverse Breakdown Voltage Change with Current	$0.5\text{ mA} \leq I_R \leq 10\text{ mA}$ $T_{MIN} \leq T_A \leq T_{MAX}$			15	mV
Breakdown Voltage Temperature Coefficient	$1.0\text{ mA} \leq I_R \leq 10\text{ mA}$ $T_{MIN} \leq T_A \leq T_{MAX}$		0.01		%/°C

Note 1: For operating at elevated temperatures, the device must be derated based on a 150°C maximum junction and a thermal resistance of 80°C/W junction to case or 440°C/W junction to ambient.

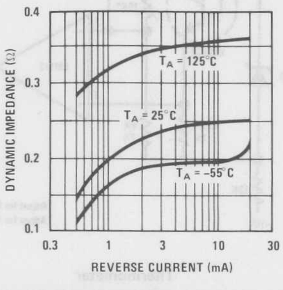
Note 2: These specifications apply for $T_A = 25°C$, unless stated otherwise. At high currents, breakdown voltage should be measured with lead lengths less than 1/4 inch. Kelvin contact sockets are also recommended. The diode should not be operated with shunt capacitances between 200 pF and 0.1 μF, unless isolated by at least a 100 Ω resistor, as it may oscillate at some currents.

Typical Performance Characteristics

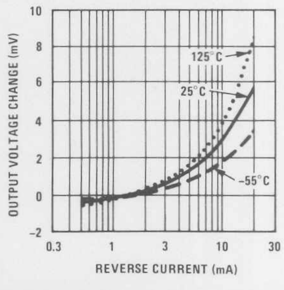
Temperature Drift



Reverse Dynamic Impedance

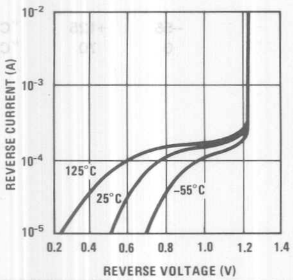


Reverse Characteristics

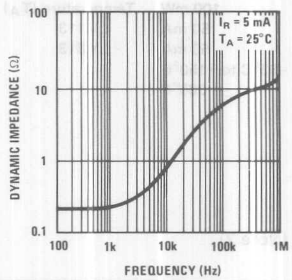


Typical Performance Characteristics (Continued)

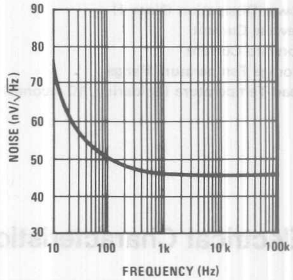
Reverse Characteristics



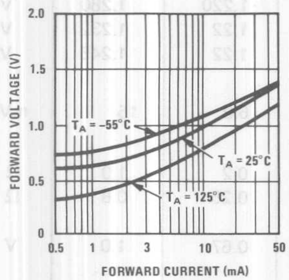
Reverse Dynamic Impedance



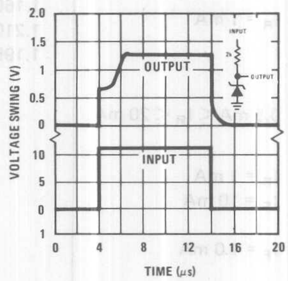
Noise Voltage



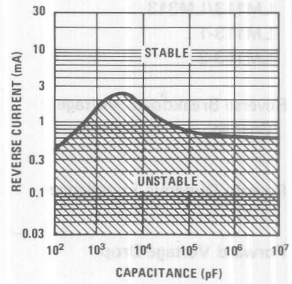
Forward Characteristics



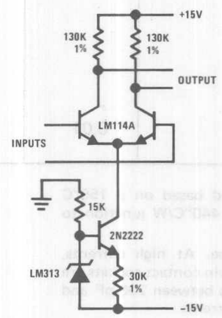
Response Time



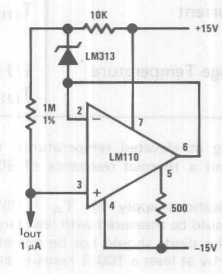
Maximum Shunt Capacitance



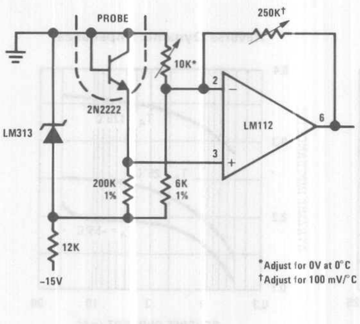
Typical Applications (Continued)



Amplifier Biasing for Constant Gain with Temperature



Constant Current Source



Thermometer

National Semiconductor

LM129/LM329 Precision Reference

General Description

The LM129 and LM329 family are precision multi-current temperature compensated 6.9V zener references with dynamic impedances a factor of 10 to 100 less than discrete diodes. Constructed in a single silicon chip, the LM129 uses active circuitry to buffer the internal zener allowing the device to operate over a 0.5 mA to 15 mA range with virtually no change in performance. The LM129 and LM329 are available with selected temperature coefficients of 0.001, 0.002, 0.005 and 0.01%/°C. These new references also have excellent long term stability and low noise.

A new subsurface breakdown zener used in the LM129 gives lower noise and better long term stability than conventional IC zeners. Further the zener and temperature compensating transistor are made by a planar process so they are immune to problems that plague ordinary zeners. For example, there is virtually no voltage shifts in zener voltage due to temperature cycling and the device is insensitive to stress on the leads.

The LM129 can be used in place of conventional zeners with improved performance. The low dynamic impedance simplifies biasing and the wide operating current allows the replacement of many zener types.

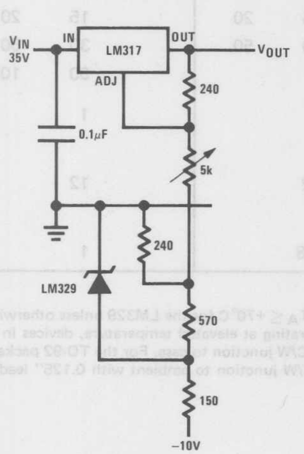
The LM129 is packaged in a 2-lead TO-46 package and is rated for operation over a −55°C to +125°C temperature range. The LM329 for operation over 0–70°C is available in both a hermetic TO-46 package and a TO-92 epoxy package.

Features

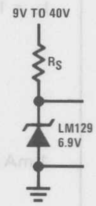
- 0.6 mA to 15 mA operating current
- 0.6Ω dynamic impedance at any current
- Available with temperature coefficients of 0.001%/°C
- 7μV wideband noise
- 5% initial tolerance
- 0.002% long term stability
- Low cost
- Subsurface zener

Typical Applications

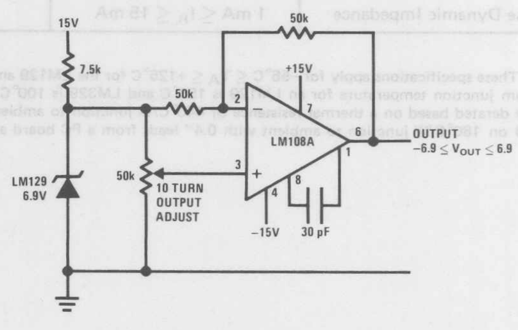
Low Cost 0–25V Regulator



Simple Reference



Adjustable Bipolar Output Reference



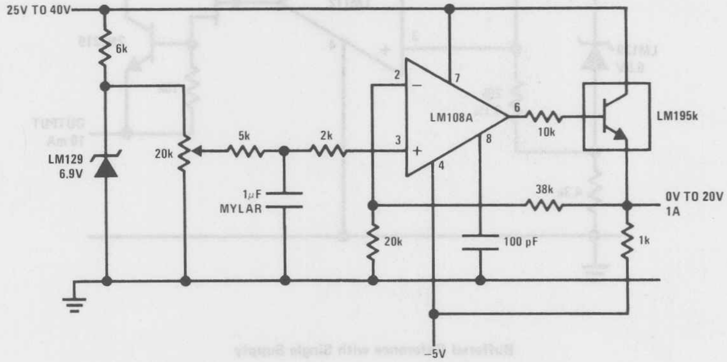
Operating Temperature Range
LM129 −55°C to +125°C
LM329 0°C to +70°C
Storage Temperature Range −55°C to +150°C
Lead Temperature (Soldering, 10 seconds) 300°C

Electrical Characteristics (Note 1)

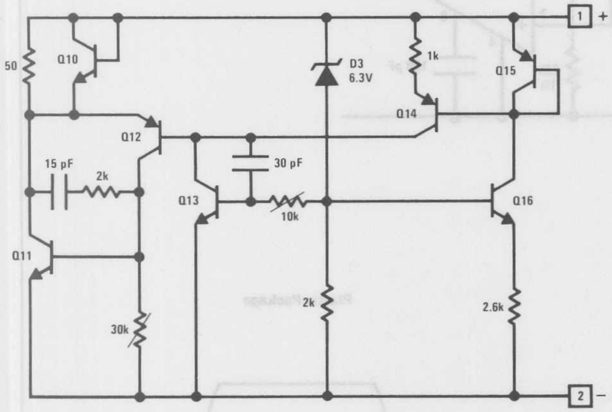
PARAMETER	CONDITIONS	LM129A, B, C			LM329B, C, D			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reverse Breakdown Voltage	$T_A = 25°C$, $0.6\ mA \leq I_R \leq 15\ mA$	6.7	6.9	7.2	6.6	6.9	7.25	V
Reverse Breakdown Change with Current	$T_A = 25°C$, $0.6\ mA \leq I_R \leq 15\ mA$		9	14		9	20	mV
Reverse Dynamic Impedance	$T_A = 25°C$, $I_R = 1\ mA$		0.6	1		0.8	2	Ω
RMS Noise	$T_A = 25°C$, $10\ Hz \leq F \leq 10\ kHz$		7	20		7	100	μV
Long Term Stability	$T_A = 45°C \pm 0.1°C$, $I_R = 1\ mA \pm 0.3\%$		20			20		ppm
Temperature Coefficient	$I_R = 1\ mA$							
LM129A, LM329A			6	10		6	10	ppm/°C
LM129B, LM329B			15	20		15	20	ppm/°C
LM129C, LM329C			30	50		30	50	ppm/°C
LM329D						50	100	ppm/°C
Change In Reverse Breakdown Temperature Coefficient	$1\ mA \leq I_R \leq 15\ mA$		1			1		ppm/°C
Reverse Breakdown Change with Current	$1\ mA \leq I_R \leq 15\ mA$		12			12		mV
Reverse Dynamic Impedance	$1\ mA \leq I_R \leq 15\ mA$		0.8			1		Ω

Note 1: These specifications apply for $-55°C \leq T_A \leq +125°C$ for the LM129 and $0°C \leq T_A \leq +70°C$ for the LM329 unless otherwise specified. The maximum junction temperature for an LM129 is 150°C and LM329 is 100°C. For operating at elevated temperature, devices in TO-46 package must be derated based on a thermal resistance of 440°C/W junction to ambient or 80°C/W junction to case. For the TO-92 package, the derating is based on 180°C/W junction to ambient with 0.4" leads from a PC board and 160°C/W junction to ambient with 0.125" lead length to a PC board.

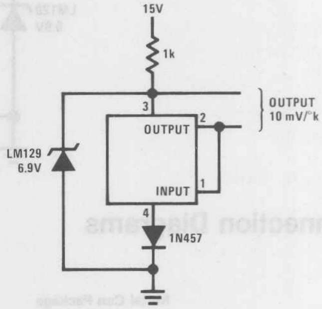
0V to 20V Power Reference



Reference

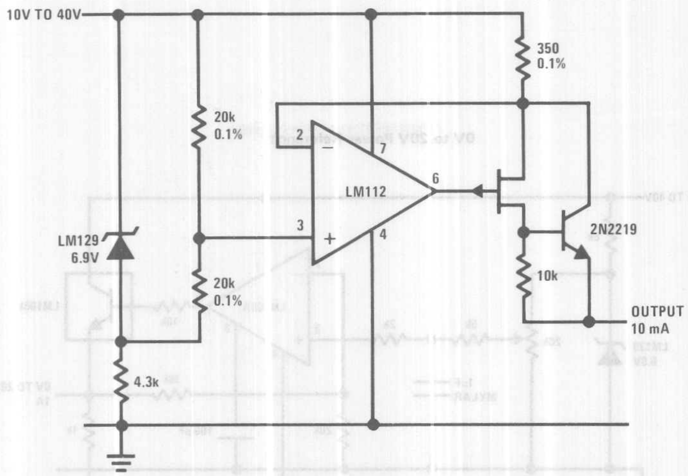


External Reference for Temperature Transducer

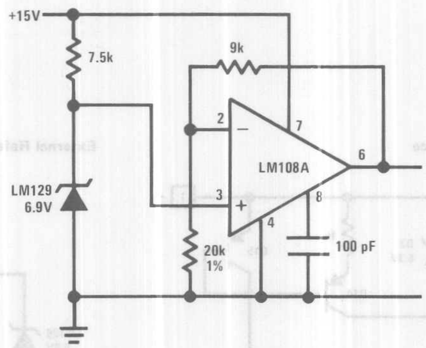


Typical Applications (Continued)

Positive Current Source

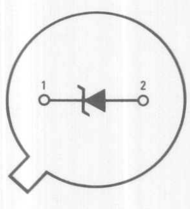


Buffered Reference with Single Supply



Connection Diagrams

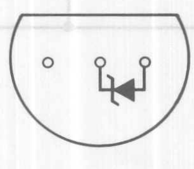
Metal Can Package



BOTTOM VIEW

Order Number LM129AH, LM129BH LM129CH, LM329AH, LM329BH, LM329CH or LM329DH
See NS Package H02A

Plastic Package

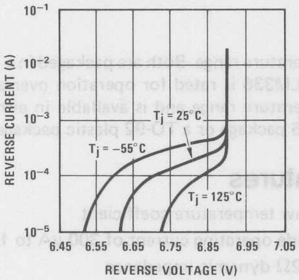


BOTTOM VIEW

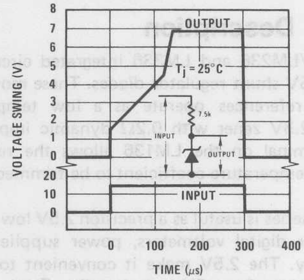
Order Number LM329BZ, LM329CZ or LM329DZ
See NS Package Z03A

Typical Performance Characteristics

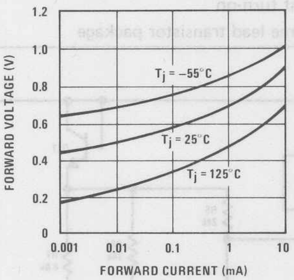
Reverse Characteristics



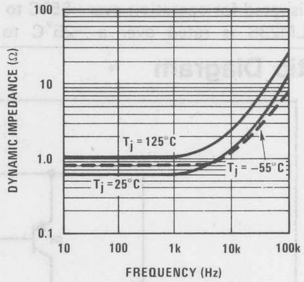
Response Time



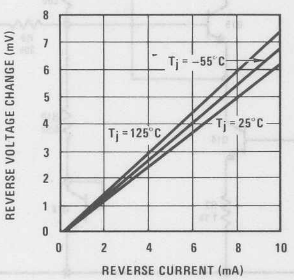
Forward Characteristics



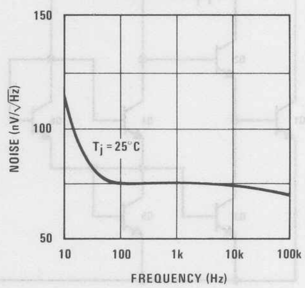
Dynamic Impedance



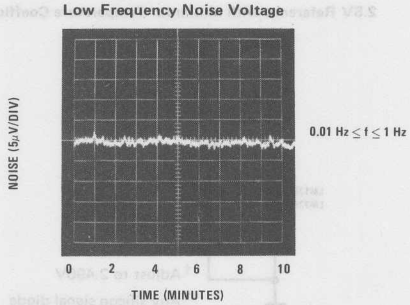
Reverse Voltage Change



Zener Noise Voltage



Low Frequency Noise Voltage



LM136/LM236/LM336 2.5V Reference Diode

General Description

The LM136/LM236 and LM336 integrated circuits are precision 2.5V shunt regulator diodes. These monolithic IC voltage references operate as a low temperature coefficient 2.5V zener with 0.2Ω dynamic impedance. A third terminal on the LM136 allows the reference voltage and temperature coefficient to be trimmed easily.

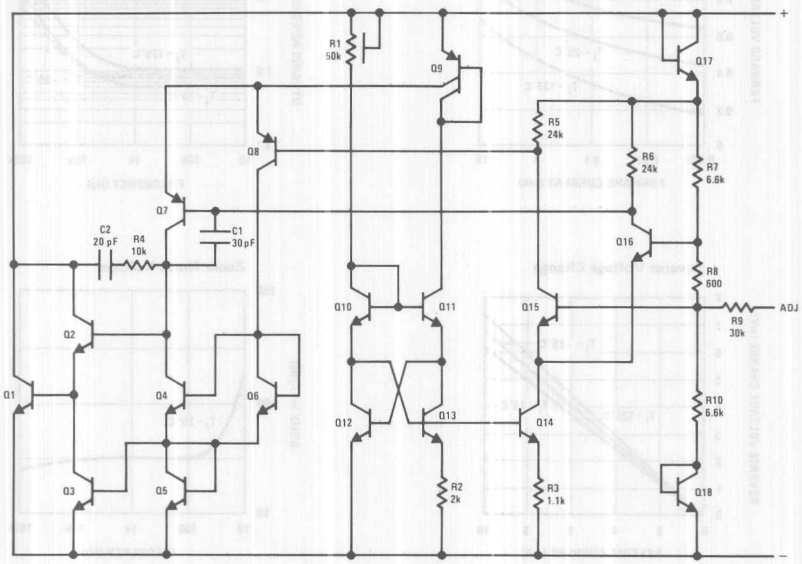
The LM136 series is useful as a precision 2.5V low voltage reference for digital voltmeters, power supplies or op amp circuitry. The 2.5V make it convenient to obtain a stable reference from 5V logic supplies. Further, since the LM136 operates as a shunt regulator, it can be used as either a positive or negative voltage reference.

The LM136 is rated for operation over −55°C to +125°C while the LM236 is rated over a −25°C to +85°C temperature range. Both are packaged in a TO-46 package. The LM336 is rated for operation over a 0°C to +70°C temperature range and is available in either a three lead TO-46 package or a TO-92 plastic package.

Features

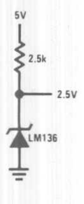
- Low temperature coefficient
- Wide operating current of 300 μA to 10 mA
- 0.2Ω dynamic impedance
- ±1% initial tolerance available
- Guaranteed temperature stability
- Easily trimmed for minimum temperature drift
- Fast turn-on
- Three lead transistor package

Schematic Diagram

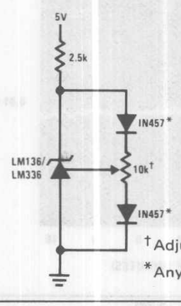


Typical Applications

2.5V Reference



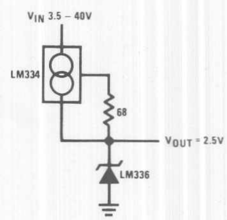
2.5V Reference with Minimum Temperature Coefficient



†Adjust to 2.490V

*Any silicon signal diode

Wide Input Range Reference



Absolute Maximum Ratings

Reverse Current	15 mA
Forward Current	10 mA
Storage Temperature	-60°C to $+150^\circ$C
Operating Temperature	
LM136	-55°C to $+150^\circ$C
LM236	-25°C to $+85^\circ$C
LM336	0°C to $+70^\circ$C
Lead Temperature (Soldering, 10 seconds)	300°C

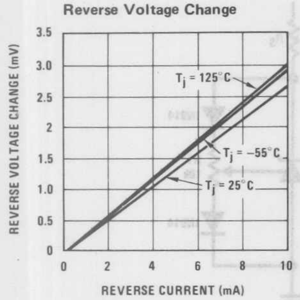
Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	LM136A/LM236A LM136/LM236			LM336B LM336			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reverse Breakdown Voltage	$T_A = 25^\circ$C, $I_R = 1$ mA							
	LM136/LM236/LM336	2.440	2.490	2.540	2.390	2.490	2.590	V
	LM136A/LM236A, LM336B	2.465	2.490	2.515	2.440	2.490	2.540	V
Reverse Breakdown Change With Current	$T_A = 25^\circ$C, $400\ \mu A \leq I_R \leq 10$ mA		2.6	6		2.6	10	mV
Reverse Dynamic Impedance	$T_A = 25^\circ$C, $I_R = 1$ mA		0.2	0.6		0.2	1	Ω
Temperature Stability	V_R Adjusted to 2.490V, $I_R = 1$ mA, *(Figure 2)*							
	$0^\circ C \leq T_A \leq 70^\circ C$ (LM336)					1.8	6	mV
	$-25^\circ C \leq T_A \leq +85^\circ C$ (LM236)		3.5	9				mV
	$-55^\circ C \leq T_A \leq +125^\circ C$ (LM136)		12	18				mV
Reverse Breakdown Change With Current	$400\ \mu A \leq I_R \leq 10$ mA		3	10		3	12	mV
Reverse Dynamic Impedance	$I_R = 1$ mA		0.4	1		0.4	1.4	Ω
Long Term Stability	$T_A = 25^\circ C \pm 0.1^\circ C$, $I_R = 1$ mA		20			20		ppm

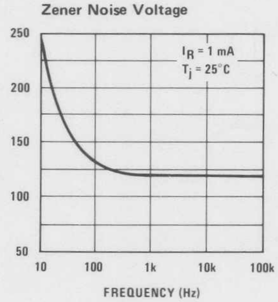
Note 1: Unless otherwise specified, the LM136 is specified from $-55^\circ C \leq T_A \leq +125^\circ C$, the LM236 from $-25^\circ C \leq T_A \leq +85^\circ C$ and the LM336 from $0^\circ C \leq T_A \leq +70^\circ C$. The maximum junction temperature of the LM136 is 150°C, LM236 is 125°C and the LM336 is 100°C. For elevated junction temperature, devices in the TO-46 package should be derated based on a thermal resistance of 440°C/W junction to ambient or 80°C/W junction to case. For the TO-92 package, the derating is based on 180°C/W junction to ambient with 0.4" leads from a PC board and 160°C/W junction to ambient with 0.125" lead length to a PC board.

Typical Performance Characteristics

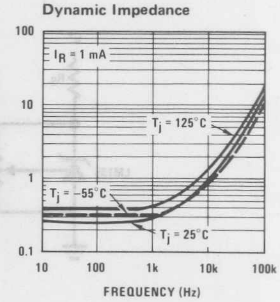
Reverse Voltage Change



Zener Noise Voltage



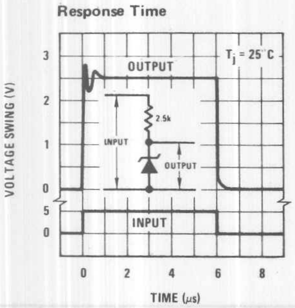
Dynamic Impedance

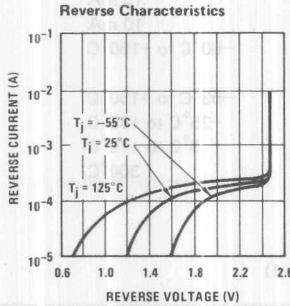


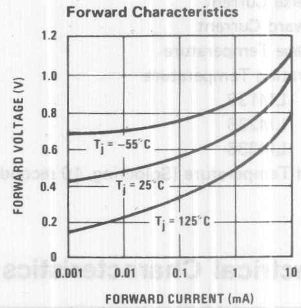
LM136/LM236/LM336

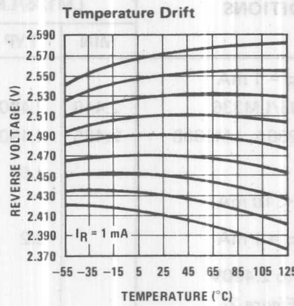
2

Typical Performance Characteristics (Continued)









Application Hints

The LM136 series voltage references are much easier to use than ordinary zener diodes. Their low impedance and wide operating current range simplify biasing in almost any circuit. Further, either the breakdown voltage or the temperature coefficient can be adjusted to optimize circuit performance.

Figure 1 shows an LM136 with a 10k potentiometer for adjusting the reverse breakdown voltage. With the addition of R1 the breakdown voltage can be adjusted without affecting the temperature coefficient of the device. The adjustment range is usually sufficient to adjust for both the initial device tolerance and inaccuracies in buffer circuitry.

If minimum temperature coefficient is desired, two diodes can be added in series with the adjustment potentiometer as shown in *Figure 2*. When the device is adjusted to 2.490V the temperature coefficient is minimized. Almost any silicon signal diode can be used for this purpose such as a 1N914, 1N4148 or a 1N457. For proper temperature compensation the diodes should be in the same thermal environment as the LM136. It is usually sufficient to mount the diodes near the LM136 on the printed circuit board. The absolute resistance of R1 is not critical and any value from 2k to 20k will work.

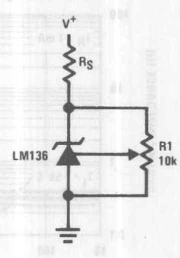


FIGURE 1. LM136 With Pot for Adjustment of Breakdown Voltage

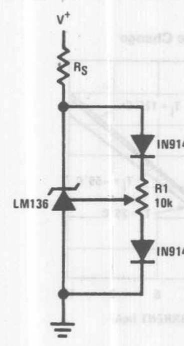
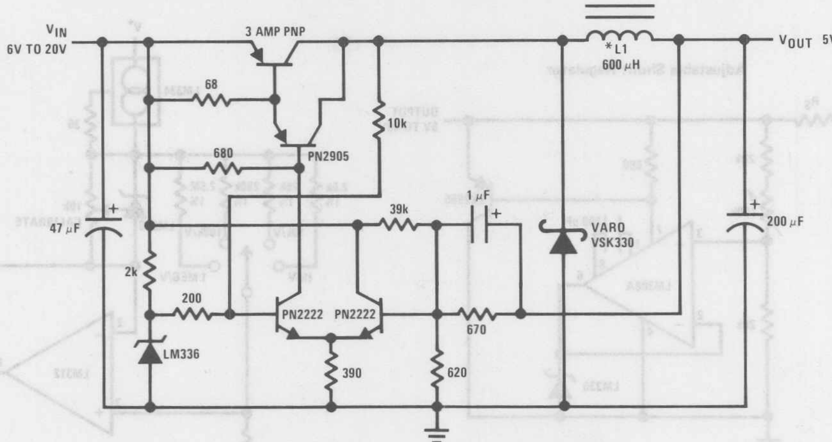


FIGURE 2. Temperature Coefficient Adjustment

Typical Applications (Continued)

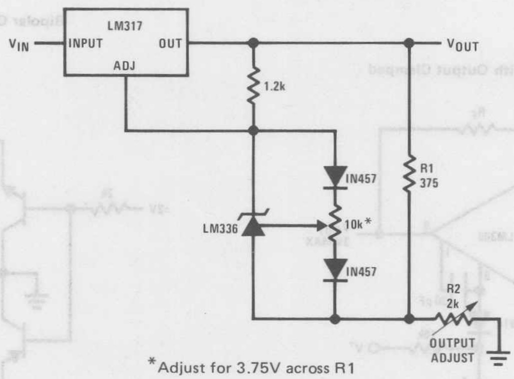
Low Cost 2 Amp Switching Regulator†



*L1 60 turns #16 wire on Arnold Core A-254168-2

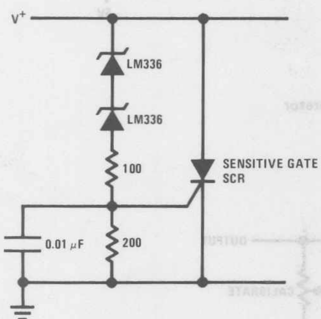
†Efficiency ≈ 80%

Precision Power Regulator with Low Temperature Coefficient

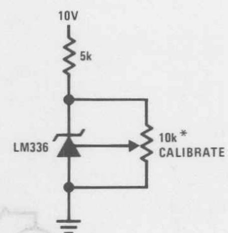


*Adjust for 3.75V across R1

5V Crowbar

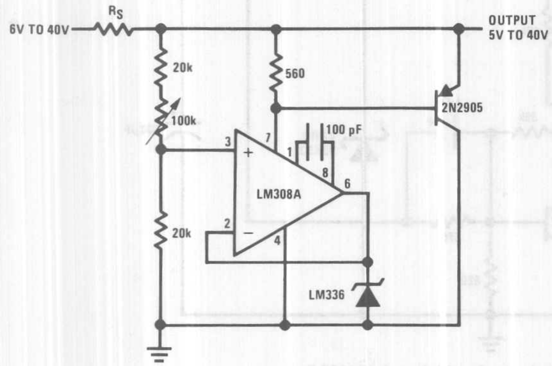


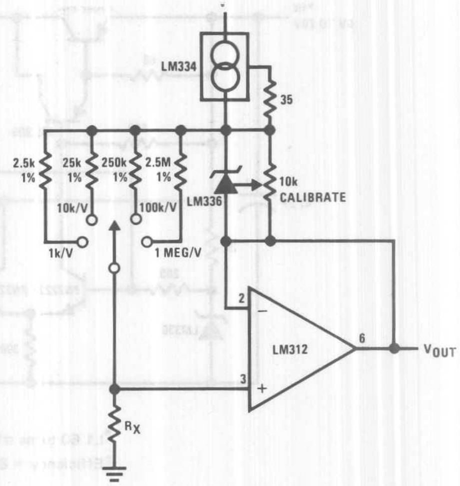
Trimmed 2.5V Reference with Temperature Coefficient Independent of Breakdown Voltage



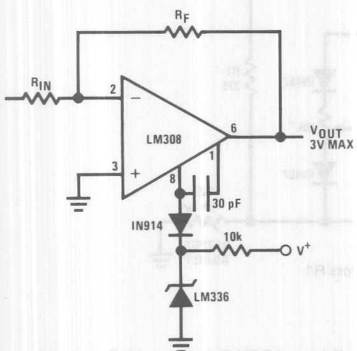
*Does not affect temperature coefficient

Adjustable Shunt Regulator

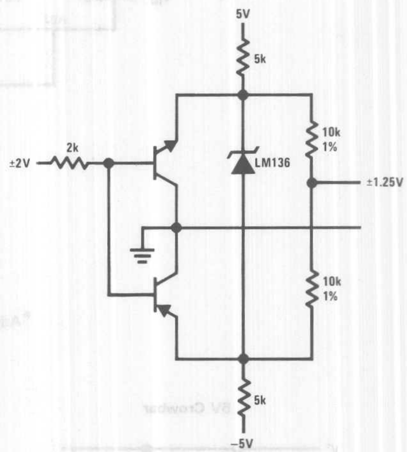




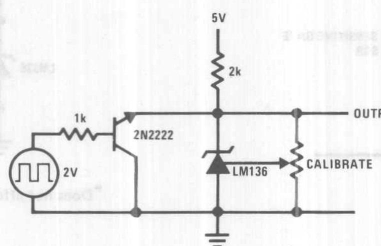
Op Amp with Output Clamped



Bipolar Output Reference

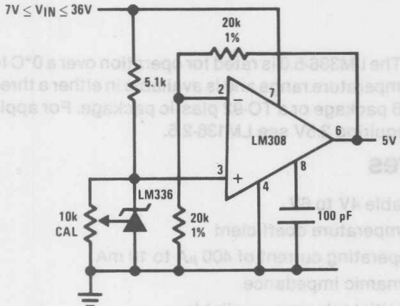


2.5V Square Wave Calibrator

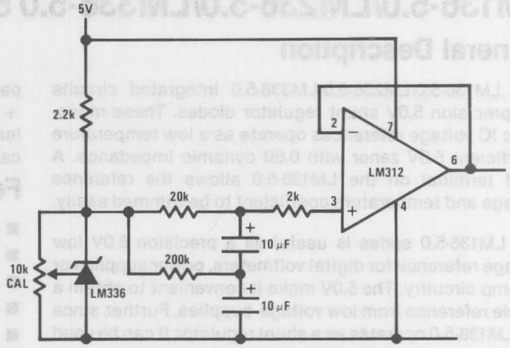


Typical Applications (Continued)

5V Buffered Reference

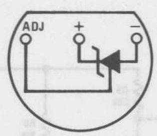


Low Noise Buffered Reference



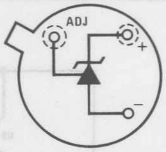
Connection Diagrams

TO-92
Plastic Package



Order Number
LM336Z-2.5 or LM336BZ-2.5
See Package Z03A

TO-46
Metal Can Package



Order Number
LM136H-2.5, LM236H-2.5, LM336H-2.5, LM136AH-2.5,
LM236AH-2.5 or LM336BH-2.5
See Package H03H

National Semiconductor

LM136-5.0/LM236-5.0/LM336-5.0 5.0V Reference Diode

General Description

The LM136-5.0/LM236-5.0/LM336-5.0 integrated circuits are precision 5.0V shunt regulator diodes. These monolithic IC voltage references operate as a low temperature coefficient 5.0V zener with 0.6Ω dynamic impedance. A third terminal on the LM136-5.0 allows the reference voltage and temperature coefficient to be trimmed easily.

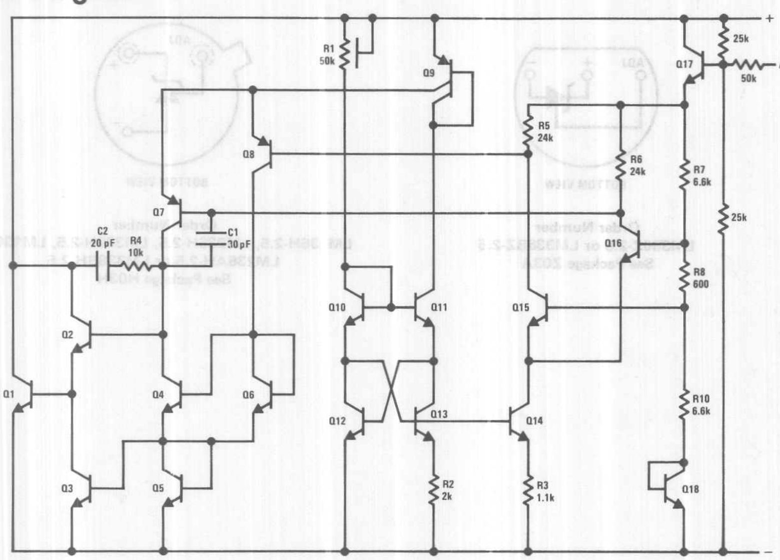
The LM136-5.0 series is useful as a precision 5.0V low voltage reference for digital voltmeters, power supplies or op amp circuitry. The 5.0V make it convenient to obtain a stable reference from low voltage supplies. Further, since the LM136-5.0 operates as a shunt regulator, it can be used as either a positive or negative voltage reference.

The LM136-5.0 is rated for operation over −55°C to +125°C while the LM236-5.0 is rated over a −25°C to +85°C temperature range. Both are packaged in a TO-46 package. The LM336-5.0 is rated for operation over a 0°C to +70°C temperature range and is available in either a three lead TO-46 package or a TO-92 plastic package. For applications requiring 2.5V see LM136-2.5.

Features

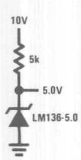
- Adjustable 4V to 6V
- Low temperature coefficient
- Wide operating current of 400 μA to 10 mA
- 0.6Ω dynamic impedance
- ±1% initial tolerance available
- Guaranteed temperature stability
- Easily trimmed for minimum temperature drift
- Fast turn-on
- Three lead transistor package

Schematic Diagram

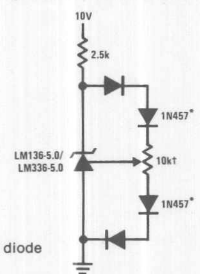


Typical Applications

5.0V Reference

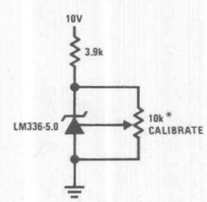


5.0V Reference with Minimum Temperature Coefficient



†Adjust to 5.00V
* Any silicon signal diode

Trimmed 4V to 6V Reference with Temperature Coefficient Independent of Breakdown Voltage



* Does not affect temperature coefficient

Absolute Maximum Ratings

Reverse Current	15 mA
Forward Current	10 mA
Storage Temperature	− 60°C to − 150°C
Operating Temperature	
LM136-5.0	− 55°C to − 150°C
LM236-5.0	− 25°C to + 85°C
LM336-5.0	0°C to + 70°C
Lead Temperature (Soldering, 10 seconds)	300°C

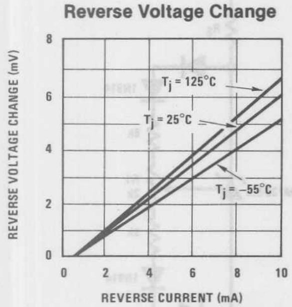
Electrical Characteristics (Note 1)

Parameter	Conditions	LM136A-5.0/LM236A-5.0 LM136-5.0/LM236-5.0			LM336B-5.0 LM336-5.0			Units
		Min	Typ	Max	Min	Typ	Max	
Reverse Breakdown Voltage	$T_A = 25°C$, $I_R = 1$ mA							
	LM136-5.0/LM236-5.0/LM336-5.0	4.9	5.00	5.1	4.8	5.00	5.2	V
	LM136A-5.0/LM236A-5.0, LM336B-5.0	4.95	5.00	5.05	4.90	5.00	5.1	V
Reverse Breakdown Change With Current	$T_A = 25°C$, $600\ \mu A \le I_R \le 10$ mA		6	12		6	20	mV
Reverse Dynamic Impedance	$T_A = 25°C$, $I_R = 1$ mA		0.6	1.2		0.6	2	Ω
Temperature Stability	V_R Adjusted 5.00V $I_R = 1$ mA, *(Figure 2)*							
	$0°C \le T_A \le 70°C$ (LM336-5.0)					4	12	mV
	$-25°C \le T_A \le +85°C$ (LM236-5.0)		7	18				mV
	$-55°C \le T_A \le +125°C$ (LM136-5.0)		20	36				mV
Reverse Breakdown Change With Current	$600\ \mu A \le I_R \le 10$ mA		6	17		6	24	mV
Adjustment Range			±1			±1		V
Reverse Dynamic Impedance	$I_R = 1$ mA		0.8	1.6		0.8	2.5	Ω
Long Term Stability	$T_A = 25°C \pm 0.1°C$, $I_R = 1$ mA		20			20		ppm

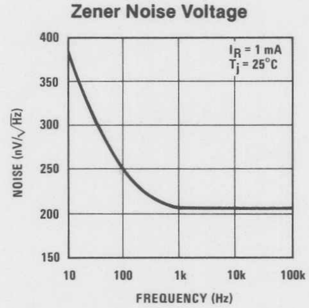
Note 1: Unless otherwise specified, the LM136-5.0 is specified from $-55°C \le T_A \le +125°C$, the LM236-5.0 from $-25°C \le T_A \le +85°C$ and the LM336-5.0 from $0°C \le T_A \le +70°C$.

Typical Performance Characteristics

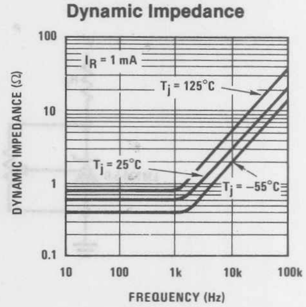
Reverse Voltage Change



Zener Noise Voltage

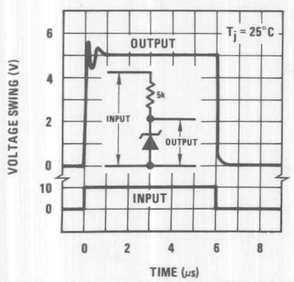


Dynamic Impedance

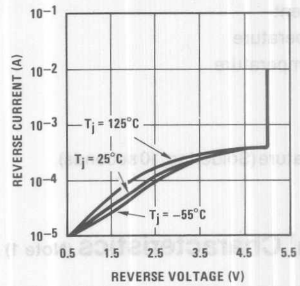


Typical Performance Characteristics (Continued)

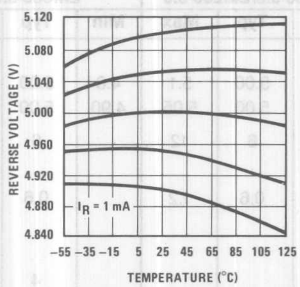
Response Time



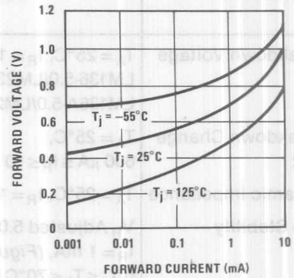
Reverse Characteristics



Temperature Drift



Forward Characteristics



Application Hints

The LM136-5.0 series voltage references are much easier to use than ordinary zener diodes. Their low impedance and wide operating current range simplify biasing in almost any circuit. Further, either the breakdown voltage or the temperature coefficient can be adjusted to optimize circuit performance.

Figure 1 shows an LM136-5.0 with a 10k potentiometer for adjusting the reverse breakdown voltage. With the addition of R1 the breakdown voltage can be adjusted without affecting the temperature coefficient of the device. The adjustment range is usually sufficient to adjust for both the initial device tolerance and inaccuracies in buffer circuitry.

If minimum temperature coefficient is desired, four diodes can be added in series with the adjustment potentiometer as shown in *Figure 2*. When the device is adjusted to 5.00V the temperature coefficient is minimized. Almost any silicon signal diode can be used for this purpose such as a 1N914, 1N4148 or a 1N457. For proper temperature compensation the diodes should be in the same thermal environment as the LM136-5.0. It is usually sufficient to mount the diodes near the LM136-5.0 on the printed circuit board. The absolute resistance of the network is not critical and any value from 2k to 20k will work. Because of the wide adjustment range, fixed resistors should be connected in series with the pot to make pot setting less critical.

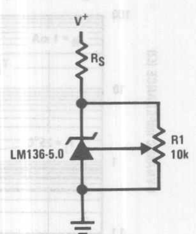


FIGURE 1. LM136-5.0 with Pot for Adjustment of Breakdown Voltage

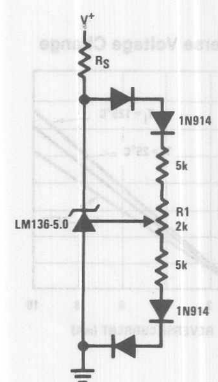
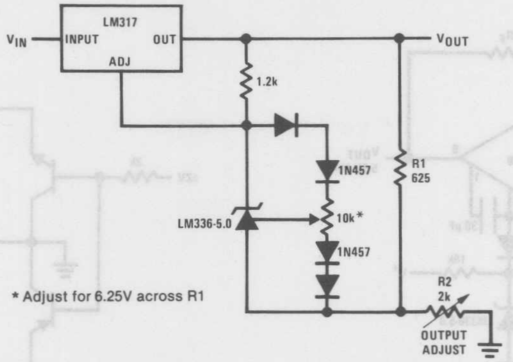
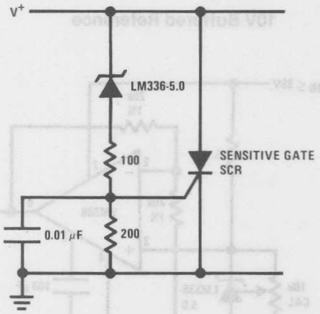


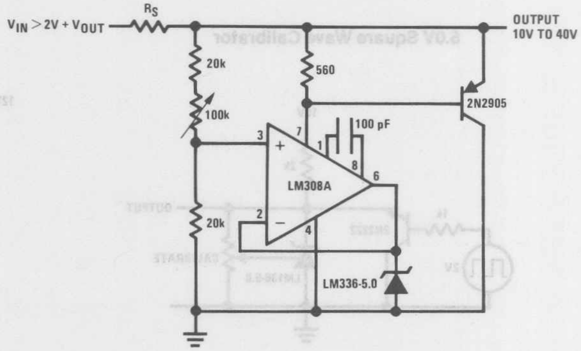
FIGURE 2. Temperature Coefficient Adjustment



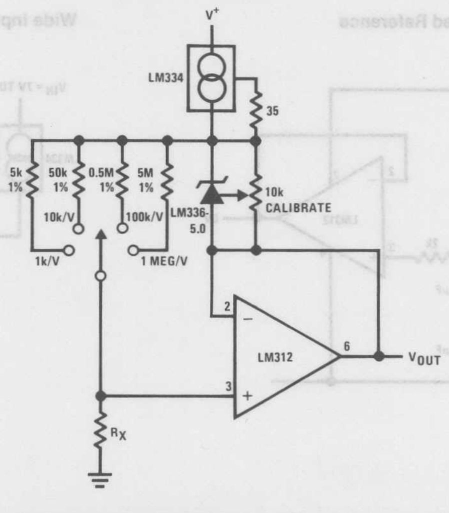
5V Crowbar



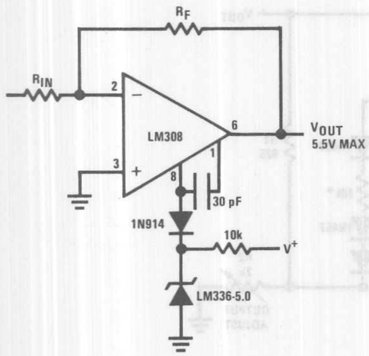
Adjustable Shunt Regulator



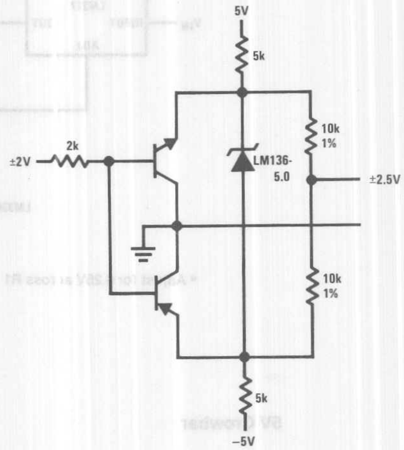
Linear Ohmmeter



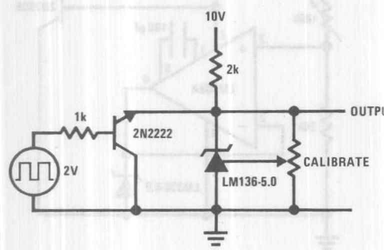
Op Amp with Output Clamped



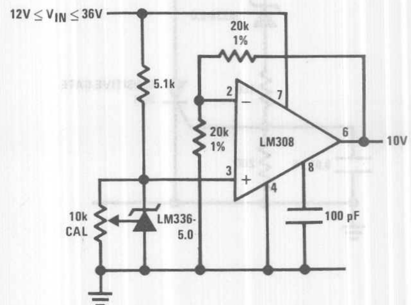
Bipolar Output Reference



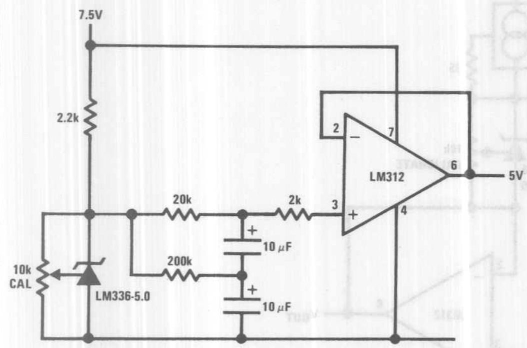
5.0V Square Wave Calibrator



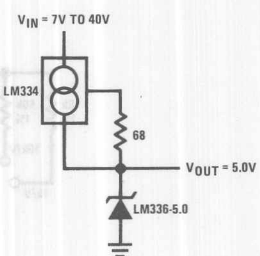
10V Buffered Reference



Low Noise Buffered Reference

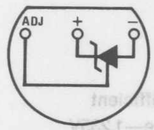


Wide Input Range Reference



Connection Diagrams

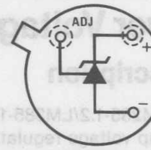
TO-92
Plastic Package



BOTTOM VIEW

Order Number LM336Z-5.0 or LM336BZ-5.0
NS Package Number Z03A

TO-46
Metal Can Package



BOTTOM VIEW

Order Number LM136H-5.0, LM236H-5.0, LM336H-5.0,
LM136AH-5.0, LM236AH-5.0 or LM336BH-5.0
NS Package Number H03H

National Semiconductor

LM185-1.2/LM285-1.2/LM385-1.2 Micropower Voltage Reference Diode

General Description

The LM185-1.2/LM285-1.2/LM385-1.2 are micropower 2-terminal band-gap voltage regulator diodes. Operating over a 10 μA to 20 mA current range, they feature exceptionally low dynamic impedance and good temperature stability. On-chip trimming is used to provide tight voltage tolerance. Since the LM185-1.2 band-gap reference uses only transistors and resistors, low noise and good long term stability result.

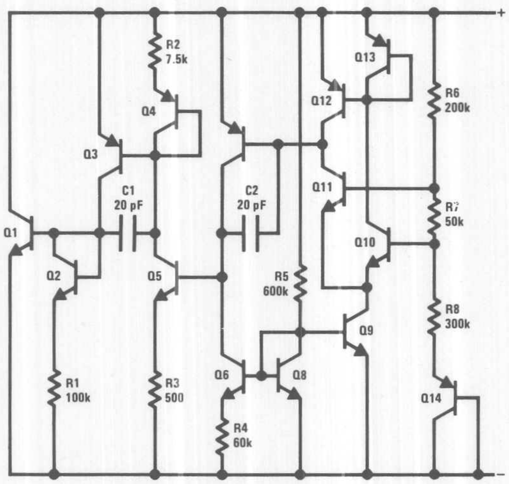
Careful design of the LM185-1.2 has made the device exceptionally tolerant of capacitive loading, making it easy to use in almost any reference application. The wide dynamic operating range allows its use with widely varying supplies with excellent regulation. Some outstanding features are:

- Operating current of 10 μA to 20 mA
- 1% and 2% initial tolerance
- 1Ω dynamic impedance
- Low temperature coefficient
- Low voltage reference—1.235V
- 2.5V device also available—LM385-2.5

The extremely low power drain of the LM185-1.2 makes it useful for micropower circuitry. This voltage reference can be used to make portable meters, regulators or general purpose analog circuitry with battery life approaching shelf life. Further, the wide operating current allows it to replace older references with a tighter tolerance part.

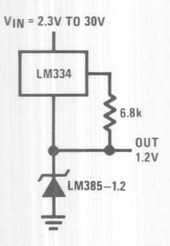
The LM185-1.2 is rated for operation over a −55°C to 125°C temperature range while the LM285-1.2 is rated −25°C to 85°C and the LM385-1.2 0°C to 70°C. The LM185-1.2/LM285-1.2/LM385-1.2 are available in a hermetic TO-46 package and the LM385-1.2 is also available in a low-cost TO-92 molded package.

Schematic Diagram

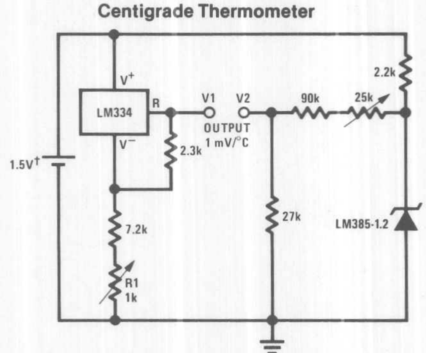


Applications

Wide Input Range Reference



Centigrade Thermometer



Calibration

1. Adjust R1 so that V1 = temp at 1 mV/°K
2. Adjust V2 to 273.2 mV

†I_Q for 1.3V to 1.6V battery voltage = 50 μA to 150 μA

Absolute Maximum Ratings

Reverse Current	30 mA
Forward Current	10 mA
Operating Temperature Range	
LM185-1.2	−55°C to +125°C
LM285-1.2	−25°C to +85°C
LM385-1.2	0°C to 70°C
Storage Temperature	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 1)

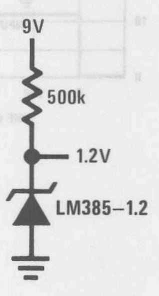
Parameter	Conditions	LM185-1.2/LM285-1.2			LM385-1.2/LM385B-1.2			Units
		Min	Typ	Max	Min	Typ	Max	
Reverse Breakdown Voltage	$T_A = 25°C$ $I_{MIN} \le I_R \le 20$ mA							
	LM185-1.2/LM285-1.2/LM385B-1.2	1.223	1.235	1.247	1.223	1.235	1.247	V
	LM385-1.2				1.205	1.235	1.260	V
Minimum Operating Current			8	10		8	15	μA
Reverse Breakdown Voltage Change with Current	$I_{MIN} \le I_R \le 1$ mA			1			1	mV
				1.5			**1.5**	mV
	$1\text{ mA} \le I_R \le 20$ mA			10			20	mV
				20			**25**	mV
Reverse Dynamic Impedance	$I_R = 100\ \mu A$		0.2	0.6		0.4	1	Ω
				1.5			**1.5**	Ω
Average Temperature Coefficient	$10\ \mu A \le I_R \le 20$ mA (Note 2)		20			20		ppm/°C
Wide Band Noise (RMS)	$I_R = 100\ \mu A$ $10\text{ Hz} \le f \le 10$ kHz		60			60		μV
Long Term Stability	$I_R = 100\ \mu A$ $T_A = 25°C \pm 0.1°C$		20			20		ppm/kHR

Note 1: Boldface type applies over the operating temperature range. Thermal resistance of the TO-46 package is 440°C/W junction to ambient or 80°C/W junction to case. Thermal resistance of the TO-92 package is 180°C/W junction to ambient.

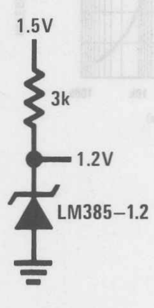
Note 2: Guaranteed maximum average temperature coefficient available as special order.

Applications (Continued)

Micropower Reference from 9V Battery



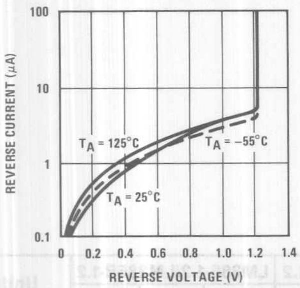
Reference from 1.5V Battery



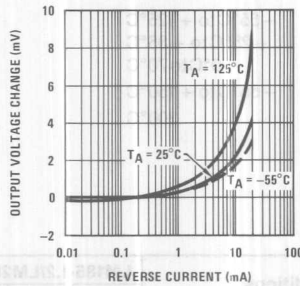
LM185-1.2/LM285-1.2/LM385-1.2

Typical Performance Characteristics

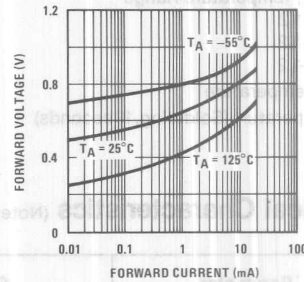
Reverse Characteristics



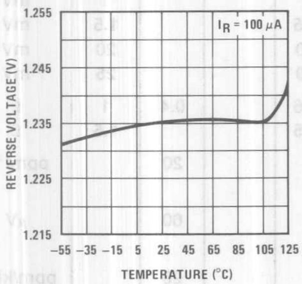
Reverse Characteristics



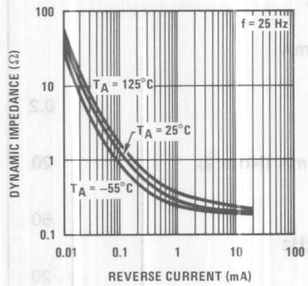
Forward Characteristics



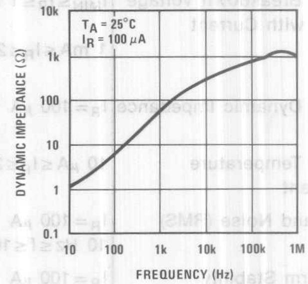
Temperature Drift



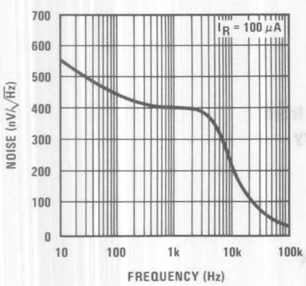
Reverse Dynamic Impedance



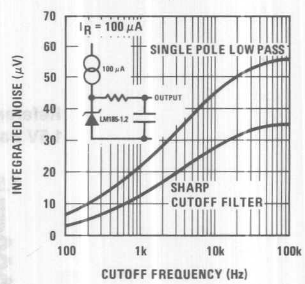
Reverse Dynamic Impedance



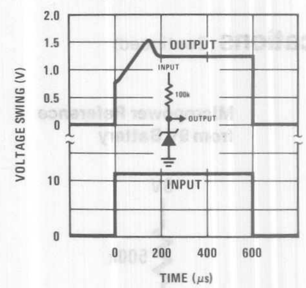
Noise Voltage



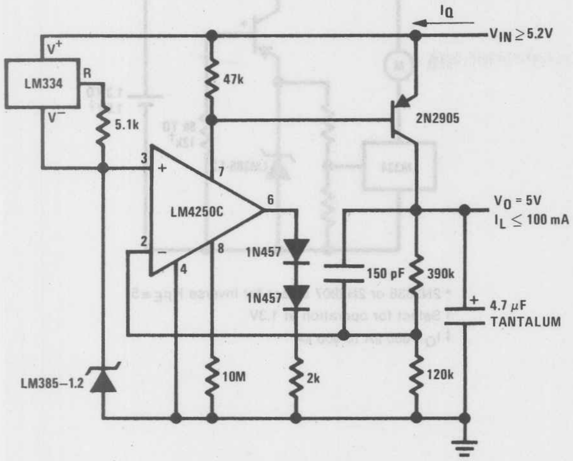
Filtered Output Noise



Response Time

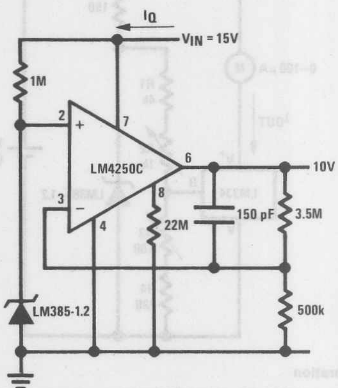


Micropower* 5V Regulator



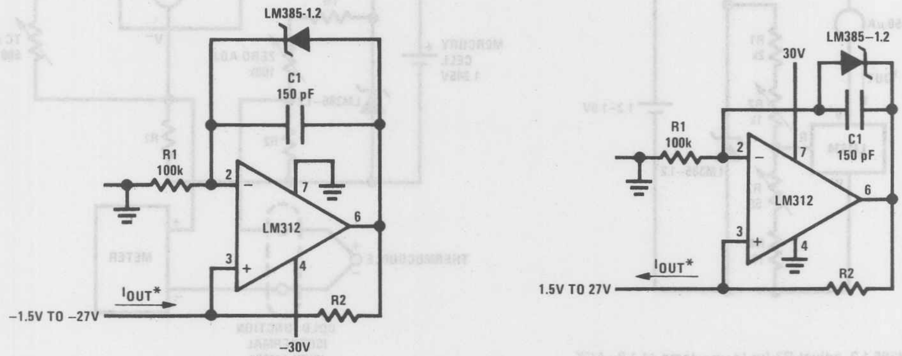
* $I_Q \cong 30\ \mu A$

Micropower* 10V Reference



* $I_Q \cong 20\ \mu A$ standby current

Precision 1 µA to 1 mA Current Sources

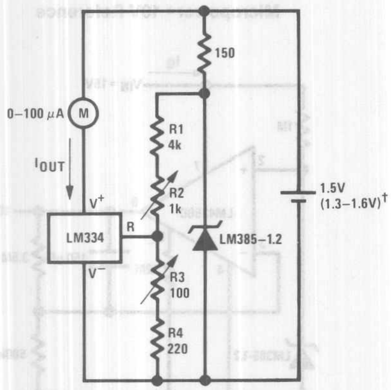


$$I_{OUT} = \frac{1.23V}{R2}$$

LM385 Applications (Continued)

METER THERMOMETERS

0°C–100°C Thermometer

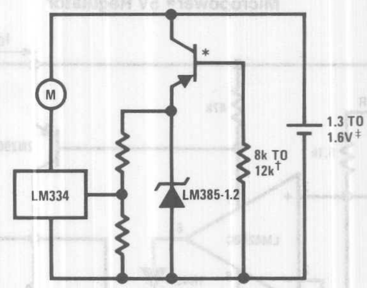


Calibration

1. Short LM385-1.2, adjust R3 for I_{OUT} = temp at 1 µA/°K
2. Remove short, adjust R2 for correct reading in centigrade

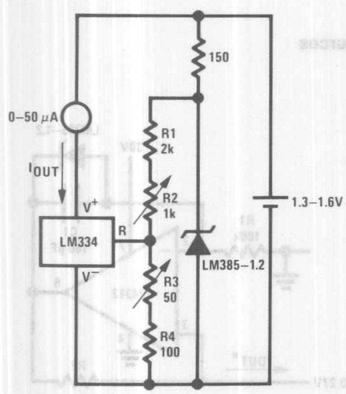
†I_Q at 1.3V ≅ 500 µA
I_Q at 1.6V ≅ 2.4 mA

Lower Power Thermometer



* 2N3638 or 2N2907 select for inverse H_{FE} ≅ 5
† Select for operation at 1.3V
‡ I_Q ≅ 600 µA to 900 µA

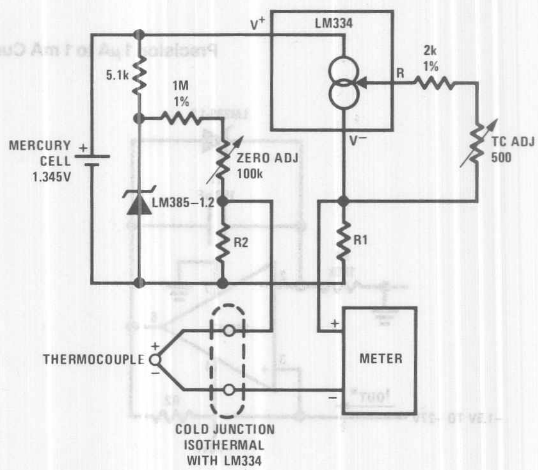
0°F–50°F Thermometer



Calibration

1. Short LM385-1.2, adjust R3 for I_{OUT} = temp at 1.8 µA/°K
2. Remove short, adjust R2 for correct reading in °F

Micropower Thermocouple Cold Junction Compensator



Adjustment Procedure

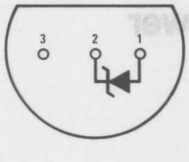
1. Adjust TC ADJ pot until voltage across R1 equals kelvin temperature multiplied by the thermocouple seebeck coefficient.
2. Adjust zero ADJ pot until voltage across R2 equals the thermocouple seedbeck coefficient multiplied by 273.2.

Thermocouple Type	Seebeck Coefficient (µV/°C)	R1 (Ω)	R2 (Ω)	Voltage Across R1 @25°C (mV)	Voltage Across R2 (mV)
J	52.3	523	1.24k	15.60	14.32
T	42.8	432	1k	12.77	11.78
K	40.8	412	953Ω	12.17	11.17
S	6.4	63.4	150Ω	1.908	1.766

Typical supply current 50 µA

Connection Diagrams

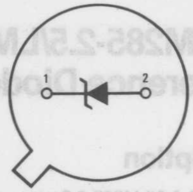
TO-92
Plastic Package



BOTTOM VIEW

Order Number LM385Z-1.2 or LM385BZ-1.2
NS Package Number Z03D

TO-46
Metal Can Package



BOTTOM VIEW

Order Number LM185H-1.2, LM285H-1.2,
LM385H-1.2 or LM385BH-1.2
NS Package Number H03A

LM185-2.5/LM285-2.5/LM385-2.5 Micropower Voltage Reference Diode

General Description

The LM185-2.5/LM285-2.5/LM385-2.5 are micropower 2-terminal band-gap voltage regulator diodes. Operating over a 20 μA to 20 mA current range, they feature exceptionally low dynamic impedance and good temperature stability. On-chip trimming is used to provide tight voltage tolerance. Since the LM185-2.5 band-gap reference uses only transistors and resistors, low noise and good long term stability result.

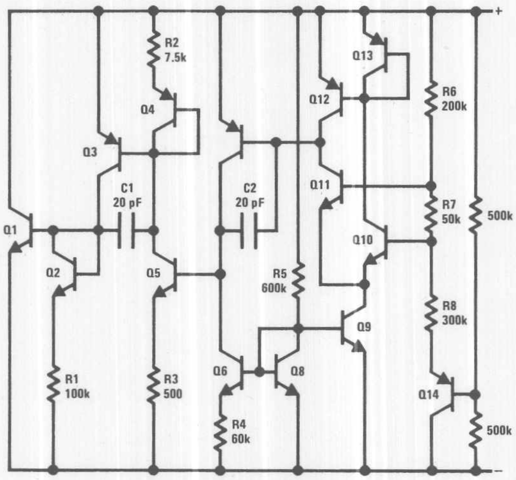
Careful design of the LM185-2.5 has made the device exceptionally tolerant of capacitive loading, making it easy to use in almost any reference application. The wide dynamic operating range allows its use with widely varying supplies with excellent regulation. Some outstanding features are:

- Operating current of 20 μA to 20 mA
- 1.5% and 3% initial tolerance
- 1Ω dynamic impedance
- Low temperature coefficient
- Low voltage reference—2.5V

The extremely low power drain of the LM185-2.5 makes it useful for micropower circuitry. This voltage reference can be used to make portable meters, regulators or general purpose analog circuitry with battery life approaching shelf life. Further, the wide operating current allows it to replace older references with a tighter tolerance part. For applications requiring 1.2V see LM185-1.2.

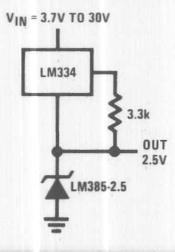
The LM185-2.5 is rated for operation over a −55°C to 125°C temperature range while the LM285-2.5 is rated −25°C to 85°C and the LM385-2.5 0°C to 70°C. The LM185-2.5/LM285-2.5/LM385-2.5 are available in a hermetic TO-46 package and the LM385-2.5 is also available in a low-cost TO-92 molded package.

Schematic Diagram



Applications

Wide Input Range Reference



Absolute Maximum Ratings

Reverse Current	30 mA
Forward Current	10 mA
Operating Temperature Range	
LM185-2.5	−55°C to +125°C
LM285-2.5	−25°C to +85°C
LM385-2.5	0°C to 70°C
Storage Temperature	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 1)

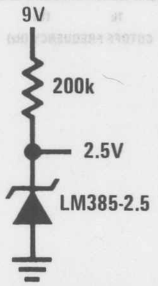
Parameter	Conditions	LM185-2.5/LM285-2.5			LM385-2.5/LM385B-2.5			Units
		Min	Typ	Max	Min	Typ	Max	
Reverse Breakdown Voltage	$T_A = 25°C$, $I_{MIN} \le I_R \le 20$ mA							
	LM185-2.5/LM285-2.5/ LM385B-2.5	2.462	2.5	2.538	2.462	2.5	2.538	V
	LM385-2.5				2.425	2.5	2.575	V
Minimum Operating Current			8	**20**		8	**20**	µA
Reverse Breakdown Voltage Change with Current	$20\ \mu A \le I_R \le 1$ mA			1			2	mV
				1.5			**2.5**	mV
	$1\ mA \le I_R \le 20$ mA			10			20	mV
				20			**25**	mV
Reverse Dynamic Impedance	$I_R = 100\ \mu A$		0.2	0.6		0.4	1	Ω
				1.5			**1.5**	Ω
Average Temperature Coefficient (Note 2)	$20\ \mu A \le I_R \le 20$ mA		20			20		ppm/°C
Wide Band Noise (RMS)	$I_R = 100\ \mu A$, $10\ Hz \le f \le 10$ kHz		120			120		µV
Long Term Stability	$I_R = 100\ \mu A$, $T_A = 25°C \pm 0.1°C$		20			20		ppm/kHR

Note 1: Boldface type applies over the operating temperature range. Thermal resistance of the TO-46 package is 440°C/W junction to ambient or 80°C junction to case. Thermal resistance of the TO-92 package is 180°C/W junction to ambient.

Note 2: Guaranteed maximum average temperature coefficient available as special order.

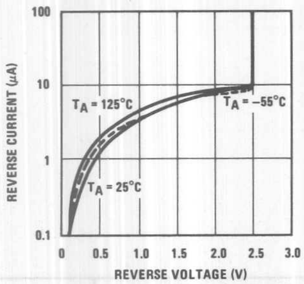
Applications (Continued)

Micropower Reference from 9V Battery

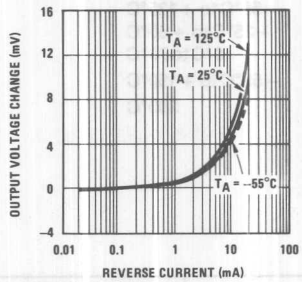


Typical Performance Characteristics

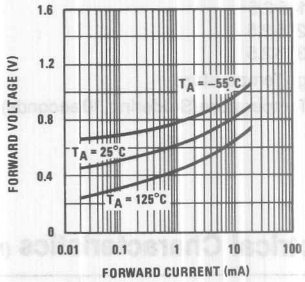
Reverse Characteristics



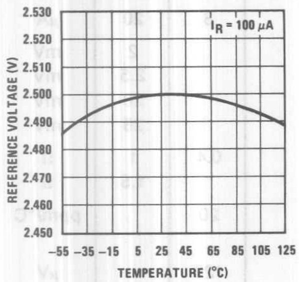
Reverse Characteristics



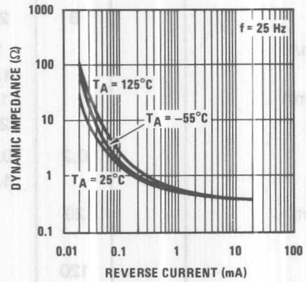
Forward Characteristics



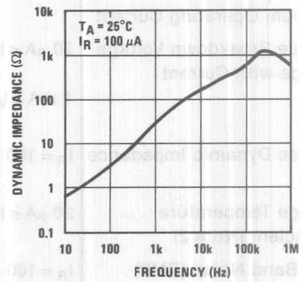
Temperature Drift



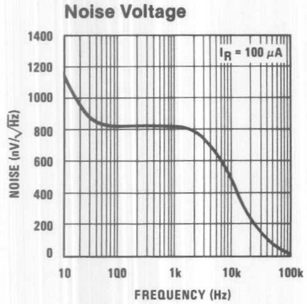
Reverse Dynamic Impedance



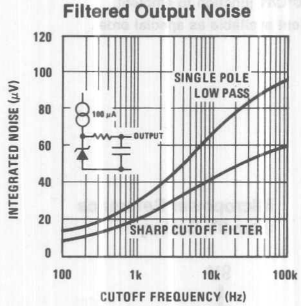
Reverse Dynamic Impedance



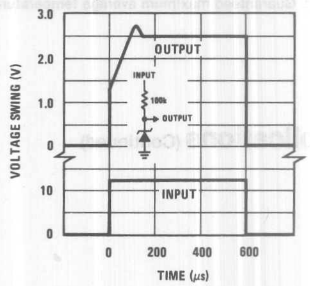
Noise Voltage



Filtered Output Noise

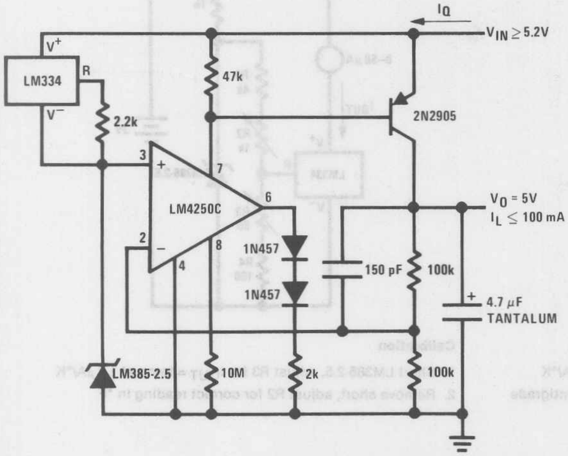


Response Time



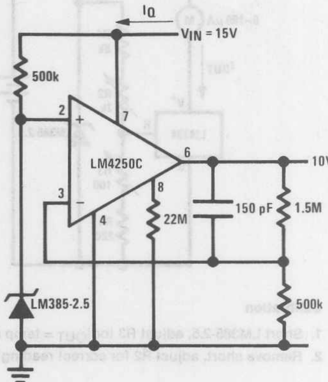
LM385-2.5 Applications

Micropower* 5V Regulator



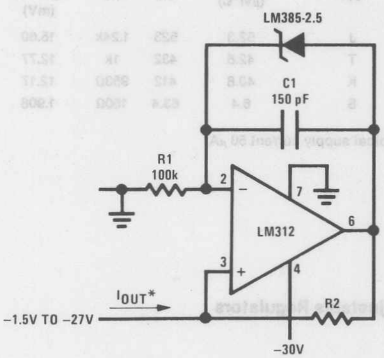
* $I_Q \cong 40\ \mu A$

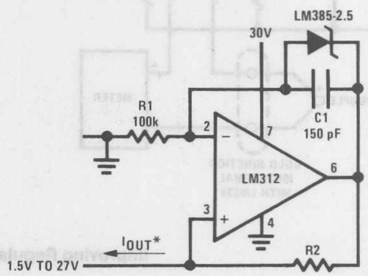
Micropower* 10V Reference



* $I_Q \cong 30\ \mu A$ standby current

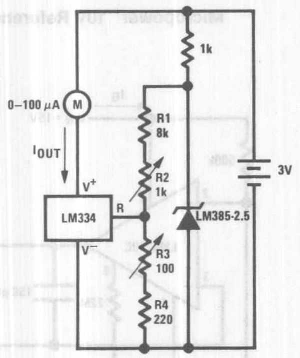
Precision 1 µA to 1 mA Current Sources





$$* I_{OUT} = \frac{2.5V}{R2}$$

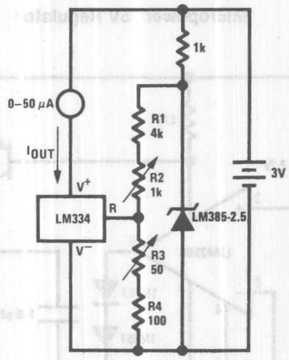
0°C–100°C Thermometer



Calibration

1. Short LM385-2.5, adjust R3 for I_{OUT} = temp at 1μA/°K
2. Remove short, adjust R2 for correct reading in centigrade

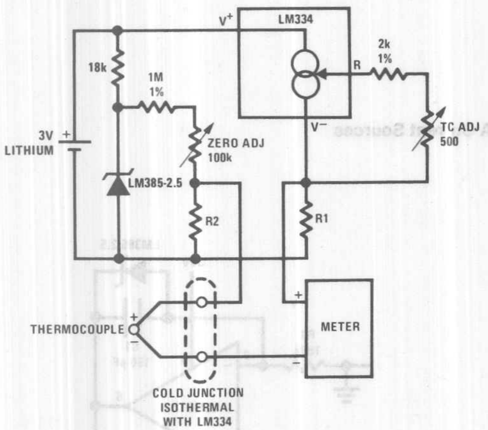
0°F–50°F Thermometer



Calibration

1. Short LM385-2.5, adjust R3 for I_{OUT} = temp at 1.8 μA/°K
2. Remove short, adjust R2 for correct reading in °F

Micropower Thermocouple Cold Junction Compensator



Adjustment Procedure

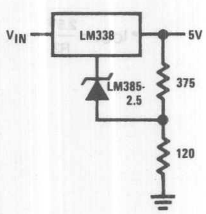
1. Adjust TC ADJ pot until voltage across R1 equals Kelvin temperature multiplied by the thermocouple Seebeck coefficient.

2. Adjust zero ADJ pot until voltage across R2 equals the thermocouple Seebeck coefficient multiplied by 273.2.

Thermocouple Type	Seebeck Coefficient (μV/°C)	R1 (Ω)	R2 (Ω)	Voltage Across R1 @25°C (mV)	Voltage Across R2 (mV)
J	52.3	523	1.24k	15.60	14.32
T	42.8	432	1k	12.77	11.78
K	40.8	412	953Ω	12.17	11.17
S	6.4	63.4	150Ω	1.908	1.766

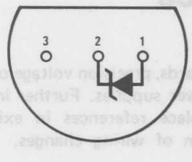
Typical supply current 50 μA

Improving Regulation of Adjustable Regulators



Connection Diagrams

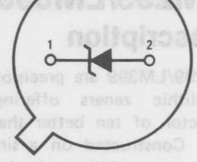
TO-92
Plastic Package



BOTTOM VIEW

Order Number LM385Z-2.5 or LM385BZ-2.5
NS Package Number Z03D

TO-46
Metal Can Package



BOTTOM VIEW

Order Number LM185H-2.5, LM285H-2.5, LM385H-2.5 or LM385BH-2.5
NS Package Number H03A

National Semiconductor

LM199/LM299/LM399 Precision Reference

General Description

The LM199/LM299/LM399 are precision, temperature-stabilized monolithic zeners offering temperature coefficients a factor of ten better than high quality reference zeners. Constructed on a single monolithic chip is a temperature stabilizer circuit and an active reference zener. The active circuitry reduces the dynamic impedance of the zener to about 0.5Ω and allows the zener to operate over 0.5 mA to 10 mA current range with essentially no change in voltage or temperature coefficient. Further, a new subsurface zener structure gives low noise and excellent long term stability compared to ordinary monolithic zeners. The package is supplied with a thermal shield to minimize heater power and improve temperature regulation.

The LM199 series references are exceptionally easy to use and free of the problems that are often experienced with ordinary zeners. There is virtually no hysteresis in reference voltage with temperature cycling. Also, the LM199 is free of voltage shifts due to stress on the leads. Finally, since the unit is temperature stabilized, warm up time is fast.

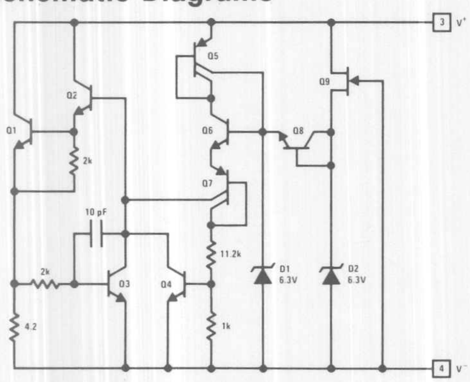
The LM199 can be used in almost any application in place of ordinary zeners with improved performance. Some ideal applications are analog to digital converters, calibration standards, precision voltage or current sources or precision power supplies. Further in many cases the LM199 can replace references in existing equipment with a minimum of wiring changes.

The LM199 series devices are packaged in a standard hermetic TO-46 package inside a thermal shield. The LM199 is rated for operation from −55°C to +125°C while the LM299 is rated for operation from −25°C to +85°C and the LM399 is rated from 0°C to +70°C.

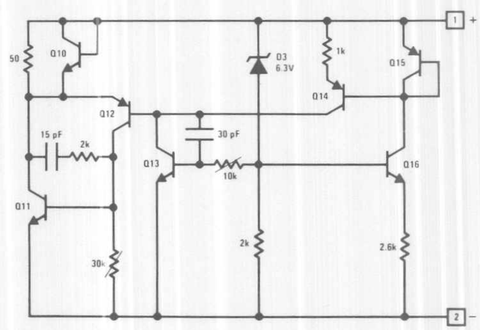
Features

- Guaranteed 0.0001%/°C temperature coefficient
- Low dynamic impedance – 0.5Ω
- Initial tolerance on breakdown voltage – 2%
- Sharp breakdown at 400μA
- Wide operating current – 500μA to 10 mA
- Wide supply range for temperature stabilizer
- Guaranteed low noise
- Low power for stabilization – 300 mW at 25°C
- Long term stability – 20 ppm

Schematic Diagrams



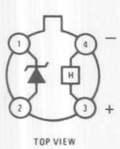
Temperature Stabilizer



Reference

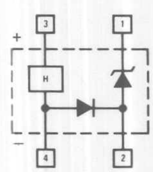
Connection Diagram

Metal Can Package



Order Number LM199H, LM299H or LM399H
See Package H04A

Functional Block Diagram



Reverse Breakdown Current	20 mA
Forward Current	1 mA
Reference to Substrate Voltage $V_{(RS)}$ (Note 1)	40V
	−0.1V
Operating Temperature Range	
LM199	−55°C to +125°C
LM299	−25°C to +85°C
LM399	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

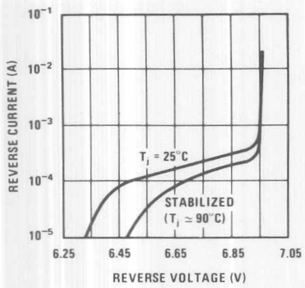
Electrical Characteristics (Note 2)

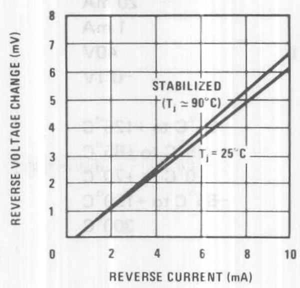
PARAMETER	CONDITIONS		LM199/LM299			LM399			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Reverse Breakdown Voltage	$0.5\text{ mA} \le I_R \le 10\text{ mA}$		6.8	6.95	7.1	6.6	6.95	7.3	V
Reverse Breakdown Voltage Change With Current	$0.5\text{ mA} \le I \le 10\text{ mA}$			6	9		6	12	mV
Reverse Dynamic Impedance	$I_R = 1\text{ mA}$			0.5	1		0.5	1.5	Ω
Reverse Breakdown Temperature Coefficient	$-55°C \le T_A \le 85°C$	LM199		0.00003	0.0001				%/°C
	$85°C \le T_A \le 125°C$	LM199		0.0005	0.0015				%/°C
	$-25°C \le T_A \le 85°C$	LM299		0.00003	0.0001				%/°C
	$0°C \le T_A \le 70°C$	LM399					0.00003	0.0002	%/°C
RMS Noise	$10\text{ Hz} \le f \le 10\text{ kHz}$			7	20		7	50	µV
Long Term Stability	Stabilized, $22°C \le T_A \le 28°C$, 1000 Hours, $I_R = 1\text{ mA} \pm 0.1\%$			20			20		ppm
Temperature Stabilizer Supply Current	$T_A = 25°C$, Still Air, $V_S = 30V$			8.5	14		8.5	15	mA
	$T_A = -55°C$			22	28				
Temperature Stabilizer Supply Voltage	(Note 3)		9		40	9		40	V
Warm-Up Time to 0.05%	$V_S = 30V$, $T_A = 25°C$			3			3		Seconds
Initial Turn-on Current	$9 \le V_S \le 40$, $T_A = 25°C$, (Note 3)			140	200		140	200	mA

Note 1: The substrate is electrically connected to the negative terminal of the temperature stabilizer. The voltage that can be applied to either terminal of the reference is 40V more positive or 0.1V more negative than the substrate.

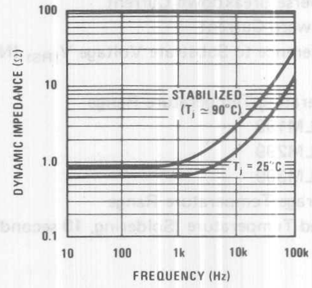
Note 2: These specifications apply for 30V applied to the temperature stabilizer and $-55°C \le T_A \le +125°C$ for the LM199; $-25°C \le T_A \le +85°C$ for the LM299 and $0°C \le T_A \le +70°C$ for the LM399.

Note 3: This initial current can be reduced by adding an appropriate resistor and capacitor to the heater circuit. See the performance characteristic graphs to determine values.

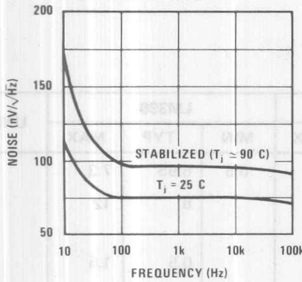




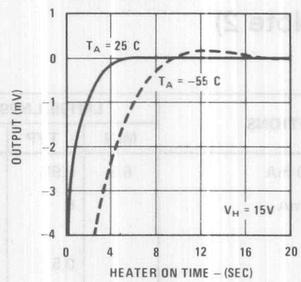
Dynamic Impedance



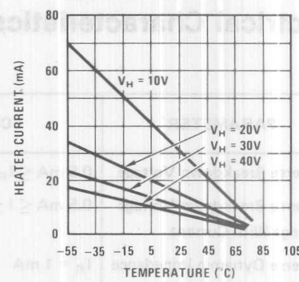
Zener Noise Voltage



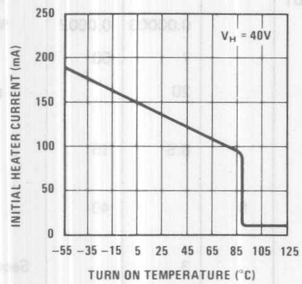
Stabilization Time



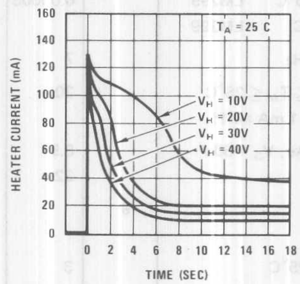
Heater Current



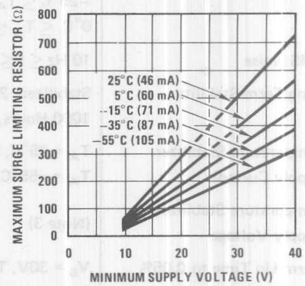
Initial Heater Current



Heater Current (To Limit This Surge, See Next Graph)

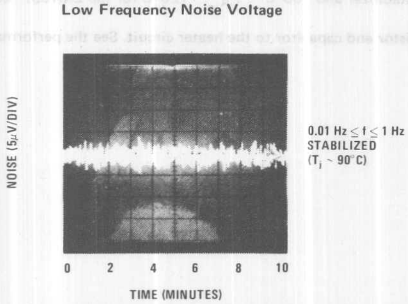


Heater Surge Limit Resistor vs Minimum Supply Voltage at Various Minimum Temperatures

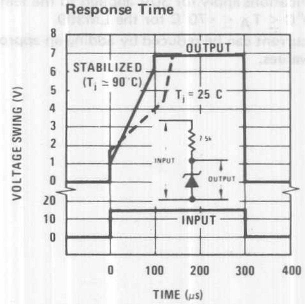


*Heater must be bypassed with a 2 μF or larger tantalum capacitor if resistors are used.

Low Frequency Noise Voltage

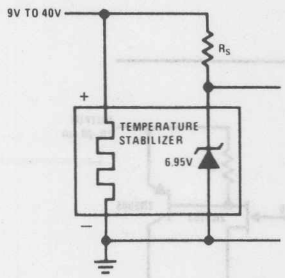


Response Time

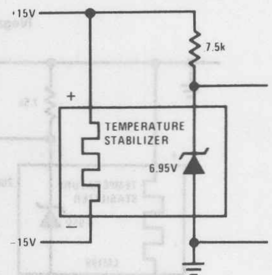


Typical Applications

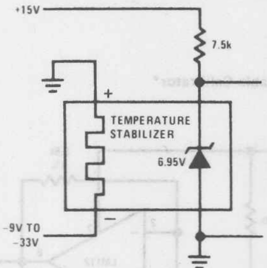
Single Supply Operation



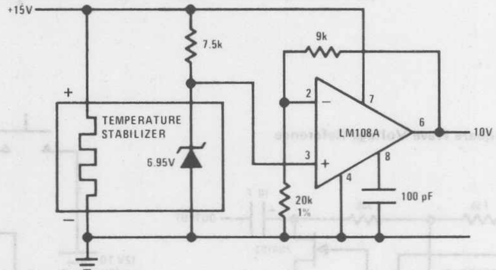
Split Supply Operation



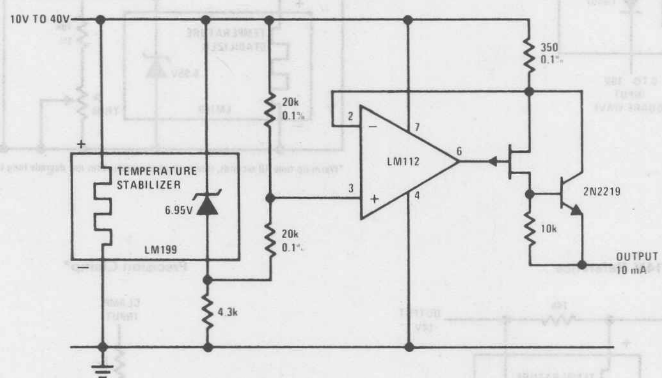
Negative Heater Supply with Positive Reference



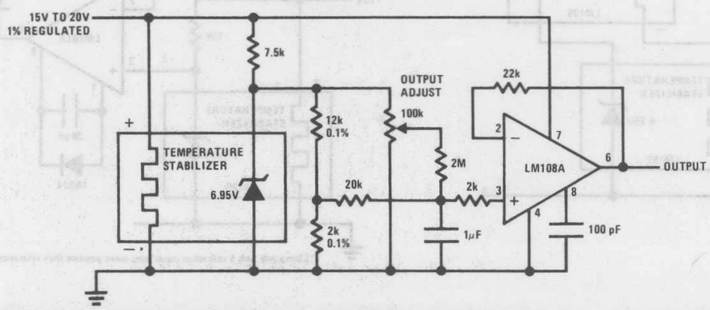
Buffered Reference With Single Supply



Positive Current Source

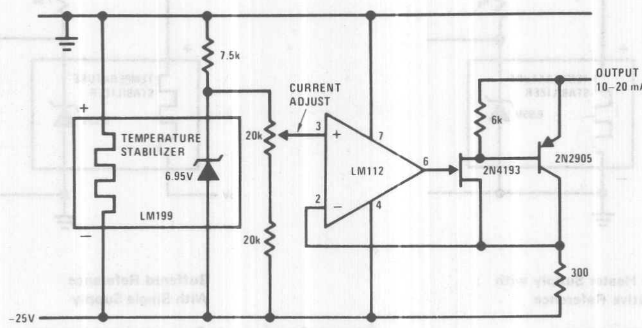


Standard Cell Replacement

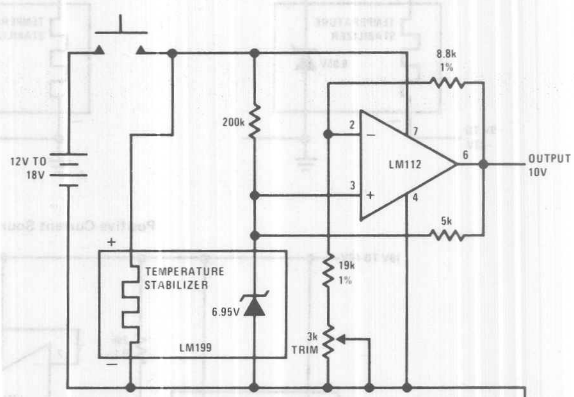


Typical Applications (cont'd.)

Negative Current Source

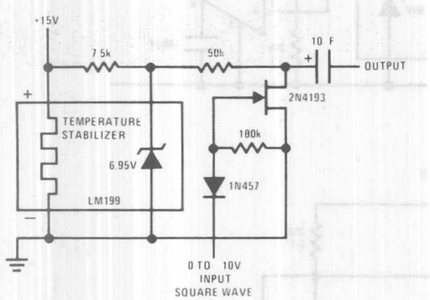


Portable Calibrator*

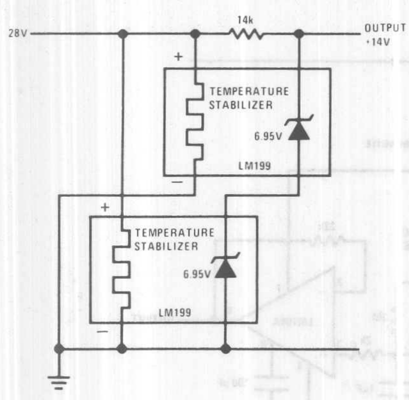


*Warm-up time 10 seconds; intermittant operation does not degrade long term stability.

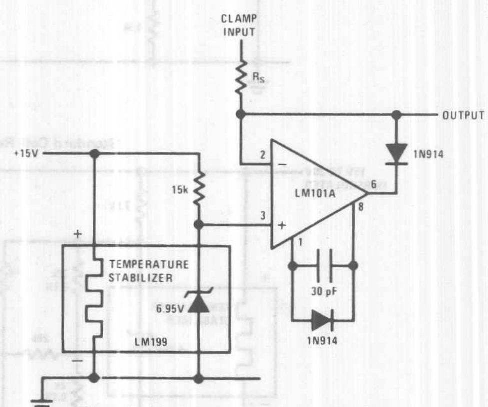
Square Wave Voltage Reference



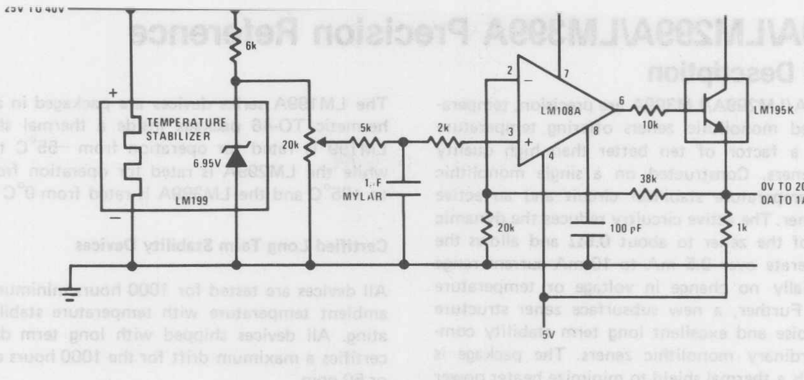
14V Reference



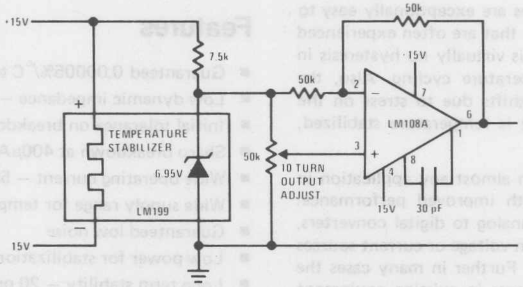
Precision Clamp*



*Clamp will sink 5 mA when input goes more positive than reference.



Bipolar Output Reference



LM199A/LM299A/LM399A Precision Reference

General Description

The LM199A/LM299A/LM399A are precision, temperature-stabilized monolithic zeners offering temperature coefficients a factor of ten better than high quality reference zeners. Constructed on a single monolithic chip is a temperature stabilizer circuit and an active reference zener. The active circuitry reduces the dynamic impedance of the zener to about 0.5Ω and allows the zener to operate over 0.5 mA to 10 mA current range with essentially no change in voltage or temperature coefficient. Further, a new subsurface zener structure gives low noise and excellent long term stability compared to ordinary monolithic zeners. The package is supplied with a thermal shield to minimize heater power and improve temperature regulation.

The LM199A series references are exceptionally easy to use and free of the problems that are often experienced with ordinary zeners. There is virtually no hysteresis in reference voltage with temperature cycling. Also, the LM199A is free of voltage shifts due to stress on the leads. Finally, since the unit is temperature stabilized, warm up time is fast.

The LM199A can be used in almost any application in place of ordinary zeners with improved performance. Some ideal applications are analog to digital converters, calibration standards, precision voltage or current sources or precision power supplies. Further in many cases the LM199A can replace references in existing equipment with a minimum of wiring changes.

The LM199A series devices are packaged in a standard hermetic TO-46 package inside a thermal shield. The LM199 is rated for operation from −55°C to +125°C while the LM299A is rated for operation from −25°C to +85°C and the LM399A is rated from 0°C to +70°C.

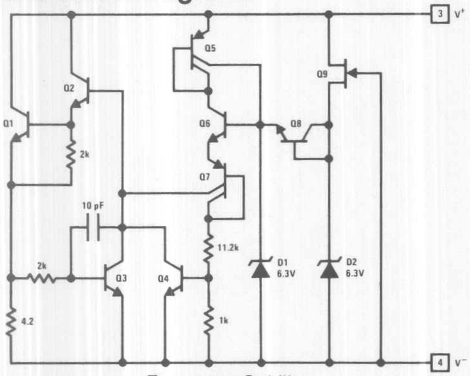
Certified Long Term Stability Devices

All devices are tested for 1000 hours minimum at 25°C ambient temperature with temperature stabilizer operating. All devices shipped with long term data which certifies a maximum drift for the 1000 hours of 20 ppm or 50 ppm.

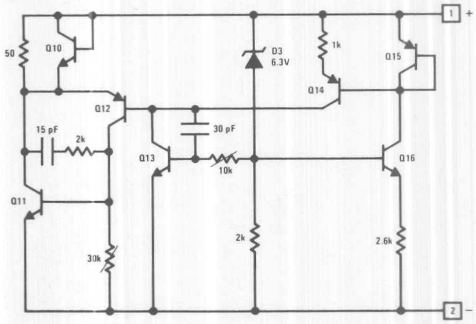
Features

- Guaranteed 0.00005%/°C temperature coefficient
- Low dynamic impedance — 0.5Ω
- Initial tolerance on breakdown voltage — 2%
- Sharp breakdown at 400μA
- Wide operating current — 500μA to 10 mA
- Wide supply range for temperature stabilizer
- Guaranteed low noise
- Low power for stabilization — 300 mW at 25°C
- Long term stability — 20 ppm
- Certified long term stability available

Schematic Diagrams



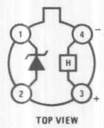
Temperature Stabilizer



Reference

Connection Diagram

Metal Can Package



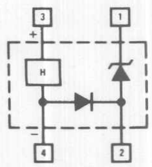
TOP VIEW

Order Number LM199AH, LM199AH-20, LM299AH, LM299AH-20, LM399AH or LM399AH-50
See NS Package H04D

Certified Long Term Stability Device

CERTIFIED LONG TERM STABILITY ppm MAX	ORDERING NUMBERS
20	LM199AH-20
20	LM299AH-20
50	LM399AH-50

Functional Block Diagram



Absolute Maximum Ratings

Temperature Stabilizer Voltage	40V
Reverse Breakdown Current	20 mA
Forward Current	1 mA
Reference to Substrate Voltage $V_{(RS)}$ (Note 1)	+40V
	−0.1V
Operating Temperature Range	
LM199A	−55°C to +125°C
LM299A	−25°C to +85°C
LM399A	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 2)

PARAMETER	CONDITIONS	LM199A, LM299A MIN	LM199A, LM299A TYP	LM199A, LM299A MAX	LM399A MIN	LM399A TYP	LM399A MAX	UNITS
Reverse Breakdown Voltage	0.5 mA $\leq I_R \leq$ 10 mA	6.8	6.95	7.1	6.6	6.95	7.3	V
Reverse Breakdown Voltage Change With Current	0.5 mA $\leq I_R \leq$ 10 mA		6	9		6	12	mV
Reverse Dynamic Impedance	I_R = 1 mA		0.5	1		0.5	1.5	Ω
Reverse Breakdown Temperature Coefficient	−55°C $\leq T_A \leq$ 85°C LM199A		0.00002	0.00005				%/°C
	85°C $\leq T_A \leq$ 125°C LM199A		0.0005	0.0010				%/°C
	−25°C $\leq T_A \leq$ 85°C LM299A		0.00002	0.00005				%/°C
	0°C $\leq T_A \leq$ 70°C LM399A					0.00003	0.0001	%/°C
RMS Noise	10 Hz $\leq$ f $\leq$ 10 kHz		7	20		7	50	μV
Long Term Stability	Stabilized, 22°C $\leq T_A \leq$ 28°C, 1000 Hours, I_R = 1 mA ±0.1%		20			20		ppm
Temperature Stabilizer Supply Current	T_A = 25°C, Still Air, V_S = 30V		8.5	14		8.5	15	mA
	T_A = −55°C		22	28				
Temperature Stabilizer Supply Voltage (Note 3)		9		40	9		40	V
Warm-Up Time to 0.05%	V_S = 30V, T_A = 25°C		3			3		Seconds
Initial Turn-on Current	9 $\leq V_S \leq$ 40, T_A = 25°C, (Note 3)		140	200		140	200	mA

Note 1: The substrate is electrically connected to the negative terminal of the temperature stabilizer. The voltage that can be applied to either terminal of the reference is 40V more positive or 0.1V more negative than the substrate.

Note 2: These specifications apply for 30V applied to the temperature stabilizer and −55°C $\leq T_A \leq$ +125°C for the LM199A; −25°C $\leq T_A \leq$ +85°C for the LM299A and 0°C $\leq T_A \leq$ +70°C for the LM399A.

Note 3: This initial current can be reduced by adding an appropriate resistor and capacitor to the heater circuit. See the performance characteristic graphs to determine values.

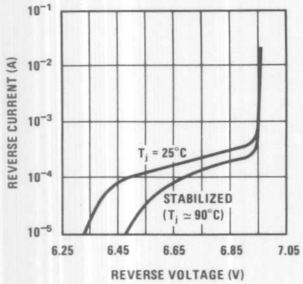
Typical Applications

For typical applications, see LM199 data sheet on preceding pages.

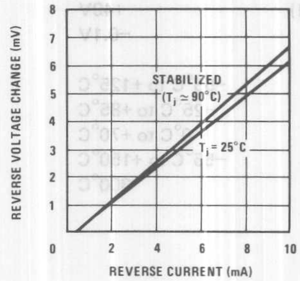
LM199A/LM299A/LM399A

Typical Performance Characteristics

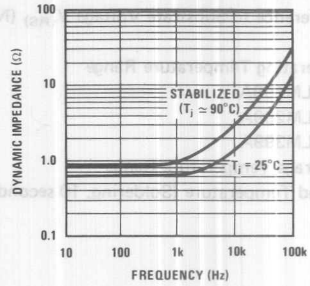
Reverse Characteristics



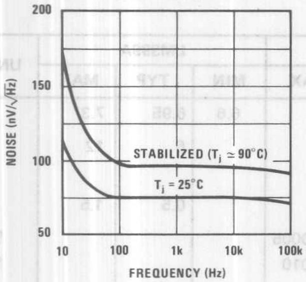
Reverse Voltage Change



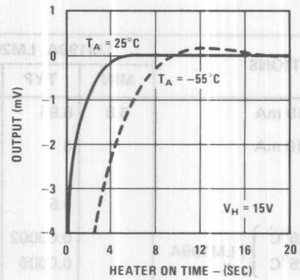
Dynamic Impedance



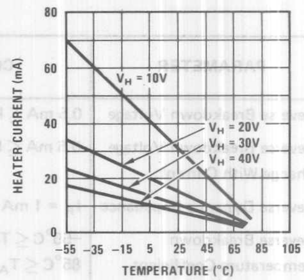
Zener Noise Voltage



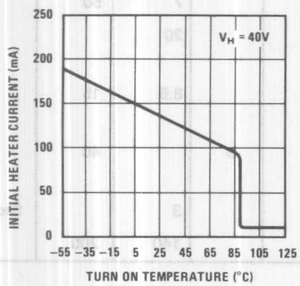
Stabilization Time



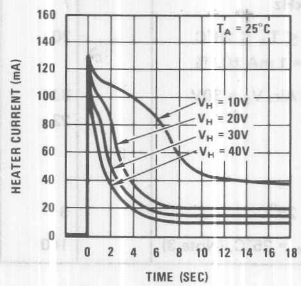
Heater Current



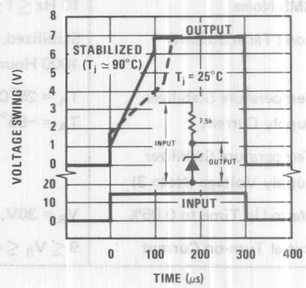
Initial Heater Current



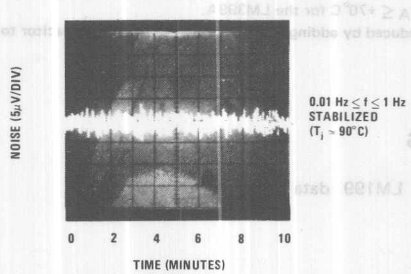
Heater Current



Response Time



Low Frequency Noise Voltage



National Semiconductor

LM3999 Precision Reference

General Description

The LM3999 is a precision, temperature-stabilized monolithic zener offering temperature coefficients a factor of ten better than high quality reference zeners. Constructed on a single monolithic chip is a temperature stabilizer circuit and an active reference zener. The active circuitry reduces the dynamic impedance of the zener to about 0.5Ω and allows the zener to operate over 0.5 mA to 10 mA current range with essentially no change in voltage or temperature coefficient. Further, a new subsurface zener structure gives low noise and excellent long term stability compared to ordinary monolithic zeners.

The LM3999 reference is exceptionally easy to use and free of the problems that are often experienced with ordinary zeners. There is virtually no hysteresis in reference voltage with temperature cycling. Also, the LM3999 is free of voltage shifts due to stress on the leads. Finally, since the unit is temperature stabilized, warm up time is fast.

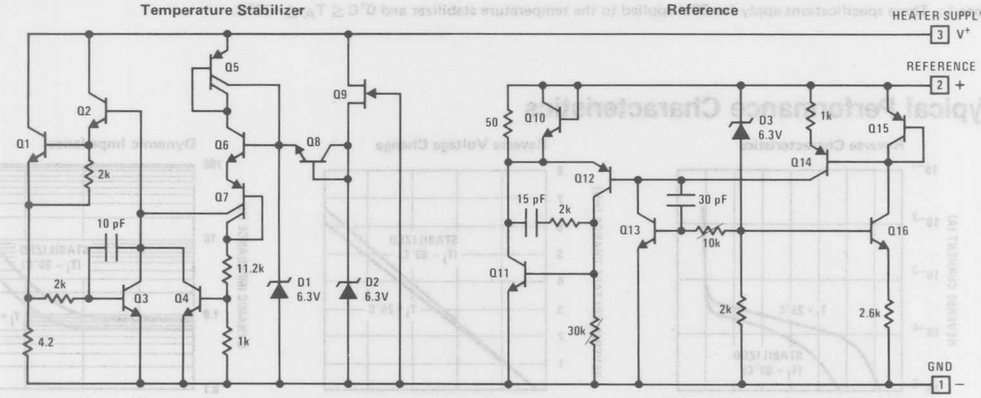
The LM3999 can be used in almost any application in place of ordinary zeners with improved performance. Some ideal applications are analog to digital converters, precision voltage or current sources or precision power supplies. Further, in many cases, the LM3999 can replace references in existing equipment with a minimum of wiring changes.

The LM3999 is packaged in a standard TO-92 package and is rated from 0°C to +70°C.

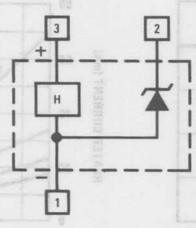
Features

- Guaranteed 0.0005%/°C temperature coefficient
- Low dynamic impedance – 0.5Ω
- Initial tolerance on breakdown voltage – 5%
- Sharp breakdown at 400μA
- Wide operating current – 500μA to 10 mA
- Wide supply range for temperature stabilizer
- Low power for stabilization – 400 mW at 25°C
- Long term stability – 20 ppm

Schematic Diagram

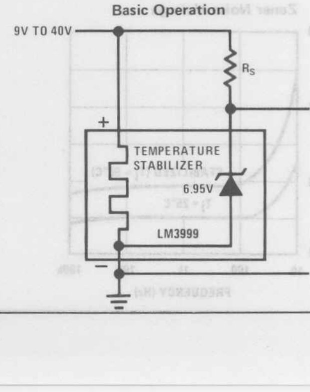


Functional Block Diagram



Typical Applications

Basic Operation



Forward Current	0.1 mA
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

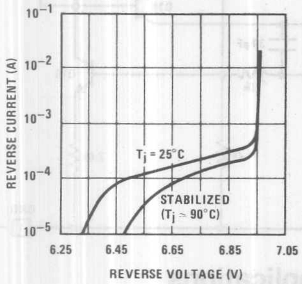
Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reverse Breakdown Voltage	$0.6\ mA \leq I_R \leq 10\ mA$	6.6	6.95	7.3	V
Reverse Breakdown Voltage Change With Current	$0.6\ mA \leq I \leq 10\ mA$		6	20	mV
Reverse Dynamic Impedance	$I_R = 1\ mA$		0.6	2.2	Ω
Reverse Breakdown Temperature Coefficient	$0°C \leq T_A \leq 70°C$		0.0002	0.0005	%/°C
RMS Noise	$10\ Hz \leq f \leq 10\ kHz$		7		μV
Long Term Stability	Stabilized, $22°C \leq T_A \leq 28°C$, 1000 Hours, $I_R = 1\ mA \pm 0.1\%$		20		ppm
Temperature Stabilizer	$T_A = 25°C$, Still Air, $V_S = 30V$		12	18	mA
Temperature Stabilizer Supply Voltage				36	V
Warm-Up Time to 0.05%	$V_S = 30V$, $T_A = 25°C$		5		Seconds
Initial Turn-on Current	$9 \leq V_S \leq 40$, $T_A = 25°C$		140	200	mA

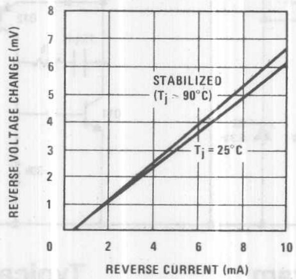
Note 1: These specifications apply for 30V applied to the temperature stabilizer and $0°C \leq T_A \leq +70°C$.

Typical Performance Characteristics

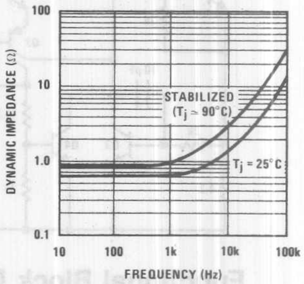
Reverse Characteristics



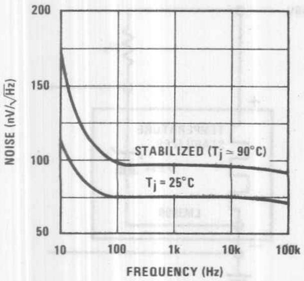
Reverse Voltage Change



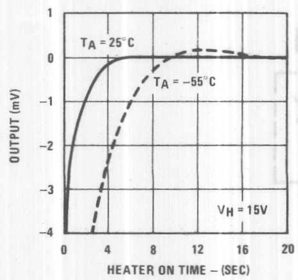
Dynamic Impedance



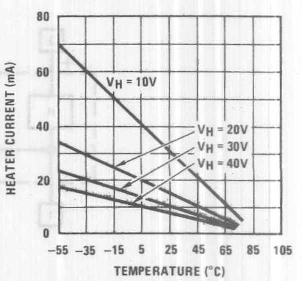
Zener Noise Voltage



Stabilization Time

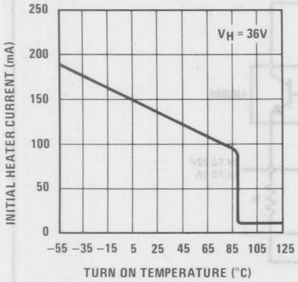


Heater Current

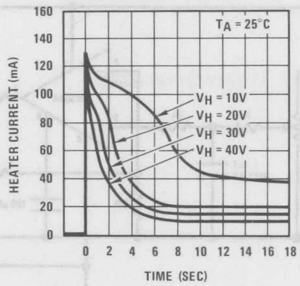


Typical Performance Characteristics (Continued)

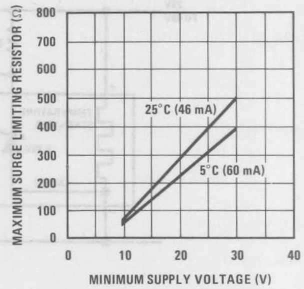
Initial Heater Current



Heater Current (To Limit This Surge, See Next Graph)

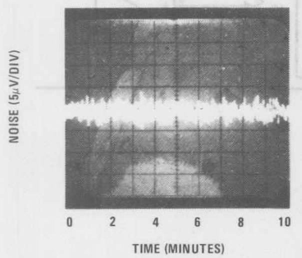


Heater Surge Limit Resistor vs Minimum Supply Voltage at Various Minimum Temperatures

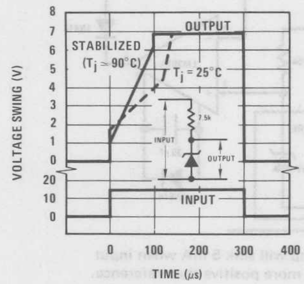


*Heater must be bypassed with a 2 μF tantalum capacitor if resistors are used.

Low Frequency Noise Voltage

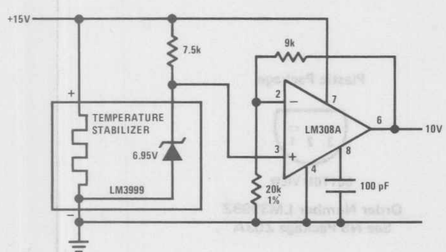


Response Time

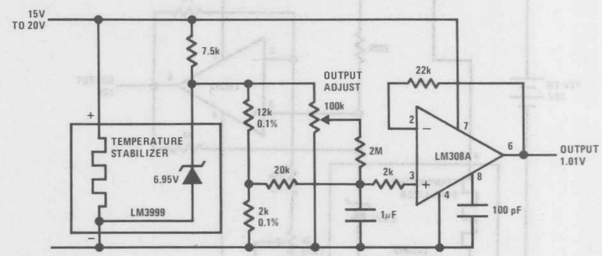


Typical Applications (Continued)

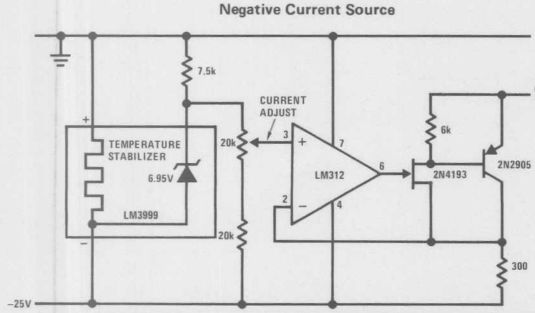
Buffered Reference With Single Supply



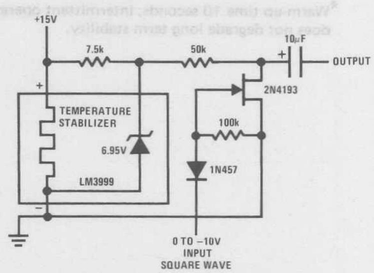
Voltage Reference



Negative Current Source

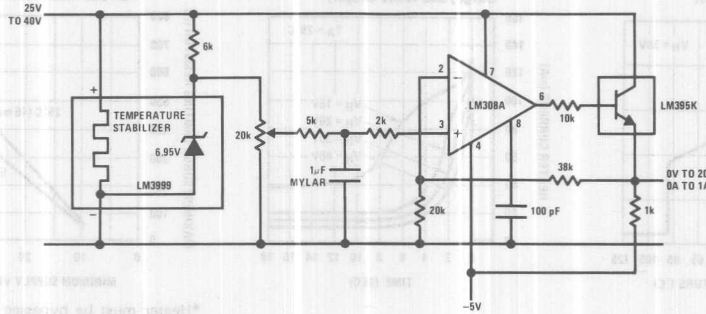


Square Wave Voltage Reference

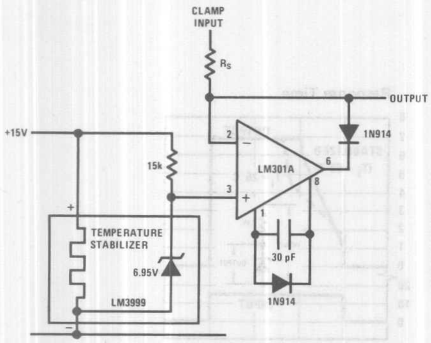


Typical Applications (Continued)

0V to 20V Power Reference

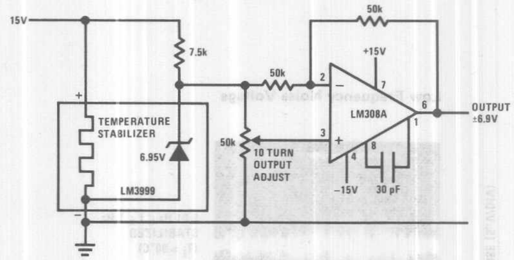


Precision Clamp*

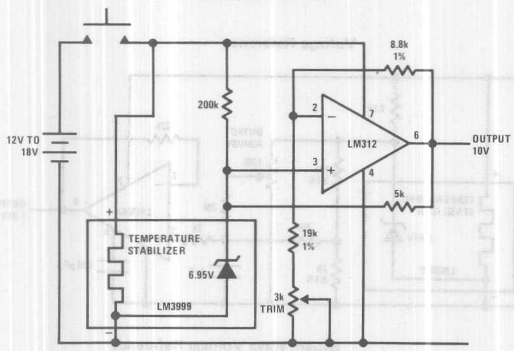


*Clamp will sink 5 mA when input goes more positive than reference.

Bipolar Output Reference



Portable Calibrator*



*Warm-up time 10 seconds; intermittent operation does not degrade long term stability.

Connection Diagram

Plastic Package

BOTTOM VIEW

Order Number LM3999Z
See NS Package Z03A

Section 3

Operational Amplifiers/Buffers

3

Section Contents

Section Contents (Continued)

Section Contents (Continued)

General Purpose, Compensated

General Purpose, Compensated (Continued)

General Purpose, Uncompensated

Op Amp—Comparator

Note. For additional information on operational amplifiers, see National Semiconductor's Hybrid Products Databook.

COMPARISON OF ELECTRICAL CHARACTERISTICS

Part Number	DC Electrical Characteristics: V_{OS}—Max Offset Voltage (mV) ($T_A = 25°C$)	DC Electrical Characteristics: $\Delta V_{OS}/\Delta T$—TC of V_{OS} ($\mu V/°C$) Typ	DC Electrical Characteristics: I_B—Max Bias Current (pA) ($T_J = 25°C$)	DC Electrical Characteristics: A_{VOL} Large Signal Voltage Gain (V/mV) Min ($T_A = 25°C$)	AC Electrical Characteristics: SR—Slew Rate ($V/\mu s$)	AC Electrical Characteristics: e_n—Equiv. Input Noise Voltage ($nV/\sqrt{Hz}$) (Note 2)
MILITARY BI-FET OP AMP (Note 1)						
LF155	5	5	100	50	5	20
LF155A	2	5 (max)	50	50	5	20
LF156	5	5	100	50	12	12
LF156A	2	5 (max)	50	50	12	12
LF157	5	5	100	50	50	12
LF157A	2	5 (max)	50	50	50	12
LF411A	0.5	10 (max)	200	50	10 (min)	25
LF411	2	10	200	50	8 (min)	25
LF441A (low power)	0.5	10 (max)	50	50	1	40
LF412A Dual	1	10 (max)	200	50	10 (min)	25
LF412	3	10	200	50	8 (min)	25
LF442A Dual (low power)	1	10	50	50	1	40
LF444 Quad (low power)	5	10	50	50	1	40
INDUSTRIAL BI-FET OP AMP (Note 1)						
LF255	5	5	100	50	5	20
LF256	5	5	100	50	12	12
LF257	5	5	100	50	50	12
COMMERCIAL BI-FET AND BI-FET II OP AMP (Note 3)						
LF351	10	10	200	25	13	16
LF355	10	5	200	25	5	25
LF355A	2	5 (max)	50	25	5	25
LF356	10	5	200	25	12	15
LF356A	2	5 (max)	50	25	12	15
LF357	10	5	200	25	50	15
LF357A	2	5 (max)	50	25	50	15
LF13741	15	10	200	25	0.5	37
LF411A	0.5	10 (max)	200	50	10	25
LF411	2.0	20	200	50	8	25
LF441A (low power)	0.5	10 (max)	50	50	1	40
LF441 (low power)	5	10	100	50	1	40
BI-FET II DUAL OP AMPS (CHARACTERISTICS FOR EACH AMPLIFIER) (Note 3)						
LF353	10	10	200	25	13	16
LF412A	1	10 (max)	200	50	10 (min)	25
LF412	3	20	200	50	8 (min)	25
LF442A (low power)	1	10 (max)	50	50	1	40
LF442 (low power)	3	20	100	50	1	40
BI-FET II QUAD OP AMPS (CHARACTERISTICS FOR EACH AMPLIFIER) (Note 3)						
LF347	10	10	200	25	13	16
LF347B	5	10	200	25	13	16
LF444A (low power)	5	10	50	50	1	40
LF444 (low power)	10	10	100	25	1	40

BI-FET™ and BI-FET II™ are trademarked terms by National Semiconductor who invented the technology in 1974.

Note 1: DC electrical characteristics are −55°C to +125°C for Military and −25°C to +85°C for Industrial unless otherwise noted; AC electrical characteristics are $T_A = 25°C$, typical specifications unless noted.

Note 2: f = 1000 Hz.

Note 3: DC electrical characteristics are 0°C to +70°C unless otherwise noted; AC electrical characteristics are $T_A = 25°C$, typical specifications unless noted.

Voltage ($T_A = 25°C$)	LF411A LF441A	LF442A LF412A	LF155A/LF355A LF156A/LF356A LF357A	LF412 LF442	LF347B LF155/LF156/LF157 LF255/LF256/LF257 LF444A	LF355/LF356/LF357 LF351 LF353 LF347 LF444	LF13741

Max Input Bias Current ($T_J = 25°C$)	**50 pA**	**100 pA**	**200 pA**
	LF155A/LF156A/LF157A LF355A/LF356A/LF357A LF441A LF442A LF444A	LF155/LF156/LF157 LF255/LF256/LF257 LF441 LF444 LF442	LF355/LF356/LF357 LF351 LF347/LF347B LF353 LF13741 LF411A LF411 LF412A LF412

Typ Equivalent Input Noise Voltage per $\sqrt{Hz}$, f = 1000 Hz $R_S = 100\Omega$	**12 nV or Less**	**15 nV to 20 nV**		**25 nV to 40 nV**		
	LF156/LF156A LF157/LF157A LF256/LF257	LF356 LF356A LF357 LF357A	LF351 LF347 LF347B LF353	LF155 LF155A LF255 LF355 LF355A	LF411A LF411 LF412A LF412 LF441A LF441	LF13741 LF442A LF442 LF444A LF444

Typ Slew Rate	**0.5V/μs**	**1V/μs**	**5V/μs**	**12V/μs**	**13V/μs**	**15V/μs**	**50V/μs**
	LF13741	LF441A LF441 LF442A LF442 LF444A LF444	LF155/LF155A LF255 LF355/LF355A	LF156 LF156A LF256 LF356 LF356A	LF351 LF353 LF347 LF347B	LF411A LF411 LF412A LF412	LF157 LF157A LF357 LF357A

ADDITIONAL NS PRODUCTS USING BI-FET TECHNOLOGY

- LF111 Comparator
- LF198 Sample and Hold
- LF11201 Series of Analog Switches
- LF11331 Series of Analog Switches
- LF11508 Series of Analog Multiplexers
- LF13300 Integrating A/D Building Block

MILITARY TEMPERATURE RANGE: $-55^{\circ}C \leq T_A \leq +125^{\circ}C$

Device	Input Offset Voltage Max (mV)	Input Offset Voltage Drift Max ($\mu V/^{\circ}C$)	Input Offset Current Max (nA)	Input Bias Current Max (nA)	Voltage Gain Min (Volts/V)	Bandwidth $A_V = 1$ Typ (MHz)	Slew Rate $A_V = 1$ Typ ($V/\mu s$)	Output Current Min @ $R_L = 2k$ (mA)	Supply Voltage Min (V)	Supply Voltage Max (V)	Common Mode Range (V)	Differential Input Voltage (V)	Supply Current $T_A = 25^{\circ}C$ Max (mA)	Compensation Components Per Amplifier	Package Types
SINGLE OP AMPS															
LM101A	3	15	20	100	25k	1	0.5	5	±3	±22	±12	±30	3	1	TO-5 DIP
LM102	7.5	6 typ	*	100	0.999	10	10	1 (R_L = 8 kΩ)	±12	±18	±10	*	5.5	0	TO-5
LM107	3	15	20	100	25k	1	0.5	7.5	±3	±22	±12	±30	3	0	TO-5 DIP
LM108A	1	5	0.4	3	40k	1	0.3	1	±2	±20	±14	(Note 1)	0.6	1	TO-5 DIP
LM108	3	15	0.4	3	25k	1	0.3	1	±2	±20	±14	(Note 1)	0.6	1	TO-5 DIP
LM110	6	12	*	10	0.999	20	30	1 (R_L = 8 kΩ)	±5	±18	±10	*	5.5	0	TO-5 DIP
LM112	3	15	0.4	3	25k	1	0.2	1.3 (R_L = 10 kΩ)	±2	±20	±14	(Note 1)	0.6	0	TO-5 DIP
LM118	4	*	50	250	20k	15	50 min	6	±5	±18	±11.5	(Note 1)	8	0	TO-5 DIP
LM121A (R_{SET}=70k)	0.65	0.2	1	30	16k	0.5	*	*	±5	±20	±15	±15	1.5	1	TO-5 DIP
LM121 (R_{SET}=70k)	1	1	3	30	16k	0.5	*	*	±5	±20	±15	±15	1.5	1	TO-5 DIP
LM143	6	*	7	35	50k	1	2.5	4.4 ($R_L \geq 5k$)	±4	±40	±38	±40	4	0	TO-5
LM144	6	*	7	35	50k	2	30 ($A_V > 10$)	4.4 ($R_L \geq 5k$)	±4	±40	±38	±40	4	1	TO-5
LF155A	**2.5**	**5**	**25**	**0.05**	**25k**	**2.5**	**5**	**5**	**±5**	**±22**	**±20**	**±40**	**4**	**0**	**TO-5**
LF155	**7**	**20**	**50**	**0.1**	**25k**	**2.5**	**5**	**5**	**±5**	**±22**	**±20**	**±40**	**4**	**0**	**TO-5**
LF156A	**2.5**	**5**	**25**	**0.05**	**25k**	**5**	**15**	**5**	**±5**	**±22**	**±20**	**±40**	**7**	**0**	**TO-5**
LF156	**7**	**20**	**50**	**0.1**	**25k**	**5**	**15**	**5**	**±5**	**±22**	**±20**	**±40**	**7**	**0**	**TO-5**
LF157A ($A_V \geq 5$)	**2.5**	**10**	**25**	**0.05**	**25k**	**25**	**75**	**5**	**±5**	**±22**	**±20**	**±40**	**7**	**0**	**TO-5**
LF157 ($A_V \geq 5$)	**7**	**20**	**50**	**0.1**	**25k**	**25**	**75**	**5**	**±5**	**±22**	**±20**	**±40**	**7**	**0**	**TO-5**
LF411A	**1.5**	**10**	**25**	**0.05**	**25**	**4**	**15**	**5**	**±6**	**±22**	**±16**	**±38**	**2.8**	**0**	**TO-5**
LF411	**4**	**20**	**25**	**0.1**	**15**	**4**	**15**	**5**	**±6**	**±18**	**±11**	**±30**	**3.4**	**0**	**TO-5**
LF441A	**1.5**	**10**	**10**	**0.05**	**25**	**1**	**1**	**5**	**±6**	**±22**	**±16**	**±38**	**0.200**	**0**	**TO-5**
LM709A	3	15	250	600	25k	1	0.3	5	±5	±22	±20	±40	3.6	3	TO-5
LM709	6	6 typ	500	1500	25k	1	0.3	5	±9	±18	±8	±5	5.5	3	TO-5 DIP
LM725A	0.7	2	18	180	1000	0.5	0.005	5	±3	±22	±13.5	±5	3.5	4	TO-5 DIP
LM725	1.5	5	40	200	1000	0.5	0.005	5	±3	±22	±13.5	±5	3.5	4	TO-5
LM741A	4	15	70	210	32k	1	0.5	7.5	±3	±22	±12	±30	4.0	0	TO-5 DIP
LM741	6	15 typ	500	1500	25k	1	0.5	5	±3	±22	±12	±30	2.8	0	TO-5 DIP
LM748	6	*	500	1500	25k	1	0.5	5	±3	±22	±12	±30	2.8	1	TO-5
LM4250 (V_S = ±15V)	4	*	3	7.5	50k	0.1	0.03	0.12 ($R_L \geq 100k$)	±1	±18	±12	±15	0.011 set	0	TO-5 DIP

Note 1: Inputs have shunt-diode protection; current must be limited. *Not specified

Military Op Amp Selection Guide

MILITARY TEMPERATURE RANGE: $-55^{\circ}C \leq T_A \leq +125^{\circ}C$

Device	Input Offset Voltage Max (mV)	Input Offset Voltage Drift Max ($\mu V/^{\circ}C$)	Input Offset Current Max (nA)	Input Bias Current Max (nA)	Voltage Gain Min (Volts/V)	Bandwidth $A_V = 1$ Typ (MHz)	Slew Rate $A_V = 1$ Typ (V/μs)	Output Current Min @ R_L = 2k (mA)	Supply Voltage Min (V)	Supply Voltage Max (V)	Common Mode Range (V)	Differential Input Voltage (V)	Supply Current $T_A = 25^{\circ}C$ Max (mA) (Note 2)	Compensation Components Per Amplifier	Package Types
DUAL OP AMPS															
LF412A	2	10	25		25	4	15		±6	±22	±16	±38	5.6	0	TO-5
LF412	5	20	25		15	4	15		±6	±22	±11	±30	6.8	0	TO-5
LF442A	2	10	10		25	1	1		±6	±22	±16	±38	0.200	0	TO-5
LM158	5	*	30	150	25k	1	*	0.8	±1.5	±16	$V^+-1.5$	V^+	1.2	0	TO-5 DIP
LM1558	6	*	500	1500	25k	1	0.5	5	±3	±22	±12	±30	5.0	0	TO-5
LM747A	4	15	70	210	32k	1	0.5	7.5	±3	±22	±12	±30	5.6	0	DIP
LM747	6	*	500	1500	25k	1	0.5	5	±3	±22	±12	±30	5.6	0	DIP
QUAD OP AMPS															
LF444A	8	10	10		25	1	1		±6	±22	±16	±38	0.8	0	DIP
LM124	7	7 typ	±30	150	50	1.0	*	10	−16	+16	0 to $V^+-1.5V$	V^+_{DC}	3	0	DIP
LM146 ($I_{SET} = 10\ \mu A$)	5	5 typ	20	100	100k	1.2	0.4	1.2	±2	±22	±0.7	±30	2	0	DIP
LM148	6	15 typ	75	325	25k	1	0.6	5	±3	±22	±12	±30	3.6	0	DIP
LM149 ($A_V \geq 5$)	6	15 typ	75	325	25k	4	3	5	±3	±22	±12	±30	3.6	0	DIP

Note 2: Supply current for all channels of amplifier in the package.

INDUSTRIAL TEMPERATURE RANGE: $-25^{\circ}C \le T_A \le +85^{\circ}C$

Device	Input Offset Voltage Max (mV)	Input Offset Voltage Drift Max ($\mu V/^{\circ}C$)	Input Offset Current Max (nA)	Input Bias Current Max (nA)	Voltage Gain Min (Volts/V)	Bandwidth $A_V = 1$ Typ (MHz)	Slew Rate $A_V = 1$ Typ ($V/\mu s$)	Output Current Min @ $R_L = 2\ k\Omega$ (mA)	Supply Voltage Min (V)	Supply Voltage Max (V)	Common Mode Range (V)	Differential Input Voltage (V)	Supply Current $T_A = 25^{\circ}C$ Max (mA) (Note 2)	Compensation Components Per Amplifier	Package Types
SINGLE OP AMPS															
LM201A	3	15	20	100	25k	1	0.5	5	±3	±22	±12	±30	3	1	TO-5 DIP
LM202	10	15 typ	*	15	0.999	10	10	1	±12	±18	±10	*	5.5	0	TO-5
LM207	2	20	20	100	25k	1	0.5	5	±3	±22	±12	±30	3	0	TO-5 DIP
LM208A	1.0	5	0.4	3	40k	1	0.3	1	±2	±20	±14	(Note 1)	0.6	1	TO-5 DIP
LM208	3	15	0.4	3	25k	1	0.3	1	±2	±20	±14	(Note 1)	0.6	1	TO-5 DIP
LM210	4	*	*	3	0.999	20	30	1	±5	±18	±10	*	5.5	0	TO-5 DIP
LM212	2	15	0.2	2	25k	1	0.3	1	±2	±20	±14	(Note 1)	0.6	0	TO-5
LM216A	3	*	0.015	0.05	20k	1	0.3	1	±5	±20	±13	(Note 1)	0.6	0	TO-5
LM216	10	*	0.05	0.15	10k	1	0.3	1	±5	±20	±13	(Note 1)	0.8	0	TO-5
LM218	4	*	50	500	25k	15	50 min	5	±5	±18	±11.5	(Note 1)	8	0	TO-5 DIP
LM221A (R_{SET} = 70k)	0.65	0.2	1	30	16k	0.5	*	*	±5	±20	±15	±15	1.5	1	TO-5 DIP
LM221 (R_{SET} = 70k)	1	1	3	30	16k	0.5	*	*	±5	±20	±15	±15	1.5	1	TO-5 DIP
LF255	6.5	5 typ	20	50	25k	2.5	5	5	±5	±22	±20	±40	4	0	TO-5
LF256	6.5	5 typ	20	50	25k	5	15	5	±5	±22	±20	±40	7	0	TO-5
LF257 ($A_V \ge 5$)	6.5	5 typ	20	50	25k	25	75	5	±5	±22	±20	±40	7	0	TO-5
DUAL OP AMPS															
LM258	7.5	7 typ	150	500	15k	1	0.5	10–source 5–sink	3 (±1.5)	32 (±16)	V^+ −1.5	32	1.2	0	TO-5 DIP
QUAD OP AMPS															
LM224	9	7 typ	150	500	15k	1	*	10	3	32	V^+−1.5	32	2	0	DIP
LM246	6	7 typ	100	250	50k	0.5	0.4	1.2	±2	±18	±1.5	±30	2.5	0	DIP
LM248	7.5	15 typ	125	500	15k	1	0.5	5	±5	±18	±18	±36	4.5	0	DIP
LM249	7.5	15 typ	125	500	15k	4	2	5	±5	±18	±18	±36	4.5	0	DIP
LM2900	*	*	*	200	1.2k	2.5	*	3–source 0.5–sink	+4	+36	*	*	10	0	DIP
LM2902	10 (T_A=25°)	*	±50 (T_A=25°C)	500 (T_A=25°C)	100k typ	1	*	20–source 8–sink	3.0 single ±1.5 dual	26 single ±13 dual	$-0.3V_{DC}$ to $+26\ V_{DC}$	26 V_{DC}	2	0	DIP

Note 1: Inputs have shunt-diode protection; current must be limited.

Note 2: Supply current for all channels of amplifier in the package.

*Not specified

COMMERCIAL TEMPERATURE RANGE: $0^\circ C \leq T_A \leq +70^\circ C$

Device	Input Offset Voltage Max (mV)	Input Offset Voltage Drift Max ($\mu V/^\circ C$)	Input Offset Current Max (nA)	Input Bias Current Max (nA)	Voltage Gain Min (Volts/V)	Bandwidth $A_V = 1$ Typ (MHz)	Slew Rate $A_V = 1$ Typ (V/μs)	Output Voltage Swing $R_L = 10\,k\Omega$ (V)	Supply Voltage Min (V)	Supply Voltage Max (V)	Common Mode Rejection Ratio (dB) Min	Differential Input Voltage (V)	Supply Current $T_A = 25^\circ C$ Max (mA) (Note 2)	Compensation Components	Pack
SINGLE OP AMPS															
LM301A	10	30	70	300	15k	1	0.5	5	±3	±18	±12	±30	3	1	TO
LM302	20	20 typ	*	30	0.9985	10	10	1	±12	±18	±10	*	5.5	0	TO
LM307	10	30	50	250	15k	1	0.5	5	±3	±18	±12	±30	3	0	TO
LM308A	0.73	5	1.5	10	60k	1	0.3	1	±2	±20	±14	(Note 1)	0.8	1	TO
LM308	10	30	1.5	10	15k	1	0.3	1	±2	±18	±14	(Note 1)	0.8	1	TO
LM310	10	10 typ	*	10	0.999	20	30	1	±5	±18	±10	*	5.5	0	TO
LM312	10	30	1.5	10	15k	1	0.3	1	±2	±18	±14	(Note 1)	0.8	0	TO
LM316A	6	*	0.03	0.1	30k	1	0.3	1	±5	±20	±13	(Note 1)	0.6	0	TO
LM316	15	*	0.1	0.25	15k	1	0.3	1	±5	±20	±13	(Note 1)	0.8	0	TO
LM318	15	*	300	750	20k	15	50	5	±5	±18	±11.5	(Note 1)	10	0	TO
LM321A (R_{SET} = 70k)	0.65	0.2	1	25	12k	0.5	*	*	±5	±20	±15	±15	2.2	1	TO
LM321 (R_{SET} = 70k)	2.5	1	4	28	12k	0.5	*	*	±5	±20	±15	±15	2.2	1	TO
LM343	10	*	14	55	50k	1	2.5	4 ($R_L \geq 5k$)	±4	±34	±34	±34	5.0	0	TO
LM344	10	*	14	55	50k	2	30	4 ($R_L \geq 5k$)	±4	±34	±34	±34	5.0	1	TO-
LF351	10	10 typ	0.1	0.2	25k	4	13	±12	−18	18	70	±30	3.4	0	TO-
LF355A	2.3	5	1	5	25k	2.5	5	5	±5	±22	±20	±40	4	0	TO-
LF355	13	5 typ	2	8	15k	2.5	5	5	±5	±18	±16	±30	4	0	TO-
LF356A	2.3	5	1	5	25k	5	15	5	±5	±22	±20	±40	10	0	TO-
LF356	13	5 typ	2	8	15k	5	15	5	±5	±18	±16	±30	10	0	TO-
LF357A ($A_V \geq 5$)	2.3	5	1	5	25k	25	75	5	±5	±22	±20	±40	10	0	TO-
LF357 ($A_V \geq 5$)	13	5 typ	2	8	15k	25	75	5	±5	±18	±16	±30	10	0	TO-
LF411A	0.5	10	0.100		50	4	15		±6	±22	±16	±38	1.8	0	TO-
LF411	2.0	20	0.100		25	4	15		±6	±18	±11	±30	3.4	0	TO-
LF441A	0.5	10	0.025		50	1	1		±6	±22	±16	±38	0.200	0	TO-
LF441	5	10 typ	0.050		25	1	1		±6	±18	±11	±30	0.250	0	TO-
LF13741	20	10 typ	2	8	15k	1	0.5	5	±4	±18	±16	±30	4	0	TO-

Note 1: Inputs have shunt-diode protection; current must must be limited. *Not specified

COMMERCIAL TEMPERATURE RANGE $0^\circ C \leq T_A \leq +70^\circ C$

Device	Input Offset Voltage Max (mV)	Input Offset Voltage Drift Max ($\mu V/^\circ C$)	Input Offset Current Max (nA)	Input Bias Current Max (nA)	Voltage Gain Min (Volts/V)	Bandwidth $A_V = 1$ Typ (MHz)	Slew Rate $A_V = 1$ Typ ($V/\mu s$)	Output Voltage Swing $R_L = 10\,k\Omega$ (V)	Supply Voltage Min (V)	Supply Voltage Max (V)	Common Mode Rejection Ratio (dB) Min	Differential Input Voltage (V)	Supply Current $T_A = 25^\circ C$ Max (mA) (Note 2)	Compensation Components	Package Types
SINGLE OP AMPS (Continued)															
LM709C	10	12 typ	500	1500	15k	1	0.3	5	±9	±18	±8	±5	6.6	3	TO-5 DIP
LM725C	3.5	2 typ	50	250	125k	0.5	0.005	5	±3	±22	±13.5	±5	5	4	TO-5 DIP
LM741C	7.5	15 typ	300	800	15k	1	0.5	5	±3	±18	±12	±30	2.8	0	TO-5 DIP
LM741E	4	15	70	210	32k	1	0.5	7.5	±3	±18	±12	±30	3.75	0	TO-5 DIP
LM748C	6	6	0.5	1.5	25k	1	0.5	5	±3	±18	±12	±30	2.8	1	TO-5 DIP
LM4250C	6	*	8	10	50k	0.1	0.03	0.12	±1	±18	±12	±15	0.011	0	TO-5 DIP
							($A_V > 10$)	($R_L \geq 100k$)					(Set)		
DUAL OP AMPS															
LF353	**10**	**10 typ**	**0.1**	**0.2**	**25k**	**4**	**13**	**±12**	**−18**	**18**	**70**	**±30**	**6.5**	**0**	**TO-5, DIP**
LF412	**3**	**20**	**0.100**		**25**	**4**	**15**		**±6**	**±18**	**±11**	**±30**	**6.8**	**0**	**TO-5, DIP**
LF412A	**1**	**10**	**0.100**		**50**	**4**	**15**		**±6**	**±22**	**±16**	**±38**	**5.6**	**0**	**TO-5, DIP**
LF442			**0.100**		**25**	**1**	**1**		**±6**	**±18**	**±11**	**±30**	**0.500**		**TO-5, DIP**
LF442A	**1**	**10**	**0.050**		**50**	**1**	**1**		**±6**	**±22**	**±16**	**±38**	**0.400**	**0**	**TO-5, DIP**
LM358	7.5	7 typ	150	500	15k	1	*	8	±1.5	±15	$V^+-1.5$	V^+	1.2	0	TO-5 DIP
LM1458	6	*	300	800	15k	1	0.2	5	±3	±18	±15	±30	5.6	0	TO-5 DIP
LM747C	6	*	300	800	15k	1	0.5	5	±3	±18	±12	±30	5.6	0	TO-5 DIP
LM747E	4	15	70	210	32k	1	0.5	7.5	±3	±18	±12	±30	5.6	0	TO-5 DIP
QUAD OP AMPS															
LF347	**10**	**10 typ**	**0.01**	**0.2**	**25k**	**4**	**13**	**±12**	**−18**	**18**	**70**	**±30**	**11**	**0**	**N, J**
LF347A	**5**	**10 typ**	**0.1**	**0.2**	**50k**	**4**	**13**	**±12**	**−18**	**18**	**80**	**±30**	**11**	**0**	**N, J**
LF444	**10**	**10 typ**	**0.100**		**25**	**1**	**1**		**±6**	**±18**	**±11**	**±30**	**1**	**0**	**DIP**
LF444A	**5**	**10 typ**	**0.050**		**50**	**1**	**1**		**±6**	**±22**	**±16**	**±38**	**0.8**	**0**	**DIP**
LM324	9	7 typ	150	500	15k	1	*	10–source	3	32	$V^+-1.5$	32	2	0	DIP
								5–sink	(±1.5)	(±16)					
LM346	5	10 typ	100	250	100k	0.8	0.4	±12	−18	18	70	±30	0.62	0	N, J
LM348	7.5	15 typ	100	400	15k	1	*	5	±5	±18	±18	±36	4.5	0	DIP
LM349	7.5	15 typ	100	400	15k	4	3	5	±5	±18	±18	±36	4.5	0	DIP
($A_V \geq 5$)															
LM3900	*	*	*	200	2.8k	2.5	20	10	4	36	*	*	10	0	DIP
									(±2)	(±18)					

Note 2: Supply current for all channels of amplifier in the package

HYBRID OPERATIONAL AMPLIFIERS

Features	Input Offset Voltage Max (mV)	Input Offset Voltage Drift Typ (μV/°C)	Input Offset Current Max (nA)	Input Bias Current Max (nA)	Voltage Gain Min (Volts/mV)	Bandwidth $A_V = 1$ Typ (MHz)	Slew Rate $A_V = 1$ Typ (V/μs)	Output Current (mA)	Supply Voltage Min (V)	Supply Voltage Max (V)	Temperature Range −55°C to 125°C	Temperature Range −25°C to 85°C	Temperature Range 0°C to 70°C	* Page Number
Wideband	3	4	200	2000	15	30	30	±100	±5	±20	LH0003	LH0003C		1-4
High Voltage	1	4	20	100	30	1	0.25	±15	±5	±45	LH0004			1-6
	1.5	4	45	120		1	0.25	±15	±5	±45		LH0004C		1-6
Wideband	3	10	5	25	4	30 (1)	20 (1)	±50	±9	±20	LH0005A			1-9
	10	20	20	50	2	30 (1)	20 (1)	±50	±9	±20	LH0005			1-9
	10	25	25	100	2	30 (1)	20 (1)	±50	±9	±20		LH0005C		1-12
High Gain Medium Power	2.5	10	50	250	100	1	0.25	±40	±5	±22	LH0020			1-14
	6	10	200	500	50	1	0.25	±40	±5	±22		LH0020C		1-14
High Power	3	3	100	300	100	1	3	±1000	±5	±18	LH0021			1-16
	6	5	200	500	100	1	3	±1000	±5	±18		LH0021C		1-16
	3	3	100	300	100	1	3	±200	±5	±18	LH0041			1-16
	6	5	200	500	100	1	3	±200	±5	±18		LH0041C		1-16
	4	5	100	300	50	15	70	±500	±5	±18	LH0061			1-56
	10	5	200	500	25	15	70	±500	±5	±18		LH0061C		1-56
General Purpose FET Input	4	5	0.002	0.01	100	1	3	±10	±5	±22	LH0022			1-23
	6	5	0.005	0.025	75	1	3	±10	±5	±22		LH0022C		1-23
	20	5	0.005	0.025	50	1	3	±10	±5	±22	LH0042			1-23
	20	10	0.01	0.05	25	1	3	±10	±5	±22		LH0042C		1-23
	0.5	2	0.0005	0.0025	100	1	3	±10	±5	±22	LH0052			1-23
	1	5	0.001	0.005	75	1	3	±10	±5	±22		LH0052C		1-23
Wideband High Slew Rate	4	20	5,000	30,000	4	50	500	±10	±9	±18	LH0024			1-30
	8	25	15,000	40,000	3	50	400	±10	±9	±18		LH0024C		1-30
Wideband FET Input	5	25	0.025	0.1	1	70	500	±10	±5	±18	LH0032			1-33
	15	25	0.05	0.2	1	70	500	±10	±5	±18		LH0032C		1-33
Precision FET Input	0.05	0.2	5	30	500	0.4	0.06	±1.3	±3	±20	LH0044			1-39
	0.1	0.2	5	30	500	0.4	0.06	±1.3	±3	±20		LH0044C		1-39
	0.025	0.1	2.5	15	1,000	0.4	0.06	±1.3	±3	±20	LH0044A			1-39
	0.025	0.1	2.5	15	1,000	0.4	0.06	±1.3	±3	±20		LH0044AC		1-39
	0.05	0.2	5	30	500	0.4	0.06	±1.3	±3	±20		LH0044B		1-39
Medium Speed. FET Input	5	5	0.002	0.01	50	15	70	±6	±5	±20	LH0062			1-59
	15	10	0.005	0.065	25	15	70	±6	±5	±20		LH0062C		1-59
Dual Precision	2	15	10	75	50	1	0.5	±5	±3	±22	LH2101A			1-91
	2	15	10	75	50	1	0.5	±5	±3	±22		LH2201A		1-91
	7.5	30	50	250	25	1	0.5	±5	±3	±22			LH2301A	1-91
	0.5	5	0.2	2	80	1	0.3	±1	±2	±20	LH2108A			1-93
	0.5	5	0.2	2	80	1	0.3	±1	±2	±20		LH2208A		1-93
	0.5	5	1.0	7	80	1	0.3	±1	±2	±20			LH2308A	1-93
	2	15	0.2	2	50	1	0.3	±1	±2	±20	LH2108			1-93
	2	15	0.2	2	50	1	0.3	±1	±2	±20		LH2208		1-93
	7.5	30	1.0	7	50	1	0.3	±1	±2	±20			LH2308	1-93
Dual Low Power	3	—	5	15	100	0.25	0.16	±0.75	±1	±18	LH24250			1-95
	6	—	10	30	75	0.25	0.16	±0.75	±1	±18		LH24250C		1-95

Note: For information on monolithic operational amplifiers, consult the *Linear Databook*.

Note 1: Specified for $A_V = -10$.

* Refers to Hybrid Products Databook, 1982 edition

HYBRID BUFFER AMPLIFIERS

Features	Voltage Gain (min)	Output Current	Slew Rate	Input Impedance	Part Number −55°C to 125°C	Part Number −25°C to 85°C	* Page Number
Bipolar Input, medium speed	0.95	±100 mA	200 V/μs	180 KΩ	LH0002H	LH0002CH LH0002CN	2-4 2-4
FET Input, high speed	0.97	±100 mA	1000 V/μs	10^{10} Ω	LH0033G	LH0033CG LH0033CJ	2-7 2-7
FET Input, very high speed	0.95	±250 mA	2000 V/μs	10^{10} Ω	LH0063K	LH0063CK	2-7

* Refers to Hybrid Products Databook, 1982 edition

Definition of Terms

Bandwidth: That frequency at which the voltage gain is reduced to $1/\sqrt{2}$ times the low frequency value.

Common-Mode Rejection Ratio: The ratio of the input common-mode voltage range to the peak-to-peak change in input offset voltage over this range.

Harmonic Distortion: That percentage of harmonic distortion being defined as one-hundred times the ratio of the root-mean-square (rms) sum of the harmonics to the fundamental. % harmonic distortion =

$$\frac{(V2^2 + V3^2 + V4^2 + \ldots)^{1/2}\,(100\%)}{V1}$$

where V1 is the rms amplitude of the fundamental and V2, V3, V4, . . . are the rms amplitudes of the individual harmonics.

Input Bias Current: The average of the two input currents.

Input Common-Mode Voltage Range: The range of voltages on the input terminals for which the amplifier is operational. Note that the specifications are not guaranteed over the full common-mode voltage range unless specifically stated.

Input Impedance: The ratio of input voltage to input current under the stated conditions for source resistance (R_S) and load resistance (R_L).

Input Offset Current: The difference in the currents into the two input terminals when the output is at zero.

Input Offset Voltage: That voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage.

Input Resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Input Voltage Range: The range of voltages on the input terminals for which the amplifier operates within specifications.

Large-Signal Voltage Gain: The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

Output Impedance: The ratio of output voltage to output current under the stated conditions for source resistance (R_S) and load resistance (R_L).

Output Resistance: The small signal resistance seen at the output with the output voltage near zero.

Output Voltage Swing: The peak output voltage swing, referred to zero, that can be obtained without clipping.

Offset Voltage Temperature Drift: The average drift rate of offset voltage for a thermal variation from room temperature to the indicated temperature extreme.

Power Supply Rejection: The ratio of the change in input offset voltage to the change in power supply voltages producing it.

Settling Time: The time between the initiation of the input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

Slew Rate: The internally-limited rate of change in output voltage with a large-amplitude step function applied to the input.

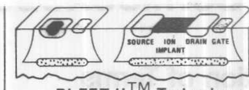
Supply Current: The current required from the power supply to operate the amplifier with no load and the output midway between the supplies.

Transient Response: The closed-loop step-function response of the amplifier under small-signal conditions.

Unity Gain Bandwidth: The frequency range from dc to the frequency where the amplifier open loop gain rolls off to one.

Voltage Gain: The ratio of output voltage to input voltage under the stated conditions for source resistance (R_S) and load resistance (R_L).

LF147/LF347 Wide Bandwidth Quad JFET Input Operational Amplifiers



BI-FET II™ Technology

General Description

The LF147 is a low cost, high speed quad JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF147 is pin compatible with the standard LM148. This feature allows designers to immediately upgrade the overall performance of existing LF148 and LM124 designs.

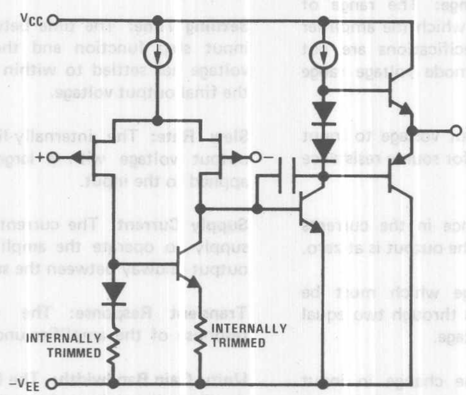
The LF147 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift.

Features

- Internally trimmed offset voltage — 2 mV
- Low input bias current — 50 pA
- Low input noise current — 0.01 pA/$\sqrt{Hz}$
- Wide gain bandwidth — 4 MHz
- High slew rate — 13 V/µs
- Low supply current — 7.2 mA
- High input impedance — $10^{12}\Omega$
- Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz–20 kHz — <0.02%
- Low 1/f noise corner — 50 Hz
- Fast settling time to 0.01% — 2 µs

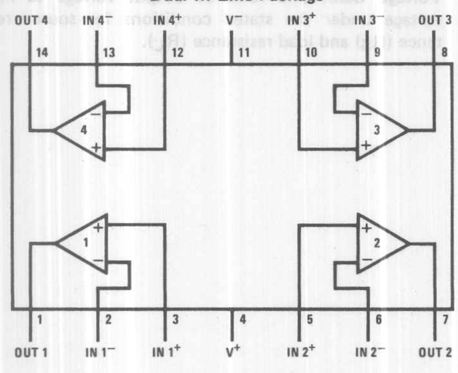
Simplified Schematic

1/4 Quad



Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number LF147D or LF347D
See NS Package D14E

Order Number LF347BN or LF347N
See NS Package N14A

			LF147	LF347B/LF347
Supply Voltage	±22V	±18V		
Differential Input Voltage	±38V	±30V		
Input Voltage Range (Note 1)	±19V	±15V		
Output Short Circuit Duration (Note 2)	Continuous	Continuous		

	LF147	LF347B/LF347
Power Dissipation (Note 3)	900 mW	500 mW
T_j max	150°C	115°C
θ_{jA}	100°C/W	150°C/W
Operating Temperature Range	(Note 4)	(Note 4)
Storage Temperature Range	$-65°C \le T_A \le 150°C$	
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

DC Electrical Characteristics (Note 5)

SYMBOL	PARAMETER	CONDITIONS	LF147			LF347B			LF347			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$R_S = 10\ k\Omega$, $T_A = 25°C$		1	5		3	5		5	10	mV
		Over Temperature			8			7			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\ k\Omega$		10			10			10		μV/°C
I_{OS}	Input Offset Current	$T_j = 25°C$, (Notes 5, 6)		25	100		25	100		25	100	pA
		Over Temperature			25			4			4	nA
I_B	Input Bias Current	$T_j = 25°C$, (Notes 5, 6)		50	200		50	200		50	200	pA
		Over Temperature			50			8			8	nA
R_{IN}	Input Resistance	$T_j = 25°C$		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm15V$, $T_A = 25°C$, $V_O = \pm10V$, $R_L = 2\ k\Omega$	50	100		50	100		25	100		V/mV
		Over Temperature	25			25			15			V/mV
V_O	Output Voltage Swing	$V_S = \pm15V$, $R_L = 10\ k\Omega$	±12	±13.5		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm15V$	±11	+15 −12		±11	+15 −12		±11	+15 −12		V V
CMRR	Common-Mode Rejection Ratio	$R_S \le 10\ k\Omega$	80	100		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 7)	80	100		80	100		70	100		dB
I_S	Supply Current			7.2	11		7.2	11		7.2	11	mA

AC Electrical Characteristics (Note 5)

SYMBOL	PARAMETER	CONDITIONS	LF147			LF347B			LF347			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
	Amplifier to Amplifier Coupling	$T_A = 25°C$, f = 1 Hz–20 kHz (Input Referred)		−120			−120			−120		dB
SR	Slew Rate	$V_S = \pm15V$, $T_A = 25°C$		13			13			13		V/μs
GBW	Gain-Bandwidth Product	$V_S = \pm15V$, $T_A = 25°C$		4			4			4		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, f = 1000 Hz		20			20			20		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_j = 25°C$, f = 1000 Hz		0.01			0.01			0.01		$pA/\sqrt{Hz}$

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 3: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{jA}.

Note 4: The LF147 is available in the military temperature range $-55°C \le T_A \le 125°C$, while the LF347B and the LF347 are available in the commercial temperature range $0°C \le T_A \le 70°C$.

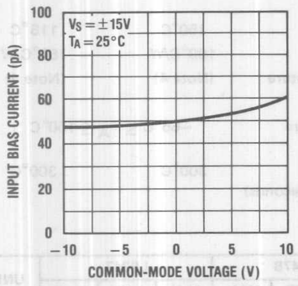
Note 5: Unless otherwise specified the specifications apply over the full temperature range and for $V_S = \pm20V$ for the LF147 and for $V_S = \pm15V$ for the LF347B/LF347. V_{OS}, I_B, and I_{OS} are measured at $V_{CM} = 0$.

Note 6. The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

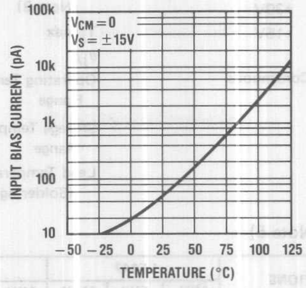
Note 7: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

Typical Performance Characteristics

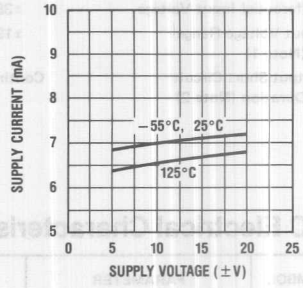
Input Bias Current



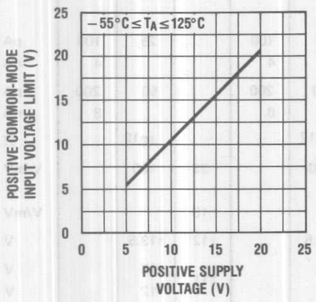
Input Bias Current



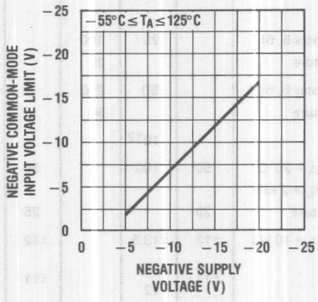
Supply Current



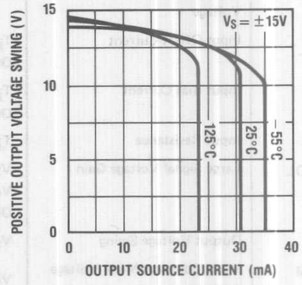
Positive Common-Mode Input Voltage Limit



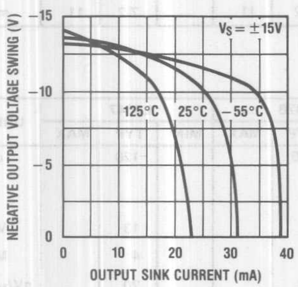
Negative Common-Mode Input Voltage Limit



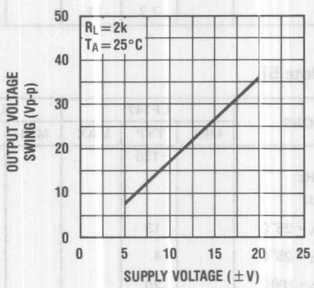
Positive Current Limit



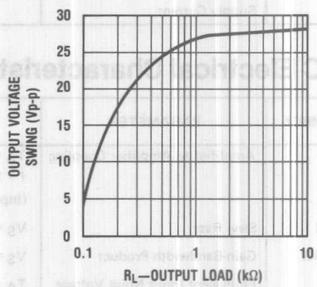
Negative Current Limit



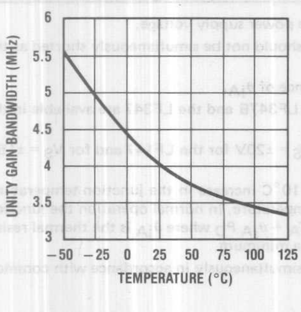
Output Voltage Swing



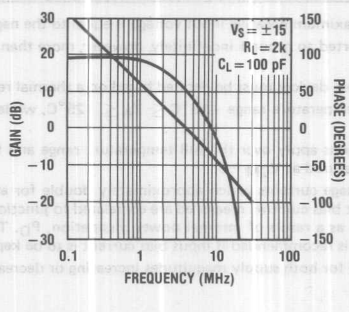
Output Voltage Swing



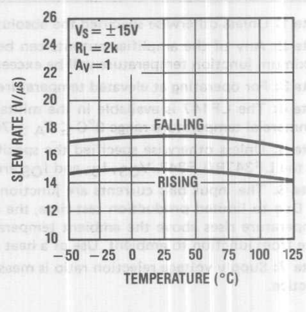
Gain Bandwidth



Bode Plot

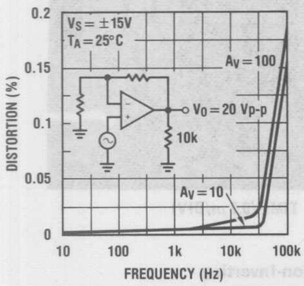


Slew Rate

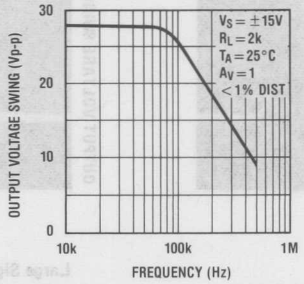


Typical Performance Characteristics (Continued)

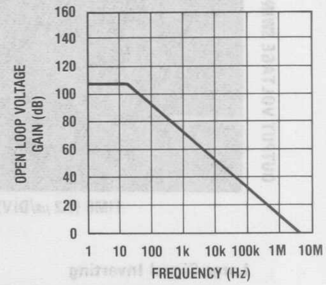
Distortion vs Frequency



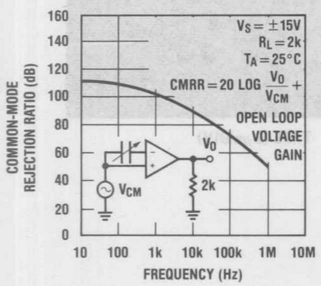
Undistorted Output Voltage Swing



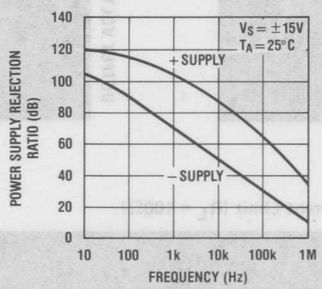
Open Loop Frequency Response



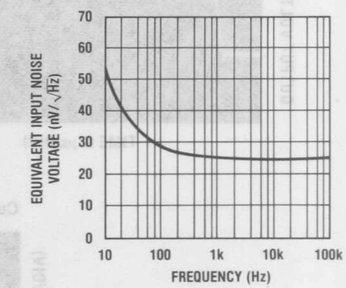
Common-Mode Rejection Ratio



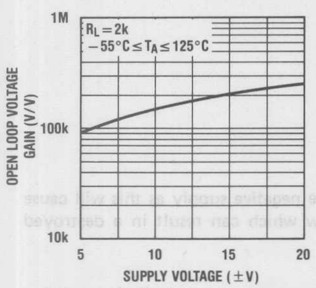
Power Supply Rejection Ratio



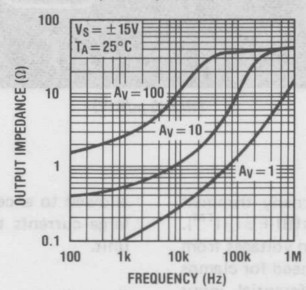
Equivalent Input Noise Voltage



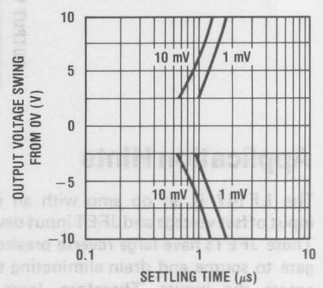
Open Loop Voltage Gain

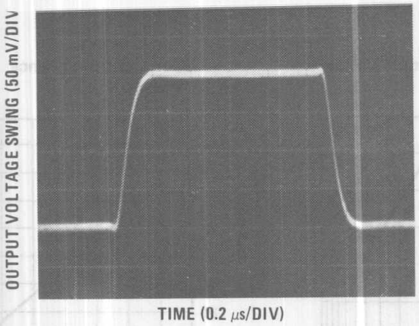


Output Impedance

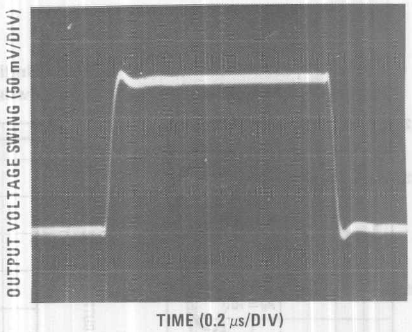


Inverter Settling Time

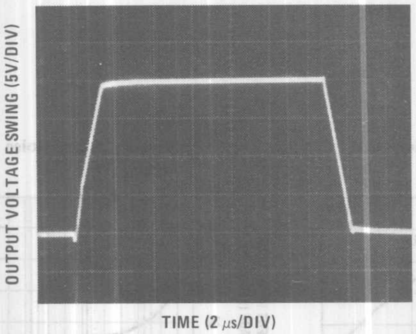


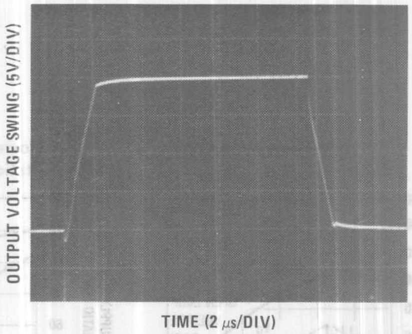


Large Signal Inverting

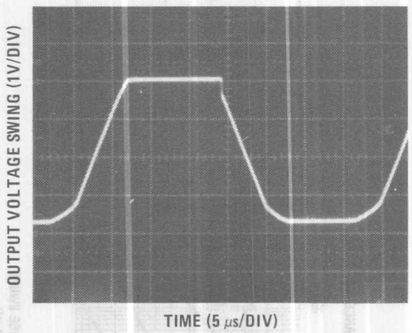


Large Signal Non-Inverting





Current Limit (R_L = 100Ω)



Application Hints

The LF147 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II™). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a

Application Hints (Continued)

high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±4.5V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF147 will drive a 2 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

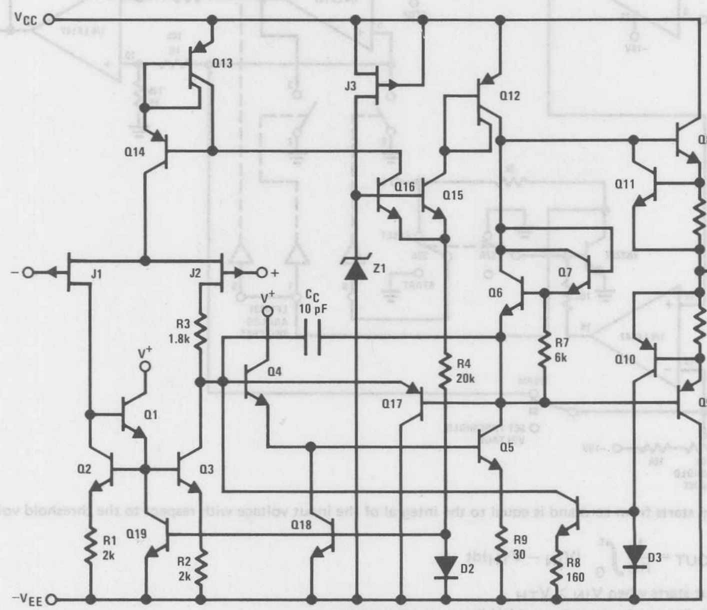
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

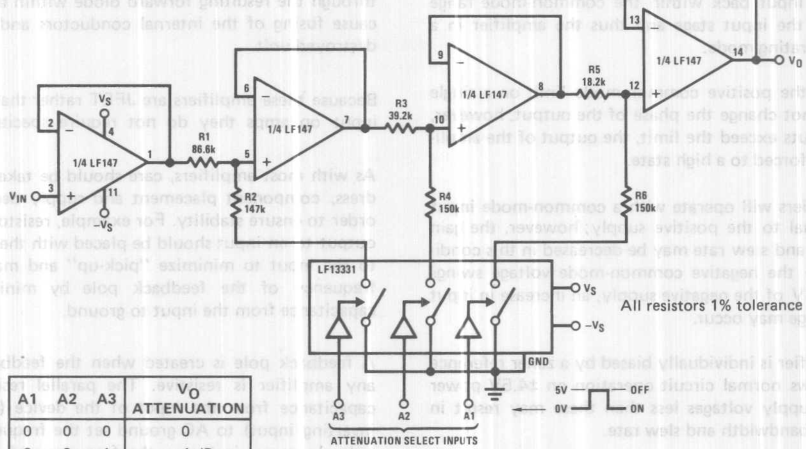
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Detailed Schematic



Typical Applications

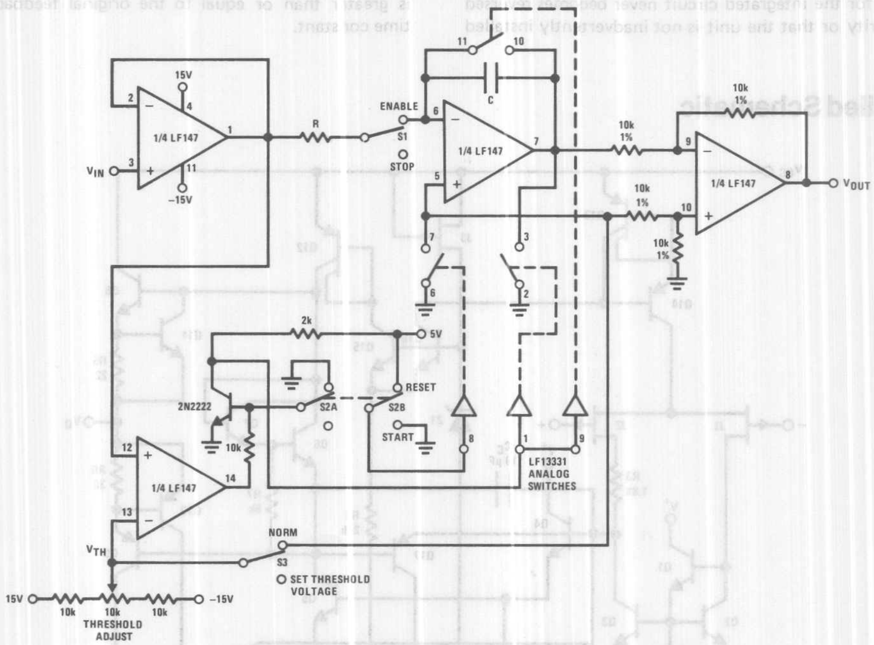
Digitally Selectable Precision Attenuator



A1	A2	A3	V_O ATTENUATION
0	0	0	0
0	0	1	−1 dB
0	1	0	−2 dB
0	1	1	−3 dB
1	0	0	−4 dB
1	0	1	−5 dB
1	1	0	−6 dB
1	1	1	−7 dB

- Accuracy of better than 0.4% with standard 1% value resistors
- No offset adjustment necessary
- Expandable to any number of stages
- Very high input impedance

Long Time Integrator with Reset, Hold and Starting Threshold Adjustment



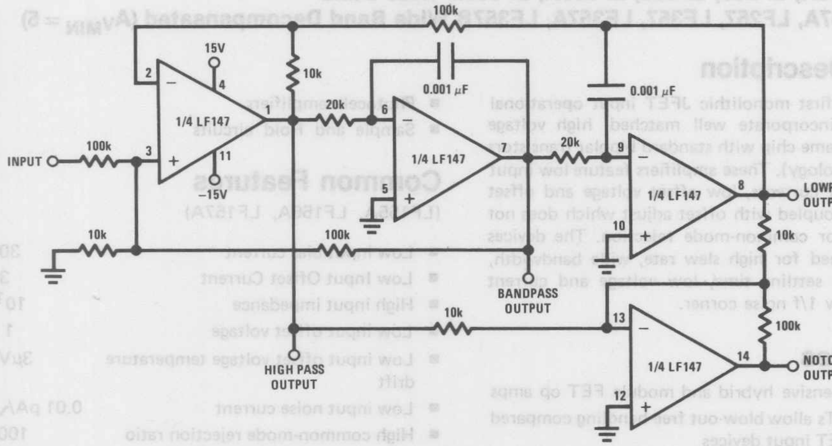
- V_{OUT} starts from zero and is equal to the integral of the input voltage with respect to the threshold voltage:

$$V_{OUT} = \frac{1}{RC}\int_0^t (V_{IN} - V_{TH})dt$$

- Output starts when $V_{IN} \geq V_{TH}$
- Switch S1 permits stopping and holding any output value
- Switch S2 resets system to zero

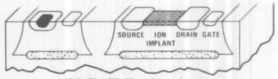
Typical Applications (Continued)

Universal State Variable Filter



For circuit shown:
$f_O = 3$ kHz, $f_{NOTCH} = 9.5$ kHz
Q = 3.4
Passband gain:
Highpass — 0.1
Bandpass — 1
Lowpass — 1
Notch — 10

- $f_O \times Q \leq 200$ kHz
- 10V peak sinusoidal output swing without slew limiting to 200 kHz
- See LM148 data sheet for design equations



BI-FET Technology

LF155/LF156/LF157 Series Monolithic JFET Input Operational Amplifiers

LF155, LF155A, LF255, LF355, LF355A, LF355B Low Supply Current
LF156, LF156A, LF256, LF356, LF356A, LF356B Wide Band
LF157, LF157A, LF257, LF357, LF357A, LF357B Wide Band Decompensated ($A_{V_{MIN}} = 5$)

General Description

These are the first monolithic JFET input operational amplifiers to incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors (BI-FET Technology). These amplifiers feature low input bias and offset currents, low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise corner.

Advantages

- Replace expensive hybrid and module FET op amps
- Rugged JFETs allow blow-out free handling compared with MOSFET input devices
- Excellent for low noise applications using either high or low source impedance—very low 1/f corner
- Offset adjust does not degrade drift or common-mode rejection as in most monolithic amplifiers
- New output stage allows use of large capacitive loads (10,000 pF) without stability problems
- Internal compensation and large differential input voltage capability

Applications

- Precision high speed integrators
- Fast D/A and A/D converters
- High impedance buffers
- Wideband, low noise, low drift amplifiers
- Logarithmic amplifiers
- Photocell amplifiers
- Sample and Hold circuits

Common Features

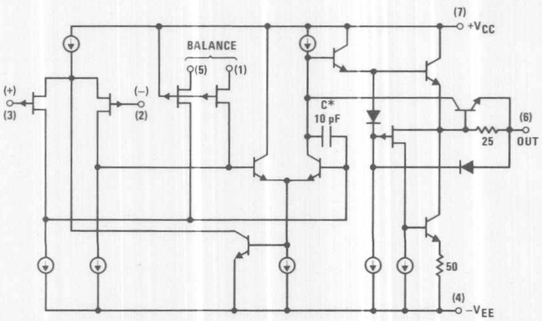
(LF155A, LF156A, LF157A)

■ Low input bias current	30 pA
■ Low Input Offset Current	3 pA
■ High input impedance	$10^{12}\Omega$
■ Low input offset voltage	1 mV
■ Low input offset voltage temperature drift	$3\mu V/^\circ C$
■ Low input noise current	$0.01\ pA/\sqrt{Hz}$
■ High common-mode rejection ratio	100 dB
■ Large dc voltage gain	106 dB

Uncommon Features

	LF155A	LF156A	LF157A ($A_V = 5$)	UNITS
■ Extremely fast settling time to 0.01%	4	1.5	1.5	μs
■ Fast slew rate	5	12	50	$V/\mu s$
■ Wide gain bandwidth	2.5	5	20	MHz
■ Low input noise voltage	20	12	12	$nV/\sqrt{Hz}$

Simplified Schematic



*C = 2 pF on LF157

Power Dissipation (P_d at 25°C) and Thermal Resistance (θ_{jA}) (Note 1)				
T_{jMAX} (H Package)	150°C	150°C	115°C	115°C
(N Package)			100°C	100°C
(H Package) P_d	670 mW	670 mW	570 mW	570 mW
θ_{jA}	150°C/W	150°C/W	150°C/W	150°C/W
(N Package) P_d			500 mW	500 mW
θ_{jA}			155°C/W	155°C/W
Differential Input Voltage	±40V	±40V	±40V	±30V
Input Voltage Range (Note 2)	±20V	±20V	±20V	±16V
Output Short Circuit Duration	Continuous	Continuous	Continuous	Continuous
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	300°C	300°C

DC Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LF155A/6A/7A			LF355A/6A/7A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$		1	2		1	2	mV
		Over Temperature			2.5			2.3	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		3	5		3	5	μV/°C
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5		μV/°C per mV
I_{OS}	Input Offset Current	$T_j = 25°C$, (Notes 3, 5)		3	10		3	10	pA
		$T_j \leq T_{HIGH}$			10			1	nA
I_B	Input Bias Current	$T_J = 25°C$, (Notes 3, 5)		30	50		30	50	pA
		$T_J \leq T_{HIGH}$			25			5	nA
R_{IN}	Input Resistance	$T_J = 25°C$		10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm15V$, $T_A = 25°C$, $V_O = \pm10V$, $R_L = 2k$	50	200		50	200		V/mV
		Over Temperature	25			25			V/mV
V_O	Output Voltage Swing	$V_S = \pm15V$, $R_L = 10k$	±12	±13		±12	±13		V
		$V_S = \pm15V$, $R_L = 2k$	±10	±12		±10	±12		V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm15V$	±11	+15.1		±11	+15.1		V
				−12			−12		V
CMRR	Common-Mode Rejection Ratio		85	100		85	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		dB

AC Electrical Characteristics $T_A = 25°C$, $V_S = \pm15V$

SYMBOL	PARAMETER	CONDITIONS	LF155A/355A			LF156A/356A			LF157A/357A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew Rate	LF155A/6A; $A_V = 1$,	3	5		10	12					V/μs
		LF157A; $A_V = 5$							40	50		V/μs
GBW	Gain Bandwidth Product			2.5		4	4.5		15	20		MHz
t_s	Settling Time to 0.01%	(Note 7)		4			1.5			1.5		μs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$										
		f = 100 Hz		25			15			15		$nV/\sqrt{Hz}$
		f = 1000 Hz		25			12			12		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	f = 100 Hz		0.01			0.01			0.01		$pA/\sqrt{Hz}$
		f = 1000 Hz		0.01			0.01			0.01		$pA/\sqrt{Hz}$
C_{IN}	Input Capacitance			3			3			3		pF

DC Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LF155/6/7 MIN	LF155/6/7 TYP	LF155/6/7 MAX	LF255/6/7 LF355B/6B/7B MIN	LF255/6/7 LF355B/6B/7B TYP	LF255/6/7 LF355B/6B/7B MAX	LF355/6/7 MIN	LF355/6/7 TYP	LF355/6/7 MAX	UNITS
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25^\circ C$		3	5		3	5		3	10	mV
		Over Temperature			7			6.5			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		5			5			5		$\mu V/^\circ C$
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5			0.5		$\mu V/^\circ C$ per mV
I_{OS}	Input Offset Current	$T_j = 25^\circ C$, (Notes 3, 5)		3	20		3	20		3	50	pA
		$T_j \leq T_{HIGH}$			20			1			2	nA
I_B	Input Bias Current	$T_J = 25^\circ C$, (Notes 3, 5)		30	100		30	100		30	200	pA
		$T_J \leq T_{HIGH}$			50			5			8	nA
R_{IN}	Input Resistance	$T_J = 25^\circ C$		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm15V$, $T_A = 25^\circ C$ $V_O = \pm10V$, $R_L = 2k$	50	200		50	200		25	200		V/mV
		Over Temperature	25			25			15			V/mV
V_O	Output Voltage Swing	$V_S = \pm15V$, $R_L = 10k$	±12	±13		±12	±13		±12	±13		V
		$V_S = \pm15V$, $R_L = 2k$	±10	±12		±10	±12		±10	±12		V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm15V$	±11	+15.1		±11	+15.1		±10	+15.1		V
				−12			−12			−12		V
CMRR	Common-Mode Rejection Ratio		85	100		85	100		80	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		80	100		dB

DC Electrical Characteristics $T_A = 25^\circ C$, $V_S = \pm15V$

PARAMETER	LF155A/155, LF255, LF355A/355B TYP	LF155A/155, LF255, LF355A/355B MAX	LF355 TYP	LF355 MAX	LF156A/156, LF256/356B TYP	LF156A/156, LF256/356B MAX	LF356A/356 TYP	LF356A/356 MAX	LF157A/157 LF257/357B TYP	LF157A/157 LF257/357B MAX	LF357A/357 TYP	LF357A/357 MAX	UNITS
Supply Current	2	4	2	4	5	7	5	10	5	7	5	10	mA

AC Electrical Characteristics $T_A = 25^\circ C$, $V_S = \pm15V$

SYMBOL	PARAMETER	CONDITIONS	LF155/255/ 355/355B TYP	LF156/256, LF356B MIN	LF156/256/ 356/356B TYP	LF157/257, LF357B MIN	LF157/257/ 357/357B TYP	UNITS
SR	Slew Rate	LF155/6: $A_V = 1$,	5	7.5	12			V/μs
		LF157: $A_V = 5$				30	50	V/μs
GBW	Gain Bandwidth Product		2.5		5		20	MHz
t_s	Settling Time to 0.01%	(Note 7)	4		1.5		1.5	μs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$						
		f = 100 Hz	25		15		15	$nV/\sqrt{Hz}$
		f = 1000 Hz	20		12		12	$nV/\sqrt{Hz}$
i_n	Equivalent Input Current Noise	f = 100 Hz	0.01		0.01		0.01	$pA/\sqrt{Hz}$
		f = 1000 Hz	0.01		0.01		0.01	$pA/\sqrt{Hz}$
C_{IN}	Input Capacitance		3		3		3	pF

Notes for Electrical Characteristics

Note 1: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{jMAX}, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d = (T_{jMAX} - T_A)/\theta_{jA}$ or the 25°C P_{dMAX}, whichever is less.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: Unless otherwise stated, these test conditions apply:

	LF155A/6A/7A LF155/6/7	LF255/6/7	LF355A/6A/7A	LF355B/6B/7B	LF355/6/7
Supply Voltage, V_S	$\pm15V \le V_S \le \pm20V$	$\pm15V \le V_S \le \pm20V$	$\pm15V \le V_S \le \pm18V$	$\pm15V \le V_S$ ±20V	$V_S = \pm15V$
T_A	$-55°C \le T_A \le +125°C$	$-25°C \le T_A \le +85°C$	$0°C \le T_A \le +70°C$	$0°C \le T_A \le +70°C$	$0°C \le T_A \le +70°C$
T_{HIGH}	+125°C	+85°C	+70°C	+70°C	+70°C

and V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.

Note 4: The Temperature Coefficient of the adjusted input offset voltage changes only a small amount (0.5μV/°C typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_j = T_A + \Theta_{jA}$ Pd where Θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

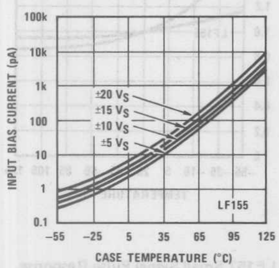
Note 6: Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

Note 7: Settling time is defined here, for a unity gain inverter connection using 2 kΩ resistors for the LF155/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. For the LF157, $A_V = -5$, the feedback resistor from output to input is 2 kΩ and the output step is 10V (See Settling Time Test Circuit, page 3-30).

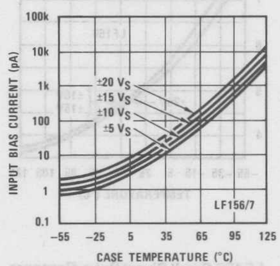
Typical DC Performance Characteristics

Curves are for LF155, LF156 and LF157 unless otherwise specified.

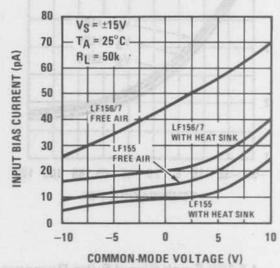
Input Bias Current



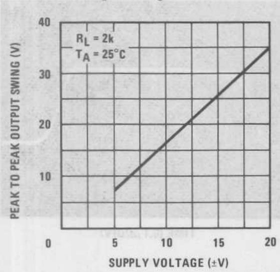
Input Bias Current



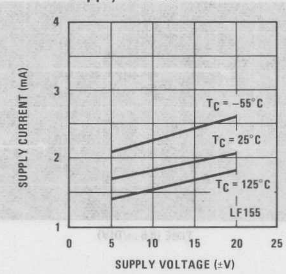
Input Bias Current



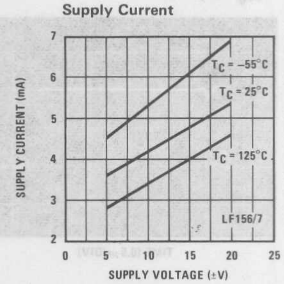
Voltage Swing



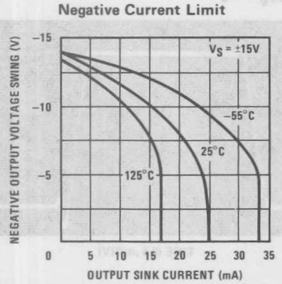
Supply Current



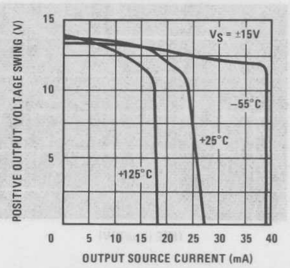
Supply Current



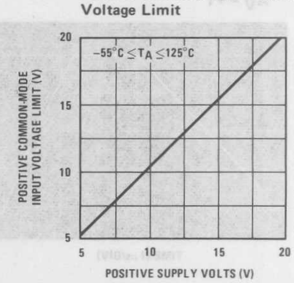
Negative Current Limit



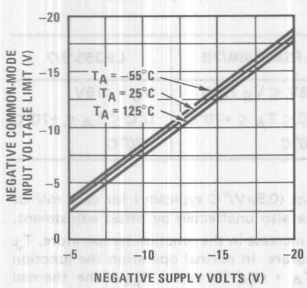
Positive Current Limit



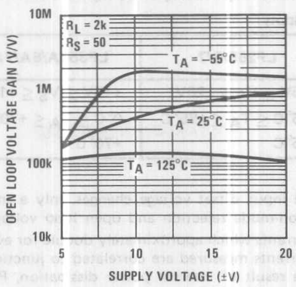
Positive Common-Mode Input Voltage Limit



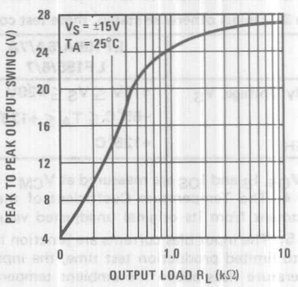
Voltage Limit



Open Loop Voltage Gain

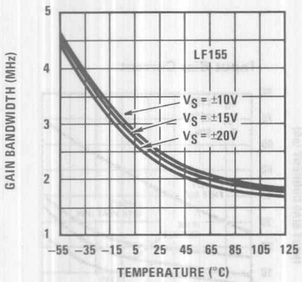


Output Voltage Swing

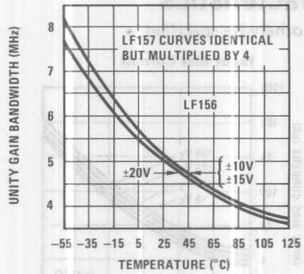


Typical AC Performance Characteristics

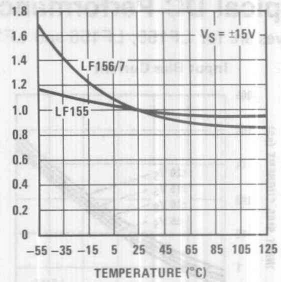
Gain Bandwidth



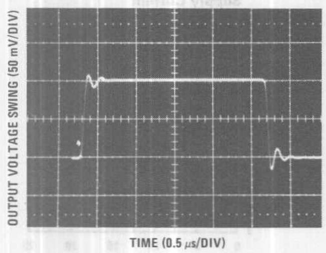
Gain Bandwidth



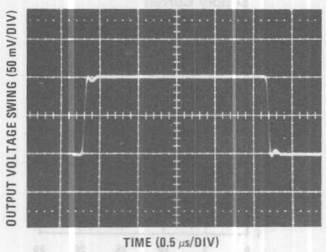
Normalized Slew Rate



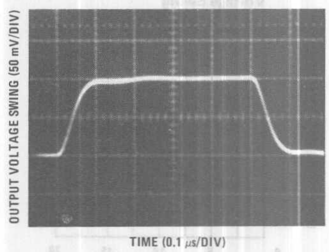
LF155 Small Signal Pulse Response, $A_V = +1$



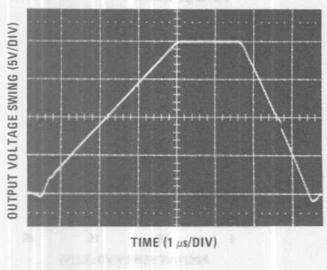
LF156 Small Signal Pulse Response, $A_V = +1$



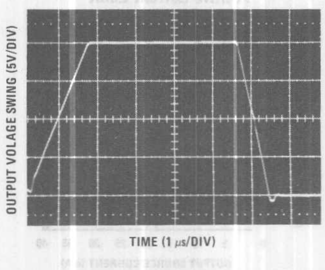
LF157 Small Signal Pulse Response, $A_V = +5$



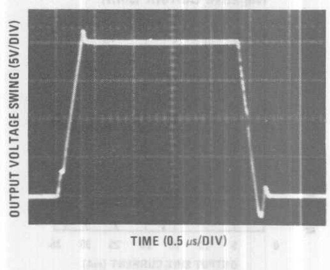
LF155 Large Signal Pulse Response, $A_V = +1$



LF156 Large Signal Pulse Response, $A_V = +1$

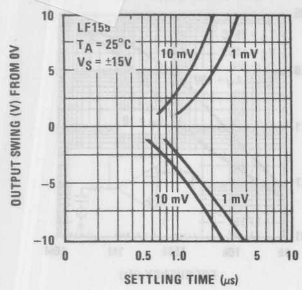


LF157 Large Signal Pulse Response, $A_V = +5$

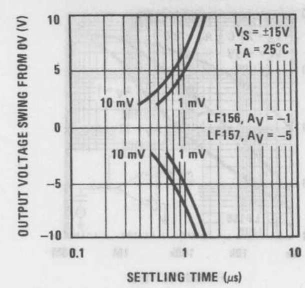


Performance Characteristics (Continued)

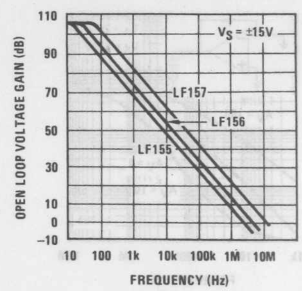
Settling Time



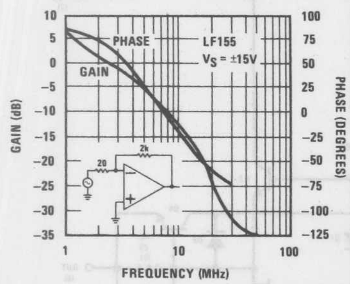
Inverter Settling Time



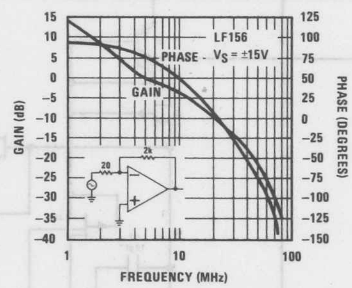
Open Loop Frequency Response



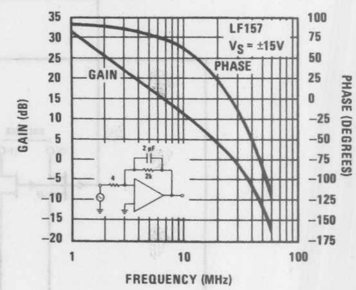
Bode Plot



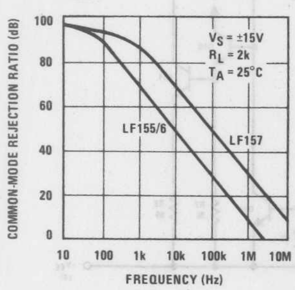
Bode Plot



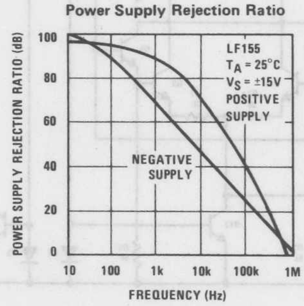
Bode Plot



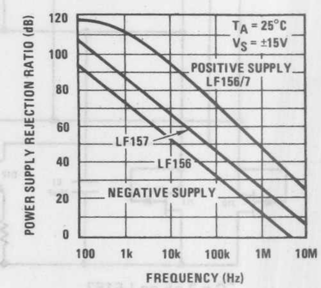
Common-Mode Rejection Ratio



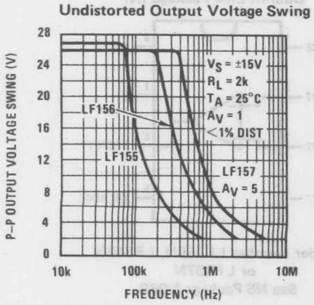
Power Supply Rejection Ratio



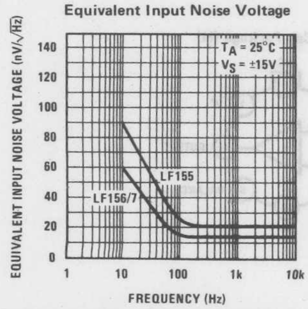
Power Supply Rejection Ratio



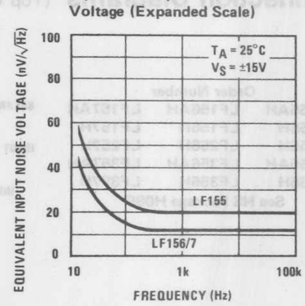
Undistorted Output Voltage Swing



Equivalent Input Noise Voltage

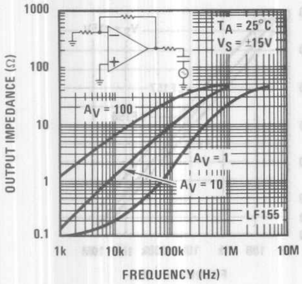


Equivalent Input Noise Voltage (Expanded Scale)

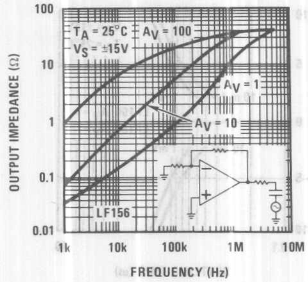


Typical AC Performance Characteristics (Continued)

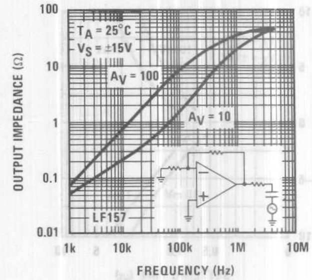
Output Impedance



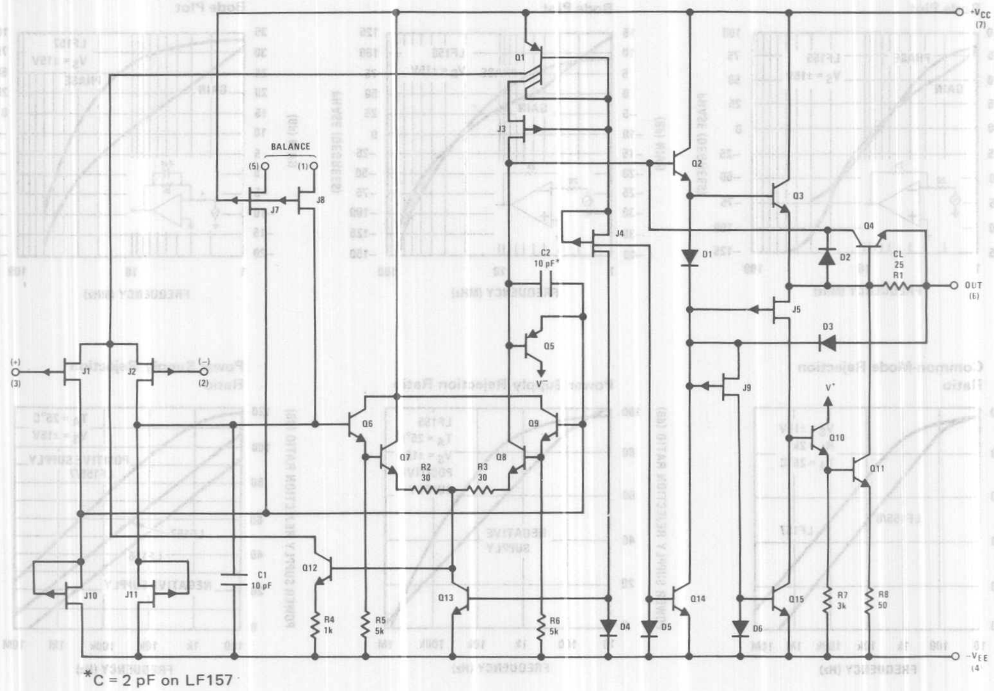
Output Impedance



Output Impedance



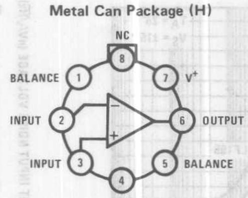
Detailed Schematic



*C = 2 pF on LF157

Connection Diagrams (Top Views)

Metal Can Package (H)

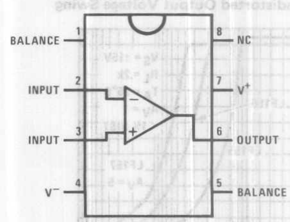


Order Number

LF155AH	LF156AH	LF157AH
LF155H	LF156H	LF157H
LF255H	LF256H	LF257H
LF355AH	LF356AH	LF357AH
LF355H	LF356H	LF357H

See NS Package H08C

Dual-In-Line Package (N)



Order Number LF355N, LF356N or LF357N

See NS Package N08B

voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accomodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed

... an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

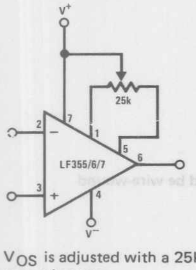
All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltage.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

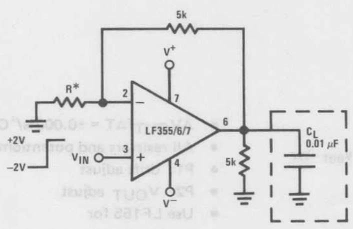
Typical Circuit Connections

V_{OS} Adjustment



- V_{OS} is adjusted with a 25k potentiometer
- The potentiometer wiper is connected to V^+
- For potentiometers with temperature coefficient of 100 ppm/°C or less the additional drift with adjust is ≈ 0.5 μV/°C/mV of adjustment
- Typical overall drift: 5 μV/°C ±(0.5 μV/°C/mV of adj.)

Driving Capacitive Loads



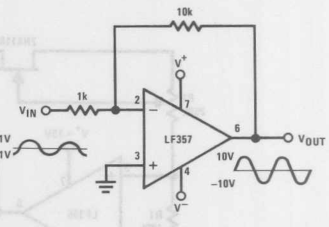
*LF155/6 R = 5k
LF157 R = 1.25k

Due to a unique output stage design, these amplifiers have the ability to drive large capacitive loads and still maintain stability. $C_{L(MAX)} \cong 0.01\ \mu F$.

Overshoot ≤ 20%

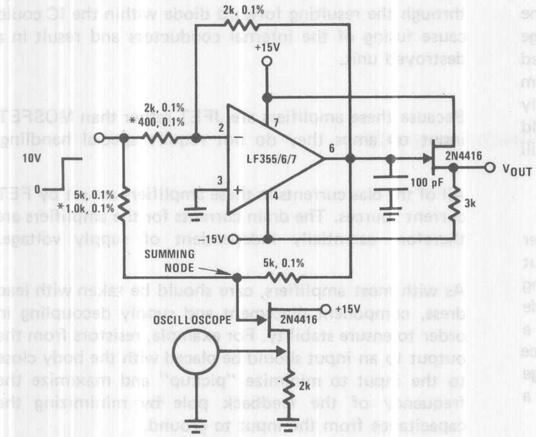
Settling time (t_s) ≅ 5 μs

LF157. A Large Power BW Amplifier



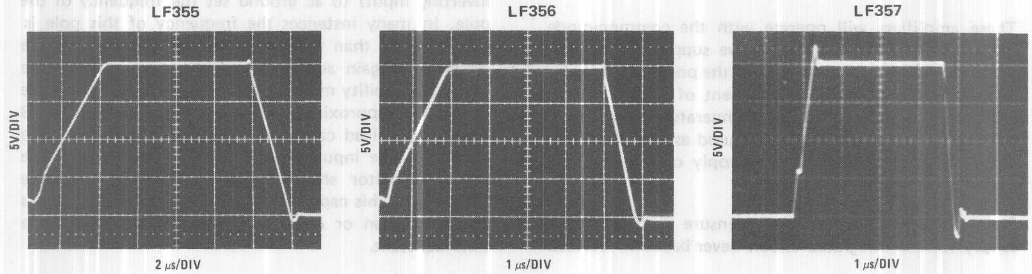
For distortion ≤ 1% and a 20 Vp-p V_{OUT} swing, power bandwidth is: 500 kHz.

Settling Time Test Circuit

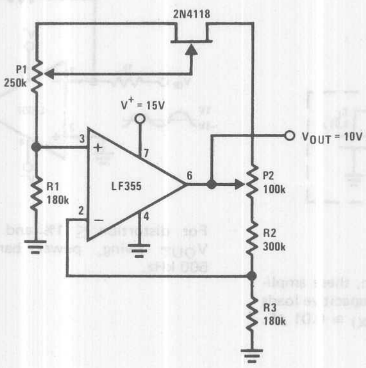


- Settling time is tested with the LF155/6 connected as unity gain inverter and LF157 connected for $A_V = -5$
- FET used to isolate the probe capacitance
- Output = 10V step
- $A_V = -5$ for LF157

Large Signal Inverter Output, V_{OUT} (from Settling Time Circuit)



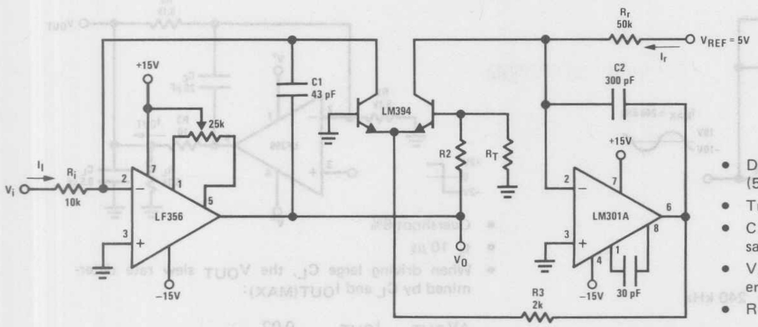
Low Drift Adjustable Voltage Reference



- $\Delta V_{OUT}/\Delta T = \pm 0.002\%/°C$
- All resistors and potentiometers should be wire-wound
- P1: drift adjust
- P2: V_{OUT} adjust
- Use LF155 for
  - ▲ Low I_B
  - ▲ Low drift
  - ▲ Low supply current

Typical Applications (Continued)

Fast Logarithmic Converter

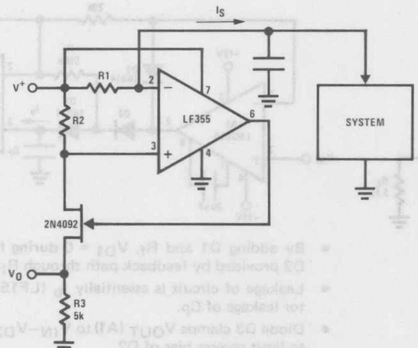


- Dynamic range: 100 $\mu A \leq I_i \leq$ 1 mA (5 decades), $|V_O|$ = 1V/decade
- Transient response: 3 μs for ΔI_i = 1 decade
- C1, C2, R2, R3: added dynamic compensation
- V_{OS} adjust the LF156 to minimize quiescent error
- R_T: Tel Labs type Q81 + 0.3%/°C

$$|V_{OUT}| = \left[1 + \frac{R2}{R_T}\right] \frac{kT}{q} \ln V_i \left[\frac{R_r}{V_{REF}\,R_i}\right] = \log V_i \frac{1}{R_i\,I_r}$$

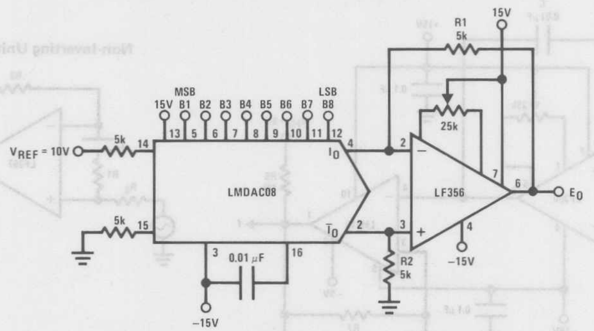
R2 = 15.7k, R_T = 1k, 0.3%/°C (for temperature compensation)

Precision Current Monitor



- V_O = 5 R1/R2 (V/mA of I_S)
- R1, R2, R3: 0.1% resistors
- Use LF155 for
  - ▲ Common-mode range to supply range
  - ▲ Low I_B
  - ▲ Low V_{OS}
  - ▲ Low supply current

8-Bit D/A Converter with Symmetrical Offset Binary Operation

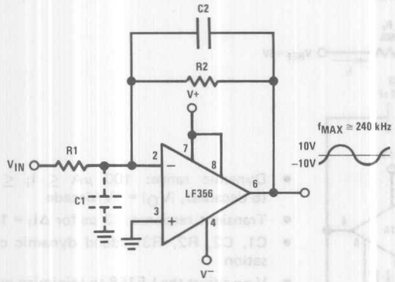


- R1, R2 should be matched within ±0.05%
- Full-scale response time: 3 μs

E_O	B1	B2	B3	B4	B5	B6	B7	B8	COMMENTS
+9.920	1	1	1	1	1	1	1	1	Positive Full-Scale
+0.040	1	0	0	0	0	0	0	0	(+) Zero-Scale
−0.040	0	1	1	1	1	1	1	1	(−) Zero-Scale
−9.920	0	0	0	0	0	0	0	0	Negative Full-Scale

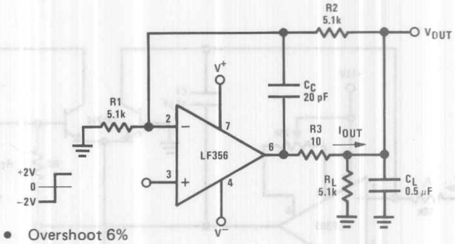
Typical Applications (Continued)

Wide BW Low Noise, Low Drift Amplifier



- Power BW: $f_{MAX} = \dfrac{S_r}{2\pi V_P} \cong 240$ kHz
- Parasitic input capacitance C1 ≅ (3 pF for LF155, LF156 and LF157 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate add C2 such that: R2C2 ≅ R1C1.

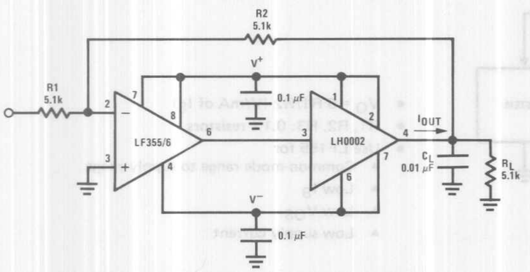
Isolating Large Capacitive Loads



- Overshoot 6%
- t_s 10 µs
- When driving large C_L, the V_{OUT} slew rate determined by C_L and $I_{OUT(MAX)}$:

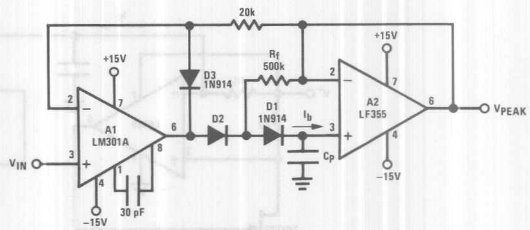
$$\frac{\Delta V_{OUT}}{\Delta T} = \frac{I_{OUT}}{C_L} \cong \frac{0.02}{0.5} \text{ V/µs} = 0.04 \text{ V/µs (with } C_L \text{ shown)}$$

Boosting the LF156 with a Current Amplifier



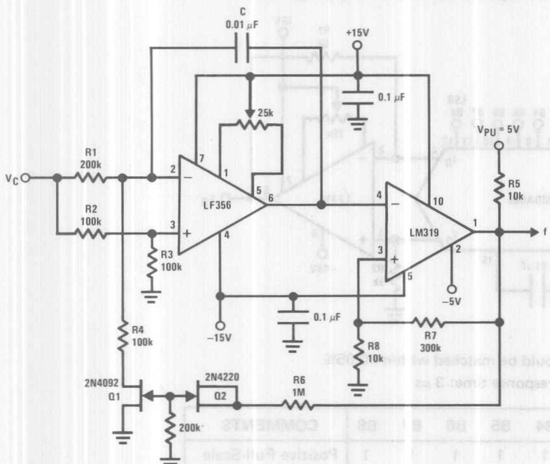
- $I_{OUT(MAX)} \cong 150$ mA (will drive $R_L \geq 100\Omega$)
- $\dfrac{\Delta V_{OUT}}{\Delta T} = \dfrac{0.15}{10^{-2}}$ V/µs (with C_L shown)
- No additional phase shift added by the current amplifier

Low Drift Peak Detector



- By adding D1 and R_f, $V_{D1} = 0$ during hold mode. Leakage of D2 provided by feedback path through R_f.
- Leakage of circuit is essentially I_b (LF155, LF156) plus capacitor leakage of C_P.
- Diode D3 clamps V_{OUT} (A1) to $V_{IN} - V_{D3}$ to improve speed and to limit reverse bias of D2.
- Maximum input frequency should be << $1/2\pi R_f C_{D2}$ where C_{D2} is the shunt capacitance of D2.

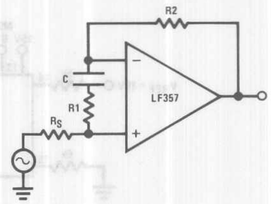
3 Decades VCO



$$f = \frac{V_C\,(R8+R7)}{[8\,V_{PU}\,R8\,R1]\,C}, \quad 0 \leq V_C \leq 30\text{V}, \; 10 \text{ Hz} \leq f \leq 10 \text{ kHz}$$

R1, R4 matched. Linearity 0.1% over 2 decades.

Non-Inverting Unity Gain Operation for LF157



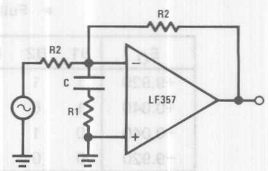
$$R1C \geq \frac{1}{(2\pi)\,(5 \text{ MHz})}$$

$$R1 = \frac{R2 + R_S}{4}$$

$A_{V(DC)} = 1$

$f_{-3\,dB} \approx 5$ MHz

Inverting Unity Gain for LF157



$$R1C \geq \frac{1}{(2\pi)\,(5 \text{ MHz})}$$

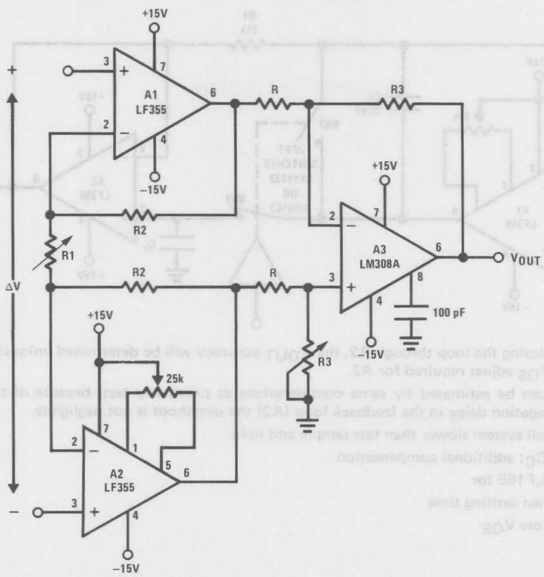
$$R1 = \frac{R2}{4}$$

$A_{V(DC)} = -1$

$f_{-3\,dB} \approx 5$ MHz

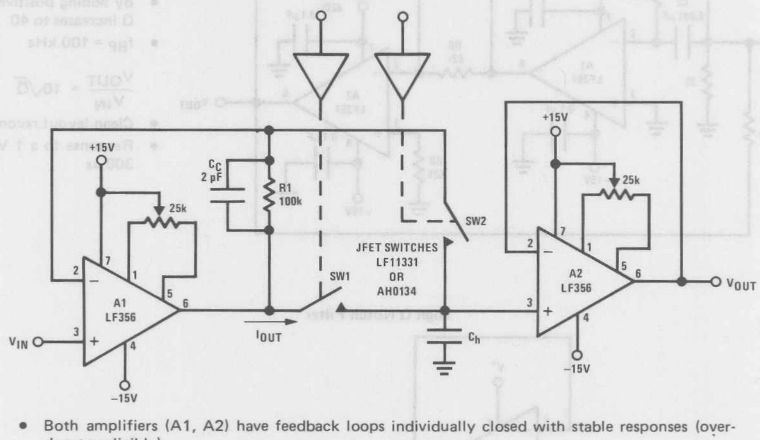
Typical Applications (Continued)

High Impedance, Low Drift Instrumentation Amplifier



- $V_{OUT} = \frac{R3}{R}\left[\frac{2R2}{R1} + 1\right] \Delta V$, $V^- + 2V \le V_{IN}$ common-mode $\le V^+$
- System V_{OS} adjusted via A2 V_{OS} adjust
- Trim R3 to boost up CMRR to 120 dB. Instrumentation amplifier Resistor array RA201 (National Semiconductor) recommended

Fast Sample and Hold

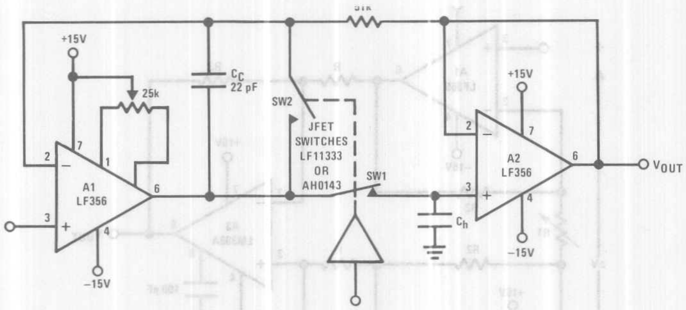


- Both amplifiers (A1, A2) have feedback loops individually closed with stable responses (overshoot negligible)
- Acquisition time T_A, estimated by:

  $T_A \cong \left[\frac{2R_{ON}, V_{IN}, C_h}{S_r}\right]^{1/2}$ provided that:

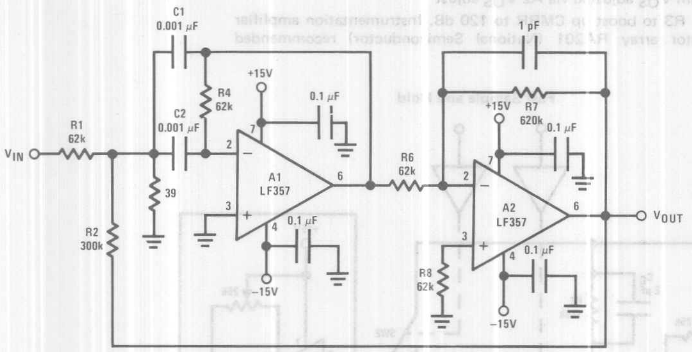
  $V_{IN} < 2\pi S_r R_{ON} C_h$ and $T_A > \frac{V_{IN} C_h}{I_{OUT(MAX)}}$, R_{ON} is of SW1

  If inequality not satisfied: $T_A \cong \frac{V_{IN} C_h}{20 \text{ mA}}$
- LF156 developes full S_r output capability for $V_{IN} \ge 1V$
- Addition of SW2 improves accuracy by putting the voltage drop across SW1 inside the feedback loop
- Overall accuracy of system determined by the accuracy of both amplifiers, A1 and A2



- By closing the loop through A2, the V_{OUT} accuracy will be determined uniquely by A1. No V_{OS} adjust required for A2.
- T_A can be estimated by same considerations as previously but, because of the added propagation delay in the feedback loop (A2) the overshoot is not negligible.
- Overall system slower than fast sample and hold
- R1, C_C: additional compensation
- Use LF156 for
  - ▲ Fast settling time
  - ▲ Low V_{OS}

High Q Band Pass Filter

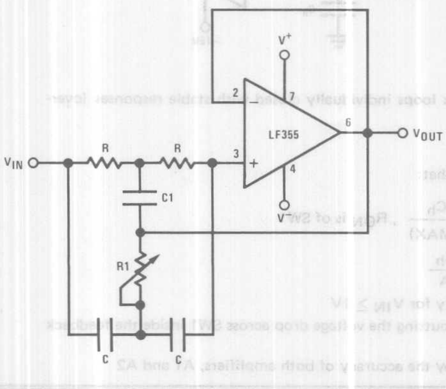


- By adding positive feedback (R2) Q increases to 40
- f_{BP} = 100 kHz

$$\frac{V_{OUT}}{V_{IN}} = 10\sqrt{Q}$$

- Clean layout recommended
- Response to a 1 Vp-p tone burst: 300 μs

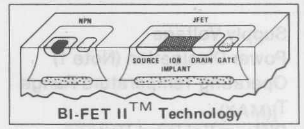
High Q Notch Filter



- 2R1 = R = 10 MΩ
  2C = C1 = 300 pF
- Capacitors should be matched to obtain high Q
- f_{NOTCH} = 120 Hz, notch = −55 dB, Q > 100
- Use LF155 for
  - ▲ Low I_B
  - ▲ Low supply current

National Semiconductor

Operational Amplifiers/Buffers



BI-FET II™ Technology

LF351 Wide Bandwidth JFET Input Operational Amplifier

General Description

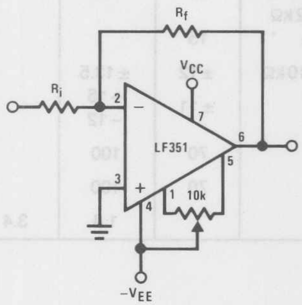
The LF351 is a low cost high speed JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF351 is pin compatible with the standard LM741 and uses the same offset voltage adjustment circuitry. This feature allows designers to immediately upgrade the overall performance of existing LM741 designs.

The LF351 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift, but for applications where these requirements are critical, the LF356 is recommended. If maximum supply current is important, however, the LF351 is the better choice.

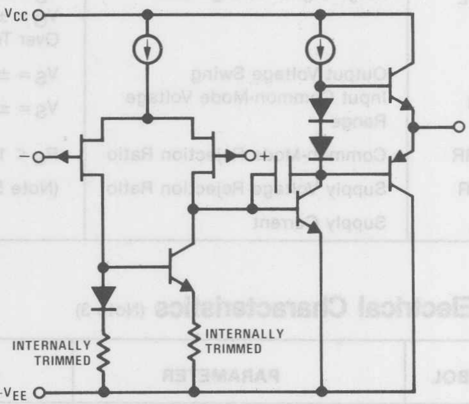
Features

- Internally trimmed offset voltage — 10 mV
- Low input bias current — 50 pA
- Low input noise voltage — 16 nV/√Hz
- Low input noise current — 0.01 pA/√Hz
- Wide gain bandwidth — 4 MHz
- High slew rate — 13 V/μs
- Low supply current — 1.8 mA
- High input impedance — $10^{12}\Omega$
- Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20\,Vp\text{-}p$, BW = 20 Hz-20 kHz — <0.02%
- Low 1/f noise corner — 50 Hz
- Fast settling time to 0.01% — 2 μs

Typical Connection

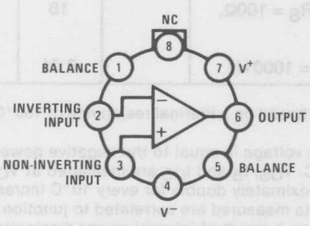


Simplified Schematic



Connection Diagrams (Top Views)

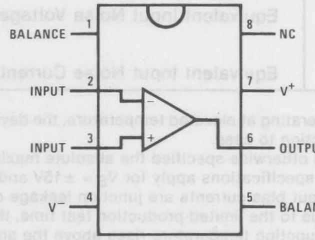
Metal Can Package



Note. Pin 4 connected to case.

Order Number LF351H
See NS Package H08C

Dual-In-Line Package



Order Number LF351N
See NS Package N08A

Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation (Note 1)	500 mW
Operating Temperature Range	0°C to +70°C
$T_{j(MAX)}$	115°C
Differential Input Voltage	±30V
Input Voltage Range (Note 2)	±15V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LF351 MIN	LF351 TYP	LF351 MAX	UNITS
V_{OS}	Input Offset Voltage	$R_S = 10\,k\Omega$, $T_A = 25°C$ Over Temperature		5	10 13	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\,k\Omega$		10		μV/°C
I_{OS}	Input Offset Current	$T_j = 25°C$, (Notes 3, 4) $T_j \leq 70°C$		25	100 4	pA nA
I_B	Input Bias Current	$T_j = 25°C$, (Notes 3, 4) $T_j \leq 70°C$		50	200 8	pA nA
R_{IN}	Input Resistance	$T_j = 25°C$		10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $T_A = 25°C$ $V_O = \pm 10V$, $R_L = 2\,k\Omega$ Over Temperature	25 15	100		V/mV V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\,k\Omega$	±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm 15V$	±11	+15 −12		V V
CMRR	Common-Mode Rejection Ratio	$R_S \leq 10\,k\Omega$	70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 5)	70	100		dB
I_S	Supply Current			1.8	3.4	mA

AC Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LF351 MIN	LF351 TYP	LF351 MAX	UNITS
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$		13		V/μs
GBW	Gain Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$		4		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, f = 1000 Hz		16		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_j = 25°C$, f = 1000 Hz		0.01		$pA/\sqrt{Hz}$

Note 1: For operating at elevated temperature, the device must be derated based on a thermal resistance of 150°C/W junction to ambient or 45°C/W junction to case.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

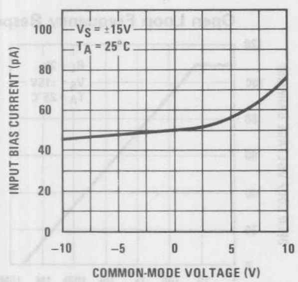
Note 3: These specifications apply for $V_S = \pm 15V$ and $0°C \leq T_A \leq +70°C$. V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.

Note 4: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \Theta_{jA} P_D$ where Θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

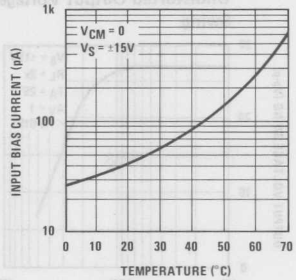
Note 5.: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

Typical Performance Characteristics

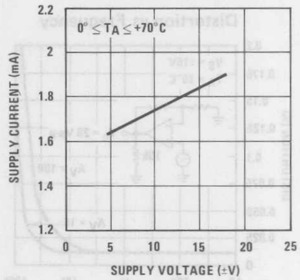
Input Bias Current



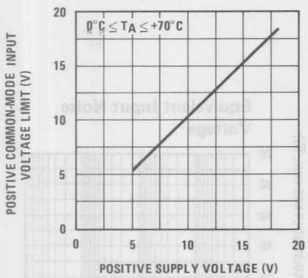
Input Bias Current



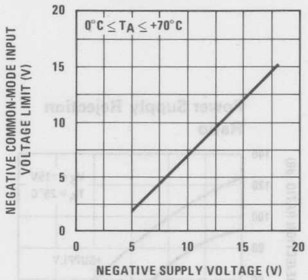
Supply Current



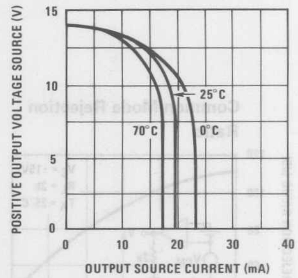
Positive Common-Mode Input Voltage Limit



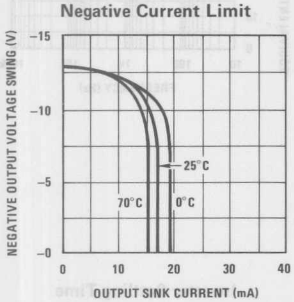
Negative Common-Mode Input Voltage Limit



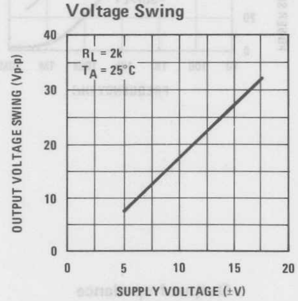
Positive Current Limit



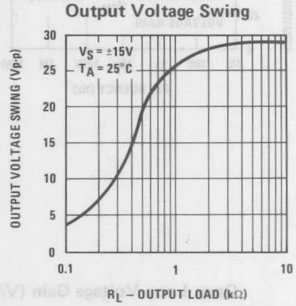
Negative Current Limit



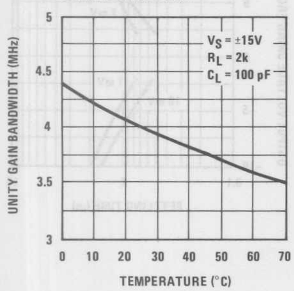
Voltage Swing



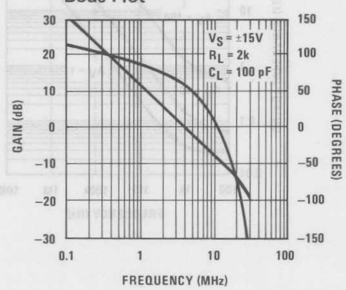
Output Voltage Swing



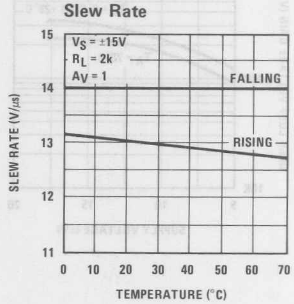
Gain Bandwidth



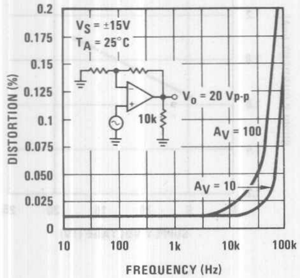
Bode Plot



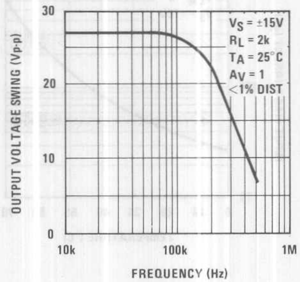
Slew Rate



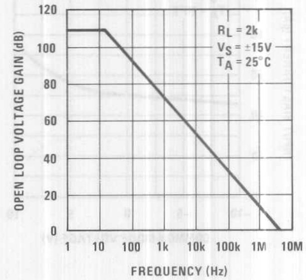
Distortion vs Frequency



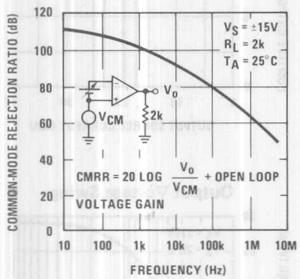
Undistorted Output Voltage Swing



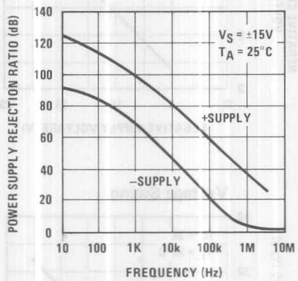
Open Loop Frequency Response



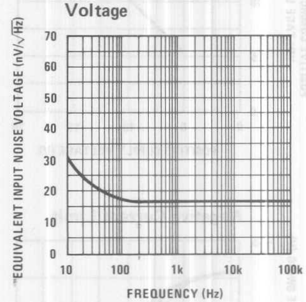
Common-Mode Rejection Ratio



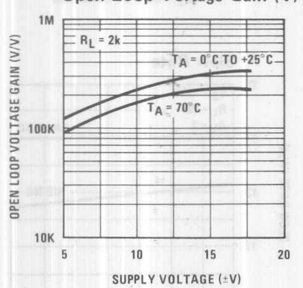
Power Supply Rejection Ratio



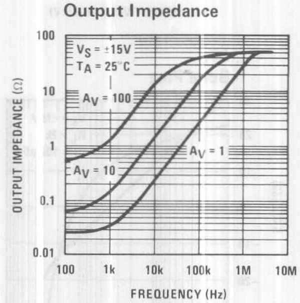
Equivalent Input Noise Voltage



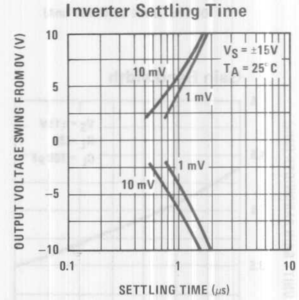
Open Loop Voltage Gain (V/V)



Output Impedance

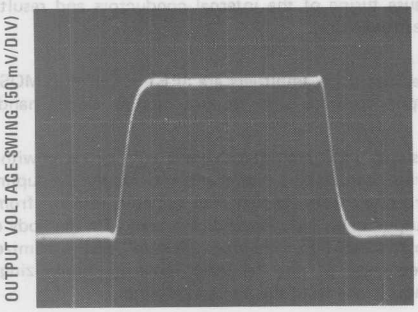


Inverter Settling Time

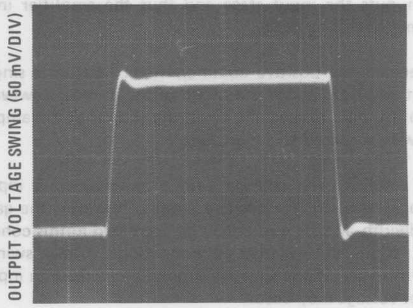


Pulse Response

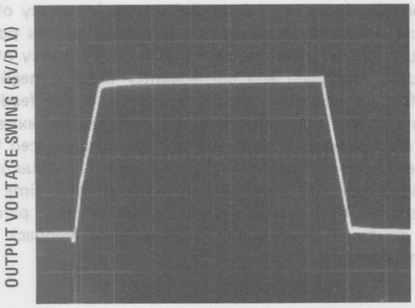
Small Signal Inverting



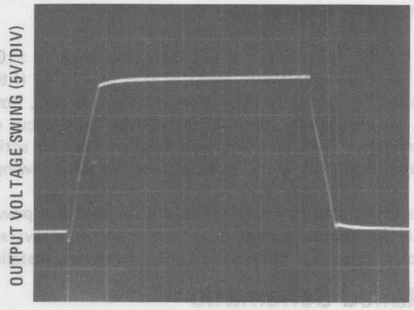
Small Signal Non-Inverting



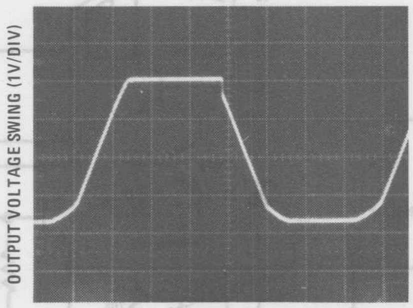
Large Signal Inverting



Large Signal Non-Inverting



Current Limit ($R_L = 100\Omega$)



Application Hints

The LF351 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II™). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a

Application Hints (Continued)

high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The LF351 is biased by a zener reference which allows normal circuit operation on ±4V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF351 will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

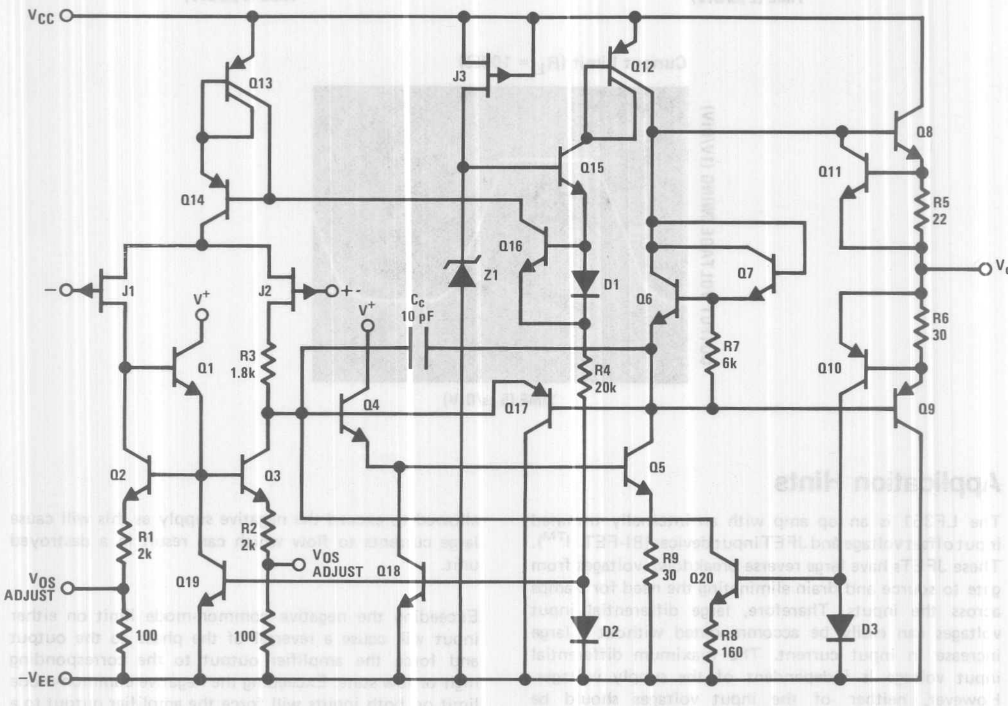
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

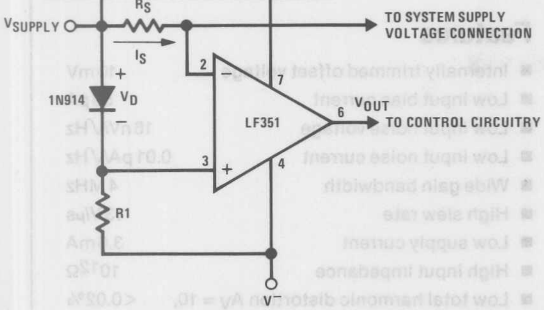
As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Detailed Schematic

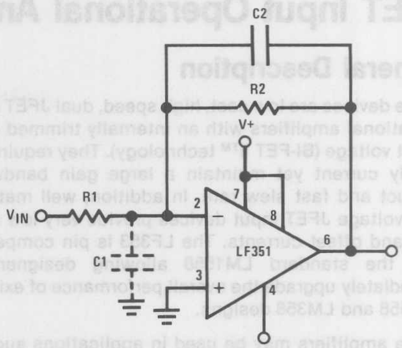


Supply Current Indicator/Limiter



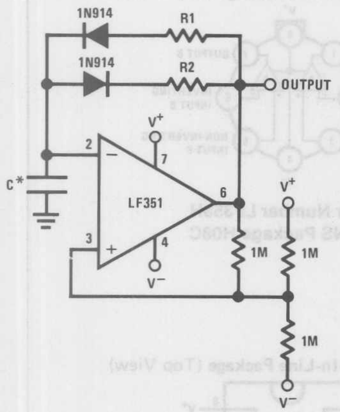
- V_{OUT} switches high when $R_S I_S > V_D$

Hi-Z_{IN} Inverting Amplifier



Parasitic input capacitance C1 ≅ (3 pF for LF351 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate, add C2 such that: R2C2 ≅ R1C1.

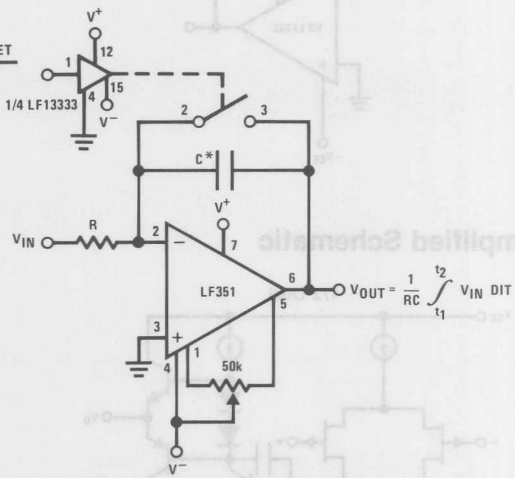
Ultra-Low (or High) Duty Cycle Pulse Generator



- $t_{OUTPUT\ HIGH} \approx R1C\ \ell n \dfrac{4.8 - 2V_S}{4.8 - V_S}$
- $t_{OUTPUT\ LOW} \approx R2C\ \ell n \dfrac{2V_S - 7.8}{V_S - 7.8}$

where $V_S = V^+ + |V^-|$
*low leakage capacitor

Long Time Integrator



* Low leakage capacitor
- 50k pot used for less sensitive V_{OS} adjust

LF353 Wide Bandwidth Dual JFET Input Operational Amplifier

BI-FET II™ Technology

General Description

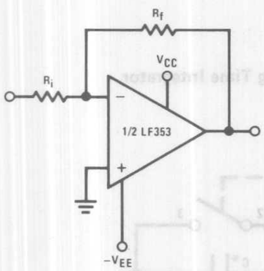
These devices are low cost, high speed, dual JFET input operational amplifiers with an internally trimmed input offset voltage (BI-FET II™ technology). They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF353 is pin compatible with the standard LM1558 allowing designers to immediately upgrade the overall performance of existing LM1558 and LM358 designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices also exhibit low noise and offset voltage drift.

Features

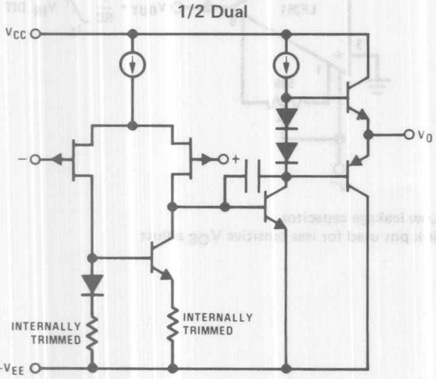
- Internally trimmed offset voltage — 10 mV
- Low input bias current — 50 pA
- Low input noise voltage — $16\,nV/\sqrt{Hz}$
- Low input noise current — $0.01\,pA/\sqrt{Hz}$
- Wide gain bandwidth — 4 MHz
- High slew rate — 13 V/μs
- Low supply current — 3.6 mA
- High input impedance — $10^{12}\Omega$
- Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20\,Vp-p$, BW = 20 Hz-20 kHz — <0.02%
- Low 1/f noise corner — 50 Hz
- Fast settling time to 0.01% — 2 μs

Typical Connection



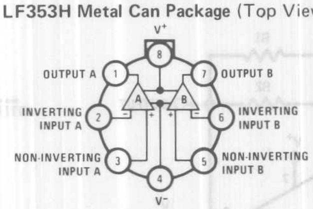
Simplified Schematic

1/2 Dual



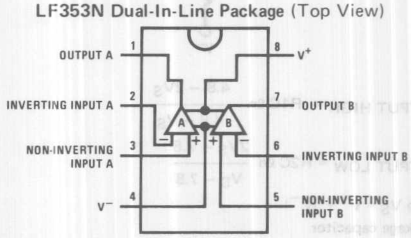
Connection Diagrams

LF353H Metal Can Package (Top View)



Order Number LF353H
See NS Package H08C

LF353N Dual-In-Line Package (Top View)



Order Number LF353N
See NS Package N08A

Absolute Maximum Ratings

Supply Voltage	±18V	Input Voltage Range (Note 2)	±15V
Power Dissipation (Note 1)	500 mW	Output Short Circuit Duration	Continuous
Operating Temperature Range	0°C to +70°C	Storage Temperature Range	−65°C to +150°C
$T_{j(MAX)}$	115°C	Lead Temperature (Soldering, 10 seconds)	300°C
Differential Input Voltage	±30V		

DC Electrical Characteristics (Note 4)

SYMBOL	PARAMETER	CONDITIONS	LF353 MIN	LF353 TYP	LF353 MAX	UNITS
V_{OS}	Input Offset Voltage	$R_S = 10\,k\Omega$, $T_A = 25°C$ Over Temperature		5	10 13	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\,k\Omega$		10		$\mu V/°C$
I_{OS}	Input Offset Current	$T_j = 25°C$, (Notes 4, 5) $T_j \leq 70°C$		25	100 4	pA nA
I_B	Input Bias Current	$T_j = 25°C$, (Notes 4, 5) $T_j \leq 70°C$		50	200 8	pA nA
R_{IN}	Input Resistance	$T_j = 25°C$		10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $T_A = 25°C$ $V_O = \pm 10V$, $R_L = 2\,k\Omega$ Over Temperature	25 15	100		V/mV V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\,k\Omega$	±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm 15V$	±11	+15 −12		V V
CMRR	Common-Mode Rejection Ratio	$R_S \leq 10\,k\Omega$	70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	70	100		dB
I_S	Supply Current			3.6	6.5	mA

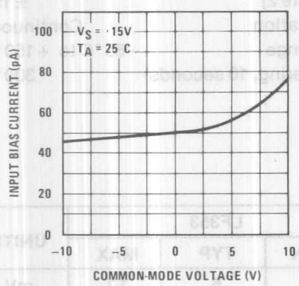
AC Electrical Characteristics (Note 4)

SYMBOL	PARAMETER	CONDITIONS	LF353 MIN	LF353 TYP	LF353 MAX	UNITS
	Amplifier to Amplifier Coupling	$T_A = 25°C$, f = 1 Hz–20 kHz (Input Referred)		−120		dB
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$		13		$V/\mu s$
GBW	Gain Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$		4		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, f = 1000 Hz		16		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_j = 25°C$, f = 1000 Hz		0.01		$pA/\sqrt{Hz}$

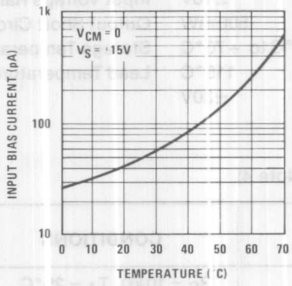
Note 1: For operating at elevated temperature, the device must be derated based on a thermal resistance of 160°C/W junction to ambient for the N package, and 150°C/W junction to ambient for the H package.
Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
Note 3: The power dissipation limit, however, cannot be exceeded.
Note 4: These specifications apply for $V_S = \pm 15V$ and $0°C \leq T_A \leq +70°C$. V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.
Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \Theta_{jA} P_D$ where Θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.
Note 6.: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

Typical Performance Characteristics

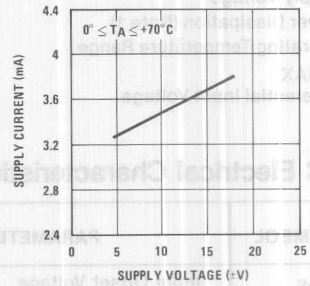
Input Bias Current



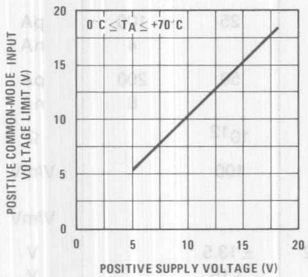
Input Bias Current



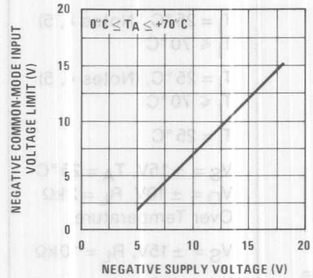
Supply Current



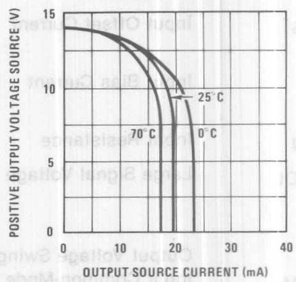
Positive Common-Mode Input Voltage Limit



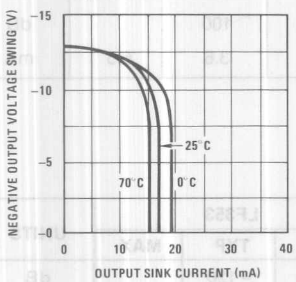
Negative Common-Mode Input Voltage Limit



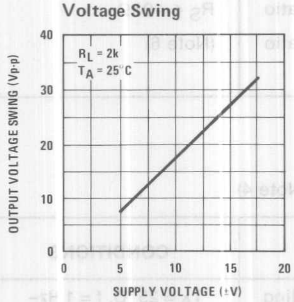
Positive Current Limit



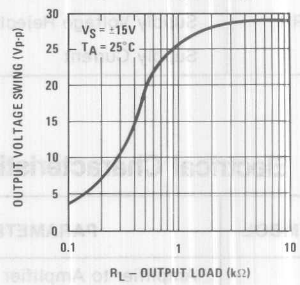
Negative Current Limit



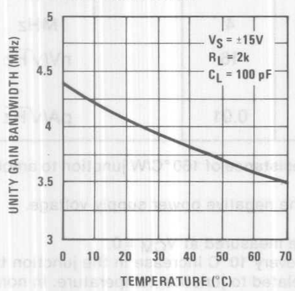
Voltage Swing



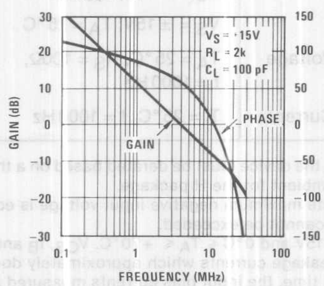
Output Voltage Swing



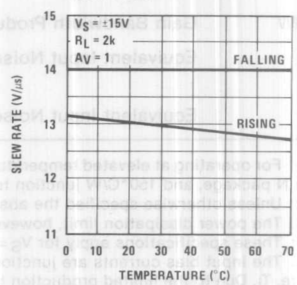
Gain Bandwidth



Bode Plot

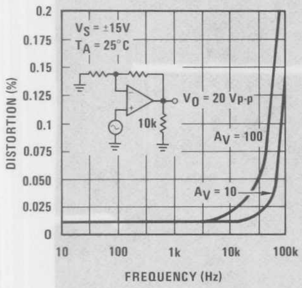


Slew Rate

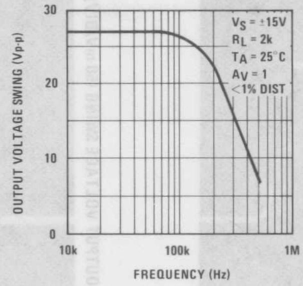


Typical Performance Characteristics (Continued)

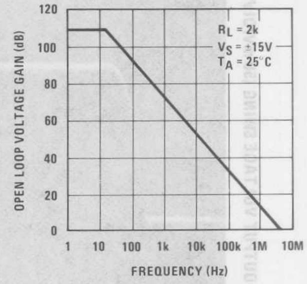
Distortion vs Frequency



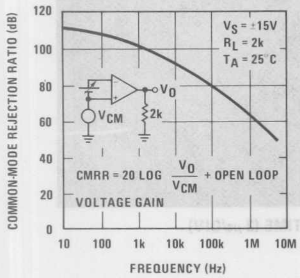
Undistorted Output Voltage Swing



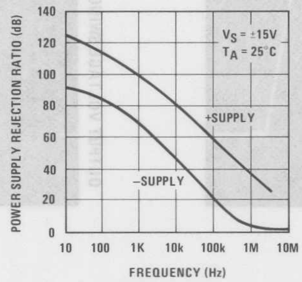
Open Loop Frequency Response



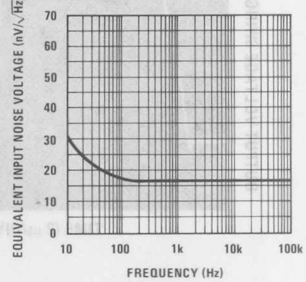
Common-Mode Rejection Ratio



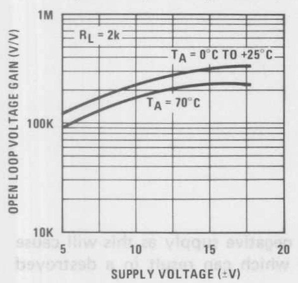
Power Supply Rejection Ratio



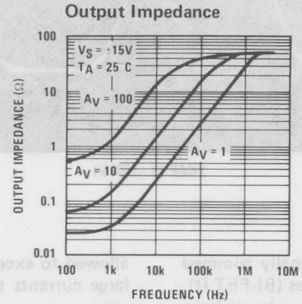
Equivalent Input Noise Voltage



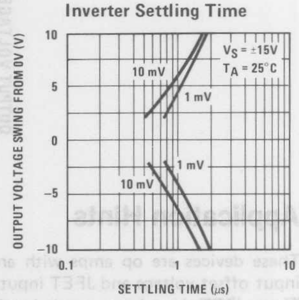
Open Loop Voltage Gain (V/V)



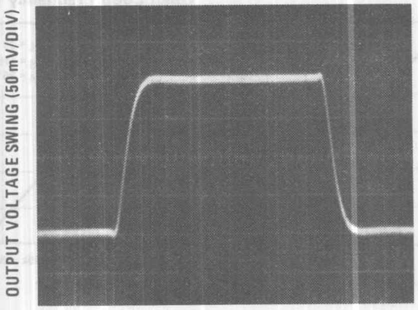
Output Impedance



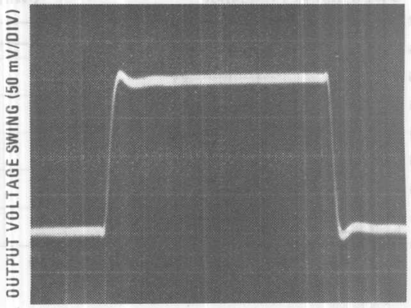
Inverter Settling Time



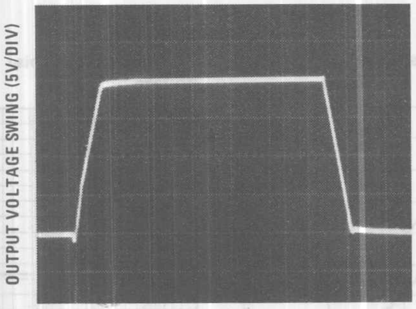
Small Signal Inverting



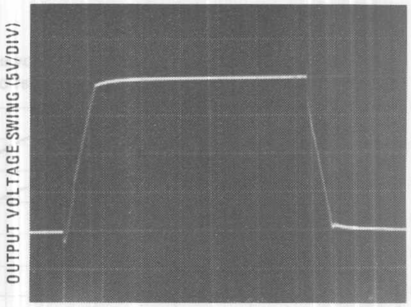
Small Signal Non-Inverting



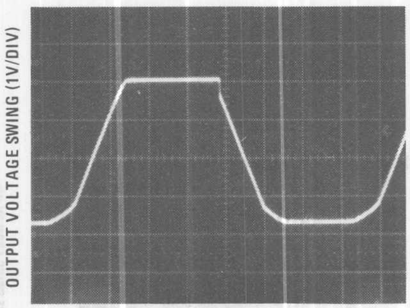
Large Signal Inverting



Large Signal Non-Inverting



Current Limit (R_L = 100Ω)



Application Hints

These devices are op amps with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a

Application Hints (Continued)

high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±4V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The amplifiers will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

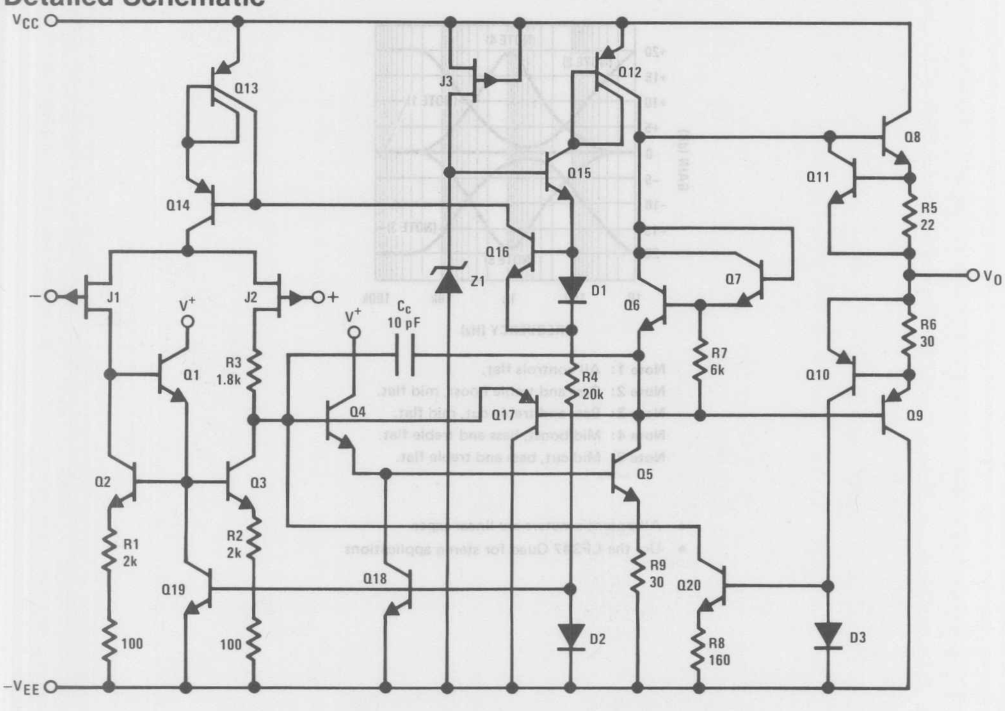
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

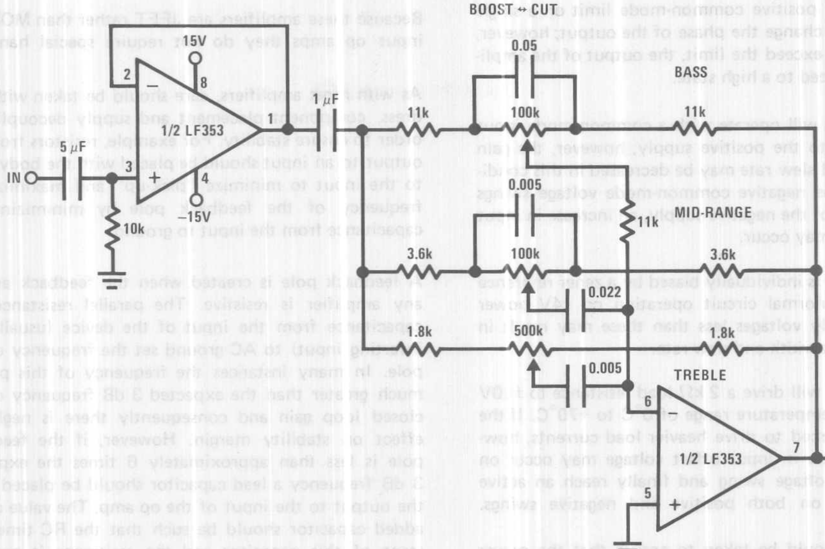
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

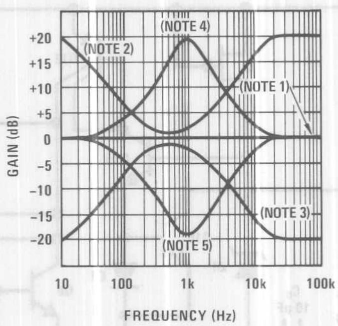
Detailed Schematic



Typical Applications

Three-Band Active Tone Control





Note 1: All controls flat.

Note 2: Bass and treble boost, mid flat.

Note 3: Bass and treble cut, mid flat.

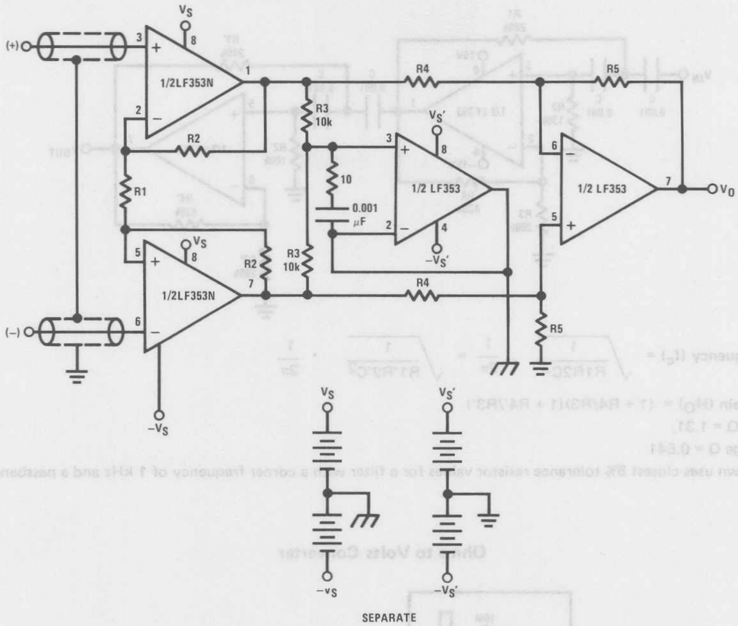
Note 4: Mid boost, bass and treble flat.

Note 5: Mid cut, bass and treble flat.

- All potentiometers are linear taper
- Use the LF347 Quad for stereo applications

Typical Applications (Continued)

Improved CMRR Instrumentation Amplifier



$$A_V = \left(\frac{2R2}{R1} + 1\right) \frac{R5}{R4}$$

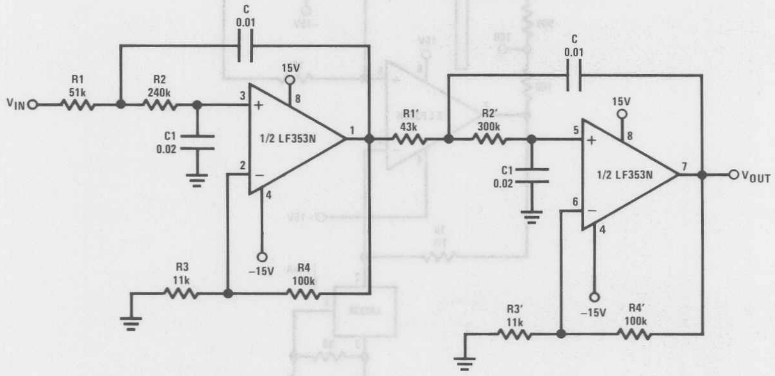
and are separate isolated grounds

Matching of R2's, R4's and R5's control CMRR

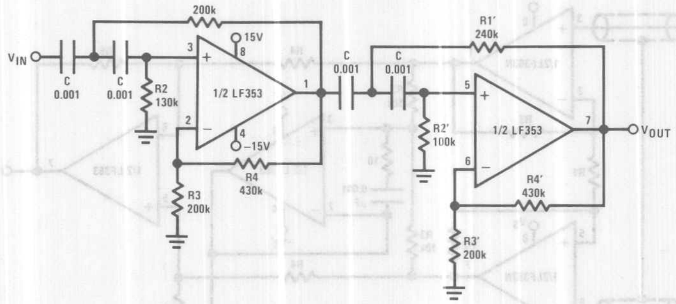
With $A_{V_T} = 1400$, resistor matching = 0.01%: CMRR = 136 dB

- Very high input impedance
- Super high CMRR

Fourth Order Low Pass Butterworth Filter

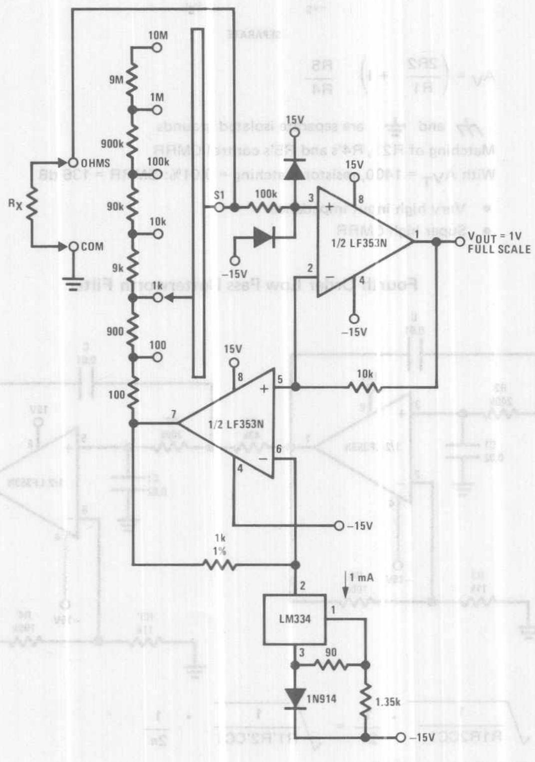


- Corner frequency $(f_c) = \sqrt{\frac{1}{R1R2CC1}} \cdot \frac{1}{2\pi} = \sqrt{\frac{1}{R1'R2'CC1}} \cdot \frac{1}{2\pi}$
- Passband gain $(H_O) = (1 + R4/R3)\ (1 + R4'/R3')$
- First stage Q = 1.31
- Second stage Q = 0.541
- Circuit shown uses nearest 5% tolerance resistor values for a filter with a corner frequency of 100 Hz and a passband gain of 100
- Offset nulling necessary for accurate DC performance



- Corner frequency (f_c) = $\sqrt{\frac{1}{R1R2C^2}} \cdot \frac{1}{2\pi} = \sqrt{\frac{1}{R1'R2'C^2}} \cdot \frac{1}{2\pi}$
- Passband gain (H_O) = (1 + R4/R3)(1 + R4′/R3′)
- First stage Q = 1.31
- Second stage Q = 0.541
- Circuit shown uses closest 5% tolerance resistor values for a filter with a corner frequency of 1 kHz and a passband gain of 10

Ohms to Volts Converter



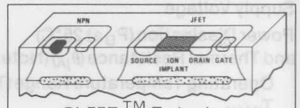
$$V_O = \frac{1V}{R_{LADDER}} \times R_X$$

Where R_{LADDER} is the resistance from switch S1 pole to pin 7 of the LF353.

National Semiconductor

Operational Amplifiers/Buffers

PRELIMINARY



BI-FET™ Technology

LF400C Fast Settling JFET Input Operational Amplifier

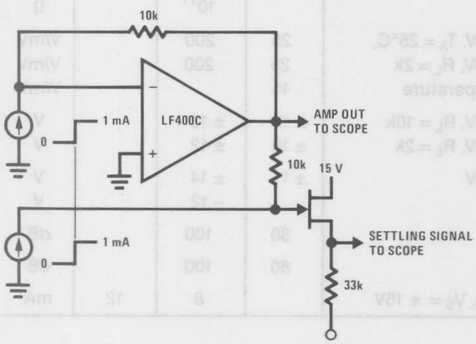
General Description

The LF400C is a fast settling (400 ns to 0.01% for a 10V output step in the test circuit) BI-FET™ operational amplifier. It also features an 18 MHz bandwidth, an inverting slew rate of 57V/μs and adjustable short circuit current limit allowing capacitive and/or 600Ω loads.

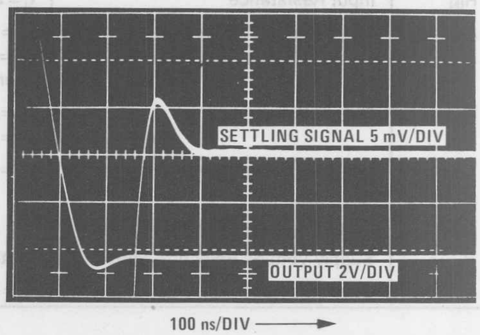
Applications

- Cable drivers
- High speed ramp generators
- DAC output amplifiers
- Fast buffers
- Sample and holds
- Fast integrators
- Piezoelectric transducer signal conditioners

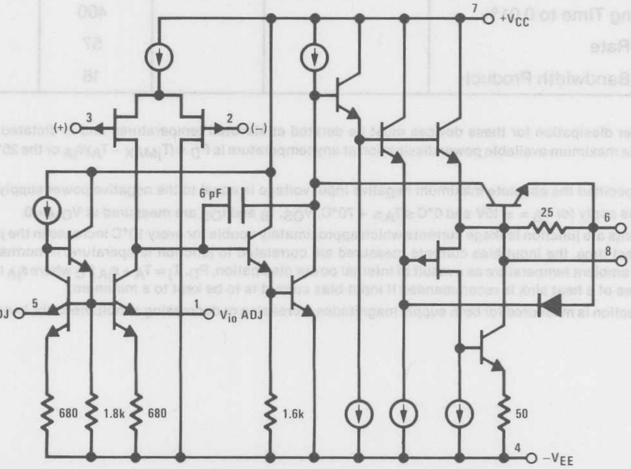
Simplified Settling Time Circuit



Output and Settling Signal



Simplified Schematic



BI-FET™ is a trademark of National Semiconductor Corp.

Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation (P_D at 25°C) and Thermal Resistance (θ_{jA}) (Note 1)	
Operating Temperature Range (T_A)	0°C to +70°C
T_{jMAX}	
(H Package)	115°C
(N Package)	100°C
(H Package) P_D	570 mW
θ_{jA}	150°C/W
(N Package) P_D	500 mW
θ_{jA}	155°C/W
Differential Input Voltage	±40V
Input Voltage Range (Note 2)	±20V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OS}	Input Offset Voltage	$R_S=50\Omega$, $T_A=25°C$ Over Temperature		4	10 13	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S=50\Omega$		20		μV/°C
I_{OS}	Input Offset Current	$T_j=25°C$, (Notes 3 and 4) $T_j \leq T_{HIGH}$		20	100 5	pA nA
I_B	Input Bias Current	$T_j=25°C$, (Notes 3 and 4) $T_j \leq T_{HIGH}$		200	600 25	pA nA
R_{IN}	Input Resistance	$T_j=25°C$		10^{11}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S=\pm15V$, $T_A=25°C$, $V_O=\pm10V$, $R_L=2k$ Over Temperature	25 25 15	200 200		V/mV V/mV V/mV
V_O	Output Voltage Swing	$V_S=\pm15V$, $R_L=10k$ $V_S=\pm15V$, $R_L=2k$	±12 ±10	±13 ±12		V V
V_{CM}	Input Common-Mode Voltage Range	$V_S=\pm15V$	±11	±14 −12		V V
C_{MRR}	Common-Mode Rejection Ratio		80	100		dB
P_{SRR}	Supply Voltage Rejection Ratio	(Note 5)	80	100		dB
I_S	Supply Current	$T_A=25°C$, $V_S=\pm15V$		8	12	mA

AC Electrical Characteristics $T_A=25°C$, $V_S=\pm15V$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_s	Settling Time to 0.01%			400		ns
SR	Slew Rate			57		V/μs
GBW	Gain Bandwidth Product			18		MHz

Note 1: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{jMAX}, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_D=(T_{jMAX}-T_A)/\theta_{jA}$ or the 25°C P_{DMAX}, whichever is less.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

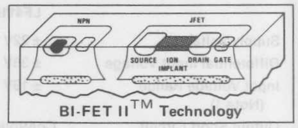
Note 3: These specifications apply for $V_S=\pm15V$ and $0°C \leq T_A \leq +70°C$. V_{OS}, I_B and I_{OS} are measured at $V_{CM}=0$.

Note 4: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j=T_A+\theta_{jA}P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 5: Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

National Semiconductor

Operational Amplifiers/Buffers



BI-FET II™ Technology

LF411A/LF411 Low Offset, Low Drift JFET Input Operational Amplifier

General Description

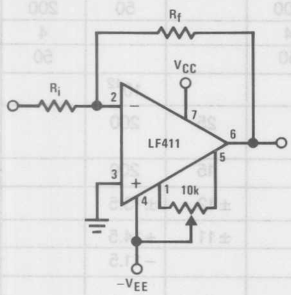
These devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and guaranteed input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF411 is pin compatible with the standard LM741 allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

- Internally trimmed offset voltage 0.5 mV (max)
- Input offset voltage drift 10 μV/°C (max)
- Low input bias current 50 pA
- Low input noise current 0.01 pA/$\sqrt{Hz}$
- Wide gain bandwidth 3 MHz (min)
- High slew rate 10V/μs (min)
- Low supply current 1.8 mA
- High input impedance $10^{12}\Omega$
- Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz–20 kHz $< 0.02\%$
- Low 1/f noise corner 50 Hz
- Fast settling time to 0.01% 2 μs

Typical Connection



Ordering Information

LF411XYZ

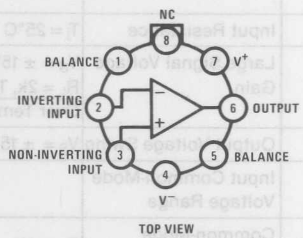
X indicates electrical grade

Y indicates temperature range
"M" for military,
"C" for commercial

Z indicates package type
"H" or "N"

Connection Diagrams

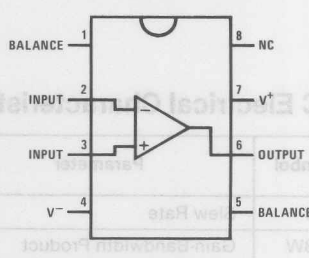
LF411AMH/LF411MH, LF411ACH/LF411CH
Metal Can Package



Note. Pin 4 connected to case.

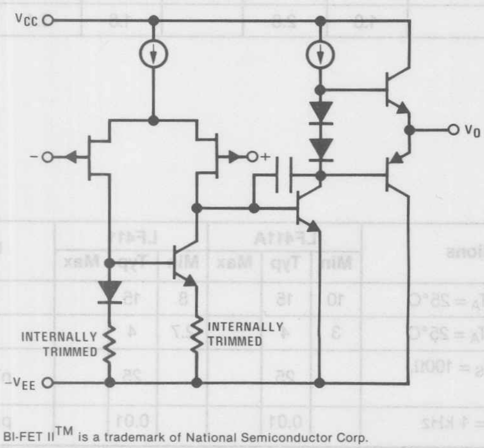
Order Number LF411AMH, LF411MH, LF411ACH or LF411CH
See NS Package H08B

LF411ACN, LF411CN
Dual-In-Line Package



Order Number LF411ACN or LF411CN
See NS Package N08A

Simplified Schematic



	LF411A	LF411
Supply Voltage	±22V	±18V
Differential Input Voltage	±38V	±30V
Input Voltage Range (Note 1)	±19V	±15V
Output Short Circuit Duration	Continuous	Continuous

	LF411A	LF411
Power Dissipation (Note 2)	670 mW	500 mW
T_j max	150°C	115°C
θ_{jA}	150°C/W	160°C/W
Operating Temperature Range	(Note 3)	(Note 3)
Storage Temperature Range	$-65°C \le T_A \le 150°C$	$-65°C \le T_A \le 150°C$
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions		LF411A Min	LF411A Typ	LF411A Max	LF411 Min	LF411 Typ	LF411 Max	Units
V_{OS}	Input Offset Voltage	$R_S = 10\ k\Omega$, $T_A = 25°C$			0.3	0.5		0.8	2.0	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\ k\Omega$ (Note 5)			7	10		7	20 (Note 5)	μV/°C
I_{OS}	Input Offset Current	$V_S = \pm 15V$ Notes 4 and 6	$T_j = 25°C$		25	100		25	100	pA
			$T_j = 70°C$			2			2	nA
			$T_j = 125°C$			25			25	nA
I_B	Input Bias Current	$V_S = \pm 15V$ Notes 4 and 6	$T_j = 25°C$		50	200		50	200	pA
			$T_j = 70°C$			4			4	nA
			$T_j = 125°C$			50			50	nA
R_{IN}	Input Resistance	$T_j = 25°C$			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 2k$, $T_A = 25°C$		50	200		25	200		V/mV
		Over Temperature		25	200		15	200		V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k$		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range			±16	+19.5		±11	+14.5		V
					−16.5			−11.5		V
CMRR	Common-Mode Rejection Ratio	$R_S \le 10k$		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 7)		80	100		70	100		dB
I_S	Supply Current				1.8	2.8		1.8	3.4	mA

AC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	LF411A Min	LF411A Typ	LF411A Max	LF411 Min	LF411 Typ	LF411 Max	Units
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$	10	15		8	15		V/μs
GBW	Gain-Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$	3	4		2.7	4		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, f = 1 kHz		25			25		nV/$\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_A = 25°C$, f = 1 kHz		0.01			0.01		pA/$\sqrt{Hz}$

Notes

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{jA}.

Note 3: These devices are available in both the commercial temperature range $0°C \leq T_A \leq 70°C$ and the military temperature range $-55°C \leq T_A \leq 125°C$. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "H" package only.

Note 4: Unless otherwise specified, the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF411A and for $V_S = \pm 15V$ for the LF411. V_{OS}, I_B, and I_{OS} are measured at $V_{CM} = 0$.

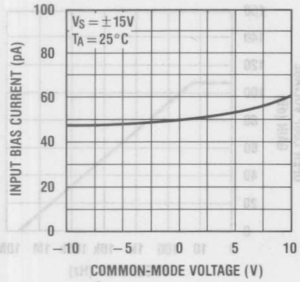
Note 5: The LF411A is 100% tested to this specification. The LF411 is sample tested to insure at least 90% of the units meet this specification.

Note 6: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

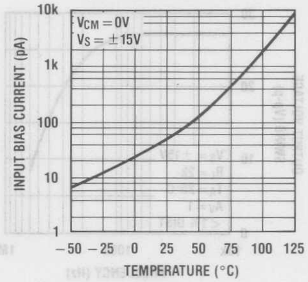
Note 7: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

Typical Performance Characteristics

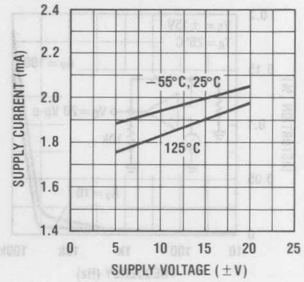
Input Bias Current



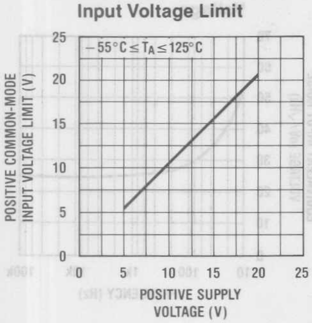
Input Bias Current



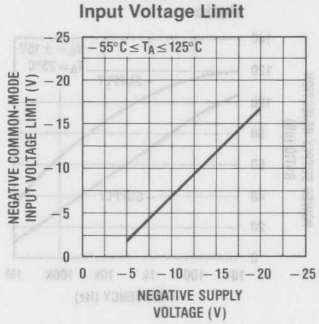
Supply Current



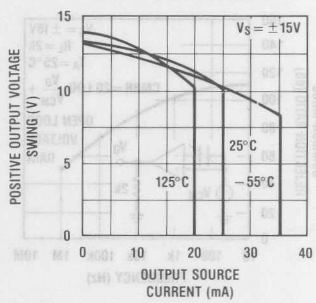
Positive Common-Mode Input Voltage Limit



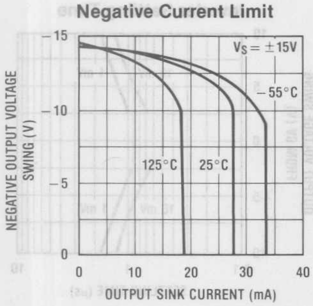
Negative Common-Mode Input Voltage Limit



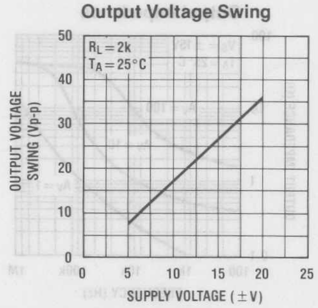
Positive Current Limit



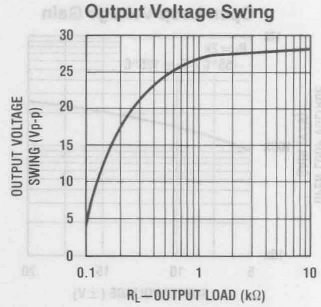
Negative Current Limit



Output Voltage Swing

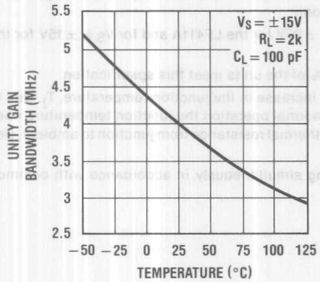


Output Voltage Swing

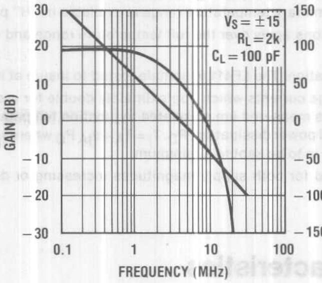


Typical Performance Characteristics (Continued)

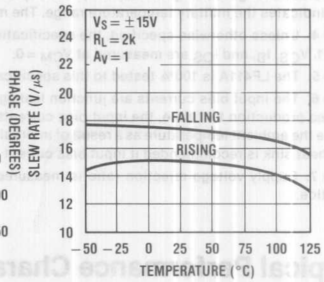
Gain Bandwidth



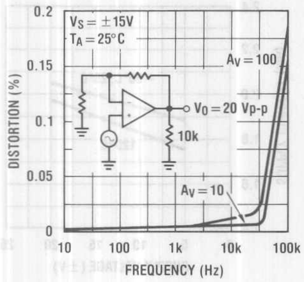
Bode Plot



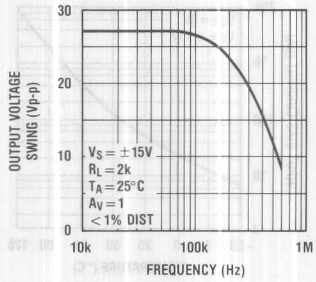
Slew Rate



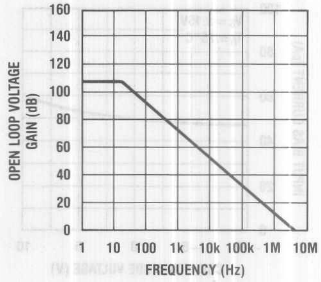
Distortion vs Frequency



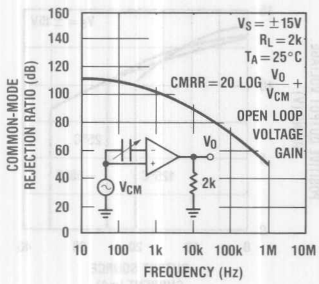
Undistorted Output Voltage Swing



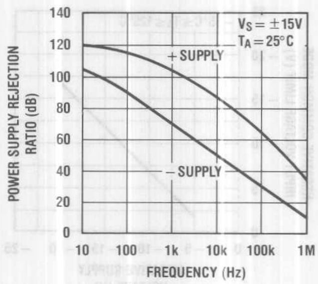
Open Loop Frequency Response



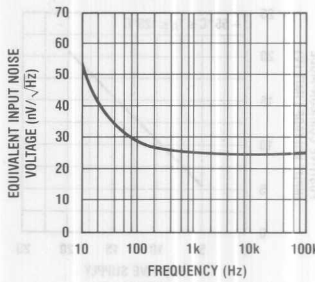
Common-Mode Rejection Ratio



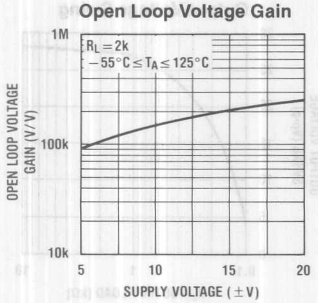
Power Supply Rejection Ratio



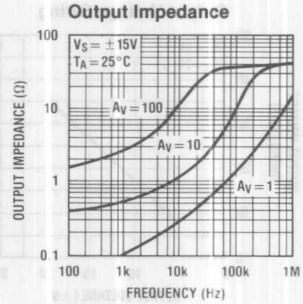
Equivalent Input Noise Voltage



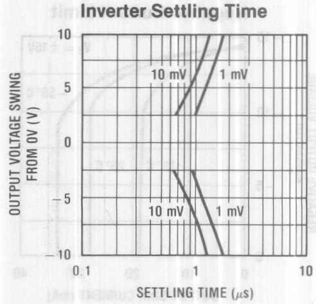
Open Loop Voltage Gain



Output Impedance

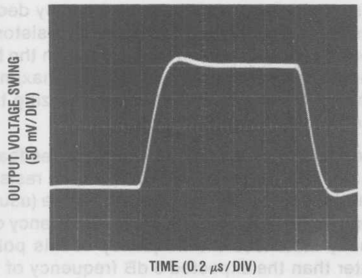


Inverter Settling Time

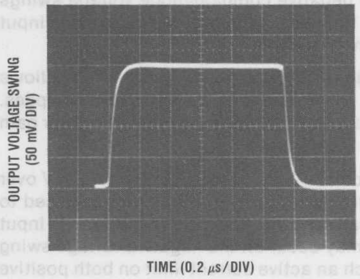


Pulse Response $R_L = 2\ k\Omega$, $C_L = 10\ pF$

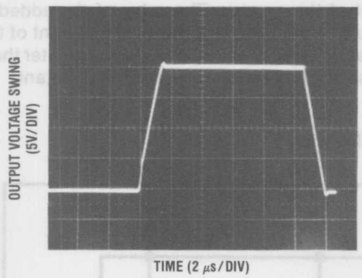
Small Signal Inverting



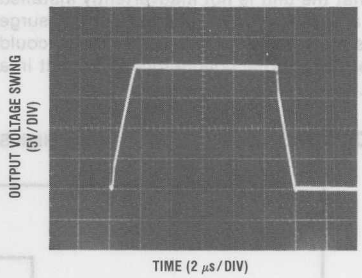
Small Signal Non-Inverting



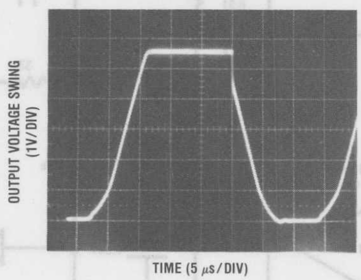
Large Signal Inverting



Large Signal Non-Inverting



Current Limit ($R_L = 100\Omega$)



Application Hints

The LF411 series of internally trimmed JFET input op amps (BI-FET II™) provide very low input offset voltage and guaranteed input offset voltage drift. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier may be forced to a high state.

bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The LF411 is biased by a zener reference which allows normal circuit operation on ±4.5V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF411 will drive a 2 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

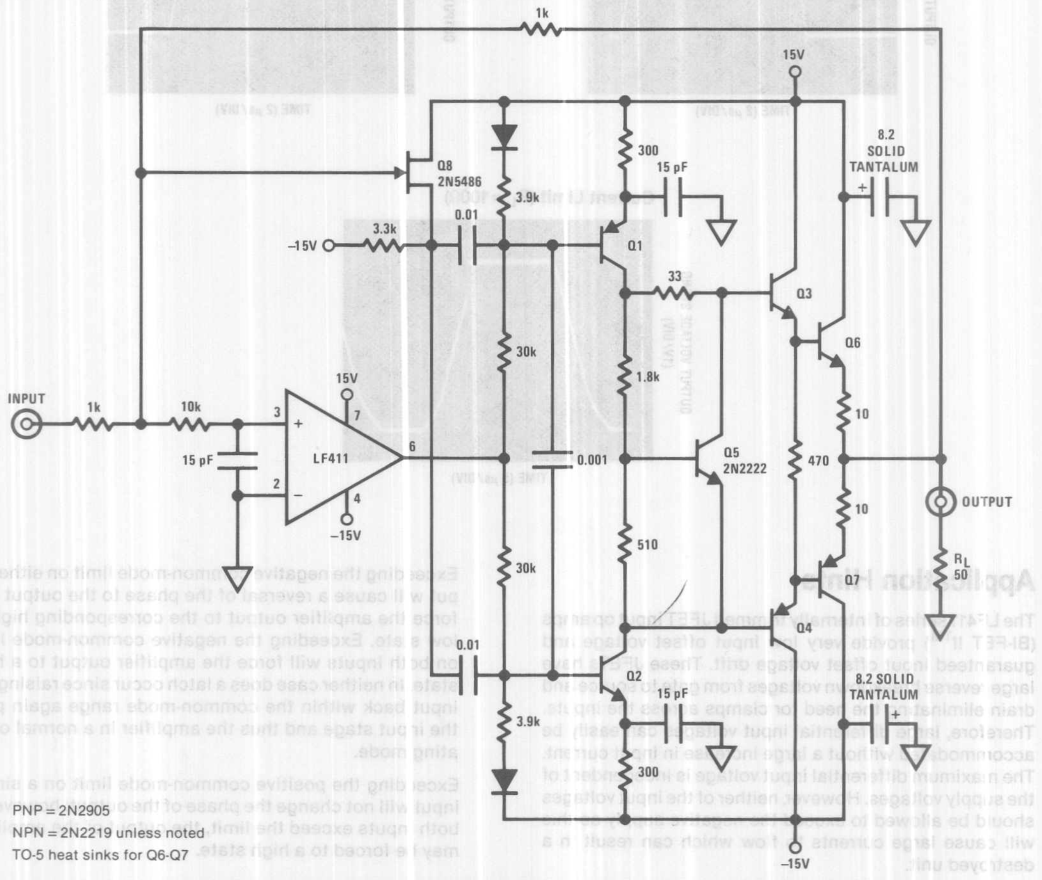
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

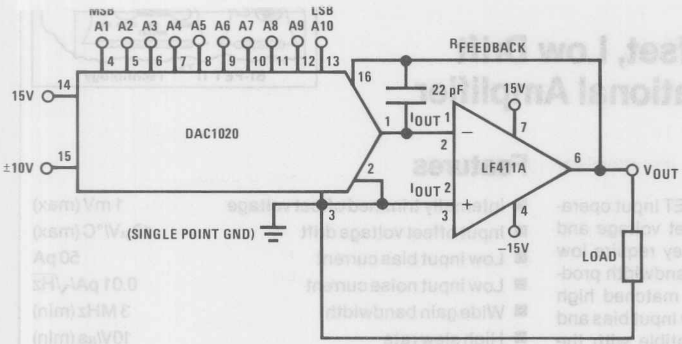
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency, a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Applications

Ultra High Speed Current Booster



PNP = 2N2905
NPN = 2N2219 unless noted
TO-5 heat sinks for Q6-Q7



$$V_{OUT} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \ldots \frac{A10}{1024}\right)$$

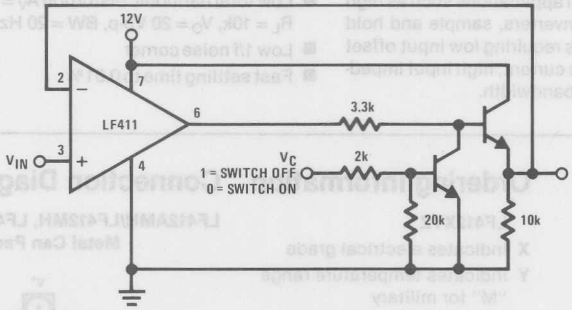
$$-10V \le V_{REF} \le 10V$$

$$0 \le V_{OUT} \le -\frac{1023}{1024} V_{REF}$$

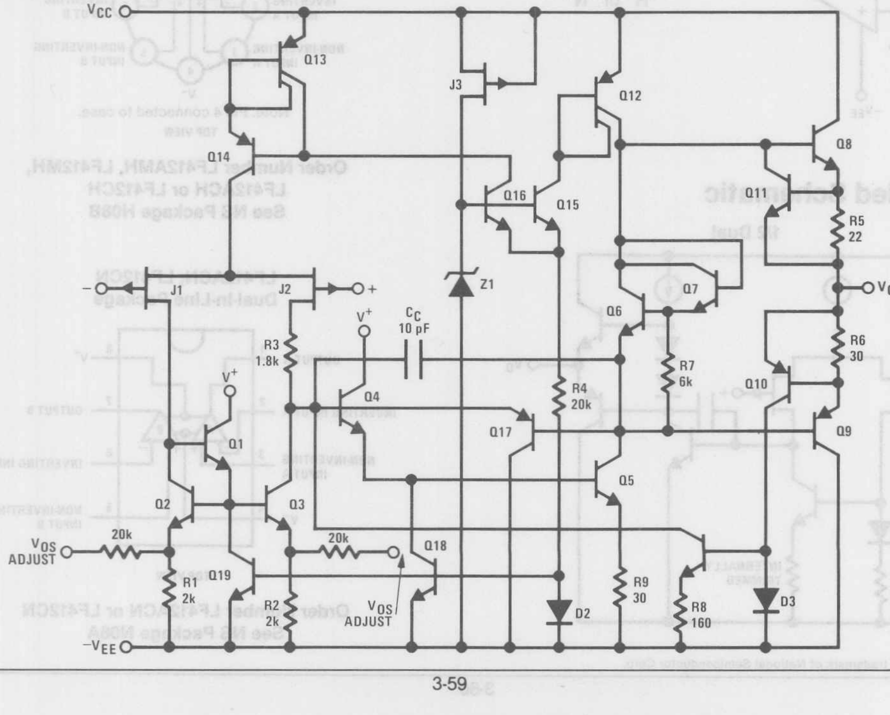
where $A_N = 1$ if the A_N digital input is high

$A_N = 0$ if the A_N digital input is low

Single Supply Analog Switch with Buffered Output

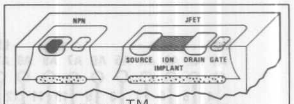


Detailed Schematic



National Semiconductor

Operational Amplifiers/Buffers



BI-FET II™ Technology

LF412A/LF412 Low Offset, Low Drift Dual JFET Input Operational Amplifier

General Description

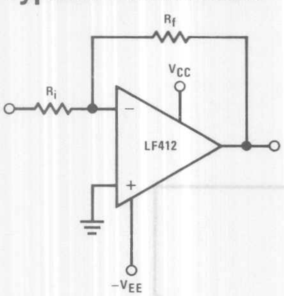
These devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and guaranteed input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. LF412 dual is pin compatible with the LM1558, allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

- Internally trimmed offset voltage — 1 mV (max)
- Input offset voltage drift — 10 μV/°C (max)
- Low input bias current — 50 pA
- Low input noise current — 0.01 pA/$\sqrt{\text{Hz}}$
- Wide gain bandwidth — 3 MHz (min)
- High slew rate — 10V/μs (min)
- Low supply current — 1.8 mA/Amplifier
- High input impedance — $10^{12}\Omega$
- Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz–20 kHz — < 0.02%
- Low 1/f noise corner — 50 Hz
- Fast settling time to 0.01% — 2 μs

Typical Connection



Ordering Information

LF412XYZ

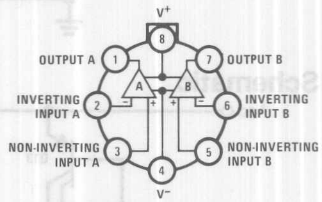
X indicates electrical grade

Y indicates temperature range
"M" for military
"C" for commercial

Z indicates package type
"H" or "N"

Connection Diagrams

LF412AMH/LF412MH, LF412ACH/LF412CH
Metal Can Package

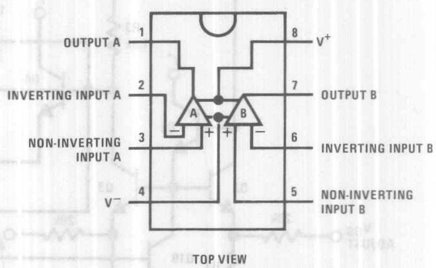


Note. Pin 4 connected to case.

TOP VIEW

Order Number LF412AMH, LF412MH, LF412ACH or LF412CH
See NS Package H08B

LF412ACN, LF412CN
Dual-In-Line Package

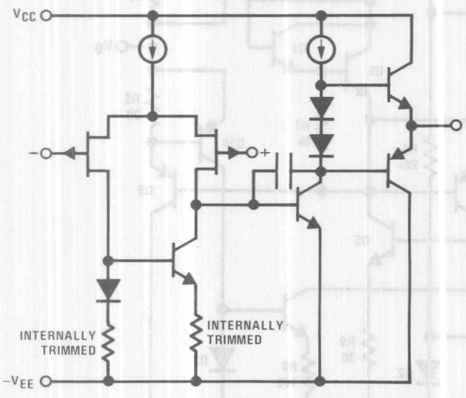


TOP VIEW

Order Number LF412ACN or LF412CN
See NS Package N08A

Simplified Schematic

1/2 Dual



Absolute Maximum Ratings

	LF412A	LF412
Supply Voltage	± 22V	± 18V
Differential Input Voltage	± 38V	± 30V
Input Voltage Range (Note 1)	± 19V	± 15V
Output Short Circuit Duration (Note 2)	Continuous	Continuous

	H Package	N Package
Power Dissipation (Note 3)	670 mW	500 mW
T_j max	150°C	115°C
θ_{jA}	150°C/W	160°C/W
Operating Temperature Range	(Note 4)	(Note 4)
Storage Temperature Range	$-65°C \le T_A \le 150°C$	$-65°C \le T_A \le 150°C$
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

DC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions		LF412A Min	LF412A Typ	LF412A Max	LF412 Min	LF412 Typ	LF412 Max	Units
V_{OS}	Input Offset Voltage	$R_S = 10\ k\Omega$, $T_A = 25°C$			0.5	1.0		1.0	3.0	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\ k\Omega$ (Note 6)			7	10		7	20 (Note 6)	μV/°C
I_{OS}	Input Offset Current	$V_S = \pm 15V$ (Notes 5 and 7)	$T_j = 25°C$		25	100		25	100	pA
			$T_j = 70°C$			2			2	nA
			$T_j = 125°C$			25			25	nA
I_B	Input Bias Current	$V_S = \pm 15V$ (Notes 5 and 7)	$T_j = 25°C$		50	200		50	200	pA
			$T_j = 70°C$			4			4	nA
			$T_j = 125°C$			50			50	nA
R_{IN}	Input Resistance	$T_j = 25°C$			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 2k$, $T_A = 25°C$		50	200		25	200		V/mV
		Over Temperature		25	200		15	200		V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k$		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range			± 16	+19.5		±11	+14.5		V
					−16.5			−11.5		V
CMRR	Common-Mode Rejection Ratio	$R_S \le 10k$		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 8)		80	100		70	100		dB
I_S	Supply Current				3.6	5.6		3.6	6.8	mA

AC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	LF412A Min	LF412A Typ	LF412A Max	LF412 Min	LF412 Typ	LF412 Max	Units
	Amplifier to Amplifier Coupling	$T_A = 25°C$, f = 1 Hz-20 kHz (Input Referred)		−120			−120		dB
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$	10	15		8	15		V/μs
GBW	Gain-Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$	3	4		2.7	4		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, f = 1 kHz		25			25		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_A = 25°C$, f = 1 kHz		0.01			0.01		$pA/\sqrt{Hz}$

Note 2: Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 3: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{jA}.

Note 4: These devices are available in both the commercial temperature range $0°C \leq T_A \leq 70°C$ and the military temperature range $-55°C \leq T_A \leq 125°C$. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "H" package only.

Note 5: Unless otherwise specified, the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF412A and for $V_S = \pm 15V$ for the LF412. V_{OS}, I_B, and I_{OS} are measured at $V_{CM} = 0$.

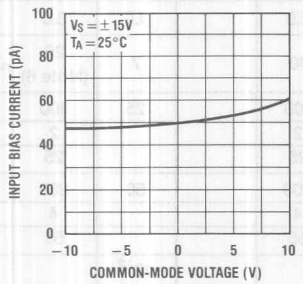
Note 6: The LF412A is 100% tested to this specification. The LF412 is sample tested on a per amplifier basis to insure at least 90% of the amplifiers meet this specification.

Note 7: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

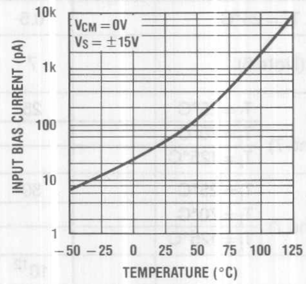
Note 8: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

Typical Performance Characteristics

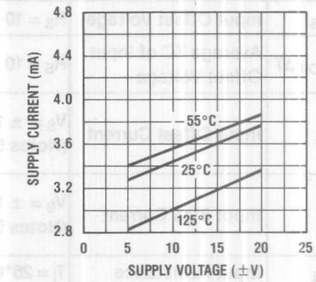
Input Bias Current



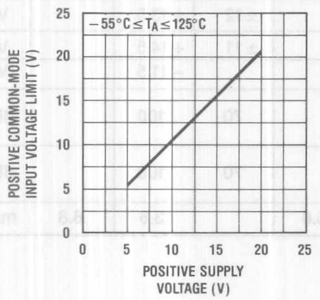
Input Bias Current



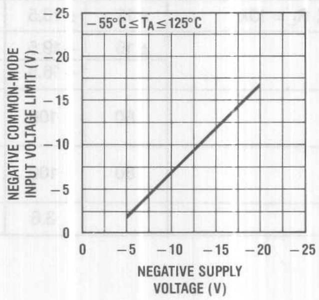
Supply Current



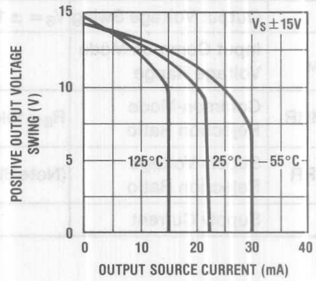
Positive Common-Mode Input Voltage Limit



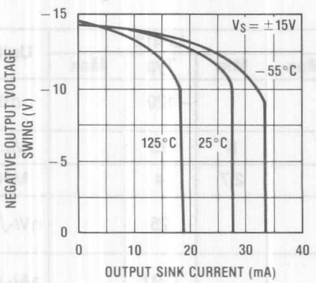
Negative Common-Mode Input Voltage Limit



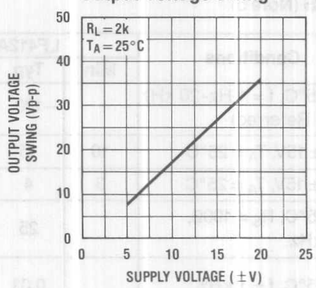
Positive Current Limit



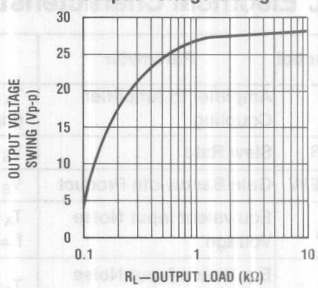
Negative Current Limit



Output Voltage Swing

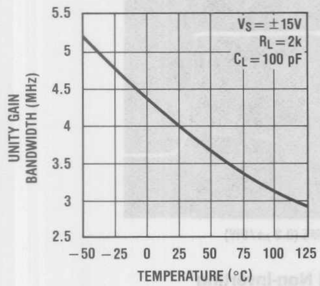


Output Voltage Swing

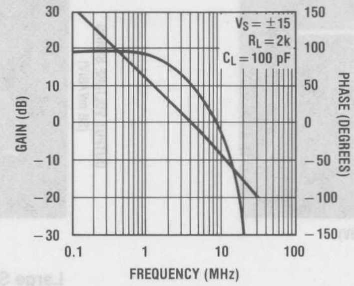


Typical Performance Characteristics (Continued)

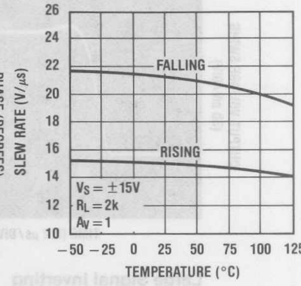
Gain Bandwidth



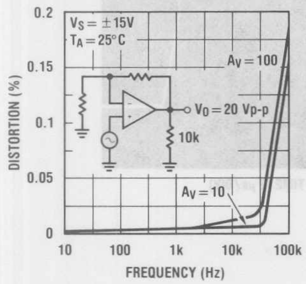
Bode Plot



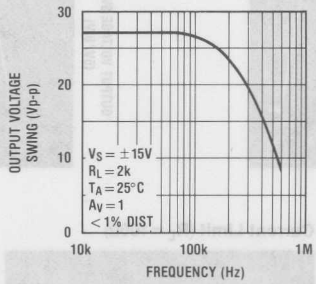
Slew Rate



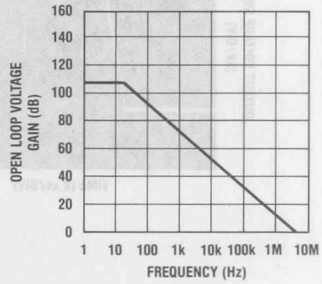
Distortion vs Frequency



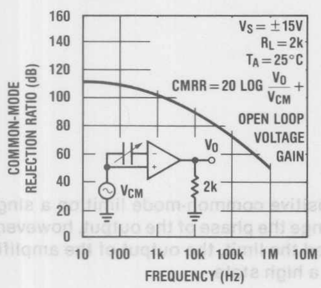
Undistorted Output Voltage Swing



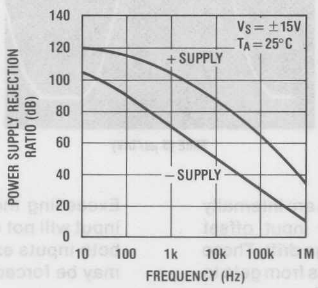
Open Loop Frequency Response



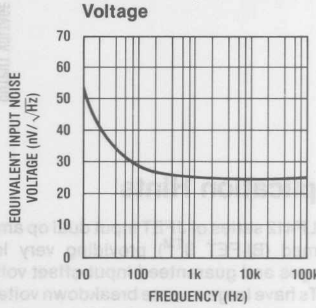
Common-Mode Rejection Ratio



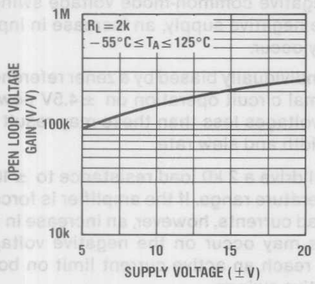
Power Supply Rejection Ratio



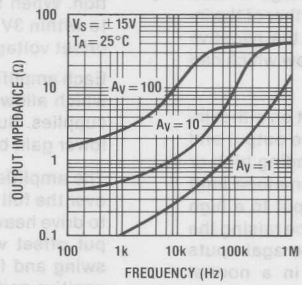
Equivalent Input Noise Voltage



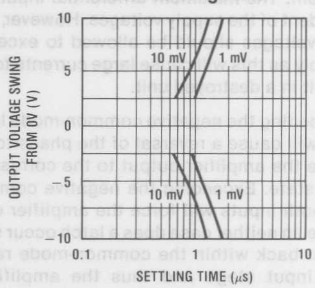
Open Loop Voltage Gain



Output Impedance

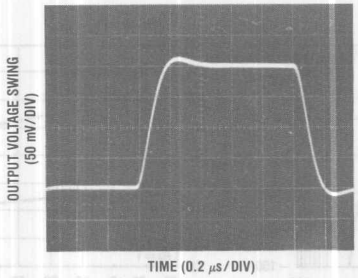


Inverter Settling Time

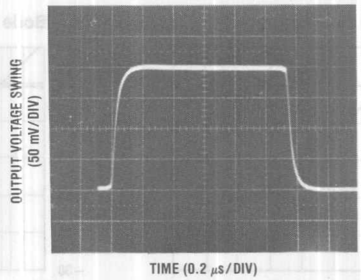


Pulse Response $R_L = 2\ k\Omega$, $C_L = 10\ pF$

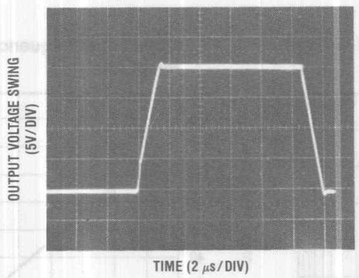
Small Signal Inverting



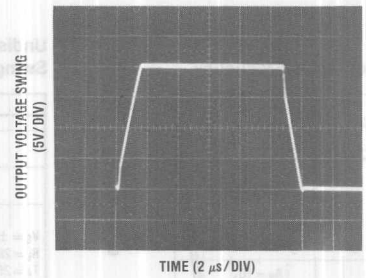
Small Signal Non-Inverting



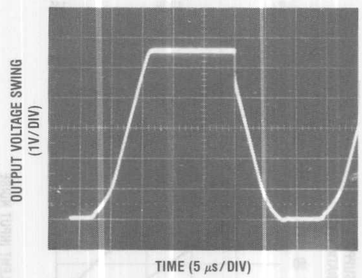
Large Signal Inverting



Large Signal Non-Inverting



Current Limit ($R_L = 100\Omega$)



Application Hints

The LF412 series of JFET input dual op amps are internally trimmed (BI-FET II™) providing very low input offset voltages and guaranteed input offset voltage drift. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output, however, if both inputs exceed the limit, the output of the amplifier may be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±4.5V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The amplifiers will drive a 2 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Application Hints (Continued)

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

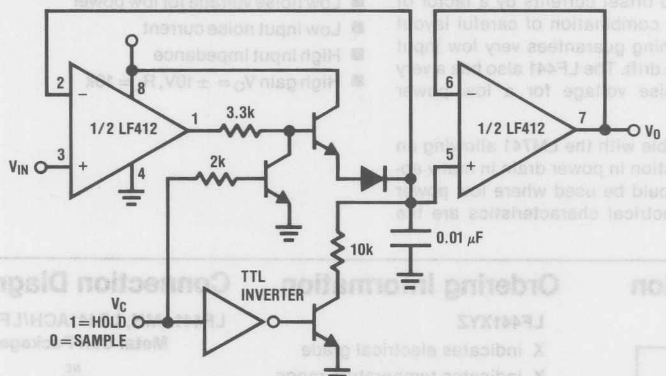
Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

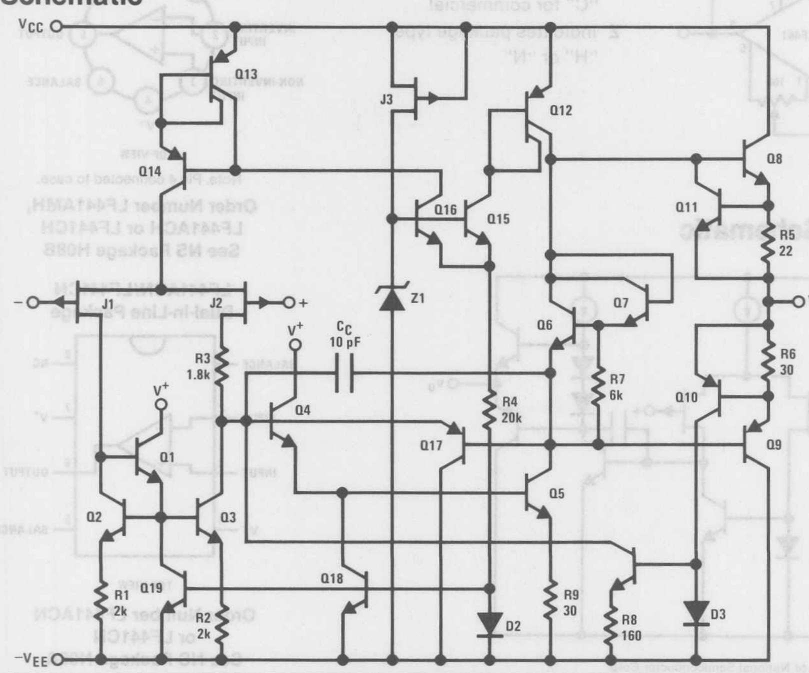
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Application

Single Supply Sample and Hold



Detailed Schematic



LF441A/LF441 Low Power JFET Input Operational Amplifier

BI-FET II™ Technology

General Description

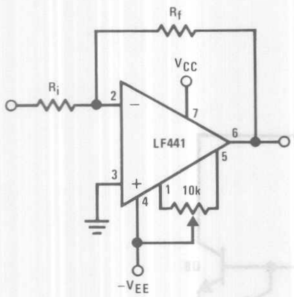
The LF441 low power operational amplifier provides many of the same AC characteristics as the industry standard LM741 while greatly improving the DC characteristics of the LM741. The amplifier has the same bandwidth, slew rate, and gain (10 kΩ load) as the LM741 and only draws one tenth the supply current of the LM741. In addition the well matched high voltage JFET input devices of the LF441 reduce the input bias and offset currents by a factor of 10,000 over the LM741. A combination of careful layout design and internal trimming guarantees very low input offset voltage and voltage drift. The LF441 also has a very low equivalent input noise voltage for a low power amplifier.

The LF441 is pin compatible with the LM741 allowing an immediate 10 times reduction in power drain in many applications. The LF441 should be used where low power dissipation and good electrical characteristics are the major considerations.

Features

- 1/10 supply current of a LM741 — 200 μA (max)
- Low input bias current — 50 pA (max)
- Low input offset voltage — 0.5 mV (max)
- Low input offset voltage drift — 10 μV/°C (max)
- High gain bandwidth — 1 MHz
- High slew rate — 1V/μs
- Low noise voltage for low power — 35 nV/$\sqrt{Hz}$
- Low input noise current — 0.01 pA/$\sqrt{Hz}$
- High input impedance — $10^{12}\Omega$
- High gain $V_O = \pm 10V$, $R_L = 10k$ — 50k (min)

Typical Connection



Ordering Information

LF441XYZ

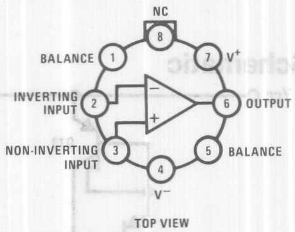
X indicates electrical grade

Y indicates temperature range
"M" for military,
"C" for commercial

Z indicates package type
"H" or "N"

Connection Diagrams

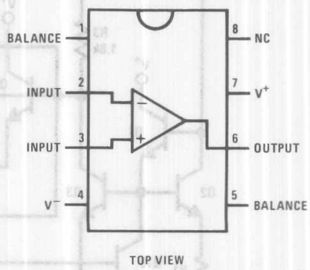
LF441AMH, LF441ACH/LF441CH
Metal Can Package



Note. Pin 4 connected to case.

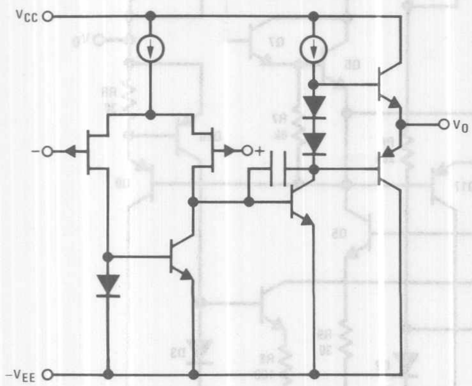
Order Number LF441AMH, LF441ACH or LF441CH
See NS Package H08B

LF441ACN/LF441CN
Dual-In-Line Package



Order Number LF441ACN or LF441CN
See NS Package N08A

Simplified Schematic



Supply Voltage	± 22V	± 18V	Power Dissipation (Note 2)	670 mW	500 mW
Differential Input Voltage	± 38V	± 30V	T_j max	150°C	115°C
Input Voltage Range (Note 1)	± 19V	± 15V	θ_{jA}	150°C/W	160°C/W
Output Short Circuit Duration	Continuous	Continuous	Operating Temperature Range	(Note 3)	(Note 3)
			Storage Temperature Range	$-65°C \le T_A \le 150°C$	$-65°C \le T_A \le 150°C$
			Lead Temperature (Soldering, 10 seconds)	300°C	300°C

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions		LF441A			LF441			Units
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 10\ k\Omega$, $T_A = 25°C$			0.3	0.5		1	5	mV
		Over Temperature							7.5	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\ k\Omega$ (Note 5)			7	10		10	20	μV/°C
I_{OS}	Input Offset Current	$V_S = \pm 15V$ (Notes 4 and 6)	$T_j = 25°C$		5	25		5	50	pA
			$T_j = 70°C$			1.5			1.5	nA
			$T_j = 125°C$			10				nA
I_B	Input Bias Current	$V_S = \pm 15V$ (Notes 4 and 6)	$T_j = 25°C$		10	50		10	100	pA
			$T_j = 70°C$			3			3	nA
			$T_j = 125°C$			20				nA
R_{IN}	Input Resistance	$T_j = 25°C$			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 10\ k\Omega$, $T_A = 25°C$		50	100		25	100		V/mV
		Over Temperature		25			15			V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$		± 12	± 13		± 12	± 13		V
V_{CM}	Input Common-Mode Voltage Range			± 16	+ 18		± 11	+ 14		V
					− 17			− 12		V
CMRR	Common-Mode Rejection Ratio	$R_S \le 10\ k\Omega$		80	100		70	95		dB
PSRR	Supply Voltage Rejection Ratio	(Note 7)		80	100		70	90		dB
I_S	Supply Current				150	200		150	250	μA

AC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	LF441A Min	LF441A Typ	LF441A Max	LF441 Min	LF441 Typ	LF441 Max	Units
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$	0.8	1		0.6	1		V/μs
GBW	Gain-Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$	0.8	1		0.6	1		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, f = 1 kHz		35			35		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_A = 25°C$, f = 1 kHz		0.01			0.01		$pA/\sqrt{Hz}$

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{jA}.

Note 3: The LF441A and LF441B are available in both the commercial temperature range $0°C \le T_A \le 70°C$ and the military temperature range $-55°C \le T_A \le 125°C$. The LF441 is available in the commercial temperature range only. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "H" package only.

Note 4: Unless otherwise specified the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF441A/LF441B and for $V_S = \pm 15V$ for the LF441. V_{OS}, I_B, and I_{OS} are measured at $V_{CM} = 0$.

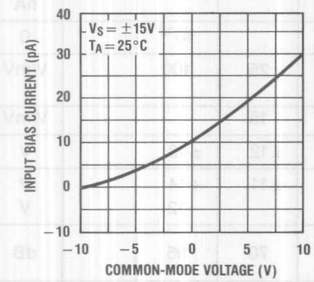
Note 5: The LF441A is 100% tested to this specification.

Note 6: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

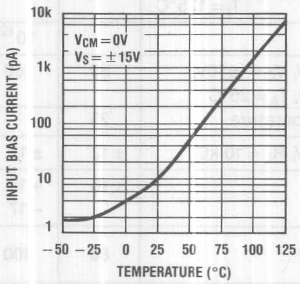
Note 7: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

Typical Performance Characteristics

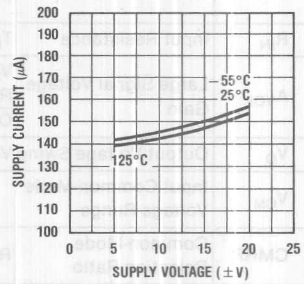
Input Bias Current



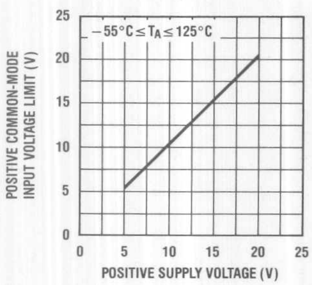
Input Bias Current



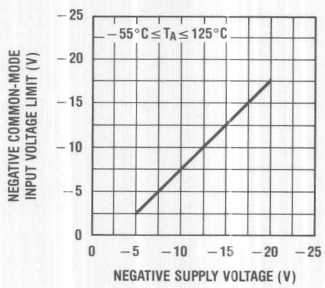
Supply Current



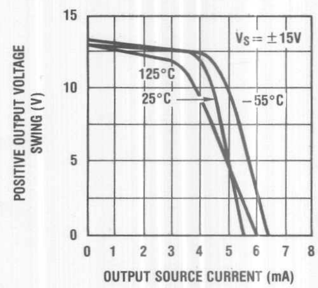
Positive Common-Mode Input Voltage Limit



Negative Common-Mode Input Voltage Limit

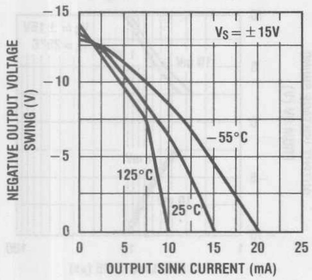


Positive Current Limit

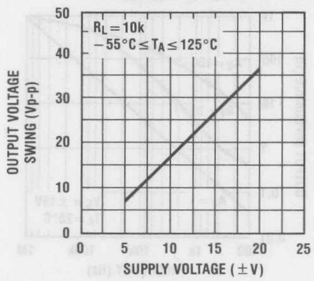


Typical Performance Characteristics (Continued)

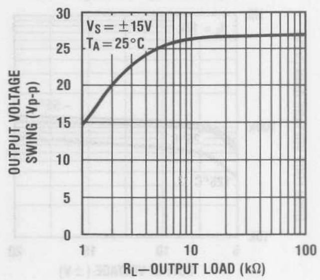
Negative Current Limit



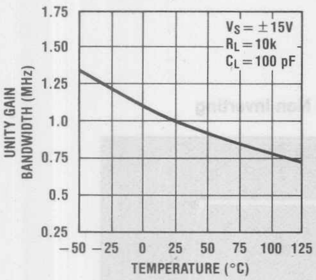
Output Voltage Swing



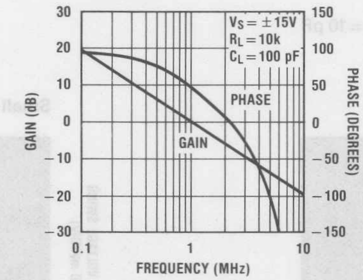
Output Voltage Swing



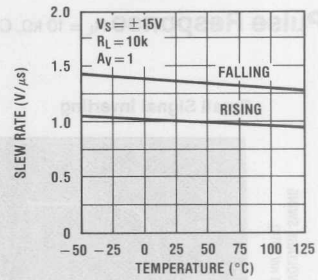
Gain Bandwidth



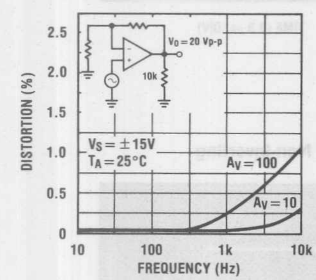
Bode Plot



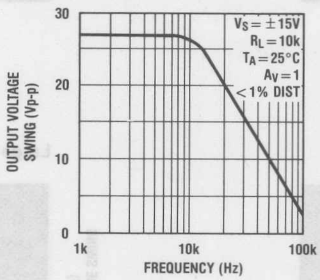
Slew Rate



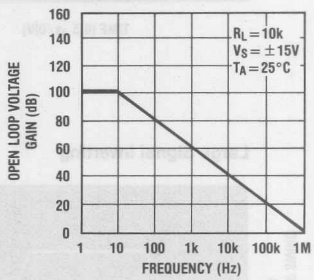
Distortion vs Frequency



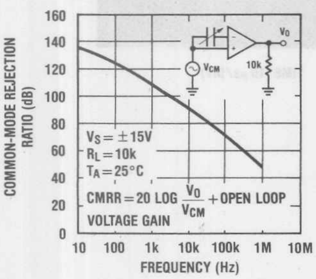
Undistorted Output Voltage Swing



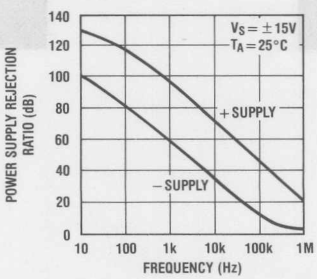
Open Loop Frequency Response



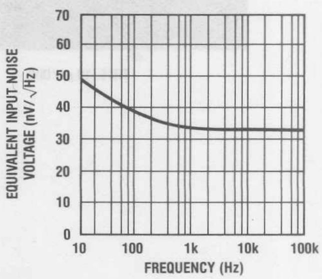
Common-Mode Rejection Ratio



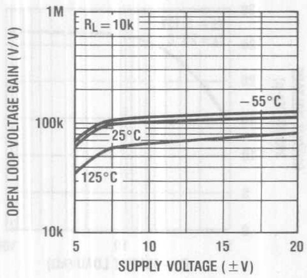
Power Supply Rejection Ratio



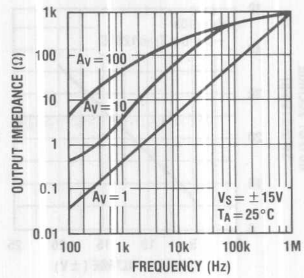
Equivalent Input Noise Voltage



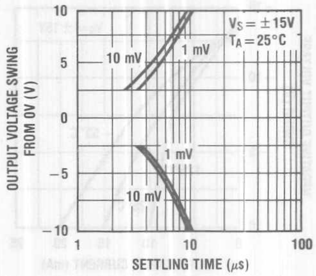
Open Loop Voltage Gain



Output Impedance

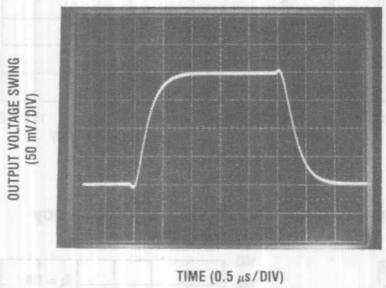


Inverter Settling Time

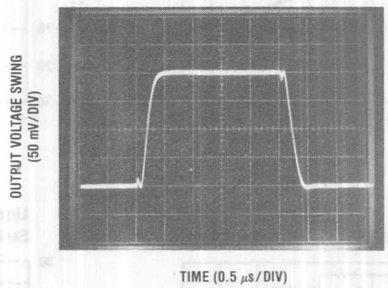


Pulse Response $R_L = 10\ k\Omega$, $C_L = 10\ pF$

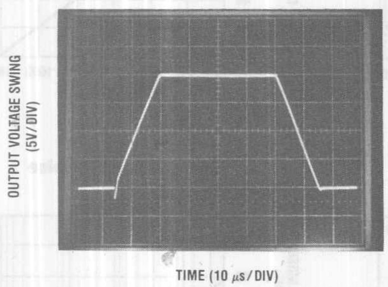
Small Signal Inverting



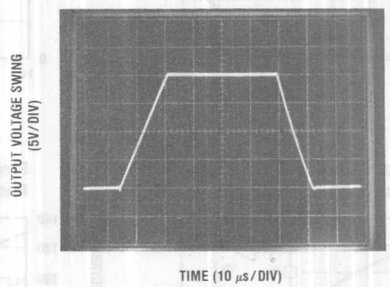
Small Signal Non-Inverting



Large Signal Inverting



Large Signal Non-Inverting



Application Hints

This device is a low power op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The amplifier is biased to allow normal circuit operation with power supplies of ±3V. Supply voltages less than these may degrade the common-mode rejection and restrict the output voltage swing.

The amplifier will drive a 10 kΩ load resistance to ±10V over the full temperature range.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

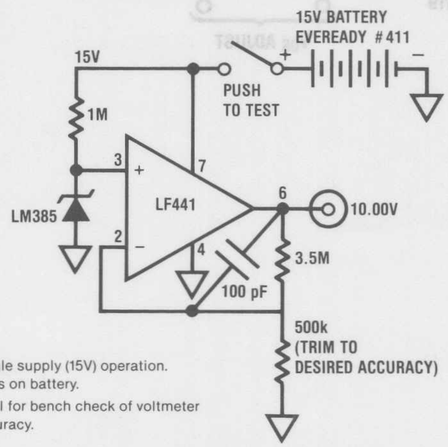
Because this amplifier is a JFET rather than MOSFET input op amp it does not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input to AC ground set the frequency of this pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Application

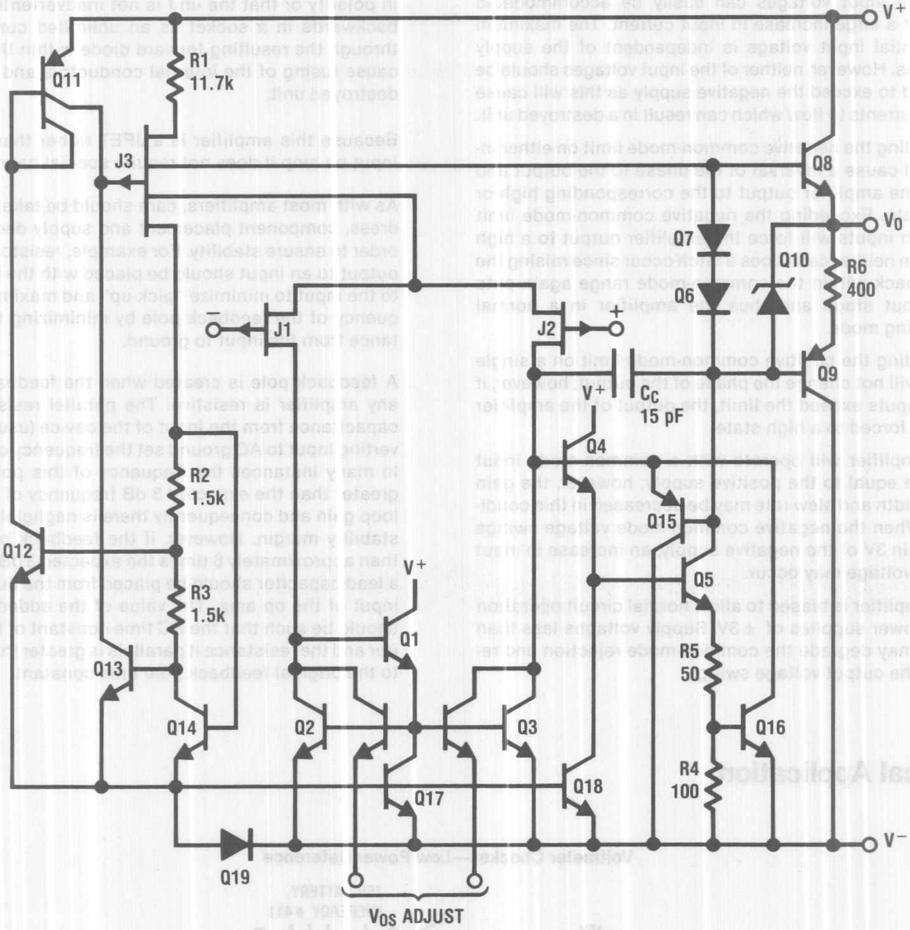
Voltmeter Checker—Low Power Reference



Single supply (15V) operation.
Runs on battery.

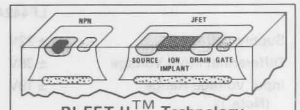
Ideal for bench check of voltmeter accuracy.

Detailed Schematic



National Semiconductor

Operational Amplifiers/Buffers



BI-FET II™ Technology

LF442A/LF442 Dual Low Power JFET Input Operational Amplifier

General Description

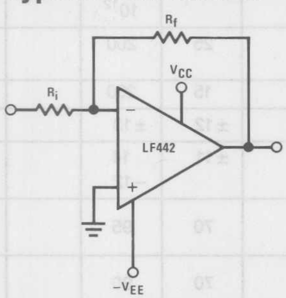
The LF442 dual low power operational amplifiers provide many of the same AC characteristics as the industry standard LM1458 while greatly improving the DC characteristics of the LM1458. The amplifiers have the same bandwidth, slew rate, and gain (10 kΩ load) as the LM1458 and only draw one tenth the supply current of the LM1458. In addition the well matched high voltage JFET input devices of the LF442 reduce the input bias and offset currents by a factor of 10,000 over the LM1458. A combination of careful layout design and internal trimming guarantees very low input offset voltage and voltage drift. The LF442 also has a very low equivalent input noise voltage for a low power amplifier.

The LF442 is pin compatible with the LM1458 allowing an immediate 10 times reduction in power drain in many applications. The LF442 should be used where low power dissipation and good electrical characteristics are the major considerations.

Features

- 1/10 supply current of a LM1458 — 400 μA (max)
- Low input bias current — 50 pA (max)
- Low input offset voltage — 1 mV (max)
- Low input offset voltage drift — 10 μV/°C (max)
- High gain bandwidth — 1 MHz
- High slew rate — 1 V/μs
- Low noise voltage for low power — 35 nV/$\sqrt{Hz}$
- Low input noise current — 0.01 pA/$\sqrt{Hz}$
- High input impedance — $10^{12}\,\Omega$
- High gain $V_O = \pm 10V$, $R_L = 10k$ — 50k (min)

Typical Connection



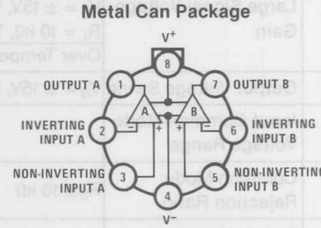
Ordering Information

LF442XYZ

- X indicates electrical grade
- Y indicates temperature range "M" for military, "C" for commercial
- Z indicates package type "H" or "N"

Connection Diagrams

LF442AMH, LF442ACH, LF442CH
Metal Can Package

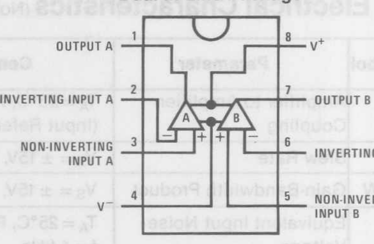


TOP VIEW

Note. Pin 4 connected to case.

Order Number LF442AMH, LF442ACH or LF442CH
See NS Package H08B

LF442ACN, LF442CN
Dual-In-Line Package

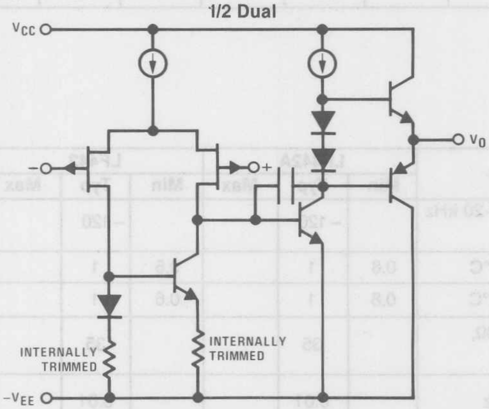


TOP VIEW

Order Number LF442ACN or LF442CN
See NS Package N08A

Simplified Schematic

1/2 Dual



BI-FET II™ is a trademark of National Semiconductor Corp.

Input Voltage Range (Note 1)	±19V	±15V
Output Short Circuit Duration (Note 2)	Continuous	Continuous
T_j max	150°C	115°C
θ_{jA}	150°C/W	160°C/W
Operating Temperature Range	(Note 4)	(Note 4)
Storage Temperature Range	$-65°C \le T_A \le 150°C$	$-65°C \le T_A \le 150°C$
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

DC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions		LF442A Min	LF442A Typ	LF442A Max	LF442 Min	LF442 Typ	LF442 Max	Units
V_{OS}	Input Offset Voltage	$R_S = 10\ k\Omega$, $T_A = 25°C$			0.5	1.0		1.0	5.0	mV
		Over Temperature							7.5	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\ k\Omega$			7	10		7		μV/°C
I_{OS}	Input Offset Current	$V_S = \pm 15V$ (Notes 5 and 6)	$T_j = 25°C$		5	25		5	50	pA
			$T_j = 70°C$			1.5			1.5	nA
			$T_j = 125°C$			10				nA
I_B	Input Bias Current	$V_S = \pm 15V$ (Notes 5 and 6)	$T_j = 25°C$		10	50		10	100	pA
			$T_j = 70°C$			3			3	nA
			$T_j = 125°C$			20				nA
R_{IN}	Input Resistance	$T_j = 25°C$			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 10\ k\Omega$, $T_A = 25°C$		50	200		25	200		V/mV
		Over Temperature		25	200		15	200		V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$		±12	±13		±12	±13		V
V_{CM}	Input Common-Mode Voltage Range			±16	+18		±11	14		V
					−17			−12		V
CMRR	Common-Mode Rejection Ratio	$R_S \le 10\ k\Omega$		80	100		70	95		dB
PSRR	Supply Voltage Rejection Ratio	(Note 7)		80	100		70	90		dB
I_S	Supply Current				300	400		400	500	μA

AC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	LF442A Min	LF442A Typ	LF442A Max	LF442 Min	LF442 Typ	LF442 Max	Units
	Amplifier to Amplifier Coupling	$T_A = 25°C$, f = 1 Hz–20 kHz (Input Referred)		−120			−120		dB
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$	0.8	1		0.6	1		V/μs
GBW	Gain-Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$	0.8	1		0.6	1		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, f = 1 kHz		35			35		nV/$\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_A = 25°C$, f = 1 kHz		0.01			0.01		pA/$\sqrt{Hz}$

Notes

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 3: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{jA}.

Note 4: These devices are available in both the commercial temperature range $0°C \leq T_A \leq 70°C$ and the military temperature range $-55°C \leq T_A \leq 125°C$. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "H" package only.

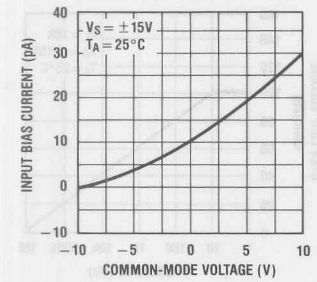
Note 5: Unless otherwise specified, the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF442A and for $V_S = \pm 15V$ for the LF442. V_{OS}, I_B, and I_{OS} are measured at $V_{CM} = 0$.

Note 6: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

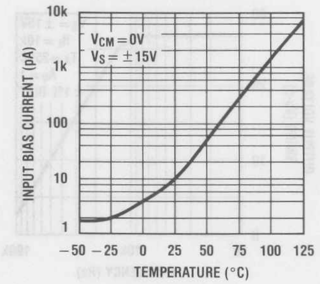
Note 7: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

Typical Performance Characteristics

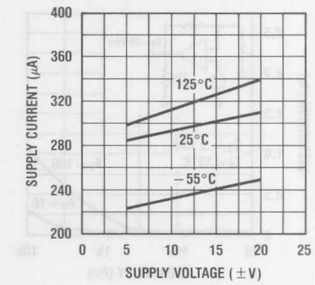
Input Bias Current



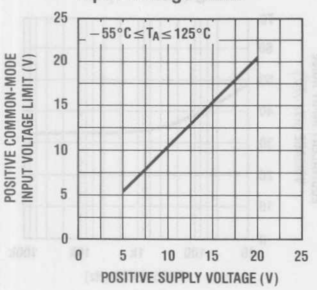
Input Bias Current



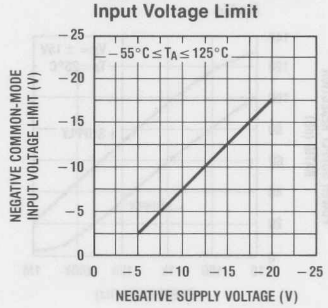
Supply Current



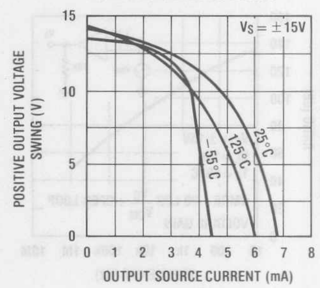
Positive Common-Mode Input Voltage Limit



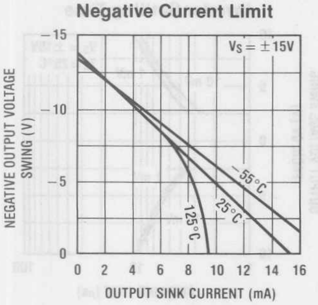
Negative Common-Mode Input Voltage Limit



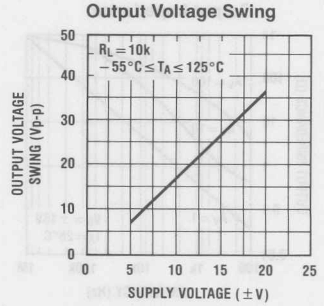
Positive Current Limit



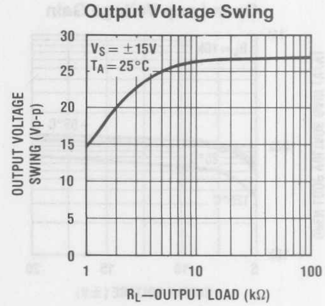
Negative Current Limit



Output Voltage Swing

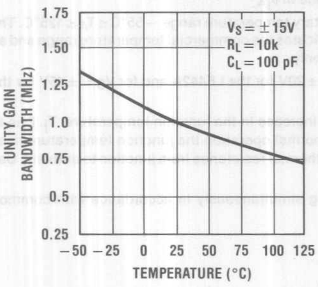


Output Voltage Swing

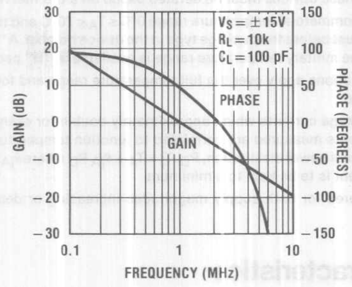


Typical Performance Characteristics (Continued)

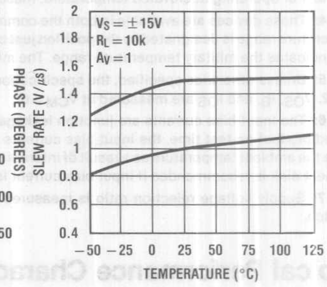
Gain Bandwidth



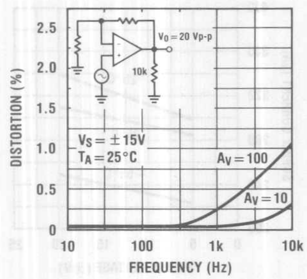
Bode Plot



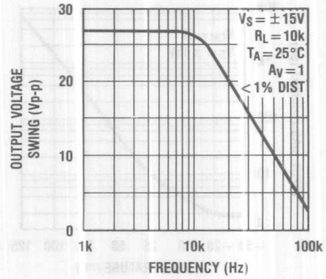
Slew Rate



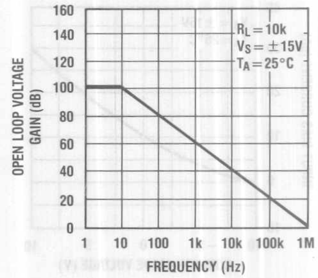
Distortion vs Frequency



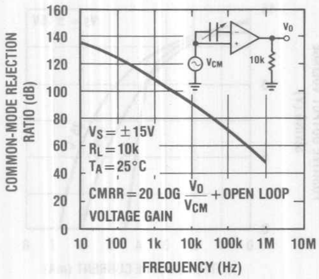
Undistorted Output Voltage Swing



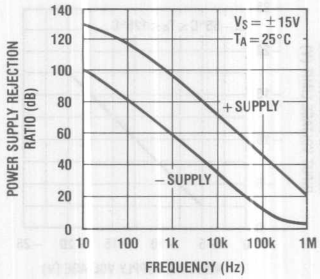
Open Loop Frequency Response



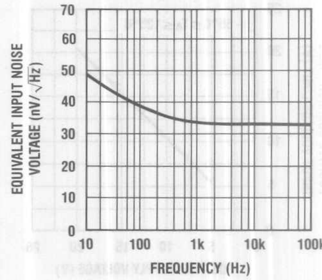
Common-Mode Rejection Ratio



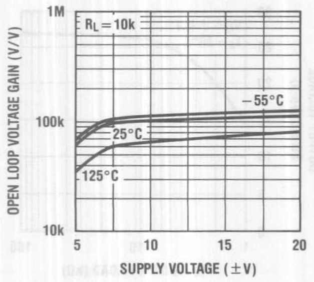
Power Supply Rejection Ratio



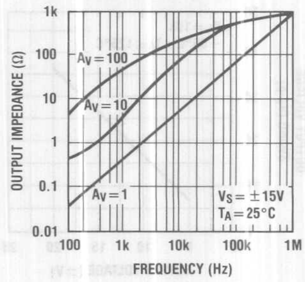
Equivalent Input Noise Voltage



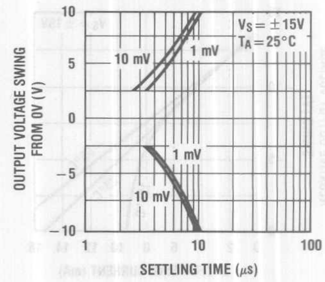
Open Loop Voltage Gain



Output Impedance

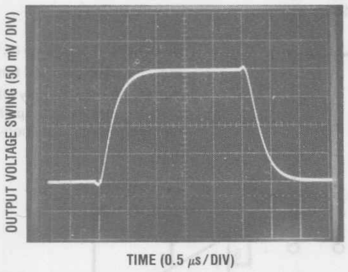


Inverter Settling Time

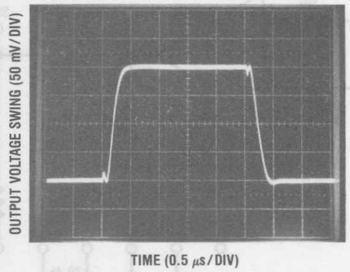


Pulse Response $R_L = 10\ k\Omega$, $C_L = 10\ pF$

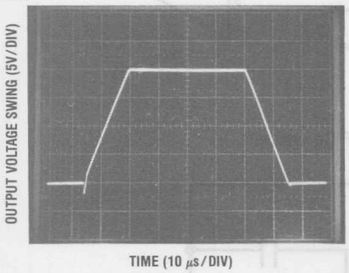
Small Signal Inverting



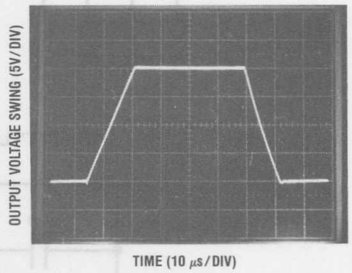
Small Signal Non-Inverting



Large Signal Inverting



Large Signal Non-Inverting



Application Hints

This device is a dual low power op amp with internally trimmed input offset voltages and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased to allow normal circuit operation with power supplies of ±3.0V. Supply voltages less than these may degrade the common-mode rejection and restrict the output voltage swing.

The amplifiers will drive a 10 kΩ load resistance to ±10V over the full temperature range.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

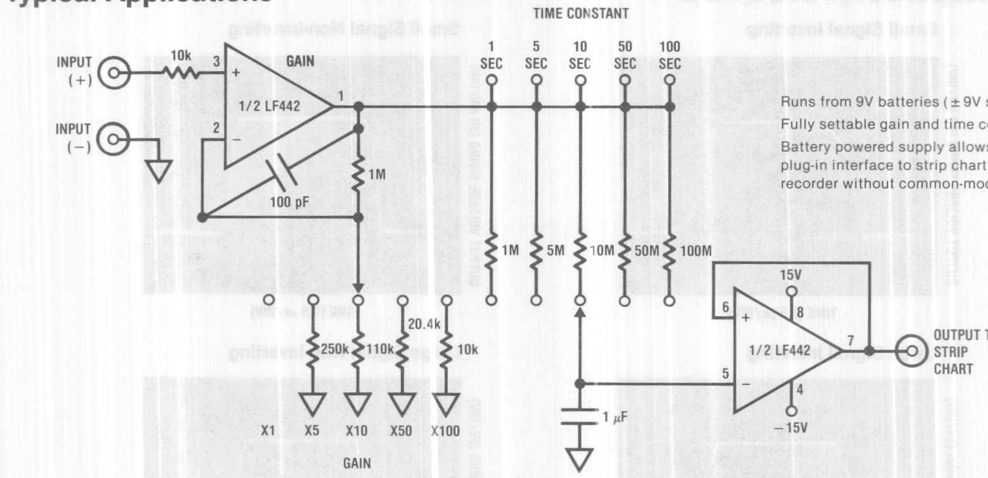
Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

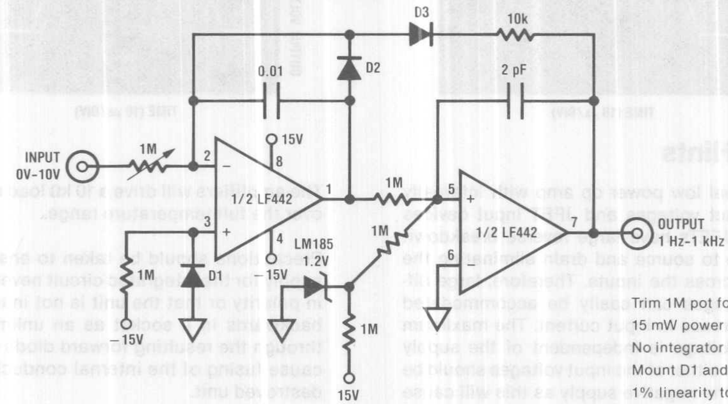
Typical Applications

Battery Powered Strip Chart Preamplifier



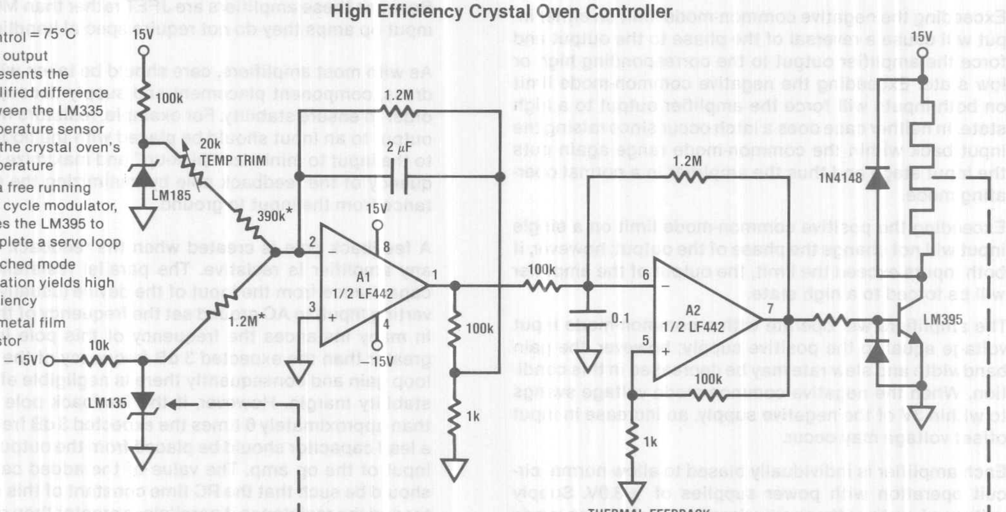
Runs from 9V batteries (± 9V supplies)
Fully settable gain and time constant
Battery powered supply allows direct plug-in interface to strip chart recorder without common-mode problems

"No FET" Low Power V→F Converter



Trim 1M pot for 1 kHz full-scale output
15 mW power drain
No integrator reset FET required
Mount D1 and D2 in close proximity
1% linearity to 1 kHz

High Efficiency Crystal Oven Controller

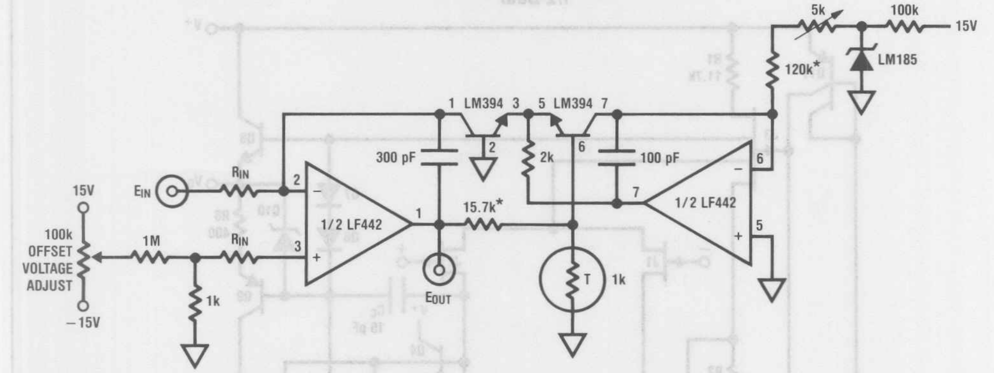


- $T_{control}$ = 75°C
- A1's output represents the amplified difference between the LM335 temperature sensor and the crystal oven's temperature
- A2, a free running duty cycle modulator, drives the LM395 to complete a servo loop
- Switched mode operation yields high efficiency

*1% metal film resistor

Typical Applications (Continued)

Conventional Log Amplifier



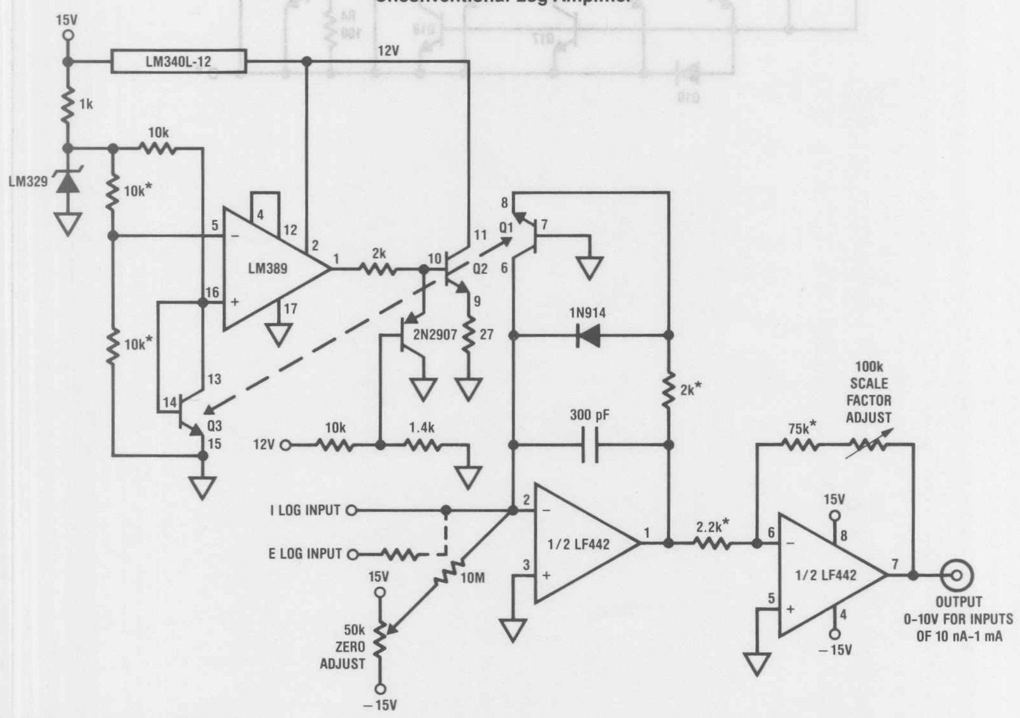
$$E_{OUT} = -\left[\log 10\left(\frac{E_{IN}}{R_{IN}}\right) + 5\right]$$

R_T = Tel Labs type Q81

Trim 5k for 10 μA through the 5k-120k combination

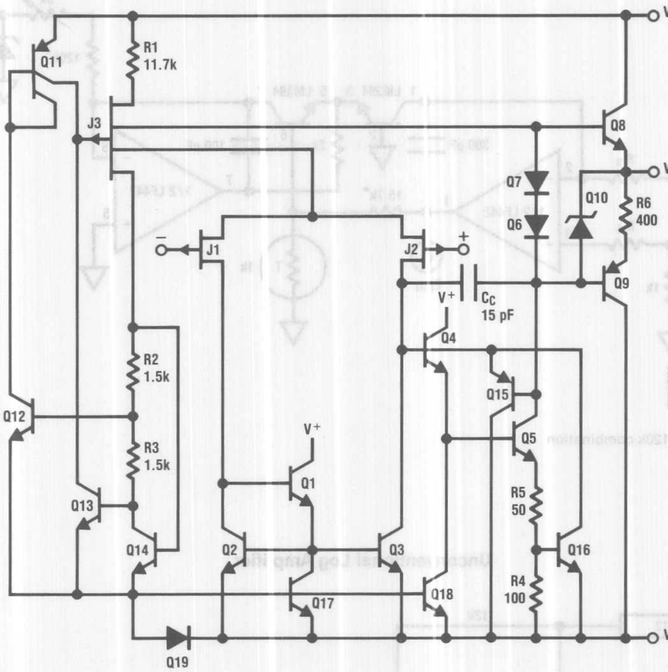
*1% film resistor

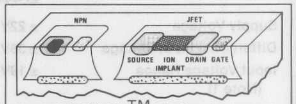
Unconventional Log Amplifier



Q1, Q2, Q3 are included on LM389 amplifier chip which is temperature-stabilized by the LM389 and Q2-Q3, which act as a heater-sensor pair. Q1, the logging transistor, is thus immune to ambient temperature variation and requires no temperature compensation at all.

1/2 Dual


V+
Q11
R1
11.7k
J3
Q8
V0
Q7
Q10
R6
400
Q6
J1
J2
Q9
Cc
15 pF
Q4
R2
1.5k
Q15
Q12
Q5
R3
1.5k
Q1
R5
50
Q13
Q14
Q2
Q3
Q16
Q17
Q18
R4
100
V−
Q19



BI-FET II™ Technology

LF444A/LF444 Quad Low Power JFET Input Operational Amplifier

General Description

The LF444 quad low power operational amplifier provides many of the same AC characteristics as the industry standard LM148 while greatly improving the DC characteristics of the LM148. The amplifier has the same bandwidth, slew rate, and gain (10 kΩ load) as the LM148 and only draws one fourth the supply current of the LM148. In addition the well matched high voltage JFET input devices of the LF444 reduce the input bias and offset currents by a factor of 10,000 over the LM148. The LF444 also has a very low equivalent input noise voltage for a low power amplifier.

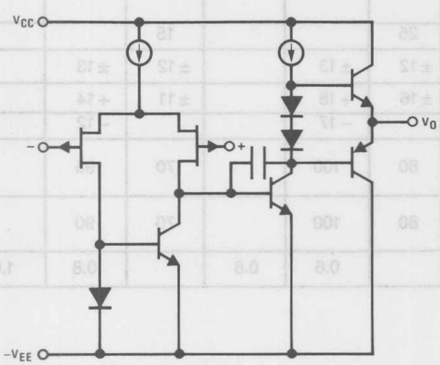
The LF444 is pin compatible with the LM148 allowing an immediate 4 times reduction in power drain in many applications. The LF444 should be used wherever low power dissipation and good electrical characteristics are the major considerations.

Features

- 1/4 supply current of a LM148 — 200 μA/Amplifier (max)
- Low input bias current — 50 pA (max)
- High gain bandwidth — 1 MHz
- High slew rate — 1V/μs
- Low noise voltage for low power — 35 nV/$\sqrt{\text{Hz}}$
- Low input noise current — 0.01 pA/$\sqrt{\text{Hz}}$
- High input impedance — $10^{12}\Omega$
- High gain $V_O = \pm 10V$, $R_L = 10k$ — 50k (min)

Simplified Schematic

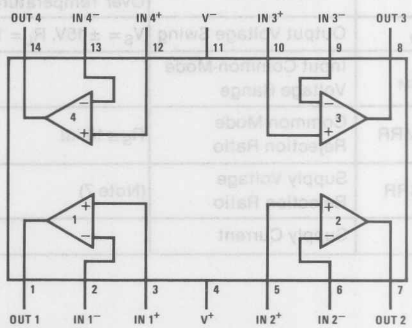
1/4 Quad



Connection Diagram

LF444AMD/LF444CD/LF444ACN/LF444CN

Dual-In-Line Package



TOP VIEW

Order Number LF444AMD or LF444CD See NS Package D14E

Order Number LF444ACN or LF444CN See NS Package N14A

Ordering Information

LF444XYZ

X indicates electrical grade

Y indicates temperature range "M" for military, "C" for commercial

Z indicates package type "D" or "N"

BI-FET II™ is a trademark of National Semiconductor Corp.

Absolute Maximum Ratings

	LF444A	LF444
Supply Voltage	±22V	±18V
Differential Input Voltage	±38V	±30V
Input Voltage Range (Note 1)	±19V	±15V
Output Short Circuit Duration (Note 2)	Continuous	Continuous

	H Package	N Package
Power Dissipation (Note 3)	900 mW	500 mW
T_j max	150°C	115°C
θ_{jA}	100°C/W	150°C/W
Operating Temperature Range	(Note 4)	(Note 4)
Storage Temperature Range	$-65°C \leq T_A \leq 150°C$	$-65°C \leq T_A \leq 150°C$
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

DC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions		LF444A Min	LF444A Typ	LF444A Max	LF444 Min	LF444 Typ	LF444 Max	Units
V_{OS}	Input Offset Voltage	$R_S = 10k$, $T_A = 25°C$			2	5		3	10	mV
		$0°C \leq T_A \leq 70°C$				6.5			12	mV
		$-55°C \leq T_A \leq 125°C$				8				mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\ k\Omega$			10			10		μV/°C
I_{OS}	Input Offset Current	$V_S = \pm 15V$ (Notes 5 and 6)	$T_j = 25°C$		5	25		5	50	pA
			$T_j = 70°C$			1.5			1.5	nA
			$T_j = 125°C$			10				nA
I_B	Input Bias Current	$V_S = \pm 15V$ (Notes 5 and 6)	$T_j = 25°C$		10	50		10	100	pA
			$T_j = 70°C$			3			3	nA
			$T_j = 125°C$			20				nA
R_{IN}	Input Resistance	$T_j = 25°C$			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 10\ k\Omega$, $T_A = 25°C$		50	100		25	100		V/mV
		Over Temperature		25			15			V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$		±12	±13		±12	±13		V
V_{CM}	Input Common-Mode Voltage Range			±16	+18		±11	+14		V
					−17			−12		V
CMRR	Common-Mode Rejection Ratio	$R_S \leq 10\ k\Omega$		80	100		70	95		dB
PSRR	Supply Voltage Rejection Ratio	(Note 7)		80	100		70	90		dB
I_S	Supply Current				0.6	0.8		0.8	1.0	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Min	Typ	Max	Units
	Amplifier-to-Amplifier Coupling			−120			−120		dB
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$		1			1		V/μs
GBW	Gain-Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$		1			1		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, f = 1 kHz		35			35		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_A = 25°C$, f = 1 kHz		0.01			0.01		$pA/\sqrt{Hz}$

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 3: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{jA}.

Note 4: The LF444A is available in both the commercial temperature range $0°C \leq T_A \leq 70°C$ and the military temperature range $-55°C \leq T_A \leq 125°C$. The LF444 is available in the commercial temperature range only. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "D" package only.

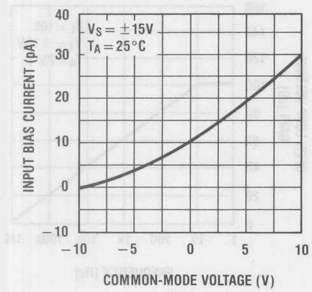
Note 5: Unless otherwise specified the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF444A and for $V_S = \pm 15V$ for the LF444. V_{OS}, I_B, and I_{OS} are measured at $V_{CM} = 0$.

Note 6: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

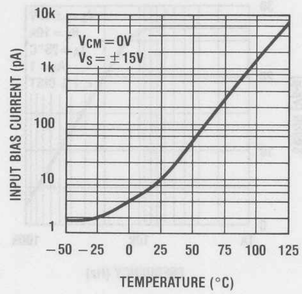
Note 7: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

Typical Performance Characteristics

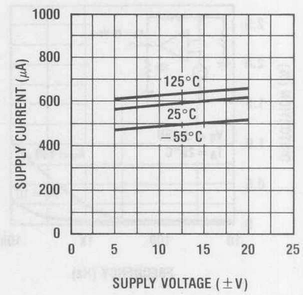
Input Bias Current



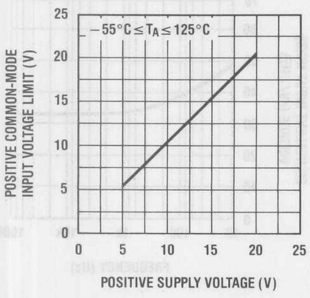
Input Bias Current



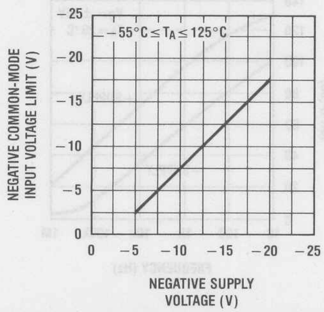
Supply Current



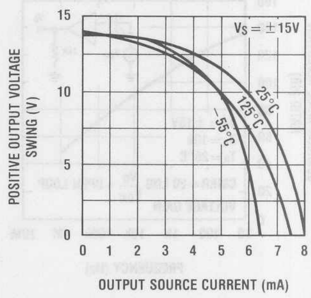
Positive Common-Mode Input Voltage Limit

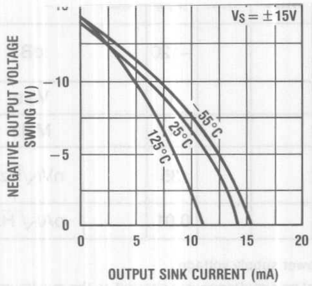


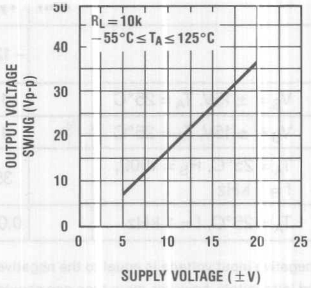
Negative Common-Mode Input Voltage Limit

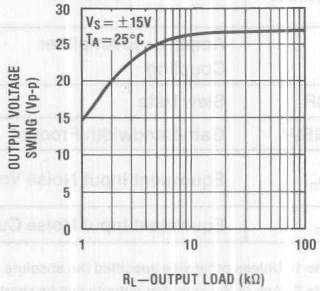


Positive Current Limit

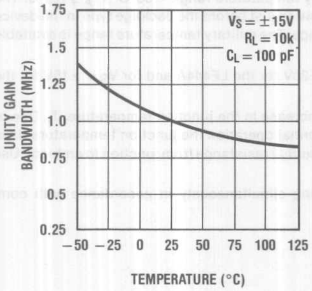




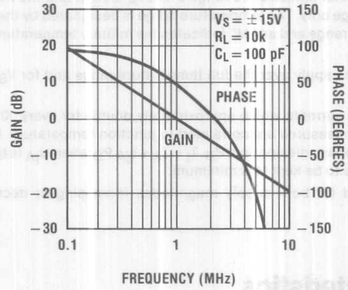




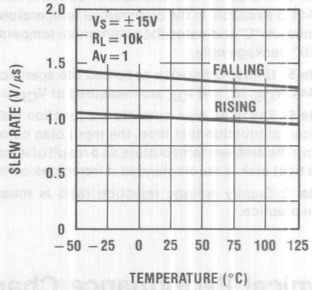
Gain Bandwidth



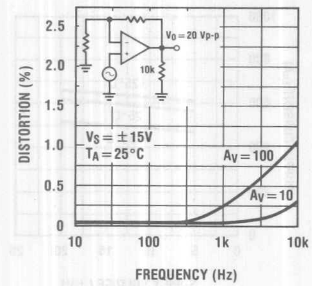
Bode Plot



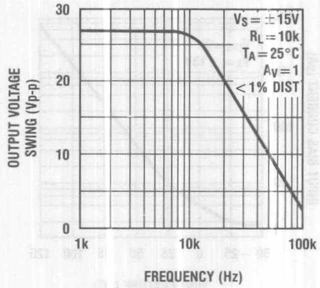
Slew Rate



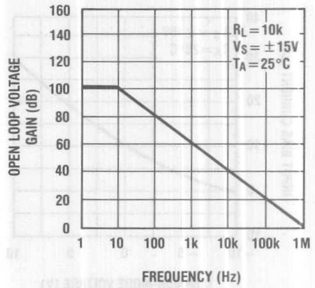
Distortion vs Frequency



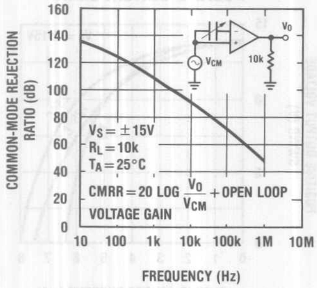
Undistorted Output Voltage Swing



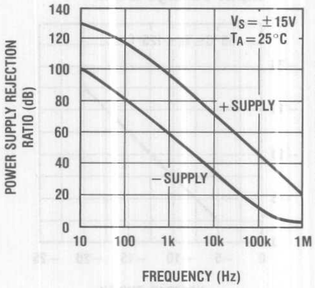
Open Loop Frequency Response



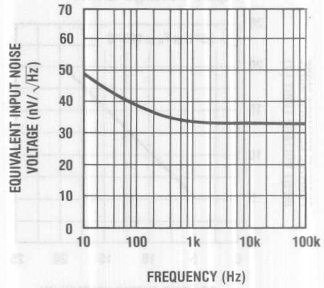
Common-Mode Rejection Ratio



Power Supply Rejection Ratio

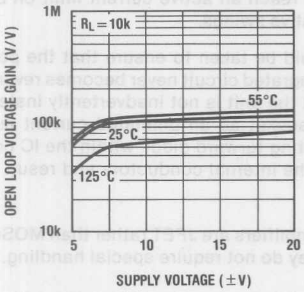


Equivalent Input Noise Voltage

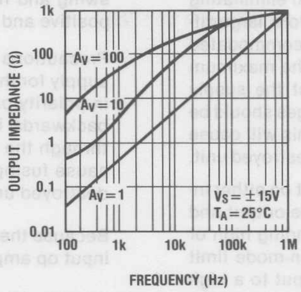


Typical Performance Characteristics (Continued)

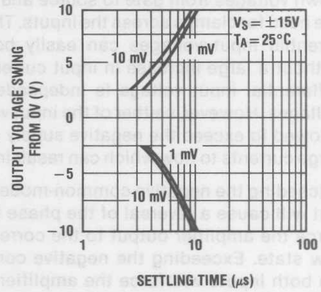
Open Loop Voltage Gain



Output Impedance

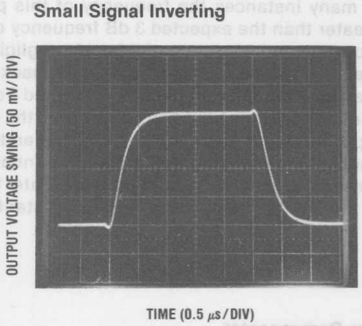


Inverter Settling Time

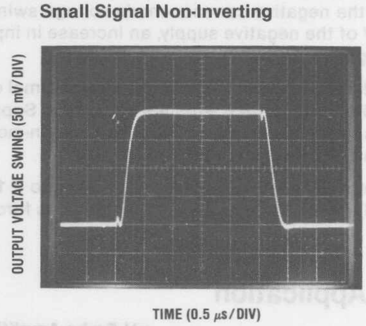


Pulse Response $R_L = 10\ k\Omega$, $C_L = 10\ pF$

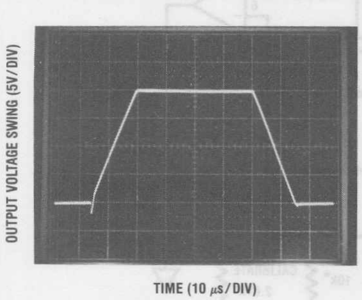
Small Signal Inverting



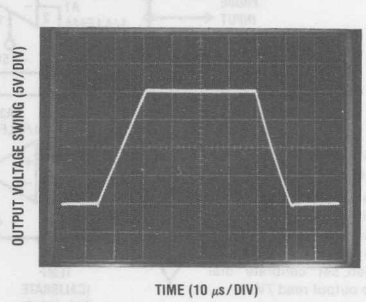
Small Signal Non-Inverting



Large Signal Inverting



Large Signal Non-Inverting



Application Hints

This device is a quad low power op amp with JFET input devices (BI-FET). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased to allow normal circuit operation with power supplies of ±3.0V. Supply voltages less than these may degrade the common-mode rejection and restrict the output voltage swing.

The amplifiers will drive a 10 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

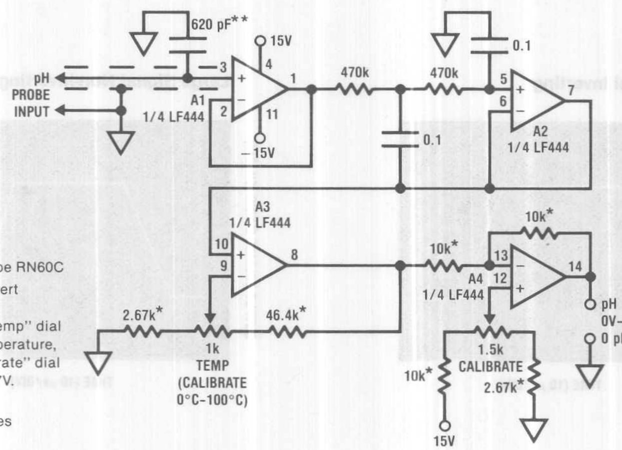
Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Application

pH Probe Amplifier/Temperature Compensator



** Polystyrene

* Film resistor type RN60C

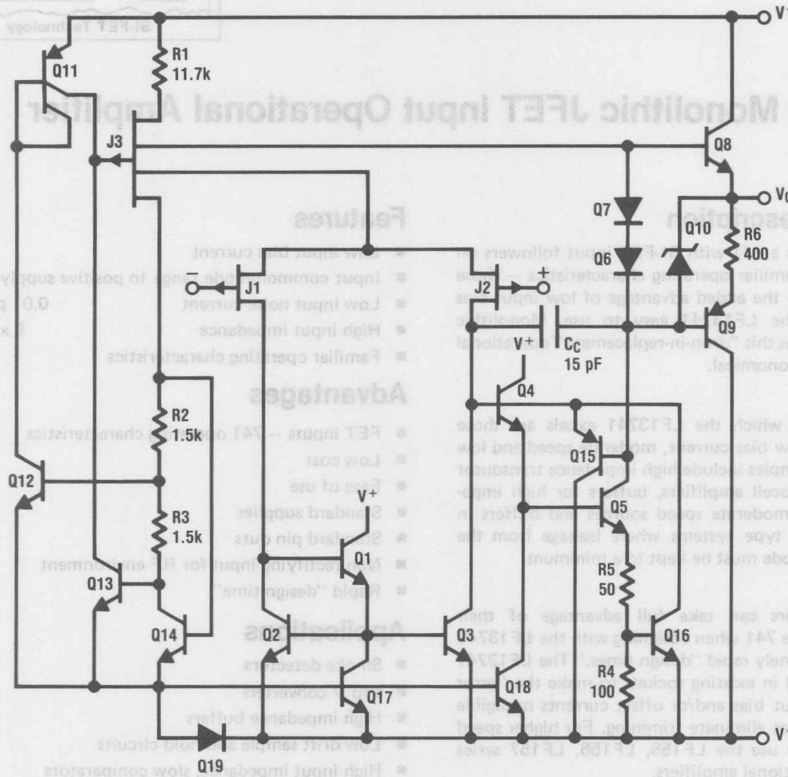
To calibrate, insert probe in pH = 7 solution. Set "temp" dial to solution temperature, then, set "calibrate" dial so output read 7V.

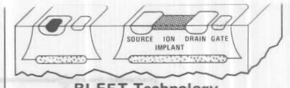
Typical probe = Ingold Electrodes #465-35

BI-FET™ is a trademark of National Semiconductor Corp.

Detailed Schematic

1/4 Quad





BI-FET Technology

LF13741 Monolithic JFET Input Operational Amplifier

General Description

The LF13741 is a 741 with BI-FET input followers on the same die. Familiar operating characteristics — those of a 741 — with the added advantage of low input bias current make the LF13741 easy to use. Monolithic fabrication makes this "drop-in-replacement" operational amplifier very economical.

Applications in which the LF13741 excels are those which require low bias current, moderate speed and low cost. A few examples include high impedance transducer amplifiers, photocell amplifiers, buffers for high impedance, slow to moderate speed sources and buffers in sample-and-hold type systems where leakage from the hold capacitor node must be kept to a minimum.

Systems designers can take full advantage of their knowledge of the 741 when designing with the LF13741 to achieve extremely rapid "design times." The LF13741 can also be used in existing sockets to make the "error budget" for input bias and/or offset currents negligible and in many cases eliminate trimming. For higher speed and lower noise use the LF155, LF156, LF157 series of BI-FET operational amplifiers.

Features

- Low input bias current 50 pA
- Input common-mode range to positive supply voltage
- Low input noise current $0.01\ pA/\sqrt{Hz}$
- High input impedance $5 \times 10^{11}\Omega$
- Familiar operating characteristics

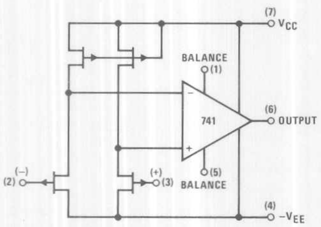
Advantages

- FET inputs — 741 operating characteristics
- Low cost
- Ease of use
- Standard supplies
- Standard pin outs
- Non-rectifying input for RF environment
- Rapid "design time"

Applications

- Smoke detectors
- I to V converters
- High impedance buffers
- Low drift sample and hold circuits
- High input impedance, slow comparators
- Long time timers
- Low drift peak detectors
- Supply current monitors
- Low error budget systems

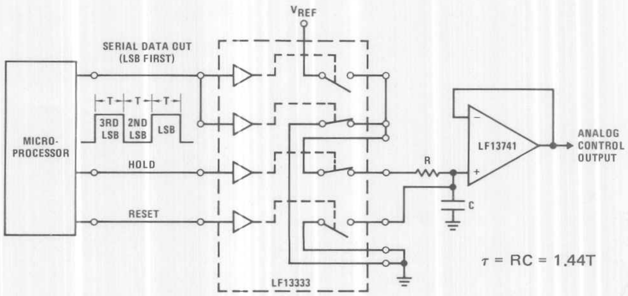
Simplified Schematic



All on one die.

Typical Applications

Inexpensive Microprocessor D/A



$\tau = RC = 1.44T$

Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation (Note 1)	500 mW
Operating Temperature Range	0°C to +70°C
$T_{j(MAX)}$	100°C
Differential Input Voltage	±30V
Input Voltage Range (Note 2)	±16V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$R_S = 10\ k\Omega$, $T_A = 25°C$		5	15	mV
		Over Temperature			20	mV
	Voltage Offset Adjustment Range		10			mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\ k\Omega$		10		μV/°C
I_{OS}	Input Offset Current	$T_j = 25°C$, (Notes 3, 4)		10	50	pA
		$T_j \leq 70°C$			2	nA
I_B	Input Bias Current	$T_j = 25°C$, (Notes 3, 4)		50	200	pA
		$T_j \leq 70°C$		1.6	8	nA
R_{IN}	Input Resistance	$T_j = 25°C$		5×10^{11}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $T_A = 25°C$ $V_O = \pm 10V$, $R_L = 2\ k\Omega$	25	100		V/mV
		Over Temperature	15			V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$	±12	±13		V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm 15V$	±11	+15.1		V
				−12		V
CMRR	Common-Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	90		dB
PSRR	Supply Voltage Rejection Ratio	(Note 5)	77	96		dB
I_S	Supply Current			2	4	mA

AC Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$		0.5		V/μs
GBW	Gain-Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$		1.0		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\ \Omega$				
		f = 100 Hz		50		$nV/\sqrt{Hz}$
		f = 1000 Hz		37		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_j = 25°C$				
		f = 100 Hz		0.01		$pA/\sqrt{Hz}$
		f = 1000 Hz		0.01		$pA/\sqrt{Hz}$

Note 1: For operating at elevated temperature, the device must be derated based on a thermal resistance of 150°C/W junction to ambient or 45°C/W junction to case.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

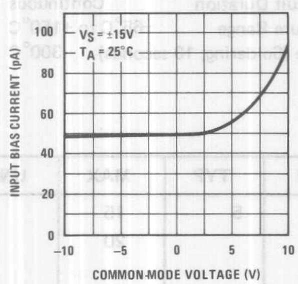
Note 3: These specifications apply for $V_S = \pm 15V$ and $0°C \leq T_A \leq +70°C$. V_{OS}, I_B, and I_{OS} are measured at $V_{CM} = 0$.

Note 4: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \Theta_{jA} P_D$ where Θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

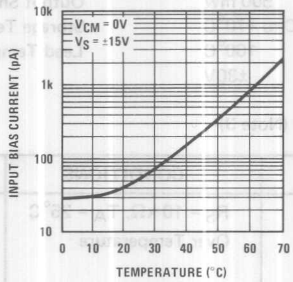
Note 5: Supply Voltage Rejection Ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

Typical Performance Characteristics

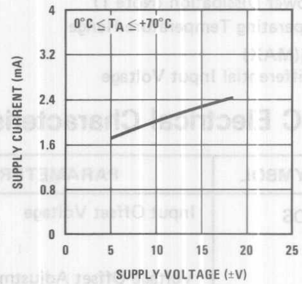
Input Bias Current



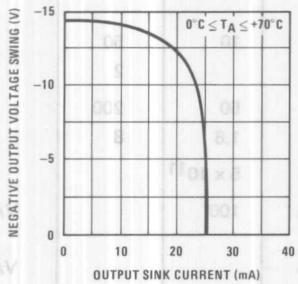
Input Bias Current



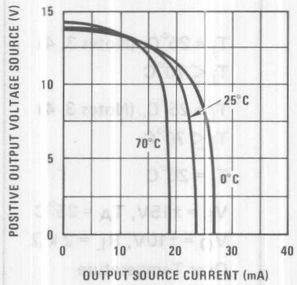
Supply Current



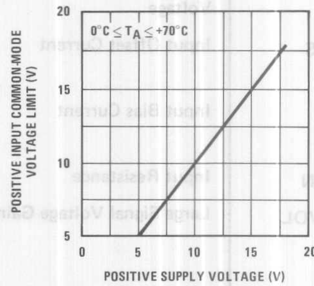
Negative Current Limit



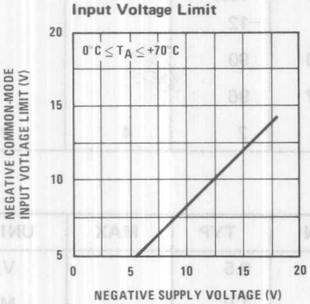
Positive Current Limit



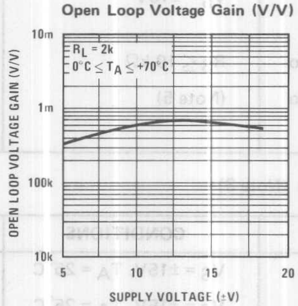
Positive Common-Mode Input Voltage Limit



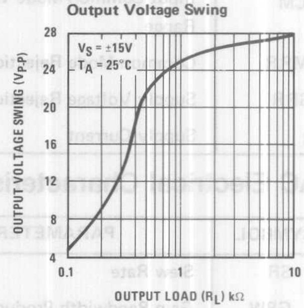
Negative Common-Mode Input Voltage Limit



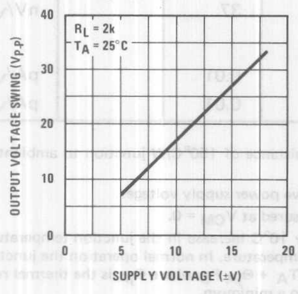
Open Loop Voltage Gain (V/V)



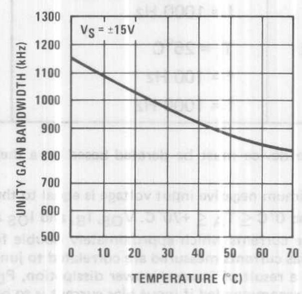
Output Voltage Swing



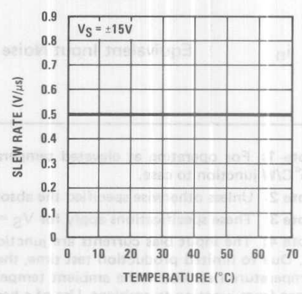
Voltage Swing



Gain Bandwidth

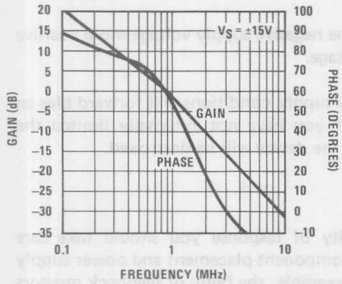


Slew Rate

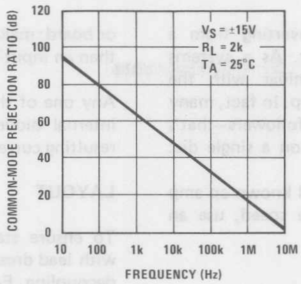


Typical Performance Characteristics (Continued)

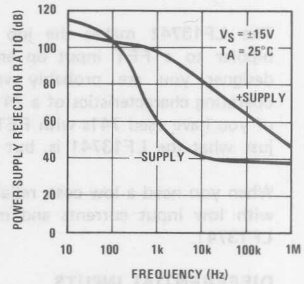
Bode Plot



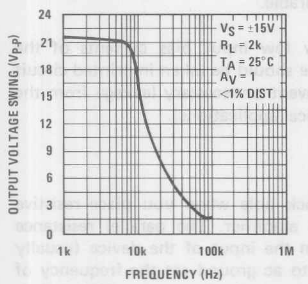
Common-Mode Rejection Ratio



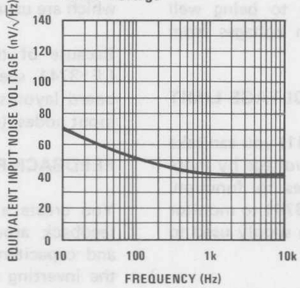
Power Supply Rejection Ratio



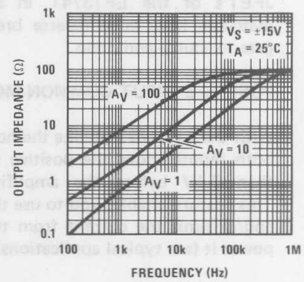
Undistorted Output Voltage Swing



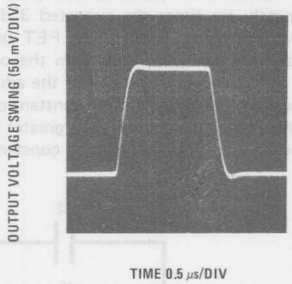
Equivalent Input Noise Voltage



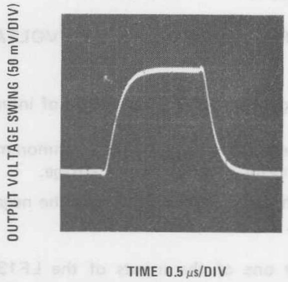
Output Impedance



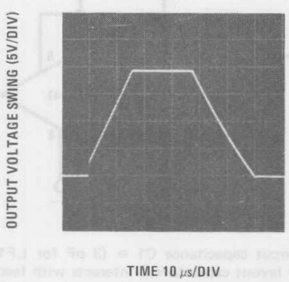
Small Signal Non-Inverting Pulse Response



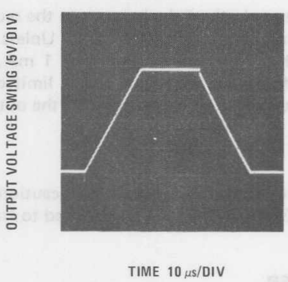
Small Signal Inverting Pulse Response



Large Signal Non-Inverting Pulse Response



Large Signal Inverting Pulse Response



bipolar to a FET input op amp easy. As a systems designer you are probably very familiar with the operating characteristics of a 741 op amp. In fact, many of you have used 741s with FET input followers—that's just what the LF13741 is, but it's all on a single die.

When you need a low cost, reliable, well known op amp with low input currents and moderate speed, use an LF13741.

DIFFERENTIAL INPUTS

You don't have to use clamps across the inputs for differential input voltages of less than 40V. The input JFET's of the LF13741, in addition to being well matched, have large reverse breakdown voltages from gate to source and drain.

POSITIVE INPUT COMMON-MODE VOLTAGE LIMIT

With the LF13741 (unlike the normal 741) you can take both inputs above the positive supply voltage by more than 0.1V before the amplifier ceases to function. This feature enables you to use the LF13741 to monitor and/or limit the current from the same supply used to power it (see typical applications).

If you exceed the positive common-mode voltage limit on only one input the output phase will remain correct. When you exceed the limit on both inputs, the output phase is unpredictable.

NEGATIVE INPUT COMMON-MODE VOLTAGE LIMIT

There are two negative input voltage ranges of interest:

1. The range between the negative common-mode voltage limit and the negative supply voltage.
2. Voltages which are more negative than the negative supply voltage.

If you take only one of the inputs of the LF13741 into the first range, the output phase will remain correct. When you take both inputs into this range the output will go toward the positive supply voltage.

If you force either or both of the inputs into the second range, an internal diode will be turned "ON." Unless you externally limit the diode current to about 1 mA, the device will be destroyed. In either case, limited or unlimited input current, you cannot predict the output.

HANDLING

You do not have to take any special precautions in handling the LF13741. It has JFET, as opposed to fragile MOSFET, inputs.

APPLYING POWER

You should never: reverse the power supplies to the LF13741; plug a part in backwards in a powered socket than an input voltage.

Any one of these supply conditions will forward bias an internal diode. If you have not externally limited the resulting current, the device will be destroyed.

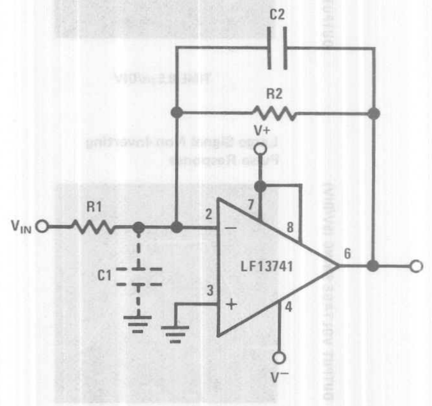
LAYOUT

To ensure stability of response you should take care with lead dress, component placement and power supply decoupling. For example, the body of feedback resistors (from output to input pins) should be placed close to the inverting input pin. Noise "pickup" and capacitance to ground from the input pin will be minimized—effects which are usually desirable.

Because of the very low input bias currents of the LF13741, special care should be taken in printed circuit board layouts to prevent unnecessary leakage from the input nodes, (see typical applications).

FEEDBACK POLE

You create a feedback pole when you place resistive feedback around an amplifier. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency, (a distinct possibility when using FET op amps) you should place a lead capacitor from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant *(Figure 1)*.



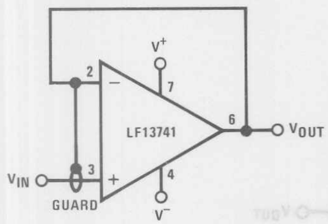
Parasitic input capacitance C1 ≅ (3 pF for LF13741 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate, add C2 such that: R2C2 ≅ R1C1.

FIGURE 1

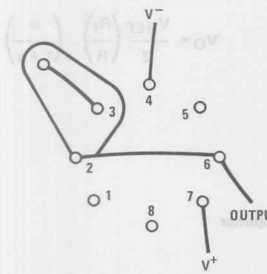
Typical Applications (Continued)

Circuits Using Guard Rings to Prevent Leakage Currents Between Inputs and V^-

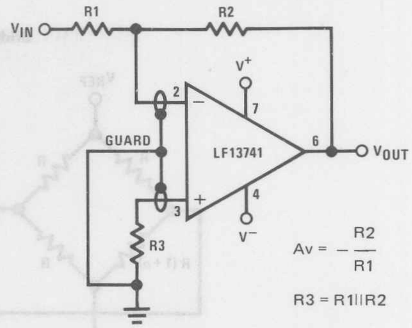
Guarded Voltage Follower



PC Layout



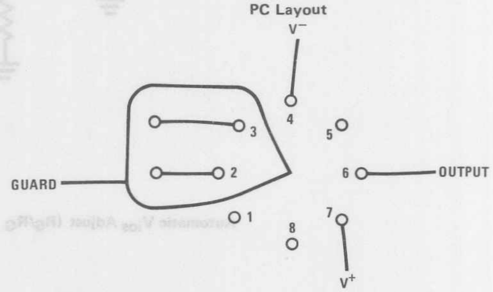
Guarded Inverting Amplifier



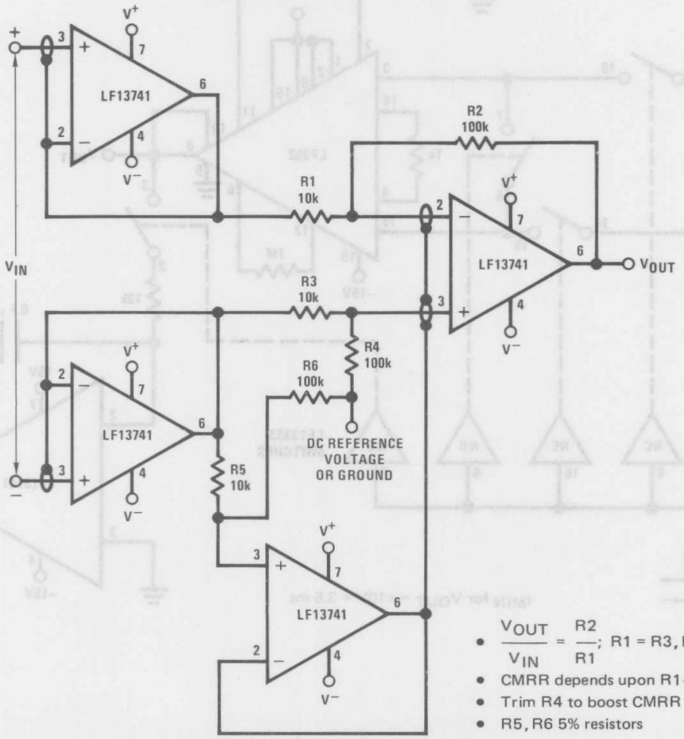
$$A_V = -\frac{R2}{R1}$$

$R3 = R1 \| R2$

PC Layout



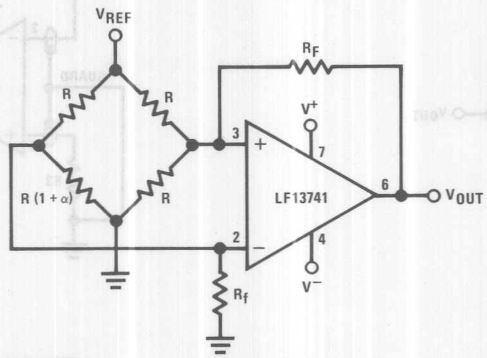
Guarded Instrumentation Amplifier



- $\frac{V_{OUT}}{V_{IN}} = \frac{R2}{R1}$; $R1 = R3, R2 = R4$
- CMRR depends upon R1–R3, R2–R4 matching
- Trim R4 to boost CMRR
- R5, R6 5% resistors

Typical Applications (Continued)

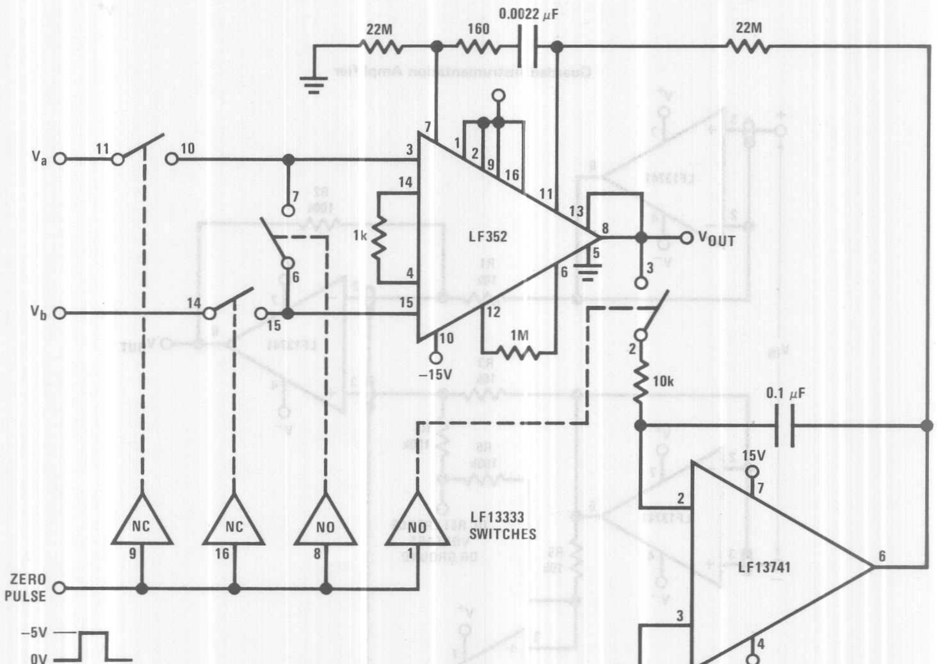
Bridge Amplifier



For $R_f >> R$

$$V_O = \frac{V_{REF}}{2}\left(\frac{R_f}{R}\right)\left(\frac{\alpha}{1+\alpha}\right)$$

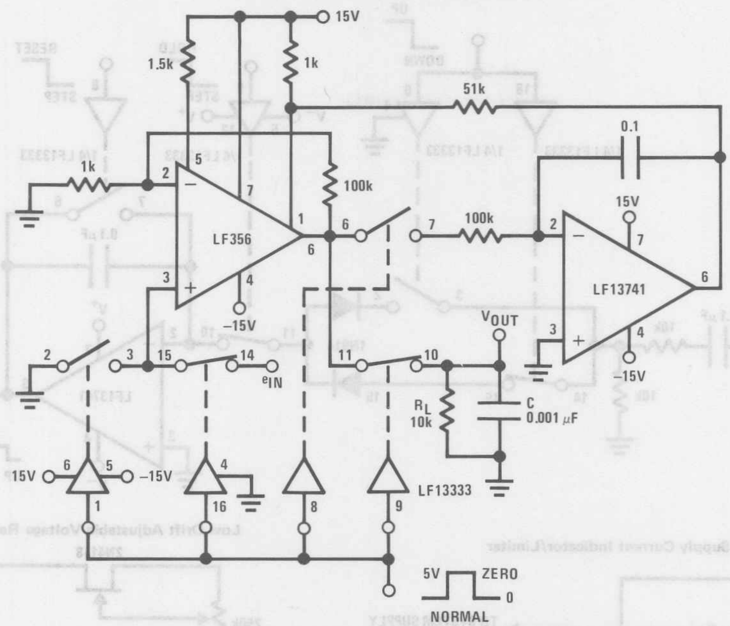
Automatic V_{ios} Adjust ($R_S/R_G \geq 100$) For Instrumentation Amplifier



t_{MIN} for $V_{OUT} = \pm 10V = 3.5$ ms

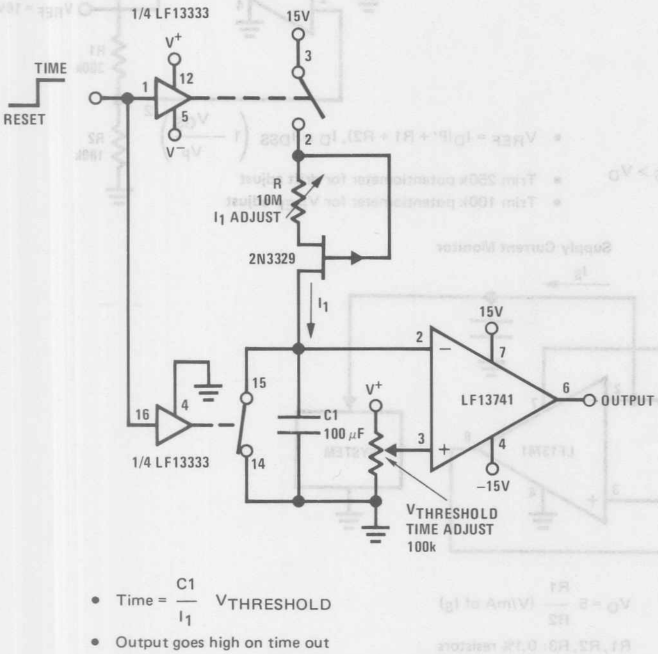
Typical Applications (Continued)

Auto Zero Circuit for LF356



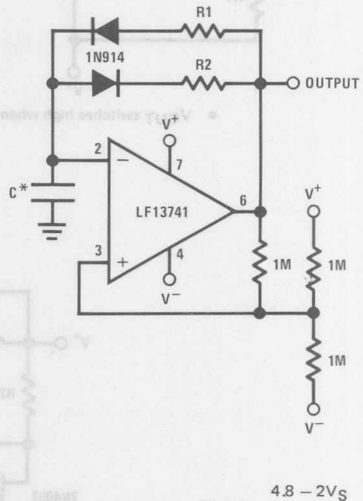
- With the output having a 10k load resistor minimum pulse width to zero ≈800 μs
- The capacitor on the output reduces the output switch glitch

Long Time Timer



- Time = $\frac{C1}{I_1} V_{THRESHOLD}$
- Output goes high on time out
- Reverse op amp inputs for output low on time out
- C1 low leakage capacitor

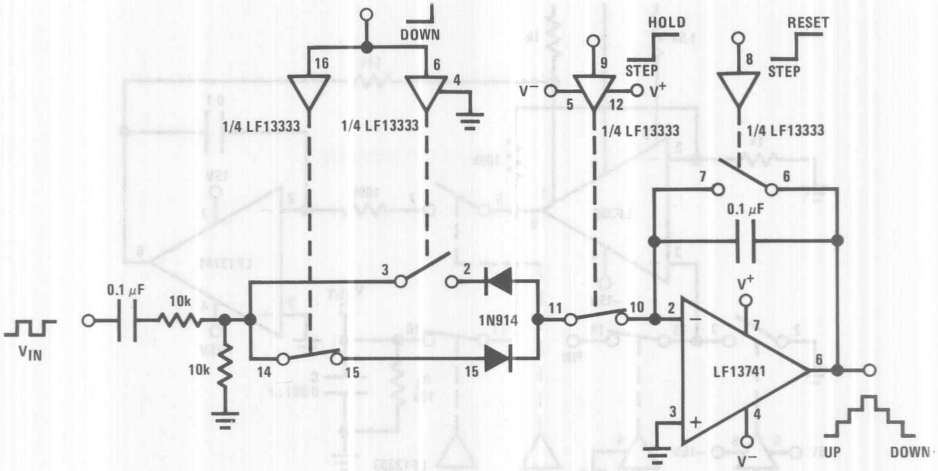
Ultra-Low (Or High) Duty Cycle Pulse Generator



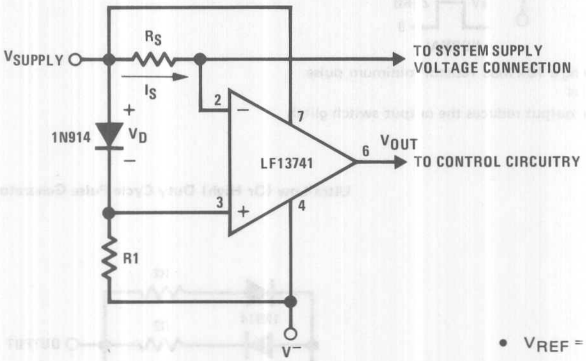
- $t_{OUTPUT\ HIGH} \approx R1C \ln \frac{4.8 - 2V_S}{4.8 - V_S}$
- $t_{OUTPUT\ LOW} \approx R2C \ln \frac{2V_S - 7.8}{V_S - 7.8}$

where $V_S = V^+ + |V^-|$

*low leakage capacitor

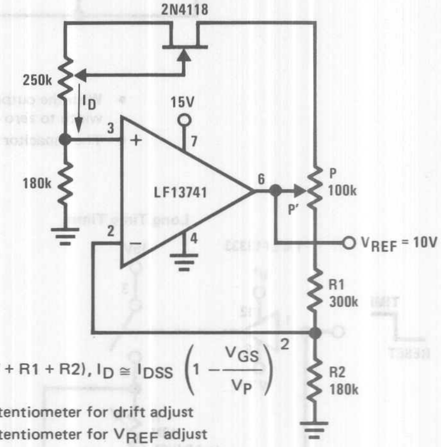


Supply Current Indicator/Limiter



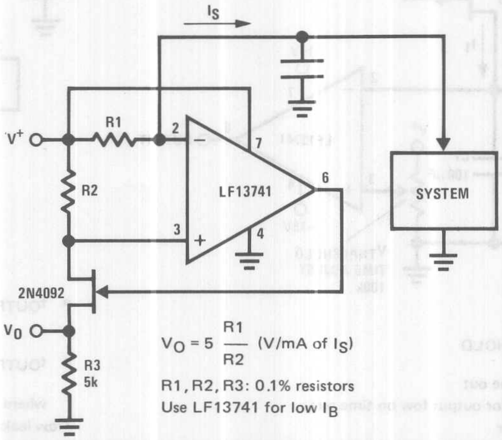
- V_{OUT} switches high when $R_S I_S > V_D$

Low Drift Adjustable Voltage Reference



- $V_{REF} = I_D(P' + R1 + R2),\ I_D \cong I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$
- Trim 250k potentiometer for drift adjust
- Trim 100k potentiometer for V_{REF} adjust

Supply Current Monitor



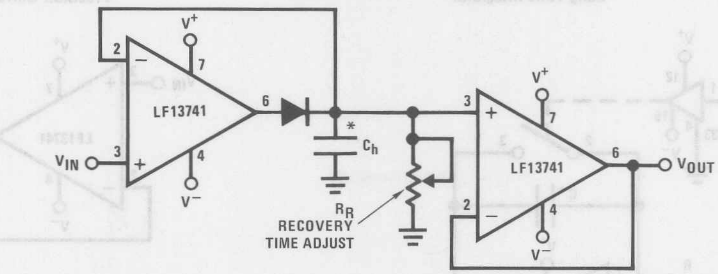
$$V_O = 5\ \frac{R1}{R2}\ \text{(V/mA of } I_S\text{)}$$

R1, R2, R3: 0.1% resistors

Use LF13741 for low I_B

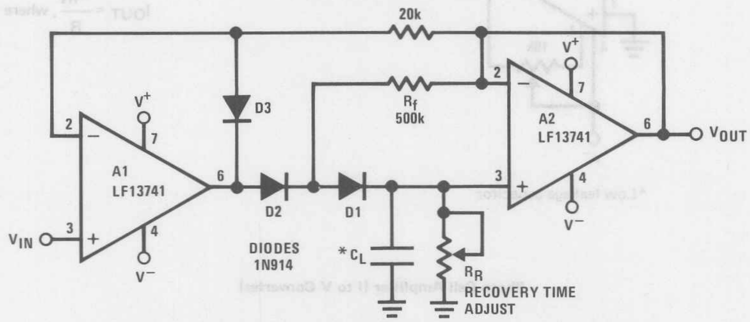
Typical Applications (Continued)

Low Drift Peak Detector



*Low leakage capacitor

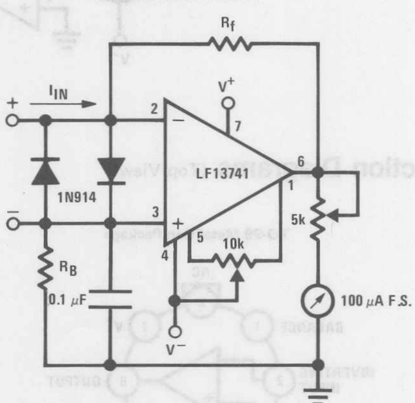
Ultra-Low Drift Peak Detector



- By adding D1 and R_f, V_{D1} = 0 during hold mode. Leakage of D2 provided by feedback path through R_f.
- Leakage of circuit is I_B plus leakage of C_h.
- D3 clamps V_{OUT} A1 to $V_{IN} - V_{D3}$ to improve speed and to limit the reverse bias of D2.
- Maximum input frequency should be << $1/2\pi R_f C_{D2}$, where C_{D2} is the shunt capacitance of D2.

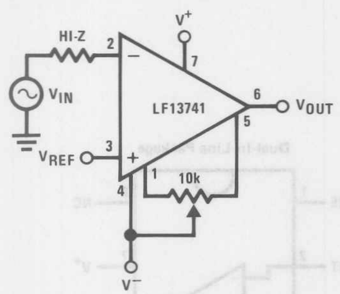
*Low leakage capacitor

Low Current Ammeter



$I_{FULL\ SCALE}$	R_F	R_B
100 nA	1.5M	1.5M
500 nA	300k	300k
1 μA	300k	0
5 μA	60k	0
10 μA	30k	0
50 μA	6k	0
100 μA	3k	0

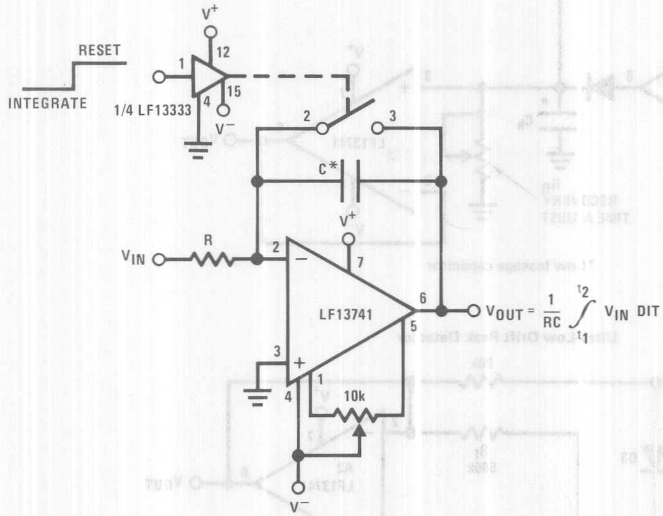
Comparator with Offset Adjust for Hi-Z Inputs



$V^- + 3V \leq V_{IN} \leq V^+ + 0.1V$

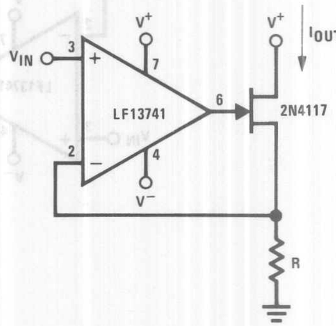
Typical Applications (Continued)

Long Time Integrator



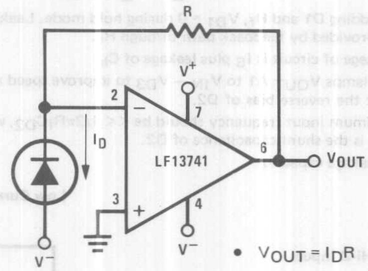
*Low leakage capacitor

Precision Current Sink



$I_{OUT} = \frac{V_{IN}}{R}$, where $I_{OUT} \leq I_{DSS}$

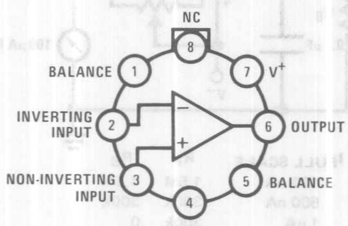
Photo Cell Amplifier (I to V Converter)



- $V_{OUT} = I_D R$

Connection Diagrams (Top Views)

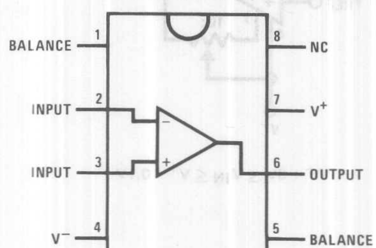
TO-99 Metal Can Package



Order Number LF13741H
See NS Package H08C

Note: Pin 4 connected to case.

Dual-In-Line Package



Order Number LF13741N
See NS Package N08B

LM10/LM10B(L)/LM10C(L) Op Amp and Voltage Reference

General Description

The LM10 series are monolithic linear ICs consisting of a precision reference, an adjustable reference buffer and an independent, high quality op amp.

The unit can operate from a total supply voltage as low as 1.1V or as high as 40V, drawing only 270μA. A complementary output stage swings within 15 mV of the supply terminals or will deliver ±20 mA output current with ±0.4V saturation. Reference output can be as low as 200 mV. Some other characteristics of the LM10 are

- input-offset voltage 2.0 mV (max)
- input-offset current 0.7 nA (max)
- input-bias current 20 nA (max)
- reference regulation 0.1% (max)
- offset-voltage drift 2μV/°C
- reference drift 0.002%/°C

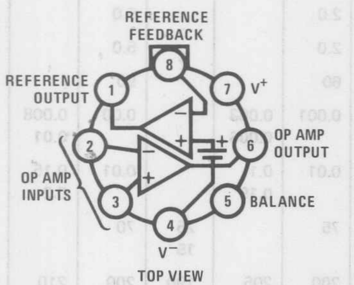
The circuit is recommended for portable equipment and is completely specified for operation from a single power cell. In contrast, high output-drive capability, both voltage and current, along with thermal overload protection, suggest it in demanding general-purpose applications.

The device is capable of operating in a floating mode, independent of fixed supplies. It can function as a remote comparator, signal conditioner, SCR controller or transmitter for analog signals, delivering the processed signal on the same line used to supply power. It is also suited for operation in a wide range of voltage- and current-regulator applications, from low voltages to several hundred volts, providing greater precision than existing ICs.

This series is available in the three standard temperature ranges, with the commercial part having relaxed limits. In addition, a low-voltage specification (suffix "L") is available in the limited temperature ranges at a cost savings.

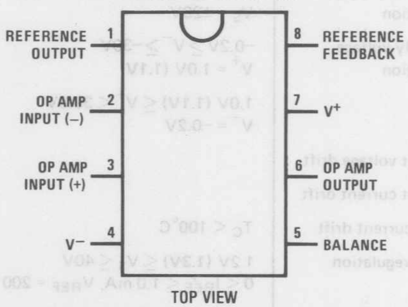
Connection and Functional Diagrams

Metal Can Package (H)

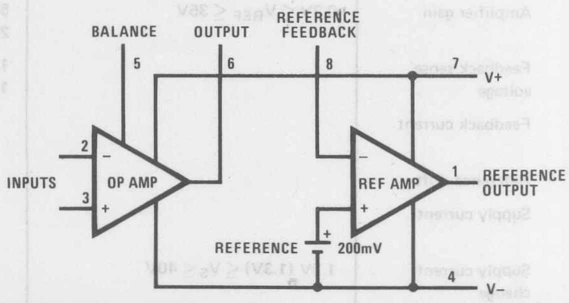


Order Number LM10H, LM10BH, LM10CH, LM10BLH or LM10CLH See NS Package H08A

Dual-In-Line Package (N)



Order Number LM10CN or LM10CLN See NS Package N08B



Differential input voltage (note 1)	±40V	±7V
Power dissipation (note 2)	internally limited	
Output short-circuit duration (note 3)	indefinite	
Storage-temperature range	−55°C to +150°C	
Lead temperature (soldering, 10s)	300°C	

Electrical Characteristics ($T_J = 25°C$, $T_{MIN} \le T_J \le T_{MAX}$, note 4)

(Boldface type refers to limits over temperature range.)

PARAMETER	CONDITIONS	LM10/LM10B MIN	LM10/LM10B TYP	LM10/LM10B MAX	LM10C MIN	LM10C TYP	LM10C MAX	UNITS
Input offset voltage			0.3	2.0		0.5	4.0	mV
				3.0			**5.0**	mV
Input offset current			0.25	0.7		0.4	2.0	nA
(note 5)				**1.5**			**3.0**	nA
Input bias current			10	20		12	30	nA
				30			**40**	nA
Input resistance		250	500		150	400		kΩ
		150			**115**			kΩ
Large signal voltage	$V_S = \pm 20V$, $I_{OUT} = 0$	120	400		80	400		V/mV
gain	$V_{OUT} = \pm 19.95V$	**80**			**50**			V/mV
	$V_S = \pm 20V$, $V_{OUT} = \pm 19.4V$	50	130		25	130		V/mV
	$I_{OUT} = \pm 20$ mA **(±15 mA)**	**20**			**15**			V/mV
	$V_S = \pm 0.6V$ **(0.65V)**, $I_{OUT} = \pm 2$ mA	1.5	3.0		1.0	3.0		V/mV
	$V_{OUT} = \pm 0.4V$ **(±0.3V)**, $V_{CM} = -0.4V$	**0.5**			**0.75**			V/mV
Shunt gain (note 6)	1.2V **(1.3V)** $\le V_{OUT} \le$ 40V, $R_L = 1.1$ kΩ	14	33		10	33		V/mV
	0.1 mA $\le I_{OUT} \le$ 5 mA	**6**			**6**			V/mV
	1.5V $\le V^+ \le$ 40V, $R_L = 250Ω$	8	25		6	25		V/mV
	0.1 mA $\le I_{OUT} \le$ 20 mA	**4**			**4**			V/mV
Common-mode	−20V $\le V_{CM} \le$ 19.15V **(19V)**	93	102		90	102		dB
rejection	$V_S = \pm 20V$	**87**			**87**			dB
Supply-voltage	−0.2V $\ge V^- \ge$ −39V	90	96		87	96		dB
rejection	$V^+ = 1.0V$ **(1.1V)**	**84**			**84**			dB
	1.0V **(1.1V)** $\le V^+ \le$ 39.8V	96	106		93	106		dB
	$V^- = -0.2V$	**90**			**90**			dB
Offset voltage drift			2.0			5.0		μV/°C
Offset current drift			2.0			5.0		pA/°C
Bias current drift	$T_C < 100°C$		60			90		pA/°C
Line regulation	1.2V **(1.3V)** $\le V_S \le$ 40V		0.001	0.003		0.001	0.008	%/V
	0 $\le I_{REF} \le$ 1.0 mA, V_{REF} = 200 mV			**0.006**			**0.01**	%/V
Load regulation	0 $\le I_{REF} \le$ 1.0 mA		0.01	0.1		0.01	0.15	%
	$V^+ - V_{REF} \ge$ 1.0V **(1.1V)**			**0.15**			**0.2**	%
Amplifier gain	0.2V $\le V_{REF} \le$ 35V	50	75		25	70		V/mV
		23			**15**			V/mV
Feedback sense		195	200	205	190	200	210	mV
voltage		**194**		**206**	**189**		**211**	mV
Feedback current			20	50		22	75	nA
				65			**90**	nA
Reference drift			0.002			0.003		%/°C
Supply current			270	400		300	500	μA
				500			**570**	μA
Supply current change	1.2V **(1.3V)** $\le V_S \le$ 40V		15	75		15	75	μA

Electrical Characteristics ($T_J = 25°C$, $\mathbf{T_{MIN} \leq T_J \leq T_{MAX}}$, note 4)

(Boldface type refers to limits over temperature range.)

PARAMETER	CONDITIONS	LM10BL MIN	LM10BL TYP	LM10BL MAX	LM10CL MIN	LM10CL TYP	LM10CL MAX	UNITS
Input offset voltage			0.3	2.0 **3.0**		0.5	4.0 **5.0**	mV mV
Input offset current (note 5)			0.1	0.7 **1.5**		0.2	2.0 **3.0**	nA nA
Input bias current			10	20 **30**		12	30 **40**	nA nA
Input resistance		250 **150**	500		150 **115**	400		kΩ kΩ
Large signal voltage gain	$V_S = \pm 3.25V$, $I_{OUT} = 0$ $V_{OUT} = \pm 3.2V$	60 **40**	300		40 **25**	300		V/mV V/mV
	$V_S = \pm 3.25V$, $I_{OUT} = 10$ mA $V_{OUT} = \pm 2.75V$	10 **4**	25		5 **3**	25		V/mV V/mV
	$V_S = \pm 0.6V$ **(0.65V)**, $I_{OUT} = \pm 2$ mA $V_{OUT} = \pm 0.4V$ **(±0.3V)**, $V_{CM} = -0.4V$	1.5 **0.5**	3.0		1.0 **0.75**	3.0		V/mV V/mV
Shunt gain (note 6)	$1.5V \leq V^+ \leq 6.5V$, $R_L = 500\Omega$ $0.1\text{ mA} \leq I_{OUT} \leq 10$ mA	8 **4**	30		6 **4**	30		V/mV V/mV
Common-mode rejection	$-3.25V \leq V_{CM} \leq 2.4V$ **(2.25V)** $V_S = \pm 3.25V$	89 **83**	102		80 **74**	102		dB dB
Supply-voltage rejection	$-0.2V \geq V^- \geq -5.4V$ $V^+ = 1.0V$ **(1.2V)**	86 **80**	96		80 **74**	96		dB dB
	$1.0V$ **(1.1V)** $\leq V^+ \leq 6.3V$ $V^- = 0.2V$	94 **88**	106		80 **74**	106		dB dB
Offset voltage drift			2.0			5.0		µV/°C
Offset current drift			2.0			5.0		pA/°C
Bias current drift			60			90		pA/°C
Line regulation	$1.2V$ **(1.3V)** $\leq V_S \leq 6.5V$ $0 \leq I_{REF} \leq 0.5$ mA, $V_{REF} = 200$ mV		0.001	0.01 **0.02**		0.001	0.02 **0.03**	%/V %/V
Load regulation	$0 \leq I_{REF} \leq 0.5$ mA $V^+ - V_{REF} \geq 1.0V$ **(1.1V)**		0.01	0.1 **0.15**		0.01	0.15 **0.2**	% %
Amplifier gain	$0.2V \leq V_{REF} \leq 5.5V$	30 **20**	70		20 **15**	70		V/mV V/mV
Feedback sense voltage		195 **194**	200	205 **206**	190 **189**	200	210 **211**	mV mV
Feedback current			20	50 **65**		22	75 **90**	nA nA
Reference drift			0.002			0.003		%/°C
Supply current			260	400 **500**		280	500 **570**	µA µA

Note 1: The input voltage can exceed the supply voltages provided that the voltage from the input to any other terminal does not exceed the maximum differential input voltage and excess dissipation is accounted for when $V_{IN} < V^-$.

Note 2: The maximum, operating-junction temperature is 150°C for the LM10, 100°C for the LM10B(L) and 85°C for the LM10C(L). At elevated temperatures, devices must be derated based on package thermal resistance.

Note 3: Internal thermal limiting prevents excessive heating that could result in sudden failure, but the IC can be subjected to accelerated stress with a shorted output and worst-case conditions.

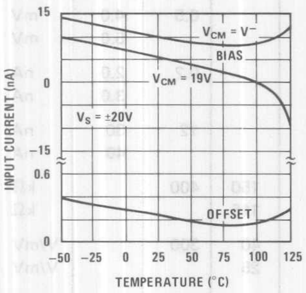
Note 4: These specifications apply for $V^- \leq V_{CM} \leq V^+ - 0.85V$ **(1.0V)**, $1.2V$ **(1.3V)** $< V_S \leq V_{MAX}$, $V_{REF} = 0.2V$ and $0 \leq I_{REF} \leq 1.0$ mA, unless otherwise specified: $V_{MAX} = 40V$ for the standard part and 6.5V for the low voltage part. Normal typeface indicates 25°C limits. **Boldface type indicates limits and altered test conditions for full-temperature-range operation**; this is −55°C to 125°C for the LM10, −25°C to 85°C for the LM10B(L) and 0°C to 70°C for the LM10C(L). The specifications do not include the effects of thermal gradients ($\tau_1 \cong 20$ ms), die heating ($\tau_2 \cong 0.2$s) or package heating. Gradient effects are small and tend to offset the electrical error (see curves).

Note 5: For $T_J > 90°C$, I_{OS} may exceed 1.5 nA for $V_{CM} = V^-$. With $T_J = 125°C$ and $V^- \leq V_{CM} \leq V^- + 0.1V$, $I_{OS} \leq 5$ nA.

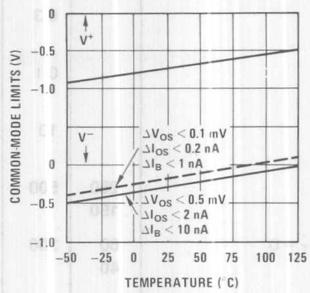
Note 6: This defines operation in floating applications such as the bootstrapped regulator or two-wire transmitter. Output is connected to the V^+ terminal of the IC and input common mode is referred to V^- (see typical applications). Effect of larger output-voltage swings with higher load resistance can be accounted for by adding the positive-supply rejection error.

Typical Performance Characteristics (Op Amp)

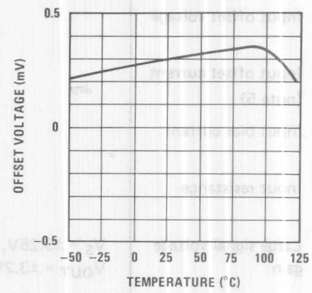
input current



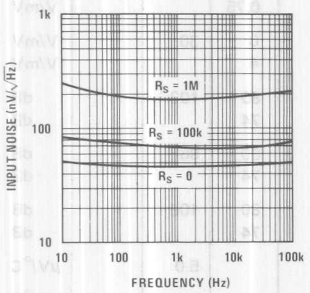
common mode limits



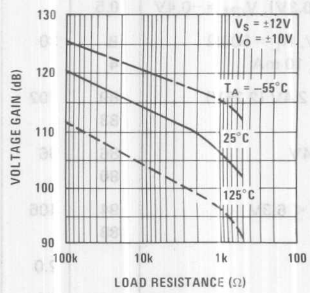
offset voltage drift



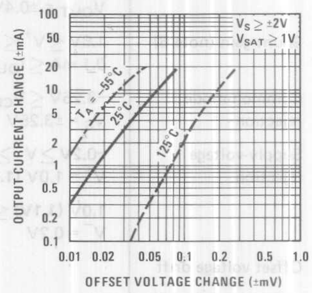
input noise voltage



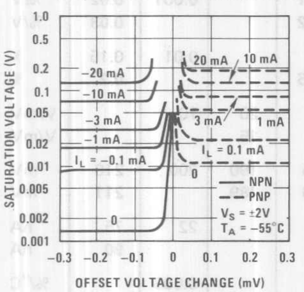
dc voltage gain



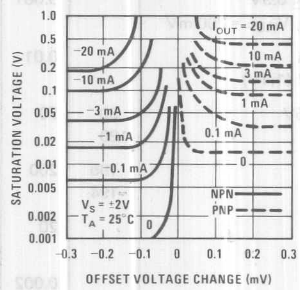
transconductance



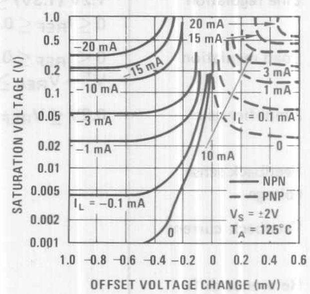
output saturation characteristics



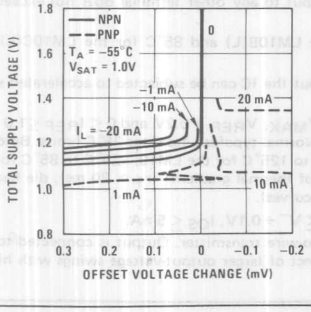
output saturation characteristics



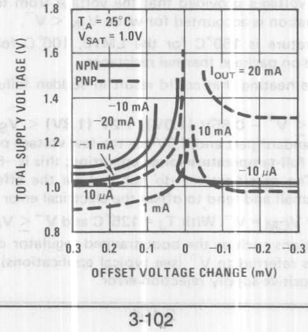
output saturation characteristics



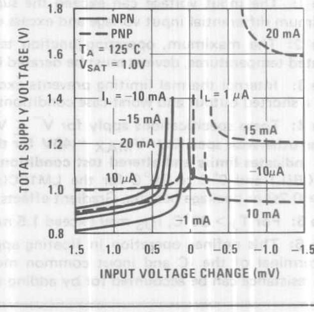
minimum supply voltage



minimum supply voltage

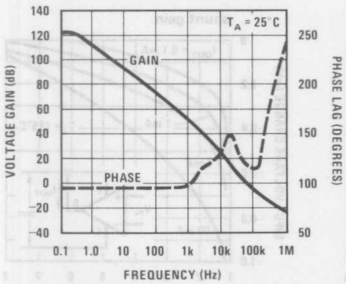


minimum supply voltage

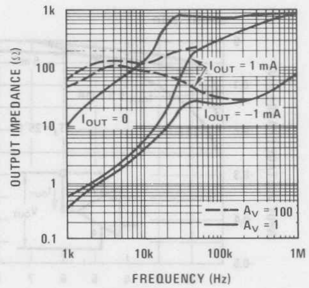


Typical Performance Characteristics (Op Amp)

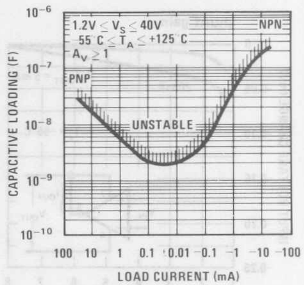
frequency response



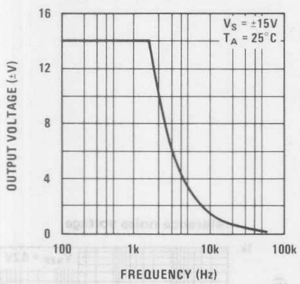
output impedance



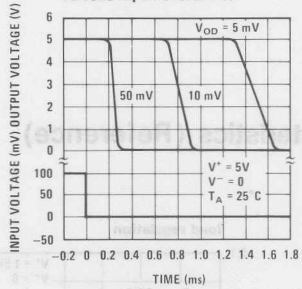
typical stability range



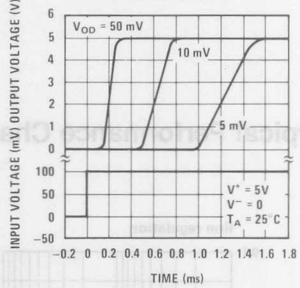
large signal response



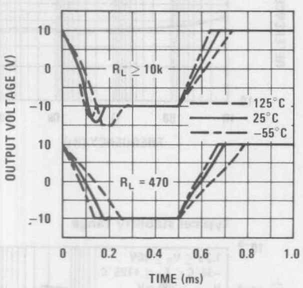
comparator response time for various input overdrives



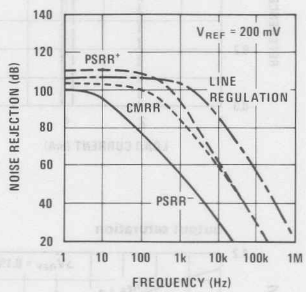
comparator response time for various input overdrives



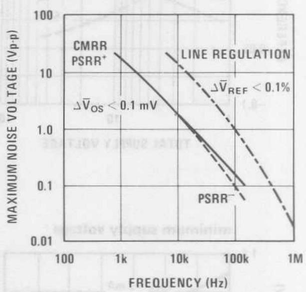
follower pulse response



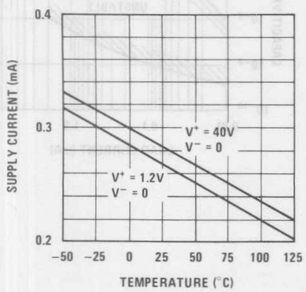
noise rejection



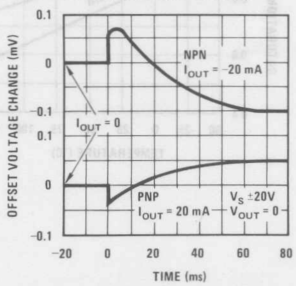
rejection slew limiting



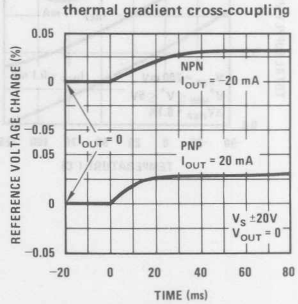
supply current



thermal gradient feedback

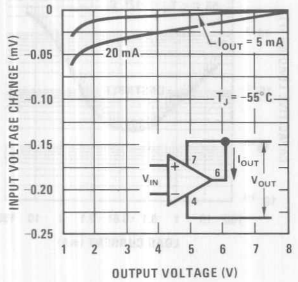


thermal gradient cross-coupling

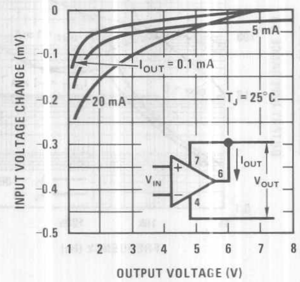


3

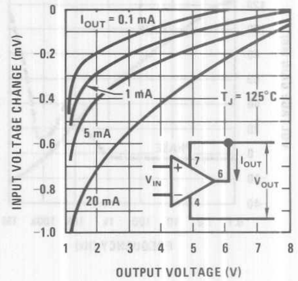
shunt gain



shunt gain

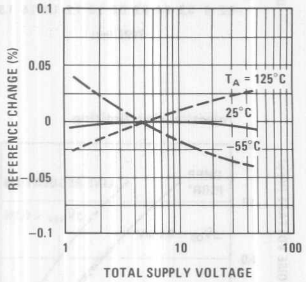


shunt gain

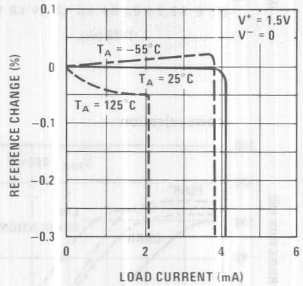


Typical Performance Characteristics (Reference)

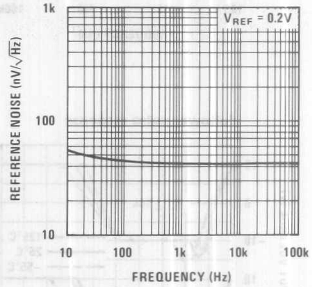
line regulation



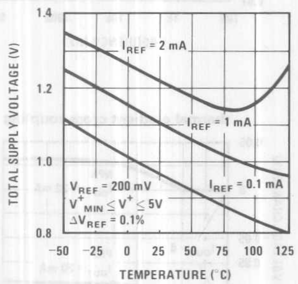
load regulation



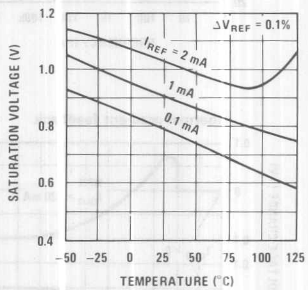
reference noise voltage



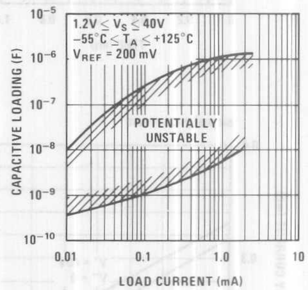
minimum supply voltage



output saturation



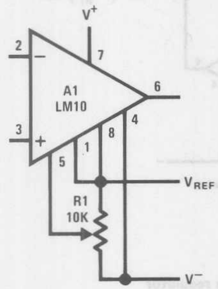
typical stability range



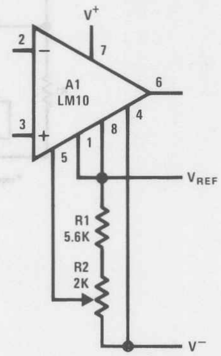
Typical Applications††

op amp offset adjustment

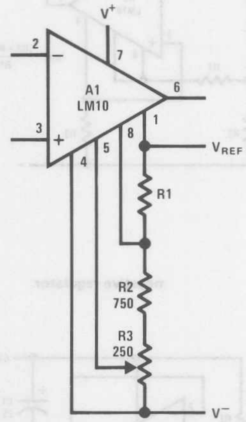
standard



limited range

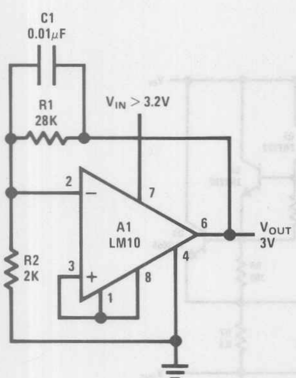


limited range with boosted reference

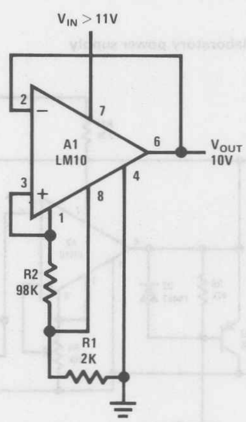


positive regulators†

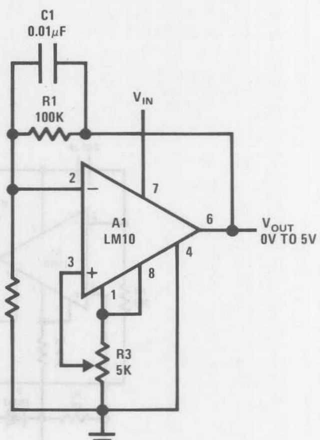
low voltage



best regulation



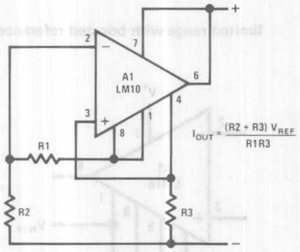
zero output



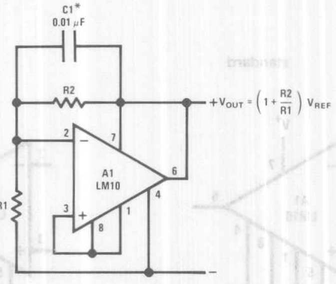
†Use only electrolytic output capacitors.
††Circuit descriptions available in application note AN-211.

Typical Applications ††

current regulator

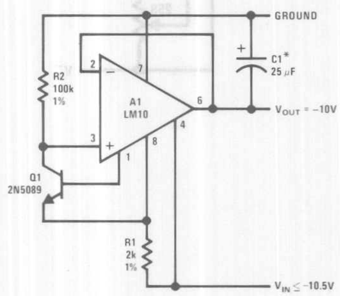


shunt regulator



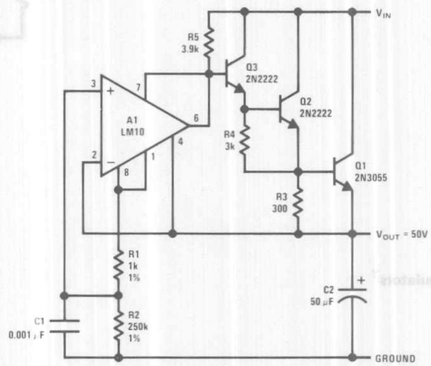
*required for capacitive loading

negative regulator

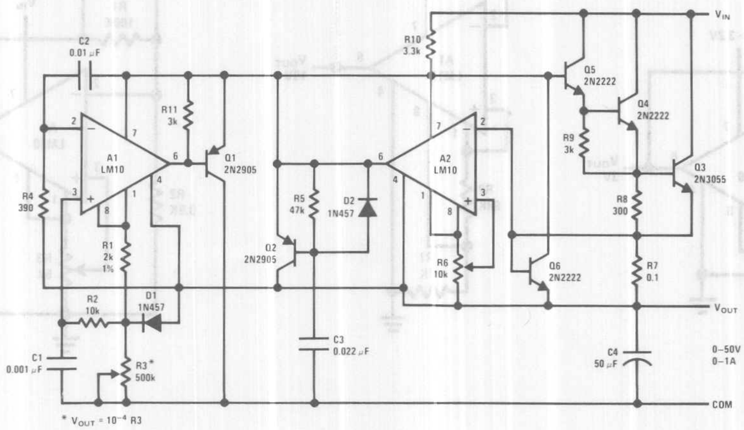


*electrolytic

precision regulator



laboratory power supply

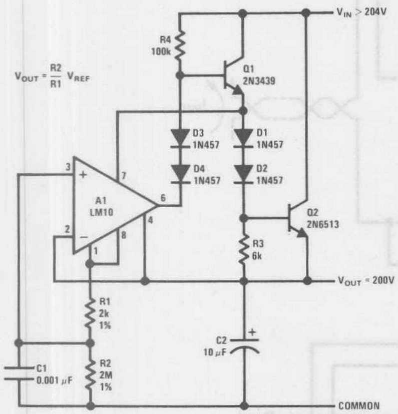


$* V_{OUT} = 10^{-4}\ R3$

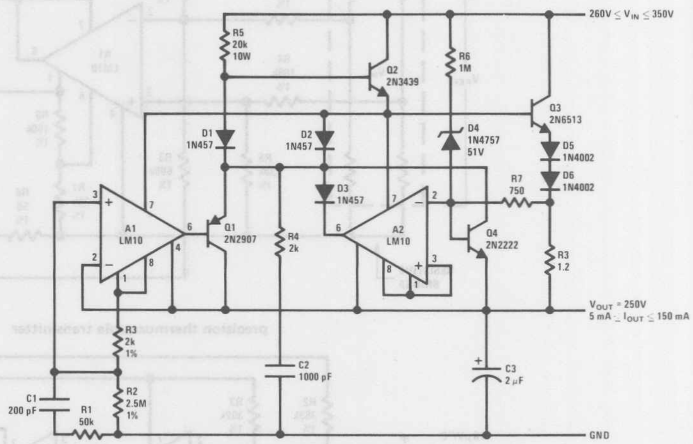
††Circuit descriptions available in application note AN-211.

Typical Applications ††

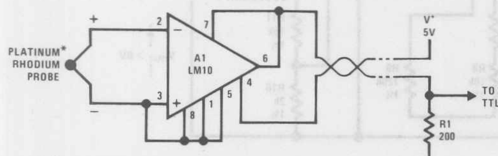
hv regulator



protected hv regulator

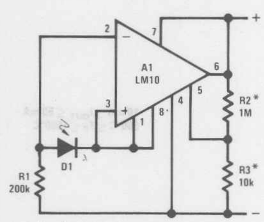


flame detector



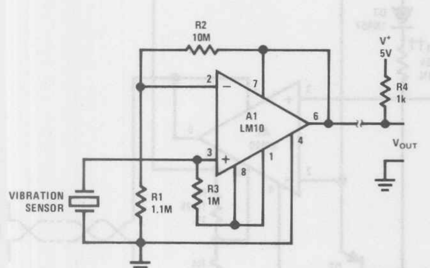
*800°C threshold is established by connecting balance to V_{REF}.

light level sensor

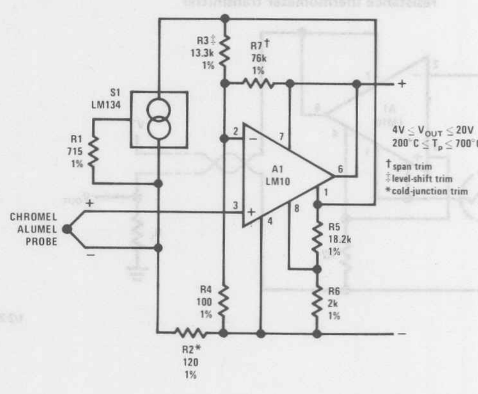


* provides hysteresis

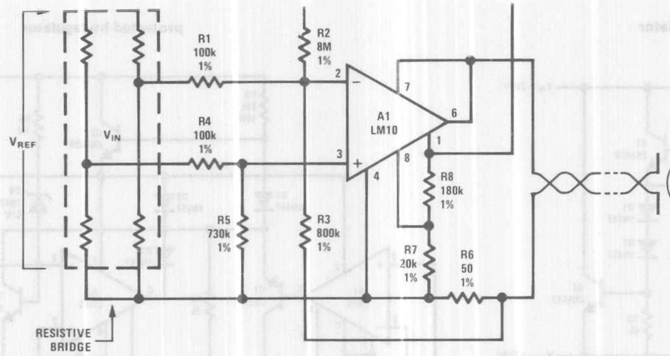
remote amplifier



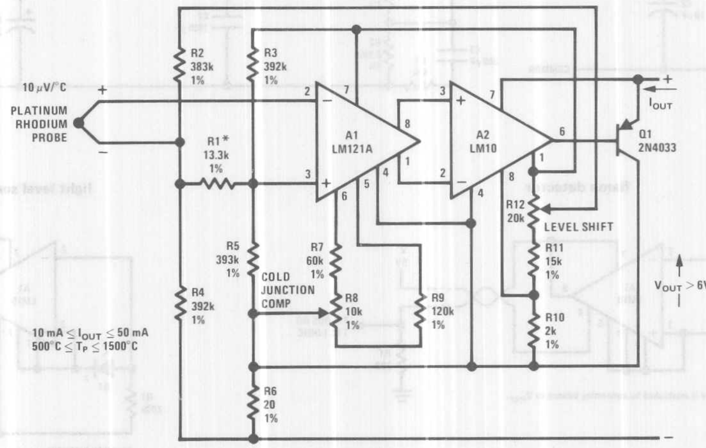
remote thermocouple amplifier



††Circuit descriptions available in application note AN-211.

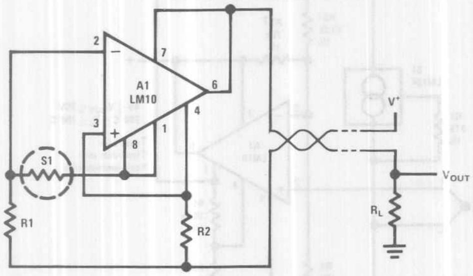


precision thermocouple transmitter

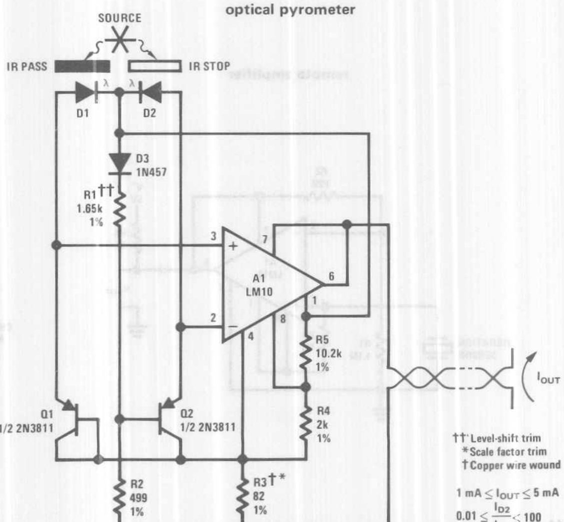


*gain trim

resistance thermometer transmitter



optical pyrometer



††Level-shift trim
*Scale factor trim
†Copper wire wound

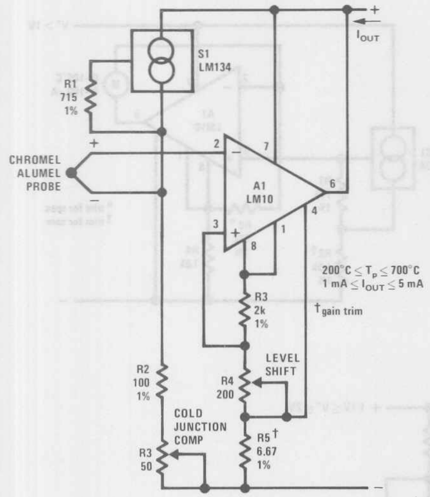
$1\ mA \leq I_{OUT} \leq 5\ mA$

$0.01 \leq \frac{I_{D2}}{I_{D1}} \leq 100$

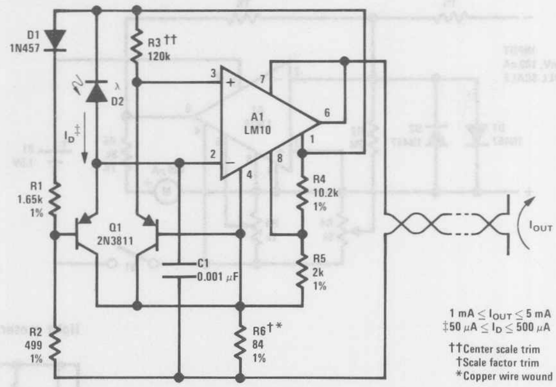
††Circuit descriptions available in application note AN-211.

Typical Applications ††

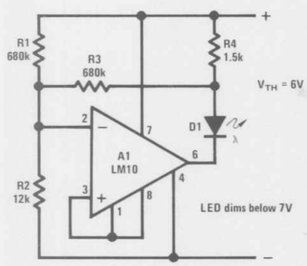
thermocouple transmitter



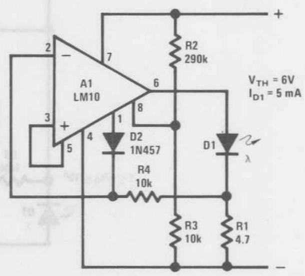
logarithmic light sensor



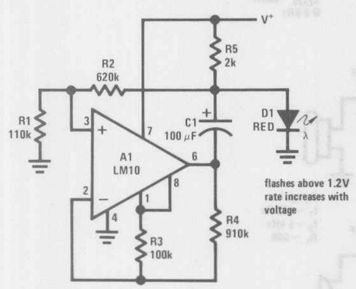
battery-level indicator



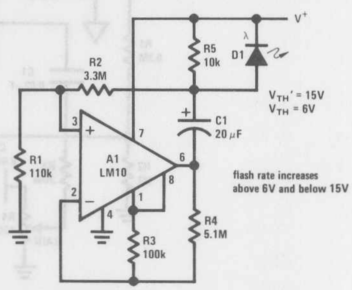
battery-threshold indicator



single-cell voltage monitor



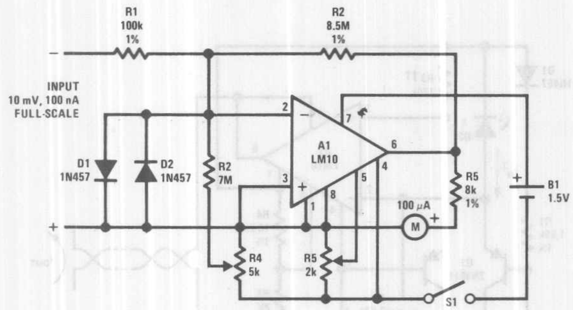
double-ended voltage monitor



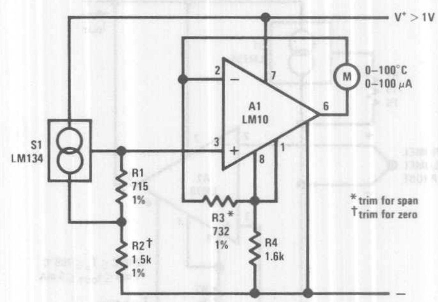
††Circuit descriptions available in application note AN-211.

Typical Applications ††

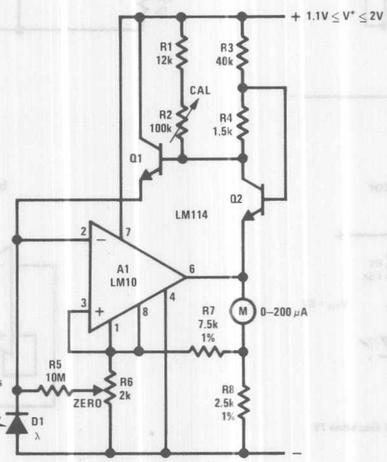
meter amplifier



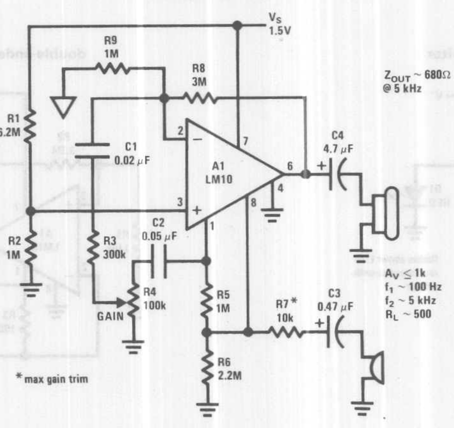
thermometer



light meter



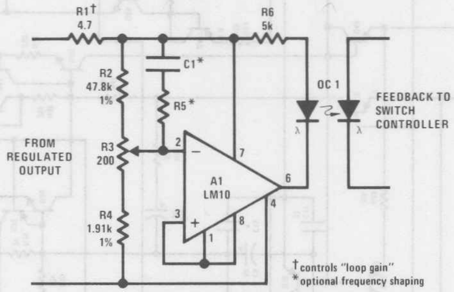
microphone amplifier



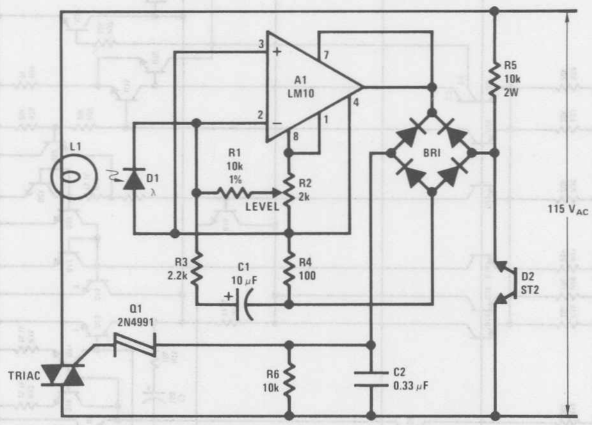
††Circuit descriptions available in application note AN-211.

Typical Applications ††

isolated voltage sensor



light-level controller

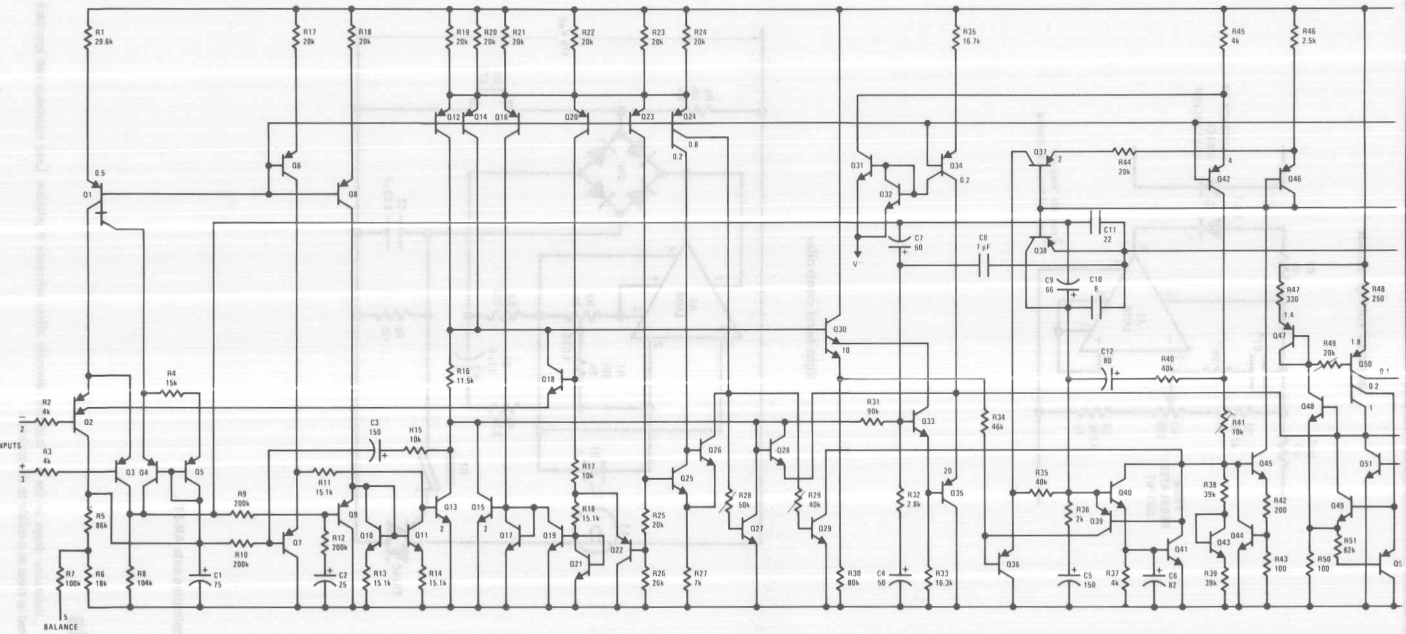


††Circuit descriptions available in application note AN-211.

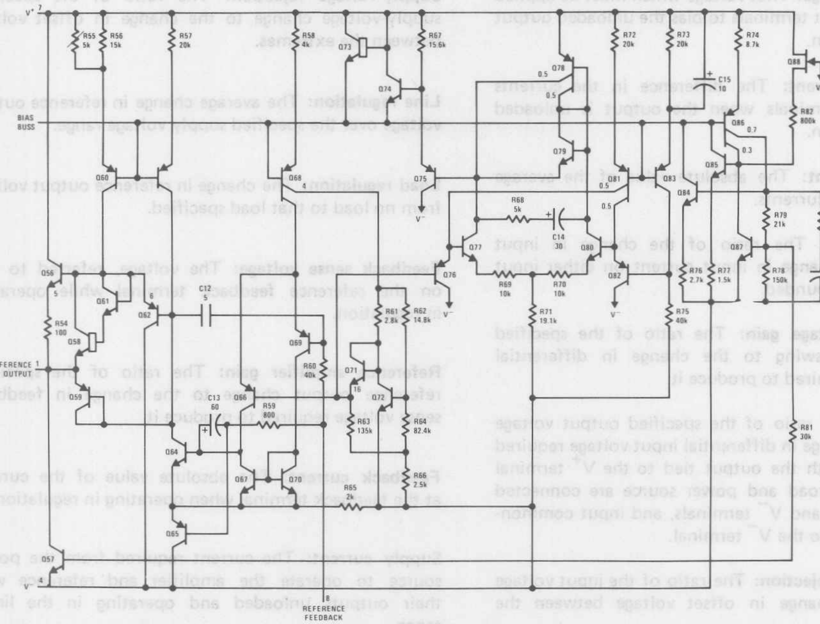
Application Hints

With heavy amplifier loading to V⁻, resistance drops in the V⁻ lead can adversely affect reference regulation. Lead resistance can approach 1Ω. Therefore, the common to the reference circuitry should be connected as close as possible to the package.

Operational Amplifier Schematic



Reference and Internal Regulator



LM10/LM10B(L)/LM10C(L)

3

Definition of Terms

Input offset voltage: That voltage which must be applied between the input terminals to bias the unloaded output in the linear region.

Input offset current: The difference in the currents at the input terminals when the output is unloaded in the linear region.

Input bias current: The absolute value of the average of the two input currents.

Input resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Large signal voltage gain: The ratio of the specified output voltage swing to the change in differential input voltage required to produce it.

Shunt gain: The ratio of the specified output voltage swing to the change in differential input voltage required to produce it with the output tied to the V^+ terminal of the IC. The load and power source are connected between the V^+ and V^- terminals, and input common-mode is referred to the V^- terminal.

Common-mode rejection: The ratio of the input voltage range to the change in offset voltage between the extremes.

Supply-voltage rejection: The ratio of the specified supply-voltage change to the change in offset voltage between the extremes.

Line regulation: The average change in reference output voltage over the specified supply voltage range.

Load regulation: The change in reference output voltage from no load to that load specified.

Feedback sense voltage: The voltage, referred to V^-, on the reference feedback terminal while operating in regulation.

Reference amplifier gain: The ratio of the specified reference output change to the change in feedback sense voltage required to produce it.

Feedback current: The absolute value of the current at the feedback terminal when operating in regulation.

Supply current: The current required from the power source to operate the amplifier and reference with their outputs unloaded and operating in the linear range.

National Semiconductor

Operational Amplifiers/Buffers

LM11/LM11C/LM11CL Operational Amplifiers

General Description

The LM11 is a precision dc amplifier combining the best features of existing bipolar and FET op amps. It is similar to the LM108A, except that input currents have been reduced by more than a factor of ten. Offset voltage and drift have also been improved.

Compared to FETs, the device provides inherently lower offset voltage and offset voltage drift, along with at least an order of magnitude better long-term stability. Low frequency noise is also somewhat reduced. Bias current is significantly lower even under laboratory conditions, and its low drift makes compensation practical. Offset current is almost unmeasureable. Although not as fast as FETs, it does have a much lower power drain. This low dissipation has the added advantage of eliminating warm up time in critical applications.

Typical characteristics for 25°C (**−55°C** to **125°C**) are:

- offset voltage: 100 μV (**200 μV**)
- bias current: 25 pA (**65 pA**)
- offset current: 0.5 pA (**3 pA**)
- temperature drift: **1 μV/°C**
- long-term stability: 10 μV/year

The LM11 is internally compensated, but external compensation can be added for improved frequency stability, particularly with capacitive loads. Offset voltage balancing is also provided, with the balance range determined by a low-resistance potentiometer.

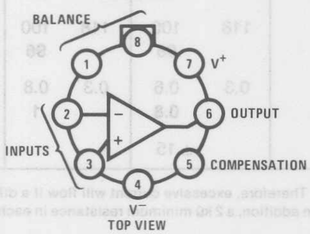
Otherwise, the device is the electrical equivalent of the LM108, except that the negative common-mode limit is 0.6V less, performance is specified down to ± 2.5V and the guaranteed output drive has been increased to ± 2 mA. The input noise is somewhat higher, but amplifier noise is obscured by resistor noise with higher source resistances.

This monolithic IC has obvious applications as electrometer amplifiers, charge integrators, analog memories, low frequency active filters or for frequency shaping in slow servo loops. It can be substituted for existing circuits to provide improved performance or eliminate trimming operations. The greater precision can also be used to extend the dynamic range of logarithmic amplifiers, light meters and solid-state particle detectors.

The LM11 is manufactured with standard bipolar processing using super-gain transistors.

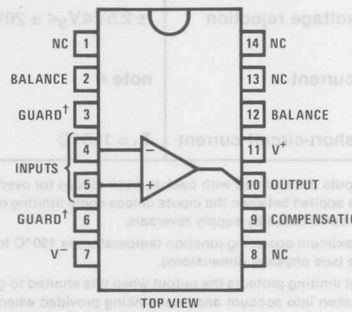
Connection Diagrams

metal can*



Order Number LM11H, LM11CH, or LM11CLH
See NS Package H08C

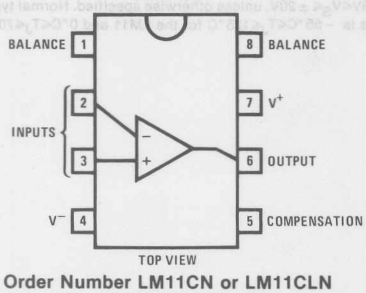
dual-in-line package



Order Number LM11D, LM11CD, or LM11CLD
See NS Package D14E

Order Number LM11CN-14 or LM11CLN-14
See NS Package N14A

mini-DIP



Order Number LM11CN or LM11CLN
See NS Package N08B

* case connected to V−

† guard pins have no internal connection

pin connections shown on schematic diagram and for typical applications are for metal can or mini-DIP.

power dissipation (note 2)	500 mW
output short-circuit duration (note 3)	indefinite
storage temperature range	$-65\,°C$ to $150\,°C$
lead temperature (soldering, 10 seconds)	$300\,°C$

Electrical Characteristics ($T_J = 25\,°C$, $T_{MIN} \leqslant T_J \leqslant T_{MAX}$, note 4)

(Boldface type refers to limits over temperature range.)

parameter	conditions	LM11 typ	LM11 lim	LM11C typ	LM11C lim	LM11CL typ	LM11CL lim	units
input offset voltage	**note 4**	0.1	0.3	0.2	0.6	0.5	5	mV
			0.6		**0.8**		**6**	mV
input offset current	**note 4**	0.5	10	1	10	4	25	pA
			30		**20**		**50**	pA
input bias current	**note 4**	25	50	40	100	70	200	pA
			150		**150**		**300**	pA
input resistance	**note 4**	10^{11}		10^{11}		10^{11}		Ω
offset voltage drift	**note 4**	1	3	2	5	3		μV/°C
offset current drift	$T_{MIN} \leqslant T_J \leqslant T_{MAX}$	20		10		50		fA/°C
bias current drift	$T_{MIN} \leqslant T_J \leqslant T_{MAX}$	0.5	**1.5**	0.8	**3**	1.4		pA/°C
large signal voltage gain	$V_S \pm 15V$, $I_{OUT} = \pm 2$ mA	300	100	300	100	300	25	V/mV
	$V_{OUT} = \pm 12V$ (**±11.5V**)		**50**		**50**		**15**	V/mV
	$V_S = \pm 15V$, $I_{OUT} = \pm 0.5$ mA	1200	250	1200	250	800	50	V/mV
	$V_{OUT} \pm 12V$		**100**		**100**		**30**	V/mV
common-mode rejection	$-13V$ (**−12.5V**)$\leqslant V_{CM} \leqslant 14V$	130	110	130	110	110	96	dB
	$V_S = \pm 15V$		**100**		**100**		**90**	dB
supply-voltage rejection	$\pm 2.5V \leqslant V_S \leqslant \pm 20V$	118	100	118	100	100	84	dB
			96		**96**		**80**	dB
supply current	**note 4**	0.3	0.6	0.3	0.8	0.3	0.8	mA
			0.8		**1**		**1**	mA
output short-circuit current	$T_J = 150\,°C$		±15					mA

note 1: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used. In addition, a 2 kΩ minimum resistance in each input is advised to avoid possible latch up initiated by supply reversals.

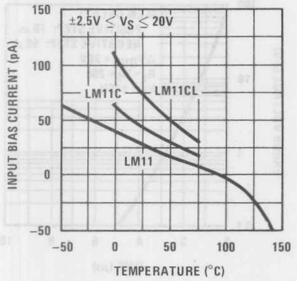
note 2: The maximum operating-junction temperature is 150 °C for the LM11 and 85 °C for the LM11C(L). Devices must be derated based on package thermal resistance (see physical dimensions).

note 3: Current limiting protects the output when it is shorted to ground or any voltage less than the supplies. With continuous overloads, package dissipation must be taken into account and heat sinking provided when necessary.

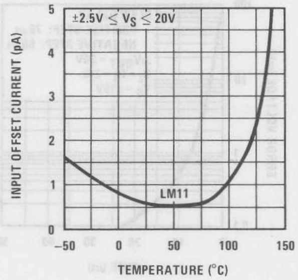
note 4: These specifications apply for $V^- + 2V$ (**2.5V**)$\leqslant V_{CM} \leqslant V^+ - 1V$ and $\pm 2.5V \leqslant V_S \leqslant \pm 20V$, unless otherwise specified. Normal typeface indicates 25 °C limits. **Boldface type indicates limits for full-temperature range operation.** This is $-55\,°C \leqslant T_J \leqslant 125\,°C$ for the LM11 and $0\,°C \leqslant T_J \leqslant 70\,°C$ for the LM11C(L).

Typical Characteristics

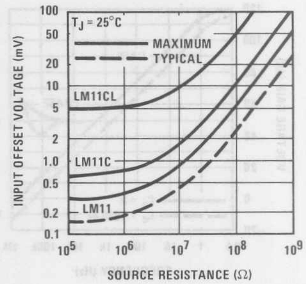
input bias current



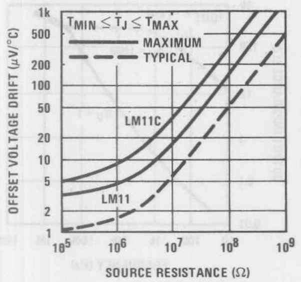
input offset current



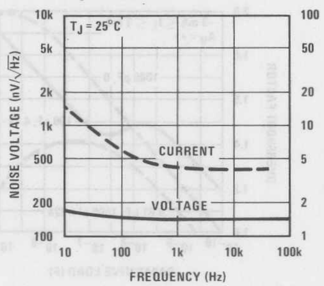
offset: single source resistor (unbalanced)



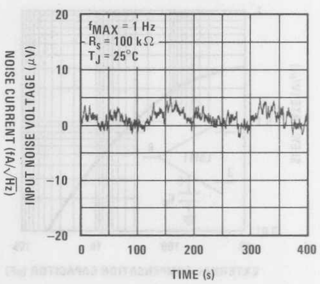
drift: single source resistor (unbalanced)



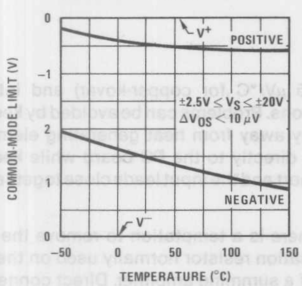
input noise



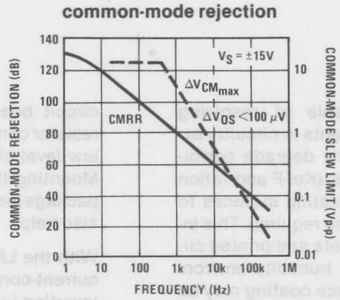
input noise



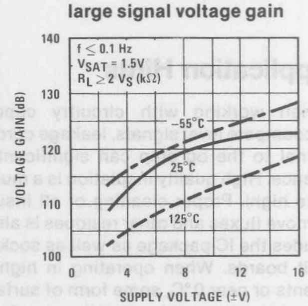
common-mode limits



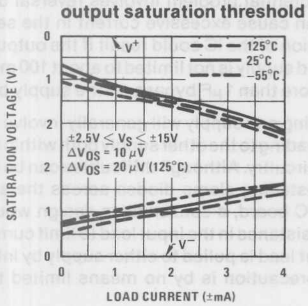
common-mode rejection



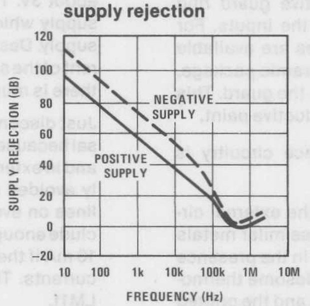
large signal voltage gain



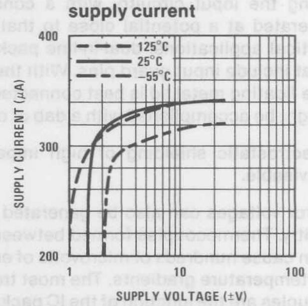
output saturation threshold



supply rejection

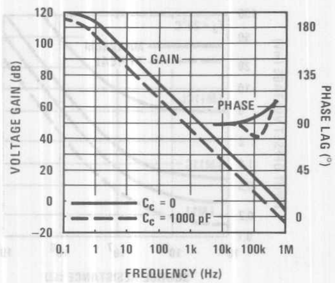


supply current

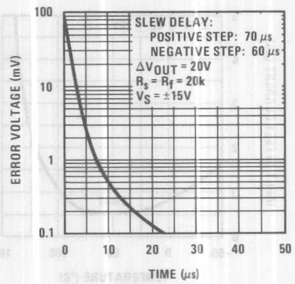


Typical Characteristics (Continued)

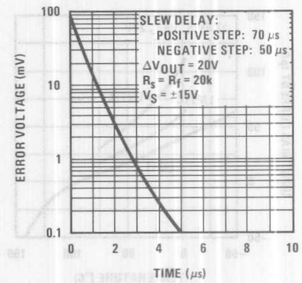
open loop response



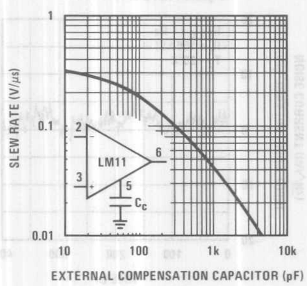
follower final settling time



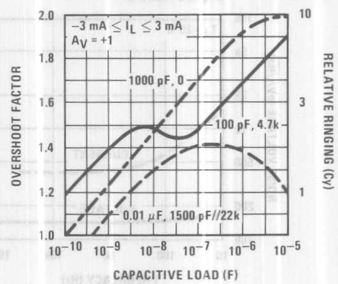
inverter final settling time



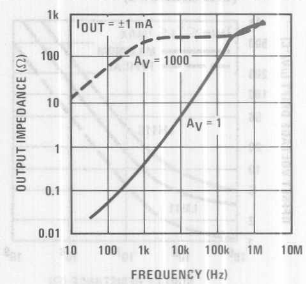
slew rate



stability with over-compensation



closed loop output impedance



Application Hints

When working with circuitry capable of resolving picoampere level signals, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation is a must (Kel-F and Teflon rate high). Proper cleaning of all insulating surfaces to remove fluxes and other residues is also required. This includes the IC package as well as sockets and printed circuit boards. When operating in high humidity environments or near 0 °C, some form of surface coating may be necessary to provide a moisture barrier.

The effects of board leakage can be minimized by encircling the input circuitry with a conductive guard ring operated at a potential close to that of the inputs. For critical applications, dual-in-line packages are available that include input guard pins. With the ceramic package, the floating metal lid is best connected to the guard. This might be accomplished with a dab of conductive paint.

Electrostatic shielding of high impedance circuitry is advisable.

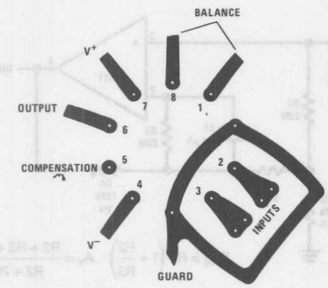
Error voltages can also be generated in the external circuitry. Thermocouples formed between dissimilar metals can cause hundreds of microvolts of error in the presence of temperature gradients. The most troublesome thermocouples are the junction of the IC package and the printed circuit board (35 μV/°C for copper-kovar) and internal resistor connections. Problems can be avoided by keeping low level circuitry away from heat generating elements. Mounting the IC directly to the PC board while keeping package leads short and the input leads close together can also help.

With the LM11 there is a temptation to remove the bias-current-compensation resistor normally used on the non-inverting input of a summing amplifier. Direct connection of the inputs to ground or a low-impedance voltage source is not recommended with supply voltages greater than about 3V. The potential problem involves reversal of one supply which can cause excessive current in the second supply. Destruction of the IC could result if the output current of the second supply is not limited to about 100 mA or if there is much more than 1 μF bypass on the supply buss.

Just disconnecting one supply will generally involve reversal because of loading to the other supply both within the IC and in external circuitry. Although difficulties can be largely avoided by installing clamp diodes across the supply lines on every PC board, a conservative design would include enough resistance in the input lead to limit current to 10 mA if the input lead is pulled to either supply by internal currents. This precaution is by no means limited to the LM11.

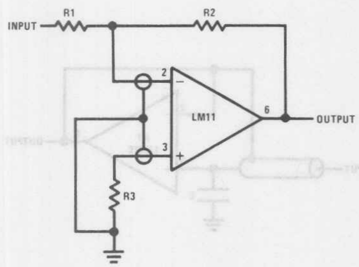
input guarding

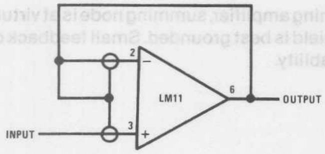
Input guarding can drastically reduce surface leakage. Layout for metal can is shown here. Guarding both sides of board is required. Bulk leakage reduction is less and depends on guard ring width.

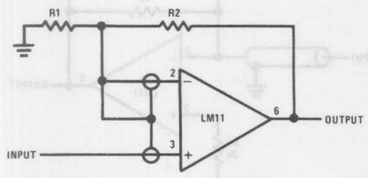


BOTTOM VIEW

Guard ring is connected to low impedance point at same potential as sensitive input leads. Connections for various op amp configurations are shown here.

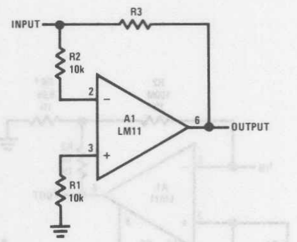




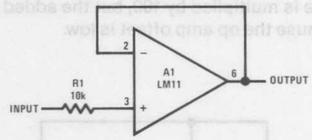


input protection

Current is limited by R2 even when input is connected to voltage source outside common mode range. If one supply reverses, current is controlled by R1. These resistors do not affect normal operation.

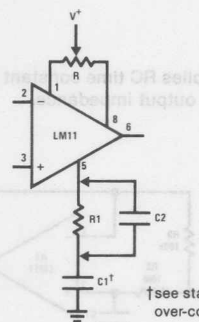


Input resistor controls current when input exceeds supply voltages, when power for op amp is turned off or when output is shorted.



balancing and over-compensation

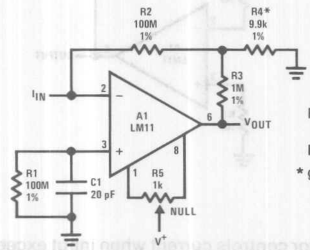
Over-compensation will improve stability with capacitive loading (see curves). Offset voltage adjustment range is determined by balance potentiometer resistance as indicated in the table.



†see stability with over-compensation curve

min. adj range	R
±5 mV	100 kΩ
±2	10k
±1	3k
±0.8	3k
±0.4	1k

Equivalent feedback resistance is 10 GΩ, but only standard resistors are used. Even though the offset voltage is multiplied by 100, output offset is actually reduced because error is dependent on offset current rather than bias current. Voltage on summing junction is less than 5 mV.

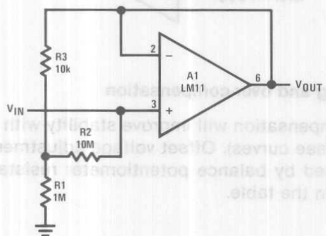


$$R_f = R2\left(1 + \frac{R3}{R4}\right)$$

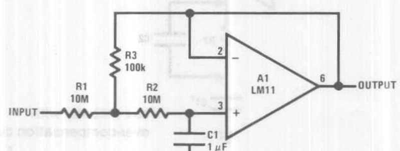
$R2 >> R3 \,/\!/\, R4$

* gain trim

Follower input resistance is 1 GΩ. With the input open, offset voltage is multiplied by 100, but the added error is not great because the op amp offset is low.



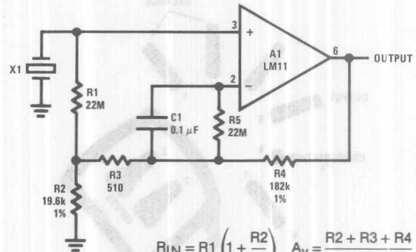
This circuit multiplies RC time constant to 1000 seconds and provides low output impedance.



$$\tau = \frac{R1\,C}{R3}(R2 + R3)$$

$$\Delta V_{OUT} = \frac{R1 + R3}{R3}(I_B\,R2 + V_{OS})$$

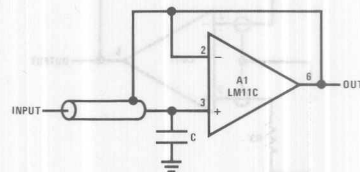
A high-input-impedance ac amplifier for a piezoelectric transducer. Input resistance of 880 MΩ and gain of 10 is obtained.



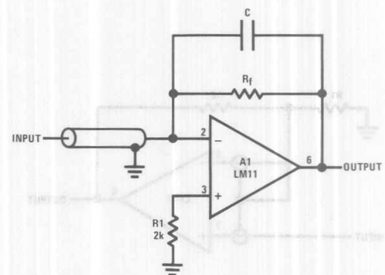
$$R_{IN} = R1\left(1 + \frac{R2}{R3}\right) \qquad A_V = \frac{R2 + R3 + R4}{R2 + R3}$$

cable bootstrapping

Bootstrapping input shield for a follower reduces cable capacitance, leakage and spurious voltages from cable flexing. Instability can be avoided with small capacitor on input.



With summing amplifier, summing node is at virtual ground so input shield is best grounded. Small feedback capacitor insures stability.

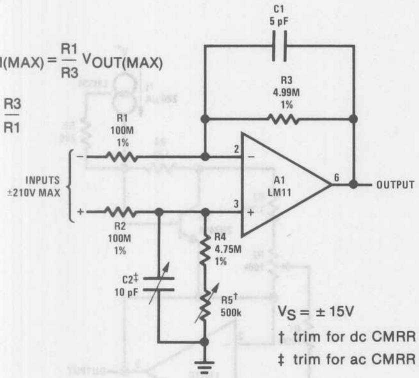


differential amplifiers

This differential amplifier handles high input voltages. Resistor mismatches and stray capacitors should be balanced out for best common-mode rejection.

$$V_{CM(MAX)} = \frac{R1}{R3} V_{OUT(MAX)}$$

$$A_V = \frac{R3}{R1}$$

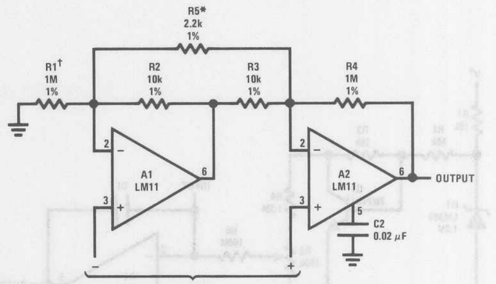


$V_S = \pm 15V$

† trim for dc CMRR

‡ trim for ac CMRR

Two op-amp instrumentation amplifier has poor ac common mode rejection. This can be improved at the expense of differential bandwidth with C2.

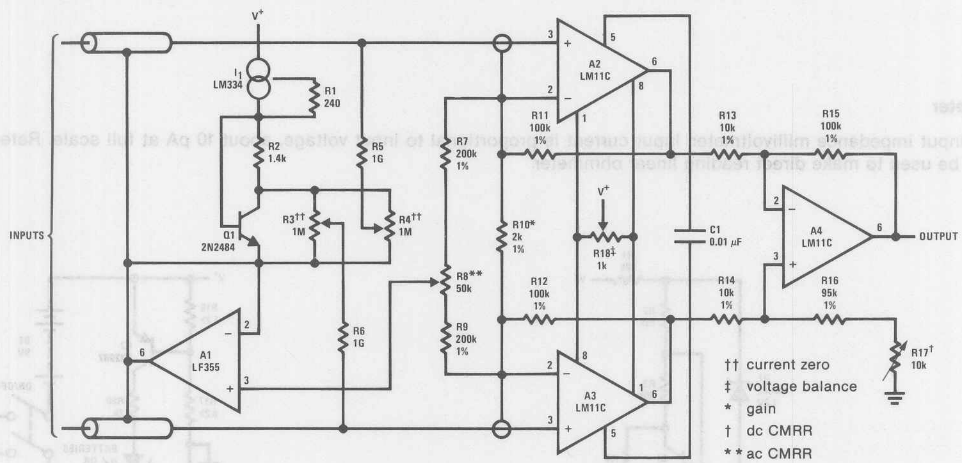


* gain set

† trim for dc CMRR

$f_o = 10$ Hz

High gain differential instrumentation amplifier includes input guarding, cable bootstrapping and bias current compensation. Differential bandwidth is reduced by C1 which also makes common-mode rejection less dependent on matching of input amplifiers.



†† current zero

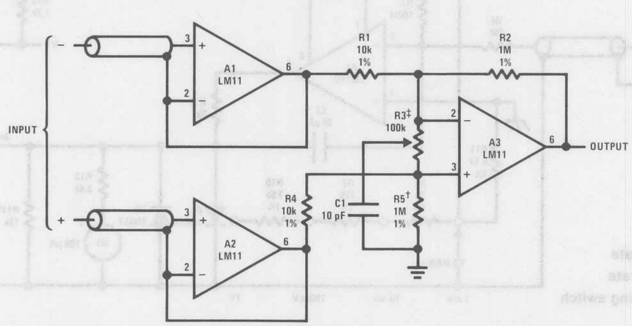
‡ voltage balance

* gain

† dc CMRR

** ac CMRR

For moderate-gain instrumentation amplifiers, input amplifiers can be connected as followers. This simplifies circuitry, but A3 must also have low drift.



R1 = R3; R2 = R4

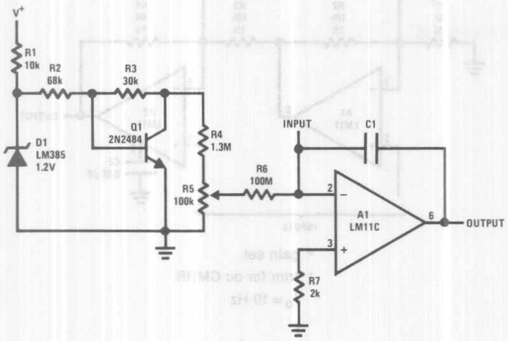
$$A_V = \frac{R2}{R1}$$

†trim for dc CMRR

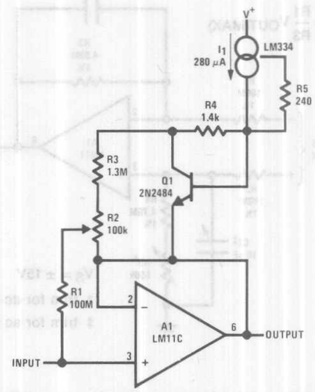
‡set for ac CMRR

bias current compensation

Precise bias current compensation for use with unregulated supplies. Reference voltage is available for other circuitry.

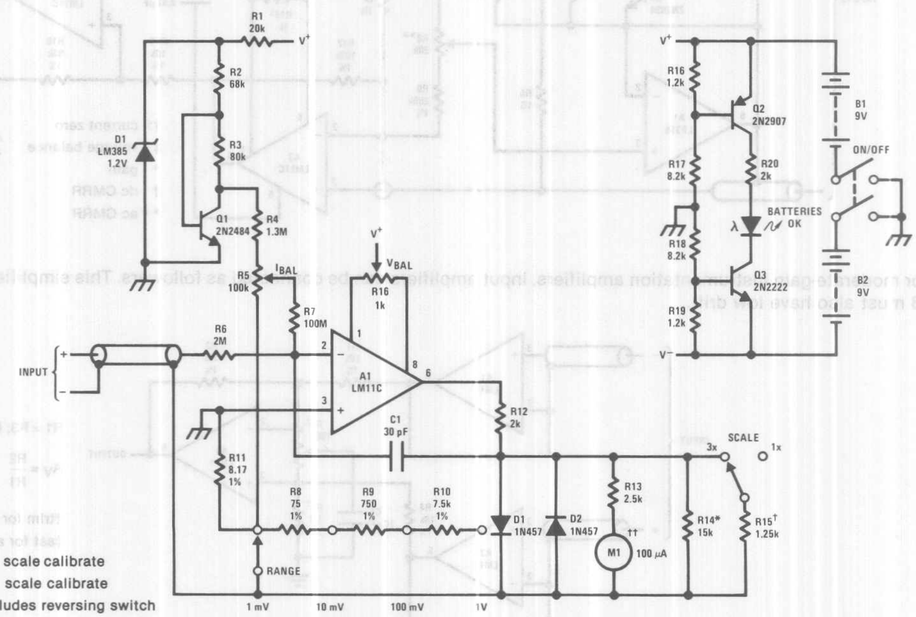


This circuit shows how bias current compensation can be used on a voltage follower.



voltmeter

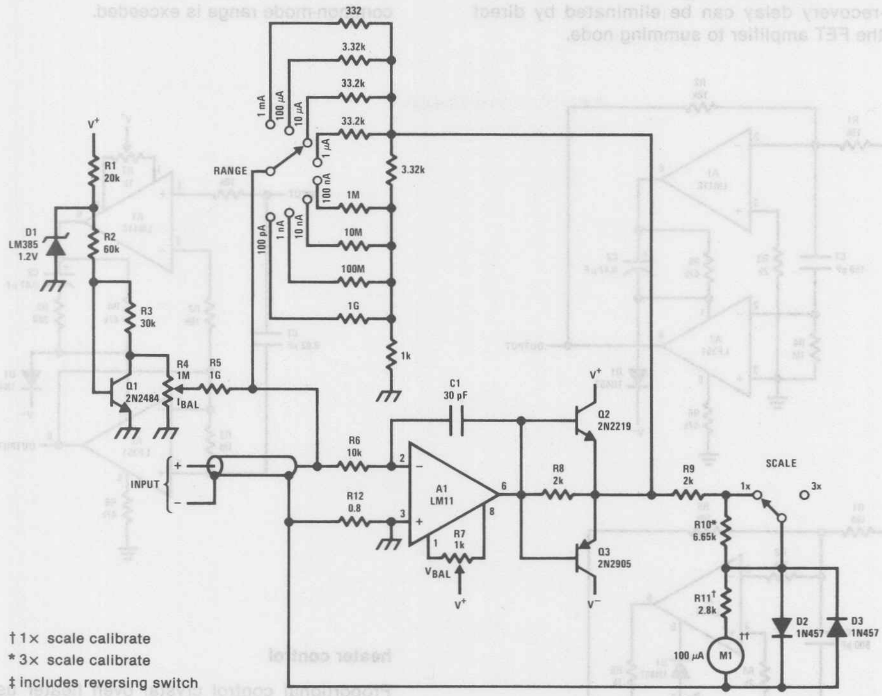
High input impedance millivoltmeter. Input current is proportional to input voltage, about 10 pA at full scale. Reference could be used to make direct reading linear ohmmeter.



* 1× scale calibrate
† 3× scale calibrate
‡ includes reversing switch

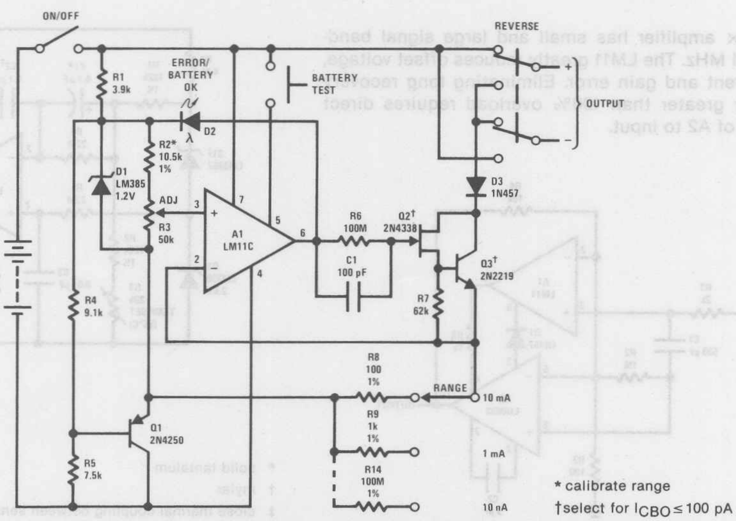
ammeter

Current meter ranges from 100 pA to 3 mA full scale. Voltage across input is 100 μV at lower ranges rising to 3 mV at 3 mA. Buffers on op amp are to remove ambiguity with high-current overload. Output can also drive DVM or DPM.

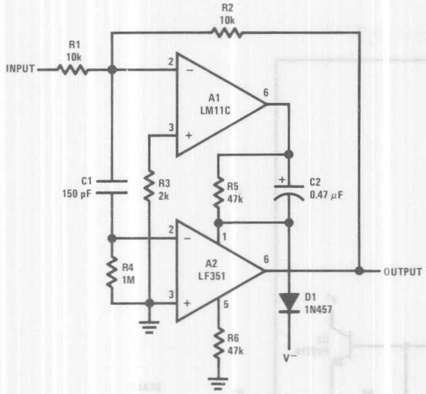


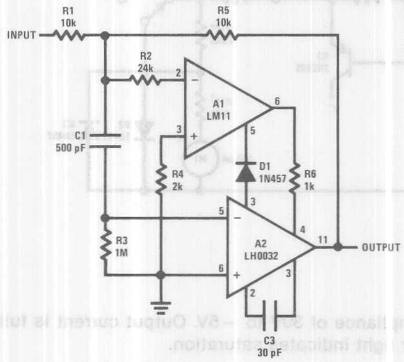
current source

Precision current source has 10 μA to 10 mA ranges with output compliance of 30V to −5V. Output current is fully adjustable on each range with a calibrated, ten-turn potentiometer. Error light indicates saturation.

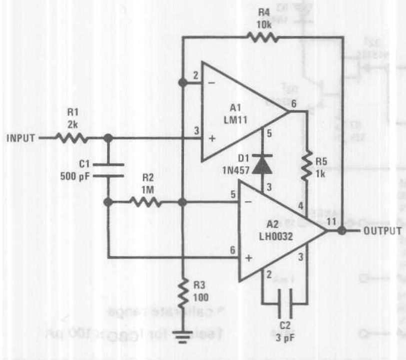


LM11 along with speed of the FET op amps. Open loop gain is about 140 dB and settling time to 1 mV about 8 μs. Overload-recovery delay can be eliminated by direct coupling the FET amplifier to summing node.

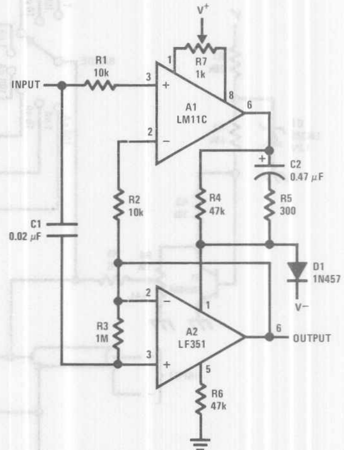




This 100× amplifier has small and large signal bandwidth of 1 MHz. The LM11 greatly reduces offset voltage, bias current and gain error. Eliminating long recovery delay for greater than 100% overload requires direct coupling of A2 to input.

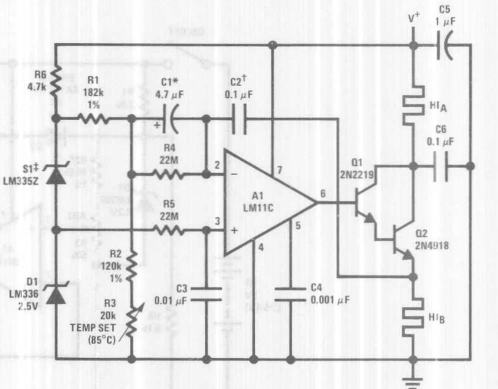


frequency should not exceed 10 kHz if the FET amplifier is ac coupled to input. The circuit does not behave well if common-mode range is exceeded.



heater control

Proportional control crystal oven heater uses lead/lag compensation for fast settling. Time constant is changed with R4 and compensating resistor R5. If Q2 is inside oven, a regulated supply is recommended for 0.1°C control.



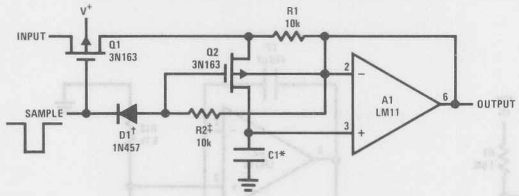
* solid tantalum

† mylar

‡ close thermal coupling between sensor and oven shell is recommended.

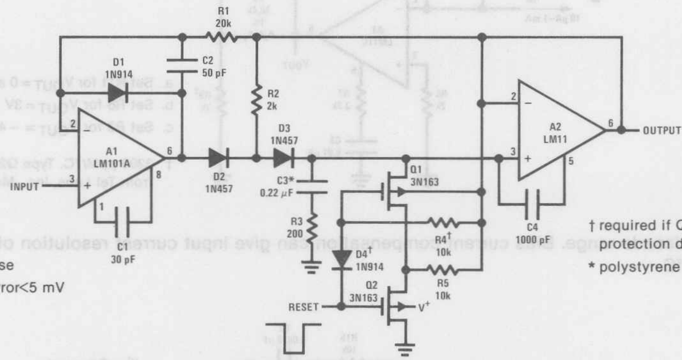
leakage isolation

Switch leakage in this sample and hold does not reach storage capacitor.



* polystyrene or Telfon
†required if protected-gate switch is used

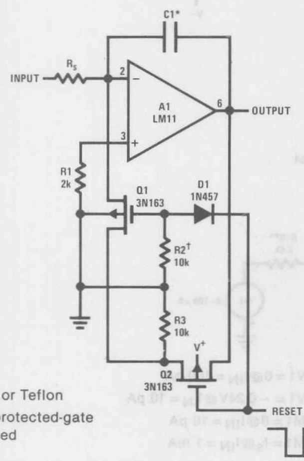
A peak detector designed for extended hold. Leakage currents of peak-detecting diodes and reset switch are absorbed before reaching storage capacitor.



300 μs min single pulse
200 μs min repetitive pulse
300 Hz max sine wave error<5 mV

† required if Q1 has gate-protection diode
* polystyrene or Teflon

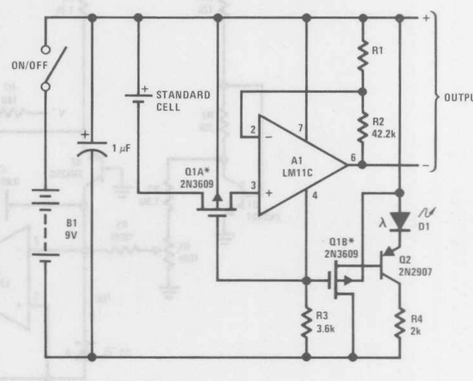
Reset is provided for this integrater and switch leakage is isolated from the summing junction. Greater precision can be provided if bias-current compensation is included.



* polystyrene or Teflon
† required if protected-gate switch is used

standard-cell buffer

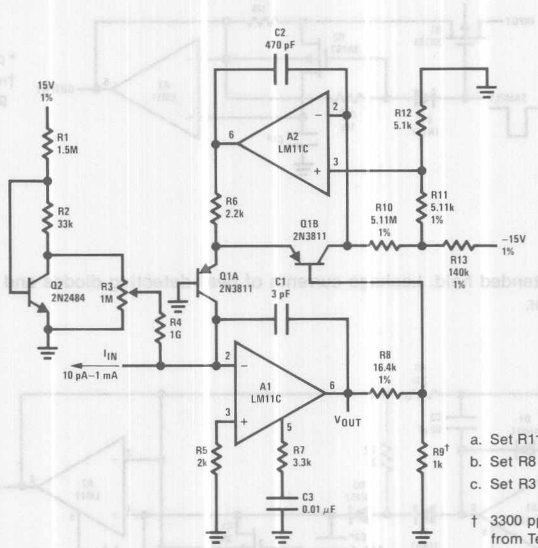
Battery powered buffer amplifier for standard cell has negligible loading and disconnects cell for low supply voltage or overload on output. Indicator diode extinguishes as disconnect circuitry is activated.



* cannot have gate protection diode; $V_{TH} > V_{OUT}$

logarithmic amplifiers

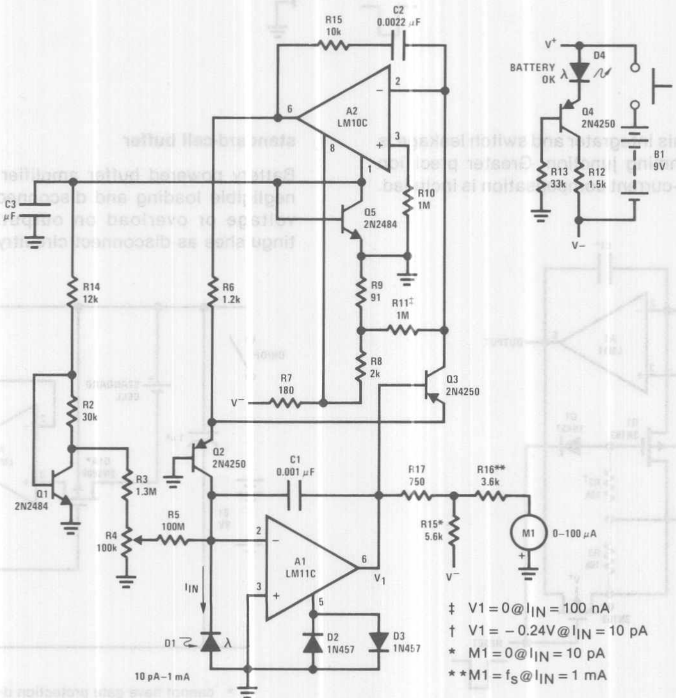
Unusual frequency compensation gives this logarithmic converter a 100 μs time constant from 1 mA down to 100 μA, increasing from 200 μs to 200 ms from 10 nA to 10 pA. Optional bias current compensation can give 10 pA resolution from −55°C to 100°C. Scale factor is 1V/decade and temperature compensated.



a. Set R11 for $V_{OUT} = 0$ at $I_{IN} = 100$ nA
b. Set R8 for $V_{OUT} = 3V$ at $I_{IN} = 100\ \mu A$
c. Set R3 for $V_{OUT} = -4V$ at $I_{IN} = 10$ pA

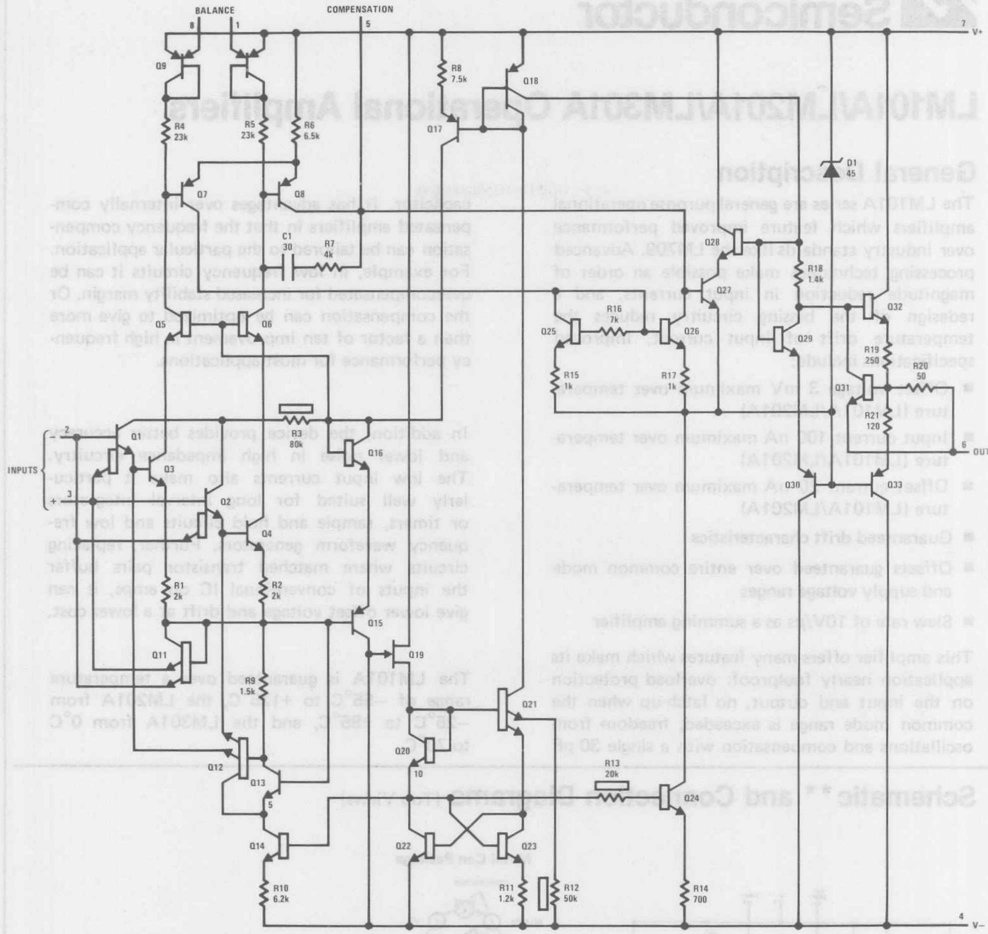
† 3300 ppM/°C. Type Q209 available from Tel Labs, Inc., Manchester, N.H.

Light meter has eight-decade range. Bias current compensation can give input current resolution of better than ±2 pA over 15°C to 55°C.



‡ $V1 = 0 @ I_{IN} = 100$ nA
† $V1 = -0.24V @ I_{IN} = 10$ pA
* $M1 = 0 @ I_{IN} = 10$ pA
** $M1 = f_S @ I_{IN} = 1$ mA

Schematic Diagram



Definition of Terms

Input offset voltage: That voltage which must be applied between the input terminals to bias the unloaded output in the linear region.

Input offset current: The difference in the currents at the input terminals when the output is unloaded in the linear region.

Input bias current: The absolute value of the average of the two input currents.

Input resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Large signal voltage gain: The ratio of the specified output voltage swing to the change in differential input voltage required to produce it.

Common-mode rejection: The ratio of the input voltage range to the change in offset voltage between the extremes.

Temperature drift: The change of a parameter measured at 25°C and either temperature extreme divided by the temperature change.

Supply-voltage rejection: The ratio of the specified supply-voltage change (either or both supplies) to the change in offset voltage between the extremes.

Supply current: The current required from the power source to operate the amplifier with the output unloaded and operating in the linear range.

LM101A/LM201A/LM301A Operational Amplifiers

General Description

The LM101A series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. Advanced processing techniques make possible an order of magnitude reduction in input currents, and a redesign of the biasing circuitry reduces the temperature drift of input current. Improved specifications include:

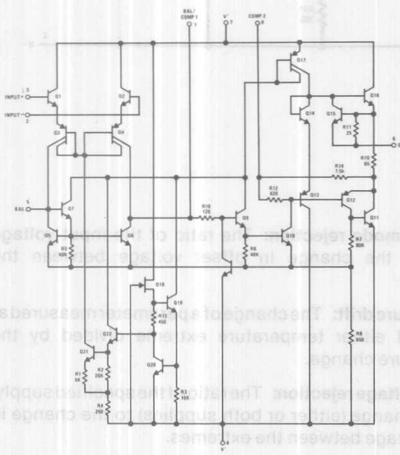
- Offset voltage 3 mV maximum over temperature (LM101A/LM201A)
- Input current 100 nA maximum over temperature (LM101A/LM201A)
- Offset current 20 nA maximum over temperature (LM101A/LM201A)
- Guaranteed drift characteristics
- Offsets guaranteed over entire common mode and supply voltage ranges
- Slew rate of 10V/μs as a summing amplifier

This amplifier offers many features which make its application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, freedom from oscillations and compensation with a single 30 pF capacitor. It has advantages over internally compensated amplifiers in that the frequency compensation can be tailored to the particular application. For example, in low frequency circuits it can be overcompensated for increased stability margin. Or the compensation can be optimized to give more than a factor of ten improvement in high frequency performance for most applications.

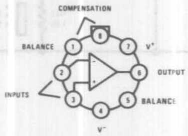
In addition, the device provides better accuracy and lower noise in high impedance circuitry. The low input currents also make it particularly well suited for long interval integrators or timers, sample and hold circuits and low frequency waveform generators. Further, replacing circuits where matched transistor pairs buffer the inputs of conventional IC op amps, it can give lower offset voltage and drift at a lower cost.

The LM101A is guaranteed over a temperature range of −55°C to +125°C, the LM201A from −25°C to +85°C, and the LM301A from 0°C to 70°C.

Schematic ** and Connection Diagrams (Top Views)

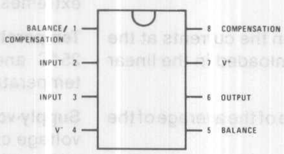


Metal Can Package



Order Number LM101AH, LM201AH or LM301AH
See NS Package H08C

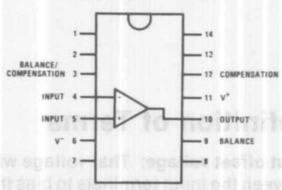
Dual-In-Line Package



Order Number LM101AJ, LM201AJ, LM301AJ
See NS Package J08A

Order Number LM301AN
See NS Package N08A

Dual-In-Line Package



Note: Pin 6 connected to bottom of package.

Order Number LM101AJ-14
LM201AJ-14 or LM301AJ-14
See NS Package J14A

**Pin connections shown are for metal can.

	LM101A/LM201A	LM301A
Power Dissipation (Note 1)	500 mW	500 mW
Differential Input Voltage	±30V	±30V
Input Voltage (Note 2)	±15V	±15V
Output Short Circuit Duration (Note 3)	Indefinite	Indefinite
Operating Temperature Range	−55°C to +125°C (LM101A) −25°C to +85°C (LM201A)	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

Electrical Characteristics (Note 4)

PARAMETER	CONDITIONS	LM101A/LM201A			LM301A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$							
LM101A, LM201A, LM301A	$R_S \leq 50\ k\Omega$		0.7	2.0		2.0	7.5	mV
Input Offset Current	$T_A = 25°C$		1.5	10		3.0	50	nA
Input Bias Current	$T_A = 25°C$		30	75		70	250	nA
Input Resistance	$T_A = 25°C$	1.5	4.0		0.5	2.0		MΩ
Supply Current	$T_A = 25°C$							
	$V_S = \pm 20V$		1.8	3.0				mA
	$V_S = \pm 15V$					1.8	3.0	mA
Large Signal Voltage Gain	$T_A = 25°C, V_S = \pm 15V$ $V_{OUT} = \pm 10V, R_L \geq 2\ k\Omega$	50	160		25	160		V/mV
Input Offset Voltage	$R_S \leq 50\ k\Omega$			3.0			10	mV
	$R_S \leq 10\ k\Omega$							mV
Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 50\ k\Omega$		3.0	15		6.0	30	μV/°C
	$R_S \leq 10\ k\Omega$							μV/°C
Input Offset Current				20			70	nA
	$T_A = T_{MAX}$							nA
	$T_A = T_{MIN}$							nA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq T_{MAX}$		0.01	0.1		0.01	0.3	nA/°C
	$T_{MIN} \leq T_A \leq 25°C$		0.02	0.2		0.02	0.6	nA/°C
Input Bias Current				0.1			0.3	μA
Supply Current	$T_A = T_{MAX}, V_S = \pm 20V$		1.2	2.5				mA
Large Signal Voltage Gain	$V_S = \pm 15V, V_{OUT} = \pm 10V,$ $R_L \geq 2k$	25			15			V/mV
Output Voltage Swing	$V_S = \pm 15V$							
	$R_L = 10\ k\Omega$	±12	±14		±12	±14		V
	$R_L = 2\ k\Omega$	±10	±13		±10	±13		V
Input Voltage Range	$V_S = \pm 20V$	±15						V
	$V_S = \pm 15V$		+15, −13		±12	+15, −13		V
Common-Mode Rejection Ratio	$R_S \leq 50\ k\Omega$	80	96		70	90		dB
	$R_S \leq 10\ k\Omega$							dB
Supply Voltage Rejection Ratio	$R_S \leq 50\ k\Omega$	80	96		70	96		dB
	$R_S \leq 10\ k\Omega$							dB

Note 1: The maximum junction temperature of the LM101A is 150°C, and that of the LM201A/LM301A is 100°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 187°C/W, junction to ambient.

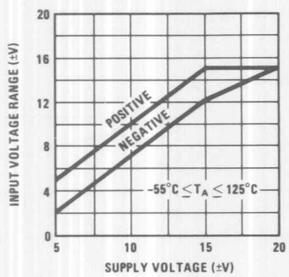
Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: Continuous short circuit is allowed for case temperatures to 125°C and ambient temperatures to 75°C for LM101A/LM201A, and 70°C and 55°C respectively for LM301A.

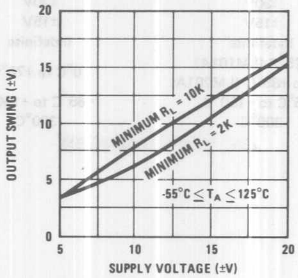
Note 4: Unless otherwise specified, these specifications apply for C1 = 30 pF, $\pm 5V \leq V_S \leq \pm 20V$ and $-55°C \leq T_A \leq +125°C$ (LM101A), $\pm 5V \leq V_S \leq \pm 20V$ and $-25°C \leq T_A \leq +85°C$ (LM201A), $\pm 5V \leq V_S \leq \pm 15V$ and $0°C \leq T_A \leq +70°C$ (LM301A).

Guaranteed Performance Characteristics LM101A/LM201A

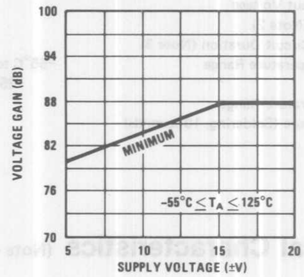
Input Voltage Range



Output Swing

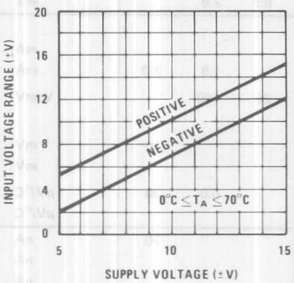


Voltage Gain

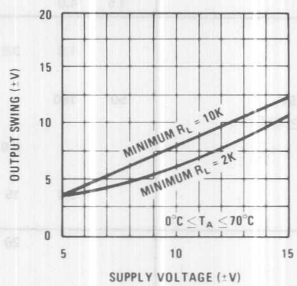


Guaranteed Performance Characteristics LM301A

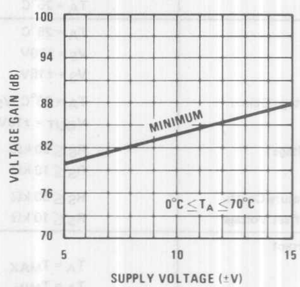
Input Voltage Range



Output Swing

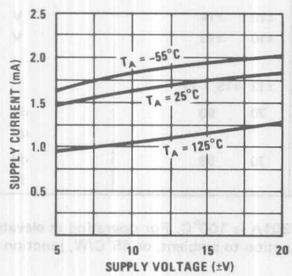


Voltage Gain

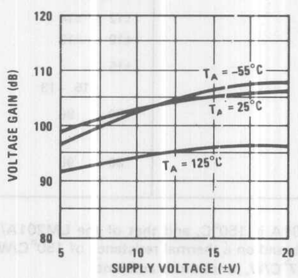


Typical Performance Characteristics

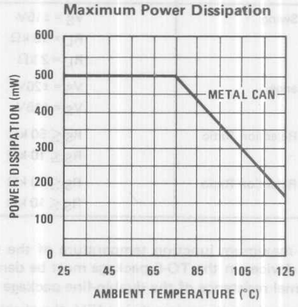
Supply Current



Voltage Gain

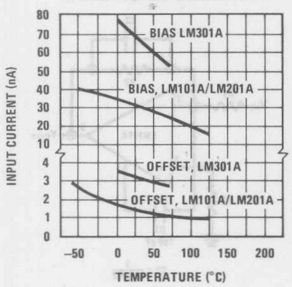


Maximum Power Dissipation

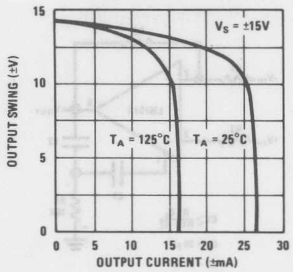


Typical Performance Characteristics (Continued)

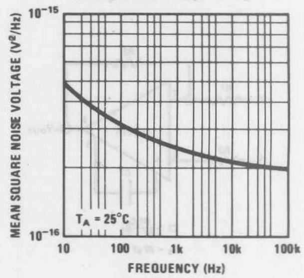
Input Current, LM101A/LM201A/LM301A



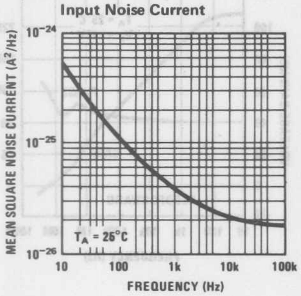
Current Limiting



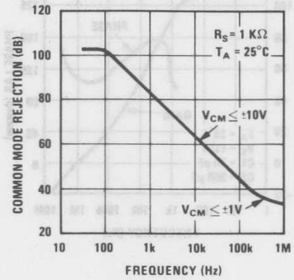
Input Noise Voltage



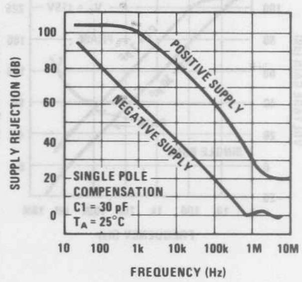
Input Noise Current



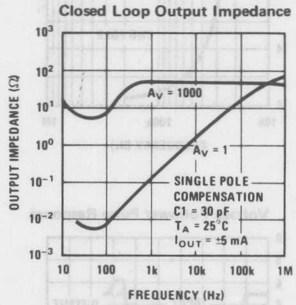
Common Mode Rejection

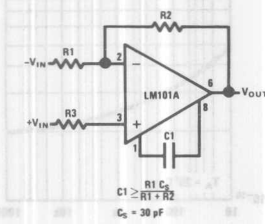


Power Supply Rejection



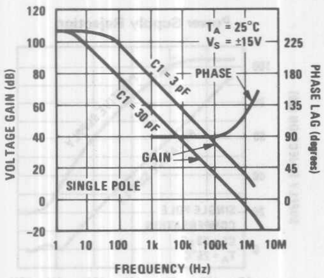
Closed Loop Output Impedance



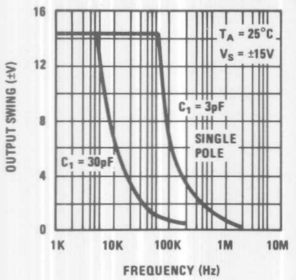


**Pin connections shown are for metal can.

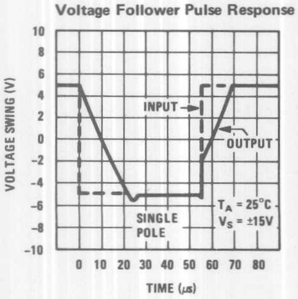
Open Loop Frequency Response

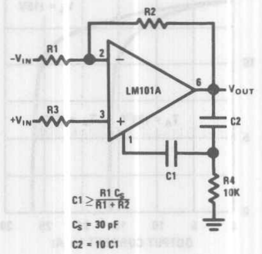


Large Signal Frequency Response

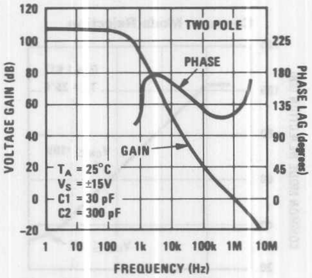


Voltage Follower Pulse Response

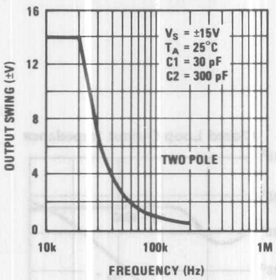




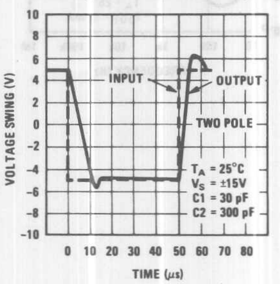
Open Loop Frequency Response

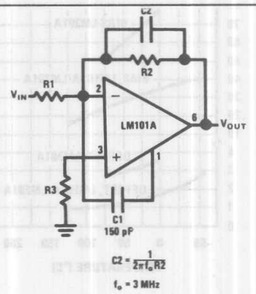


Large Signal Frequency Response

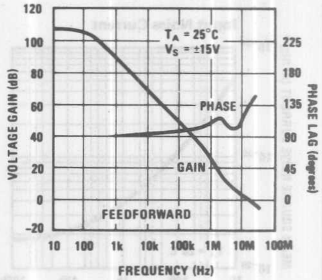


Voltage Follower Pulse Response

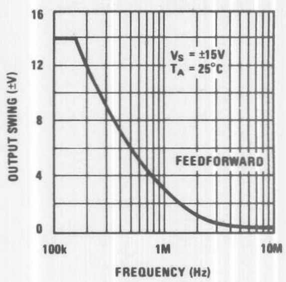




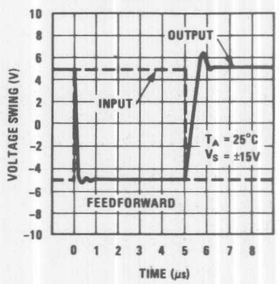
Open Loop Frequency Response



Large Signal Frequency Response

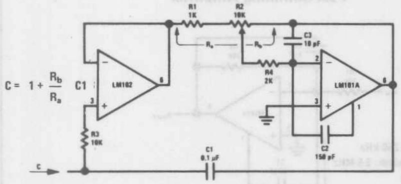


Inverter Pulse Response

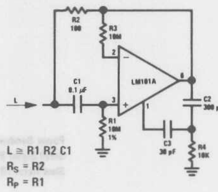


Typical Applications **

Variable Capacitance Multiplier

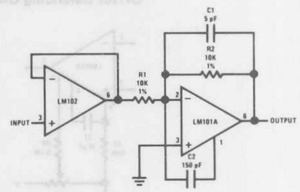


Simulated Inductor

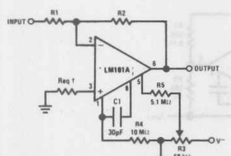


$L \geq R1\ R2\ C1$
$R_S = R2$
$R_P = R1$

Fast Inverting Amplifier With High Input Impedance

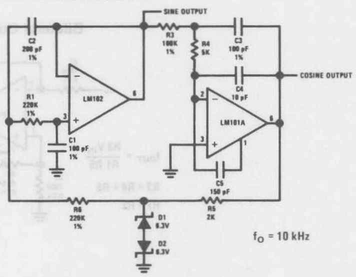


Inverting Amplifier with Balancing Circuit



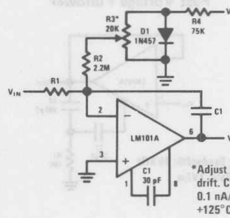
†May be zero or equal to parallel combination of R1 and R2 for minimum offset.

Sine Wave Oscillator



$f_O = 10$ kHz

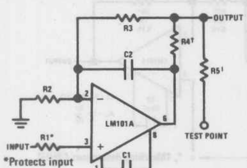
Integrator with Bias Current Compensation



*Adjust for zero integrator drift. Current drift typically 0.1 nA/°C over −55°C to +125°C temperature range.

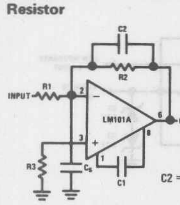
Application Hints **

Protecting Against Gross Fault Conditions



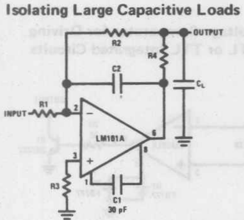
*Protects input
†Protects output
‡Protects output—not needed when R4 is used.

Compensating For Stray Input Capacitances Or Large Feedback Resistor



$$C2 = \frac{R1\ C_S}{R2}$$

Isolating Large Capacitive Loads



Although the LM101A is designed for trouble free operation, experience has indicated that it is wise to observe certain precautions given below to protect the devices from abnormal operating conditions. It might be pointed out that the advice given here is applicable to practically any IC op amp, although the exact reason why may differ with different devices.

When driving either input from a low-impedance source, a limiting resistor should be placed in series with the input lead to limit the peak instantaneous output current of the source to something less than 100 mA. This is especially important when the inputs go outside a piece of equipment where they could accidentally be connected to high voltage sources. Large capacitors on the input (greater than 0.1 μF) should be treated as a low source impedance and isolated with a resistor. Low impedance sources do not cause a problem unless their output voltage exceeds the supply voltage. However, the supplies go to zero when they are turned off, so the isolation is usually needed.

The output circuitry is protected against damage from shorts to ground. However, when the amplifier output is connected to a test point, it should be isolated by a limiting resistor, as test points frequently get shorted to bad places. Further, when the amplifier drives a load external to the equipment, it is also advisable to use some sort of limiting resistance to preclude mishaps.

Precautions should be taken to insure that the power supplies for the integrated circuit never become reversed—even under transient conditions. With reverse voltages greater than 1V, the IC will conduct excessive current, fuzing internal aluminum interconnects. If there is a possibility of this happening, clamp diodes with a high peak current rating should be installed on the supply lines. Reversal of the voltage between V^+ and V^- will always cause a problem, although reversals with respect to ground may also give difficulties in many circuits.

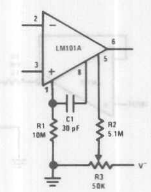
The minimum values given for the frequency compensation capacitor are stable only for source resistances less than 10 kΩ, stray capacitances on the summing junction less than 5 pF and capacitive loads smaller than 100 pF. If any of these conditions are not met, it becomes necessary to overcompensate the amplifier with a larger compensation capacitor. Alternately, lead capacitors can be used in the feedback network to negate the effect of stray capacitance and large feedback resistors or an RC network can be added to isolate capacitive loads.

Although the LM101A is relatively unaffected by supply bypassing, this cannot be ignored altogether. Generally it is necessary to bypass the supplies to ground at least once on every circuit card, and more bypass points may be required if more than five amplifiers are used. When feed-forward compensation is employed, however, it is advisable to bypass the supply leads of each amplifier with low inductance capacitors because of the higher frequencies involved.

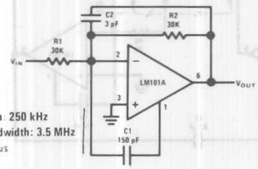
**Pin connections shown are for metal can.

Typical Applications** (Continued)

Standard Compensation and Offset Balancing Circuit

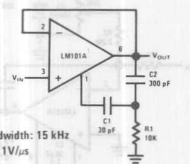


Fast Summing Amplifier



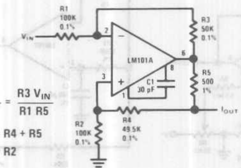
Power Bandwidth: 250 kHz
Small Signal Bandwidth: 3.5 MHz
Slew Rate: 10V/μs

Fast Voltage Follower



Power Bandwidth: 15 kHz
Slew Rate: 1V/μs

Bilateral Current Source

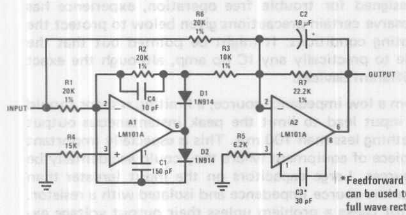


$$I_{OUT} = \frac{R3\ V_{IN}}{R1\ R5}$$

$R3 = R4 + R5$

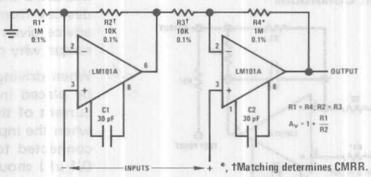
$R1 = R2$

Fast AC/DC Converter*



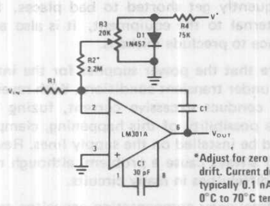
*Feedforward compensation can be used to make a fast full wave rectifier without a filter.

Instrumentation Amplifier



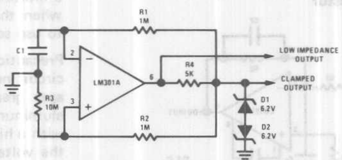
*, †Matching determines CMRR.

Integrator with Bias Current Compensation

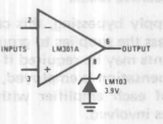


*Adjust for zero integrator drift. Current drift typically 0.1 nA/°C over 0°C to 70°C temperature range.

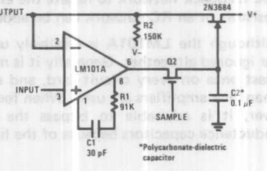
Low Frequency Square Wave Generator



Voltage Comparator for Driving RTL Logic or High Current Driver

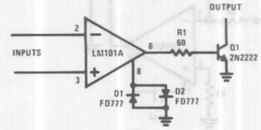


Low Drift Sample and Hold



*Polycarbonate-dielectric capacitor

Voltage Comparator for Driving DTL or TTL Integrated Circuits



**Pin connections shown are for metal can.

LM102/LM202/LM302 Voltage Followers

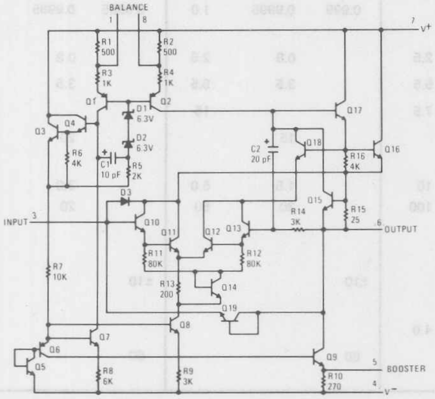
General Description

The LM102 series are high-gain operational amplifiers designed specifically for unity-gain voltage follower applications. Built on a single silicon chip, the devices incorporate advanced processing techniques to obtain very low input current and high input impedance. Further, the input transistors are operated at zero collector-base voltage to virtually eliminate high temperature leakage currents. It can therefore be operated in a temperature stabilized component oven to get extremely low input currents and low offset voltage drift. Other outstanding characteristics of the device include:

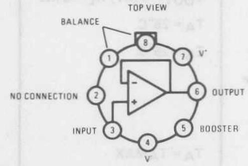
- Fast slewing — 10V/μs
- Low input current — 10 nA (max)
- High input resistance — 10,000 MΩ
- No external frequency compensation required
- Simple offset balancing with optional 1K potentiometer
- Plug-in replacement for both the LM101 and LM709 in voltage follower applications.

The LM102, which is designed to operate with supply voltages between ±12V and ±15V, also features low input capacitance as well as excellent small signal and large signal frequency response — all of which minimize high frequency gain error. Because of the low wiring capacitances inherent in monolithic construction, this fast operation can be realized without increasing power consumption.

Schematic** and Connection Diagrams



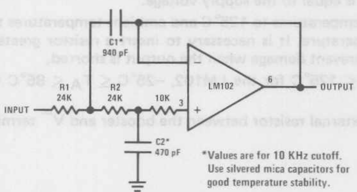
Metal Can Package



Order Number LM102H, LM202H or LM302H
See NS Package H08C

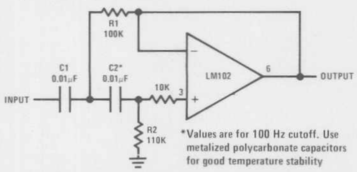
Typical Applications**

Low Pass Active Filter



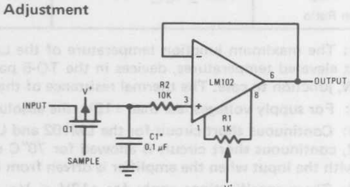
*Values are for 10 KHz cutoff. Use silvered mica capacitors for good temperature stability.

High Pass Active Filter



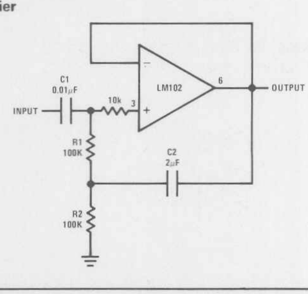
*Values are for 100 Hz cutoff. Use metalized polycarbonate capacitors for good temperature stability

Sample and Hold With Offset Adjustment



*Polycarbonate-dielectric capacitor.

High Input Impedance AC Amplifier



**Pin connections shown are for metal can.

Supply Voltage		±18V
Power Dissipation (Note 1)		500 mW
Input Voltage (Note 2)		±15V
Output Short Circuit Duration (Note 3)		Indefinite
Operating Temperature Range	LM102	−55°C to 125°C
	LM202	−25°C to 85°C
	LM302	0°C to 70°C
Storage Temperature Range		−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)		300°C

Electrical Characteristics (Note 4)

PARAMETER	CONDITIONS	LM102			LM202			LM302			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$		2	5		3	10		5	15	mV
Input Bias Current	$T_A = 25°C$		3	10		7	15		10	30	nA
Input Resistance	$T_A = 25°C$	10^{10}	10^{12}		10^{10}	10^{12}		10^9	10^{12}		Ω
Input Capacitance				3.0		3.0			3.0		pF
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm15V$, $V_{OUT} = \pm10V$, $R_L = 8\ k\Omega$	0.999	0.9996		0.999	0.9995	1.0	0.9985	0.9995	1.0	V/V
Output Resistance	$T_A = 25°C$		0.8	2.5		0.8	2.5		0.8	2.5	Ω
Supply Current	$T_A = 25°C$		3.5	5.5		3.5	5.5		3.5	5.5	mA
Input Offset Voltage				7.5			15			20	mV
Offset Voltage Temperature Drift			6			15			20		μV/°C
Input Bias Current	$T_A = T_AMAX$		3	10		1.5	5.0		3.0	15	nA
	$T_A = T_AMIN$		30	100		30	50		20	50	nA
Large Signal Voltage Gain	$V_S = \pm15V$, $V_{OUT} = \pm10V$ $R_L = 10\ k\Omega$	0.999									
Output Voltage Swing	$V_S = \pm15V$, $R_L = 10\ k\Omega$, (Note 5)	±10			±10			±10			V
Supply Current	$T_A = 125°C$		2.6	4.0							mA
Supply Voltage Rejection Ratio	$\pm12V \le V_S \le \pm15V$	60			60			60			dB

Note 1: The maximum junction temperature of the LM102 is 150°C, while that of the LM202 is 100°C and that of the LM302 is 85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

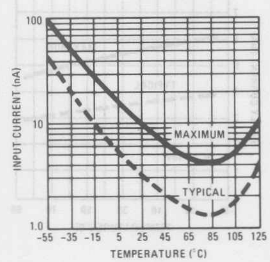
Note 3: Continuous short circuit for the LM102 and LM202 is allowed for case temperatures to 125°C and ambient temperatures to 70°C. For the LM302, continuous short circuit is allowed for 70°C case or 55°C ambient temperature. It is necessary to insert a resistor greater than 2 kΩ in series with the input when the amplifier is driven from low impedance sources to prevent damage when the output is shorted.

Note 4: These specifications apply for $\pm12V \le V_S \le \pm15V$ and $-55°C \le T_A \le 125°C$ for the LM102, $-25°C \le T_A \le 85°C$ for the LM202, and $0°C \le T_A \le 70°C$ for the LM302 unless otherwise specified.

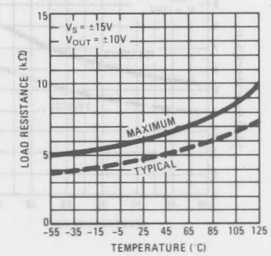
Note 5: Increased output swing under load can be obtained by connecting an external resistor between the booster and V^- terminals. See curve.

Guaranteed Performance Characteristics LM102

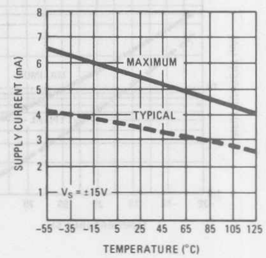
Input Current



Output Swing

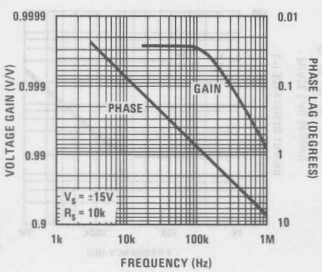


Supply Current

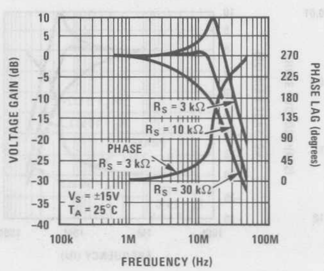


Typical Performance Characteristics LM102

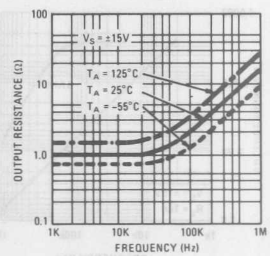
Voltage Gain and Phase Lag



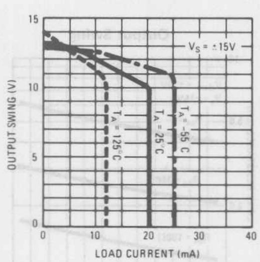
Voltage Gain and Phase Lag



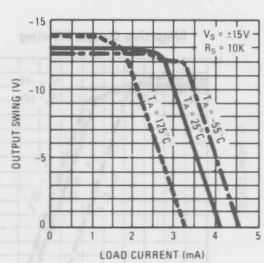
Output Resistance



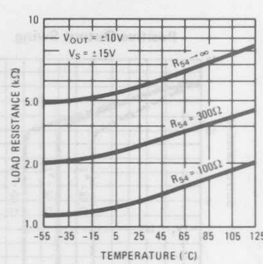
Positive Output Swing



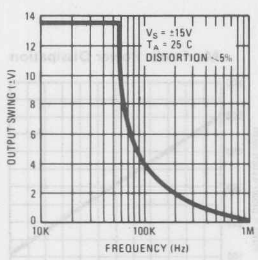
Negative Output Swing



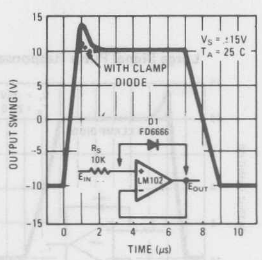
Output Swing



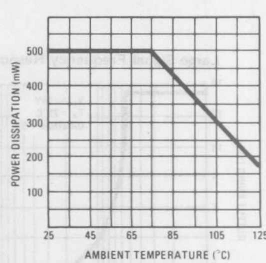
Large Signal Frequency Response



Large Signal Pulse Response



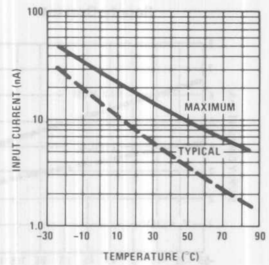
Maximum Power Dissipation



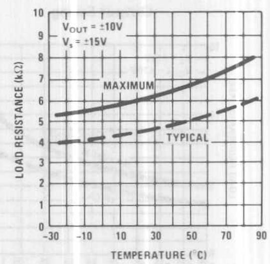
3

Guaranteed Performance Characteristics LM202

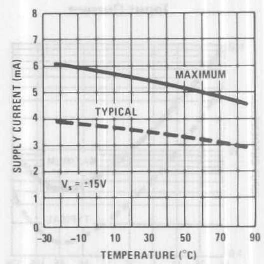
Input Current



Output Swing

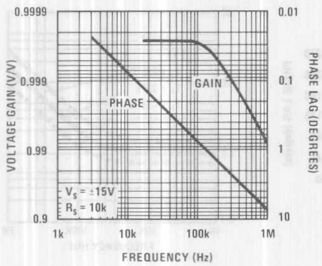


Supply Current

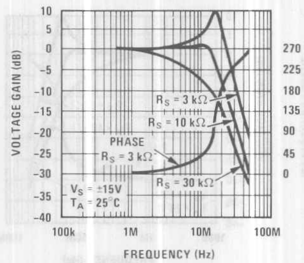


Typical Performance Characteristics LM202

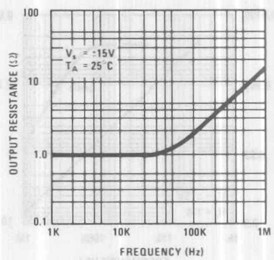
Voltage Gain and Phase Lag



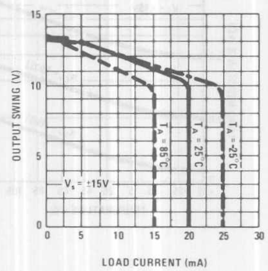
Voltage Gain and Phase Lag



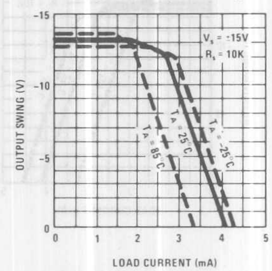
Output Resistance



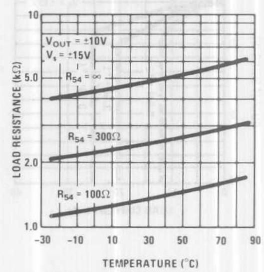
Positive Output Swing



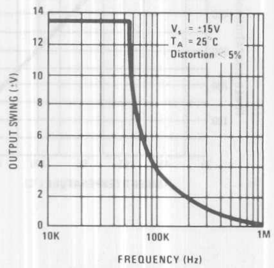
Negative Output Swing



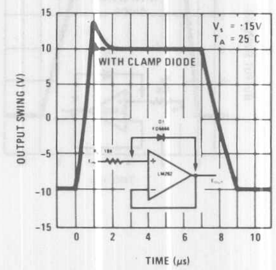
Output Swing



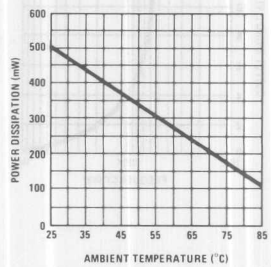
Large Signal Frequency Response



Large Signal Pulse Response

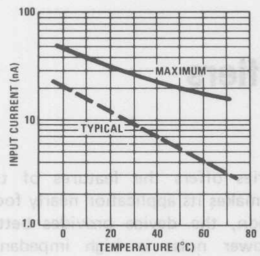


Maximum Power Dissipation

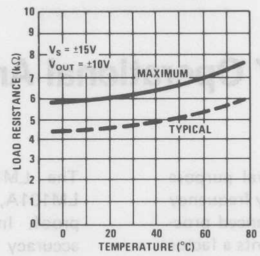


Guaranteed Performance Characteristics LM302

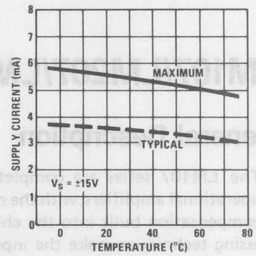
Input Current



Output Swing

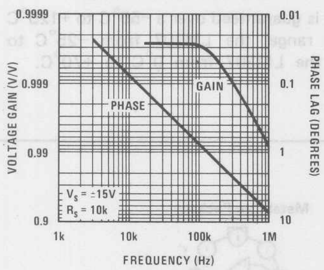


Supply Current

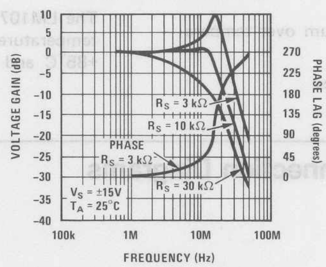


Typical Performance Characteristics LM302

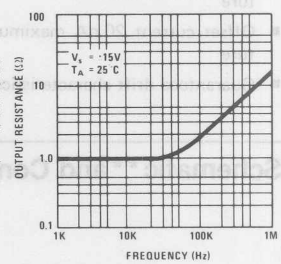
Voltage Gain and Phase Lag



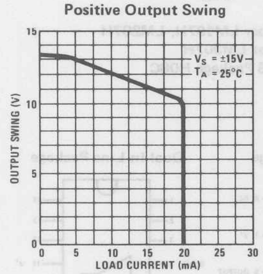
Voltage Gain and Phase Lag



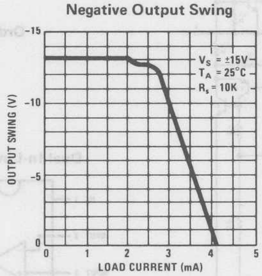
Output Resistance



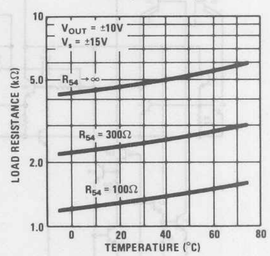
Positive Output Swing



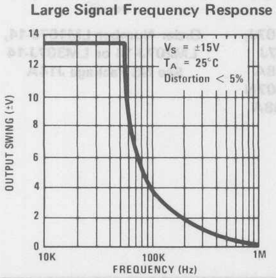
Negative Output Swing



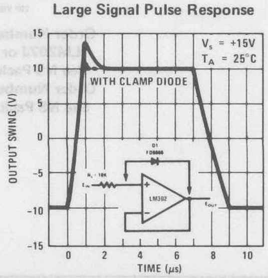
Output Swing



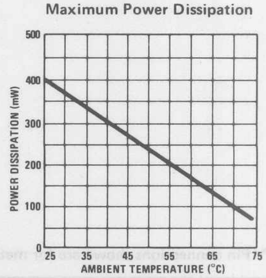
Large Signal Frequency Response



Large Signal Pulse Response



Maximum Power Dissipation



Semiconductor

LM107/LM207/LM307 Operational Amplifiers

General Description

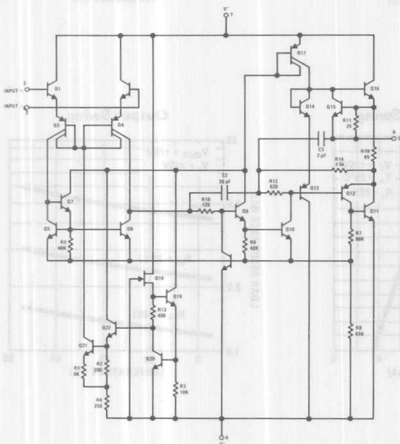
The LM107 series are complete, general purpose operational amplifiers, with the necessary frequency compensation built into the chip. Advanced processing techniques make the input currents a factor of ten lower than industry standards like the 709. Yet, they are a direct, plug-in replacement for the 709, LM101A and 741.

- Offset voltage 3 mV maximum over temperature
- Input current 100 nA maximum over temperature
- Offset current 20 nA maximum over temperature
- Guaranteed drift characteristics

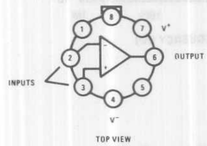
The LM107 series offers the features of the LM101A, which makes its application nearly foolproof. In addition, the device provides better accuracy and lower noise in high impedance circuitry. The low input currents also make it particularly well suited for long interval integrators or timers, sample and hold circuits and low frequency waveform generators. Further, replacing circuits where matched transistor pairs buffer the inputs of conventional IC op amps, it can give lower offset voltage and drift at a lower cost.

The LM107 is guaranteed over a $-55^\circ C$ to $+125^\circ C$ temperature range, the LM207 from $-25^\circ C$ to $+85^\circ C$ and the LM307 from $0^\circ C$ to $+70^\circ C$.

Schematic** and Connection Diagrams

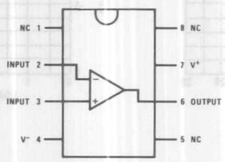


Metal Can Package



Order Number LM107H, LM207H or LM307H
See NS Package H08C

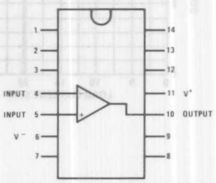
Dual-In-Line Package



Note: Pin 4 connected to bottom of package.
TOP VIEW

Order Number LM107J, LM207J or LM307J
See NS Package J08A
Order Number LM307N
See NS Package N08A

Dual-In-Line Package



Note: Pin 6 connected to bottom of package.
TOP VIEW

Order Number LM107J-14, LM207J-14 or LM307J-14
See NS Package J14A

**Pin connections shown are for metal can.

Absolute Maximum Ratings

	LM107/LM207	LM307
Supply Voltage	±22V	±18V
Power Dissipation (Note 1)	500 mW	500 mW
Differential Input Voltage	±30V	±30V
Input Voltage (Note 2)	±15V	±15V
Output Short-Circuit Duration	Indefinite	Indefinite
Operating Temperature Range		
(LM107)	−55°C to +125°C	0°C to +70°C
(LM207)	−25°C to +85°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

	T_{MIN}	T_{MAX}
LM107	−55°C	+125°C
LM207	−25°C	+85°C
LM307	0°C	+70°C

Electrical Characteristics (Note 3)

PARAMETER	CONDITIONS	LM107/LM207			LM307			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$, $R_S \le 50\ k\Omega$		0.7	2.0		2.0	7.5	mV
Input Offset Current	$T_A = 25°C$		1.5	10		3.0	50	nA
Input Bias Current	$T_A = 25°C$		30	75		70	250	nA
Input Resistance	$T_A = 25°C$	1.5	4.0		0.5	2.0		MΩ
Supply Current	$T_A = 25°C$							
	$V_S = \pm 20V$		1.8	3.0				mA
	$V_S = \pm 15V$					1.8	3.0	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \ge 2\ k\Omega$	50	160		25	160		V/mV
Input Offset Voltage	$R_S \le 50\ k\Omega$			3.0			10	mV
Average Temperature Coefficient of Input Offset Voltage			3.0	15		6.0	30	μV/°C
Input Offset Current				20			70	nA
Average Temperature Coefficient of Input Offset Current	$25°C \le T_A \le T_{MAX}$		0.01	0.1		0.01	0.3	nA/°C
	$T_{MIN} \le T_A \le 25°C$		0.02	0.2		0.02	0.6	nA/°C
Input Bias Current				100			300	nA
Supply Current	$T_A = +125°C$, $V_S = \pm 20V$		1.2	2.5				mA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \ge 2\ k\Omega$	25			15			V/mV
Output Voltage Swing	$V_S = \pm 15V$							
	$R_L = 10\ k\Omega$	±12	±14		±12	±14		V
	$R_L = 2\ k\Omega$	±10	±13		±10	±13		V
Input Voltage Range	$V_S = \pm 20V$	±15						V
	$V_S = \pm 15V$		+15 −13		±12	+15 −13		V
Common Mode Rejection Ratio	$R_S \le 50\ k\Omega$	80	96		70	90		dB
Supply Voltage Rejection Ratio	$R_S \le 50\ k\Omega$	80	96		70	96		dB

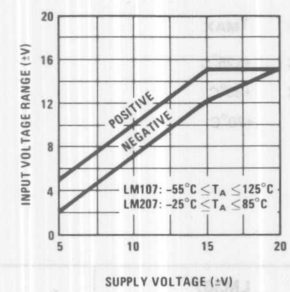
Note 1: The maximum junction temperature of the LM107 is 150°C, and the LM207/LM307 is 100°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: For supply voltages less than −15V, the absolute maximum input voltage is equal to the supply voltage.

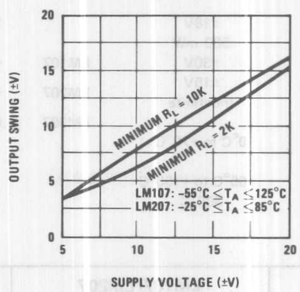
Note 3: These specifications apply for $\pm 5V \le V_S \le +20V$ and $-55°C \le T_A \le +125°C$ for the LM107 or $-25°C \le T_A \le +85°C$ for the LM207, and $0°C \le T_A \le +70°C$ and $\pm 5V \le V_S \le \pm 15V$ for the LM307 unless otherwise specified.

Guaranteed Performance Characteristics LM107/LM207

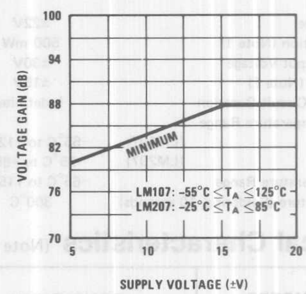
Input Voltage Range



Output Swing

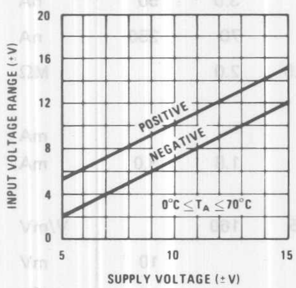


Voltage Gain

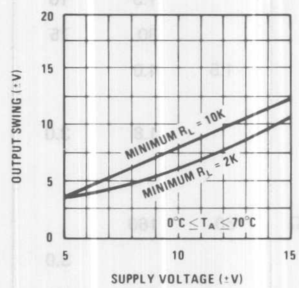


Guaranteed Performance Characteristics LM307

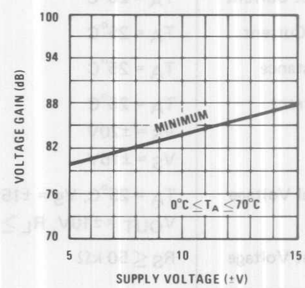
Input Voltage Range



Output Swing

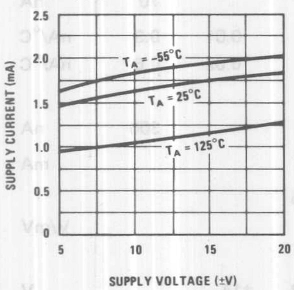


Voltage Gain

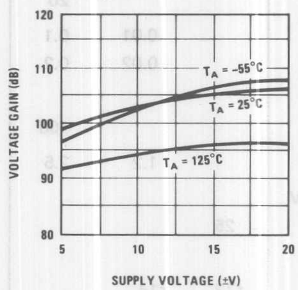


Typical Performance Characteristics

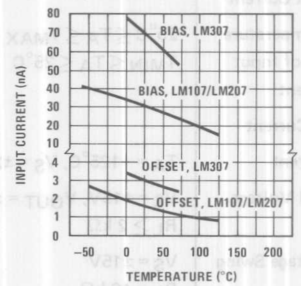
Supply Current



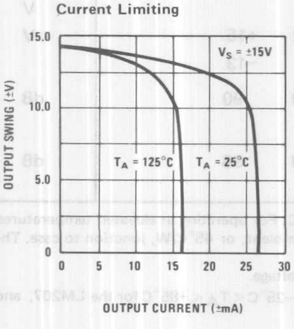
Voltage Gain



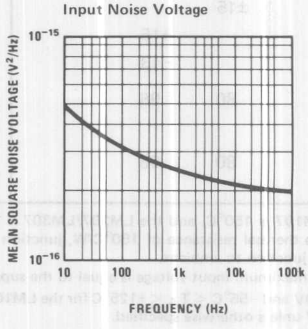
Input Current



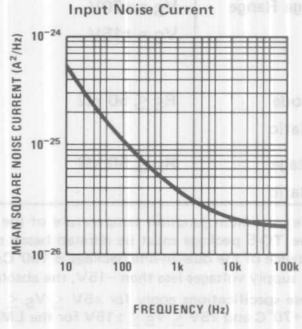
Current Limiting



Input Noise Voltage

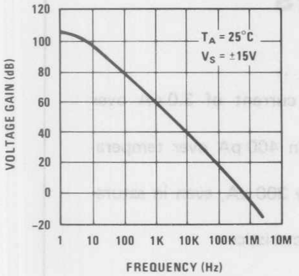


Input Noise Current

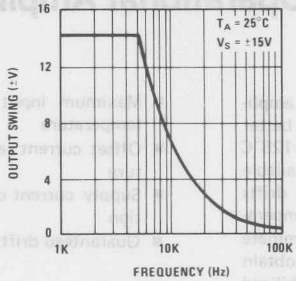


Typical Performance Characteristics (Continued)

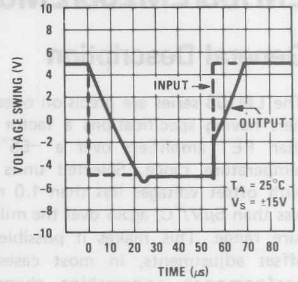
Open Loop Frequency Response



Large Signal Frequency Response

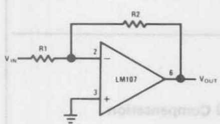


Voltage Follower Pulse Response



Typical Applications**

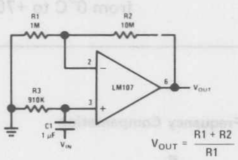
Inverting Amplifier



$$V_{OUT} = -\frac{R2}{R1} V_{IN}$$

$R_{IN} = R1$

Non-Inverting AC Amplifier

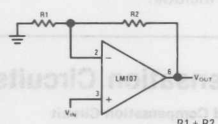


$$V_{OUT} = \frac{R1 + R2}{R1} V_{IN}$$

$R_{IN} = R3$

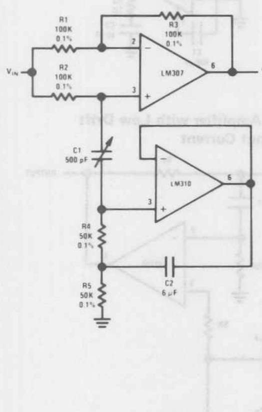
$R3 = R1/R2$

Non-Inverting Amplifier



$$V_{OUT} = \frac{R1 + R2}{R1} V_{IN}$$

Tunable Notch Filter



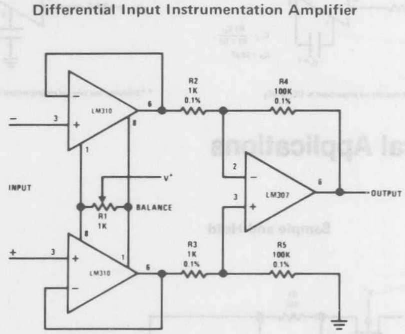
$R1 = R2 = R3$

$R4 = R5 = \frac{R1}{2}$

$$f_O = \frac{1}{2\pi \sqrt{C1\ C2\ (R2)^2}}$$

$= 60$ Hz

Differential Input Instrumentation Amplifier



**Pin connections shown are for metal can.

LM108/LM208/LM308 Operational Amplifiers

General Description

The LM108 series are precision operational amplifiers having specifications a factor of ten better than FET amplifiers over a −55°C to +125°C temperature range. Selected units are available with offset voltages less than 1.0 mV and drifts less than 5μV/°C, again over the military temperature range. This makes it possible to eliminate offset adjustments, in most cases, and obtain performance approaching chopper stabilized amplifiers.

The devices operate with supply voltages from ±2V to ±20V and have sufficient supply rejection to use unregulated supplies. Although the circuit is interchangeable with and uses the same compensation as the LM101A, an alternate compensation scheme can be used to make it particularly insensitive to power supply noise and to make supply bypass capacitors unnecessary. Outstanding characteristics include:

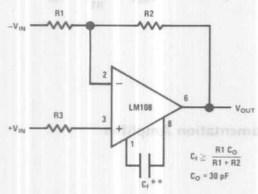
- Maximum input bias current of 3.0 nA over temperature
- Offset current less than 400 pA over temperature
- Supply current of only 300 μA, even in saturation
- Guaranteed drift characteristics

The low current error of the LM108 series makes possible many designs that are not practical with conventional amplifiers. In fact, it operates from 10 MΩ source resistances, introducing less error than devices like the 709 with 10 kΩ sources. Integrators with drifts less than 500 μV/sec and analog time delays in excess of one hour can be made using capacitors no larger than 1 μF.

The LM108 is guaranteed from −55°C to +125°C, the LM208 from −25°C to +85°C, and the LM308 from 0°C to +70°C.

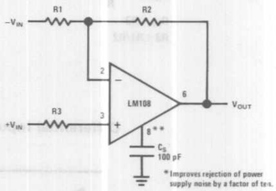
Compensation Circuits

Standard Compensation Circuit



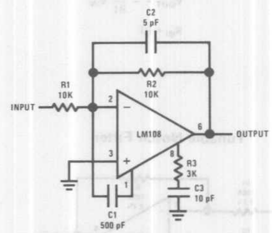
** Bandwidth and slew rate are proportional to $1/C_f$ or $1/C_s$

Alternate* Frequency Compensation



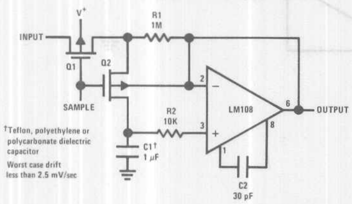
** Bandwidth and slew rate are proportional to $1/C_f$ or $1/C_s$

Feedforward Compensation

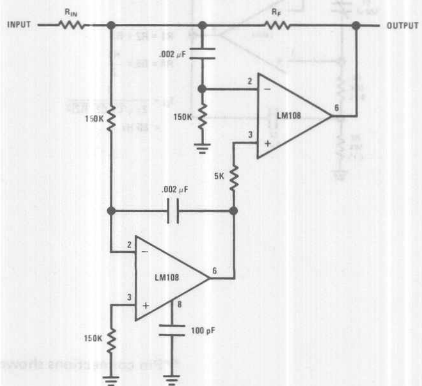


Typical Applications

Sample and Hold



High Speed Amplifier with Low Drift and Low Input Current



Absolute Maximum Ratings

	LM108/LM208	LM308
Supply Voltage	±20V	±18V
Power Dissipation (Note 1)	500 mW	500 mW
Differential Input Current (Note 2)	±10 mA	±10 mA
Input Voltage (Note 3)	±15V	±15V
Output Short-Circuit Duration	Indefinite	Indefinite
Operating Temperature Range (LM108)	−55°C to +125°C	0°C to +70°C
(LM208)	−25°C to +85°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

Electrical Characteristics (Note 4)

PARAMETER	CONDITIONS	LM108/LM208			LM308			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$		0.7	2.0		2.0	7.5	mV
Input Offset Current	$T_A = 25°C$		0.05	0.2		0.2	1	nA
Input Bias Current	$T_A = 25°C$		0.8	2.0		1.5	7	nA
Input Resistance	$T_A = 25°C$	30	70		10	40		MΩ
Supply Current	$T_A = 25°C$		0.3	0.6		0.3	0.8	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 10\ k\Omega$	50	300		25	300		V/mV
Input Offset Voltage				3.0			10	mV
Average Temperature Coefficient of Input Offset Voltage			3.0	15		6.0	30	µV/°C
Input Offset Current				0.4			1.5	nA
Average Temperature Coefficient of Input Offset Current			0.5	2.5		2.0	10	pA/°C
Input Bias Current				3.0			10	nA
Supply Current	$T_A = 125°C$		0.15	0.4				mA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 10\ k\Omega$	25			15			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$	±13	±14		±13	±14		V
Input Voltage Range	$V_S = \pm 15V$	±13.5			±14			V
Common-Mode Rejection Ratio		85	100		80	100		dB
Supply Voltage Rejection Ratio		80	96		80	96		dB

Note 1: The maximum junction temperature of the LM108 is 150°C, for the LM208, 100°C and for the LM308, 85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

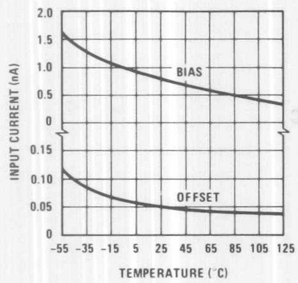
Note 2: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

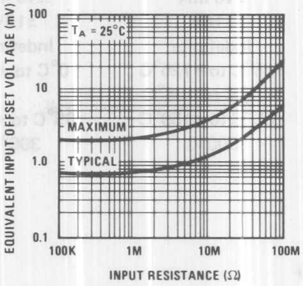
Note 4: These specifications apply for $\pm 5V \leq V_S \leq \pm 20V$ and $-55°C \leq T_A \leq 125°C$, unless otherwise specified. With the LM208, however, all temperature specifications are limited to $-25°C \leq T_A \leq 85°C$, and for the LM308 they are limited to $0°C \leq T_A \leq 70°C$.

Typical Performance Characteristics LM108/LM208

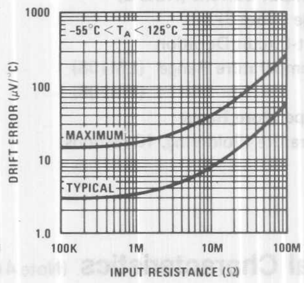
Input Currents



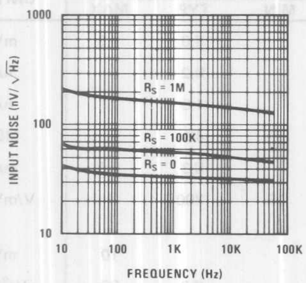
Offset Error



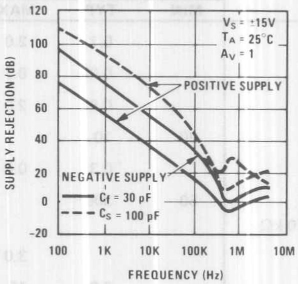
Drift Error



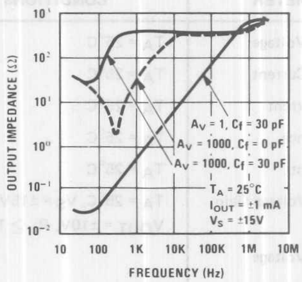
Input Noise Voltage



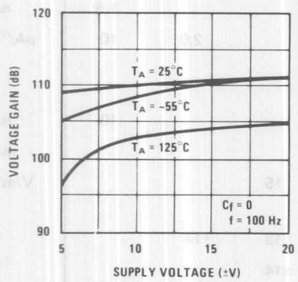
Power Supply Rejection



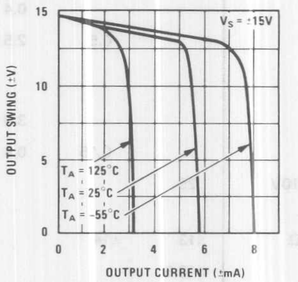
Closed Loop Output Impedance



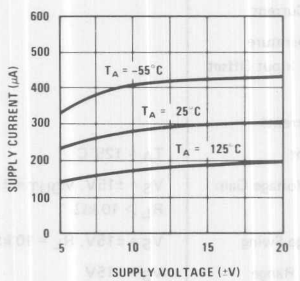
Voltage Gain



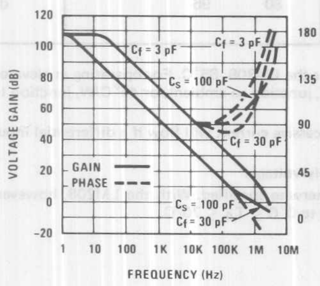
Output Swing



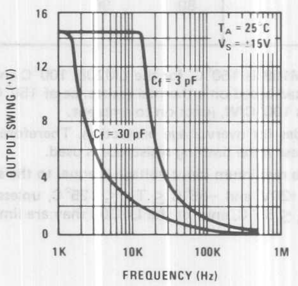
Supply Current



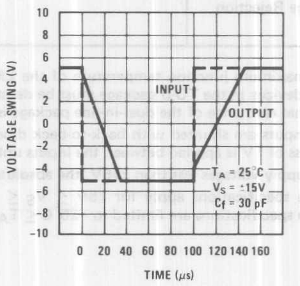
Open Loop Frequency Response



Large Signal Frequency Response

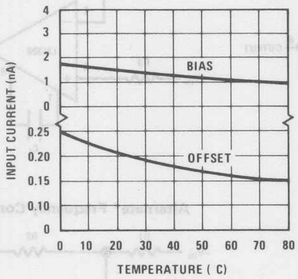


Voltage Follower Pulse Response

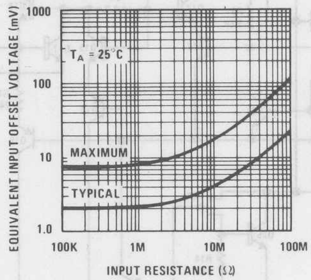


Typical Performance Characteristics LM308

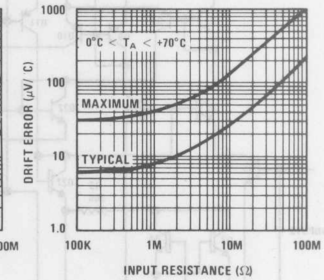
Input Currents



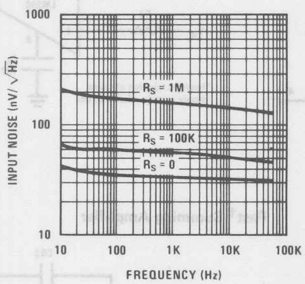
Offset Error



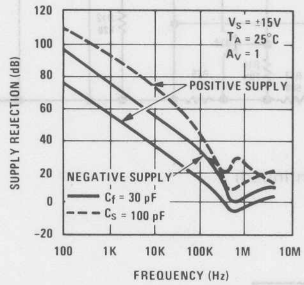
Drift Error



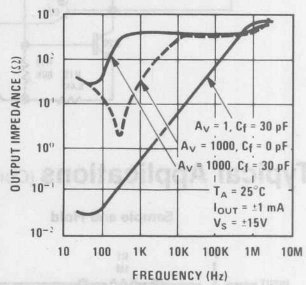
Input Noise Voltage



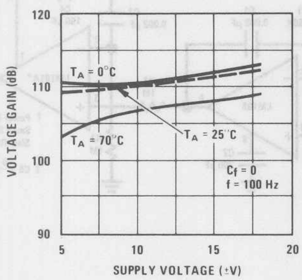
Power Supply Rejection



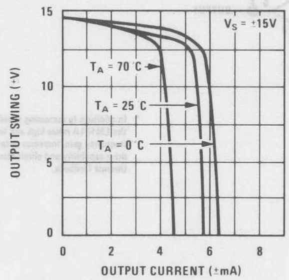
Closed Loop Output Impedance



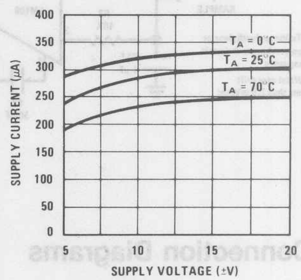
Voltage Gain



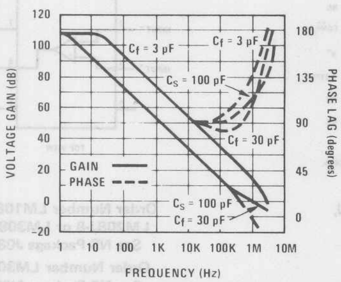
Output Swing



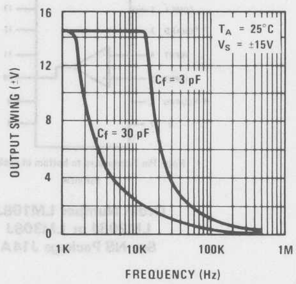
Supply Current



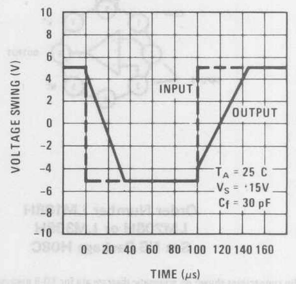
Open Loop Frequency Response

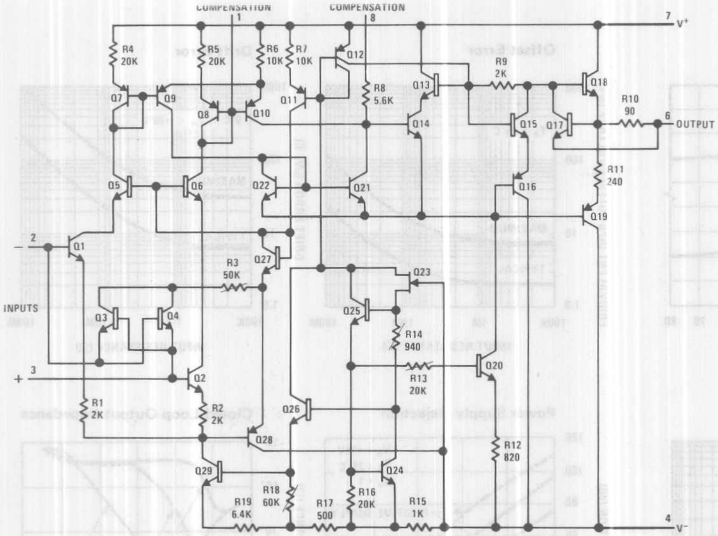


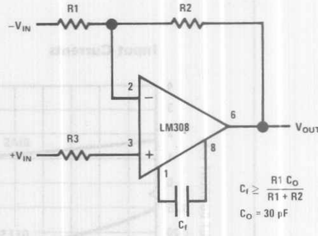
Large Signal Frequency Response



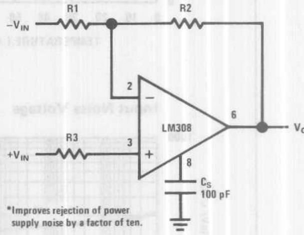
Voltage Follower Pulse Response







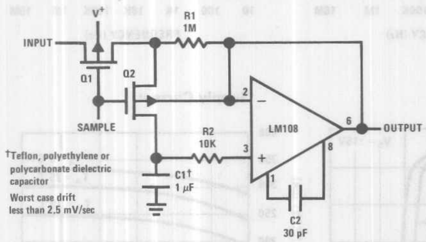
Alternate* Frequency Compensation



*Improves rejection of power supply noise by a factor of ten.

Typical Applications (Continued)

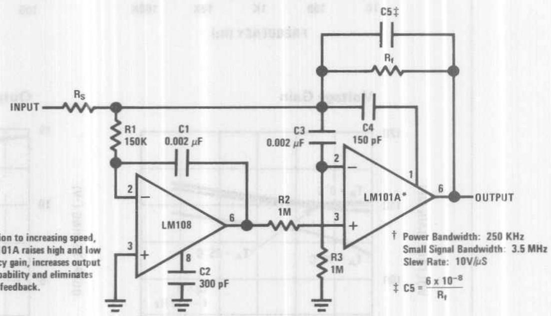
Sample and Hold



†Teflon, polyethylene or polycarbonate dielectric capacitor

Worst case drift less than 2.5 mV/sec

Fast† Summing Amplifier



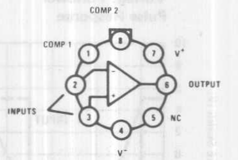
* In addition to increasing speed, the LM101A raises high and low frequency gain, increases output drive capability and eliminates thermal feedback.

† Power Bandwidth: 250 KHz
Small Signal Bandwidth: 3.5 MHz
Slew Rate: 10V/µS

‡ $C5 = \frac{6 \times 10^{-8}}{R_f}$

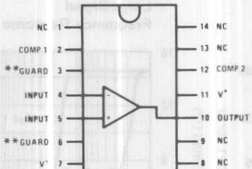
Connection Diagrams

Metal Can Package



Order Number LM108H
LM208H or LM308H
See NS Package H08C

Dual-In-Line Package

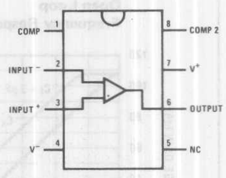


Note: Pin 7 connected to bottom of package.

TOP VIEW

Order Number LM108J,
LM208J or LM308J
See NS Package J14A

Dual-In-Line Package



TOP VIEW

Order Number LM108J-8,
LM208J-8 or LM308J-8
See NS Package J08A

Order Number LM308N
See NS Package N08B

*Pin connections shown on schematic diagram are for TO-5 package.

**Unused pin (no internal connection) to allow for input anti-leakage guard ring on printed circuit board layout.

National Semiconductor

Operational Amplifiers/Buffers

LM108A/LM208A/LM308A, LM308A-1, LM308A-2 Operational Amplifiers

General Description

The LM108/LM108A series are precision operational amplifiers having specifications about a factor of ten better than FET amplifiers over their operating temperature range. In addition to low input currents, these devices have extremely low offset voltage, making it possible to eliminate offset adjustments, in most cases, and obtain performance approaching chopper stabilized amplifiers.

The devices operate with supply voltages from ±2V to ±18V and have sufficient supply rejection to use unregulated supplies. Although the circuit is interchangeable with and uses the same compensation as the LM101A, an alternate compensation scheme can be used to make it particularly insensitive to power supply noise and to make supply bypass capacitors unnecessary. Outstanding characteristics include:

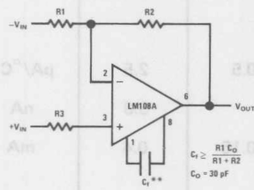
- Offset voltage guaranteed less than 0.5 mV
- Maximum input bias current of 3.0 nA over temperature
- Offset current less than 400 pA over temperature
- Supply current of only 300 μA, even in saturation
- Guaranteed 5 $\mu V/^{\circ}C$ drift.
- Guaranteed 1 $\mu V/^{\circ}C$ for LM308A-1

The low current error of the LM108A series makes possible many designs that are not practical with conventional amplifiers. In fact, it operates from 10 MΩ source resistances, introducing less error than devices like the 709 with 10 kΩ sources. Integrators with drifts less than 500 μV/sec and analog time delays in excess of one hour can be made using capacitors no larger than 1 μF.

The LM208A is identical to the LM108A, except that the LM208A has its performance guaranteed over a −25°C to 85°C temperature range, instead of −55°C to 125°C. The LM308A devices have slightly-relaxed specifications and performance guaranteed over a 0°C to 70°C temperature range.

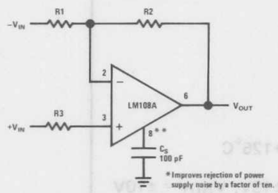
Compensation Circuits

Standard Compensation Circuit



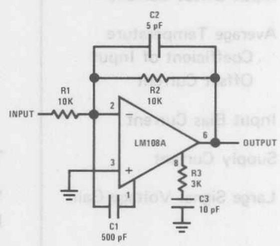
**Bandwidth and slew rate are proportional to $1/C_f$ or $1/C_s$

Alternate* Frequency Compensation



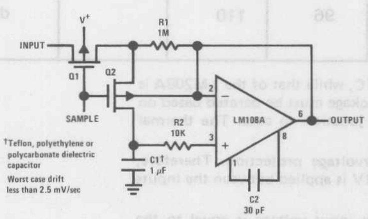
**Bandwidth and slew rate are proportional to $1/C_f$ or $1/C_s$

Feedforward Compensation



Typical Applications

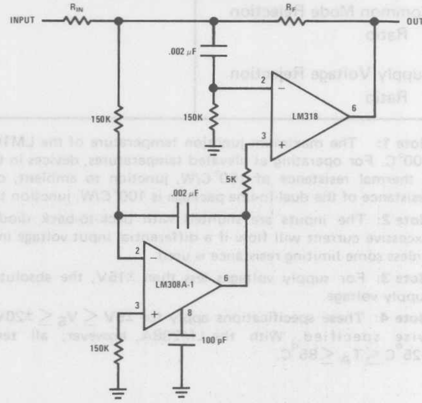
Sample and Hold



†Teflon, polyethylene or polycarbonate dielectric capacitor

Worst case drift less than 2.5 mV/sec

High Speed Amplifier with Low Drift and Low Input Current



LM108A/LM208A

Absolute Maximum Ratings

Supply Voltage		±20V
Power Dissipation (Note 1)		500 mW
Differential Input Current (Note 2)		±10 mA
Input Voltage (Note 3)		±15V
Output Short-Circuit Duration		Indefinite
Operating Temperature Range	LM108A	−55°C to 125°C
	LM208A	−25°C to 85°C
Storage Temperature Range		−65°C to 150°C
Lead Temperature (Soldering, 10 sec)		300°C

Electrical Characteristics (Note 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$T_A = 25°C$		0.3	0.5	mV
Input Offset Current	$T_A = 25°C$		0.05	0.2	nA
Input Bias Current	$T_A = 25°C$		0.8	2.0	nA
Input Resistance	$T_A = 25°C$	30	70		MΩ
Supply Current	$T_A = 25°C$		0.3	0.6	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = ±15V$ $V_{OUT} = ±10V$, $R_L \geq 10\ k\Omega$	80	300		V/mV
Input Offset Voltage				1.0	mV
Average Temperature Coefficient of Input Offset Voltage			1.0	5.0	μV/°C
Input Offset Current				0.4	nA
Average Temperature Coefficient of Input Offset Current			0.5	2.5	pA/°C
Input Bias Current				3.0	nA
Supply Current	$T_A = +125°C$		0.15	0.4	mA
Large Signal Voltage Gain	$V_S = ±15V$, $V_{OUT} = ±10V$ $R_L \geq 10\ k\Omega$	40			V/mV
Output Voltage Swing	$V_S = ±15V$, $R_L = 10\ k\Omega$	±13	±14		V
Input Voltage Range	$V_S = ±15V$	±13.5			V
Common Mode Rejection Ratio		96	110		dB
Supply Voltage Rejection Ratio		96	110		dB

Note 1: The maximum junction temperature of the LM108A is 150°C, while that of the LM208A is 100°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: These specifications apply for $±5V \leq V_S \leq ±20V$ and $-55°C \leq T_A \leq 125°C$, unless otherwise specified. With the LM208A, however, all temperature specifications are limited to $-25°C \leq T_A \leq 85°C$.

LM308A, LM308A-1, LM308A-2

Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation (Note 1)	500 mW
Differential Input Current (Note 2)	±10 mA
Input Voltage (Note 3)	±15V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics (Note 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$T_A = 25°C$		0.3	0.5	mV
Input Offset Current	$T_A = 25°C$		0.2	1	nA
Input Bias Current	$T_A = 25°C$		1.5	7	nA
Input Resistance	$T_A = 25°C$	10	40		MΩ
Supply Current	$T_A = 25°C$, $V_S = \pm15V$		0.3	0.8	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm15V$, $V_{OUT} = \pm10V$, $R_L \geq 10\ k\Omega$	80	300		V/mV
Input Offset Voltage	$V_S = \pm15V$, $R_S = 100\Omega$				
LM308A				0.73	mV
LM308A-1				0.54	mV
LM308A-2				0.59	mV
Average Temperature Coefficient of Input Offset Voltage	$V_S = \pm15V$, $R_S = 100\Omega$				
LM308A			2.0	5.0	μV/°C
LM308A-1			0.6	1.0	μV/°C
LM308A-2			1.3	2.0	μV/°C
Input Offset Current				1.5	nA
Average Temperature Coefficient of Input Offset Current			2.0	10	pA/°C
Input Bias Current				10	nA
Large Signal Voltage Gain	$V_S = \pm15V$, $V_{OUT} = \pm10V$, $R_L \geq 10\ k\Omega$	60			V/mV
Output Voltage Swing	$V_S = \pm15V$, $R_L = 10\ k\Omega$	±13	±14		V
Input Voltage Range	$V_S = \pm15V$	±14			V
Common-Mode Rejection Ratio		96	110		dB
Supply Voltage Rejection Ratio		96	110		dB

Note 1: The maximum junction temperature of the LM308A, LM308-1 and LM308-2 is 85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W junction to ambient.

Note 2: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: These specifications apply for $\pm5V \leq V_S \leq \pm15V$ and $0°C \leq T_A \leq 70°C$, unless otherwise specified.

error can cause the apparent circuit drift to be much higher than would be predicted.

Thermocouple effects caused by temperature gradient across dissimilar metals are perhaps the worst offenders. Only a few degrees gradient can cause hundreds of microvolts of error. The two places this shows up, generally, are the package-to printed circuit board interface and temperature gradients across resistors. Keeping package leads short and the two input leads close together help greatly.

Resistor choice as well as physical placement is important for minimizing thermocouple effects. Carbon, oxide film and some metal film resistors can cause large thermocouple errors. Wirewound resistors of evanohm or manganin are best since they only generate about 2 $\mu V/^{\circ}C$ referenced to copper. Of course, keeping the resistor ends at the same temperature is important. Generally, shielding a low drift stage electrically and thermally will yield good results.

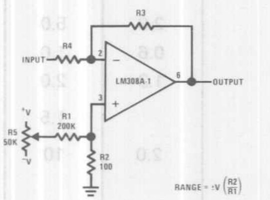
Resistors can cause other errors besides gradient generated voltages. If the gain setting resistors do not track with temperature a gain error will result. For example a gain of 1000 amplifier with a constant 10 ppm/°C difference would have 0.1% error...

erature range, the error at the output is 50 mV. Referred to input, this is a 50 μV error. All of the gain fixing resistor should be the same material.

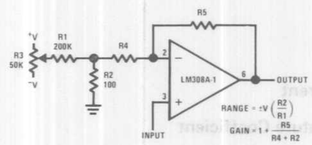
Offset balancing the LM308A-1 can be a problem since there is no easy offset adjustment incorporated into the circuit. These devices are selected for low drift with no offset adjustment to the internal circuitry, so any change of the internal currents will change the drift – probably for the worse. Offset adjustment must be done at the input. The three most commonly needed circuits are shown here.

Testing low drift amplifiers is also difficult. Standard drift testing technique such as heating the device in an oven and having the leads available through a connector, thermoprobe, or the soldering iron method – do not work. Thermal gradients cause much greater errors than the amplifier drift. Coupling microvolt signal through connectors is especially bad since the temperature difference across the connector can be 50°C or more. The device under test along with the gain setting resistor should be isothermal. The following circuit will yield good results if well constructed.

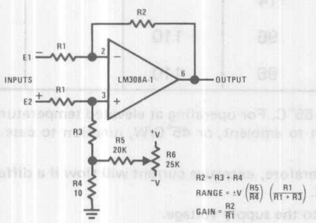
Offset Adjustment for Inverting Amplifiers



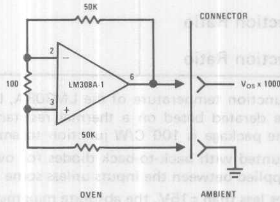
Offset Adjustment for Non-Inverting Amplifiers



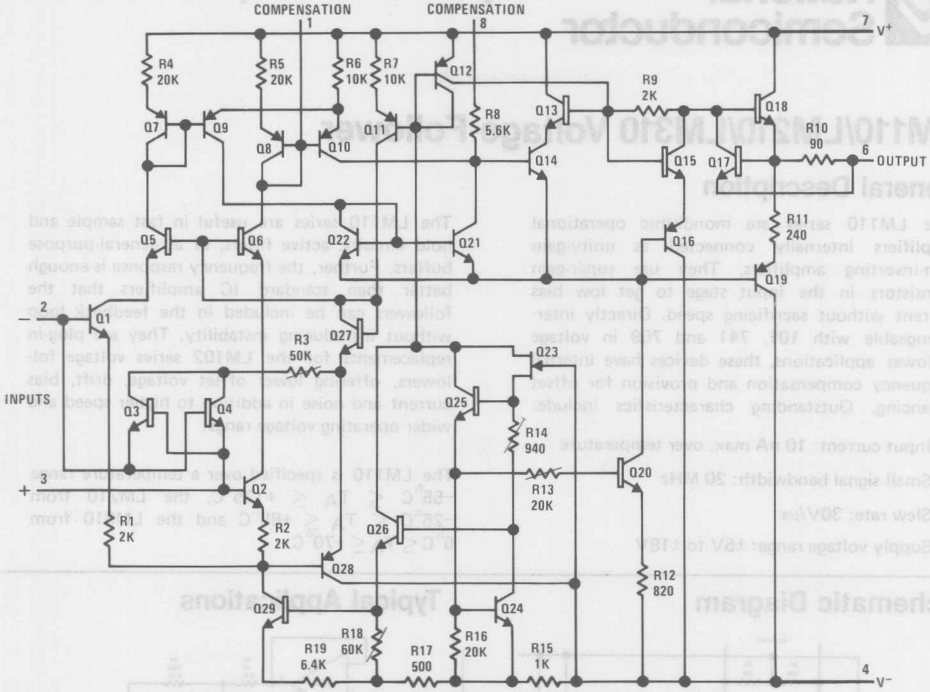
Offset Adjustment for Differential Amplifiers



Drift Measurement Circuit



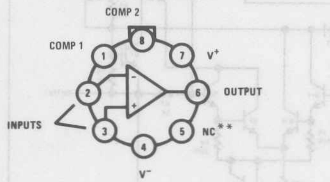
Schematic Diagram*



*Pin connections shown on schematic diagram refer to TO-5 package.

Connection Diagrams

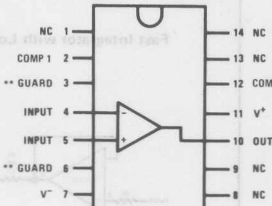
Metal Can Package



Order Number LM108AH, LM208AH, LM308AH, LM308AH-1 or LM308AH-2
See NS Package H08C

**Unused pin (no internal connection) to allow for input anti-leakage guard ring on printed circuit board layout.

Dual-In-Line Package

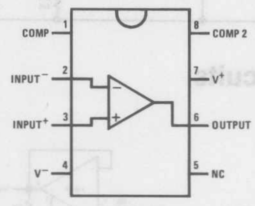


Note: Pin 7 connected to bottom of package.

TOP VIEW

Order Number LM108AJ, LM208AJ, or LM308AJ
See NS Package J14A

Dual-In-Line Package



TOP VIEW

Order Number LM108AJ-8, LM208AJ-8 or LM308AJ-8
See NS Package J08A
Order Number LM208AN or LM308AN
See NS Package N08B

National Semiconductor

Operational Amplifiers/Buffers

LM110/LM210/LM310 Voltage Follower

General Description

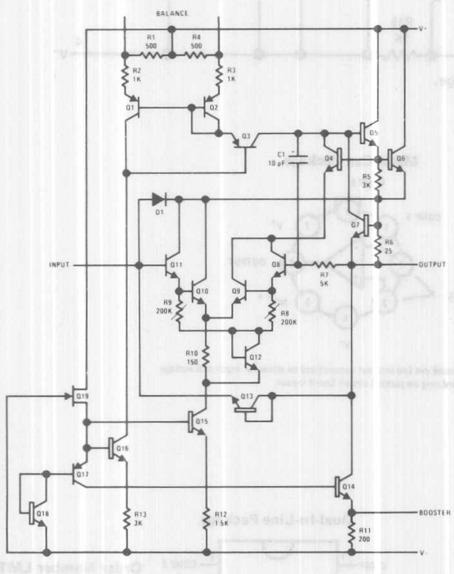
The LM110 series are monolithic operational amplifiers internally connected as unity-gain non-inverting amplifiers. They use super-gain transistors in the input stage to get low bias current without sacrificing speed. Directly interchangeable with 101, 741 and 709 in voltage follower applications, these devices have internal frequency compensation and provision for offset balancing. Outstanding characteristics include:

- Input current: 10 nA max. over temperature
- Small signal bandwidth: 20 MHz
- Slew rate: 30V/μs
- Supply voltage range: ±5V to ±18V

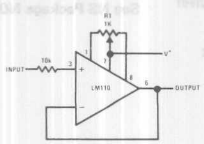
The LM110 series are useful in fast sample and hold circuits, active filters, or as general-purpose buffers. Further, the frequency response is enough better than standard IC amplifiers that the followers can be included in the feedback loop without introducing instability. They are plug-in replacements for the LM102 series voltage followers, offering lower offset voltage, drift, bias current and noise in addition to higher speed and wider operating voltage range.

The LM110 is specified over a temperature range $-55°C \leq T_A \leq +125°C$, the LM210 from $-25°C \leq T_A \leq +85°C$ and the LM310 from $0°C \leq T_A \leq +70°C$.

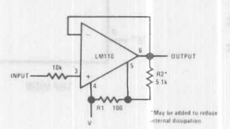
Schematic Diagram



Auxiliary Circuits

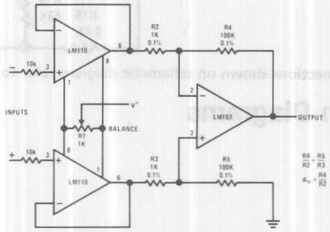


Offset Balancing Circuit

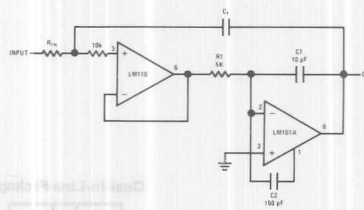


Increasing Negative Swing Under Load

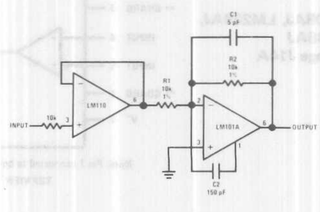
Typical Applications



Differential Input Instrumentation Amplifier



Fast Integrator with Low Input Current



Fast Inverting Amplifier with High Input Impedance

Absolute Maximum Ratings

Supply Voltage		±18V
Power Dissipation (Note 1)		500 mW
Input Voltage (Note 2)		±15V
Output Short Circuit Duration (Note 3)		Indefinite
Operating Temperature Range	LM110	−55°C to 125°C
	LM210	−25°C to 85°C
	LM310	0°C to +70°C
Storage Temperature Range		−65°C to 150°C
Lead Temperature (Soldering, 10 sec)		300°C

Electrical Characteristics (Note 4)

PARAMETER	CONDITIONS	LM110			LM210			LM310			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$		1.5	4.0		1.5	4.0		2.5	7.5	mV
Input Bias Current	$T_A = 25°C$		1.0	3.0		1.0	3.0		2.0	7.0	nA
Input Resistance	$T_A = 25°C$	10^{10}	10^{12}		10^{10}	10^{12}		10^{10}	10^{12}		Ω
Input Capacitance			1.5			1.5			1.5		pF
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = ±15V$, $V_{OUT} = ±10V$, $R_L = 8\ k\Omega$	0.999	0.9999		0.999	0.9999		0.999	0.9999		V/V
Output Resistance	$T_A = 25°C$		0.75	2.5		0.75	2.5		0.75	2.5	Ω
Supply Current	$T_A = 25°C$		3.9	5.5		3.9	5.5		3.9	5.5	mA
Input Offset Voltage				6.0			6.0			10	mV
Offset Voltage Temperature Drift	$-55°C \leq T_A \leq +85°C$		6			6					μV/°C
	$T_A = 125°C$		12			12					μV/°C
	$0°C \leq T_A \leq +70°C$								10		μV/°C
Input Bias Current				10			10			10	nA
Large Signal Voltage Gain	$V_S = ±15V$, $V_{OUT} = ±10V$, $R_L = 10\ k\Omega$	0.999			0.999			0.999			V/V
Output Voltage Swing (Note 5)	$V_S = ±15V$, $R_L = 10\ k\Omega$	±10			±10			±10			V
Supply Current	$T_A = 125°C$		2.0	4.0		2.0	4.0				mA
Supply Voltage Rejection Ratio	$±5V \leq V_S \leq ±18V$	70	80		70	80		70	80		dB

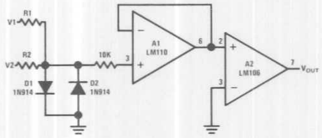
Note 1: The maximum junction temperature of the LM110 is 150°C, of the LM210 is 100°C, and of the LM310 is 85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

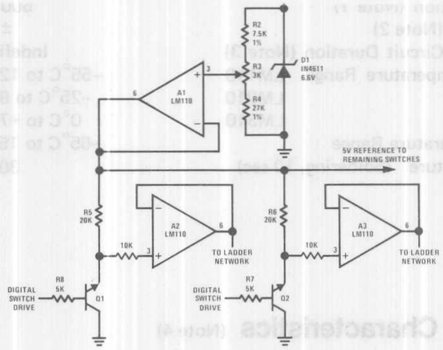
Note 3: Continuous short circuit for the LM110 and LM210 is allowed for case temperatures to 125°C and ambient temperatures to 70°C, and for the LM310, 70°C case temperature or 55°C ambient temperature. It is necessary to insert a resistor greater than 2kΩ in series with the input when the amplifier is driven from low impedance sources to prevent damage when the output is shorted.

Note 4: These specifications apply for $±5V \leq V_S \leq ±18V$ and $-55°C \leq T_A \leq 125°C$ for the LM110, $-25°C \leq T_A \leq 85°C$ for the LM210, and $0°C \leq T_A \leq 70°C$ for the LM310 unless otherwise specified.

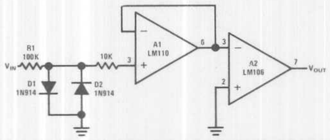
Note 5: Increased output swing under load can be obtained by connecting an external resistor between the booster and V^- terminals. See curve.



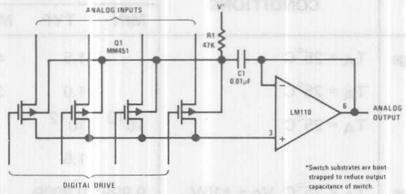
Comparator for Signals of Opposite Polarity



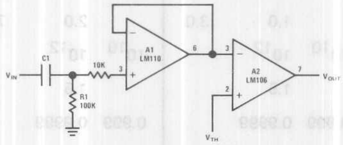
Driver for A/D Ladder Network



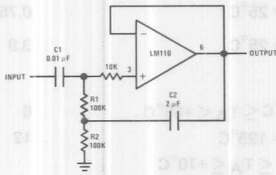
Zero Crossing Detector



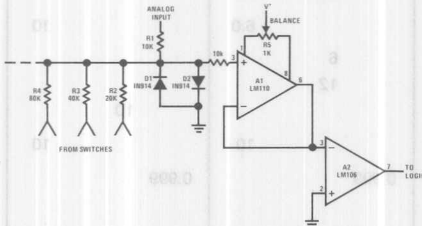
Buffer for Analog Switch*



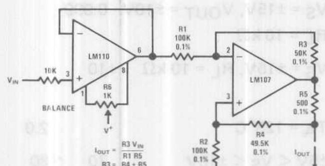
Comparator for AC Coupled Signals



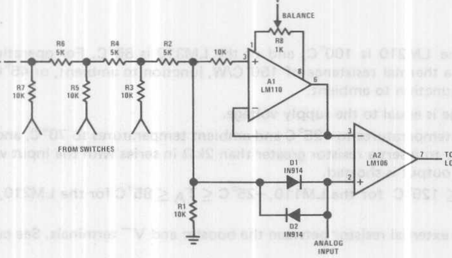
High Input Impedance AC Amplifier



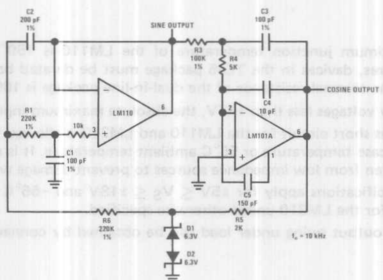
Comparator for A/D Converter Using a Binary-Weighted Network



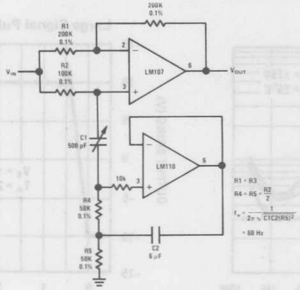
Bilateral Current Source



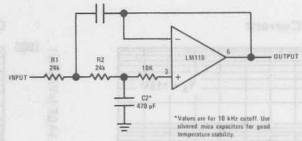
Comparator for A/D Converter Using a Ladder Network



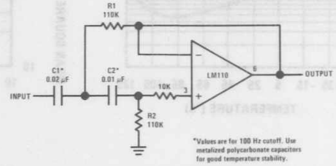
Sine Wave Oscillator



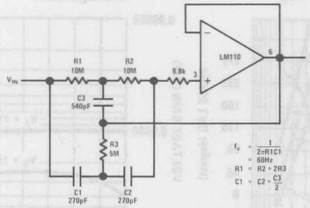
Tunable Notch Filter



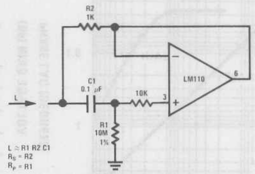
Low Pass Active Filter



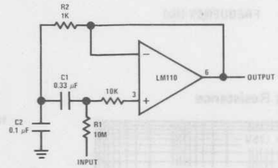
High Pass Active Filter



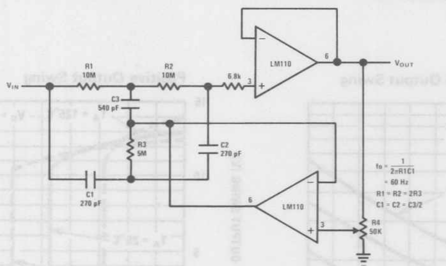
High Q Notch Filter



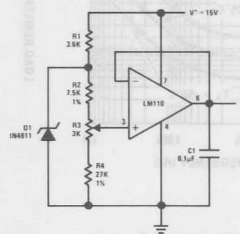
Simulated Inductor



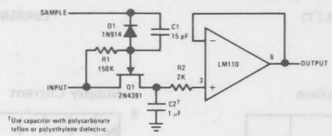
Bandpass Filter



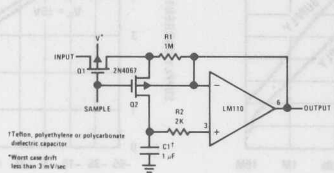
Adjustable Q Notch Filter



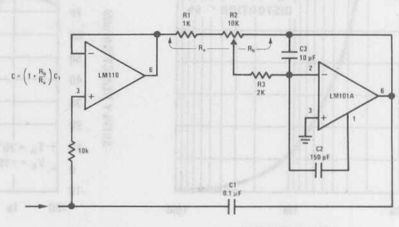
Buffered Reference Source



Sample and Hold



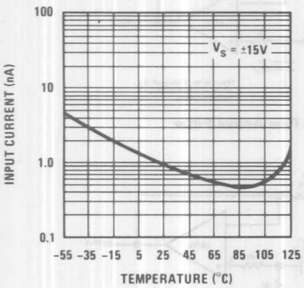
Low Drift Sample and Hold*



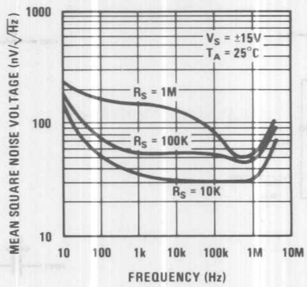
Variable Capacitance Multiplier

Typical Performance Characteristics (LM110/LM210)

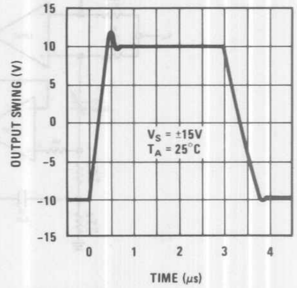
Input Current



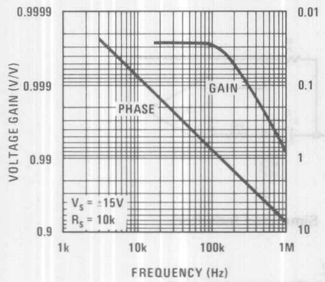
Output Noise Voltage



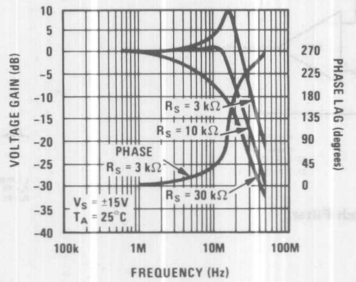
Large Signal Pulse Response



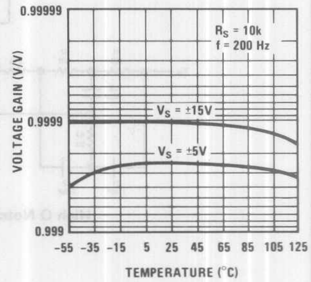
Voltage Gain and Phase Lag



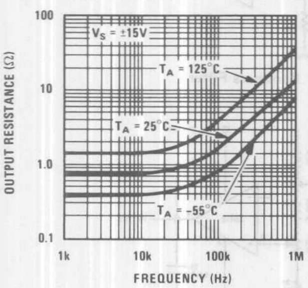
Voltage Gain and Phase Lag



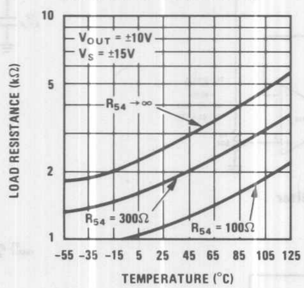
Voltage Gain



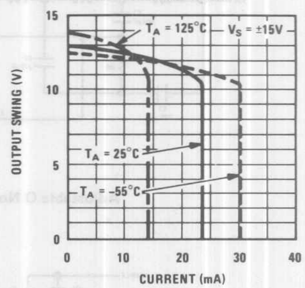
Output Resistance



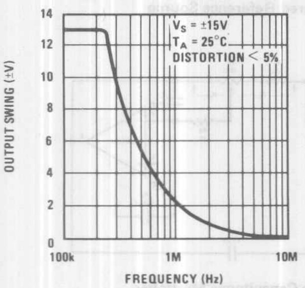
Symmetrical Output Swing



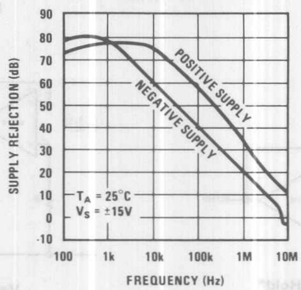
Positive Output Swing



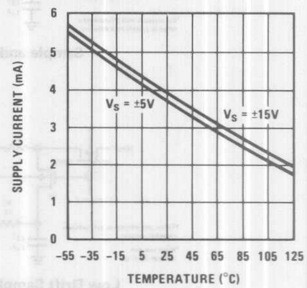
Large Signal Frequency Response



Power Supply Rejection

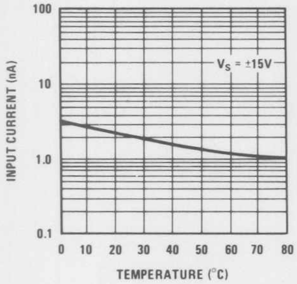


Supply Current

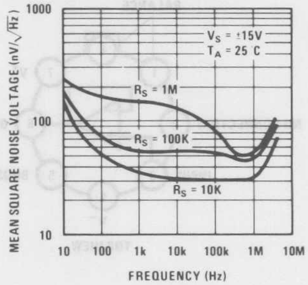


Typical Performance Characteristics (LM310)

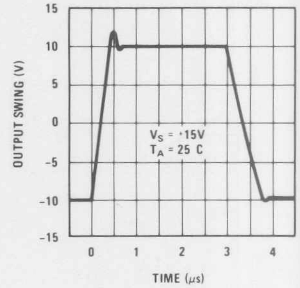
Input Current



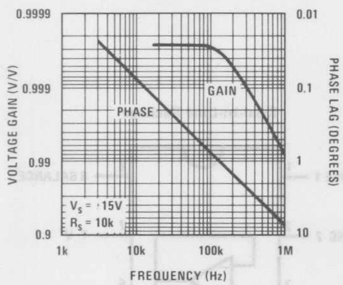
Output Noise Voltage



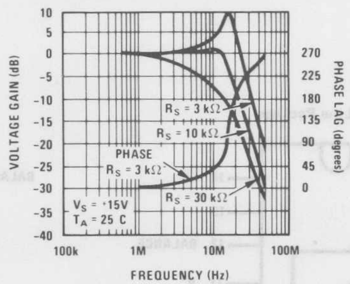
Large Signal Pulse Response



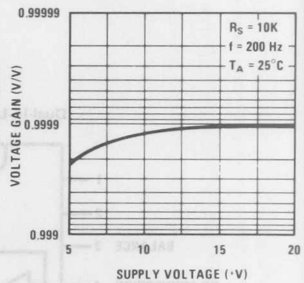
Voltage Gain and Phase Lag



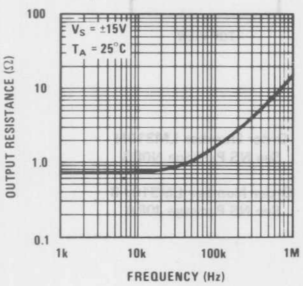
Voltage Gain and Phase Lag



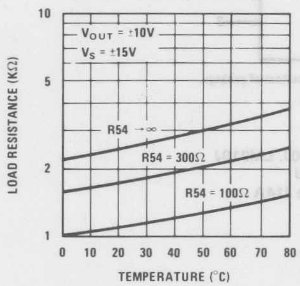
Voltage Gain



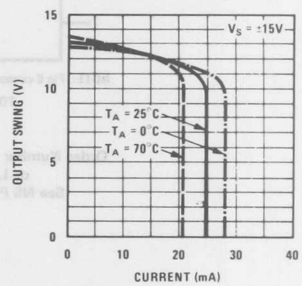
Output Resistance



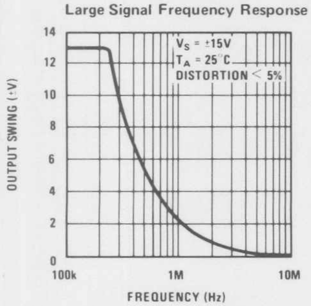
Symmetrical Output Swing



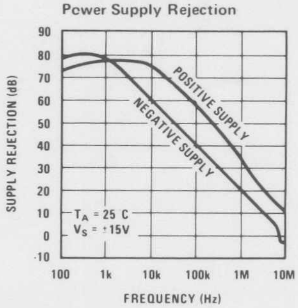
Positive Output Swing



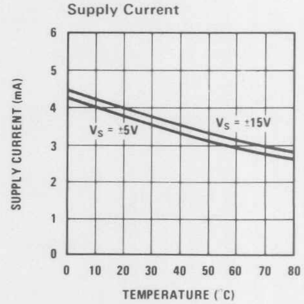
Large Signal Frequency Response



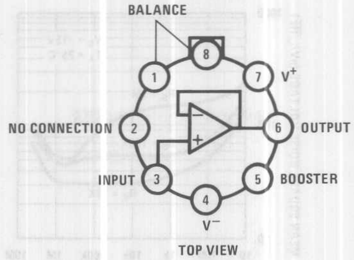
Power Supply Rejection



Supply Current

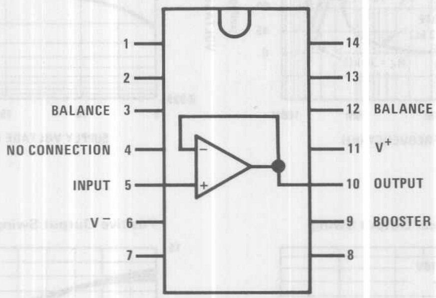


Metal Can Package



Order Number LM110H, LM210H
or LM310H
See NS Package H08C

Dual-In-Line Package

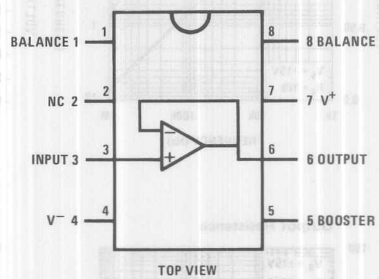


NOTE: Pin 6 connected to bottom of package.

TOP VIEW

Order Number LM110J, LM210J
or LM310J
See NS Package J14A

Dual-In-Line Package



Order Number LM310N
See NS Package N08B

Order Number LM310J-8
See NS Package J08A

National Semiconductor

Operational Amplifiers/Buffers

LM112/LM212/LM312 Operational Amplifiers

General Description

The LM112 series are micropower operational amplifiers with very low offset-voltage and input-current errors—at least a factor of ten better than FET amplifiers over a −55°C to +125°C temperature range. Similar to the LM108 series, that also use supergain transistors, they differ in that they include internal frequency compensation and have provisions for offset adjustment with a single potentiometer.

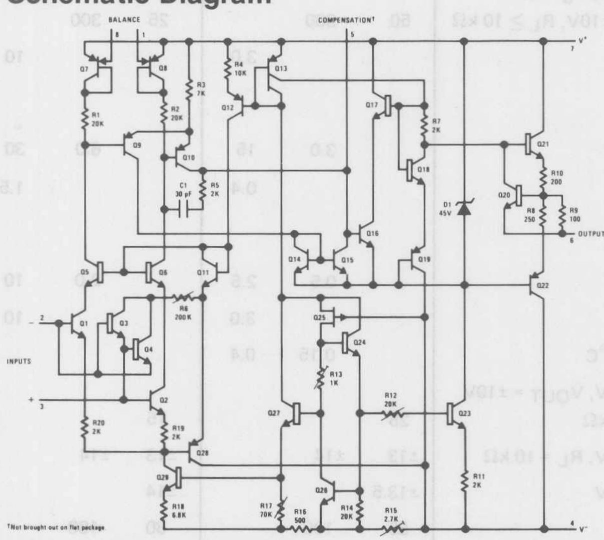
These amplifiers will operate on supply voltages of ±2V to ±20V, drawing a quiescent current of only 300 μA. Performance is not appreciably affected over this range of voltages, so operation from unregulated power sources is easily accomplished. They can also be run from a single supply like the 5V used for digital circuits. Some noteworthy features are:

- Maximum input bias current of 3 nA over temperature
- Offset current less than 400 pA over temperature
- Low noise
- Guaranteed drift specifications

The LM112 series are the first IC amplifiers to improve reliability by including overvoltage protection for the MOS compensation capacitor. Without this feature, IC's have been known to suffer catastrophic failure caused by short-duration overvoltage spikes on the supplies. Unlike other internally-compensated IC amplifiers, it is possible to overcompensate with an external capacitor to increase stability margin.

The LM212 is identical to the LM112, except that the LM212 has its performance guaranteed over a −25°C to 85°C temperature range instead of −55°C to 125°C. The LM312 is guaranteed over a 0°C to 70°C temperature range.

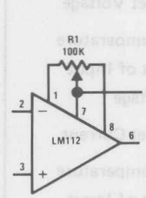
Schematic Diagram **



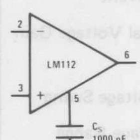
**Pin connections shown are for metal can.

Auxiliary Circuits **

Offset Balancing

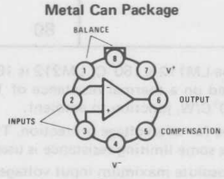


Overcompensation for Greater Stability Margin



Connection Diagram

Metal Can Package



Order Number LM112H, LM212H, or LM312H
See NS Package H08C

Absolute Maximum Ratings

	LM112/LM212	LM312
Supply Voltage	±20V	±18V
Power Dissipation (Note 1)	500 mW	500 mW
Differential Input Current (Note 2)	±10 mA	±10 mA
Input Voltage (Note 3)	±15V	±15V
Output Short-Circuit Duration	Indefinite	Indefinite
Operating Temperature Range		0°C to +70°C
LM112	−55°C to +125°C	
LM212	−25°C to +85°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

Electrical Characteristics (Note 4)

PARAMETER	CONDITIONS	LM112/LM212			LM312			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25^\circ C$		0.7	2.0		2.0	7.5	mV
Input Offset Current	$T_A = 25^\circ C$		0.05	0.2		0.2	1	nA
Input Bias Current	$T_A = 25^\circ C$		0.8	2.0		1.5	7	nA
Input Resistance	$T_A = 25^\circ C$	30	70		10	40		MΩ
Supply Current	$T_A = 25^\circ C$		0.3	0.6		0.3	0.8	mA
Large Signal Voltage Gain	$T_A = 25^\circ C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 10\ k\Omega$	50	300		25	300		V/mV
Input Offset Voltage				3.0			10	mV
Average Temperature Coefficient of Input Offset Voltage			3.0	15		6.0	30	µV/°C
Input Offset Current				0.4			1.5	nA
Average Temperature Coefficient of Input Offset Current			0.5	2.5		2.0	10	pA/°C
Input Bias Current				3.0			10	nA
Supply Current	$T_A = 125^\circ C$		0.15	0.4				mA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 10\ k\Omega$	25			15			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$	±13	±14		±13	±14		V
Input Voltage Range	$V_S = \pm 15V$	±13.5			±14			V
Common-Mode Rejection Ratio		85	100		80	100		dB
Supply Voltage Rejection Ratio		80	96		80	96		dB

Note 1: The maximum junction temperature of the LM112 is 150°C, LM212 is 100°C and LM312 is 85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

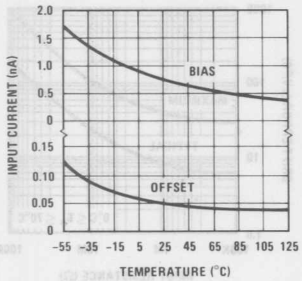
Note 2: The inputs are shunted with shunt diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

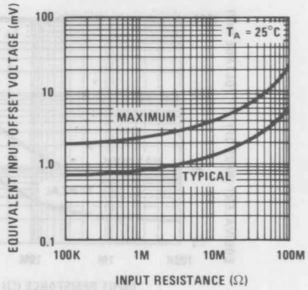
Note 4: These specifications apply for $\pm 5V \leq V_S \leq \pm 20V$ and $-55^\circ C \leq T_A \leq +125^\circ C$ (LM112), $-25^\circ C \leq T_A \leq +85^\circ C$ (LM212), $\pm 5V \leq V_S \leq \pm 15V$ and $0^\circ C \leq T_A \leq +70^\circ C$ (LM312) unless otherwise noted.

Typical Performance Characteristics LM112/LM212

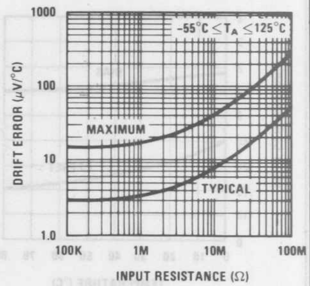
Input Currents



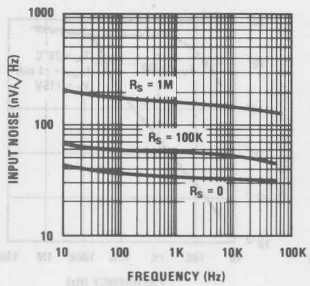
Offset Error



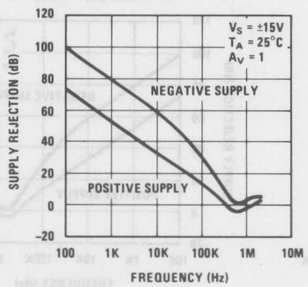
Drift Error



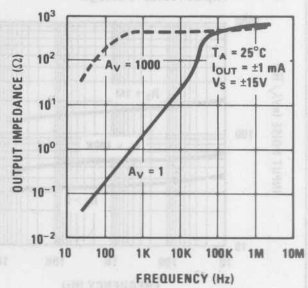
Input Noise Voltage



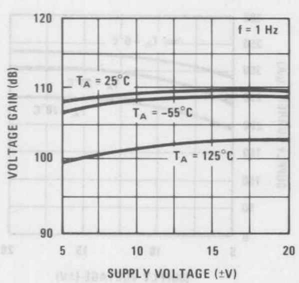
Power Supply Rejection



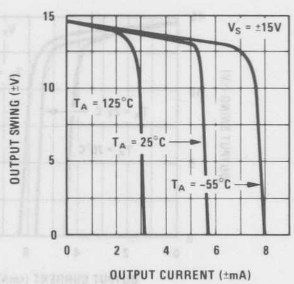
Closed Loop Output Impedance



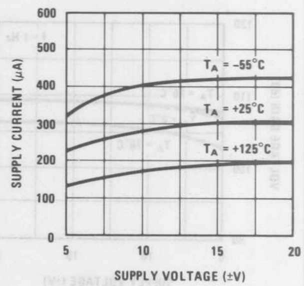
Voltage Gain



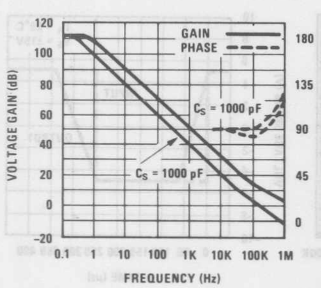
Output Swing



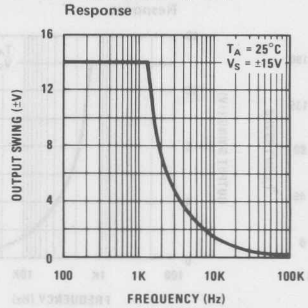
Supply Current



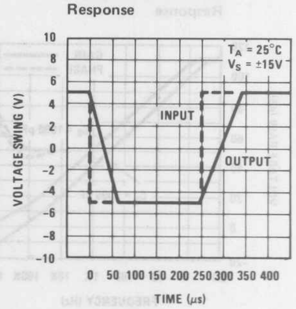
Open Loop Frequency Response



Large Signal Frequency Response



Voltage Follower Pulse Response



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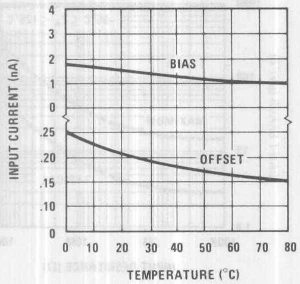
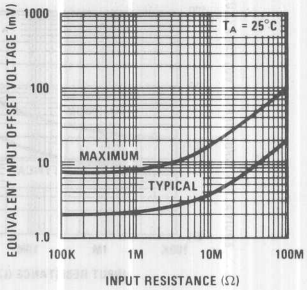
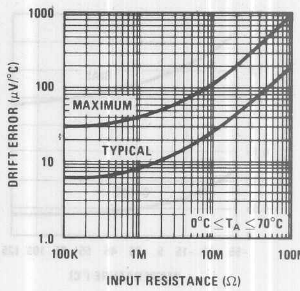
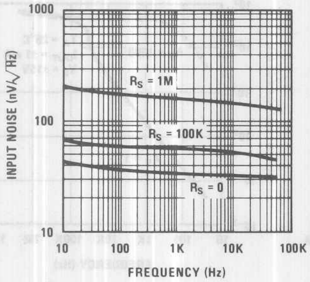


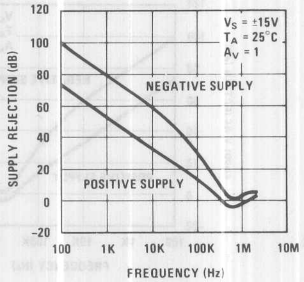




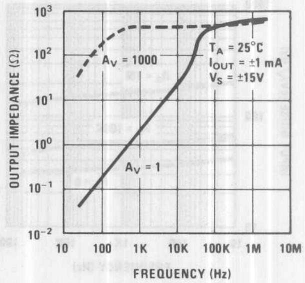
Input Noise Voltage



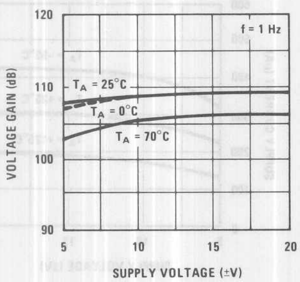
Power Supply Rejection



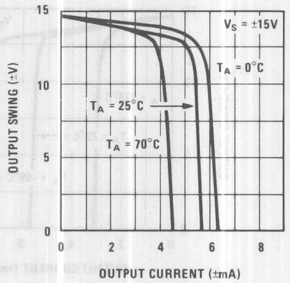
Closed Loop Output Impedance



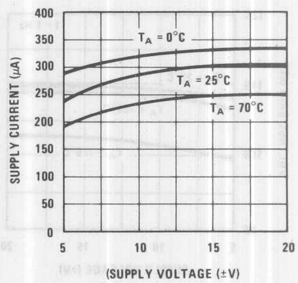
Voltage Gain



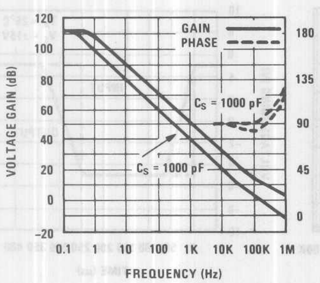
Output Swing



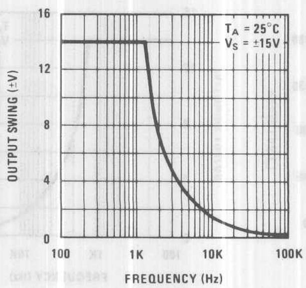
Supply Current



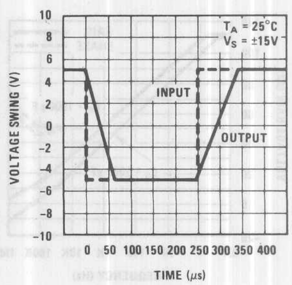
Open Loop Frequency Response



Large Signal Frequency Response



Voltage Follower Pulse Response



National Semiconductor

Operational Amplifiers/Buffers

LM118/LM218/LM318 Operational Amplifiers

General Description

The LM118 series are precision high speed operational amplifiers designed for applications requiring wide bandwidth and high slew rate. They feature a factor of ten increase in speed over general purpose devices without sacrificing DC performance.

Features

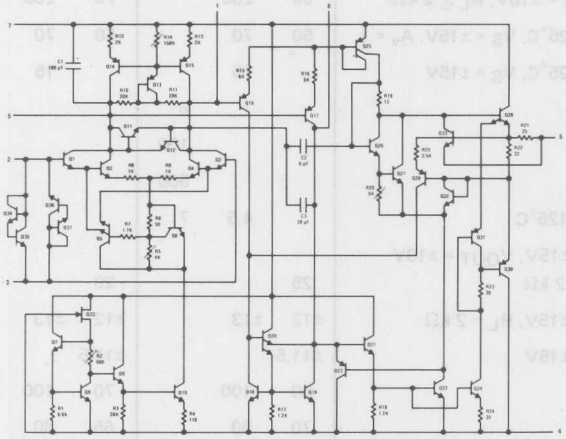
- 15 MHz small signal bandwidth
- Guaranteed 50V/μs slew rate
- Maximum bias current of 250 nA
- Operates from supplies of ±5V to ±20V
- Internal frequency compensation
- Input and output overload protected
- Pin compatible with general purpose op amps

The LM118 series has internal unity gain frequency compensation. This considerably simplifies its application since no external components are necessary for operation. However, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. For inverting applications, feedforward compensation will boost the slew rate to over 150V/μs and almost double the bandwidth. Overcompensation can be used with the amplifier for greater stability when maximum bandwidth is not needed. Further, a single capacitor can be added to reduce the 0.1% settling time to under 1 μs.

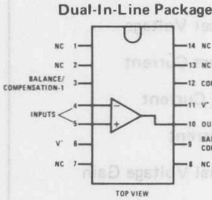
The high speed and fast settling time of these op amps make them useful in A/D converters, oscillators, active filters, sample and hold circuits, or general purpose amplifiers. These devices are easy to apply and offer an order of magnitude better AC performance than industry standards such as the LM709.

The LM218 is identical to the LM118 except that the LM218 has its performance specified over a −25°C to +85°C temperature range. The LM318 is specified from 0°C to +70°C.

Schematic and Connection Diagrams

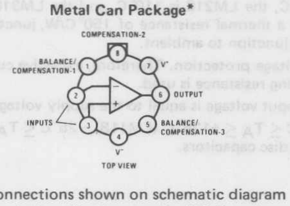


Dual-In-Line Package



Order Number LM118J, LM218J or LM318J
See NS Package J14A

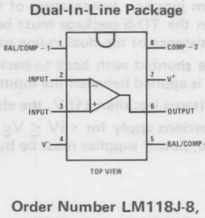
Metal Can Package*



*Pin connections shown on schematic diagram and typical applications are for TO-5 package.

Order Number LM118H, LM218H or LM318H
See NS Package H08C

Dual-In-Line Package



Order Number LM118J-8, LM218J-8 or LM318J-8
See NS Package J08A
Order Number LM318N
See NS Package N08B

Absolute Maximum Ratings

Supply Voltage	±20V
Power Dissipation (Note 1)	500 mW
Differential Input Current (Note 2)	±10 mA
Input Voltage (Note 3)	±15V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
LM118	$-55^\circ C$ to $+125^\circ C$
LM218	$-25^\circ C$ to $+85^\circ C$
LM318	$0^\circ C$ to $+70^\circ C$
Storage Temperature Range	$-65^\circ C$ to $+150^\circ C$
Lead Temperature (Soldering, 10 seconds)	$300^\circ C$

Electrical Characteristics (Note 4)

PARAMETER	CONDITIONS	LM118/LM218 MIN	LM118/LM218 TYP	LM118/LM218 MAX	LM318 MIN	LM318 TYP	LM318 MAX	UNITS
Input Offset Voltage	$T_A = 25^\circ C$		2	4		4	10	mV
Input Offset Current	$T_A = 25^\circ C$		6	50		30	200	nA
Input Bias Current	$T_A = 25^\circ C$		120	250		150	500	nA
Input Resistance	$T_A = 25^\circ C$	1	3		0.5	3		MΩ
Supply Current	$T_A = 25^\circ C$		5	8		5	10	mA
Large Signal Voltage Gain	$T_A = 25^\circ C$, $V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 2\ k\Omega$	50	200		25	200		V/mV
Slew Rate	$T_A = 25^\circ C$, $V_S = \pm 15V$, $A_V = 1$	50	70		50	70		V/µs
Small Signal Bandwidth	$T_A = 25^\circ C$, $V_S = \pm 15V$		15			15		MHz
Input Offset Voltage				6			15	mV
Input Offset Current				100			300	nA
Input Bias Current				500			750	nA
Supply Current	$T_A = 125^\circ C$		4.5	7				
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 2\ k\Omega$	25			20			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 2\ k\Omega$	±12	±13		±12	±13		V
Input Voltage Range	$V_S = \pm 15V$	±11.5			±11.5			V
Common-Mode Rejection Ratio		80	100		70	100		dB
Supply Voltage Rejection Ratio		70	80		65	80		dB

Note 1: The maximum junction temperature of the LM118 is 150°C, the LM218 is 110°C, and the LM318 is 110°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

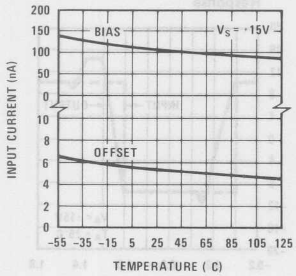
Note 2: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

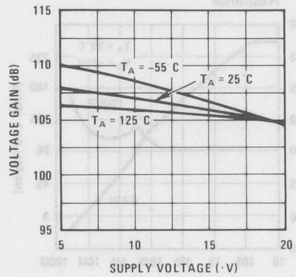
Note 4: These specifications apply for $\pm 5V \leq V_S \leq \pm 20V$ and $-55^\circ C \leq T_A \leq +125^\circ C$, (LM118), $-25^\circ C \leq T_A \leq +85^\circ C$ (LM218), and $0^\circ C \leq T_A \leq +70^\circ C$ (LM318). Also, power supplies must be bypassed with 0.1µF disc capacitors.

Typical Performance Characteristics LM118, LM218

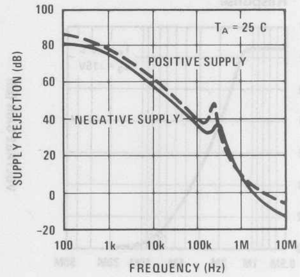
Input Current



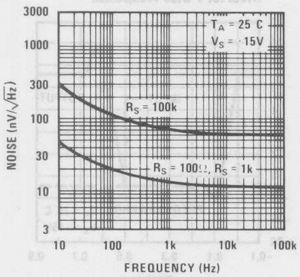
Voltage Gain



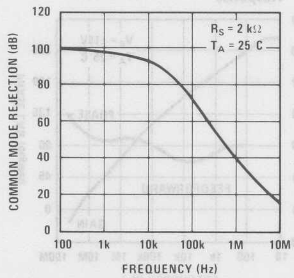
Power Supply Rejection



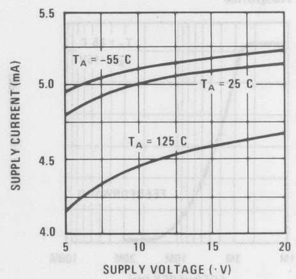
Input Noise Voltage



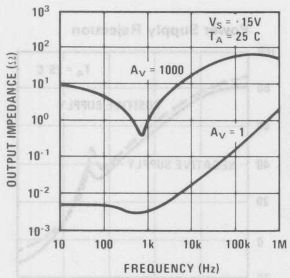
Common Mode Rejection



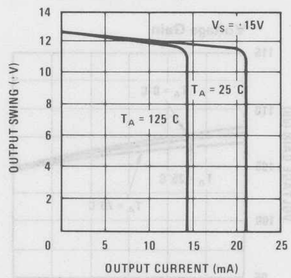
Supply Current



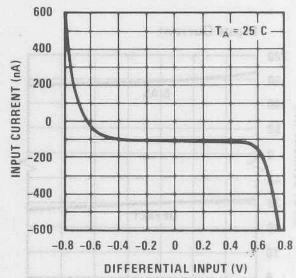
Closed Loop Output Impedance



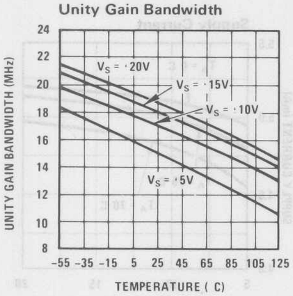
Current Limiting



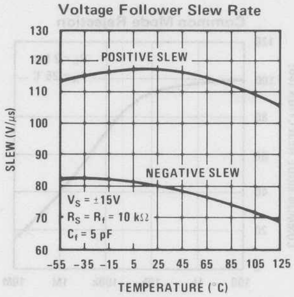
Input Current



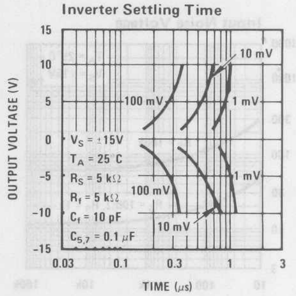
Unity Gain Bandwidth



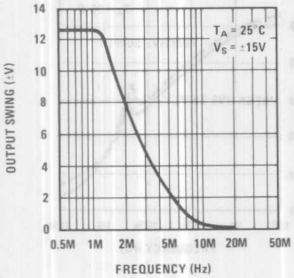
Voltage Follower Slew Rate



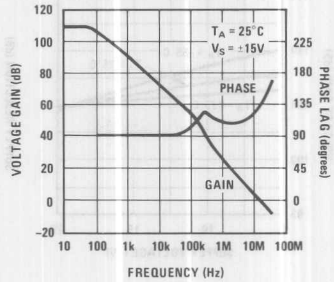
Inverter Settling Time



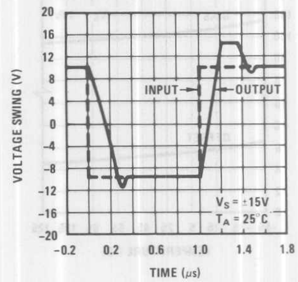
Large Signal Frequency Response



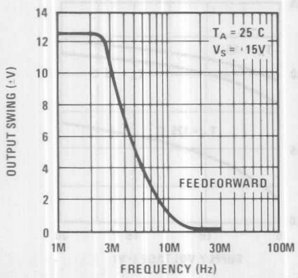
Open Loop Frequency Response



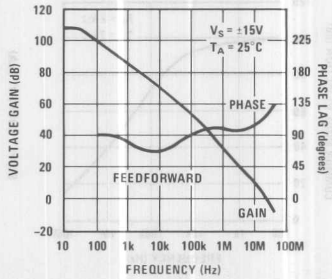
Voltage Follower Pulse Response



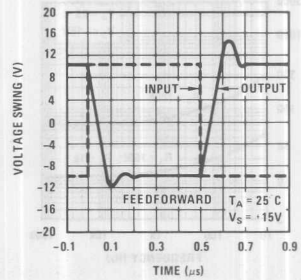
Large Signal Frequency Response



Open Loop Frequency Response

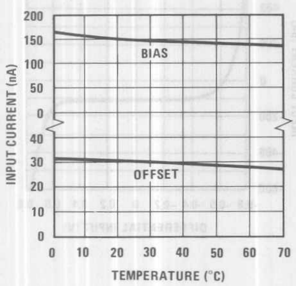


Inverter Pulse Response

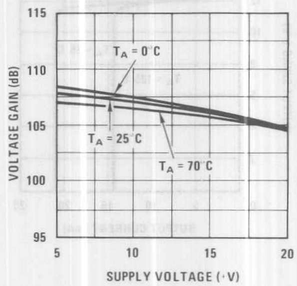


Typical Performance Characteristics LM318

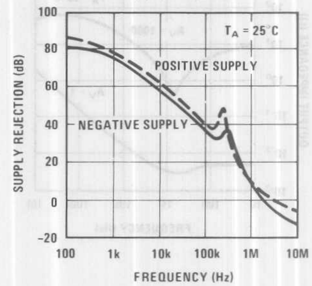
Input Current



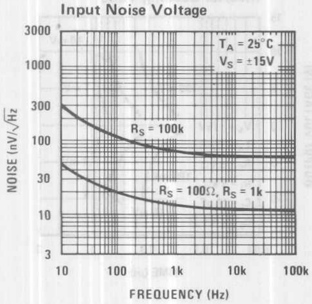
Voltage Gain



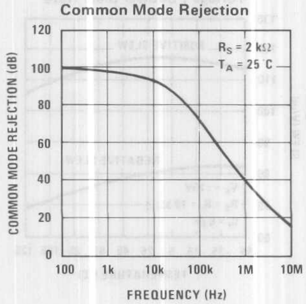
Power Supply Rejection



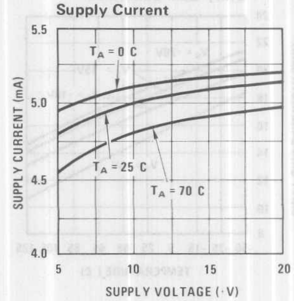
Input Noise Voltage



Common Mode Rejection

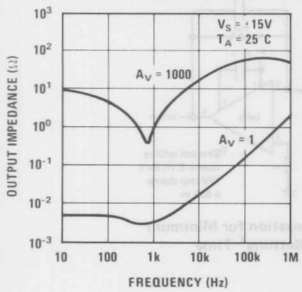


Supply Current

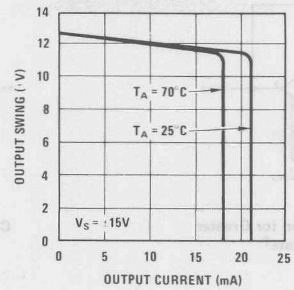


Typical Performance Characteristics LM318 (Continued)

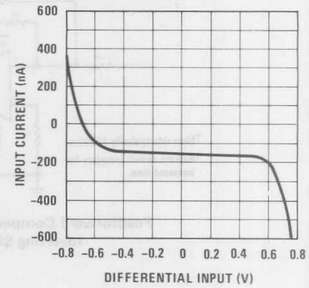
Closed Loop Output Impedance



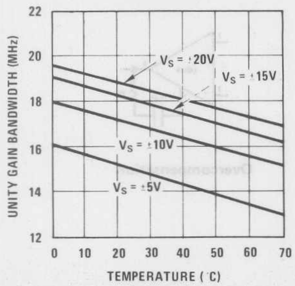
Current Limiting



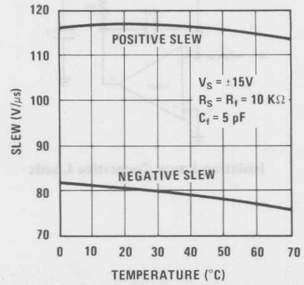
Input Current



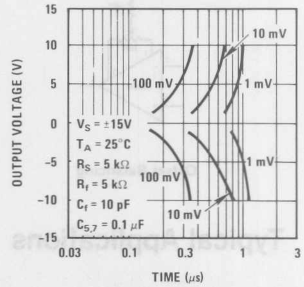
Unit Gain Bandwidth



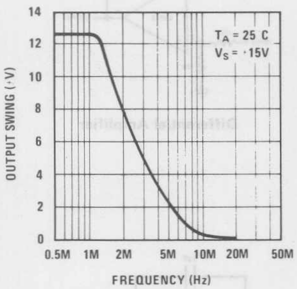
Voltage Follower Slew Rate



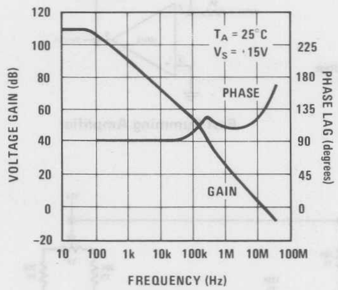
Inverter Settling Time



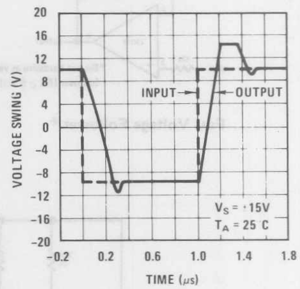
Large Signal Frequency Response



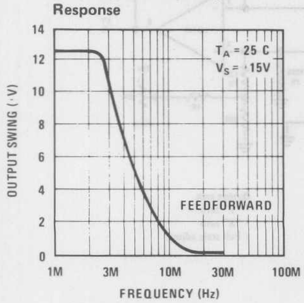
Open Loop Frequency Response



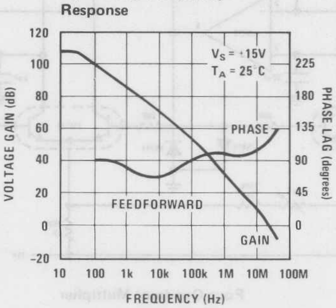
Voltage Follower Pulse Response



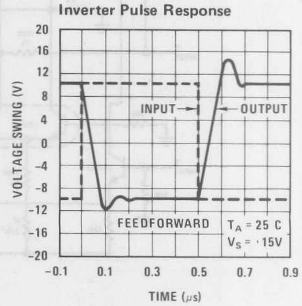
Large Signal Frequency Response



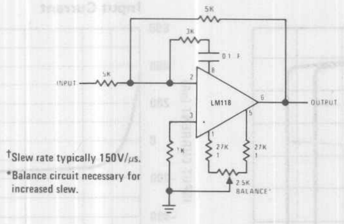
Open Loop Frequency Response



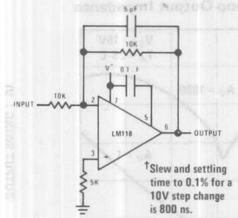
Inverter Pulse Response



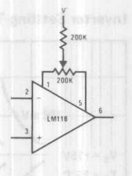
Auxiliary Circuits



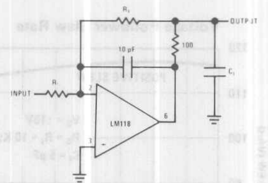
Feedforward Compensation for Greater Inverting Slew Rate†



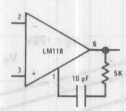
Compensation for Minimum Settling† Time



Offset Balancing

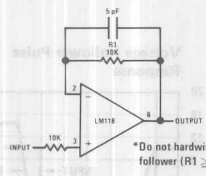


Isolating Large Capacitive Loads



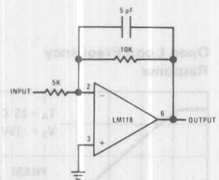
Overcompensation

Typical Applications

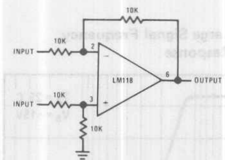


*Do not hardwire as voltage follower (R1 ≥ 5 kΩ)

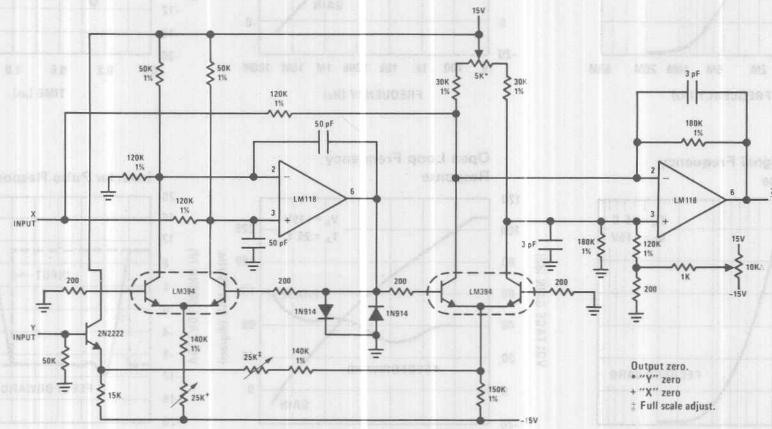
Fast Voltage Follower *



Fast Summing Amplifier

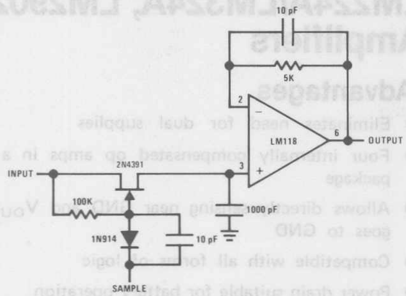


Differential Amplifier

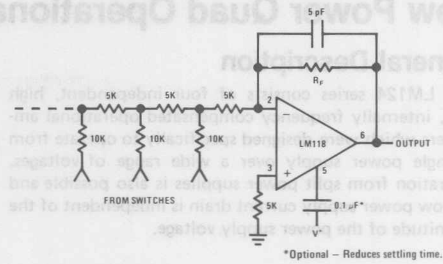


Four Quadrant Multiplier

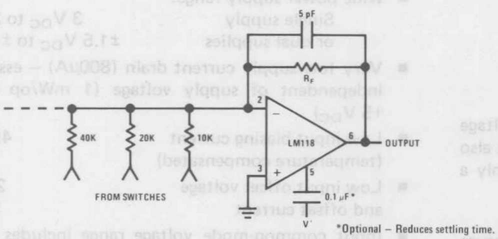
Typical Applications (Continued)



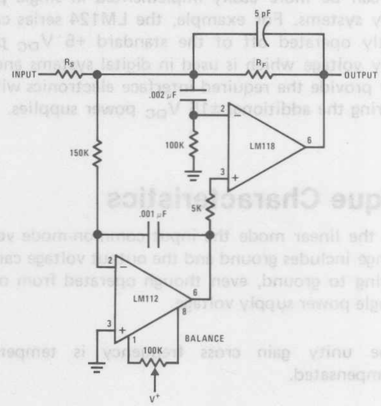
Fast Sample and Hold



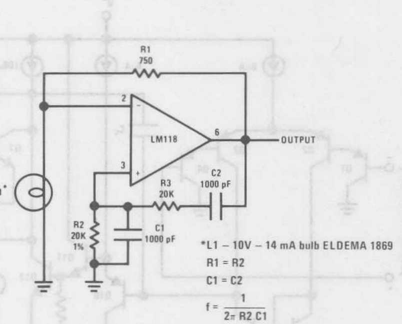
D/A Converter Using Ladder Network



D/A Converter Using Binary Weighted Network

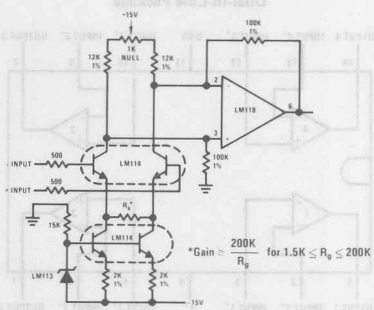


Fast Summing Amplifier with Low Input Current



Wein Bridge Sine Wave Oscillator

$$f = \frac{1}{2\pi\ R2\ C1}$$



Instrumentation Amplifier

LM124/LM224/LM324, LM124A/LM224A/LM324A, LM2902
Low Power Quad Operational Amplifiers

General Description

The LM124 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124 series can be directly operated off of the standard +5 V_{DC} power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15 V_{DC} power supplies.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
- The unity gain cross frequency is temperature compensated.
- The input bias current is also temperature compensated.

Advantages

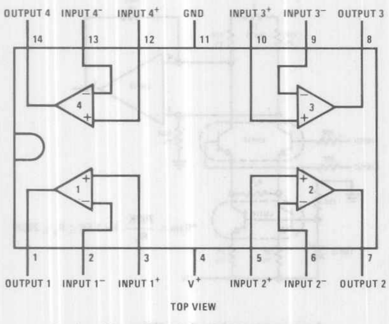
- Eliminates need for dual supplies
- Four internally compensated op amps in a single package
- Allows directly sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

Features

- Internally frequency compensated for unity gain
- Large dc voltage gain 100 dB
- Wide bandwidth (unity gain) 1 MHz
  (temperature compensated)
- Wide power supply range:
  Single supply 3 V_{DC} to 30 V_{DC}
  or dual supplies ±1.5 V_{DC} to ±15 V_{DC}
- Very low supply current drain (800μA) – essentially independent of supply voltage (1 mW/op amp at +5 V_{DC})
- Low input biasing current 45 nA_{DC}
  (temperature compensated)
- Low input offset voltage 2 mV_{DC}
  and offset current 5 nA_{DC}
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0 V_{DC} to V^+ – 1.5 V_{DC}

Connection Diagram

Dual-In-Line Package

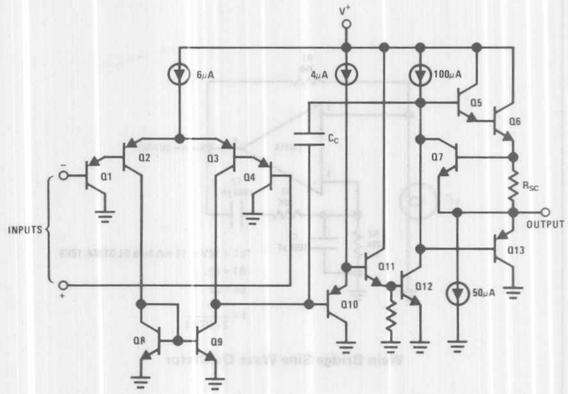


TOP VIEW

Order Number LM124J, LM124AJ, LM224J, LM224AJ, LM324J, LM324AJ or LM2902J
See NS Package J14A

Order Number LM324N, LM324AN or LM2902N
See NS Package N14A

Schematic Diagram (Each Amplifier)



Absolute Maximum Ratings

	LM124/LM224/LM324 LM124A/LM224A/LM324A	LM2902
Supply Voltage, V^+	32 V_{DC} or ±16 V_{DC}	26 V_{DC} or ±13 V_{DC}
Differential Input Voltage	32 V_{DC}	26 V_{DC}
Input Voltage	−0.3 V_{DC} to +26 V_{DC}	−0.3 V_{DC} to +26 V_{DC}
Power Dissipation (Note 1)		
Molded DIP	570 mW	570 mW
Cavity DIP	900 mW	
Flat Pack	800 mW	
Output Short-Circuit to GND (One Amplifier) (Note 2) $V^+ \leq 15$ V_{DC} and T_A = 25°C	Continuous	Continuous

	LM124/LM224/LM324 LM124A/LM224A/LM324A	LM2902
Input Current ($V_{IN} < -0.3$ V_{DC}) (Note 3)	50 mA	50 mA
Operating Temperature Range		−40°C to +85°C
LM324/LM324A	0°C to +70°C	
LM224/LM224A	−25°C to +85°C	
LM124/LM124A	−55°C to +125°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

Electrical Characteristics (V^+ = +5.0 V_{DC}, Note 4)

PARAMETER	CONDITIONS	LM124A			LM224A			LM324A			LM124/LM224			LM324			LM2902			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	T_A = 25°C, (Note 5)		1	2		1	3		2	3		±2	±5		±2	±7		±2	±7	mV_{DC}
Input Bias Current (Note 6)	$I_{IN(+)}$ or $I_{IN(-)}$, T_A = 25°C		20	50		40	80		45	100		45	150		45	250		45	250	nA_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, T_A = 25°C		2	10		2	15		5	30		±3	±30		±5	±50		±5	±50	nA_{DC}
Input Common-Mode Voltage Range (Note 7)	V^+ = 30 V_{DC}, T_A = 25°C	0		V^+−1.5	0		V^+−1.5	0		V^+−1.5	0		V^+−1.5	0		V^+−1.5	0		V^+−1.5	V_{DC}
Supply Current	$R_L = \infty$, V_{CC} = 30V, (LM2902 V_{CC} = 26V)		1.5	3		1.5	3		1.5	3		1.5	3		1.5	3		1.5	3	mA_{DC}
	$R_L = \infty$ On All Op Amps Over Full Temperature Range		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2	mA_{DC}
Large Signal Voltage Gain	V^+ = 15 V_{DC} (For Large V_O Swing) $R_L \geq 2$ kΩ, T_A = 25°C	50	100		50	100		25	100		50	100		25	100			100		V/mV
Output Voltage Swing	R_L = 2 kΩ, T_A = 25°C (LM2902 $R_L \geq 10$ kΩ)	0		V^+−1.5	0		V^+−1.5	0		V^+−1.5	0		V^+−1.5	0		V^+−1.5	0		V^+−1.5	V_{DC}
Common-Mode Rejection Ratio	DC, T_A = 25°C	70	85		70	85		65	85		70	85		65	70		50	70		dB
Power Supply Rejection Ratio	DC, T_A = 25°C	65	100		65	100		65	100		65	100		65	100		50	100		dB
Amplifier-to-Amplifier Coupling (Note 8)	f = 1 kHz to 20 kHz, T_A = 25°C (Input Referred)		−120			−120			−120			−120			−120			−120		dB
Output Current																				
Source	V_{IN}^+ = 1 V_{DC}, V_{IN}^- = 0 V_{DC}, V^+ = 15 V_{DC}, T_A = 25°C	20	40		20	40		20	40		20	40		20	40		20	40		mA_{DC}
Sink	V_{IN}^- = 1 V_{DC}, V_{IN}^+ = 0 V_{DC}, V^+ = 15 V_{DC}, T_A = 25°C	10	20		10	20		10	20		10	20		10	20		10	20		mA_{DC}
	V_{IN}^- = 1 V_{DC}, V_{IN}^+ = 0 V_{DC}, T_A = 25°C, V_O = 200 mV_{DC}	12	50		12	50		12	50		12	50		12	50					μA_{DC}
Short Circuit to Ground	T_A = 25°C, (Note 2)		40	60		40	60		40	60		40	60		40	60		40	60	mA_{DC}

Electrical Characteristics (Continued)

PARAMETER	CONDITIONS	LM124A			LM224A			LM324A			LM124/LM224			LM324			LM2902			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	(Note 5)			4			4			5			±7			±9			±10	mV_{DC}
Input Offset Voltage Drift	$R_S = 0\Omega$		7	20		7	20		7	30		7			7			7		$\mu V/^\circ C$
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			30			30			75			±100			±150		45	±200	nA_{DC}
Input Offset Current Drift			10	200		10	200		10	300		10			10			10		$pA_{DC}/^\circ C$
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$		40	100		40	100		40	200		40	300		40	500		40	500	nA_{DC}
Input Common-Mode Voltage Range (Note 7)	$V^+ = 30\ V_{DC}$	0		V^+-2	0		V^+-2	0		V^+-2	0		V^+-2	0		V^+-2	0		V^+-2	V_{DC}
Large Signal Voltage Gain	$V^+ = +15\ V_{DC}$ (For Large V_O Swing) $R_L \geq 2\ k\Omega$	25			25			15			25			15			15			V/mV
Output Voltage Swing																				
V_{OH}	$V^+ = +30\ V_{DC}$, $R_L = 2\ k\Omega$	26			26			26			26			26			22			V_{DC}
	$R_L \geq 10\ k\Omega$	27	28		27	28		27	28		27	28		27	28		23	24		V_{DC}
V_{OL}	$V^+ = 5\ V_{DC}$, $R_L \leq 10\ k\Omega$		5	20		5	20		5	20		5	20		5	20		5	100	mV_{DC}
Output Current																				
Source	$V_{IN}^+ = +1\ V_{DC}$, $V_{IN}^- = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$	10	20		10	20		10	20		10	20		10	20		10	20		mA_{DC}
Sink	$V_{IN}^- = +1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$	10	15		5	8		5	8		5	8		5	8		5	8		mA_{DC}
Differential Input Voltage	(Note 7)			32			32			32			32			32			26	V_{DC}

Note 1: For operating at high temperatures, the LM324/LM324A, LM2902 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM224/LM224A and LM124/LM124A can be derated based on a +150°C maximum junction temperature. The dissipation is the total of all four amplifiers—use external resistors, where possible, to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of +15 V_{DC}, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3 V_{DC} (at 25°C).

Note 4: These specifications apply for $V^+ = +5\ V_{DC}$ and $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise stated. With the LM224/LM224A, all temperature specifications are limited to $-25^\circ C \leq T_A \leq +85^\circ C$, the LM324/LM324A temperature specifications are limited to $0^\circ C \leq T_A \leq +70^\circ C$, and the LM2902 specifications are limited to $-40^\circ C \leq T_A \leq +85^\circ C$.

Note 5: $V_O \cong 1.4\ V_{DC}$, $R_S = 0\Omega$ with V^+ from 5 V_{DC} to 30 V_{DC}; and over the full input common-mode range (0 V_{DC} to $V^+ - 1.5\ V_{DC}$).

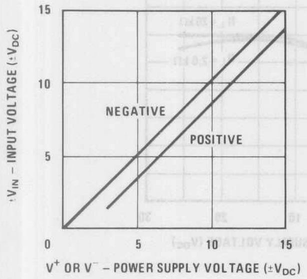
Note 6: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

Note 7: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is $V^+ - 1.5V$, but either or both inputs can go to +32 V_{DC} without damage (+26 V_{DC} for LM2902).

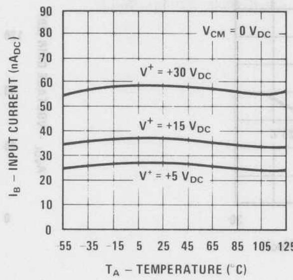
Note 8: Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitive increases at higher frequencies.

Typical Performance Characteristics

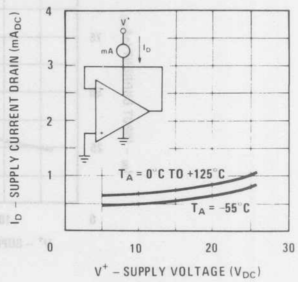
Input Voltage Range



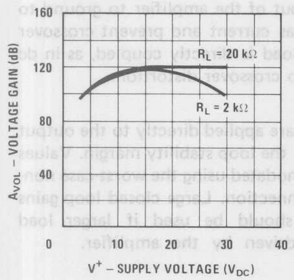
Input Current



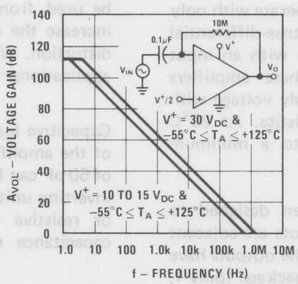
Supply Current



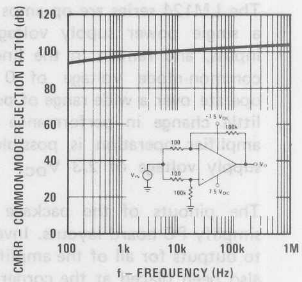
Voltage Gain



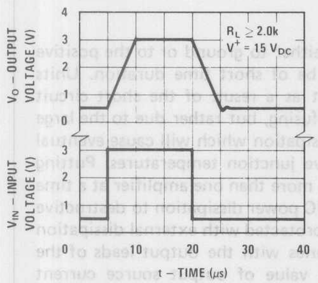
Open Loop Frequency Response



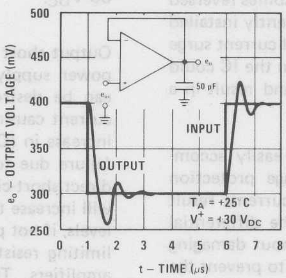
Common Mode Rejection Ratio



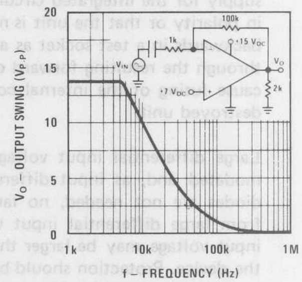
Voltage Follower Pulse Response



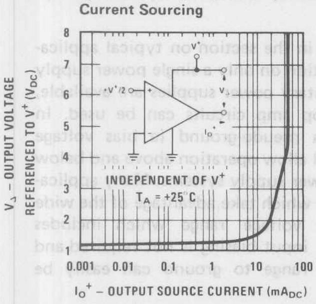
Voltage Follower Pulse Response (Small Signal)



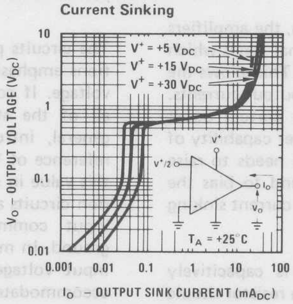
Large Signal Frequency Response



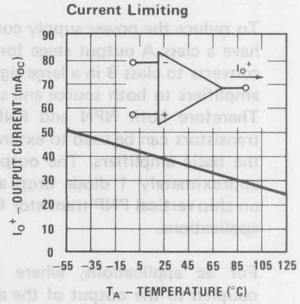
Output Characteristics Current Sourcing



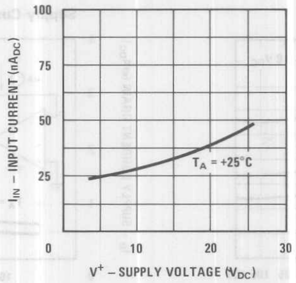
Output Characteristics Current Sinking



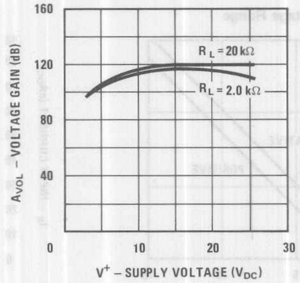
Current Limiting



Input Current



Voltage Gain



Application Hints

The LM124 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 V_{DC}.

The pinouts of the package have been designed to simplify PC board layouts. Inverting inputs are adjacent to outputs for all of the amplifiers and the outputs have also been placed at the corners of the package (pins 1, 7, 8, and 14).

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than -0.3 V_{DC} (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply current drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion. Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accommodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

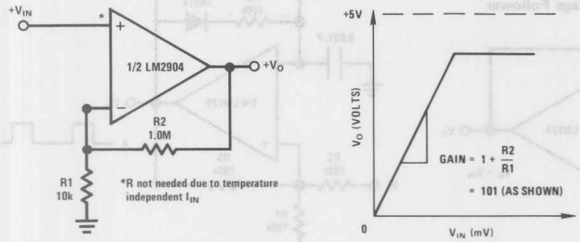
The bias network of the LM124 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 3 V_{DC} to 30 V_{DC}.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

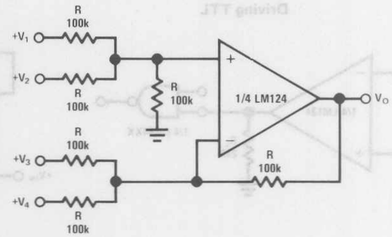
The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$)

Non-Inverting DC Gain (0V Input = 0V Output)

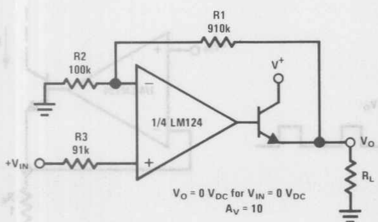


DC Summing Amplifier
(V_{IN}'S $\geq 0\ V_{DC}$ AND $V_O \geq 0\ V_{DC}$)

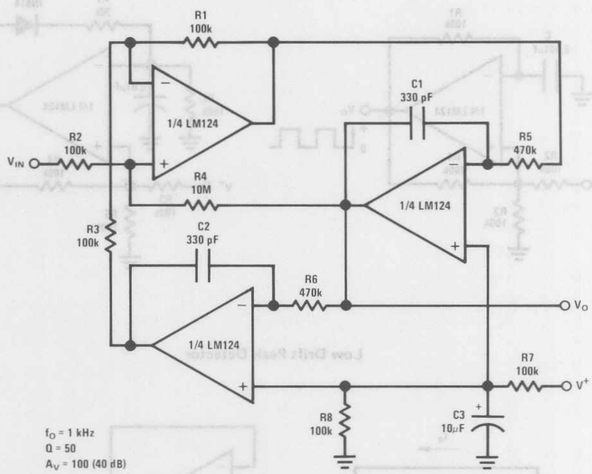


Where: $V_O = V_1 + V_2 - V_3 - V_4$
$(V_1 + V_2) \geq (V_3 + V_4)$ to keep $V_O > 0\ V_{DC}$

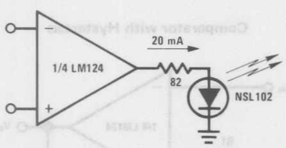
Power Amplifier



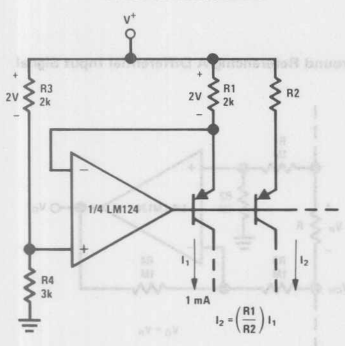
"BI-QUAD" RC Active Bandpass Filter



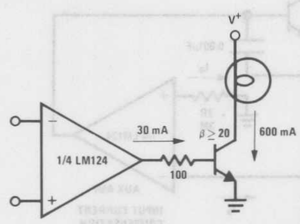
LED Driver



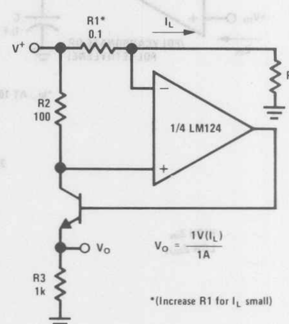
Fixed Current Sources



Lamp Driver

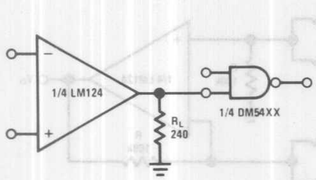


Current Monitor

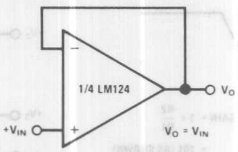


Typical Single-Supply Applications (Continued) ($V^+ = 5.0\ V_{DC}$)

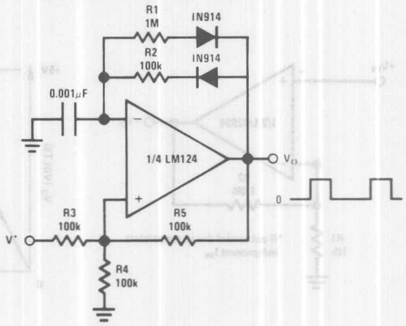
Driving TTL



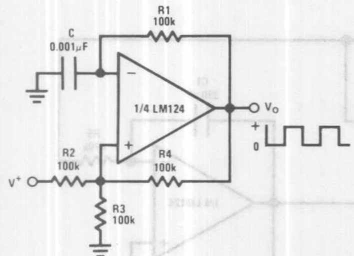
Voltage Follower



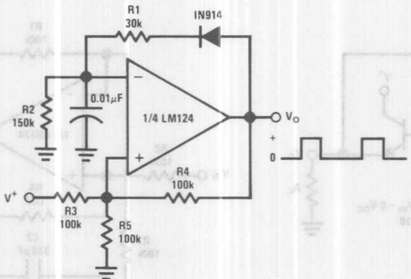
Pulse Generator



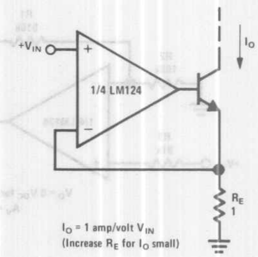
Squarewave Oscillator



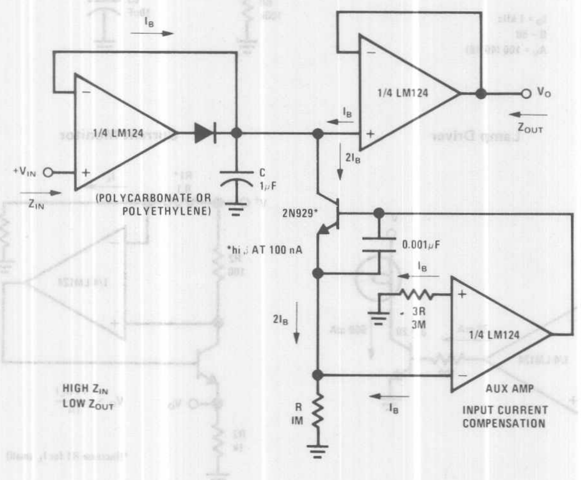
Pulse Generator



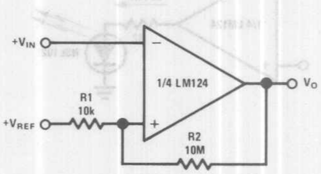
High Compliance Current Sink



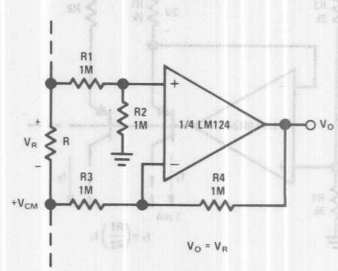
Low Drift Peak Detector



Comparator with Hysteresis



Ground Referencing A Differential Input Signal



Typical Single-Supply Applications (Continued) ($V^+ = 5.0\ V_{DC}$)

Voltage Controlled Oscillator Circuit

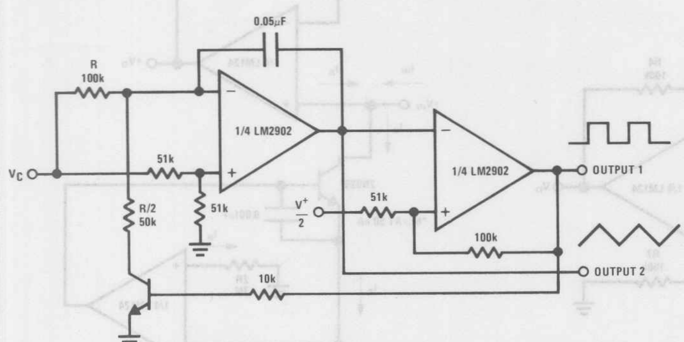
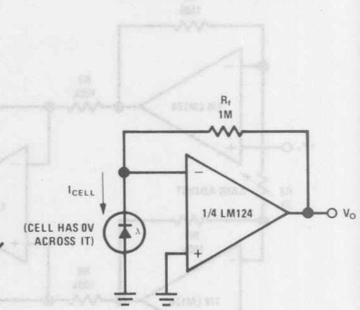
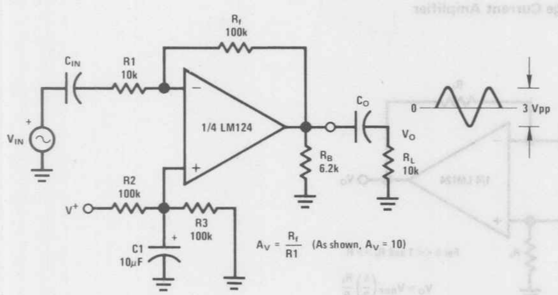


Photo Voltaic-Cell Amplifier

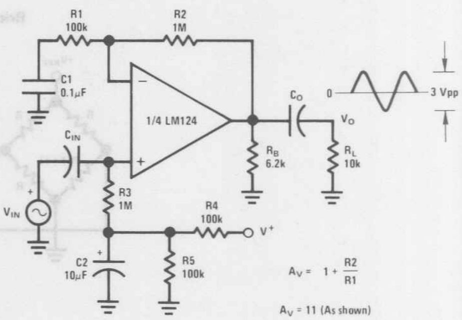


AC Coupled Inverting Amplifier



$A_V = \frac{R_f}{R1}$ (As shown, $A_V = 10$)

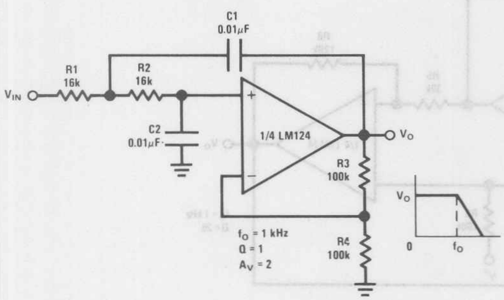
AC Coupled Non-Inverting Amplifier



$A_V = 1 + \frac{R2}{R1}$

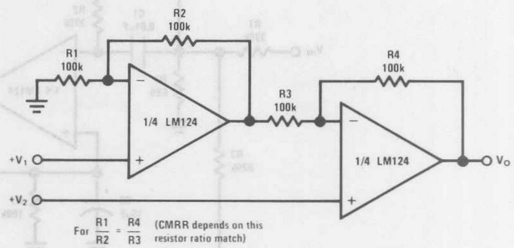
$A_V = 11$ (As shown)

DC Coupled Low-Pass RC Active Filter



$f_O = 1$ kHz
$Q = 1$
$A_V = 2$

High Input Z, DC Differential Amplifier



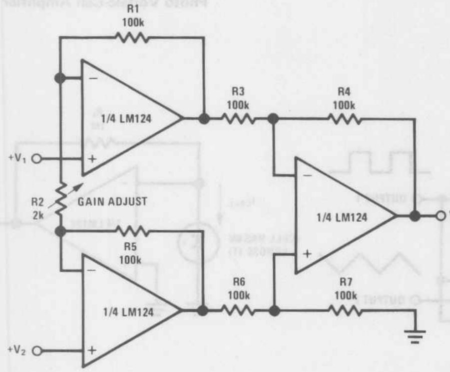
For $\frac{R1}{R2} = \frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

$V_O = 1 + \frac{R4}{R3}\ (V_2 - V_1)$

As shown: $V_O = 2(V_2 - V_1)$

Typical Single-Supply Applications (Continued) ($V^+ = 5.0\ V_{DC}$)

High Input Z Adjustable-Gain DC Instrumentation Amplifier

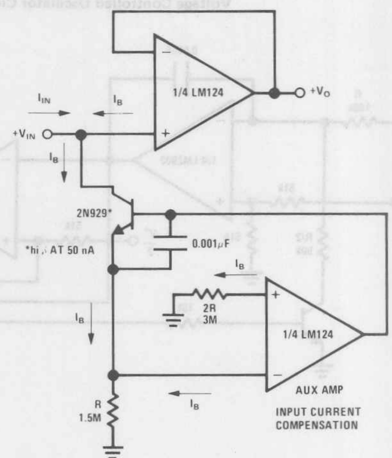


If R1 = R5 & R3 = R4 = R6 = R7 (CMRR depends on match)

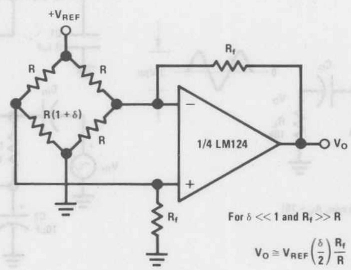
$$V_O = 1 + \frac{2R1}{R2}(V_2 - V_1)$$

As shown $V_O = 101\ (V_2 - V_1)$

Using Symmetrical Amplifiers to Reduce Input Current (General Concept)



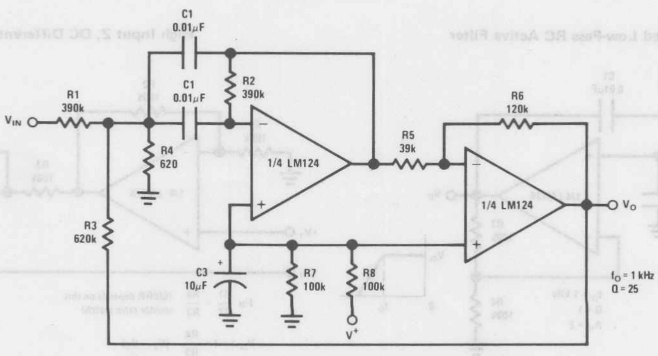
Bridge Current Amplifier



For $\delta << 1$ and $R_f >> R$

$$V_O \cong V_{REF}\left(\frac{\delta}{2}\right)\frac{R_f}{R}$$

Bandpass Active Filter



LM143/LM343 High Voltage Operational Amplifier

General Description

The LM143 is a general purpose high voltage operational amplifier featuring operation to ±40V, complete input overvoltage protection up to ±40V and input currents comparable to those of other super-β op amps. Increased slew rate, together with higher common-mode and supply rejection, insure improved performance at high supply voltages. Operating characteristics, in particular supply current, slew rate and gain, are virtually independent of supply voltage and temperature. Furthermore, gain is unaffected by output loading at high supply voltages due to thermal symmetry on the die. The LM143 is pin compatible with general purpose op amps and has offset null capability.

Application areas include those of general purpose op amps, but can be extended to higher voltages and higher output power when externally boosted. For example, when used in audio power applications, the LM143 provides a power bandwidth that covers the entire audio spectrum. In addition, the LM143 can be reliably operated in environments with large overvoltage spikes on the power supplies, where other internally-compensated op amps would suffer catastrophic failure.

The LM343 is similar to the LM143 for applications in less severe supply voltage and temperature environments.

Features

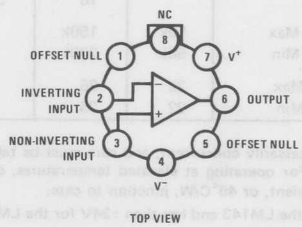
- Wide supply voltage range ±4.0V to ±40V
- Large output voltage swing ±37V
- Wide input common-mode range ±38V
- Input overvoltage protection Full ±40V
- Supply current is virtually independent of supply voltage and temperature

Unique Characteristics

- Low input bias current 8.0 nA
- Low input offset current 1.0 nA
- High slew rate—essentially independent of temperature and supply voltage 2.5V/µs
- High voltage gain—virtually independent of resistive loading, temperature, and supply voltage 100k min
- Internally compensated for unity gain
- Output short circuit protection
- Pin compatible with general purpose op amps

Connection Diagram

Metal Can Package



TOP VIEW

Order Number LM143H
or LM343H
See NS Package H08C

Absolute Maximum Ratings (Note 1)

	LM143	LM343
Supply Voltage	±40V	±34V
Power Dissipation (Note 1)	680 mW	680 mW
Differential Input Voltage (Note 2)	80V	68V
Input Voltage (Note 2)	±40V	±34V
Operating Temperature Range	−55°C to +125°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Output Short Circuit Duration	5 seconds	5 seconds
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

Electrical Characteristics (Note 3)

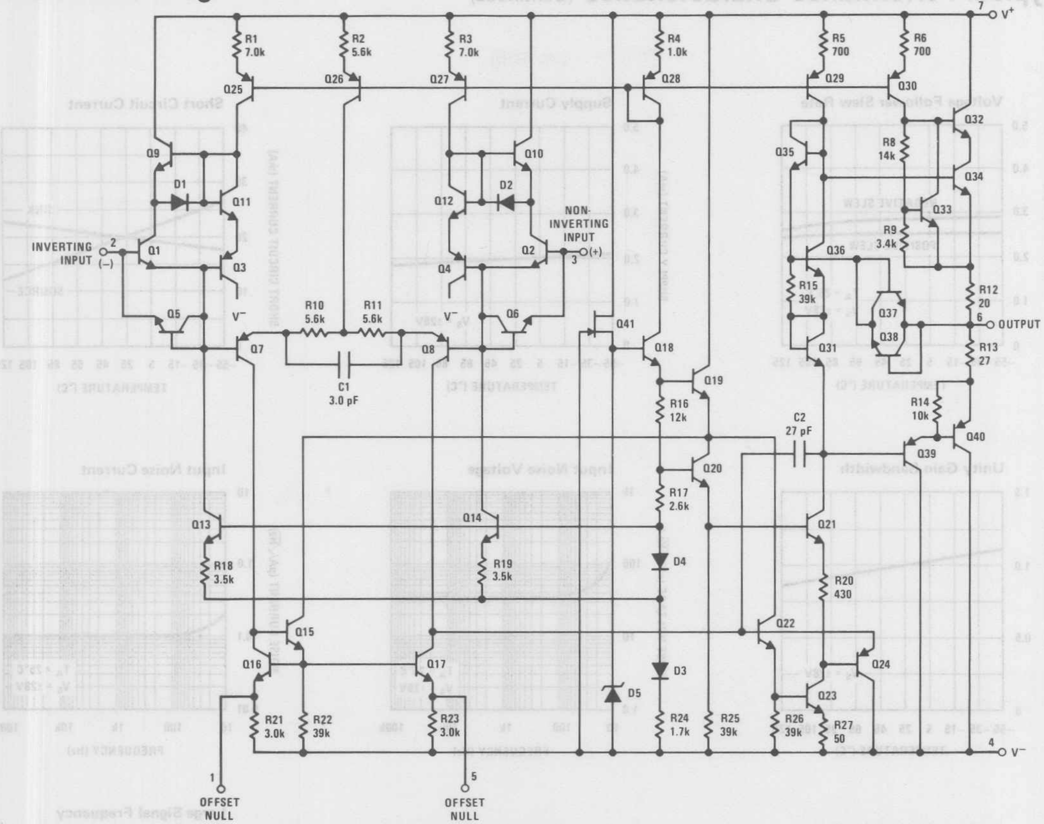
PARAMETER	CONDITIONS	LM143 MIN	LM143 TYP	LM143 MAX	LM343 MIN	LM343 TYP	LM343 MAX	UNITS
Input Offset Voltage	$T_A = 25°C$		2.0	5.0		2.0	8.0	mV
Input Offset Current	$T_A = 25°C$		1.0	3.0		1.0	10	nA
Input Bias Current	$T_A = 25°C$		8.0	20		8.0	40	nA
Supply Voltage Rejection Ratio	$T_A = 25°C$		10	100		10	200	μV/V
Output Voltage Swing	$T_A = 25°C$, $R_L \geq 5\ k\Omega$	22	25		20	25		V
Large Signal Voltage Gain	$T_A = 25°C$, $V_{OUT} = \pm 10V$, $R_L \geq 100\ k\Omega$	100k	180k		70k	180k		V/V
Common-Mode Rejection Ratio	$T_A = 25°C$	80	90		70	90		dB
Input Voltage Range	$T_A = 25°C$	24	26		22	26		V
Supply Current (Note 4)	$T_A = 25°C$		2.0	4.0		2.0	5.0	mA
Short Circuit Current	$T_A = 25°C$		20			20		mA
Slew Rate	$T_A = 25°C$, $A_V = 1$		2.5			2.5		V/μs
Power Bandwidth	$T_A = 25°C$, $V_{OUT} = 40\ V_{P\text{-}P}$, $R_L = 5\ k\Omega$, THD $\leq 1\%$		20k			20k		Hz
Unity Gain Frequency	$T_A = 25°C$		1.0M			1.0M		Hz
Input Offset Voltage	T_A = Max			6.0			10	mV
	T_A = Min			6.0			10	mV
Input Offset Current	T_A = Max		0.8	4.5		0.8	14	nA
	T_A = Min		1.8	7.0		1.8	14	nA
Input Bias Current	T_A = Max		5.0	35		5.0	55	nA
	T_A = Min		16	35		16	55	nA
Large Signal Voltage Gain	$R_L \geq 100\ k\Omega$, T_A = Max	50k	150k		50k	150k		V/V
	$R_L \geq 100\ k\Omega$, T_A = Min	50k	220k		50k	220k		V/V
Output Voltage Swing	$R_L \geq 5.0\ k\Omega$, T_A = Max	22	26		20	26		V
	$R_L \geq 5.0\ k\Omega$, T_A = Min	22	25		20	25		V

Note 1: Absolute maximum ratings are not necessarily concurrent, and care must be taken not to exceed the maximum junction temperature of the LM143 (150°C) or the LM343 (100°C). For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case.

Note 2: For supply voltage less than ±40V for the LM143 and less than ±34V for the LM343, the absolute maximum input voltage is equal to the supply voltage.

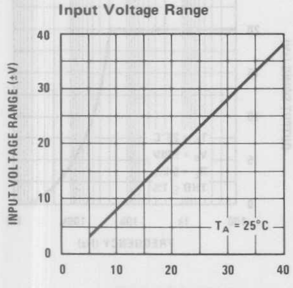
Note 3: These specifications apply for $V_S = \pm 28V$. For LM143, T_A = max = 125°C and T_A = min = −55°C. For LM343, T_A = max = 70°C and T_A = min = 0°C.

Schematic Diagram

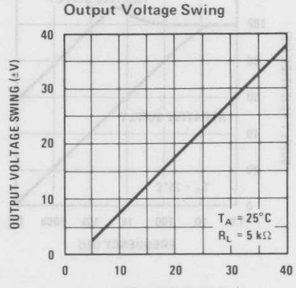


Typical Performance Characteristics

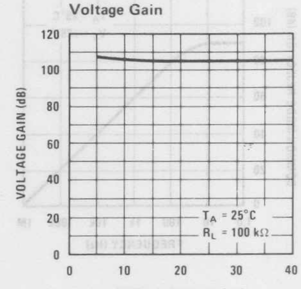
Input Voltage Range



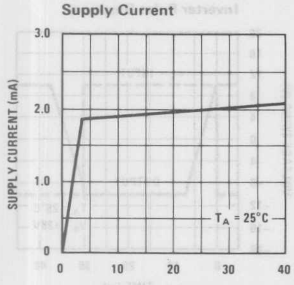
Output Voltage Swing



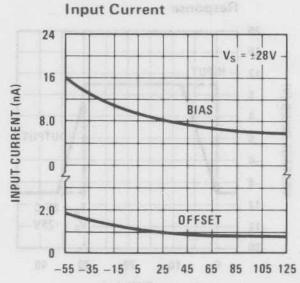
Voltage Gain



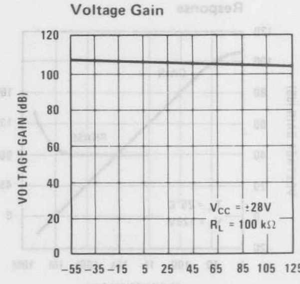
Supply Current



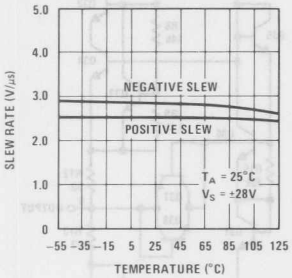
Input Current



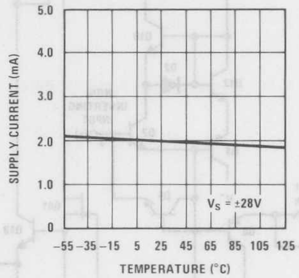
Voltage Gain



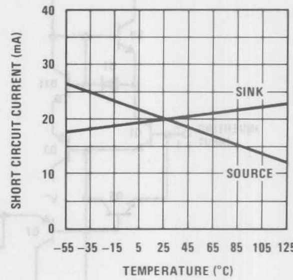
Voltage Follower Slew Rate



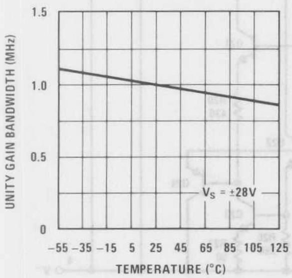
Supply Current



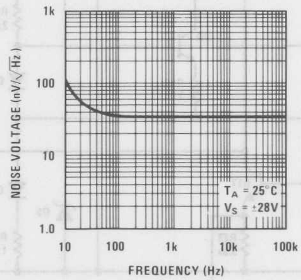
Short Circuit Current



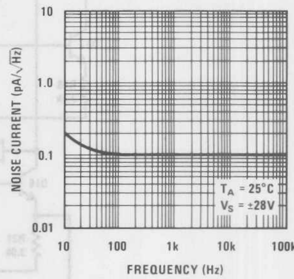
Unity Gain Bandwidth



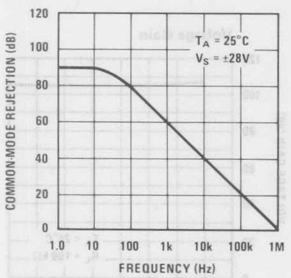
Input Noise Voltage



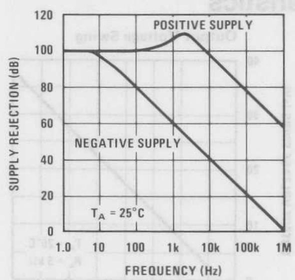
Input Noise Current



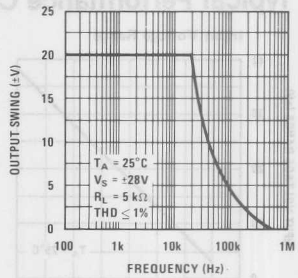
Common-Mode Rejection



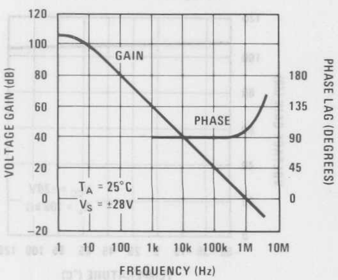
Power Supply Rejection



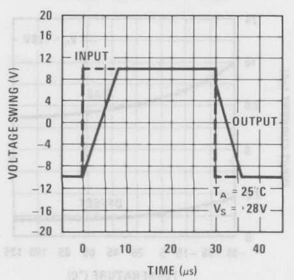
Large Signal Frequency Response



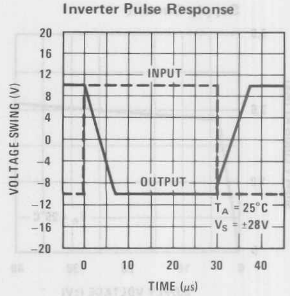
Open Loop Frequency Response



Voltage Follower Pulse Response



Inverter Pulse Response



Application Hints (See AN-127)

The LM143 is designed for trouble free operation at any supply voltage up to and including the guaranteed maximum of ±40V. Input overvoltage protection, both common-mode and differential, is 100% tested and guaranteed at the maximum supply voltage. Furthermore, all possible high voltage destructive modes during supply voltage turn-on have been eliminated by design. As with most IC op amps, however, certain precautions should be observed to insure that the LM143 remains virtually blow-out proof.

Although output short circuits to ground or either supply can be sustained indefinitely at lower supply voltages, these short circuits should be of limited duration when operating at higher supply voltages. Units can be destroyed by any combination of high ambient temperature, high supply voltages, and high power dissipation which results in excessive die temperature. This is also true when driving low impedance or reactive loads or loads that can revert to low impedance; for example, the LM143 can drive most general purpose op amps outside of the maximum input voltage range, causing heavy current to flow and possibly destroying both devices.

Precautions should be taken to insure that the power supplies never become reversed in polarity—even under transient conditions. With reverse voltage, the IC will conduct excessive current, fusing the internal aluminum interconnects. Voltage reversal between the power supplies will almost always result in a destroyed unit.

In high voltage applications which are sensitive to very low input currents, special precautions should be exercised. For example, with high source resistances, care should be taken to prevent the magnitude of the PC board leakage currents, although quite small, from approaching those of the op amp input currents. These leakage currents become larger at 125°C and are made worse by high supply voltages. To prevent this, PC boards should be properly cleaned and coated to prevent contamination and to provide protection from condensed water vapor when operating below 0°C. A guard ring is also recommended to significantly reduce leakage currents from the op amp input pins to the adjacent high voltage pins in the standard op amp pin connection as shown in *Figure 1. Figures 2, 3 and 4* show how the guard ring is connected for the three most common op amp configurations.

Finally, caution should be exercised in high voltage applications as electrical shock hazards are present. Since the negative supply is connected to the case, users may inadvertantly contact voltages equal to those across the power supplies.

The LM143 can be used as a plug-in replacement in most general purpose op amp applications. The circuits presented in the following section emphasize those applications which take advantage of the unique high voltage capabilities of the LM143.

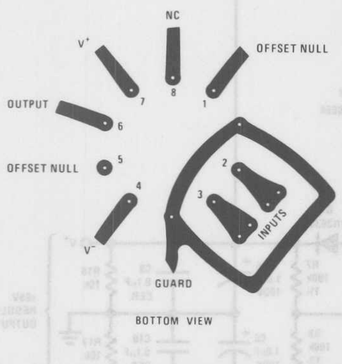


FIGURE 1. Printed Circuit Layout for Input Guarding with TO-5 Package

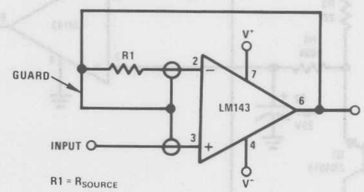


FIGURE 2. Guarded Voltage Follower

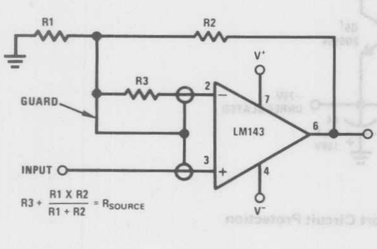


FIGURE 3. Guarded Non-Inverting Amplifier

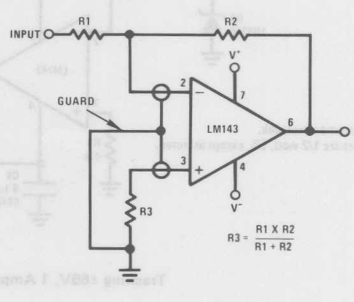
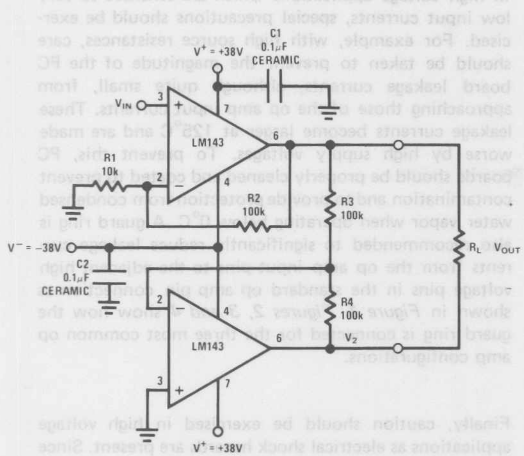
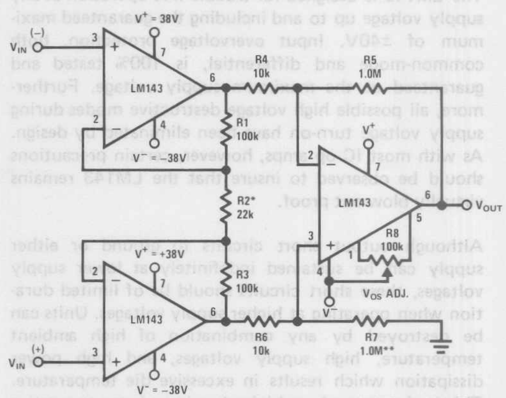


FIGURE 4. Guarded Inverting Amplifier

Typical Applications ‡ (For more detail see AN-127)



130 $V_{P\text{-}P}$ Drive Across a Floating Load

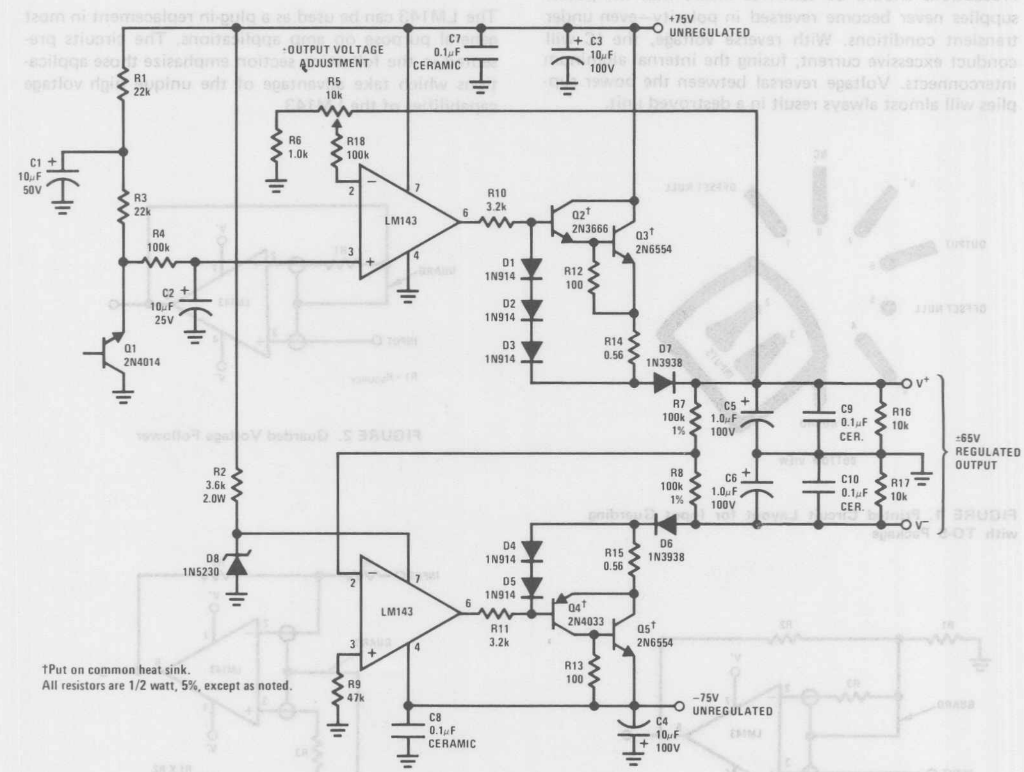


$$A_V = \left(1 + \frac{2\,R1}{R2}\right)\frac{R5}{R4}$$ WHERE: R4 = R6, R5 = R7

*R2 may be adjustable to trim the gain.

**R7 may be adjusted to compensate for the resistance tolerance of R4 – R7 for best CMR.

±34V Common-Mode Instrumentation Amplifier

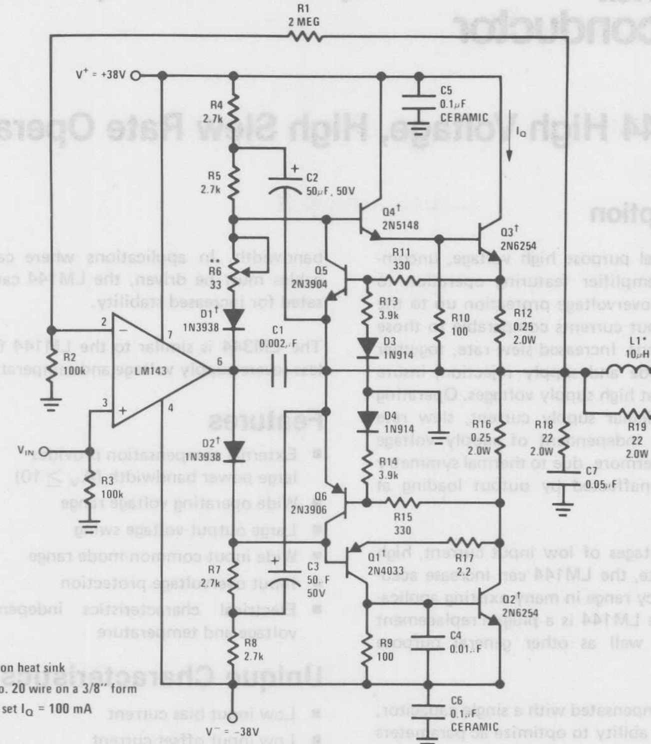


†Put on common heat sink.
All resistors are 1/2 watt, 5%, except as noted.

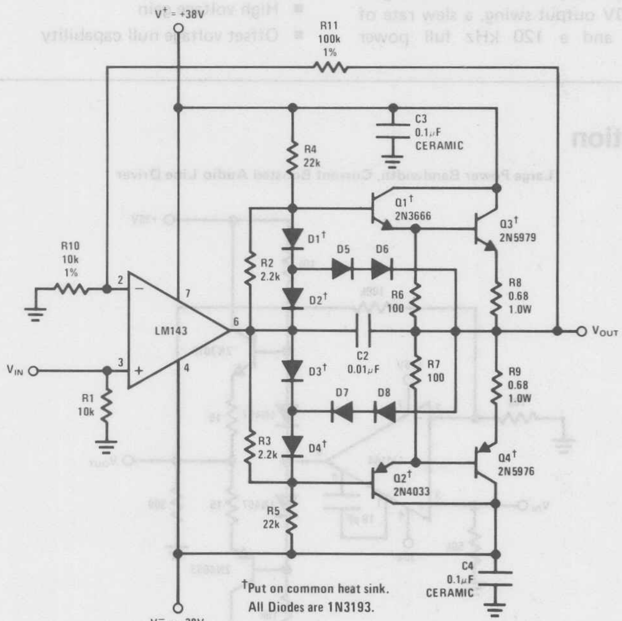
Tracking ±65V, 1 Amp Power Supply with Short Circuit Protection

‡The 38V supplies allow for a 5% voltage tolerance. All resistors are 1/2 watt, except as noted.

Typical Applications (Continued) (For more detail see AN-127)



90W Audio Power Amplifier with Safe Area Protection



1 Amp Power Amplifier with Short Circuit Protection

‡The 38V supplies allow for a 5% voltage tolerance. All resistors are 1/2 watt, except as noted.

LM144/LM344 High Voltage, High Slew Rate Operational Amplifier

General Description

The LM144 is a general purpose high voltage, uncompensated operational amplifier featuring operation to ±36V, complete input overvoltage protection up to the supply voltages and input currents comparable to those of other super-β op amps. Increased slew rate, together with high common-mode and supply rejection, insure excellent performance at high supply voltages. Operating characteristics, in particular supply current, slew rate and gain, are virtually independent of supply voltage and temperature. Furthermore, due to thermal symmetry on the die, gain is unaffected by output loading at high supply voltages.

With the unique advantages of low input current, high gain, and high slew rate, the LM144 can increase accuracy and useful frequency range in many existing applications. For example, the LM144 is a plug-in replacement for the LM101A, as well as other general purpose op amps.

The LM144 can be compensated with a single capacitor, thus giving the user the ability to optimize ac parameters to suit the application. For example, in applications such as audio power amplifiers, the LM144 with a gain of 10 can provide a ±30V output swing, a slew rate of approximately 30V/μs, and a 120 kHz full power bandwidth. In applications where capacitive loads or cables must be driven, the LM144 can be overcompensated for increased stability.

The LM344 is similar to the LM144 for applications in less severe supply voltage and temperature environments.

Features

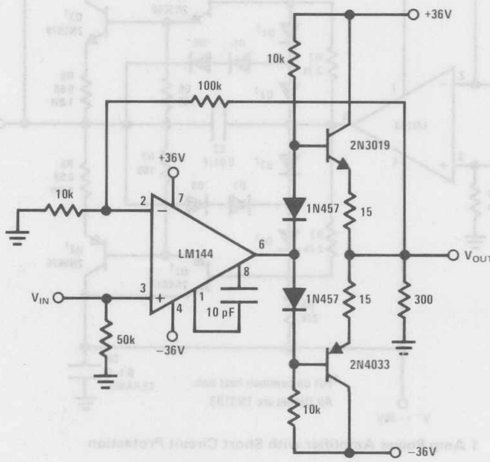
- External compensation provides large power bandwidth ($A_V \geq 10$) — 120 kHz
- Wide operating voltage range — ±4.0V to ±36V
- Large output voltage swing — ±30V
- Wide input common-mode range
- Input overvoltage protection
- Electrical characteristics independent of supply voltage and temperature

Unique Characteristics

- Low input bias current — 8.0 nA
- Low input offset current — 1.0 nA
- High slew rate ($A_V \geq 10$) — 30V/μs
- High voltage gain — 100k min
- Offset voltage null capability

Typical Application

Large Power Bandwidth, Current Boosted Audio Line Driver



Absolute Maximum Ratings (These ratings are not concurrent)

	LM144	LM344
Supply Voltage	±40V	±34V
Power Dissipation (Note 1)	680 mW	680 mW
Differential Input Voltage (Note 2)	80V	68V
Input Voltage (Note 2)	±40V	±34V
Operating Temperature Range	−55°C to +125°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Output Short Circuit Duration	5 seconds	5 seconds
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

Electrical Characteristics (Note 3)

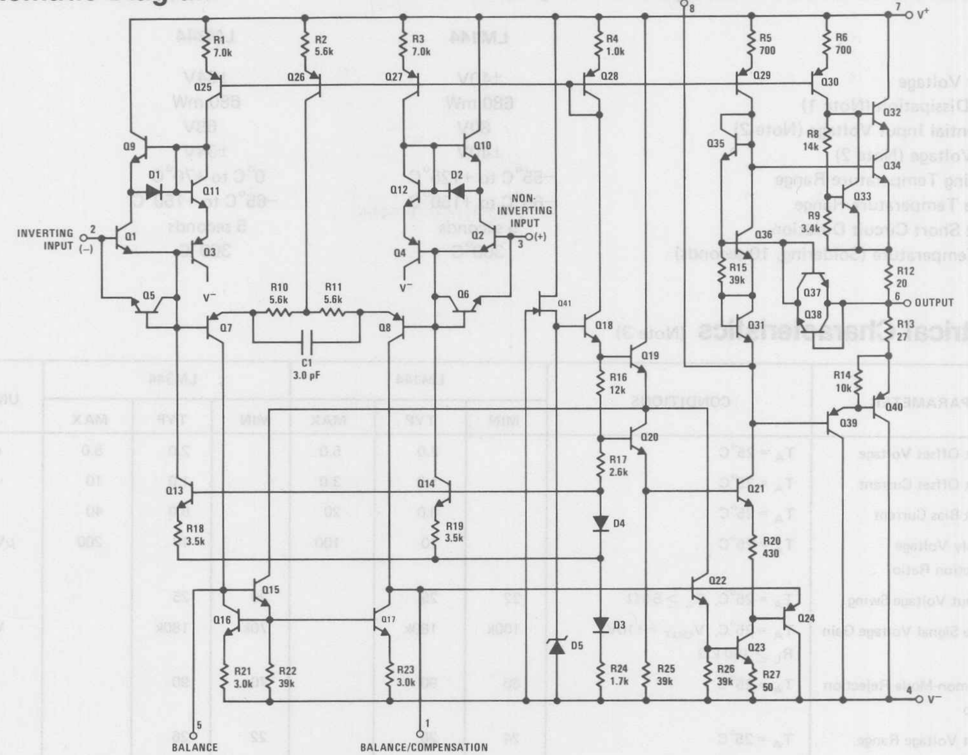
PARAMETER	CONDITIONS	LM144			LM344			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$		2.0	5.0		2.0	8.0	mV
Input Offset Current	$T_A = 25°C$		1.0	3.0		1.0	10	nA
Input Bias Current	$T_A = 25°C$		8.0	20		8.0	40	nA
Supply Voltage Rejection Ratio	$T_A = 25°C$		10	100		10	200	μV/V
Output Voltage Swing	$T_A = 25°C$, $R_L \geq 5\,k\Omega$	22	25		20	25		V
Large Signal Voltage Gain	$T_A = 25°C$, $V_{OUT} = \pm 10V$, $R_L \geq 100\,k\Omega$	100k	180k		70k	180k		V/V
Common-Mode Rejection Ratio	$T_A = 25°C$	80	90		70	90		dB
Input Voltage Range	$T_A = 25°C$	24	26		22	26		V
Supply Current	$T_A = 25°C$		2.0	4.0		2.0	5.0	mA
Short Circuit Current	$T_A = 25°C$		20			20		mA
Slew Rate	$T_A = 25°C$, $A_V = 1$		2.5			2.5		V/μs
	$T_A = 25°C$, $A_V = 10$, $C1 = 3\,pF$		30			30		V/μs
Power Bandwidth	$T_A = 25°C$, $V_{OUT} = 40\,V_{P\text{-}P}$, $R_L = 5\,k\Omega$, THD $\leq 1\%$, $A_V = 1$		20k			20k		Hz
Unity Gain Frequency	$T_A = 25°C$		1.0M			1.0M		Hz
Input Offset Voltage	T_A = Max			6.0			10	mV
	T_A = Min			6.0			10	mV
Input Offset Current	T_A = Max		0.8	4.5		0.8	14	nA
	T_A = Min		1.8	7.0		1.8	14	nA
Input Bias Current	T_A = Max		5.0	35		5.0	55	nA
	T_A = Min		16	35		16	55	nA
Large Signal Voltage Gain	$R_L \geq 100\,k\Omega$, T_A = Max	50k	150k		50k	150k		V/V
	$R_L \geq 100\,k\Omega$, T_A = Min	50k	220k		50k	220k		V/V
Output Voltage Swing	$R_L \geq 5.0\,k\Omega$, T_A = Max	22	26		20	26		V
	$R_L \geq 5.0\,k\Omega$, T_A = Min	22	25		20	25		V

Note 1: The maximum junction temperature of the LM144 is 150°C, while that of the LM344 is 100°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case.

Note 2: For supply voltage less than ±40V for the LM144 and less than ±34V for the LM344, the absolute maximum input voltage is equal to the supply voltage.

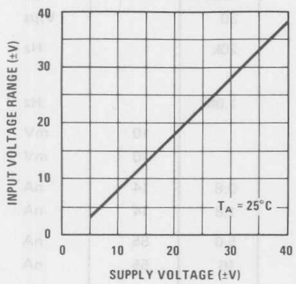
Note 3: These specifications apply for $V_S = \pm 28V$. For the LM144, T_A = max = 125°C and T_A = min = −55°C. For the LM344, T_A = max = 70°C and T_A = min = 0°C.

Schematic Diagram

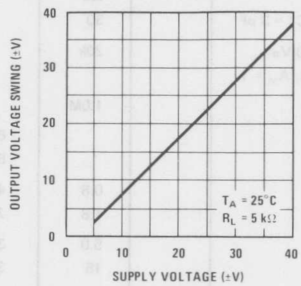


Typical Performance Characteristics

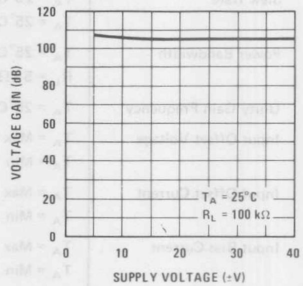
Input Voltage Range



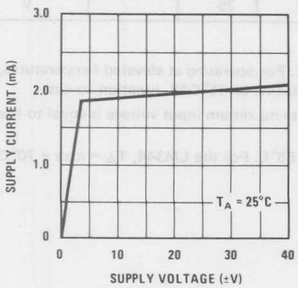
Output Voltage Swing



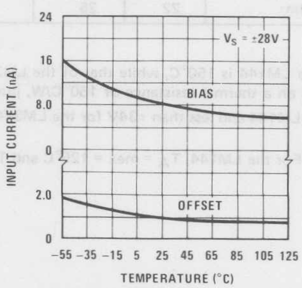
Voltage Gain



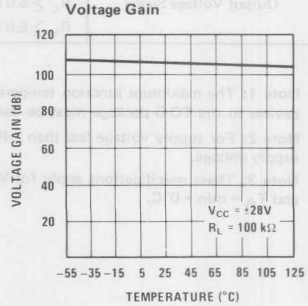
Supply Current



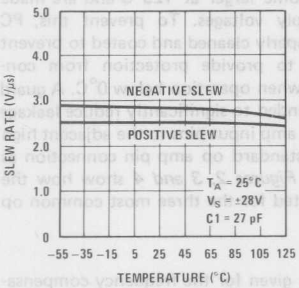
Input Current



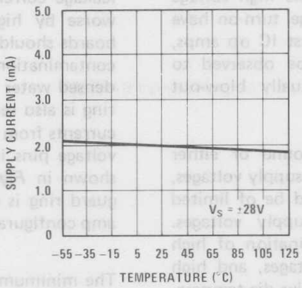
Voltage Gain



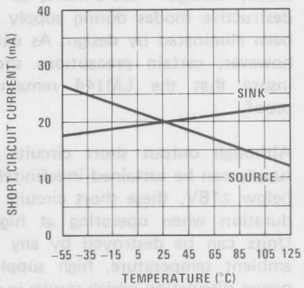
Voltage Follower Slew Rate



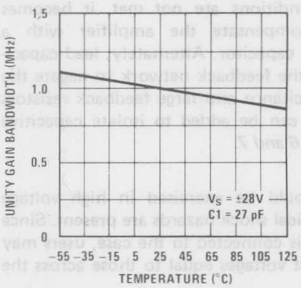
Supply Current



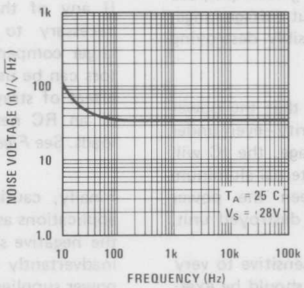
Short Circuit Current



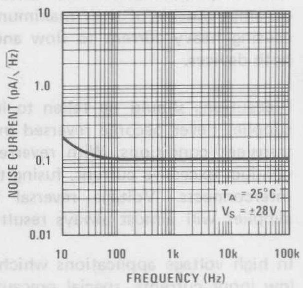
Unity Gain Bandwidth



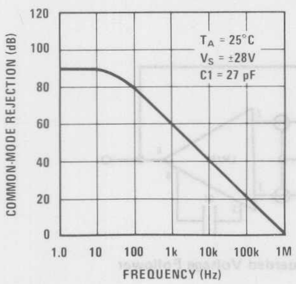
Input Noise Voltage



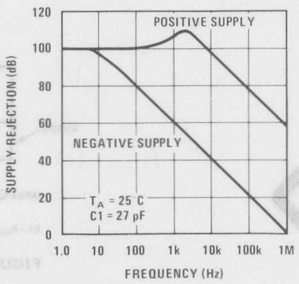
Input Noise Current



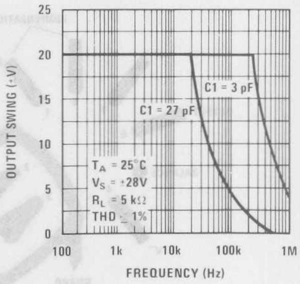
Common-Mode Rejection



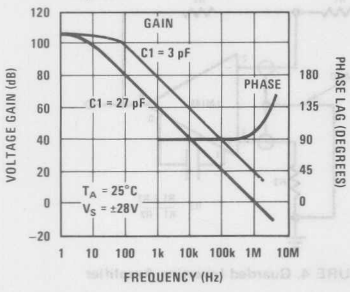
Power Supply Rejection



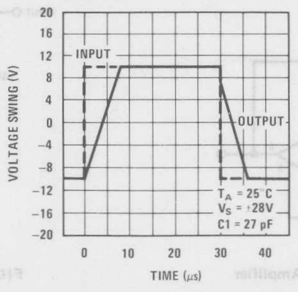
Large Signal Frequency Response



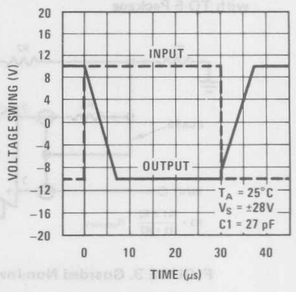
Open Loop Frequency Response



Voltage Follower Pulse Response



Inverter Pulse Response



supply voltage up to a maximum of ±40V. Input overvoltage protection, both common-mode and differential, is 100% tested and guaranteed at the maximum supply voltage. Furthermore, all possible high voltage destructive modes during supply voltage turn-on have been eliminated by design. As with most IC op amps, however, certain precautions should be observed to insure that the LM144 remains virtually blow-out proof.

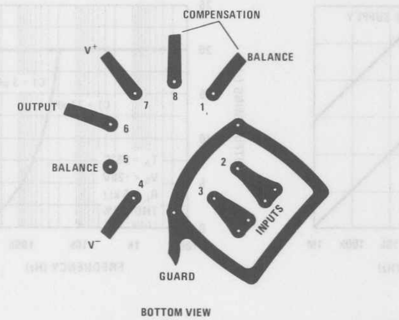
Although output short circuits to ground or either supply can be sustained indefinitely for supply voltages, below ±18V, these short circuits should be of limited duration when operating at higher supply voltages. Units can be destroyed by any combination of high ambient temperature, high supply voltages, and high power dissipation which results in excessive die temperature. This is also true when driving low impedance or reactive loads or loads that can revert to low impedance; for example, the LM144 can drive most general purpose op amps outside of their maximum input voltage range, causing heavy current to flow and possibly destroying both devices.

Precautions should be taken to insure that the power supplies never become reversed in polarity—even under transient conditions. With reverse voltage, the IC will conduct excessive current, fusing the internal aluminum interconnects. Voltage reversal between the power supplies will almost always result in a destroyed unit.

In high voltage applications which are sensitive to very low input currents, special precautions should be exercised to prevent the magnitude of the PC board leakage currents, although quite small, from approaching those of the op amp input currents. These leakage currents become larger at 125°C and are made worse by high supply voltages. To prevent this, PC boards should be properly cleaned and coated to prevent contamination and to provide protection from condensed water vapor when operation below 0°C. A guard ring is also recommended to significantly reduce leakage currents from the op amp input pins to the adjacent high voltage pins in the standard op amp pin connection as shown in *Figure 1. Figures 2, 3 and 4* show how the guard ring is connected for the three most common op amp configurations.

The minimum values given for the frequency compensation capacitor are stable only for source resistances less than 10 kΩ, stray capacitances on the summing junction less than 5 pF and capacitive loads smaller than 100 pF. If any of these conditions are not met, it becomes necessary to overcompensate the amplifier with a larger compensation capacitor. Alternately, lead capacitors can be used in the feedback network to negate the effect of stray capacitance and large feedback resistors or an RC network can be added to isolate capacitive loads. See *Figures 5, 6 and 7.*

Finally, caution should be exercised in high voltage applications as electrical shock hazards are present. Since the negative supply is connected to the case, users may inadvertantly contact voltages equal to those across the power supplies.



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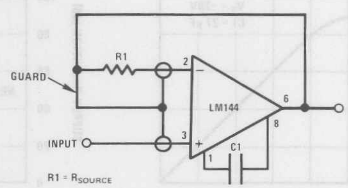


FIGURE 2. Guarded Voltage Follower

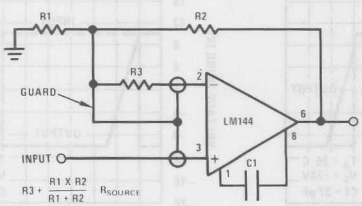


FIGURE 3. Guarded Non-Inverting Amplifier

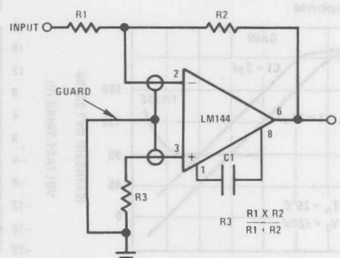


FIGURE 4. Guarded Inverting Amplifier

Application Hints (Continued)

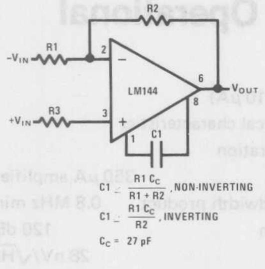


FIGURE 5. Single Pole Compensation

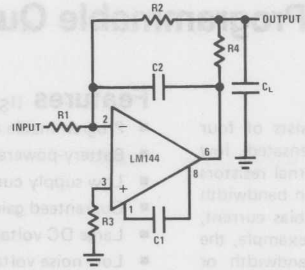


FIGURE 6. Isolating Large Capacitive Loads

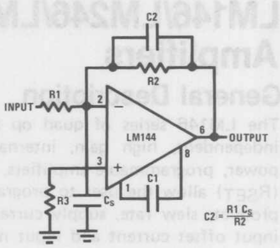


FIGURE 7. Compensating For Stray Input Capacitances or Large Feedback Resistor

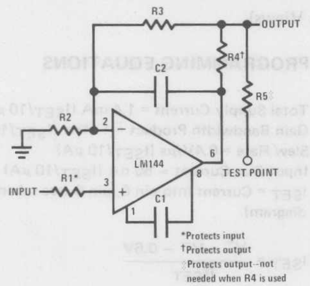


FIGURE 8. Protecting Against Gross Fault Conditions

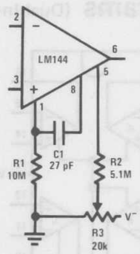
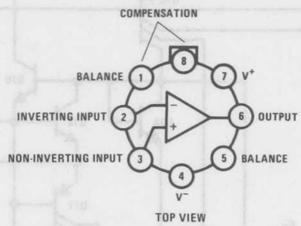


FIGURE 9. Balancing Circuit

Connection Diagrams

Metal Can Package



Order Number LM144H or LM344H See NS Package H08C

National Semiconductor

Operational Amplifiers/Buffers

LM146/LM246/LM346 Programmable Quad Operational Amplifiers

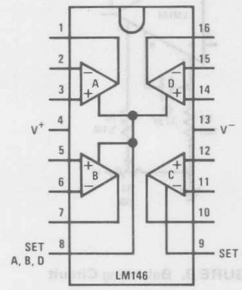
General Description

The LM146 series of quad op amps consists of four independent, high gain, internally compensated, low power, programmable amplifiers. Two external resistors (R_{SET}) allow the user to program the gain bandwidth product, slew rate, supply current, input bias current, input offset current and input noise. For example, the user can trade-off supply current for bandwidth or optimize noise figure for a given source resistance. In a similar way, other amplifier characteristics can be tailored to the application. Except for the two programming pins at the end of the package, the LM146 pin-out is the same as the LM124 and LM148.

Features (I_{SET} = 10 μA)

- Programmable electrical characteristics
- Battery-powered operation
- Low supply current — 350 μA amplifier
- Guaranteed gain bandwidth product — 0.8 MHz min
- Large DC voltage gain — 120 dB
- Low noise voltage — 28 nV/$\sqrt{Hz}$
- Wide power supply range — ±1.5V to ±22V
- Class AB output stage—no crossover distortion
- Ideal pin out for Biquad active filters
- Input bias currents are temperature compensated

Connection Diagrams (Dual-In-Line Packages, Top Views)



Order Number LM146J, LM246J or LM346J
See NS Package J16A

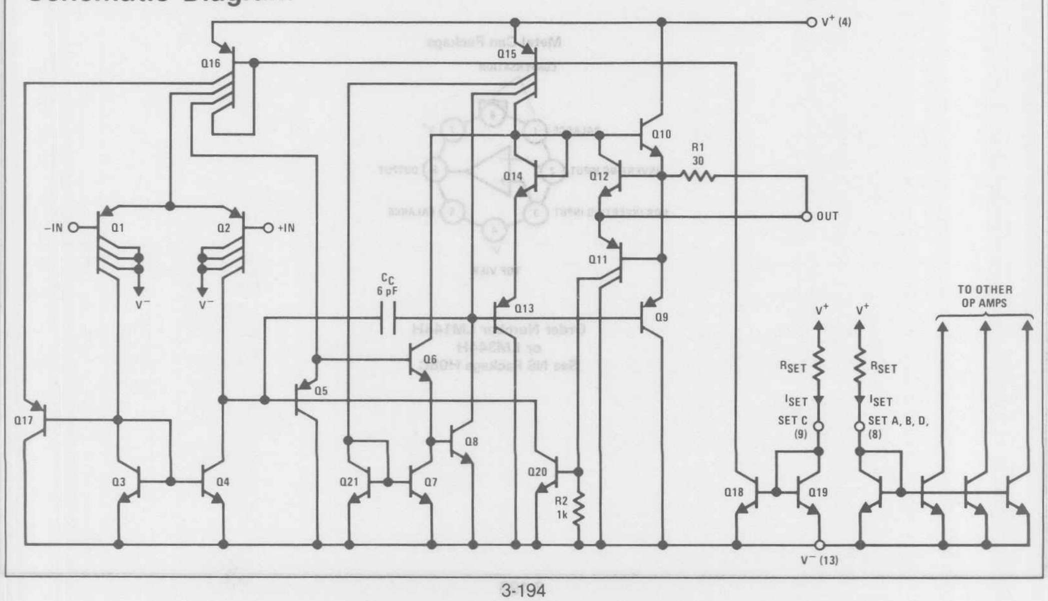
Order Number LM246N or LM346N
See NS Package N16A

PROGRAMMING EQUATIONS

Total Supply Current = 1.4 mA (I_{SET}/10 μA)
Gain Bandwidth Product = 1 MHz (I_{SET}/10 μA)
Slew Rate = 0.4V/μs (I_{SET}/10 μA)
Input Bias Current ≃ 50 nA (I_{SET}/10 μA)
I_{SET} = Current into pin 8, pin 9 (see schematic diagram)

$$I_{SET} = \frac{V^+ - V^- - 0.6V}{R_{SET}}$$

Schematic Diagram



Absolute Maximum Ratings (Note 1)

	LM146	LM246	LM346
Supply Voltage	±22V	±18V	±18V
Differential Input Voltage (Note 1)	±30V	±30V	±30V
CM Input Voltage (Note 1)	±15V	±15V	±15V
Power Dissipation (Note 2)	900 mW	500 mW	500 mW
Output Short-Circuit Duration (Note 3)	Indefinite	Indefinite	Indefinite
Operating Temperature Range	−55°C to +125°C	−25°C to +85°C	0°C to +70°C
Maximum Junction Temperature	150°C	110°C	100°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	300°C
Thermal Resistance (θ_{jA}), (Note 2)			
Cavity DIP (D) (J) P_d	900 mW	900 mW	900 mW
θ_{jA}	90°C/W	90°C/W	90°C/W
Molded DIP (N) P_d			500 mW
θ_{jA}			140°C/W

DC Electrical Characteristics (V_S = ±15V, I_{SET} = 10 μA, Note 4)

PARAMETER	CONDITIONS	LM146 MIN	LM146 TYP	LM146 MAX	LM246/LM346 MIN	LM246/LM346 TYP	LM246/LM346 MAX	UNITS
Input Offset Voltage	V_{CM} = 0V, $R_S \leq 50\ \Omega$, T_A = 25°C		0.5	5		0.5	6	mV
Input Offset Current	V_{CM} = 0V, T_A = 25°C		2	20		2	100	nA
Input Bias Current	V_{CM} = 0V, T_A = 25°C		50	100		50	250	nA
Supply Current (4 Op Amps)	T_A = 25°C		1.4	2.0		1.4	2.5	mA
Large Signal Voltage Gain	R_L = 10 kΩ, ΔV_{OUT} = ±10V, T_A = 25°C	100	1000		50	1000		V/mV
Input CM Range	T_A = 25°C	±13.5	±14		±13.5	±14		V
CM Rejection Ratio	$R_S \leq 10$ kΩ, T_A = 25°C	80	100		70	100		dB
Power Supply Rejection Ratio	$R_S \leq 10$ kΩ, T_A = 25°C	80	100		74	100		dB
Output Voltage Swing	$R_L \geq 10$ kΩ, T_A = 25°C	±12	±14		±12	±14		V
Short-Circuit Current	T_A = 25°C	5	20	35	5	20	35	mA
Gain Bandwidth Product	T_A = 25°C	0.8	1.2		0.5	1.2		MHz
Phase Margin	T_A = 25°C		60			60		Deg
Slew Rate	T_A = 25°C		0.4			0.4		V/μs
Input Noise Voltage	f = 1 kHz, T_A = 25°C		28			28		nV/$\sqrt{\text{Hz}}$
Channel Separation	R_L = 10 kΩ, ΔV_{OUT} = 0V to ±12V, T_A = 25°C		120			120		dB
Input Resistance	T_A = 25°C		1.0			1.0		MΩ
Input Capacitance	T_A = 25°C		2.0			2.0		pF
Input Offset Voltage	V_{CM} = 0V, $R_S \leq 50\ \Omega$		0.5	6		0.5	7.5	mV
Input Offset Current	V_{CM} = 0V		2	25		2	100	nA
Input Bias Current	V_{CM} = 0V		50	100		50	250	nA
Supply Current (4 Op Amps)			1.5	2.0		1.5	2.5	mA
Large Signal Voltage Gain	R_L = 10 kΩ, ΔV_{OUT} = ±10V	50	1000		25	1000		V/mV
Input CM Range		±13.5	±14		±13.5	±14		V
CM Rejection Ratio	$R_S \leq 50\ \Omega$	70	100		70	100		dB
Power Supply Rejection Ratio	$R_S \leq 50\ \Omega$	76	100		74	100		dB
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		±12	±14		V

Input Offset Voltage	$V_{CM} = 0V$, $R_S \leq 50\ \Omega$, $T_A = 25^\circ C$		0.5	5		0.5	7	mV
Input Bias Current	$V_{CM} = 0V$, $T_A = 25^\circ C$		7.5	20		7.5	100	nA
Supply Current (4 Op Amps)	$T_A = 25^\circ C$		140	250		140	300	μA
Gain Bandwidth Product	$T_A = 25^\circ C$	80	100		50	100		kHz

DC Electrical Characteristics ($V_S = \pm 1.5V$, $I_{SET} = 10\ \mu A$)

PARAMETER	CONDITIONS	LM146			LM246/LM346			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_{CM} = 0V$, $R_S \leq 50\ \Omega$, $T_A = 25^\circ C$		0.5	5		0.5	7	mV
Input CM Range	$T_A = 25^\circ C$	±0.7			±0.7			V
CM Rejection Ratio	$R_S \leq 50\ \Omega$, $T_A = 25^\circ C$		80			80		dB
Output Voltage Swing	$R_L \geq 10\ k\Omega$, $T_A = 25^\circ C$	±0.6			±0.6			V

Note 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

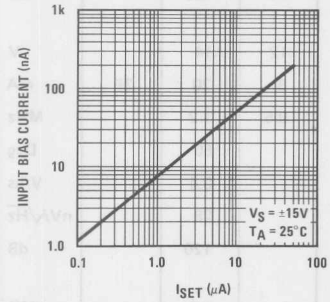
Note 2: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{jMAX}, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d = (T_{jMAX} - T_A)/\theta_{jA}$ or the 25°C P_{dMAX}, whichever is less.

Note 3: Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

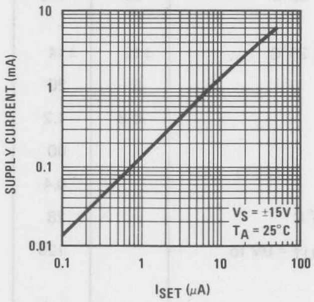
Note 4: These specifications apply over the absolute maximum operating temperature range unless otherwise noted.

Typical Performance Characteristics

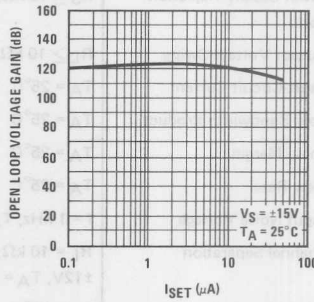
Input Bias Current vs I_{SET}



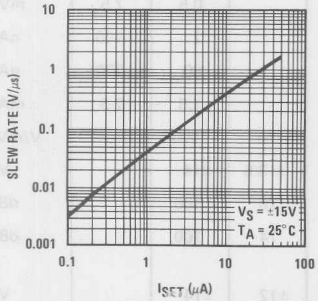
Supply Current vs I_{SET}



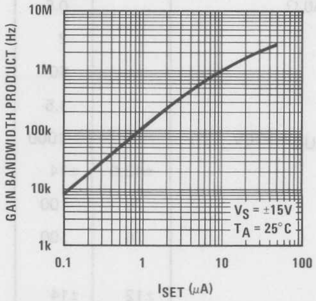
Open Loop Voltage Gain vs I_{SET}



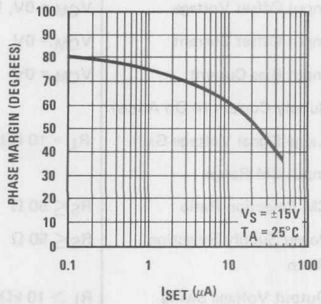
Slew Rate vs I_{SET}



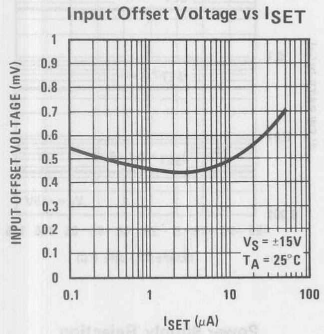
Gain Bandwidth Product vs I_{SET}

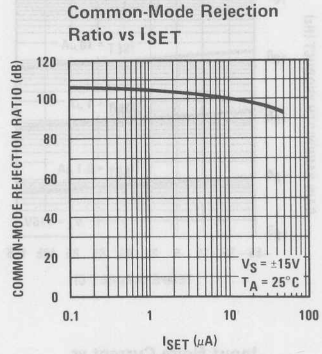


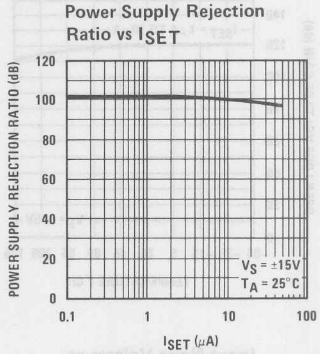
Phase Margin vs I_{SET}

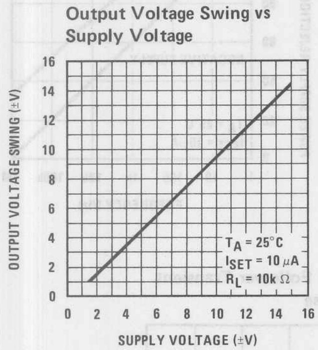


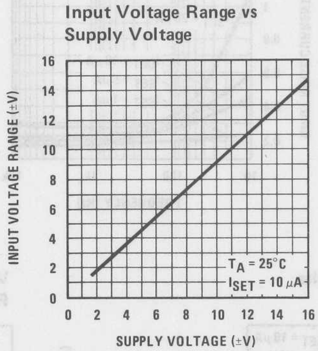
Typical Performance Characteristics (Continued)

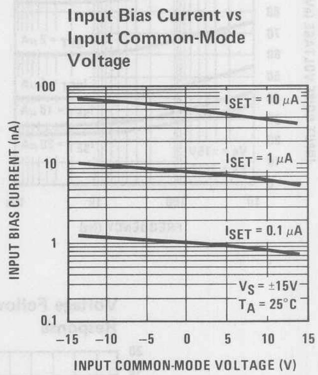


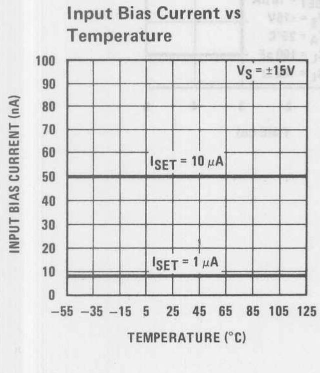


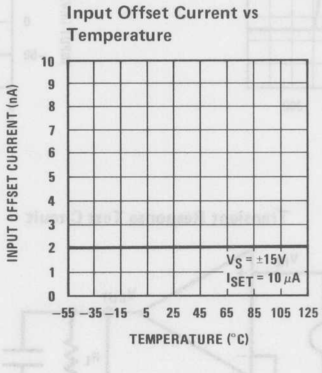


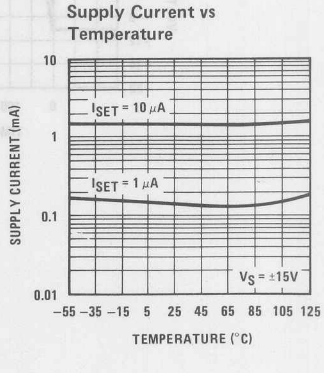






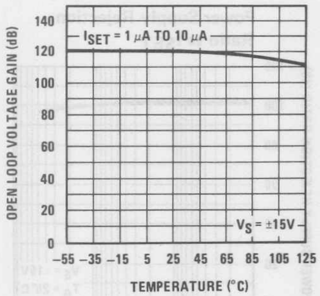




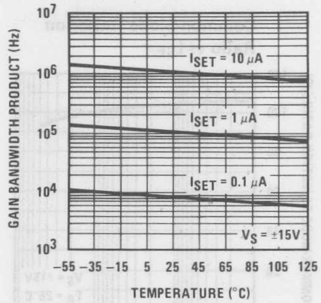


Typical Performance Characteristics (Continued)

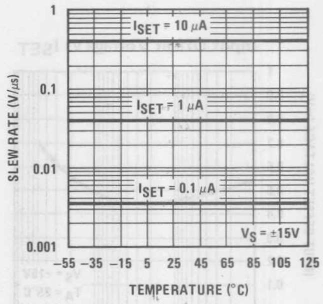
Open Loop Voltage Gain vs Temperature



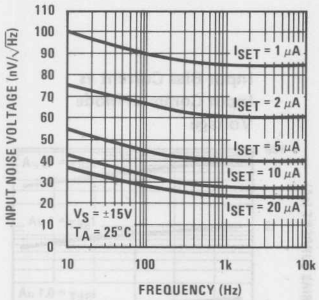
Gain Bandwidth Product vs Temperature



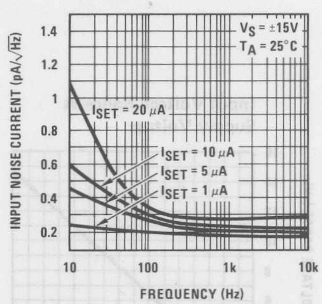
Slew Rate vs Temperature



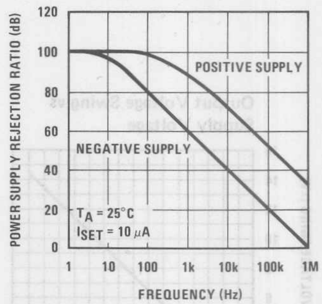
Input Noise Voltage vs Frequency



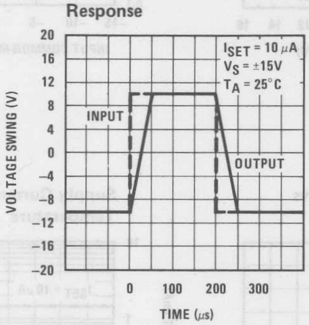
Input Noise Current vs Frequency



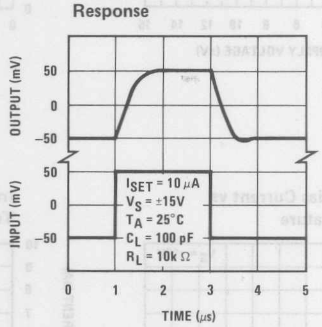
Power Supply Rejection Ratio vs Frequency



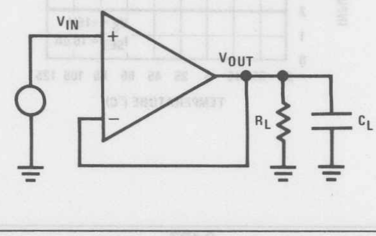
Voltage Follower Pulse Response



Voltage Follower Transient Response



Transient Response Test Circuit



Application Hints

Avoid reversing the power supply polarity, the device will fail.

Common-Mode Input Voltage: The negative common-mode voltage limit is one diode drop above the negative supply voltage. Exceeding this limit on either input will result in an output phase reversal. The positive common-mode limit is typically 1V below the positive supply voltage. No output phase reversal will occur if this limit is exceeded by either input.

Output Voltage Swing vs I_{SET}: For a desired output voltage swing the value of the minimum load depends on the positive and negative output curent capability of the op amp. The maximum available positive output current, (I_{CL+}), of the device increases with I_{SET} whereas the negative output current (I_{CL-}) is independent of I_{SET}. *Figure 1* illustrates the above.

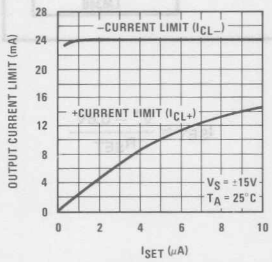


FIGURE 1. Output Current Limit vs I_{SET}

Input Capacitance: The input capacitance, C_{IN}, of the LM146 is approximately 2 pF; any stray capacitance, C_S, (due to external circuit circuit layout) will add to C_{IN}. When resistive or active feedback is applied, an additional pole is added to the open loop frequency response of the device. For instance with resistive feedback *(Figure 2)*, this pole occurs at $1/2\pi$ (R1||R2) (C_{IN} + C_S). Make sure that this pole occurs at least 2 octaves beyond the expected −3 dB frequency corner of the closed loop gain of the amplifier; if not, place a lead capacitor in the feedback such that the time constant of this capacitor and the resistance it parallels is equal to the $R_I(C_S + C_{IN})$, where R_I is the input resistance of the circuit.

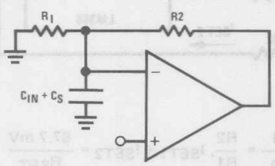


FIGURE 2

Temperature Effect on the GBW: The GBW (gain bandwidth product), of the LM146 is directly proportional to I_{SET} and inversely proportional to the absolute temperature. When using resistors to set the bias current, I_{SET}, of the device, the GBW product will decrease with increasing temperature. Compensation can be provided by creating an I_{SET} current directly proportional to temperature (see typical applications).

Isolation Between Amplifiers: The LM146 die is isothermally layed out such that crosstalk between *all 4* amplifiers is in excess of −105 dB (DC). Optimum isolation (better than −110 dB) occurs between amplifiers A and D, B and C; that is, if amplifier A dissipates power on its output stage, amplifier D is the one which will be affected the least, and vice versa. Same argument holds for amplifiers B and C.

LM146 Typical Performance Summary: The LM146 typical behavior is shown in *Figure 3*. The device is fully predictable. As the set current, I_{SET}, increases, the speed, the bias current, and the supply current increase while the noise power decreases proportionally and the V_{OS} remains constant. The usable GBW range of the op amp is 10 kHz to 3.5–4 MHz.

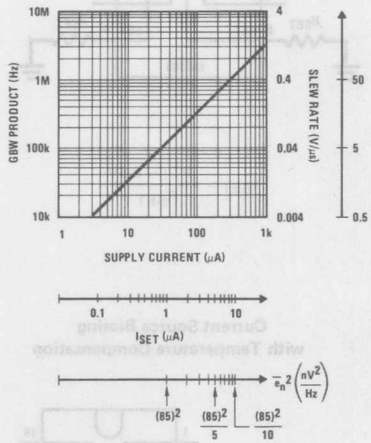


FIGURE 3. LM146 Typical Characteristics

Low Power Supply Operation: The quad op amp operates down to ±1.3V supply. Also, since the internal circuitry is biased through programmable current sources, no degradation of the device speed will occur.

Speed vs Power Consumption: LM146 vs LM4250 (single programmable). Through *Figure 4*, we observe that the LM146's power consumption has been optimized for GBW products above 200 kHz, whereas the LM4250 will reach a GBW of no more than 300 kHz, for GBW products below 200 kHz, the LM4250 will consume less.

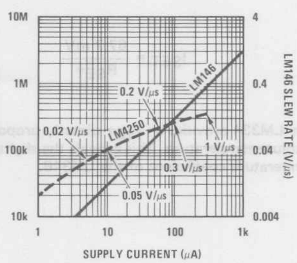
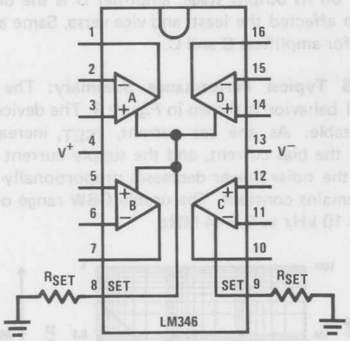


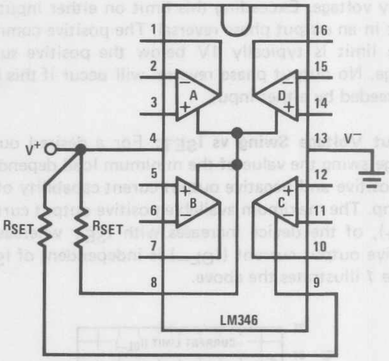
FIGURE 4. LM146 vs LM4250

Dual Supply or Negative Supply Biasing



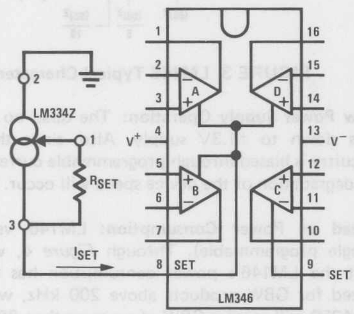
$$I_{SET} \simeq \frac{|V^-| - 0.6V}{R_{SET}}$$

Single (Positive) Supply Biasing



$$I_{SET} \simeq \frac{V^+ - 0.6V}{R_{SET}}$$

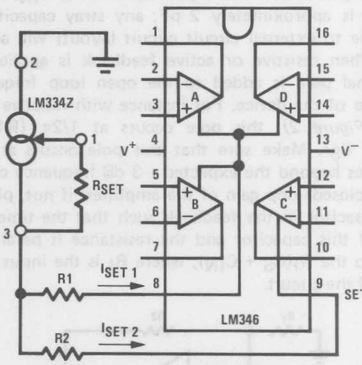
Current Source Biasing with Temperature Compensation



$$I_{SET} = \frac{67.7\ mV}{R_{SET}}$$

- The LM334 provides an I_{SET} directly proportional to absolute temperature. This cancels the slight GBW product temperature coefficient of the LM346.

Biasing all 4 Amplifiers with Single Current Source

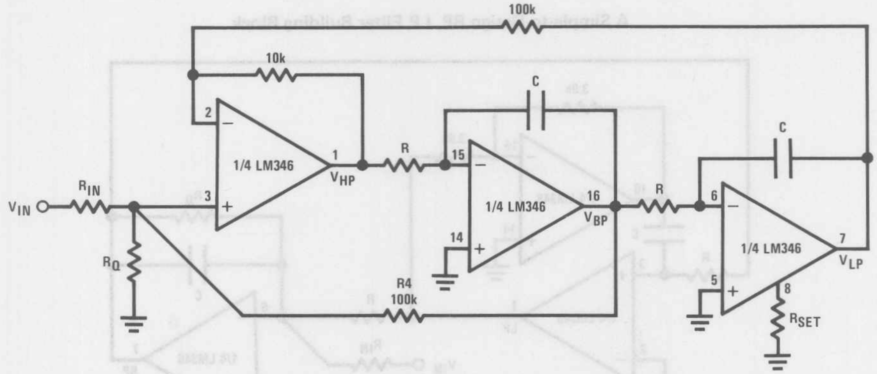


$$\frac{I_{SET1}}{I_{SET2}} = \frac{R2}{R1},\ I_{SET1} + I_{SET2} = \frac{67.7\ mV}{R_{SET}}$$

- For $I_{SET1} \approx I_{SET2}$ resistors R1 and R2 are not required if a slight error between the 2 set currents can be tolerated. If not, then use R1 = R2 to create a 100 mV drop across these resistors.

Active Filters Applications

Basic (Non-Inverting "State Variable") Active Filter Building Block



- The LM146 quad programmable op amp is especially suited for active filters because of their adequate GBW product and low power consumption.

  Circuit synthesis equations (for circuit analysis equations, consult with the AF100 and LM148 data sheet).

  Need to know desired: f_o = center frequency measured at the BP output
  Q_o = quality factor measured at the BP output
  H_o = gain at the output of interest (BP or HP or LP or all of them)

  ▲ Relation between different gains: $H_{o(BP)} = 0.316 \times Q_o \times H_{o(LP)}$; $H_{o(LP)} = 10 \times H_{o(HP)}$

  ▲ $R \times C = \dfrac{5.033 \times 10^{-2}}{f_o}$ (sec)

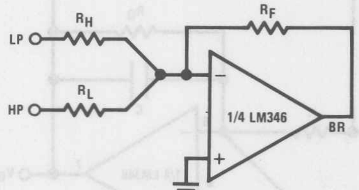
  ▲ For BP output: $R_Q = \left(\dfrac{3.478\ Q_o - H_{o(BP)}}{10^5} - \dfrac{H_{o(BP)}}{10^5 \times 3.478 \times Q_o}\right)^{-1}$; $R_{IN} = \dfrac{\left(\dfrac{3.478\ Q_o}{H_{o(BP)}} - 1\right)}{\dfrac{1}{R_Q} + 10^{-5}}$

  ▲ For HP output: $R_Q = \dfrac{1.1 \times 10^5}{3.478\ Q_o\ (1.1 - H_{o(HP)}) - H_{o(HP)}}$; $R_{IN} = \dfrac{\dfrac{1.1}{H_{o(HP)}} - 1}{\dfrac{1}{R_Q} + 10^{-5}}$

  Note. All resistor values are given in ohms.

  ▲ For LP output: $R_Q = \dfrac{11 \times 10^5}{3.478\ Q_o\ (11 - H_{o(LP)}) - H_{o(LP)}}$; $R_{IN} = \dfrac{\dfrac{11}{H_{o(LP)}} - 1}{\dfrac{1}{R_Q} + 10^{-5}}$

  ▲ For BR (notch) output: Use the 4th amplifier of the LM146 to sum the LP and HP outputs of the basic filter.



$$\sqrt{\frac{R_H}{R_L}} = 0.316\ \frac{f_{notch}}{f_o}$$

  Determine R_F according to the desired gains: $H_{o(BR)}\Big|_{f << f_{notch}} = \dfrac{R_F}{R_L} H_{o(LP)}$, $H_{o(BR)}\Big|_{f >> f_{notch}} = \dfrac{R_F}{R_H} H_{o(HP)}$

- **Where to use amplifier C:** Examine the above gain relations and determine the dynamics of the filter. Do not allow slew rate limiting in any output (V_{HP}, V_{BP}, V_{LP}), that is:

  $V_{IN(peak)} < 63.66 \times 10^3 \times \dfrac{I_{SET}}{10\ \mu A} \times \dfrac{1}{f_o \times H_o}$ (Volts)

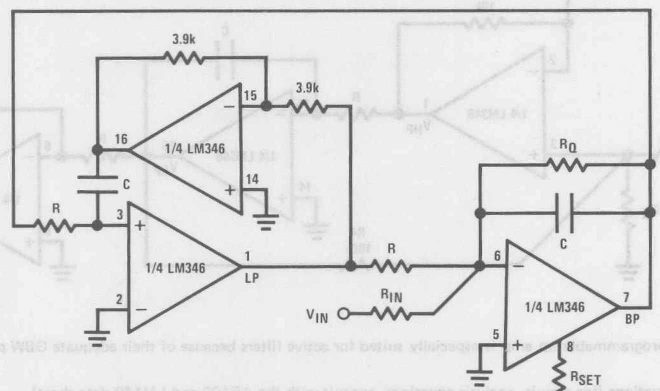
  If necessary, use amplifier C, biased at higher I_{SET}, where you get the largest output swing.

  Deviation from Theoretical Predictions: Due to the finite GBW products of the op amps the f_o, Q_o will be slightly different from the theoretical predictions.

  $f_{real} \simeq \dfrac{f_o}{1 + \dfrac{2\ f_o}{GBW}}$, $Q_{real} \simeq \dfrac{Q_o}{1 - \dfrac{3.2\ f_o \times Q_o}{GBW}}$

Active Filters Applications (Continued)

A Simple-to-Design BP, LP Filter Building Block



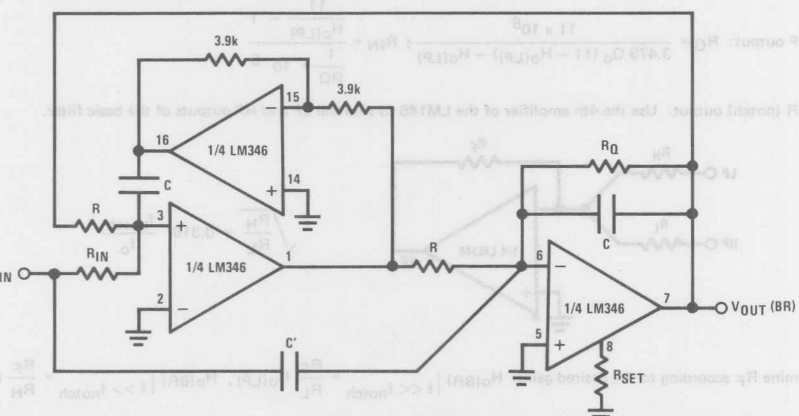
- If resistive biasing is used to set the LM346 performance, the Q_O of this filter building block is nearly insensitive to the op amp's GBW product temperature drift; it has also better noise performance than the state variable filter.

Circuit Synthesis Equations

$$H_{O(BP)} = Q_O H_{O(LP)};\ R \times C = \frac{0.159}{f_O};\ R_Q = Q_O \times R;\ R_{IN} = \frac{R_Q}{H_{O(BP)}} = \frac{R}{H_{O(LP)}}$$

- For the eventual use of amplifier C, see comments on the previous page.

A 3-Amplifier Notch Filter (or Elliptic Filter Building Block)



Circuit Synthesis Equations

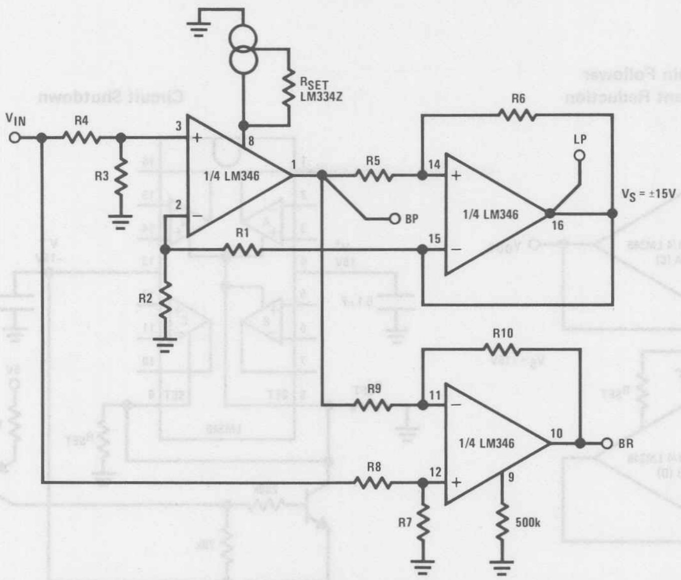
$$R \times C = \frac{0.159}{f_O};\ R_Q = Q_O \times R;\ R_{IN} = \frac{0.159 \times f_O}{C' \times f^2_{notch}}$$

$$H_{O(BR)}\Big|_{f << f_{notch}} = \frac{R}{R_{IN}} \qquad H_{O(BR)}\Big|_{f >> f_{notch}} = \frac{C'}{C}$$

- For nothing but a notch output: $R_{IN} = R$, $C' = C$.

Active Filters Applications (Continued)

Capacitorless Active Filters (Basic Circuit)

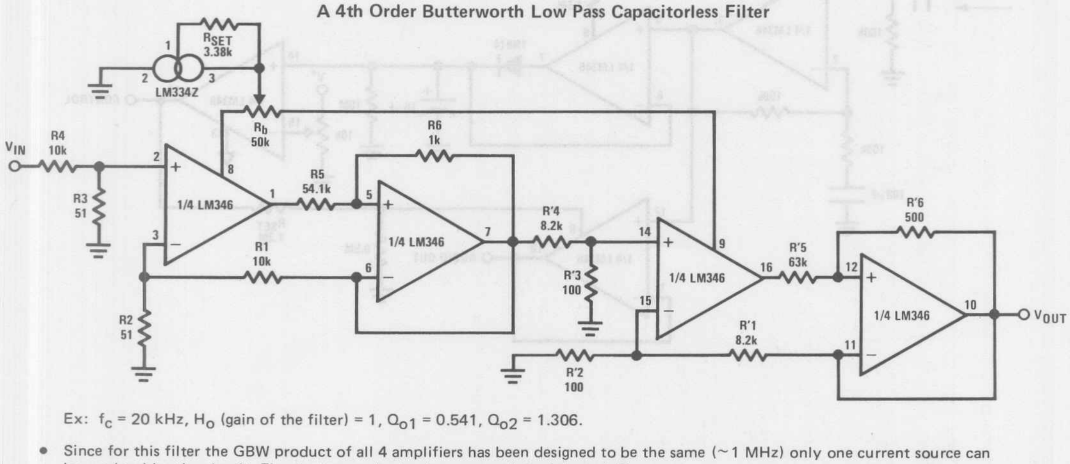


- This is a BP, LP, BR filter. The filter characteristics are created by using the tunable frequency response of the LM346.
- **Limitations:** $Q_o < 10$, $f_o \times Q_o < 1.5$ MHz, output voltage should not exceed $\text{Vpeak(out)} \leq \dfrac{63.66 \times 10^3}{f_o} \times \dfrac{I_{SET}\ (\mu A)}{10\ \mu A}$ (V)
- Design equations: $a = \dfrac{R6 + R5}{R6}$, $b = \dfrac{R2}{R1 + R2}$, $c = \dfrac{R3}{R3 + R4}$, $d = \dfrac{R7}{R8 + R7}$, $e = \dfrac{R10}{R9 + R10}$, $f_{o(BP)} = f_u \sqrt{\dfrac{b}{a}}$, $H_{o(BP)} = a \times c$,

  $H_{o(LP)} = \dfrac{c}{b}$, $Q_o = \sqrt{a \times b}$

  $f_{o(BR)} = f_{o(BP)} \left(1 - \dfrac{c}{b}\right) \simeq f_{o(BP)}$ $(C << 1)$ provided that $d = H_{o(BP)} \times e$, $H_{o(BR)} = \dfrac{R10}{R9}$.
- Advantage: f_o, Q_o, H_o can be independently adjusted; that is, the filter is extremely easy to tune.
- Tuning procedure (ex. BP tuning)
  1. Pick up a convenient value for b; $(b < 1)$
  2. Adjust Q_o through R5
  3. Adjust $H_{o(BP)}$ through R4
  4. Adjust f_o through R_{SET}

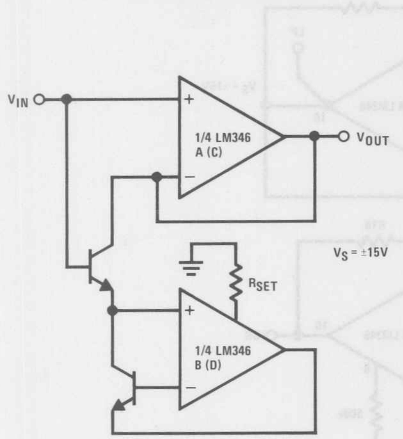
A 4th Order Butterworth Low Pass Capacitorless Filter



Ex: $f_c = 20$ kHz, H_o (gain of the filter) = 1, $Q_{o1} = 0.541$, $Q_{o2} = 1.306$.

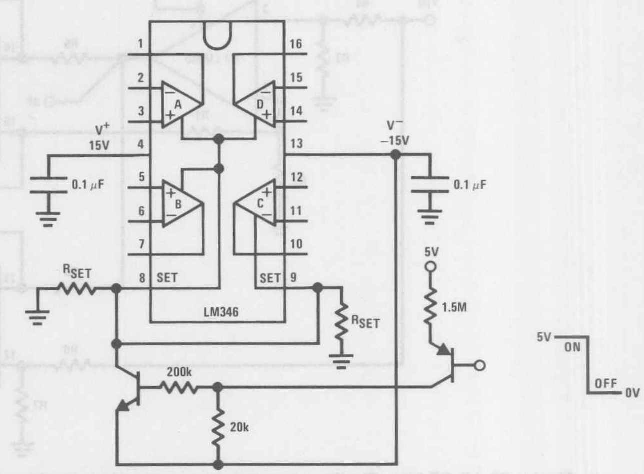
- Since for this filter the GBW product of all 4 amplifiers has been designed to be the same (~1 MHz) only one current source can be used to bias the circuit. Fine tuning can be further accomplished through R_b.

A Unity Gain Follower with Bias Current Reduction



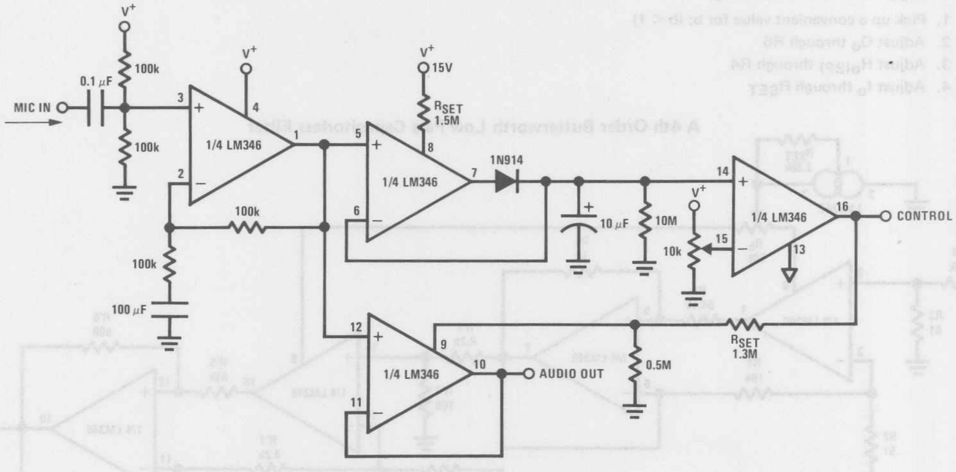
- For better performance, use a matched NPN pair.

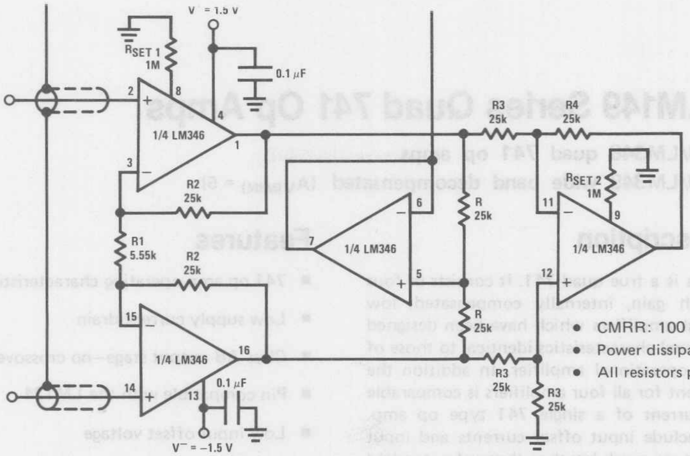
Circuit Shutdown



- By pulling the SET pin(s) to V^- the op amp(s) shuts down and its output goes to a high impedance state. According to this property, the LM346 can be used as a very low speed analog switch.

Voice Activated Switch and Amplifier





- CMRR: 100 dB (typ)
- Power dissipation: 0.4 mW
- All resistors part of RA201 array

National Semiconductor

Operational Amplifiers/Buffers

LM148, LM149 Series Quad 741 Op Amps

LM148/LM248/LM348 quad 741 op amps
LM149/LM249/LM349 wide band decompensated ($A_{V(MIN)} = 5$)

General Description

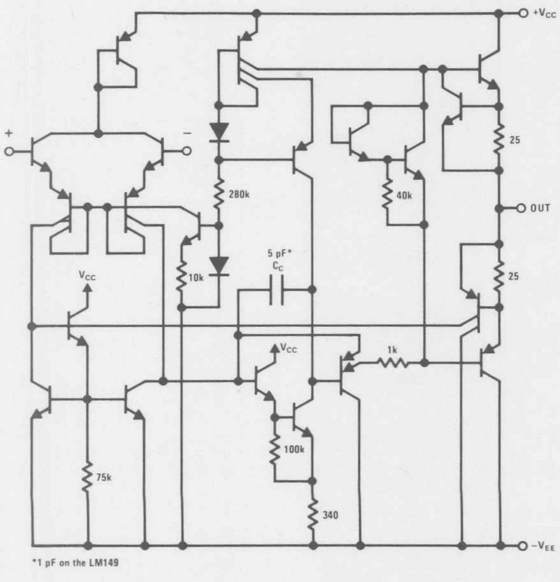
The LM148 series is a true quad 741. It consists of four independent, high gain, internally compensated, low power operational amplifiers which have been designed to provide functional characteristics identical to those of the familiar 741 operational amplifier. In addition the total supply current for all four amplifiers is comparable to the supply current of a single 741 type op amp. Other features include input offset currents and input bias current which are much less than those of a standard 741. Also, excellent isolation between amplifiers has been achieved by independently biasing each amplifier and using layout techniques which minimize thermal coupling. The LM149 series has the same features as the LM148 plus a gain bandwidth product of 4 MHz at a gain of 5 or greater.

The LM148 can be used anywhere multiple 741 or 1558 type amplifiers are being used and in applications where amplifier matching or high packing density is required.

Features

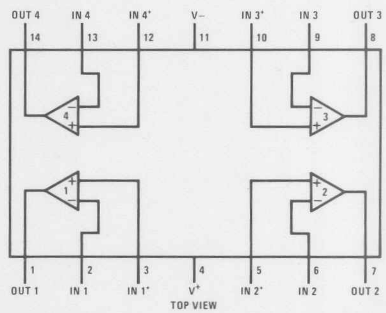
- 741 op amp operating characteristics
- Low supply current drain 0.6 mA/Amplifier
- Class AB output stage—no crossover distortion
- Pin compatible with the LM124
- Low input offset voltage 1 mV
- Low input offset current 4 nA
- Low input bias current 30 nA
- Gain bandwidth product
  - LM148 (unity gain) 1.0 MHz
  - LM149 ($A_V \geq 5$) 4 MHz
- High degree of isolation between amplifiers 120 dB
- Overload protection for inputs and outputs

Schematic and Connection Diagrams



*1 pF on the LM149

Dual-In-Line Package



TOP VIEW

Order Number LM148J, LM248J, LM348J, LM149J, LM249J or LM349J
See NS Package J14A
Order Number LM348N or LM349N
See NS Package N14A

LM148, LM149 Series

Absolute Maximum Ratings

	LM148/LM149	LM248/LM249	LM348/LM349
Supply Voltage	±22V	±18V	±18V
Differential Input Voltage	±44V	±36V	±36V
Input Voltage	±22V	±18V	±18V
Output Short Circuit Duration (Note 1)	Continuous	Continuous	Continuous
Power Dissipation (P_d at 25°C) and Thermal Resistance (θ_{jA}), (Note 2)			
Molded DIP (N) P_d	—	—	500 mW
θ_{jA}	—	—	150°C/W
Cavity DIP (J) P_d	900 mW	900 mW	900 mW
θ_{jA}	100°C/W	100°C/W	100°C/W
Maximum Junction Temperature (T_{jMAX})	150°C	110°C	100°C
Operating Temperature Range	$-55°C \le T_A \le +125°C$	$-25°C \le T_A \le +85°C$	$0°C \le T_A \le +70°C$
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	300°C	300°C	300°C

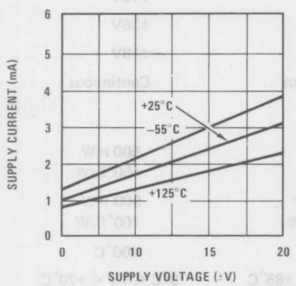
Electrical Characteristics (Note 3)

PARAMETER	CONDITIONS	LM148/LM149 MIN	LM148/LM149 TYP	LM148/LM149 MAX	LM248/LM249 MIN	LM248/LM249 TYP	LM248/LM249 MAX	LM348/LM349 MIN	LM348/LM349 TYP	LM348/LM349 MAX	UNITS
Input Offset Voltage	$T_A = 25°C$, $R_S \le 10\ k\Omega$		1.0	5.0		1.0	6.0		1.0	6.0	mV
Input Offset Current	$T_A = 25°C$		4	25		4	50		4	50	nA
Input Bias Current	$T_A = 25°C$		30	100		30	200		30	200	nA
Input Resistance	$T_A = 25°C$	0.8	2.5		0.8	2.5		0.8	2.5		MΩ
Supply Current All Amplifiers	$T_A = 25°C$, $V_S = \pm 15V$		2.4	3.6		2.4	4.5		2.4	4.5	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \ge 2\ k\Omega$	50	160		25	160		25	160		V/mV
Amplifier to Amplifier Coupling	$T_A = 25°C$, f = 1 Hz to 20 kHz (Input Referred) See Crosstalk Test Circuit		−120			−120			−120		dB
Small Signal Bandwidth	$T_A = 25°C$ LM148 series		1.0			1.0			1.0		MHz
	LM149 series		4.0			4.0			4.0		MHz
Phase Margin	$T_A = 25°C$ LM148 series ($A_V = 1$)		60			60			60		degrees
	LM149 series ($A_V = 5$)		60			60			60		degrees
Slew Rate	$T_A = 25°C$ LM148 series ($A_V = 1$)		0.5			0.5			0.5		V/µs
	LM149 series ($A_V = 5$)		2.0			2.0			2.0		V/µs
Output Short Circuit Current	$T_A = 25°C$		25			25			25		mA
Input Offset Voltage	$R_S \le 10\ k\Omega$			6.0			7.5			7.5	mV
Input Offset Current				75			125			100	nA
Input Bias Current				325			500			400	nA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L > 2\ k\Omega$	25			15			15			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$,	±12	±13		±12	±13		±12	±13		V
	$R_L = 2\ k\Omega$	±10	±12		±10	±12		±10	±12		V
Input Voltage Range	$V_S = \pm 15V$	±12			±12			±12			V
Common-Mode Rejection Ratio	$R_S \le 10\ k\Omega$	70	90		70	90		70	90		dB
Supply Voltage Rejection	$R_S \le 10\ k\Omega$	77	96		77	96		77	96		dB

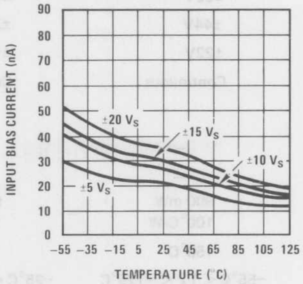
Note 1. Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 2: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{jMAX}, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d = (T_{jMAX} - T_A)/\theta_{jA}$ or the 25°C P_{dMAX}, whichever is less.

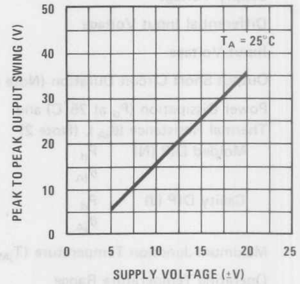
Note 3: These specifications apply for $V_S = \pm 15V$ and over the absolute maximum operating temperature range ($T_L \le T_A \le T_H$) unless otherwise noted.



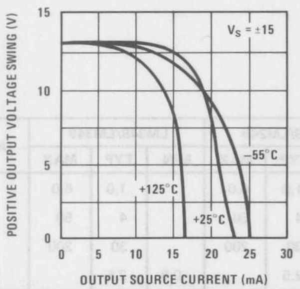
Input Bias Current



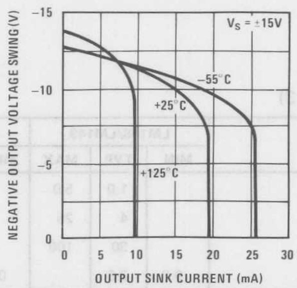
Voltage Swing



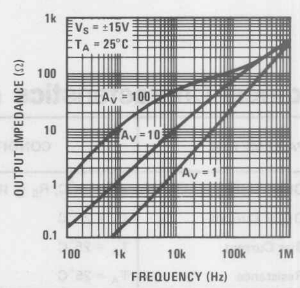
Positive Current Limit



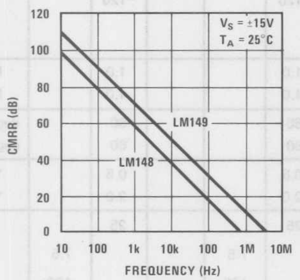
Negative Current Limit



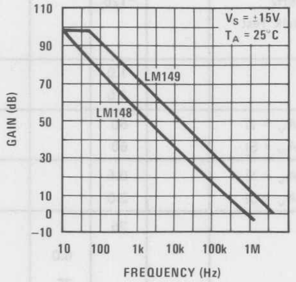
Output Impedance



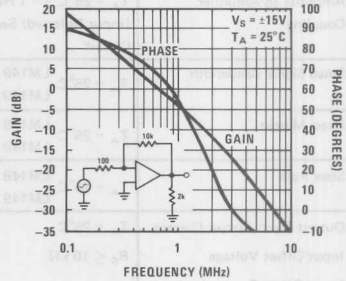
Common-Mode Rejection Ratio



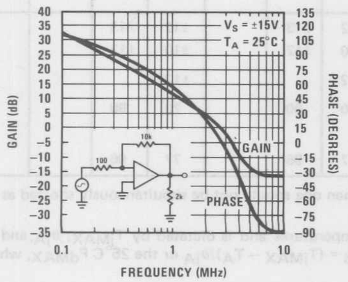
Open Loop Frequency Response



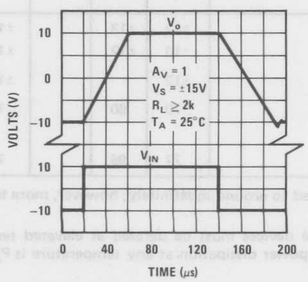
Bode Plot LM148



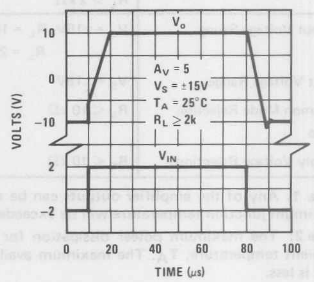
Bode Plot LM149



Large Signal Pulse Response (LM148)

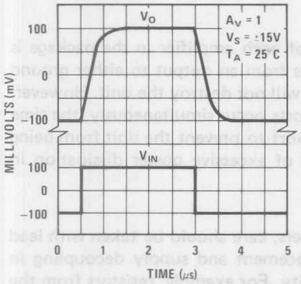


Large Signal Pulse Response (LM149)

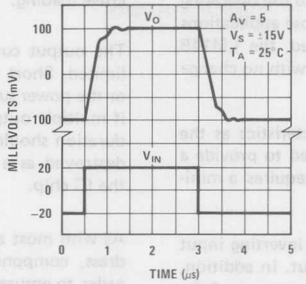


Typical Performance Characteristics (Continued)

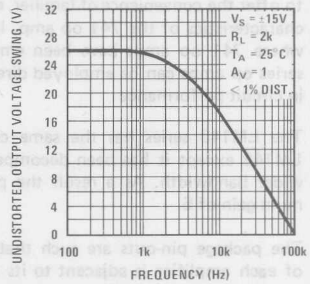
Small Signal Pulse Response (LM148)



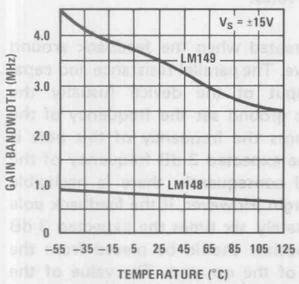
Small Signal Pulse Response (LM149)



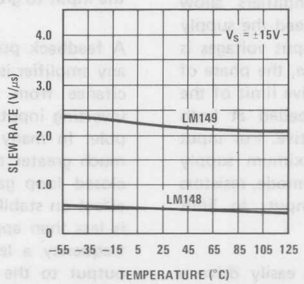
Undistorted Output Voltage Swing



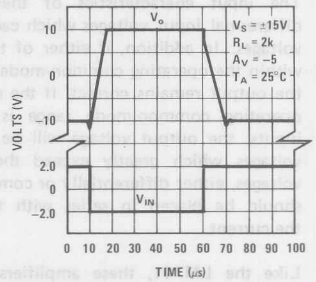
Gain Bandwidth



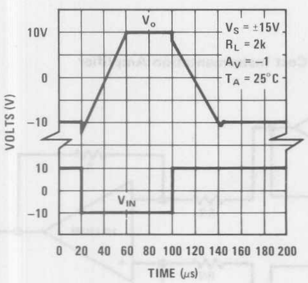
Slew Rate



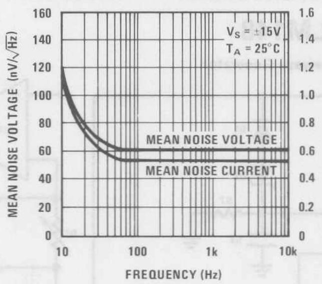
Inverting Large Signal Pulse Response (LM149)



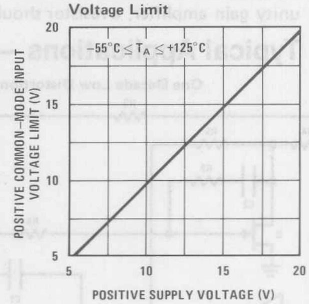
Inverting Large Signal Pulse Response (LM148)



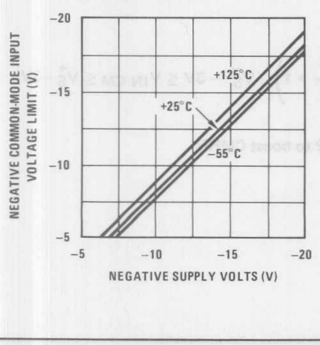
Input Noise Voltage and Noise Current



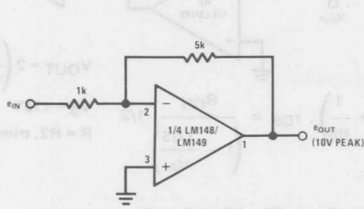
Positive Common-Mode Input Voltage Limit

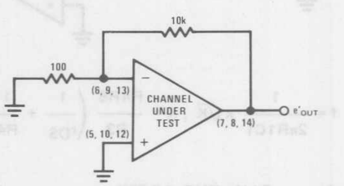


Negative Common-Mode Input Voltage Limit



Cross Talk Test Circuits





$$\text{Crosstalk} = -20 \log \frac{e'OUT}{101 \times e_{OUT}} \ (\text{dB})$$

$V_S = \pm 15V$

Application Hints

The LM148 series are quad low power 741 op amps. In the proliferation of quad op amps, these are the first to offer the convenience of familiar, easy to use operating characteristics of the 741 op amp. In those applications where 741 op amps have been employed, the LM148 series op amps can be employed directly with no change in circuit performance.

The LM149 series has the same characteristics as the LM148 except it has been decompensated to provide a wider bandwidth. As a result the part requires a minimum gain of 5.

The package pin-outs are such that the inverting input of each amplifier is adjacent to its output. In addition, the amplifier outputs are located in the corners of the package which simplifies PC board layout and minimizes package related capacitive coupling between amplifiers.

The input characteristics of these amplifiers allow differential input voltages which can exceed the supply voltages. In addition, if either of the input voltages is within the operating common-mode range, the phase of the output remains correct. If the negative limit of the operating common-mode range is exceeded at both inputs, the output voltage will be positive. For input voltages which greatly exceed the maximum supply voltages, either differentially or common-mode, resistors should be placed in series with the inputs to limit the current.

Like the LM741, these amplifiers can easily drive a 100 pF capacitive load throughout the entire dynamic output voltage and current range. However, if very large capacitive loads must be driven by a non-inverting unity gain amplifier, a resistor should be placed between the output (and feedback connection) and the capacitance to reduce the phase shift resulting from the capacitive loading.

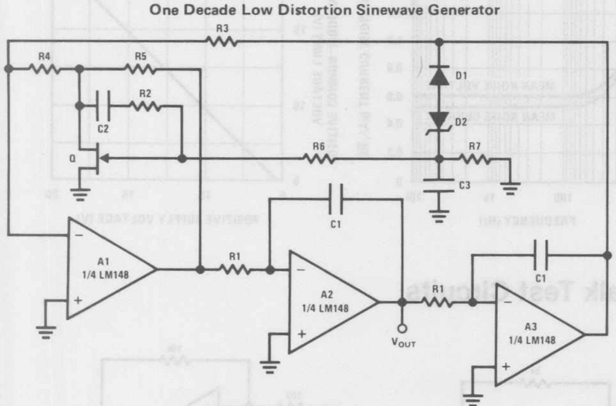
The output current of each amplifier in the package is limited. Short circuits from an output to either ground or the power supplies will not destroy the unit. However, if multiple output shorts occur simultaneously, the time duration should be short to prevent the unit from being destroyed as a result of excessive power dissipation in the IC chip.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole which capacitance from the input to ground creates.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Applications — LM148

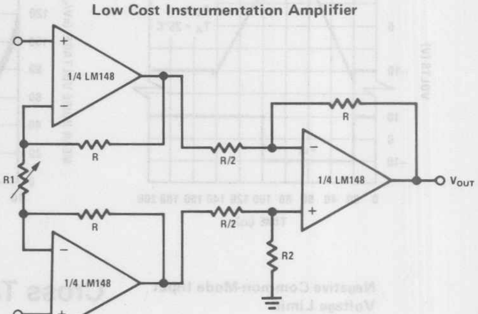
One Decade Low Distortion Sinewave Generator



$$f = \frac{1}{2\pi R1C1} \times \sqrt{K},\ K = \frac{R4R5}{R3}\left(\frac{1}{r_{DS}} + \frac{1}{R4} + \frac{1}{R5}\right),\ r_{DS} \cong \frac{R_{ON}}{\left(1 - \frac{V_{GS}}{V_P}\right)^{1/2}}$$

f_{MAX} = 5 kHz, THD ≤ 0.03%
R1 = 100k pot., C1 = 0.0047µF, C2 = 0.01µF, C3 = 0.1µF, R2 = R6 = R7 = 1M, R3 = 5.1k, R4 = 12Ω, R5 = 240Ω, Q = NS5102, D1 = 1N914, D2 = 3.6V avalanche diode (ex. LM103), V_S = ±15V
A simpler version with some distortion degradation at high frequencies can be made by using A1 as a simple inverting amplifier, and by putting back to back zeners in the feedback loop of A3.

Low Cost Instrumentation Amplifier

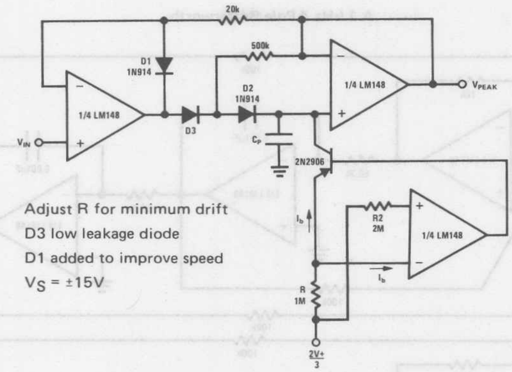


$$V_{OUT} = 2\left(\frac{2R}{R1} + 1\right),\ V_S^- - 3V \le V_{IN\ CM} \le V_S^+ - 3V,$$

V_S = ±15V
R = R2, trim R2 to boost CMRR

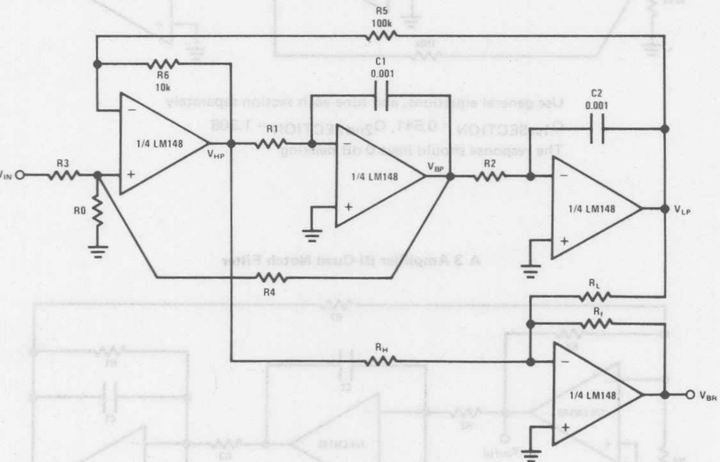
Typical Applications — LM148 (Continued)

Low Drift Peak Detector with Bias Current Compensation



Adjust R for minimum drift
D3 low leakage diode
D1 added to improve speed
$V_S = \pm 15V$

Universal State-Space Filter



Tune Q through R0,
For predictable results: $f_O\,Q \le 4 \times 10^4$
Use Band Pass output to tune for Q

$$\frac{V_{(s)}}{V_{IN(s)}} = \frac{N(s)}{D(s)}, \quad D(s) = S^2 + \frac{S\omega_o}{Q} + \omega_o^2$$

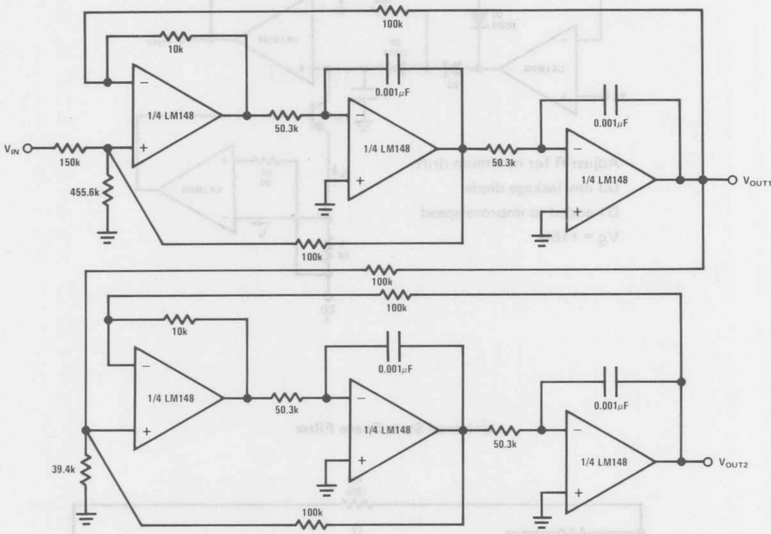
$$N_{HP(s)} = S^2 H_{OHP}, \quad N_{BP(s)} = \frac{-S\omega_O H_{OBP}}{Q} \quad N_{LP} = \omega_o^2 H_{OLP}$$

$$f_o = \frac{1}{2\pi}\sqrt{\frac{R6}{R5}}\sqrt{\frac{1}{t1t2}}, \quad t_i = R_iC_i, \quad Q = \left(\frac{1 + R4/R3 + R4/R0}{1 + R6/R5}\right)\left(\frac{R6}{R5}\,\frac{t_1}{t_2}\right)^{1/2}$$

$$f_{NOTCH} = \frac{1}{2\pi}\left(\frac{R_H}{R_L t_1 t_2}\right)^{1/2}, \quad H_{OHP} = \frac{1 + R6/R5}{1 + R3/R0 + R3/R4}, \quad H_{OBP} = \frac{1 + R4/R3 + R4/R0}{1 + R3/R0 + R3/R4}$$

$$H_{OLP} = \frac{1 + R5/R6}{1 + R3/R0 + R3/R4}$$

A 1 kHz 4 Pole Butterworth

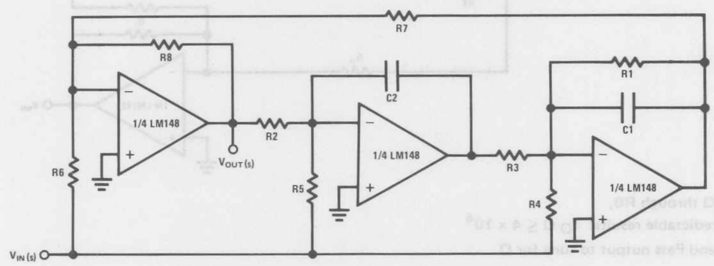


Use general equations, and tune each section separately

$Q_{1stSECTION} = 0.541,\ Q_{2ndSECTION} = 1.306$

The response should have 0 dB peaking

A 3 Amplifier Bi-Quad Notch Filter

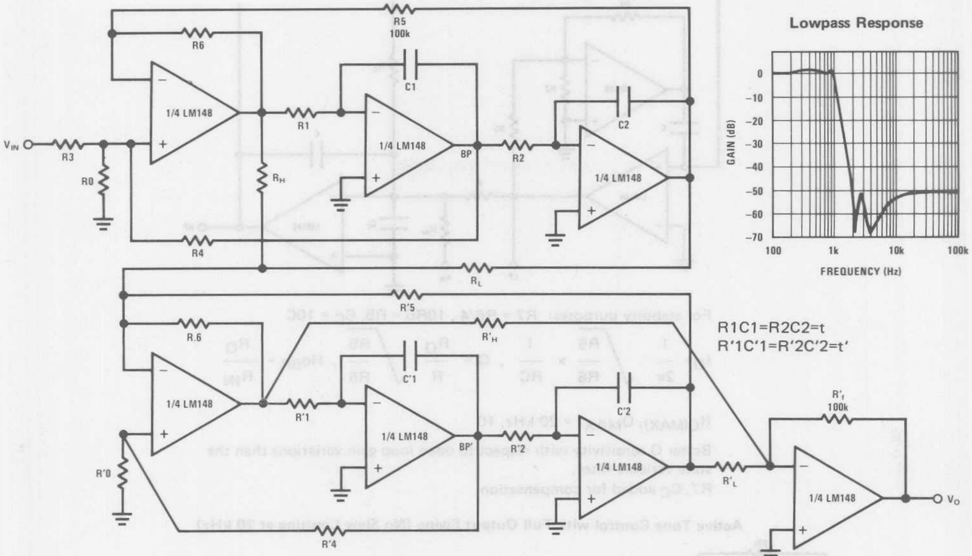


$$Q = \sqrt{\frac{R8}{R7}} \times \frac{R1C1}{\sqrt{R3C2R2C1}},\quad f_o = \frac{1}{2\pi}\sqrt{\frac{R8}{R7}} \times \frac{1}{\sqrt{R2R3C1C2}},\quad f_{NOTCH} = \frac{1}{2\pi}\sqrt{\frac{R6}{R3R5R7C1C2}}$$

Necessary condition for notch: $\frac{1}{R6} = \frac{R1}{R4R7}$

Ex: f_{NOTCH} = 3 kHz, Q = 5, R1 = 270k, R2 = R3 = 20k, R4 = 27k, R5 = 20k, R6 = R8 = 10k, R7 = 100k, C1 = C2 = 0.001μF

Better noise performance than the state-space approach



R1C1=R2C2=t
R'1C'1=R'2C'2=t'

f_C = 1 kHz, f_S = 2 kHz, f_P = 0.543, f_Z = 2.14, Q = 0.841, f'_P = 0.987, f'_Z = 4.92, Q' = 4.403, normalized to ripple BW

$$f_P = \frac{1}{2\pi}\sqrt{\frac{R6}{R5}} \times \frac{1}{t},\ f_Z = \frac{1}{2\pi}\sqrt{\frac{R_H}{R_L}} \times \frac{1}{t},\ Q = \left(\frac{1 + R4/R3 + R4/R0}{1 + R6/R5}\right) \times \sqrt{\frac{R6}{R5}},\ Q' = \sqrt{\frac{R'6}{R'5}}\ \frac{1 + R'4/R'0}{1 + R'6/R'5 + R'6/R_P}$$

$$R_P = \frac{R_H R_L}{R_H + R_L}$$

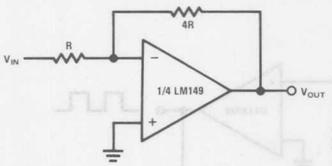
Use the BP outputs to tune Q, Q', tune the 2 sections separately

R1 = R2 = 92.6k, R3 = R4 = R5 = 100k, R6 = 10k, R0 = 107.8k, R_L = 100k, R_H = 155.1k,

R'1 = R'2 = 50.9k, R'4 = R'5 = 100k, R'6 = 10k, R'0 = 5.78k, R'_L = 100k, R'_H = 248.12k, R'f = 100k. All capacitors are 0.001μF.

Typical Applications — LM149

Minimum Gain to Insure LM149 Stability



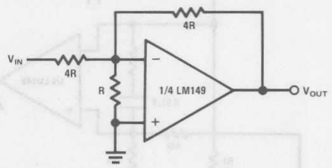
$$A_{CL(S)} = \frac{V_{OUT}}{V_{IN}} = \frac{-4}{\left(1 + \frac{5}{A_{OL(s)}}\right)} \cong -4$$

$$V_O \Big|_{V_{IN}=0} \cong \pm 5\ V_{OS}$$

Power BW = 40 kHz

Small Signal BW = G BW/5

The LM149 as a Unity Gain Inverter



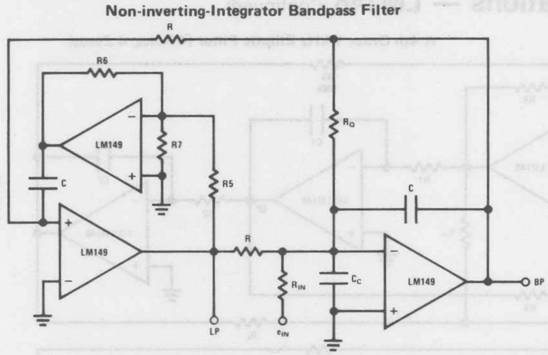
$$A_{CL(s)} = \frac{V_{OUT}}{V_{IN}} = \frac{-1}{\left(1 + \frac{6}{A_{OL(s)}}\right)} \cong -1$$

$$V_O \Big|_{V_{IN}=0} \cong \pm 5\ V_{OS}$$

Small signal BW = G BW/5

Typical Applications — LM149 (Continued)

Non-inverting-Integrator Bandpass Filter



For stability purposes: R7 = R6/4 , 10R6 = R5, C_C = 10C

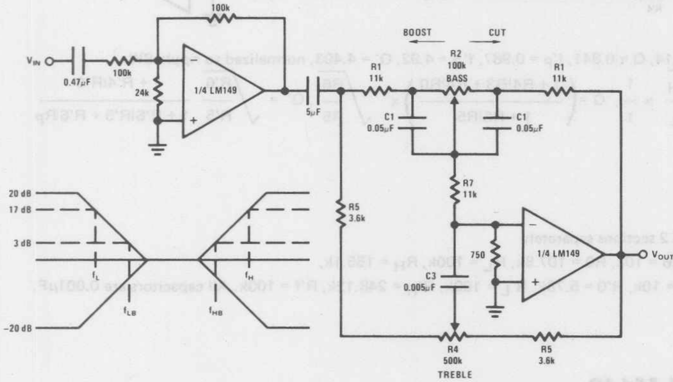
$$f_O = \frac{1}{2\pi}\sqrt{\frac{R5}{R6} \times \frac{1}{RC}},\quad Q = \frac{R_Q}{R}\sqrt{\frac{R5}{R6}},\quad Ho_{BP} = \frac{R_Q}{R_{IN}}$$

$(f_{O(MAX)}, Q_{MAX})$ = 20 kHz, 10

Better Q sensitivity with respect to open loop gain variations than the state variable filter.

R7, C_C added for compensation

Active Tone Control with Full Output Swing (No Slew Limiting at 20 kHz)



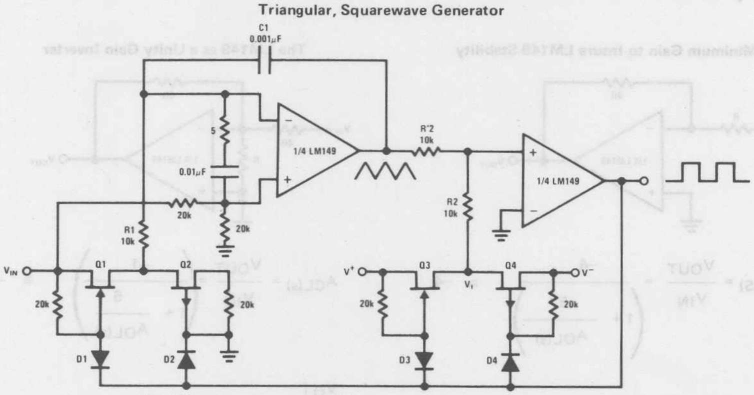
V_S = ±15V, $V_{OUT(MAX)}$ = 9.1 V_{RMS},
f_{MAX} = 20 kHz, THD ≤ 1%
Duplicate the above circuit for stereo

$$f_L = \frac{1}{2\pi R2C1},\quad f_{LB} = \frac{1}{2\pi R1C1}$$

$$f_H = \frac{1}{2\pi R5C3},\quad f_{HB} = \frac{1}{2\pi(R1 + 2R7)\,C3}$$

Max Bass Gain ≅ (R1 + R2)/R1
Max Treble Gain ≅ (R1 + 2R7)/R5
as shown: f_L ≅ 32 Hz, f_{LB} ≅ 320 Hz
f_H ≅ 11 kHz, f_{HB} ≅ 1.1 Hz

Triangular, Squarewave Generator



$$f = \frac{K \times V_{IN}}{8V^+C1R1},\quad K = R2/R'2,\quad \frac{2V_I}{K} \le 25V,\ V^+ = V^-,\ V_S = \pm 15V$$

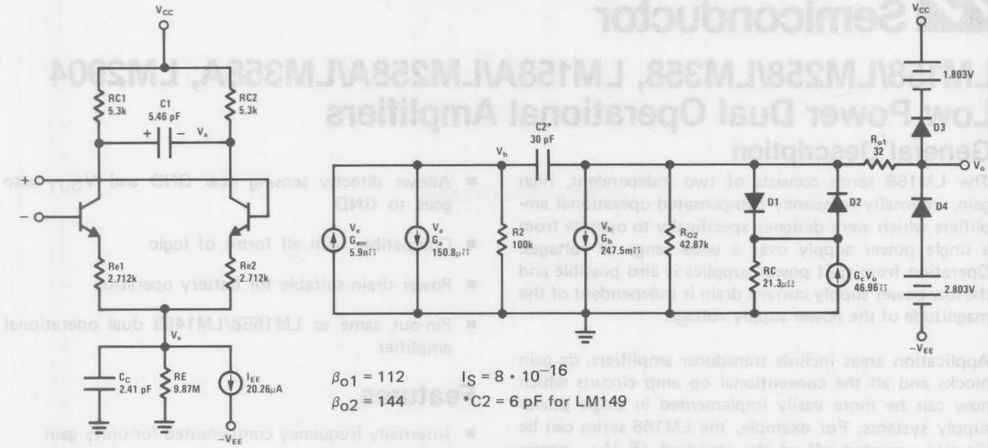
Use LM125 for ±15V supply

The circuit can be used as a low frequency V/F for process control.

Q1, Q3: KE4393, Q2, Q4: P1087E, D1–D4 = 1N914

Typical Simulation

LM148, LM149, LM741 Macromodel for Computer Simulation



$\beta_{O1} = 112$ $\quad I_S = 8 \cdot 10^{-16}$

$\beta_{O2} = 144$ $\quad$ *C2 = 6 pF for LM149

—For more details, see IEEE Journal of Solid-State Circuits, Vol. SC-9, No. 6, December 1974

LM158/LM258/LM358, LM158A/LM258A/LM358A, LM2904 Low Power Dual Operational Amplifiers

General Description

The LM158 series consists of two independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM158 series can be directly operated off of the standard +5 V_{DC} power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15 V_{DC} power supplies.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
- The unity gain cross frequency is temperature compensated.
- The input bias current is also temperature compensated.

Advantages

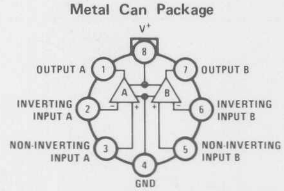
- Eliminates need for dual supplies
- Two internally compensated op amps in a single package
- Allows directly sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation
- Pin-out same as LM1558/LM1458 dual operational amplifier

Features

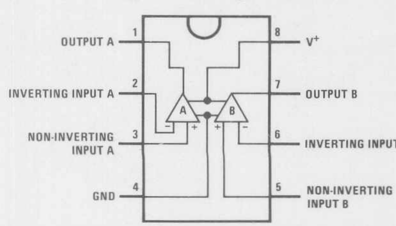
- Internally frequency compensated for unity gain
- Large dc voltage gain — 100 dB
- Wide bandwidth (unity gain) (temperature compensated) — 1 MHz
- Wide power supply range:
  - Single supply — 3 V_{DC} to 30 V_{DC}
  - or dual supplies — ±1.5 V_{DC} to ±15 V_{DC}
- Very low supply current drain (500μA) — essentially independent of supply voltage (1 mW/op amp at +5 V_{DC})
- Low input biasing current (temperature compensated) — 45 nA_{DC}
- Low input offset voltage — 2 mV_{DC}
  and offset current — 5 nA_{DC}
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing — 0 V_{DC} to V^+ − 1.5 V_{DC}

Connection Diagrams (Top Views)

Metal Can Package

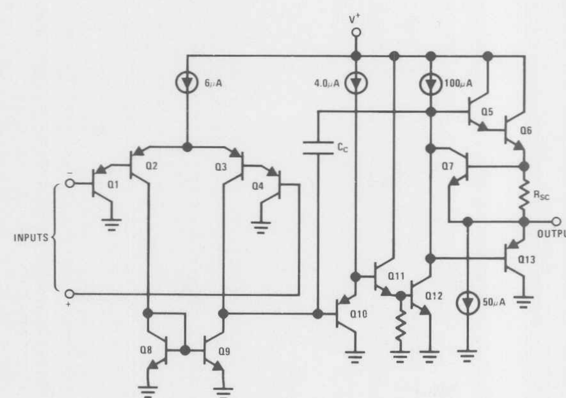


Order Number LM158AH, LM158H, LM258AH, LM258H, LM358AH or LM358H
See NS Package H08C



Order Number LM358AN, LM358N or LM2904N
See NS Package N08B

Schematic Diagram (Each Amplifier)



Absolute Maximum Ratings

	LM158/LM258/LM358 LM158A/LM258A/LM358A	LM2904
Supply Voltage, V^+	32 V_{DC} or ±16 V_{DC}	26 V_{DC} or ±13 V_{DC}
Differential Input Voltage	32 V_{DC}	26 V_{DC}
Input Voltage	−0.3 V_{DC} to +32 V_{DC}	−0.3 V_{DC} to +26 V_{DC}
Power Dissipation (Note 1)		
Molded DIP (LM358N)	570 mW	570 mW
Metal Can (LM158H/LM258H/LM358H)	830 mW	
Output Short-Circuit to GND (One Amplifier) (Note 2) $V^+ \leq 15\ V_{DC}$ and $T_A = 25^\circ C$	Continuous	Continuous
Input Current ($V_{IN} < -0.3\ V_{DC}$) (Note 3)	50 mA	50 mA
Operating Temperature Range		
LM358	0°C to +70°C	−40°C to +85°C
LM258	−25°C to +85°C	
LM158	−55°C to +125°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

Electrical Characteristics ($V^+ = +5.0\ V_{DC}$, Note 4)

PARAMETER	CONDITIONS	LM158A			LM258A			LM358A			LM158/LM258			LM358			LM2904			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25^\circ C$, (Note 5)		1	2		1	3		2	3		±2	±5		±2	±7		±2	±7	mV_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$, $T_A = 25^\circ C$, (Note 6)		20	50		40	80		45	100		45	150		45	250		45	250	nA_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $T_A = 25^\circ C$		2	10		2	15		5	30		±3	±30		±5	±50		±5	±50	nA_{DC}
Input Common-Mode Voltage Range	$V^+ = 30\ V_{DC}$, $T_A = 25^\circ C$ (Note 7)	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	V_{DC}
Supply Current	$R_L = \infty$, $V_{CC} = 30V$ (LM2904 $V_{CC} = 26V$)		1	2		1	2		1	2		1	2		1	2		1	2	mA_{DC}
	$R_L = \infty$ On All Op Amps Over Full Temperature Range		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2	mA_{DC}
Large Signal Voltage Gain	$V^+ = 15\ V_{DC}$ (For Large V_O Swing) $R_L \geq 2\ k\Omega$, $T_A = 25^\circ C$	50	100		50	100		25	100		50	100		25	100			100		V/mV
Output Voltage Swing	$R_L = 2\ k\Omega$, $T_A = 25^\circ C$ (LM2904 $R_L \geq 10\ k\Omega$)	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	V_{DC}
Common-Mode Rejection Ratio	DC, $T_A = 25^\circ C$	70	85		70	85		65	85		70	85		65	70		50	70		dB
Power Supply Rejection Ratio	DC, $T_A = 25^\circ C$	65	100		65	100		65	100		65	100		65	100		50	100		dB
Amplifier-to-Amplifier Coupling	f = 1 kHz to 20 kHz, $T_A = 25^\circ C$ (Input Referred), (Note 8)		−120			−120			−120			−120			−120			−120		dB
Output Current																				
Source	$V_{IN}^+ = 1\ V_{DC}$, $V_{IN}^- = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $T_A = 25^\circ C$	20	40		20	40		20	40		20	40		20	40		20	40		mA_{DC}

Electrical Characteristics (Continued) ($V^+ = +5.0\ V_{DC}$, Note 4)

PARAMETER	CONDITIONS	LM158A			LM258A			LM358A			LM158/LM258			LM358			LM2904			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Sink	$V_{IN}^- = 1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $T_A = 25°C$	10	20		10	20		10	20		10	20		10	20		10	20		mA_{DC}
	$V_{IN}^- = 1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$, $T_A = 25°C$, $V_O = 200\ mV_{DC}$	12	50		12	50		12	50		12	50		12	50					μA_{DC}
Short Circuit to Ground	$T_A = 25°C$, (Note 2)		40	60		40	60		40	60		40	60		40	60		40	60	mA_{DC}
Input Offset Voltage	(Note 5)			4			4			5			±7			±9			±10	mV_{DC}
Input Offset Voltage Drift	$R_S = 0\Omega$		7	15		7	15		7	20		7			7			7		$\mu V/°C$
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			30			30			75			±100			±150		45	±200	nA_{DC}
Input Offset Current Drift			10	200		10	200		10	300		10			10			10		$pA_{DC}/°C$
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$		40	100		40	100		40	200		40	300		40	500		40	500	nA_{DC}
Input Common-Mode Voltage Range	$V^+ = 30\ V_{DC}$, (Note 7)	0		V^+-2	0		V^+-2	0		V^+-2	0		V^+-2	0		V^+-2	0		V^+-2	V_{DC}
Large Signal Voltage Gain	$V^+ = +15\ V_{DC}$ (For Large V_O Swing), $R_L \geq 2\ k\Omega$	25			25			15			25			15			15			V/mV
Output Voltage Swing																				
V_{OH}	$V^+ = +30\ V_{DC}$, $R_L = 2\ k\Omega$	26			26			26			26			26			22			V_{DC}
	$R_L \geq 10\ k\Omega$	27	28		27	28		27	28		27	28		27	28		23	24		V_{DC}
V_{OL}	$V^+ = 5\ V_{DC}$, $R_L \leq 10\ k\Omega$		5	20		5	20		5	20		5	20		5	20		5	100	mV_{DC}
Output Current																				
Source	$V_{IN}^+ = +1\ V_{DC}$, $V_{IN}^- = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$	10	20		10	20		10	20		10	20		10	20		10	20		mA_{DC}
Sink	$V_{IN}^- = +1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$	10	15		5	8		5	8		5	8		5	8		5	8		mA_{DC}
Differential Input Voltage	(Note 7)			32			32			32			32			32			26	V_{DC}

Note 1: For operating at high temperatures, the LM358/LM358A, LM2904 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM258/LM258A and LM158/LM158A can be derated based on a +150°C maximum junction temperature. The dissipation is the total of all four amplifiers—use external resistors, where possible, to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of $+15\ V_{DC}$, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3\ V_{DC}$ (at 25°C).

Note 4: These specifications apply for $V^+ = +5\ V_{DC}$ and $-55°C \leq T_A \leq +125°C$, unless otherwise stated. With the LM258/LM258A, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$, the LM358/LM358A temperature specifications are limited to $0°C \leq T_A \leq +70°C$, and the LM2904 specifications are limited to $-40°C \leq T_A \leq +85°C$.

Note 5: $V_O \cong 1.4\ V_{DC}$, $R_S = 0\Omega$ with V^+ from $5\ V_{DC}$ to $30\ V_{DC}$; and over the full input common-mode range ($0\ V_{DC}$ to $V^+ - 1.5\ V_{DC}$).

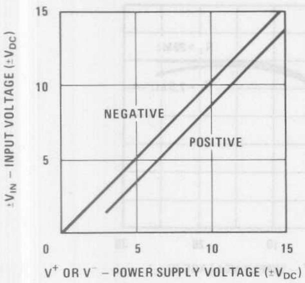
Note 6: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

Note 7: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is $V^+ -1.5V$, but either or both inputs can go to $+32\ V_{DC}$ without damage ($+26\ V_{DC}$ for LM2904).

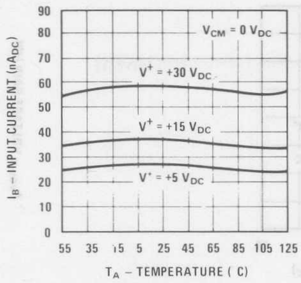
Note 8: Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitive increases at higher frequencies.

Typical Performance Characteristics

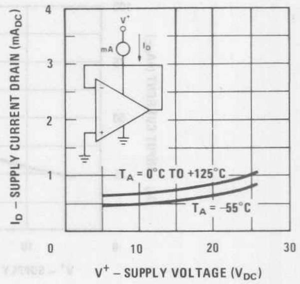
Input Voltage Range



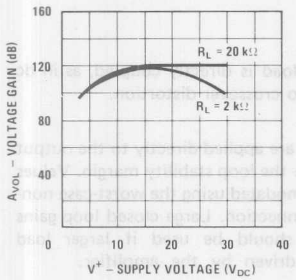
Input Current



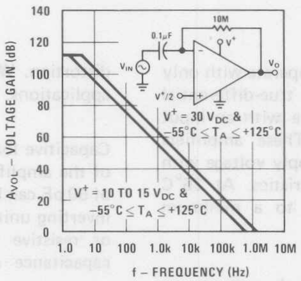
Supply Current



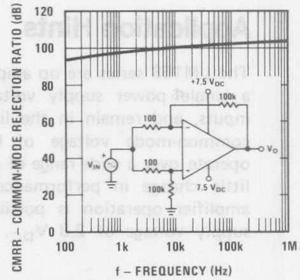
Voltage Gain



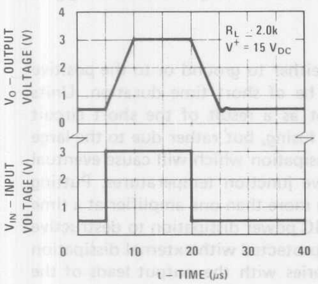
Open Loop Frequency Response



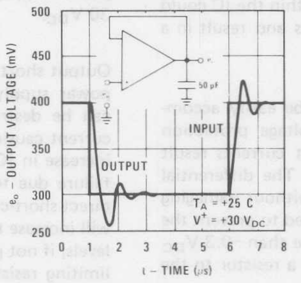
Common Mode Rejection Ratio



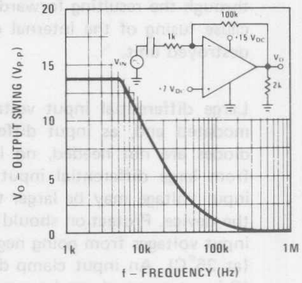
Voltage Follower Pulse Response



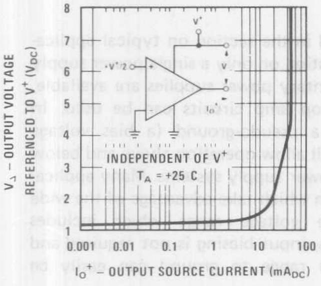
Voltage Follower Pulse Response (Small Signal)



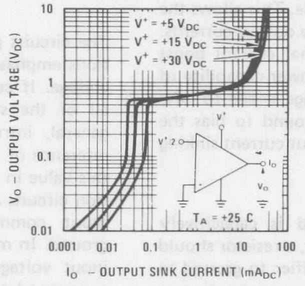
Large Signal Frequency Response



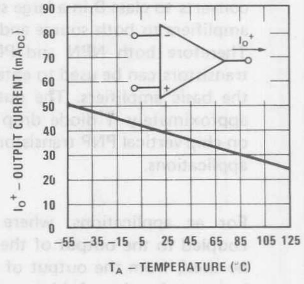
Output Characteristics Current Sourcing



Output Characteristics Current Sinking

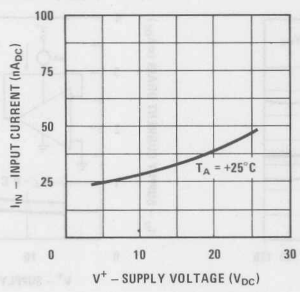


Current Limiting

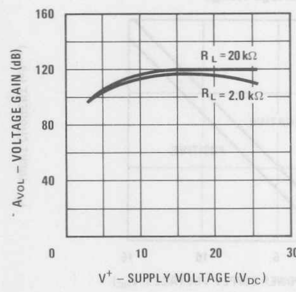


Typical Performance Characteristics (Continued) (LM2902 only)

Input Current



Voltage Gain



Application Hints

The LM158 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 V_{DC}.

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply current drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion. Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accommodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

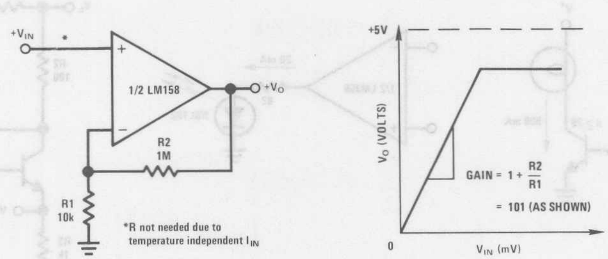
The bias network of the LM158 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 3 V_{DC} to 30 V_{DC}.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

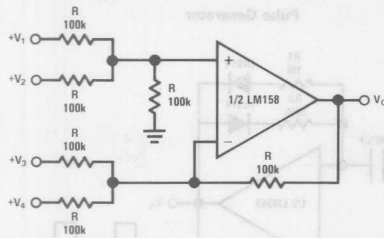
The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$)

Non-Inverting DC Gain (0V Input = 0V Output)

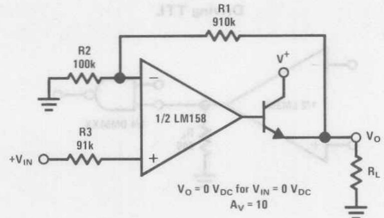


DC Summing Amplifier
(V_{IN}'S $\geq 0\ V_{DC}$ AND $V_O \geq 0\ V_{DC}$)

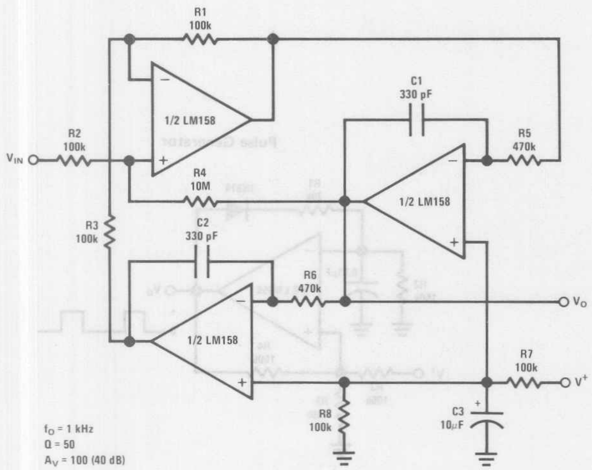


Where: $V_O = V_1 + V_2 - V_3 - V_4$
$(V_1 + V_2) \geq (V_3 + V_4)$ to keep $V_O > 0\ V_{DC}$

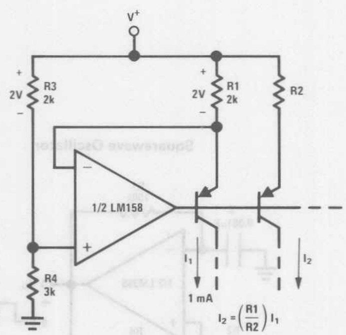
Power Amplifier



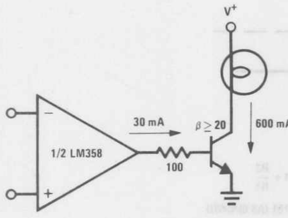
"BI-QUAD" RC Active Bandpass Filter



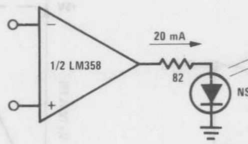
Fixed Current Sources

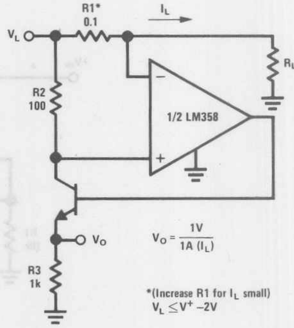


Lamp Driver



LED Driver

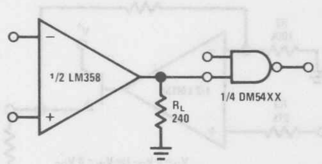




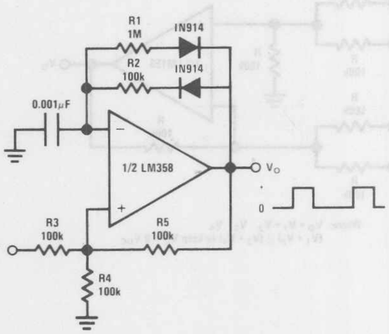
$V_O = \frac{1V}{1A\ (I_L)}$

*(Increase R1 for I_L small)
$V_L \leq V^+ - 2V$

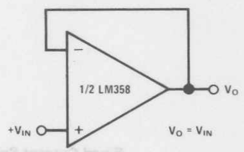
Driving TTL



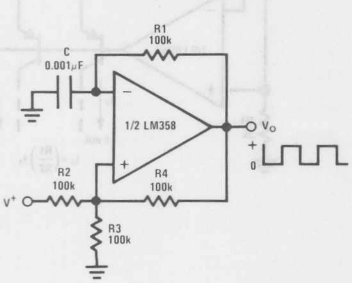
Pulse Generator



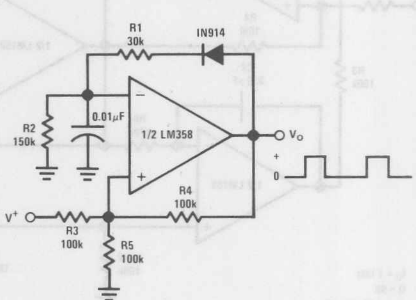
Voltage Follower

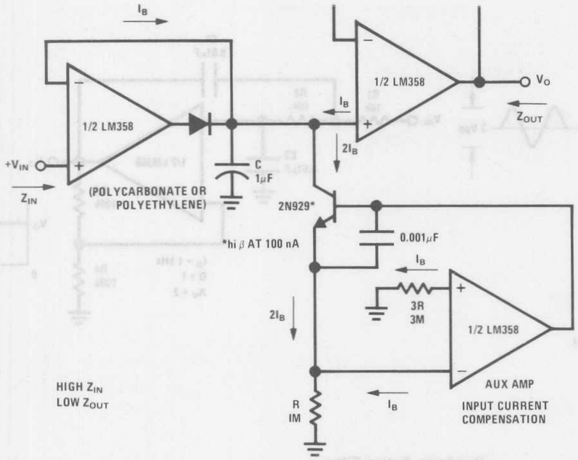


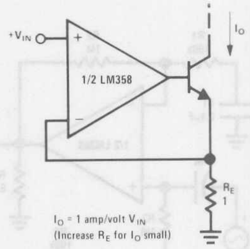
Squarewave Oscillator



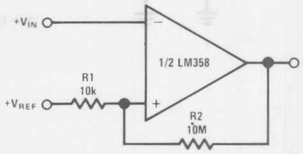
Pulse Generator



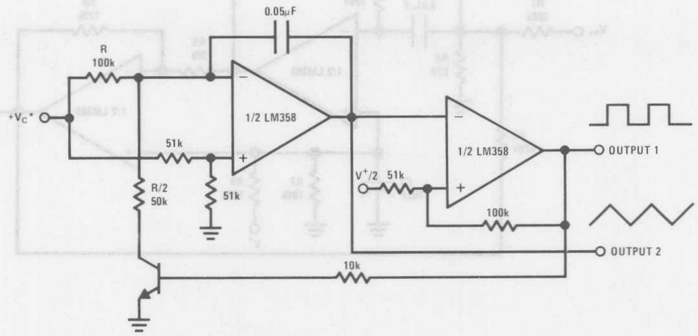




Comparator with Hysteresis

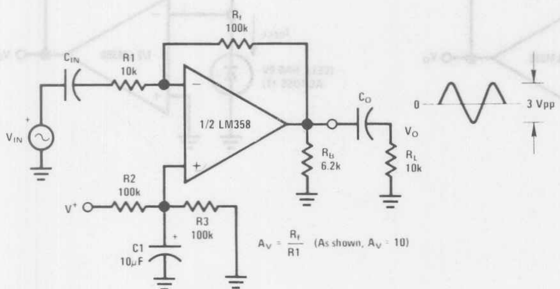


Voltage Controlled Oscillator (VCO)



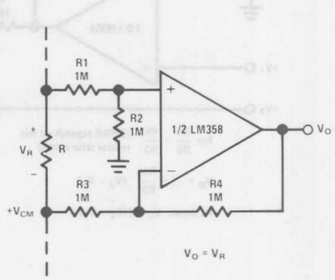
*WIDE CONTROL VOLTAGE RANGE: $0\ V_{DC} \leq V_C \leq 2\,(V^+ - 1.5\ V_{DC})$

AC Coupled Inverting Amplifier



$A_V = \frac{R_f}{R1}$ (As shown, $A_V = 10$)

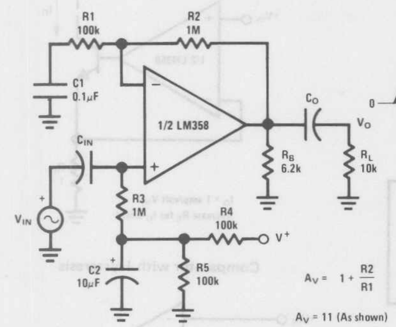
Ground Referencing A Differential Input Signal



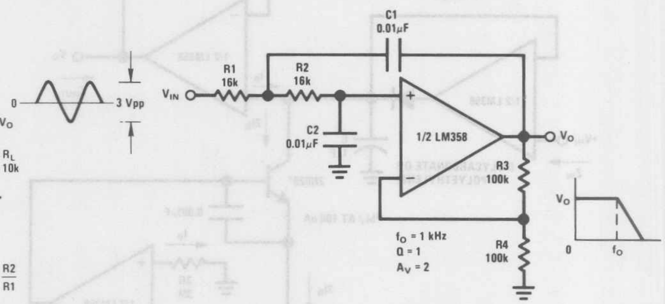
$V_O = V_R$

Typical Single-Supply Applications (Continued) ($V^+ = 5.0\ V_{DC}$)

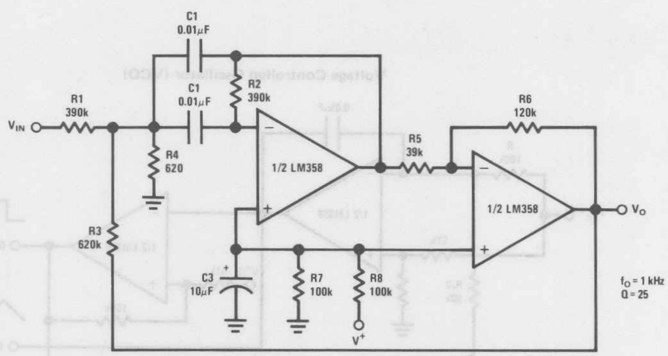
AC Coupled Non-Inverting Amplifier



DC Coupled Low-Pass RC Active Filter



Bandpass Active Filter



High Input Z, DC Differential Amplifier

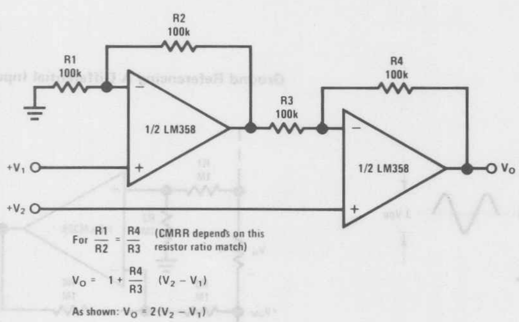
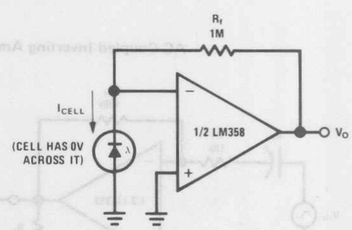
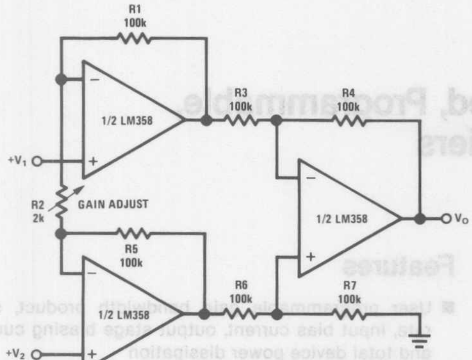


Photo Voltaic-Cell Amplifier



Typical Single-Supply Applications (Continued) ($V^+ = 5.0\ V_{DC}$)

High Input Z Adjustable-Gain DC Instrumentation Amplifier

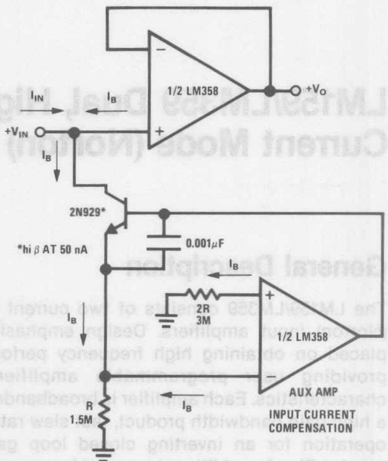


If R1 = R5 & R3 = R4 = R6 = R7 (CMRR depends on match)

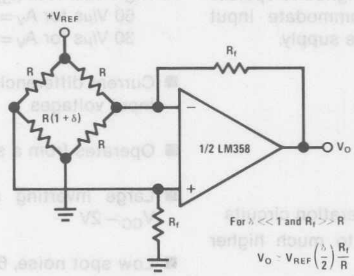
$$V_O = 1 + \frac{2R1}{R2}(V_2 - V_1)$$

As shown $V_O = 101\ (V_2 - V_1)$

Using Symmetrical Amplifiers to Reduce Input Current (General Concept)



Bridge Current Amplifier



For $\delta << 1$ and $R_f >> R$

$$V_O \cong V_{REF}\left(\frac{\delta}{2}\right)\frac{R_f}{R}$$

LM159/LM359 Dual, High Speed, Programmable, Current Mode (Norton) Amplifiers

General Description

The LM159/LM359 consists of two current differencing (Norton) input amplifiers. Design emphasis has been placed on obtaining high frequency performance and providing user programmable amplifier operating characteristics. Each amplifier is broadbanded to provide a high gain bandwidth product, fast slew rate and stable operation for an inverting closed loop gain of 10 or greater. Pins for additional external frequency compensation are provided. The amplifiers are designed to operate from a single supply and can accommodate input common-mode voltages greater than the supply.

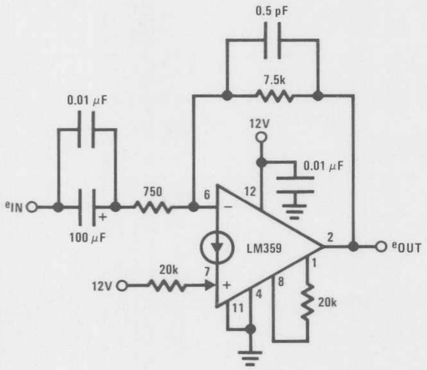
Applications

- General purpose video amplifiers
- High frequency, high Q active filters
- Photo-diode amplifiers
- Wide frequency range waveform generation circuits
- All LM3900 AC applications work to much higher frequencies

Features

- User programmable gain bandwidth product, slew rate, input bias current, output stage biasing current and total device power dissipation
- High gain bandwidth product ($I_{SET} = 0.5$ mA)
  - 400 MHz for $A_V = 10$ to 100
  - 30 MHz for $A_V = 1$
- High slew rate ($I_{SET} = 0.5$ mA)
  - 60 V/µs for $A_V = 10$ to 100
  - 30 V/µs for $A_V = 1$
- Current differencing inputs allow high common-mode input voltages
- Operates from a single 5V to 22V supply
- Large inverting amplifier output swing, 2 mV to $V_{CC} - 2V$
- Low spot noise, 6 nV/$\sqrt{Hz}$, for f>1 kHz

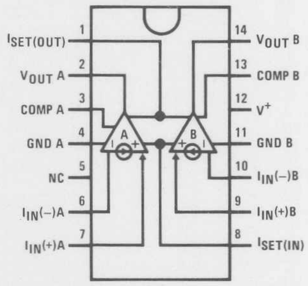
Typical Application



- $A_V = 20$ dB
- −3 dB bandwidth = 2.5 Hz to 25 MHz
- Differential phase error<1° at 3.58 MHz
- Differential gain error <0.5% at 3.58 MHz

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number LM159J or LM359J
See NS Package J14A
Order Number LM359N
See NS Package N14A

	±11 V_{DC}
Power Dissipation (Note 1)	
J Package	1W
N Package	750 mW
Maximum T_j	
J Package	150°C
N Package	125°C
θ_{jA}	
J Package	100°C/W
N Package	160°C/W

Set Currents, $I_{SET(IN)}$ or $I_{SET(OUT)}$	2 mA_{DC}
Operating Temperature Range	
LM159	−55°C to +125°C
LM359	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

$I_{SET(IN)} = I_{SET(OUT)} = 0.5$ mA, $V_{supply} = 12V$, $T_A = 25°C$ unless otherwise noted.

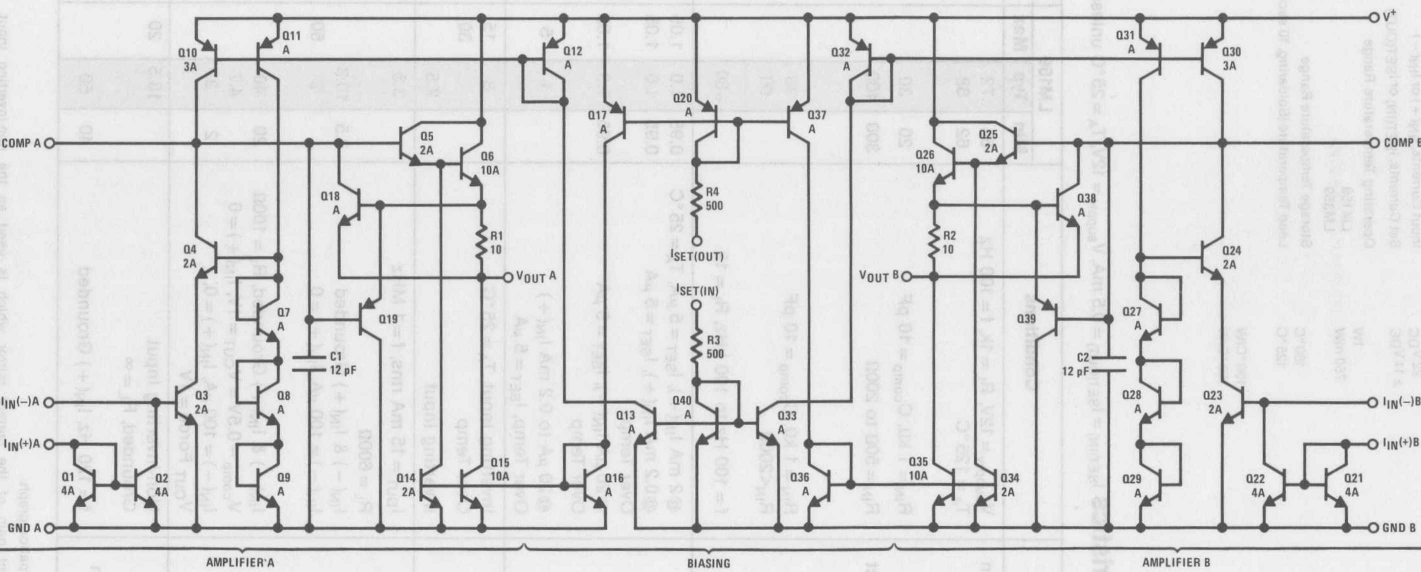
Parameter	Conditions	LM159			LM359			Units
		Min	Typ	Max	Min	Typ	Max	
Open Loop Voltage Gain	$V_{supply} = 12V$, $R_L = 1k$, $f = 100$ Hz	66	72		62	72		dB
	$T_A = 125°C$	62	68			68		dB
Bandwidth								
Unity Gain	$R_{IN} = 1$ kΩ, $C_{comp} = 10$ pF	20	30		15	30		MHz
Gain Bandwidth Product Gain of 10 to 100	$R_{IN} = 50Ω$ to $200Ω$	300	400		200	400		MHz
Slew Rate								
Unity Gain	$R_{IN} = 1$ kΩ, $C_{comp} = 10$ pF		30			30		V/μs
Gain of 10 to 100	$R_{IN} < 200Ω$		60			60		V/μs
Amplifier to Amplifier Coupling	$f = 100$ Hz to 100 kHz, $R_L = 1k$		−80			−80		dB
Mirror Gain (Note 2)	@2 mA $I_{IN}(+)$, $I_{SET} = 5$ μA, $T_A = 25°C$	0.95	1.0	1.05	0.9	1.0	1.1	μA/μA
	@0.2 mA $I_{IN}(+)$, $I_{SET} = 5$ μA Over Temp	0.95	1.0	1.05	0.9	1.0	1.1	μA/μA
	@20 μA $I_{IN}(+)$, $I_{SET} = 5$ μA Over Temp	0.95	1.0	1.05	0.9	1.0	1.1	μA/μA
ΔMirror Gain (Note 2)	@20 μA to 0.2 mA $I_{IN}(+)$ Over Temp, $I_{SET} = 5$ μA		1	5		3	5	%
Input Bias Current	Inverting Input, $T_A = 25°C$		8	15		8	15	μA
	Over Temp			30			30	μA
Input Resistance (βre)	Inverting Input		2.5			2.5		kΩ
Output Resistance	$I_{OUT} = 15$ mA rms, $f = 1$ MHz		3.5			3.5		Ω
Output Voltage Swing	$R_L = 600Ω$							
V_{OUT} High	$I_{IN}(-)$ & $I_{IN}(+)$ Grounded	9.5	10.3		9.5	10.3		V
V_{OUT} Low	$I_{IN}(-) = 100$ μA, $I_{IN}(+) = 0$		2	50		2	50	mV
Output Currents								
Source	$I_{IN}(-)$ & $I_{IN}(+)$ Grounded, $R_L = 100Ω$	20	40		16	40		mA
Sink (Linear Region)	$V_{comp} - 0.5V = V_{OUT} = 1V$, $I_{IN}(+) = 0$		4.7			4.7		mA
Sink (Overdriven)	$I_{IN}(-) = 100$ μA, $I_{IN}(+) = 0$, V_{OUT} Force = 1V	2	3		1.5	3		mA
Supply Current	Non-Inverting Input Grounded, $R_L = \infty$		18.5	20		18.5	22	mA
Power Supply Rejection (Note 3)	$f = 120$ Hz, $I_{IN}(+)$ Grounded	40	50		40	50		dB

Note 1: See Maximum Power Dissipation graph.

Note 2: Mirror gain is the current gain of the current mirror which is used as the non-inverting input. $\left(A_I = \frac{I_{IN}(-)}{I_{IN}(+)}\right)$ ΔMirror Gain is the % change in A_I for two different mirror currents at any given temperature.

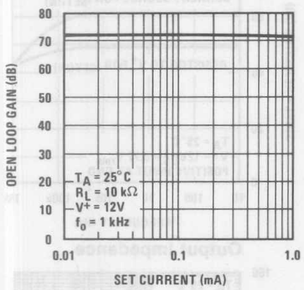
Note 3: See Supply Rejection graphs.

Schematic Diagram

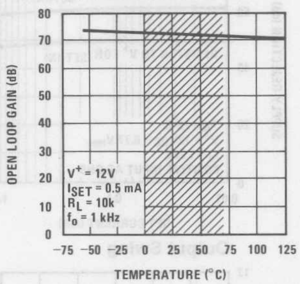


Typical Performance Characteristics

Open Loop Gain

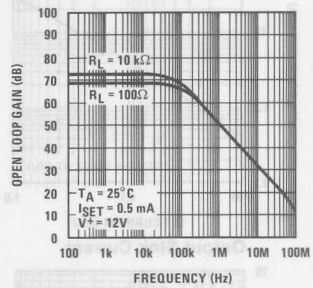


Open Loop Gain

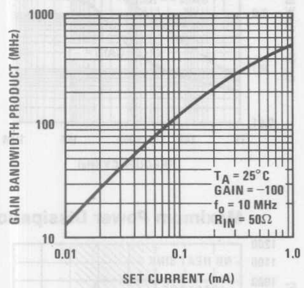


Note: Shaded area refers to LM359J/LM359N

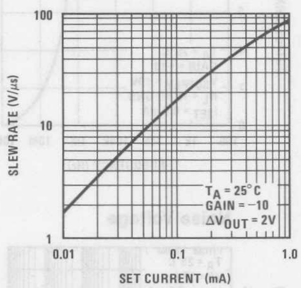
Open Loop Gain



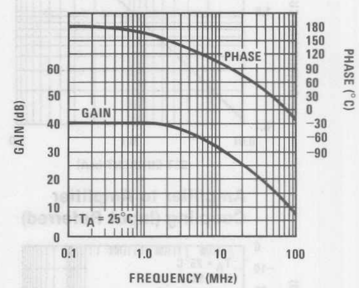
Gain Bandwidth Product



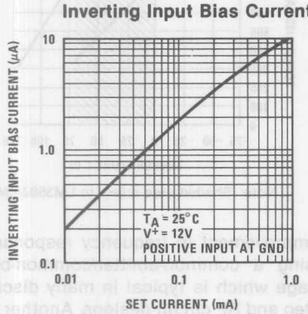
Slew Rate



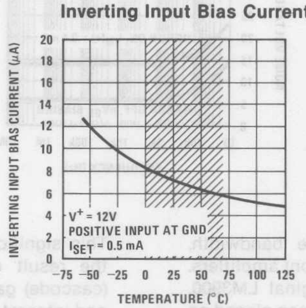
Gain and Phase Feedback Gain = −100



Inverting Input Bias Current

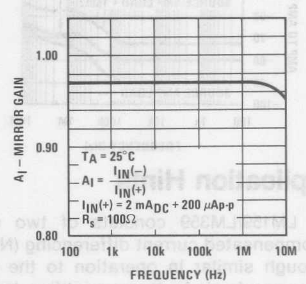


Inverting Input Bias Current

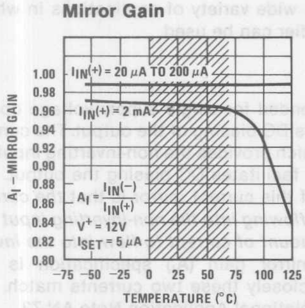


Note: Shaded area refers to LM359J/LM359N

Mirror Gain

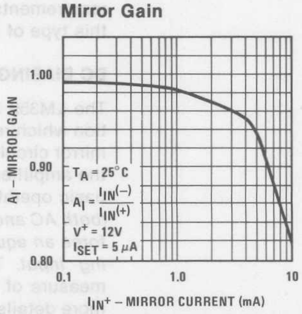


Mirror Gain

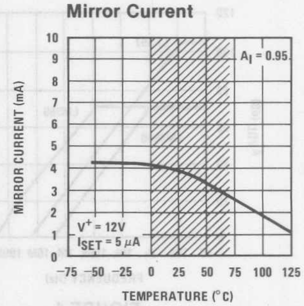


Note: Shaded area refers to LM359J/LM359N

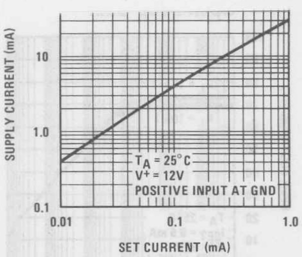
Mirror Gain

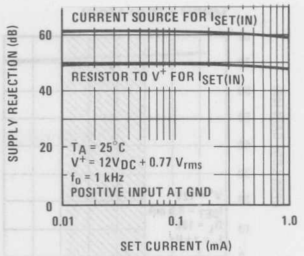


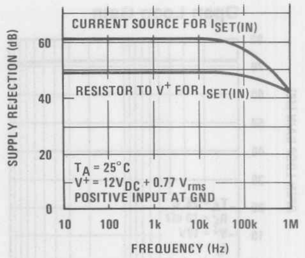
Mirror Current



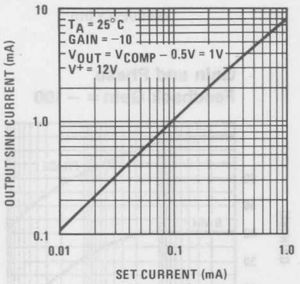
Note: Shaded area refers to LM359J/LM359N



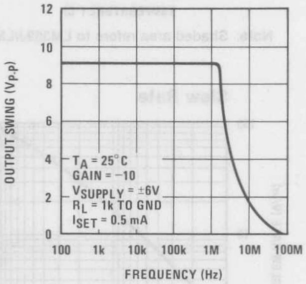




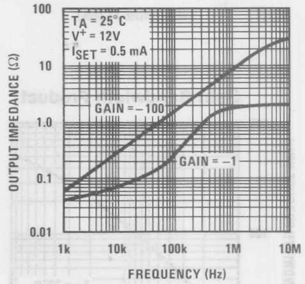
Output Sink Current



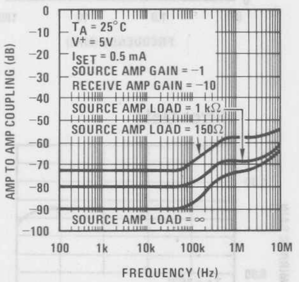
Output Swing



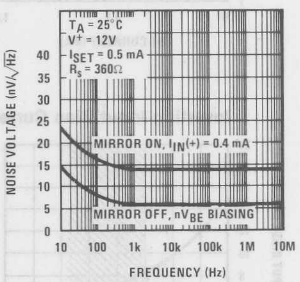
Output Impedance



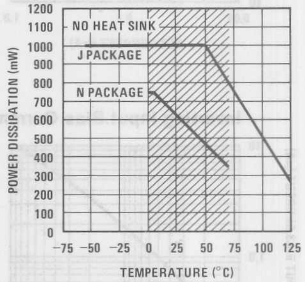
Amplifier to Amplifier Coupling (Input Referred)



Noise Voltage



Maximum Power Dissipation



Note: Shaded area refers to LM359J/LM359N

Application Hints

The LM159/LM359 consists of two wide bandwidth, decompensated current differencing (Norton) amplifiers. Although similar in operation to the original LM3900, design emphasis for these amplifiers has been placed on obtaining much higher frequency performance as illustrated in *Figure 1*.

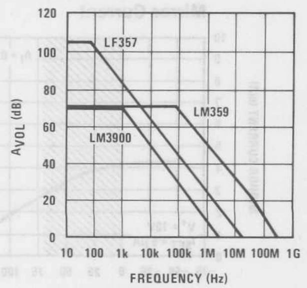


FIGURE 1

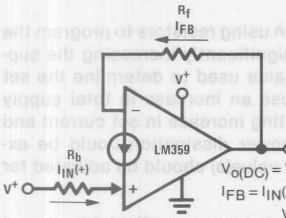
This significant improvement in frequency response is the result of using a common-emitter/common-base (cascode) gain stage which is typical in many discrete and integrated video and RF circuit designs. Another versatile aspect of these amplifiers is the ability to externally program many internal amplifier parameters to suit the requirements of a wide variety of applications in which this type of amplifier can be used.

DC BIASING

The LM359 is intended for single supply voltage operation which requires DC biasing of the output. The current mirror circuitry which provides the non-inverting input for the amplifier also facilitates DC biasing the output. The basic operation of this current mirror is that *the current (both AC and DC) flowing into the non-inverting input will force an equal amount of current to flow into the inverting input.* The mirror gain (A_I) specification is the measure of how closely these two currents match. For more details see National Application Note AN-72.

Application Hints (Continued)

DC biasing of the output is accomplished by establishing a reference DC current into the (+) input, $I_{IN}(+)$, and requiring the output to provide the (−) input current. This forces the output DC level to be whatever value necessary (within the output voltage swing of the amplifier) to provide this DC reference current, *Figure 2.*



$$V_{O(DC)} = V_{BE}(-) + I_{FB}\,R_f$$

$$I_{FB} = I_{IN}(+) \cdot A_I + I_b(-)$$

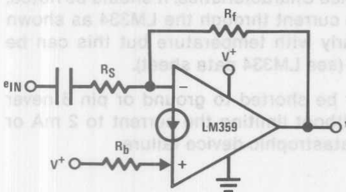
$$I_{IN}(+) = \frac{V^+ - V_{BE}(+)}{R_b}$$

$I_b(-)$ is the inverting input bias current

FIGURE 2

The DC input voltage at each input is a transistor V_{BE} ($\cong 0.6\ V_{DC}$) and must be considered for DC biasing. For most applications, the supply voltage, V^+, is suitable and convenient for establishing $I_{IN}(+)$. The inverting input bias current, $I_b(-)$, is a direct function of the programmable input stage current (see current programmability section) and to obtain predictable output DC biasing set $I_{IN}(+) \geq 10 I_b(-)$.

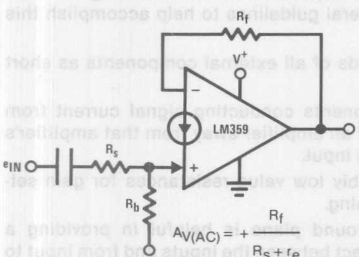
The following figures illustrate typical biasing schemes for AC amplifiers using the LM359:



$$A_{V(AC)} = -\frac{R_f}{R_S}$$

$$V_{O(DC)} = V_{BE}(-) + R_f\left[\frac{V^+ - V_{BE}(+)}{R_b} + I_b(-)\right]$$

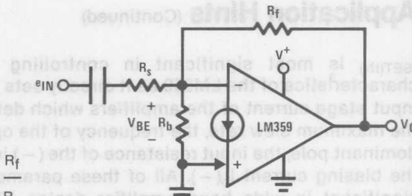
FIGURE 3. Biasing an Inverting AC Amplifier



$$A_{V(AC)} = +\frac{R_f}{R_S + r_e}$$

$$V_{O(DC)} = V_{BE}(-) + R_f\left[\frac{V^+ - V_{BE}(+)}{R_b} + I_b(-)\right]$$

FIGURE 4. Biasing a Non-Inverting AC Amplifier



$$A_{V(AC)} = -\frac{R_f}{R_S}$$

$$V_{O(DC)} = V_{BE}(-)\left(1 + \frac{R_f}{R_b}\right) + I_b(-)R_f$$

FIGURE 5. nV_{BE} Biasing

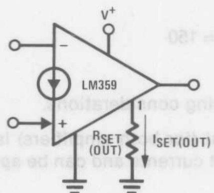
The nV_{BE} biasing configuration is most useful for low noise applications where a reduced input impedance can be accommodated (see typical applications section).

OPERATING CURRENT PROGRAMMABILITY (I_{SET})

The input bias current, slew rate, gain bandwidth product, output drive capability and total device power consumption of both amplifiers can be simultaneously controlled and optimized via the two programming pins $I_{SET(OUT)}$ and $I_{SET(IN)}$.

$I_{SET(OUT)}$

The output set current ($I_{SET(OUT)}$) is equal to the amount of current sourced from pin 1 and establishes the class A biasing current for the Darlington emitter follower output stage. Using a single resistor from pin 1 to ground, as shown in *Figure 6,* this current is equal to:



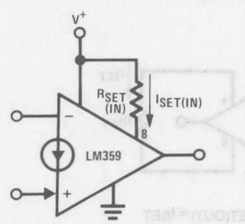
$$I_{SET(OUT)} = \frac{V^+ - V_{BE}}{R_{SET(OUT)} + 500\Omega}$$

FIGURE 6. Establishing the Output Set Current

The output set current can be adjusted to optimize the amount of current the output of the amplifier can sink to drive load capacitance and for loads connected to V^+. *The maximum output sinking current is approximately 10 times $I_{SET(OUT)}$.* This set current is best used to reduce the total device supply current if the amplifiers are not required to drive small load impedances.

$I_{SET(IN)}$

The input set current $I_{SET(IN)}$ is equal to the current flowing into pin 8. A resistor from pin 8 to V^+ sets this current to be:



$$I_{SET(IN)} = \frac{V^+ - V_{BE}}{R_{SET(IN)} + 500\Omega}$$

FIGURE 7. Establishing the Input Set Current

Application Hints (Continued)

$I_{SET(IN)}$ is most significant in controlling the AC characteristics of the LM359 as it directly sets the total input stage current of the amplifiers which determines the maximum slew rate, the frequency of the open loop dominant pole, the input resistance of the (−) input and the biasing current $I_b(-)$. All of these parameters are significant in wide band amplifier design. The input stage current is approximately 3 times $I_{SET(IN)}$ and by using this relationship the following first order approximations for these AC parameters are:

$$S_{r(MAX)} = \text{max slew rate} \cong \frac{3I_{SET(IN)}(10^{-6})}{C_{comp}} \ (\text{V}/\mu\text{s})$$

$$\text{frequency of dominant pole} \cong \frac{3I_{SET(IN)}}{2\pi\, C_{comp}\, A_{VOL}\, (0.026\ \text{V})} \ (\text{Hz})$$

$$\text{input resistance} = \beta r_e \cong \frac{150\ (0.026\ \text{V})}{3I_{SET(IN)}} \ (\Omega)$$

where C_{comp} is the total capacitance from the compensation pin (pin 3 or pin 13) to ground, A_{VOL} is the low frequency open loop voltage gain in V/V and an ambient temperature of 25°C is assumed ($KT/q = 26$ mV and $\beta_{typ} = 150$). $I_{SET(IN)}$ also controls the DC input bias current by the expression:

$$I_b(-) = \frac{3I_{SET}}{\beta} \cong \frac{I_{SET}}{50} \quad \text{for NPN } \beta = 150$$

which is important for DC biasing considerations.

The total device supply current (for both amplifiers) is also a direct function of the set currents and can be approximated by:

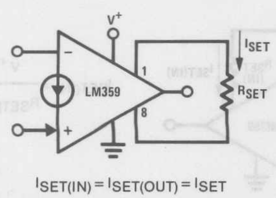
$$I_{supply} \cong 27 \times I_{SET(OUT)} + 11 \times I_{SET(IN)}$$

with each set current programmed by individual resistors.

PROGRAMMING WITH A SINGLE RESISTOR

Operating current programming may also be accomplished using only one resistor by letting $I_{SET(IN)}$ equal $I_{SET(OUT)}$. The programming current is now referred to as I_{SET} and it is created by connecting a resistor from pin 1 to pin 8 *(Figure 8)*.

$$I_{SET} = \frac{V^+ - 2V_{BE}}{R_{SET} + 1\ \text{k}\Omega} \quad \text{where } V_{BE} \cong 0.6\text{V}$$



$I_{SET(IN)} = I_{SET(OUT)} = I_{SET}$

FIGURE 8. Single Resistor Programming of I_{SET}

This configuration does not affect any of the internal set current dependent parameters differently than previously discussed except the total supply current which is now equal to:

$$I_{supply} \cong 37 \times I_{SET}$$

Care must be taken when using resistors to program the set current to prevent significantly increasing the supply voltage above the value used to determine the set current. This would cause an increase in total supply current due to the resulting increase in set current and the maximum device power dissipation could be exceeded. The set resistor value(s) should be adjusted for the new supply voltage.

One method to avoid this is to use an adjustable current source which has voltage compliance to generate the set current as shown in *Figure 9*.

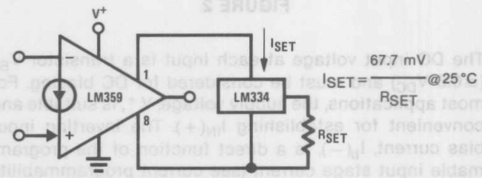


FIGURE 9. Current Source Programming of I_{SET}

This circuit allows I_{SET} to remain constant over the entire supply voltage range of the LM359 which also improves power supply ripple rejection as illustrated in the Typical Performance Characteristics. It should be noted, however, that the current through the LM334 as shown will change linearly with temperature but this can be compensated for (see LM334 data sheet).

Pin 1 must never be shorted to ground or pin 8 never shorted to V^+ without limiting the current to 2 mA or less to prevent catastrophic device failure.

CONSIDERATIONS FOR HIGH FREQUENCY OPERATION

The LM359 is intended for use in relatively high frequency applications and many factors external to the amplifier itself must be considered. Minimization of stray capacitances and their effect on circuit operation are the primary requirements. The following list contains some general guidelines to help accomplish this end:

1. Keep the leads of all external components as short as possible.
2. Place components conducting signal current from the output of an amplifier away from that amplifier's non-inverting input.
3. Use reasonably low value resistances for gain setting and biasing.
4. Use of a ground plane is helpful in providing a shielding effect between the inputs and from input to output. Avoid using vector boards.
5. Use a single-point ground and single-point supply distribution to minimize crosstalk. Always connect the two grounds (one from each amplifier) together.

7. Bypass the supply close to the device with a low inductance, low value capacitor (typically a .01 μF ceramic) to create a good high frequency ground. If long supply leads are unavoidable, a small resistor (~10Ω) in series with the bypass capacitor may be needed and using shielded wire for the supply leads is also recommended.

COMPENSATION

The LM359 is internally compensated for stability with closed loop inverting gains of 10 or more. For an inverting gain of less than 10 and all non-inverting amplifiers (the amplifier always has 100% negative current feedback regardless of the gain in the non-inverting configuration) some external frequency compensation is required because the stray capacitance to ground from the (−) input and the feedback resistor add additional lagging phase within the feedback loop. The value of the input capacitance will typically be in the range of 6 pF to 10 pF for a reasonably constructed circuit board. When using a feedback resistance of 30 kΩ or less, the best method of compensation, without sacrificing slew rate, is to add a lead capacitor in parallel with the feedback resistor with a value on the order of 1 pF to 5 pF as shown in *Figure 10*.

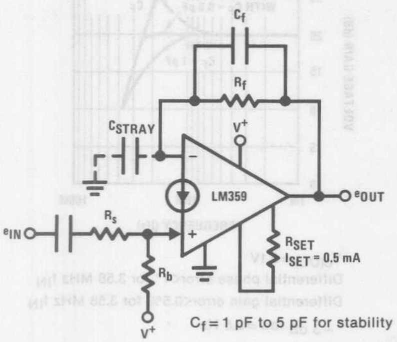


FIGURE 10. Best Method of Compensation

Another method of compensation is to increase the effective value of the internal compensation capacitor by adding capacitance from the COMP pin of an amplifier to ground. An external 20 pF capacitor will generally compensate for all gain settings but will also reduce the gain bandwidth product and the slew rate. These same results can also be obtained by reducing $I_{SET(IN)}$ if the full capabilities of the amplifier are not required. This method is termed over-compensation.

Another area of concern from a stability standpoint is that of capacitive loading. The amplifier will generally drive capacitive loads up to 100 pF without oscillation problems. Any larger C loads can be isolated from the output as shown in *Figure 11*. Over-compensation of the amplifier can also be used if the corresponding reduction of the GBW product can be afforded.

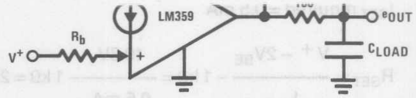


FIGURE 11. Isolating Large Capacitive Loads

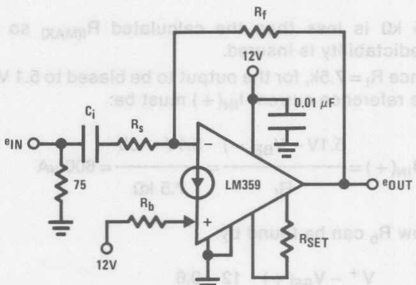
In most applications using the LM359, the input signal will be AC coupled so as not to affect the DC biasing of the amplifier. This gives rise to another subtlety of high frequency circuits which is the effective series inductance (ESL) of the coupling capacitor which creates an increase in the impedance of the capacitor at high frequencies and can cause an unexpected gain reduction. Low ESL capacitors like solid tantalum for large values of C and ceramic for smaller values are recommended. A parallel combination of the two types is even better for gain accuracy over a wide frequency range.

AMPLIFIER DESIGN EXAMPLES

The ability of the LM359 to provide gain at frequencies higher than most monolithic amplifiers can provide makes it most useful as a basic broadband amplification stage. The design of standard inverting and non-inverting amplifiers, though different than standard op amp design due to the current differencing inputs, also entail subtle design differences between the two types of amplifiers. These differences will be best illustrated by design examples. For these examples a practical video amplifier with a passband of 8 Hz to 10 MHz and a gain of 20 dB will be used. It will be assumed that the input will come from a 75Ω source and proper signal termination will be considered. The supply voltage is 12 V_{DC} and single resistor programming of the operating current, I_{SET}, will be used for simplicity.

AN INVERTING VIDEO AMPLIFIER

1. Basic circuit configuration:



2. Determine the required I_{SET} from the characteristic curves for gain bandwidth product.

$$GBW_{MIN} = 10 \times 10\ \text{MHz} = 100\ \text{MHz}$$

For a flat response to 10 MHz a closed loop response to two octaves above 10 MHz (40 MHz) will be sufficient.

I_{SET} required = 0.5 mA

$$R_{SET} = \frac{V^+ - 2V_{BE}}{I_{SET}} - 1\ k\Omega = \frac{10.8V}{0.5\ mA} - 1\ k\Omega = 20.6\ k\Omega$$

3. Determine maximum value for R_f to provide stable DC biasing

$$I_{f(MIN)} \geq 10 \times \frac{3I_{SET}}{\beta} = \begin{array}{l}100\ \mu A \text{ minimum DC} \\ \text{feedback current}\end{array}$$

Optimum output DC level for maximum symmetrical swing without clipping is:

$$V_{oDC(opt)} = \frac{V_{o(MAX)} - V_{o(MIN)}}{2} + V_{o(MIN)}$$

$$\approx \frac{(V^+ - 3V_{BE}) - 2\ mV}{2}$$

$$V_{oDC(opt)} \cong \frac{12 - 1.8V}{2} = \frac{10.2V}{2} = 5.1\ V_{DC}$$

$R_{f(MAX)}$ can now be found:

$$R_{f(MAX)} = \frac{V_{oDC(opt)} - V_{BE}(-)}{I_{f(MIN)}} = \frac{5.1V - 0.6}{100\ \mu A} = 45\ k\Omega$$

This value should not be exceeded for predictable DC biasing.

4. Select R_s to be large enough so as not to appreciably load the input termination resistance:

$R_s \geq 750\Omega$ Let $R_s = 750\Omega$

5. Select R_f for appropriate gain:

$$A_V = -\frac{R_f}{R_s} \text{ so; } R_f = 10R_s = 7.5\ k\Omega$$

7.5 kΩ is less than the calculated $R_{f(MAX)}$ so DC predictability is insured.

6. Since $R_f = 7.5k$, for the output to be biased to 5.1 V_{DC}, the reference current $I_{IN}(+)$ must be:

$$I_{IN}(+) = \frac{5.1V - V_{BE}(-)}{R_f} = \frac{5.1V - .6V}{7.5\ k\Omega} = 600\ \mu A$$

Now R_b can be found by:

$$R_b = \frac{V^+ - V_{BE}(+)}{I_{IN}(+)} = \frac{12 - 0.6}{600\ \mu A} = 19\ k\Omega$$

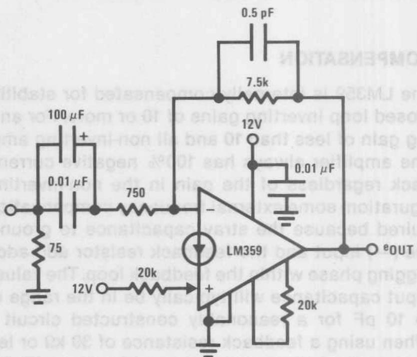
7. Select C_i to provide the proper gain for the 8 Hz minimum input frequency:

$$C_i \geq \frac{1}{2\pi\ R_s\ (f_{low})} = \frac{1}{2\pi\ (750\Omega)\ (8\ Hz)} = 26\ \mu F$$

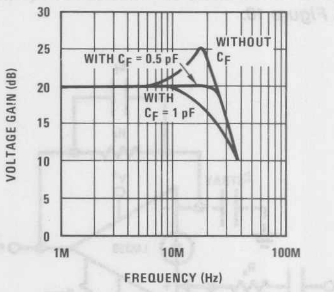
response down to 8 Hz and a 0.01 µF ceramic capacitor in parallel with C_i will maintain high frequency gain accuracy.

8. Test for peaking of the frequency response and add a feedback "lead" capacitor to compensate if necessary.

Final Circuit Using Standard 5% Tolerance Resistor Values:



Circuit Performance:



$V_{o(DC)} = 5.1V$

Differential phase error<1° for 3.58 MHz f_{IN}

Differential gain error<0.5% for 3.58 MHz f_{IN}

$f_{-3\ dB}$ low = 2.5 Hz

A NON-INVERTING VIDEO AMPLIFIER

For this case several design considerations must be dealt with.

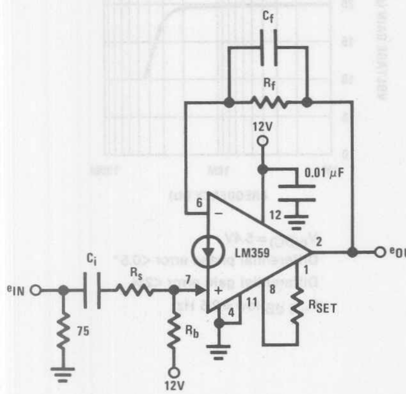
- The output voltage (AC and DC) is strictly a function of the size of the feedback resistor and the sum of AC and DC "mirror current" flowing into the (+) input.
- The amplifier always has 100% current feedback so external compensation is required. Add a small (1 pF–5 pF) feedback capacitance to leave the amplifier's open loop response and slew rate unaffected.
- To prevent saturating the mirror stage the total AC and DC current flowing into the amplifier's (+) input should be less than 2 mA.
- The output's maximum negative swing is one diode above ground due to the V_{BE} diode clamp at the (−) input.

Application Hints (Continued)

DESIGN EXAMPLE:

$e_{IN} = 50$ mV (MAX), $f_{IN} = 10$ MHz (MAX), desired circuit BW = 20 MHz, $A_V = 20$ dB, driving source impedance = 75Ω, $V^+ = 12V$.

1. Basic circuit configuration:



2. Select I_{SET} to provide adequate amplifier bandwidth so that the closed loop bandwidth will be determined by R_f and C_f. To do this, the set current should program an amplifier open loop gain of at least 20 dB at the desired closed loop bandwidth of the circuit. For this example, an I_{SET} of 0.5 mA will provide 26 dB of open loop gain at 20 MHz which will be sufficient. Using single resistor programming for I_{SET}:

$$R_{SET} = \frac{V^+ - 2V_{BE}}{I_{SET}} - 1\ k\Omega = 20.6\ k\Omega$$

3. Since the closed loop bandwidth will be determined by R_f and $C_f\left(f_{-3\ dB} = \frac{1}{2\pi R_f C_f}\right)$ to obtain a 20 MHz bandwidth, both R_f and C_f should be kept small. It can be assumed that C_f can be in the range of 1 pF to 5 pF for carefully constructed circuit boards to insure stability and allow a flat frequency response. This will limit the value of R_f to be within the range of:

$$\frac{1}{2\pi\ 5\ pF\ 20\ MHz} \leq R_f \leq \frac{1}{2\pi\ 1\ pF\ 20\ MHz}$$

or $1.6\ k\Omega \leq R_f \leq 7.96\ k\Omega$

Also, for a closed loop gain of +10, R_f must be 10 times $R_s + r_e$ where r_e is the mirror diode resistance.

4. So as not to appreciably load the 75Ω input termination resistance the value of $(R_s + r_e)$ is set to 750Ω.

5. For $A_v = 10$; R_f is set to 7.5 kΩ.

6. The optimum output DC level for symmetrical AC swing is:

$$V_{oDC(opt)} = \frac{V_{o(MAX)} - V_{o(MIN)}}{2} + V_{o(MIN)}$$

$$= \frac{(12 - 1.8)V - 0.6V}{2} + 0.6V = 5.4V_{DC}$$

7. The DC feedback current must be:

$$I_{FB} = \frac{V_{oDC(opt)} - V_{BE}(-)}{R_f} = \frac{5.4V - 0.6V}{7.5k}$$

$$= 640\ \mu A = I_{IN}(+)$$

DC biasing predictability will be insured because 640 μA is greater than the minimum of $I_{SET}/5$ or 100 μA.

For gain accuracy the total AC and DC mirror current should be less than 2 mA. For this example the maximum AC mirror current will be;

$$\frac{\pm e_{in\ peak}}{R_s + r_e} = \frac{\pm 50\ mV}{750\Omega} = \pm 66\ \mu A$$

therefore the total mirror current range will be 574 μA to 706 μA which will insure gain accuracy.

8. R_b can now be found:

$$R_b = \frac{V^+ - V_{BE}(+)}{I_{IN}(+)} = \frac{12 - 0.6}{640\ \mu A} = 17.8\ k\Omega$$

9. Since $R_s + r_e$ will be 750Ω and r_e is fixed by the DC mirror current to be:

$$r_e = \frac{KT}{q\ I_{IN(+)}} = \frac{26\ mV}{640\ \mu A} \cong 40\Omega \text{ at } 25°C$$

R_s must be 750Ω-40Ω or 710Ω which can be a 680Ω resistor in series with a 30Ω resistor which are standard 5% tolerance resistor values.

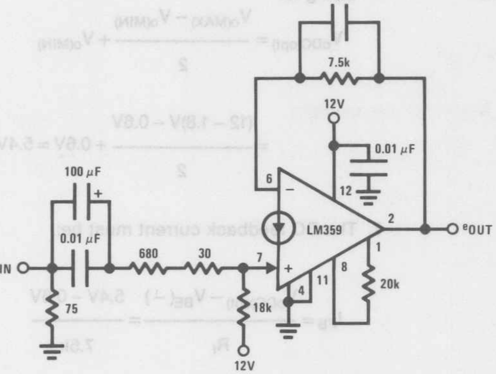
10. As a final design step, C_i must be selected to pass the lower passband frequency corner of 8 Hz for this example.

$$C_i = \frac{1}{2\pi\ (R_s + r_e)\ f_{low}} = \frac{1}{2\pi\ (750\Omega)\ (8\ Hz)} = 26.5\ \mu F$$

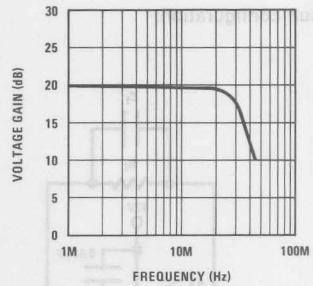
A larger value may be used and a 0.01 μF ceramic capacitor in parallel with C_i will maintain high frequency gain accuracy.

Application Hints (Continued)

Final Circuit Using Standard 5% Tolerance Resistor Values:



Circuit Performance:



$V_{O(DC)} = 5.4V$
Differential phase error <0.5°
Differential gain error <2%
$f_{-3\ dB}$ low = 2.5 Hz

GENERAL PRECAUTIONS

The LM359 is designed primarily for single supply operation but split supplies may be used if the negative supply voltage is well regulated as the amplifiers have no negative supply rejection.

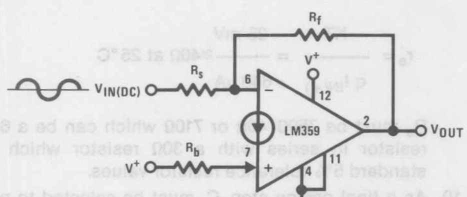
The total device power dissipation must always be kept in mind when selecting an operating supply voltage, the programming current, I_{SET}, and the load resistance, particularly when DC coupling the output to a succeeding stage. To prevent damaging the current mirror input diode, the mirror current should always be limited to 10 mA, or less, which is important if the input is susceptible to high voltage transients. The voltage at any of the inputs must not be forced more negative than −0.7V without limiting the current to 10 mA.

The supply voltage must never be reversed to the device; however, plugging the device into a socket backwards would then connect the positive supply voltage to the pin that has no internal connection (pin 5) which may prevent inadvertent device failure!

Typical Applications

DC Coupled Inputs

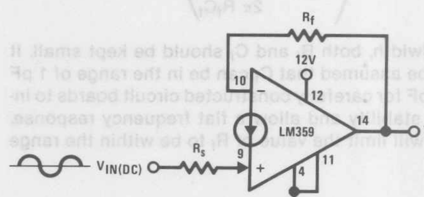
Inverting



$$V_{O(DC)} = \left[\frac{V+ - V_{BE(+)}}{R_b} - \frac{V_{IN(DC)} - V_{BE(-)}}{R_S}\right] R_f + V_{BE(-)}$$

$$A_{V(AC)} = -\frac{R_f}{R_S}$$

Non-Inverting



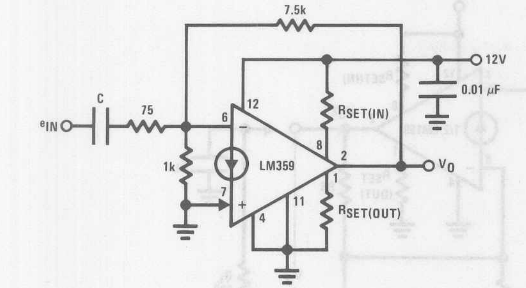
$$V_{O(DC)} = V_{BE(-)} + \frac{(V_{IN(DC)} - V_{BE(+)})R_f}{R_S}$$

$$A_{V(AC)} = +\frac{R_f}{R_S + r_e(+)}$$

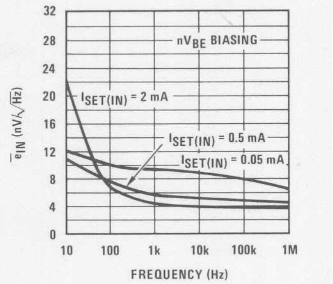
- Eliminates the need for an input coupling capacitor
- Input DC level must be stable and can exceed the supply voltage of the LM359 provided that maximum input currents are not exceeded.

Application Hints (Continued)

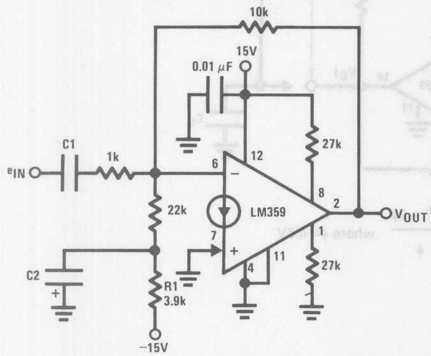
Noise Reduction using nV_{BE} Biasing



Typical Input Referred Noise Performance

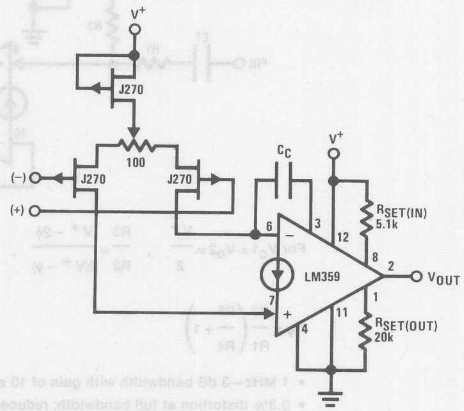


nV_{BE} Biasing with a Negative Supply



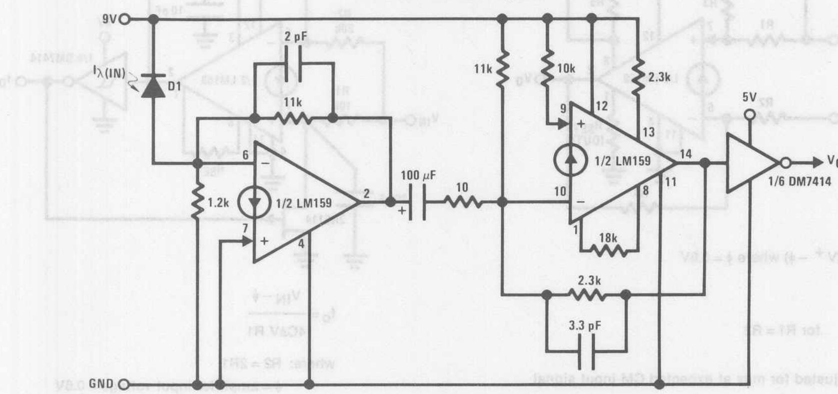
- R1 and C2 provide additional filtering of the negative biasing supply

Adding a JFET Input Stage



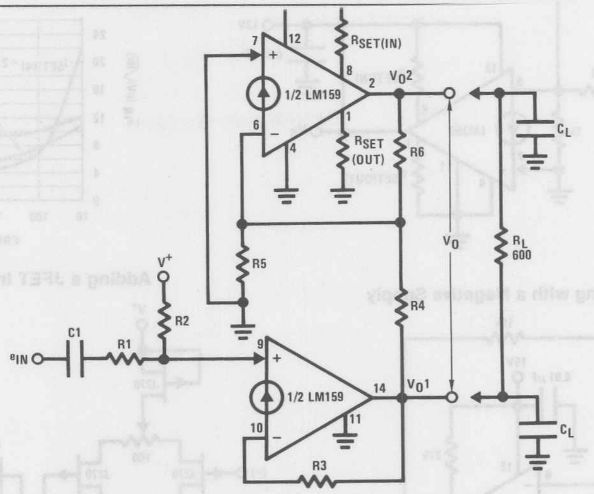
- FET input voltage mode op amp
- For $A_V = +1$; BW = 40 MHz, $S_r = 60$ V/μs; $C_C = 51$ pF
- For $A_V = +11$; BW = 24 MHz, $S_r = 130$ V/μs; $C_C = 5$ pF
- For $A_V = +100$; BW = 4.5 MHz, $S_r = 150$ V/μs; $C_C = 2$ pF
- V_{OS} is typically < 25 mV; 100Ω potentiometer allows a V_{OS} adjust range of ≈ ±200 mV
- Inputs must be DC biased for single supply operation

Photo Diode Amplifier



D1~RCA N-Type Silicon P-I-N Photodiode

- Frequency response of greater than 10 MHz
- If slow rise and fall times can be tolerated the gate on the output can be removed. In this case the rise and the fall time of the LM359 is 40 ns.
- $T_{PDL} = 45$ ns, $T_{PDH} = 50$ ns—T^2L output

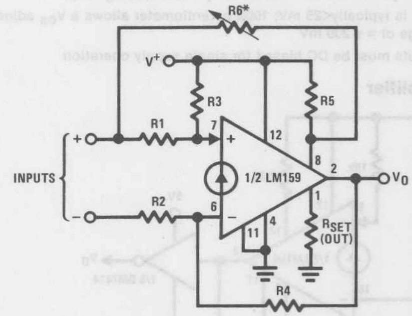


For $V_O1 = V_O2 = \frac{V^+}{2}$, $\frac{R3}{R2} = \frac{V^+ - 2\phi}{2(V^+ - \phi)}$, $\frac{R6}{R5} = \frac{V^+ - 2\phi}{\phi}$ where $\phi \approx 0.6V$

$$A_V = \frac{R3}{R1}\left(\frac{R6}{R4} + 1\right)$$

- 1 MHz—3 dB bandwidth with gain of 10 and 0 dbm into 600Ω
- 0.3% distortion at full bandwidth; reduced to 0.05% with bandwidth of 10 kHz
- Will drive $C_L = 1500$ pF with no additional compensation, ±0.01 μF with $C_{comp} = 180$ pF
- 70 dB signal to noise ratio at 0 dbm into 600Ω, 10 kHz bandwidth

Difference Amplifier



$V_{O(DC)} = \frac{R4}{R3}(V^+ - \phi)$ where $\phi = 0.6V$

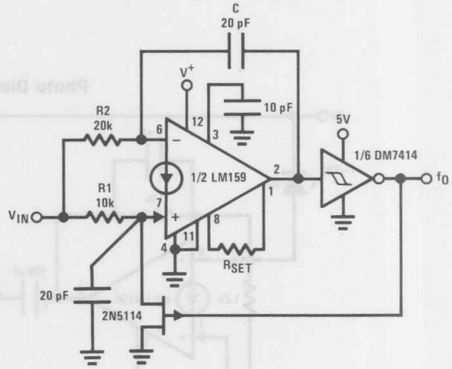
$A_V = \frac{R4}{R1}$ for R1 = R2

*CMRR is adjusted for max at expected CM input signal

$R6 \approx \frac{R5}{5}$, for R5 = 100 kΩ

- Wide bandwidth
- 70 dB CMRR typ
- Wide CM input voltage range

Voltage Controlled Oscillator



$f_O = \frac{V_{IN} - \phi}{4C\Delta V\ R1}$

where: R2 = 2R1

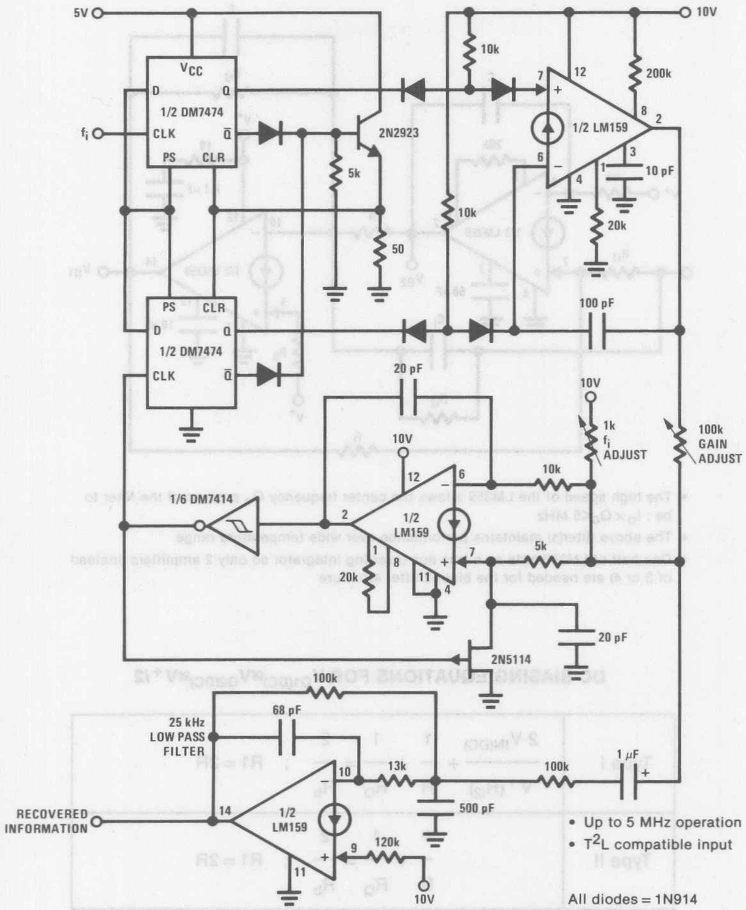
ϕ = amplifier input voltage = 0.6V

ΔV = DM7414 hysteresis, typ 1V

- 5 MHz operation
- T^2L ouput

Typical Applications (Continued)

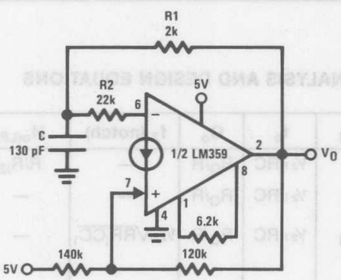
Phase Locked Loop



- Up to 5 MHz operation
- T^2L compatible input

All diodes = 1N914

Squarewave Generator



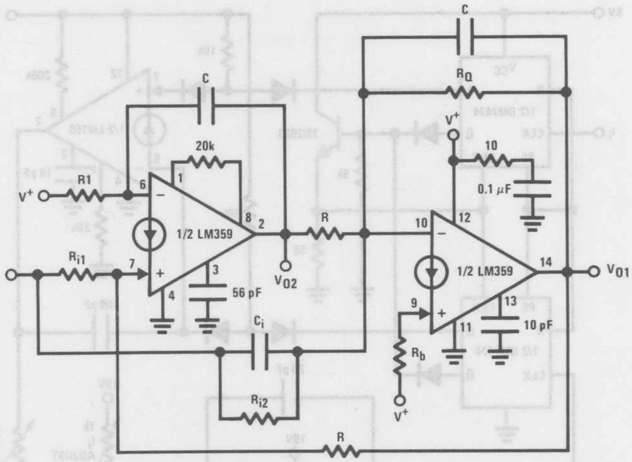
f = 1 MHz

Output is TTL compatible

Frequency is adjusted by R1 & C (R1<<R2)

Typical Applications

High Performance 2 Amplifier Biquad Filter(s)



- The high speed of the LM359 allows the center frequency Q_O product of the filter to be : $f_O \times Q_O \leq 5$ MHz
- The above filter(s) maintains performance over wide temperature range
- One half of LM359 acts as a true non-inverting integrator so only 2 amplifiers (instead of 3 or 4) are needed for the biquad filter structure

DC BIASING EQUATIONS FOR $V_{O1(DC)} \cong V_{O2(DC)} \cong V^+/2$

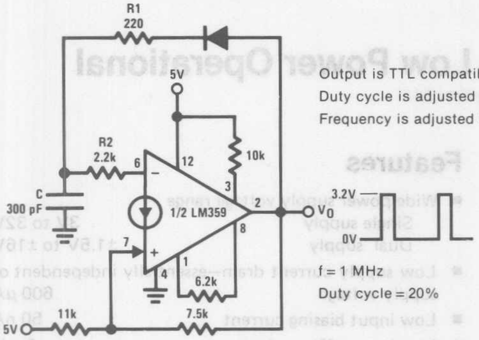
Type I	$\frac{2\,V_{IN(DC)}}{V^+(R_{i2})} + \frac{1}{R} + \frac{1}{R_Q} = \frac{2}{R_b}$; $R1 = 2R$
Type II	$\frac{1}{R} + \frac{1}{R_Q} = \frac{2}{R_b}$; $R1 = 2R$
Type III	$\frac{1}{R} + \frac{1}{R_Q} = \frac{2}{R_b}$; $\frac{1}{R1} = \frac{V_{IN(DC)}}{V^+(R_{i1})} + \frac{1}{2R}$

ANALYSIS AND DESIGN EQUATIONS

Type	V_{O1}	V_{O2}	C_i	R_{i2}	R_{i1}	f_o	Q_o	f_Z (notch)	$H_{o(LP)}$	$H_{o(BP)}$	$H_{o(HP)}$	$H_{o(BR)}$
I	BP	LP	O	R_{i2}	∞	$1/2\pi RC$	R_Q/R	—	R/R_{i2}	R_Q/R_{i2}	—	—
II	HP	BP	C_i	∞	∞	$1/2\pi RC$	R_Q/R	—	—	R_QC_i/RC	C_i/C	—
III	Notch/BR	—	C_i	∞	R_{i1}	$1/2\pi RC$	R_Q/R	$1/2\pi\sqrt{RR_iCC_i}$	—	—	—	$H_o\big\vert_{f\to\infty} = C_i/C$ $H_o\big\vert_{f\to 0} = R/R_i$

Typical Applications (Continued)

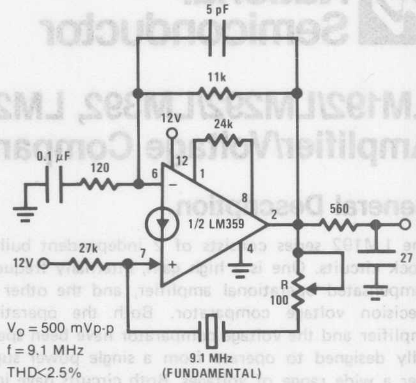
Pulse Generator



Output is TTL compatible
Duty cycle is adjusted by R1
Frequency is adjusted by C

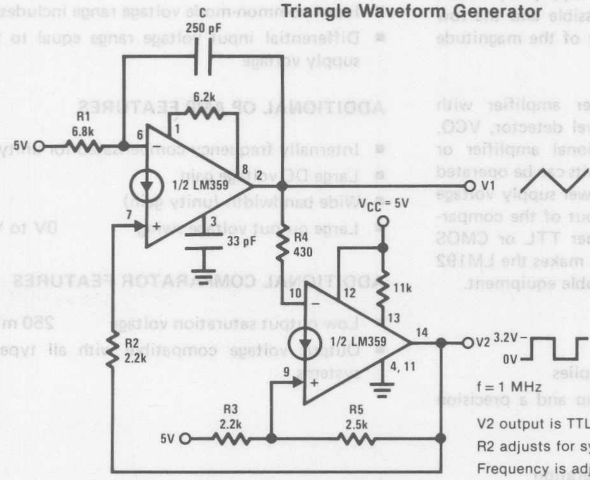
f = 1 MHz
Duty cycle = 20%

Crystal Controlled Sinewave Oscillator



V_O = 500 mVp-p
f = 9.1 MHz
THD<2.5%

Triangle Waveform Generator



f = 1 MHz
V2 output is TTL compatible
R2 adjusts for symmetry of the triangle waveform
Frequency is adjusted with R5 and C

LM192/LM292/LM392, LM2924 Low Power Operational Amplifier/Voltage Comparator

General Description

The LM192 series consists of 2 independent building block circuits. One is a high gain, internally frequency compensated operational amplifier, and the other is a precision voltage comparator. Both the operational amplifier and the voltage comparator have been specifically designed to operate from a single power supply over a wide range of voltages. Both circuits have input stages which will common-mode input down to ground when operating from a single power supply. Operation from split power supplies is also possible and the low power supply current is independent of the magnitude of the supply voltage.

Application areas include transducer amplifier with pulse shaper, DC gain block with level detector, VCO, as well as all conventional operational amplifier or voltage comparator circuits. Both circuits can be operated directly from the standard 5 V_{DC} power supply voltage used in digital systems, and the output of the comparator will interface directly with either TTL or CMOS logic. In addition, the low power drain makes the LM192 extremely useful in the design of portable equipment.

Advantages

- Eliminates need for dual power supplies
- An internally compensated op amp and a precision comparator in the same package
- Allows sensing at or near ground
- Power drain suitable for battery operation
- Pin-out is the same as both the LM158 dual op amp and the LM193 dual comparator

Features

- Wide power supply voltage range
  - Single supply 3V to 32V
  - Dual supply ±1.5V to ±16V
- Low supply current drain—essentially independent of supply voltage 600 μA
- Low input biasing current 50 nA
- Low input offset voltage 2 mV
- Low input offset current 5 nA
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage

ADDITIONAL OP AMP FEATURES

- Internally frequency compensated for unity gain
- Large DC voltage gain 100 dB
- Wide bandwidth (unity gain) 1 MHz
- Large output voltage swing 0V to $V^+ - 1.5V$

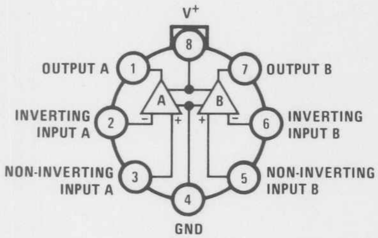
ADDITIONAL COMPARATOR FEATURES

- Low output saturation voltage 250 mV at 4 mA
- Output voltage compatible with all types of logic systems

Connection Diagrams (Top Views)

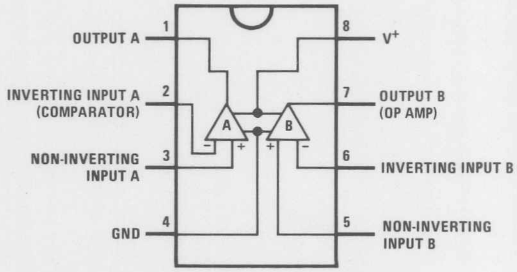
(Amplifier A = Comparator)
(Amplifier B = Operational Amplifier)

Metal Can Package



Order Number LM192H, LM292H or LM392H
See NS Package H08C

Dual-In-Line Package



Order Number LM192J, LM292J, LM392J or LM2924J
See NS Package J08A

Order Number LM392N or LM2924N
See NS Package N08B

Supply Voltage, V^+	32V or ±16V	26V or ±13V
Differential Input Voltage	32V	26V
Input Voltage	−0.3V to +32V	−0.3V to +26V
Power Dissipation (Note 1)		
Molded DIP (LM392N, LM2924N)	570 mW	570 mW
Metal Can (LM192H/LM292H/LM392H)	830 mW	
Output Short-Circuit to Ground (Note 2)	Continuous	Continuous
Input Current ($V_{IN} < -0.3\ V_{DC}$) (Note 3)	50 mA	50 mA
Operating Temperature Range		−40°C to +85°C
LM392	0°C to +70°C	
LM292	−25°C to +85°C	
LM192	−55°C to +125°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

Electrical Characteristics ($V^+ = 5\ V_{DC}$; specifications apply to both amplifiers unless otherwise stated) (Note 4)

PARAMETER	CONDITIONS	LM192			LM292/LM392			LM2924			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$, (Note 5)		±2	±5		±2	±5		±2	±7	mV
Input Bias Current	IN(+) or IN(−), $T_A = 25°C$, (Note 6)		50	150		50	250		50	250	nA
Input Offset Current	IN(+) − IN(−), $T_A = 25°C$		±3	±25		±5	±50		±5	±50	nA
Input Common-Mode Voltage Range	$V^+ = 30\ V_{DC}$, $T_A = 25°C$, (Note 7)	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	V
Supply Current	$R_L = \infty$, $V_{CC} = 30V$, (LM2924, $V_{CC} = 26V$)		1	2		1	2		1	2	mA
Supply Current	$R_L = \infty$, $V_{CC} = 5V$		0.5	1		0.5	1		0.5	1	mA
Amplifier-to-Amplifier Coupling	f = 1 kHz to 20 kHz, $T_A = 25°C$, Input Referred, (Note 8)		−100			−100			−100		dB
Input Offset Voltage	(Note 5)			±7			±7			±10	mV
Input Bias Current	IN(+) or IN(−)			300			400			500	nA
Input Offset Current	IN(+) − IN(−)			100			150			200	nA
Input Common-Mode Voltage Range	$V^+ = 30\ V_{DC}$, (Note 7)	0		V^+-2	0		V^+-2	0		V^+-2	V
Differential Input Voltage	Keep All V_{IN}'s ≥ 0 V_{DC} (or V^-, if Used), (Note 9)			32			32			26	V
OP AMP ONLY											
Large Signal Voltage Gain	$V^+ = 15\ V_{DC}$ (For Large V_o Swing), $R_L = 2\ k\Omega$, $T_A = 25°C$	50	100		25	100			100		V/mV
Output Voltage Swing	$R_L = 2\ k\Omega$, $T_A = 25°C$, (LM2924, $R_L \geq 10\ k\Omega$)	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	V
Common-Mode Rejection Ratio	DC, $T_A = 25°C$	70	85		65	70		50	70		dB
Power Supply Rejection Ratio	DC, $T_A = 25°C$	65	100		65	100		50	100		dB
Output Current Source	$V_{IN(+)} = 1\ V_{DC}$, $V_{IN(-)} = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $T_A = 25°C$	20	40		20	40		20	40		mA
Output Current Sink	$V_{IN(-)} = 1\ V_{DC}$, $V_{IN(+)} = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $V_o \geq 1\ V_{DC}$, $T_A = 25°C$	10	20		10	20		10	20		mA
	$V_{IN(-)} = 1\ V_{DC}$, $V_{IN(+)} = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $V_o = 200$ mV, $T_A = 25°C$	12	50		12	50		12	50		μA

Electrical Characteristics (Continued)

PARAMETER	CONDITIONS	LM192			LM292/LM392			LM2924			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Drift	$R_S = 0\Omega$		7			7			7		$\mu V/^{\circ}C$
Input Offset Current Drift	$R_S = 0\Omega$		10			10			10		$pA_{DC}/^{\circ}C$
COMPARATOR ONLY											
Voltage Gain	$R_L \geq 15\ k\Omega$, $V^+ = 15\ V_{DC}$, $T_A = 25^{\circ}C$	50	200		50	200		25	100		$V/\mu V$
Large Signal Response Time	V_{IN} = TTL Logic Swing, $V_{REF} = 1.4\ V_{DC}$, $V_{RL} = 5\ V_{DC}$, $R_L = 5.1\ k\Omega$, $T_A = 25^{\circ}C$		300			300			300		ns
Response Time	$V_{RL} = 5\ V_{DC}$, $R_L = 5.1\ k\Omega$, $T_A = 25^{\circ}C$, (Note 10)		1.3			1.3			1.5		μs
Output Sink Current	$V_{IN(-)} = 1\ V_{DC}$, $V_{IN(+)} = 0\ V_{DC}$, $V_o \leq 1.5\ V_{DC}$, $T_A = 25^{\circ}C$	6	16		6	16		6	16		mA
Saturation Voltage	$V_{IN(-)} \geq 1\ V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4\ mA$, $T_A = 25^{\circ}C$		250	400		250	400			400	mV
	$V_{IN(-)} \geq 1\ V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4\ mA$			700			700			700	mV
Output Leakage Current	$V_{IN(-)} = 0$, $V_{IN(+)} \geq 1\ V_{DC}$, $V_o = 5\ V_{DC}$, $T_A = 25^{\circ}C$		0.1			0.1			0.1		nA
	$V_{IN(-)} = 0$, $V_{IN(+)} \geq 1\ V_{DC}$, $V_o = 30\ V_{DC}$			1.0			1.0			1.0	μA

Note 1: For operating at temperatures above 25°C, the LM392N and the LM2924N must be derated based on a 125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in still air ambient. The LM192H/LM292H/LM392H must be derated based on a 150°C maximum junction temperature and a thermal resistance of 150°C/W. The dissipation is the total of both amplifiers—use external resistors, where possible, to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40 mA for the op amp and 30 mA for the comparator independent of the magnitude of V^+. At values of supply voltage in excess of 15V, continuous short circuits can exceed the power dissipation ratings and cause eventual destruction.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the amplifiers to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3V (at 25°C).

Note 4: These specifications apply for $V^+ = 5V$ and $-55^{\circ}C \leq T_A \leq +125^{\circ}C$, unless otherwise stated. For the LM292, all temperature specifications are limited to $-25^{\circ}C \leq T_A \leq +85^{\circ}C$, the LM392 temperature specifications are limited to $0^{\circ}C \leq T_A \leq +70^{\circ}C$ and the LM2924 temperature specifications are limited to $-40^{\circ}C \leq T_A \leq +85^{\circ}C$.

Note 5: At output switch point, $V_O \cong 1.4V$, $R_S = 0\Omega$ with V^+ from 5V to 30V; and over the full input common-mode range (0V to $V^+ - 1.5V$).

Note 6: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

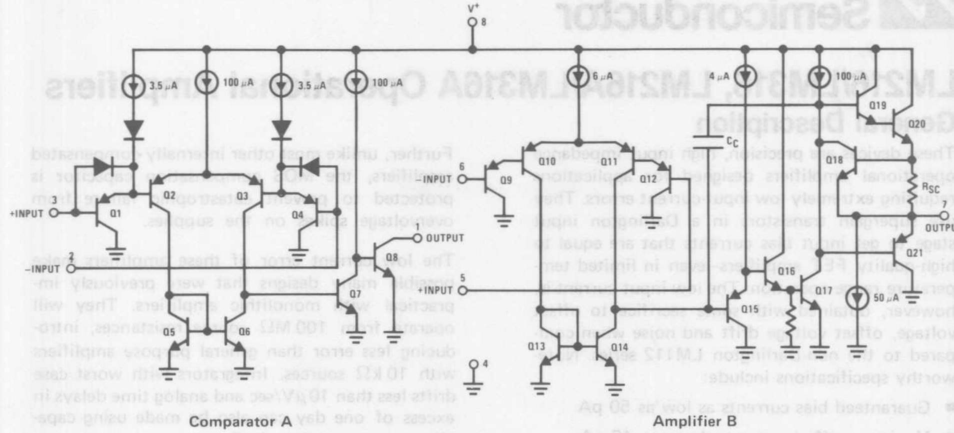
Note 7: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+ - 1.5V$, but either or both inputs can go to 32V without damage (26V for LM2924).

Note 8: Due to proximity of external components, insure that coupling is not originating via the stray capacitance between these external parts. This typically can be detected as this type of capacitive increases at higher frequencies.

Note 9: Positive excursions of input voltage may exceed the power supply level. As long as the other input voltage remains within the common-mode range, the comparator will provide a proper output state. The input voltage to the op amp should not exceed the power supply level. The input voltage state must not be less than −0.3V (or 0.3V below the magnitude of the negative power supply, if used) on either amplifier.

Note 10: The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained.

Schematic Diagram



Application Hints

Please refer to the application hints section of the LM193 and the LM158 data sheets.

LM216/LM316, LM216A/LM316A Operational Amplifiers

General Description

These devices are precision, high input impedance operational amplifiers designed for applications requiring extremely low input-current errors. They use supergain transistors in a Darlington input stage to get input bias currents that are equal to high-quality FET amplifiers—even in limited temperature range operation. The low input current is, however, obtained with some sacrifice to offset voltage, offset voltage drift and noise when compared to the non-Darlington LM112 series. Noteworthy specifications include:

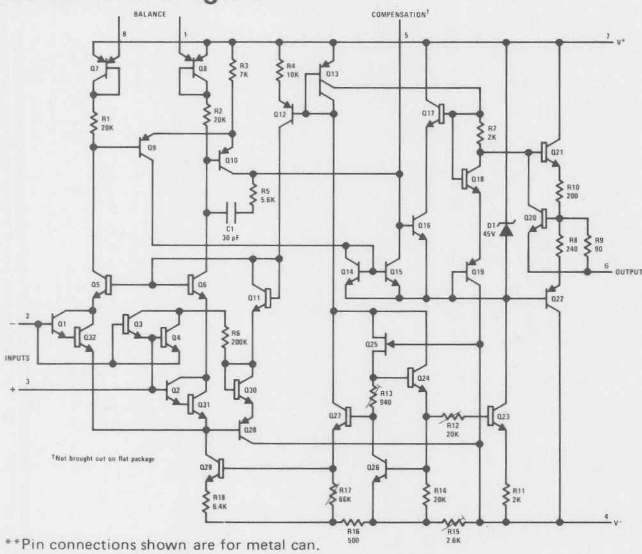
- Guaranteed bias currents as low as 50 pA
- Maximum offset currents down to 15 pA
- Operates from supplies of ±3V to ±20V
- Supply current only 300 μA at ±20V

These operational amplifiers are internally frequency compensated and have provisions for offset balancing with a single external potentiometer. Further, unlike most other internally compensated amplifiers, the MOS compensation capacitor is protected to prevent catastrophic failure from overvoltage spikes on the supplies.

The low current error of these amplifiers make possible many designs that were previously impractical with monolithic amplifiers. They will operate from 100 MΩ source resistances, introducing less error than general purpose amplifiers with 10 kΩ sources. Integrators with worst case drifts less than 10 μV/sec and analog time delays in excess of one day can also be made using capacitors no larger than 1 μF.

The LM216A and LM316A are high performance versions of the LM216 and LM316. The LM216 and LM216A are specified for operation from −25°C to 85°C, while the LM316 and LM316A are specified from 0°C to 55°C.

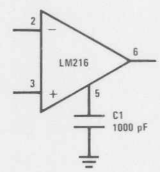
Schematic Diagram**



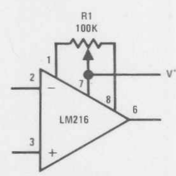
**Pin connections shown are for metal can.

Auxiliary Circuits**

Overcompensation for Greater Stability Margin

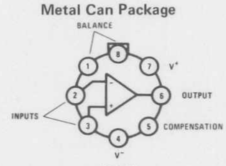


Offset Balancing



Connection Diagrams

Metal Can Package



Order Number LM216H or LM216AH or LM316H or LM316AH
See NS Package H08C

Differential Input Current (Note 2)		±10 mA
Input Voltage (Note 3)		±15V
Output Short-Circuit Duration		Indefinite
Operating Temperature Range	LM216/LM216A	$-25^{\circ}C$ to $85^{\circ}C$
	LM316/LM316A	$0^{\circ}C$ to $70^{\circ}C$
Storage Temperature Range		$-65^{\circ}C$ to $150^{\circ}C$
Lead Temperature (Soldering, 10 sec)		$300^{\circ}C$

Electrical Characteristics (Note 4)

PARAMETER	CONDITIONS	LM216A	LM216	LM316A	LM316	UNITS
Input Offset Voltage	$T_A = 25^{\circ}C$, Max	3	10	3	10	mV
Input Offset Current	$T_A = 25^{\circ}C$, Max	15	50	15	50	pA
Input Bias Current	$T_A = 25^{\circ}C$, Max	50	150	50	150	pA
Input Resistance	$T_A = 25^{\circ}C$, Min	5	1	5	1	GΩ
Supply Current	$T_A = 25^{\circ}C$, Max	0.6	0.8	0.6	0.8	mA
Large Signal Voltage Gain	$T_A = 25^{\circ}C$, $V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 10\ k\Omega$, Min	40	20	40	20	V/mV
Input Offset Voltage	Max	6	15	6	15	mV
Input Offset Current	Max	30	100	30	100	pA
Input Bias Current	Max	100	250	100	250	pA
Supply Current	$T_A = T_{MAX}$, Max	0.5		0.5		mA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L > 10\ k\Omega$, Min	20	10	30	15	V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$, Min	±13	±13	±13	±13	V
Input Voltage Range	$V_S = \pm 15V$, Min	±13	±13	±13	±13	V
Common-Mode Rejection Ratio	Min	80	80	80	80	dB
Supply Voltage Rejection Ratio	Min	80	80	80	80	dB

Note 1: The maximum junction temperature of the LM216 and LM216A is 100°C, while that of the LM316 and LM316A is 70°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case.

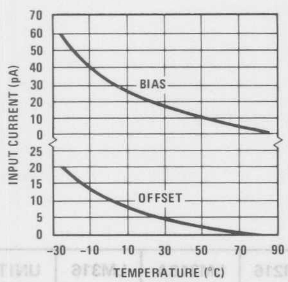
Note 2: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

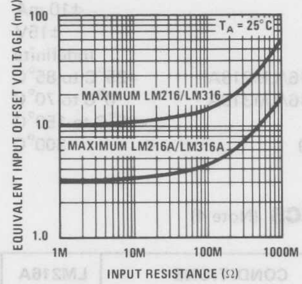
Note 4: These specifications apply for $\pm 5V \leq V_S \leq \pm 20V$ and $-25^{\circ}C \leq T_A \leq 85^{\circ}C$, unless otherwise specified. With the LM316 and LM316A however, all temperature specifications are limited to $0^{\circ}C \leq T_A \leq 55^{\circ}C$.

Typical Performance Characteristics

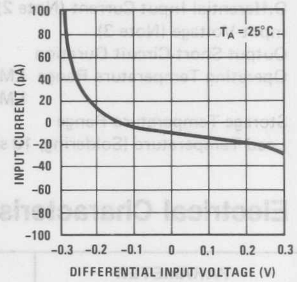
Input Currents



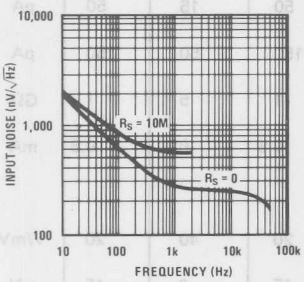
Offset Error



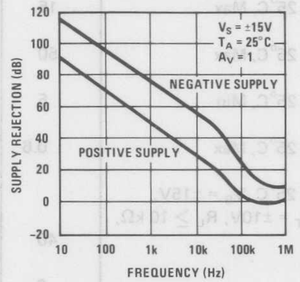
Input Current



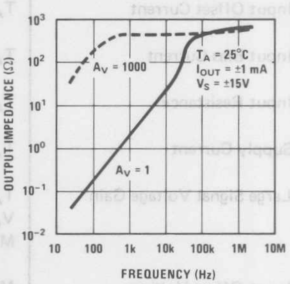
Input Noise Voltage



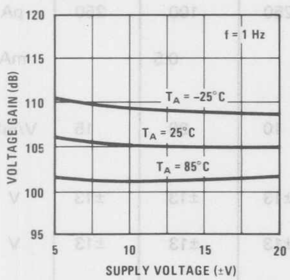
Power Supply Rejection



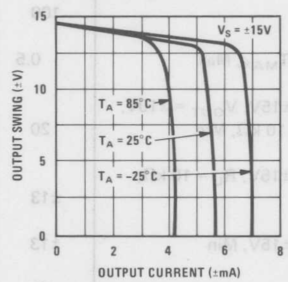
Closed Loop Output Impedance



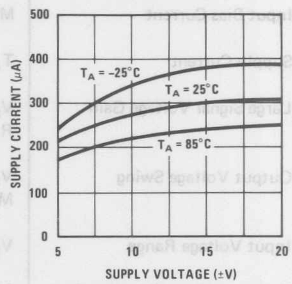
Voltage Gain



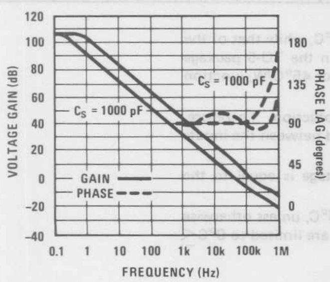
Output Swing



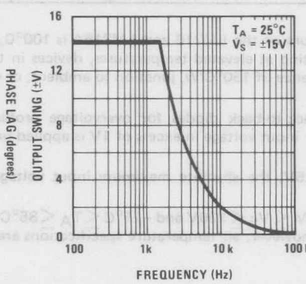
Supply Current



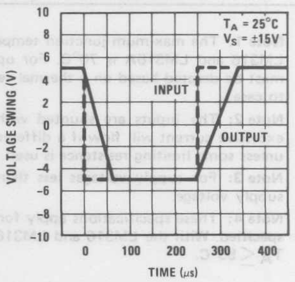
Open Loop Frequency Response



Large Signal Frequency Response



Voltage Follower Pulse Response



LM709/LM709A/LM709C Operational Amplifier

General Description

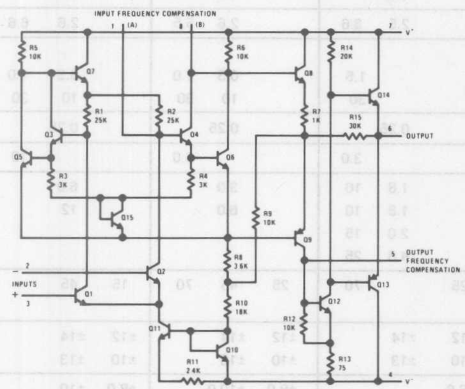
The LM709 series are a monolithic operational amplifier intended for general-purpose applications. Operation is completely specified over the range of voltages commonly used for these devices. The design, in addition to providing high gain, minimizes both offset voltage and bias currents. Further, the class-B output stage gives a large output capability with minimum power drain.

External components are used to frequency compensate the amplifier. Although the unity-gain compensation network specified will make the amplifier unconditionally stable in all feedback configurations, compensation can be tailored to optimize high-frequency performance for any gain setting.

The fact that the amplifier is built on a single silicon chip provides low offset and temperature drift at minimum cost. It also ensures negligible drift due to temperature gradients in the vicinity of the amplifier.

The LM709C is commercial-industrial version of the LM709. It is identical to the LM709/LM709A except that it is specified for operation from 0°C to +70°C.

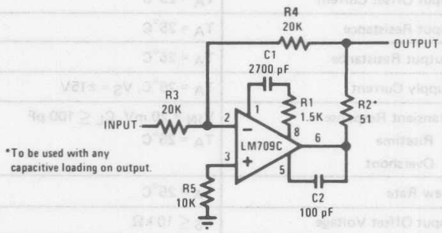
Schematic Diagram**



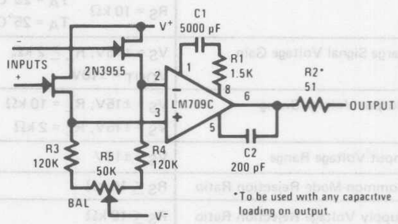
**Pin connections shown are for metal can package.

Typical Applications**

Unity Gain Inverting Amplifier

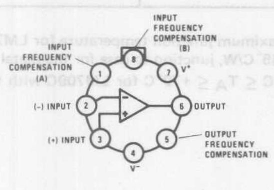


FET Operational Amplifier



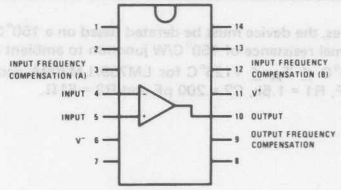
Connection Diagrams

Metal Can Package



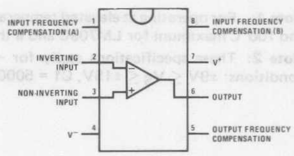
Order Number LM709H or LM709CH
See NS Package H08C

Dual-In-Line Package



Order Number LM709CN
See NS Package N14A

Dual-In-Line Package



Order Number LM709CN-8
See NS Package N08A

	LM709/LM709A	LM709C
Supply Voltage	±18V	±18V
Power Dissipation (Note 1)	300 mW	250 mW
Differential Input Voltage	±5V	±5V
Input Voltage	±10V	±10V
Output Short-Circuit Duration (T_A = 25°C)	5 seconds	5 seconds
	T_{MIN} T_{MAX}	T_{MIN} T_{MAX}
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C	0°C to +70°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

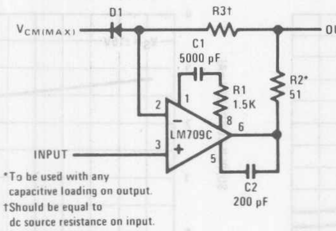
Electrical Characteristics (Note 2)

PARAMETER	CONDITIONS	LM709A MIN	LM709A TYP	LM709A MAX	LM709 MIN	LM709 TYP	LM709 MAX	LM709C MIN	LM709C TYP	LM709C MAX	UNITS
Input Offset Voltage	T_A = 25°C, $R_S \leq$ 10 kΩ		0.6	2.0		1.0	5.0		2.0	7.5	mV
Input Bias Current	T_A = 25°C		100	200		200	500		300	1500	nA
Input Offset Current	T_A = 25°C		10	50		50	200		100	500	nA
Input Resistance	T_A = 25°C	350	700		150	400		50	250		kΩ
Output Resistance	T_A = 25°C		150			150			150		Ω
Supply Current	T_A = 25°C, V_S = ±15V		2.5	3.6		2.6	5.5		2.6	6.6	mA
Transient Response	V_{IN} = 20 mV, $C_L \leq$ 100 pF										
Risetime	T_A = 25°C			1.5		0.3	1.0		0.3	1.0	µs
Overshoot				30		10	30		10	30	%
Slew Rate	T_A = 25°C		0.25			0.25			0.25		V/µs
Input Offset Voltage	$R_S \leq$ 10 kΩ			3.0			6.0			10	mV
Average Temperature Coefficient of Input Offset Voltage	R_S = 50Ω, T_A = 25°C to T_{MAX}		1.8	10		3.0			6.0		µV/°C
	R_S = 50Ω, T_A = 25°C to T_{MIN}		1.8	10		6.0			12		µV/°C
	R_S = 10 kΩ, T_A = 25°C to T_{MAX}		2.0	15							
	R_S = 10 kΩ, T_A = 25°C to T_{MIN}		4.8	25							
Large Signal Voltage Gain	V_S = ±15V, $R_L \geq$ 2 kΩ, V_{OUT} = ±10V	25		70	25	45	70	15	45		V/mV
Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±12	±14		±12	±14		±12	±14		V
	V_S = ±15V, R_L = 2 kΩ	±10	±13		±10	±13		±10	±13		V
Input Voltage Range	V_S = ±15V	±8.0			±8.0	±10.0		±8.0	±10		V
Common-Mode Rejection Ratio	$R_S \leq$ 10 kΩ	80	110		70	90		65	90		dB
Supply Voltage Rejection Ratio	$R_S \leq$ 10 kΩ		40	100		25	150		25	200	µV/V
Input Offset Current	T_A = T_{MAX}		3.5	50		20	200		75	400	nA
	T_A = T_{MIN}		40	250		100	500		125	750	nA
Input Bias Current	T_A = T_{MIN}		0.3	0.6		0.5	1.5		0.36	2.0	µA
Input Resistance	T_A = T_{MIN}	85	170		40	100		50	250		kΩ

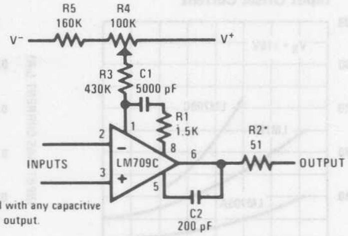
Note 1: For operating at elevated temperatures, the device must be derated based on a 150°C maximum junction temperature for LM709/LM709A and 100°C maximum for LM709C and a thermal resistance of 150°C/W junction to ambient or 45°C/W, junction to case for the metal can package.

Note 2: These specifications apply for −55°C ≤ T_A ≤ +125°C for LM709/LM709A and 0°C ≤ T_A ≤ +70°C for LM709C with the following conditions: ±9V ≤ V_S ≤ ±15V, C1 = 5000 pF, R1 = 1.5k, C2 = 200 pF and R2 = 51Ω.

Voltage Follower

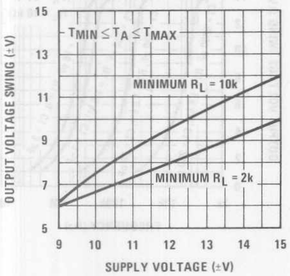


Offset Balancing Circuit

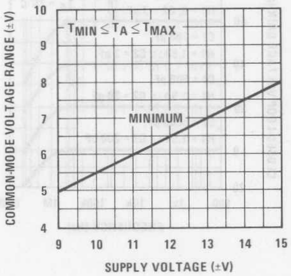


Guaranteed Performance Characteristics

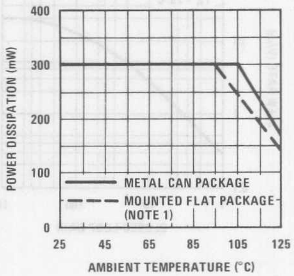
Output Voltage Swing



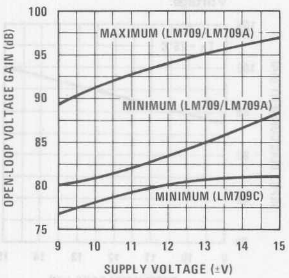
Input Common-Mode Voltage Range



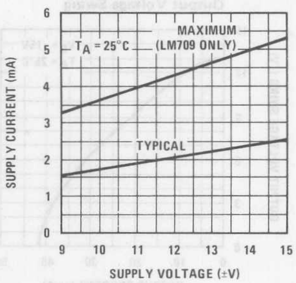
Maximum Power Dissipation



Voltage Gain

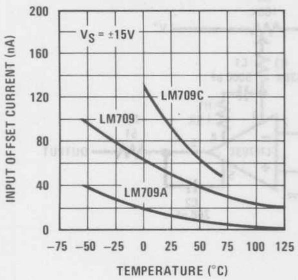


Supply Current

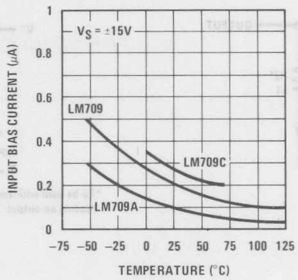


Typical Performance Characteristics

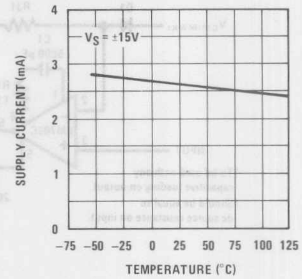
Input Offset Current



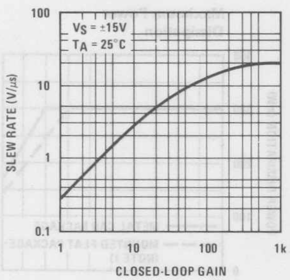
Input Bias Current



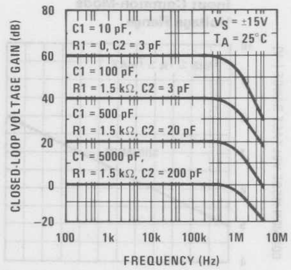
Supply Current



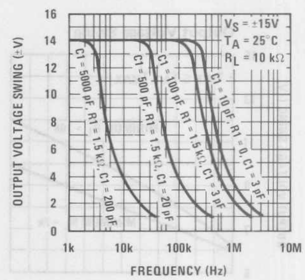
Slew Rate as a Function of Closed-Loop Gain Using Recommended Compensation Networks



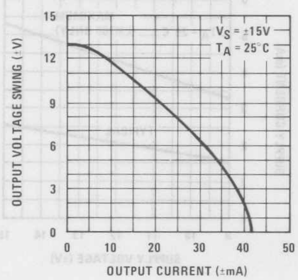
Frequency Response For Various Closed-Loop Gains



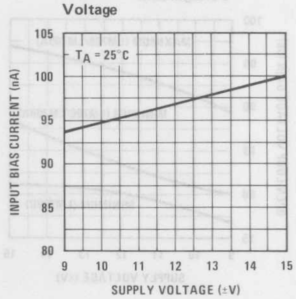
Output Voltage Swing as a Function of Frequency



Output Voltage Swing



Input Bias Current as a Function of Supply Voltage



National Semiconductor

LM725/LM725A/LM725C (Instrumentation) Operational Amplifier

General Description

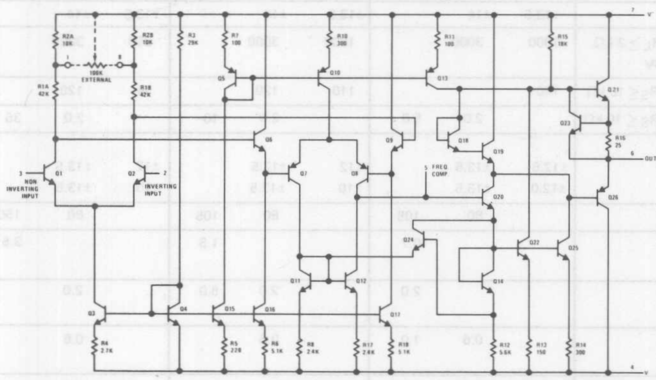
The LM725/LM725A/LM725C are operational amplifiers featuring superior performance in applications where low noise, low drift, and accurate closed-loop gain are required. With high common mode rejection and offset null capability, it is especially suited for low level instrumentation applications over a wide supply voltage range.

The LM725A has tightened electrical performance with higher input accuracy and like the LM725, is guaranteed over a −55°C to +125°C temperature range. The LM725C has slightly relaxed specifications and has its performance guaranteed over a 0°C to 70°C temperature range.

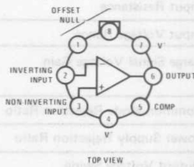
Features

- High open loop gain 3,000,000
- Low input voltage drift 0.6 μV/°C
- High common mode rejection 120 dB
- Low input noise current 0.15 pA/$\sqrt{Hz}$
- Low input offset current 2 nA
- High input voltage range ±14V
- Wide power supply range ±3V to ±22V
- Offset null capability
- Output short circuit protection

Schematic and Connection Diagrams



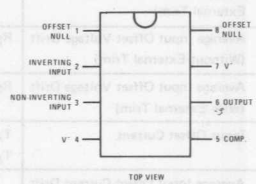
Metal Can Package



TOP VIEW

Order Number LM725H or LM725AH or LM725CH
See NS Package H08C

Dual-In-Line Package

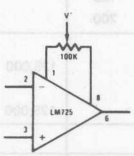


TOP VIEW

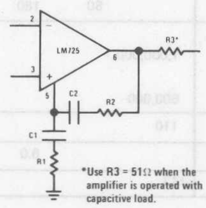
Order Number LM725CN
See NS Package N08B

Auxiliary Circuits

Voltage Offset Null Circuit



Frequency Compensation Circuit



*Use R3 = 51Ω when the amplifier is operated with capacitive load.

Compensation Component Values

A_{VCL}	R1 (Ω)	C1 (μF)	R2 (Ω)	C2 (μF)
10,000	10K	50 pF	–	–
1,000	470	.001	–	–
100	47	.01	–	–
10	27	.05	270	.0015
1	10	.05	39	.02

Internal Power Dissipation (Note 1)	500 mV
Differential Input Voltage	±5V
Input Voltage (Note 2)	±22V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

Temperature Range	$T_{A(MIN)}$		$T_{A(MAX)}$
LM725	−55°C	to	+125°C
LM725A	−55°C	to	+125°C
LM725C	0°C	to	+70°C

Electrical Characteristics (Note 3)

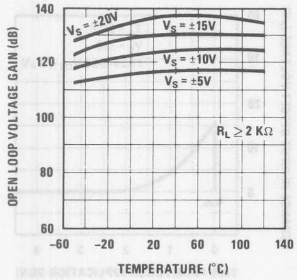
PARAMETER	CONDITIONS	LM725A			LM725			LM725C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage (Without External Trim)	$T_A = 25°C$, $R_S \leq 10\ k\Omega$			0.5		0.5	1.0		0.5	2.5	mV
Input Offset Current	$T_A = 25°C$		2.0	5.0		2.0	20		2.0	35	nA
Input Bias Current	$T_A = 25°C$		42	80		42	100		42	125	nA
Input Noise Voltage	$T_A = 25°C$										
	$f_o = 10$ Hz		15			15			15		$nV/\sqrt{Hz}$
	$f_o = 100$ Hz		9.0			9.0			9.0		$nV/\sqrt{Hz}$
	$f_o = 1$ kHz		8.0			8.0			8.0		$nV/\sqrt{Hz}$
Input Noise Current	$T_A = 25°C$										
	$f_o = 10$ Hz		1.0			1.0			1.0		$pA/\sqrt{Hz}$
	$f_o = 100$ Hz		0.3			0.3			0.3		$pA/\sqrt{Hz}$
	$f_o = 1$ kHz		0.15			0.15			0.15		$pA/\sqrt{Hz}$
Input Resistance	$T_A = 25°C$		1.5			1.5			1.5		MΩ
Input Voltage Range	$T_A = 25°C$	±13.5	±14		±13.5	±14		±13.5	±14		V
Large Signal Voltage Gain	$T_A = 25°C$, $R_L \geq 2\ k\Omega$, $V_{OUT} = \pm 10V$	1000	3000		1000	3000		250	3000		V/mV
Common-Mode Rejection Ratio	$T_A = 25°C$, $R_S \leq 10\ k\Omega$	120			110	120		94	120		dB
Power Supply Rejection Ratio	$T_A = 25°C$, $R_S \leq 10\ k\Omega$		2.0	5.0		2.0	10		2.0	35	μV/V
Output Voltage Swing	$T_A = 25°C$,										
	$R_L \geq 10\ k\Omega$	±12.5	±13.5		±12	±13.5		±12	±13.5		V
	$R_L \geq 2\ k\Omega$	±12.0	±13.5		±10	±13.5		±10	±13.5		V
Power Consumption	$T_A = 25°C$		80	105		80	105		80	150	mW
Input Offset Voltage (Without External Trim)	$R_S \leq 10\ k\Omega$			0.7			1.5			3.5	mV
Average Input Offset Voltage Drift (Without External Trim)	$R_S = 50\Omega$		2.0			2.0	5.0		2.0		μV/°C
Average Input Offset Voltage Drift (With External Trim)	$R_S = 50\Omega$		0.6	1.0		0.6			0.6		μV/°C
Input Offset Current	$T_A = T_{MAX}$		1.2	4.0		1.2	20		1.2	35	nA
	$T_A = T_{MIN}$		7.5	18.0		7.5	40		4.0	50	nA
Average Input Offset Current Drift			35	90		35	150		10		pA/°C
Input Bias Current	$T_A = T_{MAX}$		20	70		20	100			125	nA
	$T_A = T_{MIN}$		80	180		80	200			250	nA
Large Signal Voltage Gain	$R_L \geq 2\ k\Omega$, $T_A = T_{MAX}$	1,000,000			1,000,000			125,000			V/V
	$R_L \geq 2\ k\Omega$, $T_A = T_{MIN}$	500,000			250,000			125,000			V/V
Common-Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	110			100				115		dB
Power Supply Rejection Ratio	$R_S \leq 10\ k\Omega$			8.0			20		20		μV/V
Output Voltage Swing	$R_L \geq 2\ k\Omega$	±12			±10			±10			V

Note 1: Derate at 150°C/W for operation at ambient temperatures above 75°C.

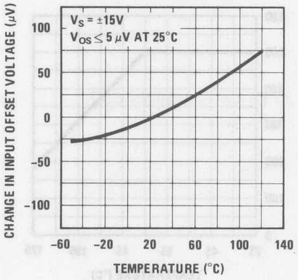
Note 2: For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: These specifications apply for $V_S = \pm 15V$ unless otherwise specified.

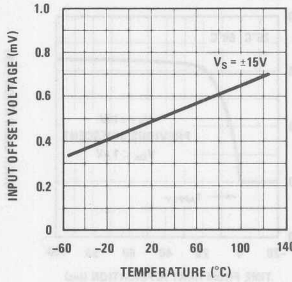
Open Loop Voltage Gain vs Temperature for Various Supply Voltages



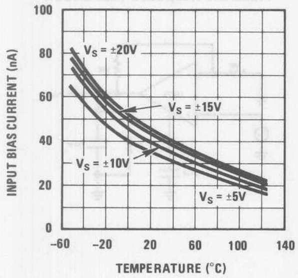
Nulled Input Offset Voltage vs Temperature



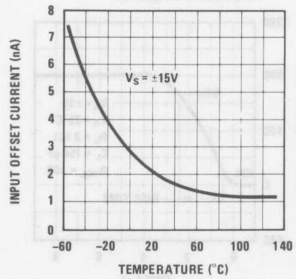
Unnulled Input Offset Voltage vs Temperature



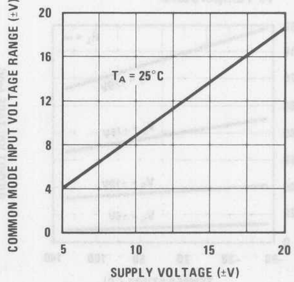
Input Bias Current vs Temperature



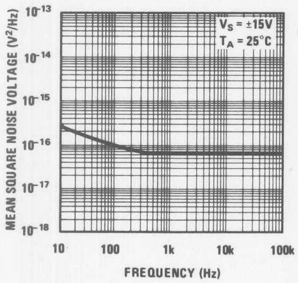
Input Offset Current vs Temperature



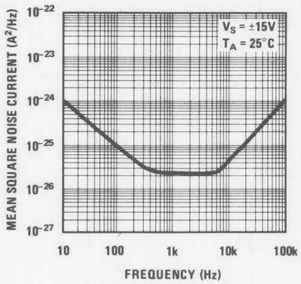
Common Mode Input Voltage vs Supply Voltage



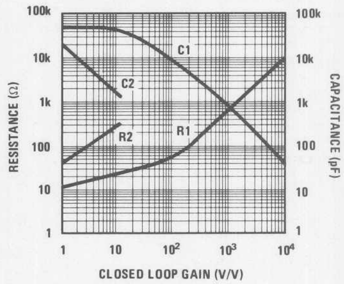
Input Noise Voltage vs Frequency



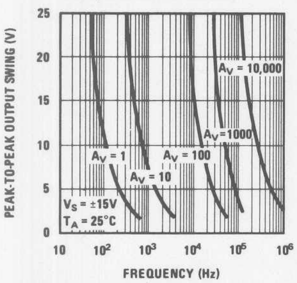
Input Noise Current vs Frequency



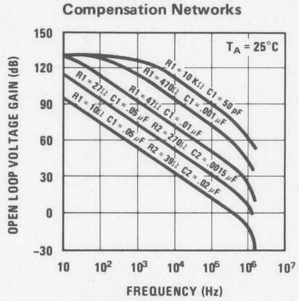
Values for Suggested Compensation Networks for Various Closed Loop Voltage Gains



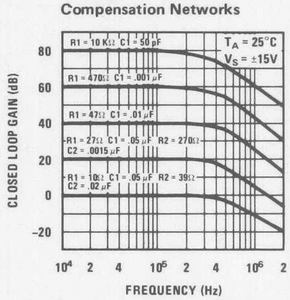
Output Voltage Swing vs Frequency for Recommended Compensation Networks



Open Loop Voltage Gain vs Frequency Using Recommended Compensation Networks

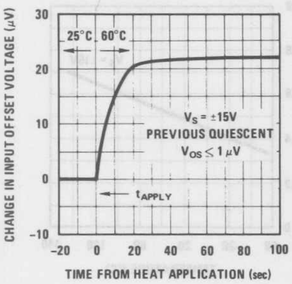


Frequency Response for Various Closed-Loop Gains Using Recommended Compensation Networks

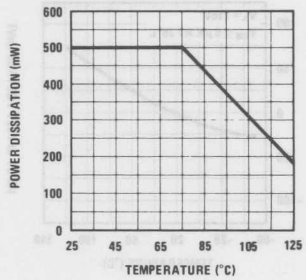


Typical Performance Characteristics (Continued)

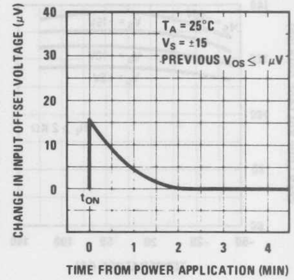
Change in Input Offset Voltage Due to Thermal Shock vs Time



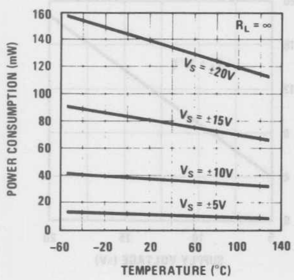
Absolute Maximum Power Dissipation vs Ambient Temperature



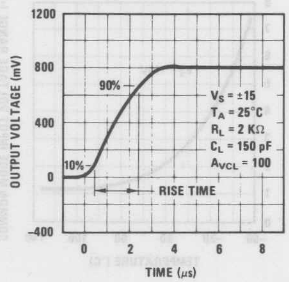
Stabilization Time of Input Offset Voltage from Power Turn-On



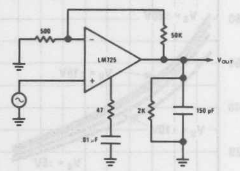
Power Consumption vs Temperature



Transient Response



Transient Response Test Circuit



National Semiconductor

Operational Amplifiers/Buffers

LM741/LM741A/LM741C/LM741E Operational Amplifier

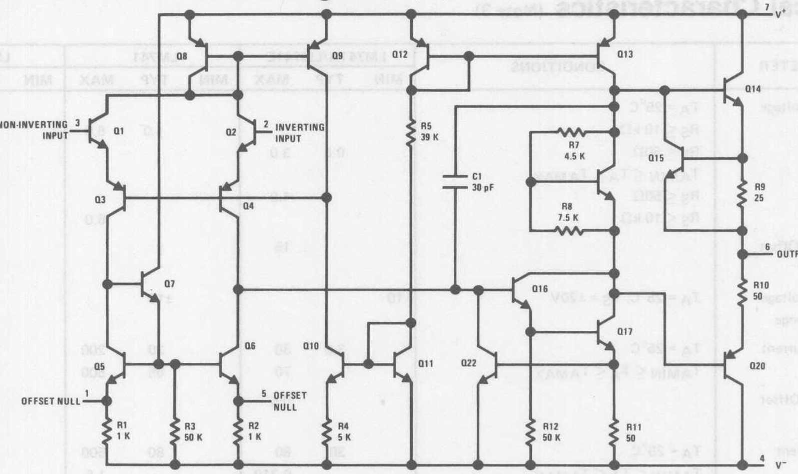
General Description

The LM741 series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439 and 748 in most applications.

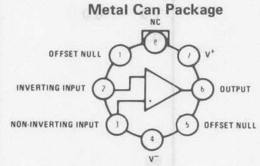
The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations.

The LM741C/LM741E are identical to the LM741/LM741A except that the LM741C/LM741E have their performance guaranteed over a 0°C to +70°C temperature range, instead of −55°C to +125°C.

Schematic and Connection Diagrams (Top Views)

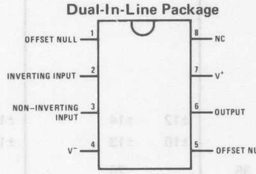


Metal Can Package



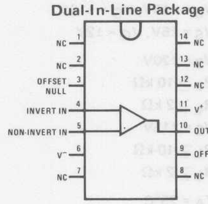
Order Number LM741H, LM741AH, LM741CH or LM741EH
See NS Package H08C

Dual-In-Line Package



Order Number LM741CN or LM741EN
See NS Package N08B
Order Number LM741CJ
See NS Package J08A

Dual-In-Line Package



Order Number LM741CN-14
See NS Package N14A
Order Number LM741J-14, LM741AJ-14 or LM741CJ-14
See NS Package J14A

Absolute Maximum Ratings

	LM741A	LM741E	LM741	LM741C
Supply Voltage	±22V	±22V	±22V	±18V
Power Dissipation (Note 1)	500 mW	500 mW	500 mW	500 mW
Differential Input Voltage	±30V	±30V	±30V	±30V
Input Voltage (Note 2)	±15V	±15V	±15V	±15V
Output Short Circuit Duration	Indefinite	Indefinite	Indefinite	Indefinite
Operating Temperature Range	−55°C to +125°C	0°C to +70°C	−55°C to +125°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	300°C	300°C

Electrical Characteristics (Note 3)

PARAMETER	CONDITIONS	LM741A/LM741E			LM741			LM741C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$										
	$R_S \leq 10\ k\Omega$					1.0	5.0		2.0	6.0	mV
	$R_S \leq 50\Omega$		0.8	3.0							mV
	$T_{AMIN} \leq T_A \leq T_{AMAX}$										
	$R_S \leq 50\Omega$			4.0							mV
	$R_S \leq 10\ k\Omega$						6.0			7.5	mV
Average Input Offset Voltage Drift				15							µV/°C
Input Offset Voltage Adjustment Range	$T_A = 25°C$, $V_S = \pm 20V$	±10				±15			±15		mV
Input Offset Current	$T_A = 25°C$		3.0	30		20	200		20	200	nA
	$T_{AMIN} \leq T_A \leq T_{AMAX}$			70		85	500			300	nA
Average Input Offset Current Drift				0.5							nA/°C
Input Bias Current	$T_A = 25°C$		30	80		80	500		80	500	nA
	$T_{AMIN} \leq T_A \leq T_{AMAX}$			0.210			1.5			0.8	µA
Input Resistance	$T_A = 25°C$, $V_S = \pm 20V$	1.0	6.0		0.3	2.0		0.3	2.0		MΩ
	$T_{AMIN} \leq T_A \leq T_{AMAX}$, $V_S = \pm 20V$	0.5									MΩ
nput Voltage Range	$T_A = 25°C$							±12	±13		V
	$T_{AMIN} \leq T_A \leq T_{AMAX}$				±12	±13					V
Large Signal Voltage Gain	$T_A = 25°C$, $R_L \geq 2\ k\Omega$										
	$V_S = \pm 20V$, $V_O = \pm 15V$	50									V/mV
	$V_S = \pm 15V$, $V_O = \pm 10V$				50	200		20	200		V/mV
	$T_{AMIN} \leq T_A \leq T_{AMAX}$, $R_L \geq 2\ k\Omega$,										
	$V_S = \pm 20V$, $V_O = \pm 15V$	32									V/mV
	$V_S = \pm 15V$, $V_O = \pm 10V$				25			15			V/mV
	$V_S = \pm 5V$, $V_O = \pm 2V$	10									V/mV
Output Voltage Swing	$V_S = \pm 20V$										
	$R_L \geq 10\ k\Omega$	±16									V
	$R_L \geq 2\ k\Omega$	±15									V
	$V_S = \pm 15V$										
	$R_L \geq 10\ k\Omega$				±12	±14		±12	±14		V
	$R_L \geq 2\ k\Omega$				±10	±13		±10	±13		V
Output Short Circuit Current	$T_A = 25°C$	10	25	35		25			25		mA
	$T_{AMIN} \leq T_A \leq T_{AMAX}$	10		40							mA
Common-Mode Rejection Ratio	$T_{AMIN} \leq T_A \leq T_{AMAX}$										
	$R_S \leq 10\ k\Omega$, $V_{CM} = \pm 12V$				70	90		70	90		dB
	$R_S \leq 50\ k\Omega$, $V_{CM} = \pm 12V$	80	95								dB

PARAMETER	CONDITIONS	LM741A/LM741E			LM741			LM741C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage Rejection Ratio	$T_{AMIN} \le T_A \le T_{AMAX}$, $V_S = \pm 20V$ to $V_S = \pm 5V$										
	$R_S \le 50\Omega$	86	96								dB
	$R_S \le 10\ k\Omega$				77	96		77	96		dB
Transient Response	$T_A = 25°C$, Unity Gain										
Rise Time			0.25	0.8		0.3			0.3		μs
Overshoot			6.0	20		5			5		%
Bandwidth (Note 4)	$T_A = 25°C$	0.437	1.5								MHz
Slew Rate	$T_A = 25°C$, Unity Gain	0.3	0.7			0.5			0.5		V/μs
Supply Current	$T_A = 25°C$					1.7	2.8		1.7	2.8	mA
Power Consumption	$T_A = 25°C$										
	$V_S = \pm 20V$		80	150							mW
	$V_S = \pm 15V$					50	85		50	85	mW
LM741A	$V_S = \pm 20V$										
	$T_A = T_{AMIN}$			165							mW
	$T_A = T_{AMAX}$			135							mW
LM741E	$V_S = \pm 20V$			150							mW
	$T_A = T_{AMIN}$			150							mW
	$T_A = T_{AMAX}$			150							mW
LM741	$V_S = \pm 15V$										
	$T_A = T_{AMIN}$					60	100				mW
	$T_A = T_{AMAX}$					45	75				mW

Note 1: The maximum junction temperature of the LM741/LM741A is 150°C, while that of the LM741C/LM741E is 100°C. For operation at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W junction to ambient, or 45°C/W junction to case. The thermal resistance of the dual-in-line package is 100°C/W junction to ambient.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: Unless otherwise specified, these specifications apply for $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$ (LM741/LM741A). For the LM741C/LM741E, these specifications are limited to $0°C \le T_A \le +70°C$.

Note 4: Calculated value from: BW (MHz) = 0.35/Rise Time(μs).

LM747/LM747A/LM747C/LM747E Dual Operational Amplifiers

General Description

The LM747 series are general purpose dual operational amplifiers. The two amplifiers share a common bias network and power supply leads. Otherwise, their operation is completely independent.

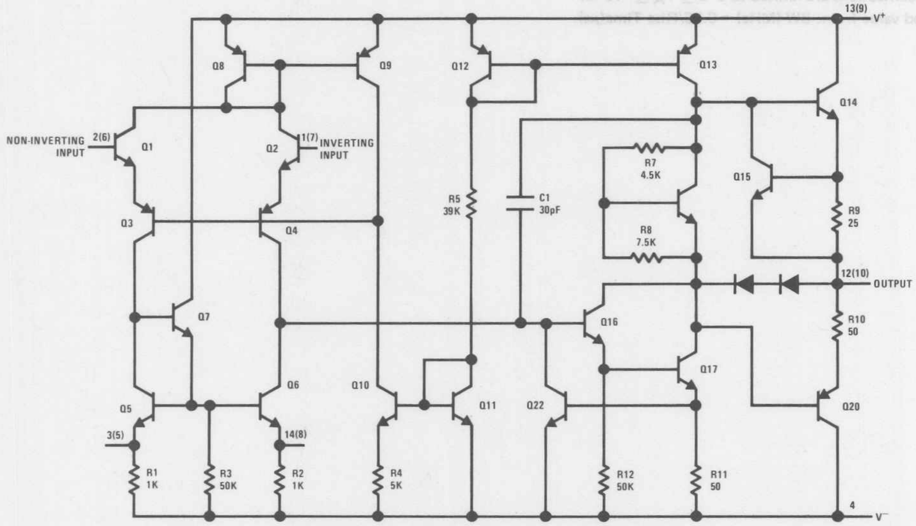
Features

- No frequency compensation required
- Short-circuit protection
- Wide common-mode and differential voltage ranges
- Low-power consumption
- No latch-up
- Balanced offset null

Additional features of the LM747 and LM747C are: no latch-up when input common mode range is exceeded, freedom from oscillations, and package flexibility.

The LM747C/LM747E is identical to the LM747/LM747A except that the LM747C/LM747E has its specifications guaranteed over the temperature range from 0°C to +70°C instead of −55°C to +125°C.

Schematic Diagram (each amplifier)



Note: Numbers in parentheses are pin numbers for amplifier B. DIP only.

Absolute Maximum Ratings

Supply Voltage LM747/LM747A	±22V
LM747C/LM747E	±18V
Power Dissipation (Note 1)	800 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
LM747/LM747A	−55°C to +125°C
LM747C/LM747E	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 3)

PARAMETER	CONDITIONS	LM747A/LM747E			LM747			LM747C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$										
	$R_S \le 10\ k\Omega$					1.0	5.0		2.0	6.0	mV
	$R_S \le 50\Omega$		0.8	3.0							mV
	$T_{AMIN} \le T_A \le T_{AMAX}$										
	$R_S \le 50\Omega$			4.0							mV
	$R_S \le 10\ k\Omega$						6.0			7.5	mV
Average Input Offset Voltage Drift				15							μV/°C
Input Offset Voltage Adjustment Range	$T_A = 25°C$, $V_S = \pm 20V$	±10				±15			±15		mV
Input Offset Current	$T_A = 25°C$		3.0	30		20	200		20	200	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			70		85	500			300	nA
Average Input Offset Current Drift				0.5							nA/°C
Input Bias Current	$T_A = 25°C$		30	80		80	500		80	500	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			0.210			1.5			0.8	μA
Input Resistance	$T_A = 25°C$, $V_S = \pm 20V$	1.0	6.0		0.3	2.0		0.3	2.0		MΩ
	$T_{AMIN} \le T_A \le T_{AMAX}$, $V_S = \pm 20V$	0.5									MΩ
Input Voltage Range	$T_A = 25°C$							±12	±13		V
	$T_{AMIN} \le T_A \le T_{AMAX}$	±12	±13		±12	±13					V
Large Signal Voltage Gain	$T_A = 25°C$, $R_L \ge 2\ k\Omega$										
	$V_S = \pm 20V$, $V_O = \pm 15V$	50									V/mV
	$V_S = \pm 15V$, $V_O = \pm 10V$				50	200		20	200		V/mV
	$T_{AMIN} \le T_A \le T_{AMAX}$, $R_L \ge 2\ k\Omega$,										
	$V_S = \pm 20V$, $V_O = \pm 15V$	32									V/mV
	$V_S = \pm 15V$, $V_O = \pm 10V$				25			15			V/mV
	$V_S = \pm 5V$, $V_O = \pm 2V$	10									V/mV
Output Voltage Swing	$V_S = \pm 20V$										
	$R_L \ge 10\ k\Omega$	±16									V
	$R_L \ge 2\ k\Omega$	±15									V
	$V_S = \pm 15V$										
	$R_L \ge 10\ k\Omega$				±12	±14		±12	±14		V
	$R_L \ge 2\ k\Omega$				±10	±13		±10	±13		V
Output Short Circuit Current	$T_A = 25°C$	10	25	35		25			25		mA
	$T_{AMIN} \le T_A \le T_{AMAX}$	10		40							mA
Common-Mode Rejection Ratio	$T_{AMIN} \le T_A \le T_{AMAX}$										
	$R_S \le 10\ k\Omega$, $V_{CM} = \pm 12V$				70	90		70	90		dB
	$R_S \le 50\ k\Omega$, $V_{CM} = \pm 12V$	80	95								dB

Electrical Characteristics (Continued)

PARAMETER	CONDITIONS	LM747A/LM747E MIN	LM747A/LM747E TYP	LM747A/LM747E MAX	LM747 MIN	LM747 TYP	LM747 MAX	LM747C MIN	LM747C TYP	LM747C MAX	UNITS
Supply Voltage Rejection Ratio	$T_{AMIN} \leq T_A \leq T_{AMAX}$, $V_S = \pm 20V$ to $V_S = \pm 5V$										
	$R_S \leq 50\Omega$	86	96								dB
	$R_S \leq 10\ k\Omega$				77	96		77	96		dB
Transient Response	$T_A = 25°C$, Unity Gain										
Rise Time			0.25	0.8		0.3			0.3		μs
Overshoot			6.0	20		5			5		%
Bandwidth (Note 4)	$T_A = 25°C$	0.437	1.5								MHz
Slew Rate	$T_A = 25°C$, Unity Gain	0.3	0.7			0.5			0.5		V/μs
Supply Current/Amp	$T_A = 25°C$			2.5		1.7	2.8		1.7	2.8	mA
Power Consumption/Amp	$T_A = 25°C$										
	$V_S = \pm 20V$		80	150							mW
	$V_S = \pm 15V$					50	85		50	85	mW
LM747A	$V_S = \pm 20V$										
	$T_A = T_{AMIN}$			165							mW
	$T_A = T_{AMAX}$			135							mW
LM747E	$V_S = \pm 20V$			150							mW
	$T_A = T_{AMIN}$			150							mW
	$T_A = T_{AMAX}$			150							mW
LM747	$V_S = \pm 15V$										
	$T_A = T_{AMIN}$					60	100				mW
	$T_A = T_{AMAX}$					45	75				mW

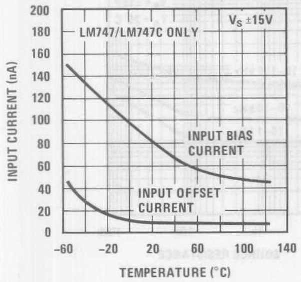
Note 1: The maximum junction temperature of the LM747/LM747A is 150°C, while that of the LM747C/LM747E is 100°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

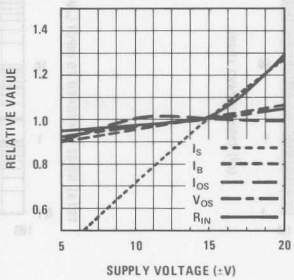
Note 3: These specifications apply for $\pm 5V \leq V_S \leq \pm 20V$ and $-55°C \leq T_A \leq 125°C$ for the LM747A and $0°C \leq T_A \leq 70°C$ for the LM747E unless otherwise specified. The LM747 and LM747C are specified for $V_S = \pm 15V$ and $-55°C \leq T_A \leq 125°C$ and $0°C \leq T_A \leq 70°C$, respectively, unless otherwise specified.

Note 4: Calculated value from: 0.35/Rise Time (μs).

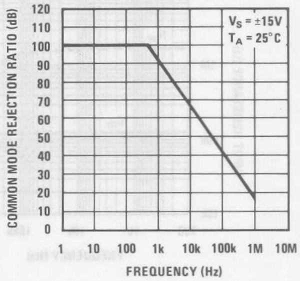
Input Bias and Offset Currents vs Ambient Temperature



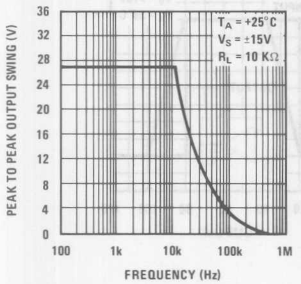
DC Parameters vs Supply Voltage



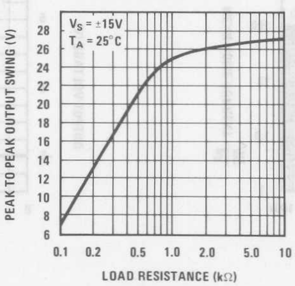
Common Mode Rejection Ratio vs Frequency



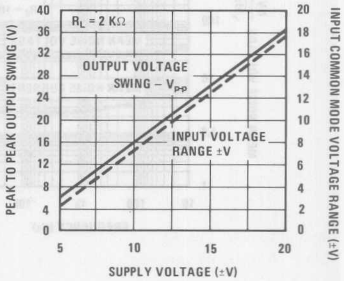
Output Voltage Swing vs Frequency



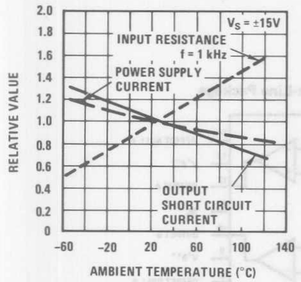
Output Voltage Swing vs Load Resistance



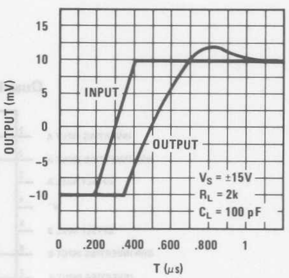
Output Swing and Input Range vs Supply Voltage



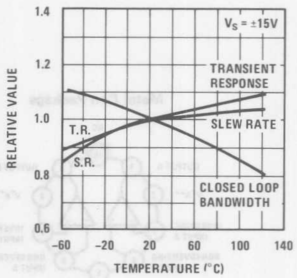
Normalized DC Parameters vs Ambient Temperature



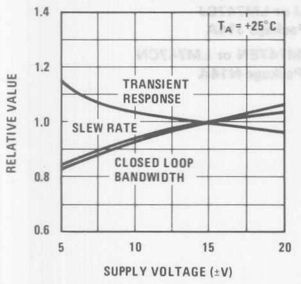
Transient Response



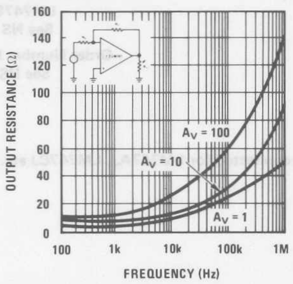
Frequency Characteristics vs Ambient Temperature



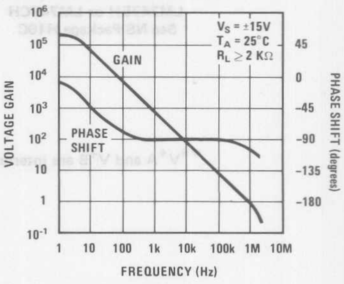
Frequency Characteristics vs Supply Voltage



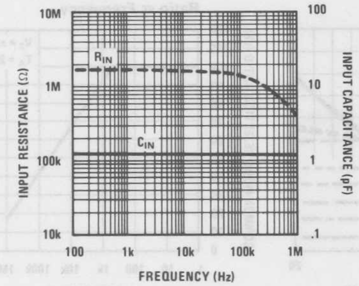
Output Resistance vs Frequency



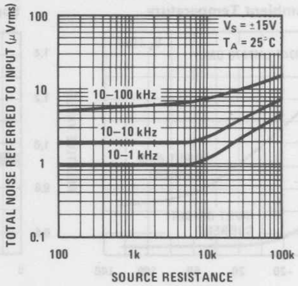
Open Loop Transfer Characteristics vs Frequency



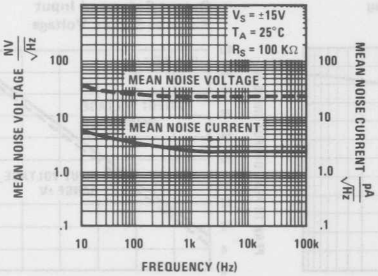
Input Resistance and Input Capacitance vs Frequency



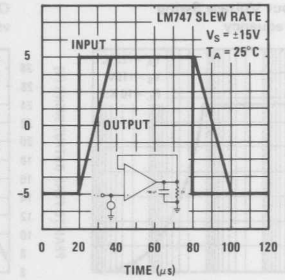
Broadband Noise for Various Bandwidths



Input Noise Voltage and Current vs Frequency

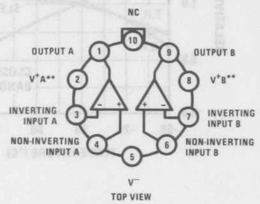


Voltage Follower Large Signal Pulse Response



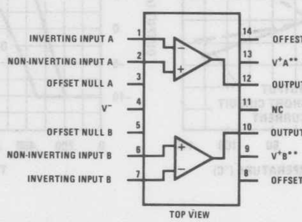
Connection Diagrams

Metal Can Package



Order Number LM747AH, LM747H, LM747EH or LM747CH
See NS Package H10C

Dual-In-Line Package



Order Number LM747AJ, LM747J, LM747EJ or LM747CJ
See NS Package J14A

Order Number LM747EN or LM747CN
See NS Package N14A

**V^+A and V^+B are internally connected for LM747AJ, LM747CJ etc.

LM748/LM748C Operational Amplifier

General Description

The LM748/LM748C is a general purpose operational amplifier built on a single silicon chip. The resulting close match and tight thermal coupling gives low offsets and temperature drift as well as fast recovery from thermal transients. In addition, the device features:

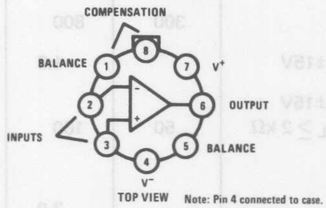
- Frequency compensation with a single 30 pF capacitor
- Operation from ±5V to ±20V
- Low current drain: 1.8 mA at ±20V
- Continuous short-circuit protection
- Operation as a comparator with differential inputs as high as ±30V
- No latch-up when common mode range is exceeded.
- Same pin configuration as the LM101.

The unity-gain compensation specified makes the circuit stable for all feedback configurations, even with capacitive loads. However, it is possible to optimize compensation for best high frequency performance at any gain. As a comparator, the output can be clamped at any desired level to make it compatible with logic circuits.

The LM748 is specified for operation over the −55°C to +125°C military temperature range. The LM748C is specified for operation over the 0°C to +70°C temperature range.

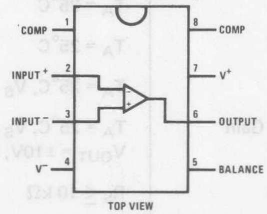
Connection Diagrams

Metal Can Package



Order Number LM748H or LM748CH
See NS Package H08C

Dual-In-Line Package

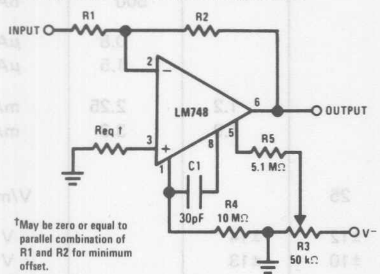


Order Number LM748CN
See NS Package N08B

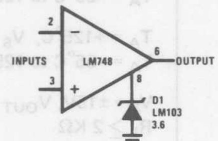
Order Number LM748J or LM748CJ
See NS Package J08A

Typical Applications

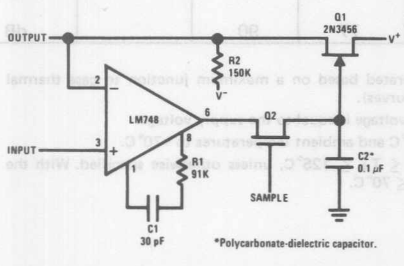
Inverting Amplifier with Balancing Circuit



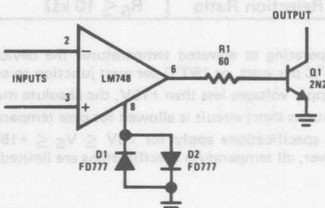
Voltage Comparator for Driving DTL or TTL Integrated Circuits



Low Drift Sample and Hold



Voltage Comparator for Driving RTL Logic or High Current Driver



Absolute Maximum Ratings

Supply Voltage	±22V
Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short-Circuit Duration (Note 3)	Indefinite
Operating Temperature Range: LM748	-55°C to +125°C
LM748C	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics (Note 4)

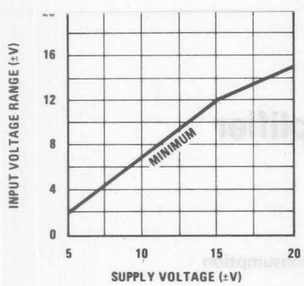
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 10\ k\Omega$		1.0	5.0	mV
Input Offset Current	$T_A = 25°C$		40	200	nA
Input Bias Current	$T_A = 25°C$		120	500	nA
Input Resistance	$T_A = 25°C$	300	800		kΩ
Supply Current	$T_A = 25°C$, $V_S = \pm 15V$		1.8	2.8	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2\ k\Omega$	50	160		V/mV
Input Offset Voltage	$R_S \leq 10\ k\Omega$			6.0	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 50\Omega$		3.0		μV/°C
	$R_S \leq 10\ k\Omega$		6.0		μV/°C
Input Offset Current	$T_A = 0°C$ to $70°C$			300	nA
	$T_A = -55°C$ to $125°C$			500	nA
Input Bias Current	$T_A = 0°C$ to $70°C$			0.8	μA
	$T_A = -55°C$ to $125°C$			1.5	μA
Supply Current	$T_A = +125°C$, $V_S = \pm 15V$		1.2	2.25	mA
	$T_A = -55°C$ to $125°C$		1.9	3.3	mA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2\ K\Omega$	25			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\Omega$	±12	±14		V
	$R_L = 2\ k\Omega$	±10	±13		V
Input Voltage Range	$V_S = \pm 15V$	±12			V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$	77	90		dB

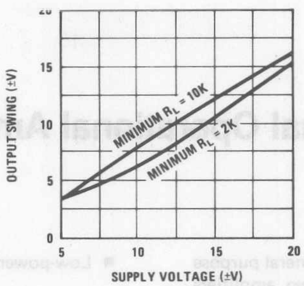
Note 1: For operating at elevated temperatures the devices must be derated based on a maximum junction to case thermal resistance of 45°C per watt, or 150°C per watt junction to ambient. (See Curves).

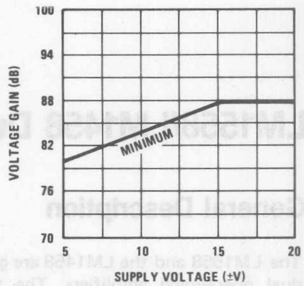
Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: Continuous short circuit is allowed for case temperatures to +125°C and ambient temperatures to +70°C.

Note 4: These specifications apply for $\pm 5V \leq V_S \leq +15V$ and $-55°C \leq T_A \leq 125°C$, unless otherwise specified. With the LM748C, however, all temperature specifications are limited to $0°C \leq T_A \leq 70°C$.

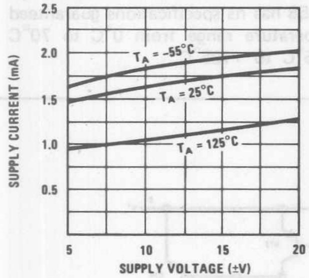




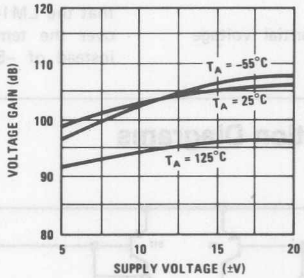


Typical Performance Characteristics

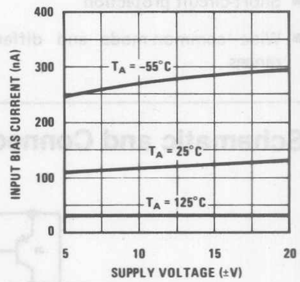
Supply Current



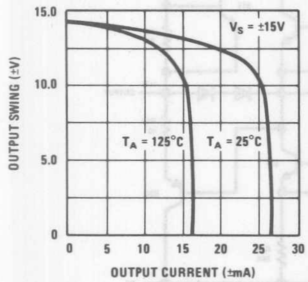
Voltage Gain



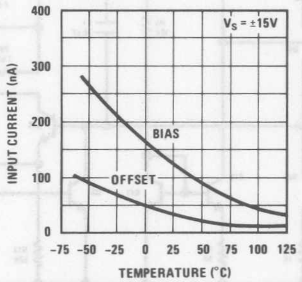
Input Bias Current



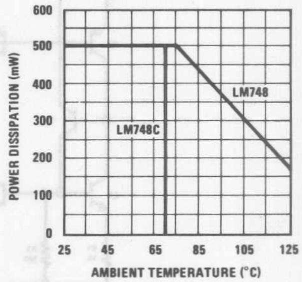
Current Limiting



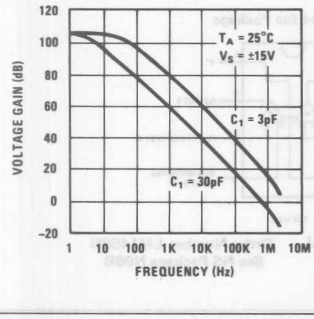
Input Current



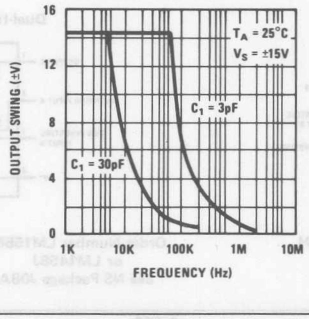
Maximum Power Dissipation



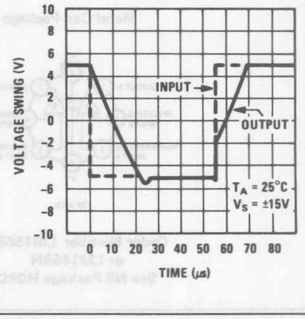
Open Loop Frequency Response



Large Signal Frequency Response



Voltage Follower Pulse Response



National Semiconductor

LM1558/LM1458 Dual Operational Amplifier

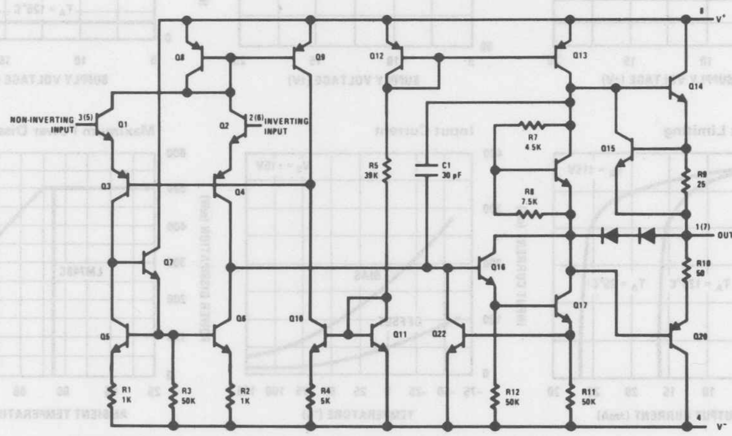
General Description

The LM1558 and the LM1458 are general purpose dual operational amplifiers. The two amplifiers share a common bias network and power supply leads. Otherwise, their operation is completely independent. Features include:

- No frequency compensation required
- Short-circuit protection
- Wide common-mode and differential voltage ranges
- Low-power consumption
- 8-lead TO-5 and 8-lead mini DIP
- No latch up when input common mode range is exceeded

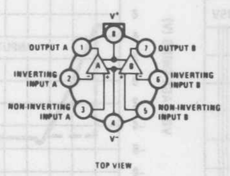
The LM1458 is identical to the LM1558 except that the LM1458 has its specifications guaranteed over the temperature range from 0°C to 70°C instead of −55°C to +125°C.

Schematic and Connection Diagrams



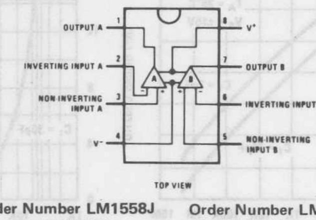
Note: Numbers in parentheses are pin numbers for amplifier B.

Metal Can Package



Order Number LM1558H or LM1458H
See NS Package H08C

Dual-In-Line Package



Order Number LM1558J or LM1458J
See NS Package J08A

Order Number LM1458N
See NS Package N08B

Absolute Maximum Ratings

Supply Voltage LM1558	±22V	Output Short-Circuit Duration	Indefinite
LM1458	±18V	Operating Temperature Range LM1558	−55°C to 125°C
Power Dissipation (Note 1) LM1558H/LM1458H	500 mW	LM1458	0°C to 70°C
LM1458N	400 mW	Storage Temperature Range	−65°C to 150°C
Differential Input Voltage	±30V	Lead Temperature (Soldering, 10 sec)	300°C
Input Voltage (Note 2)	±15V		

Electrical Characteristics (Note 3)

PARAMETER	CONDITIONS	LM1558			LM1458			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 10\ k\Omega$		1.0	5.0		1.0	6.0	mV
Input Offset Current	$T_A = 25°C$		80	200		80	200	nA
Input Bias Current	$T_A = 25°C$		200	500		200	500	nA
Input Resistance	$T_A = 25°C$	0.3	1.0		0.3	1.0		MΩ
Supply Current Both Amplifiers	$T_A = 25°C$, $V_S = \pm 15V$		3.0	5.0		3.0	5.6	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2\ k\Omega$	50	160		20	160		V/mV
Input Offset Voltage	$R_S \leq 10\ k\Omega$			6.0			7.5	mV
Input Offset Current				500			300	nA
Input Bias Current				1.5			0.8	μA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2\ k\Omega$	25			15			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$	±12	±14		±12	±14		V
	$R_L = 2\ k\Omega$	±10	±13		±10	±13		V
Input Voltage Range	$V_S = \pm 15V$	±12			±12			V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$	77	96		77	96		dB

Note 1: The maximum junction temperature of the LM1558 is 150°C, while that of the LM1458 is 100°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient or 45°C/W, junction to case. For the DIP the device must be derated based on a thermal resistance of 187°C/W, junction to ambient.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: These specifications apply for $V_S = \pm 15V$ and $-55°C \leq T_A \leq 125°C$, unless otherwise specified. With the LM1458, however, all specifications are limited to $0°C \leq T_A \leq 70°C$ and $V_S = \pm 15V$.

LM2900/LM3900, LM3301, LM3401 Quad Amplifiers

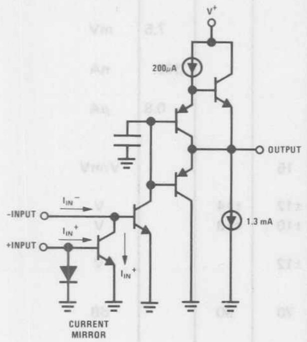
General Description

The LM2900 series consists of four independent, dual input, internally compensated amplifiers which were designed specifically to operate off of a single power supply voltage and to provide a large output voltage swing. These amplifiers make use of a current mirror to achieve the non-inverting input function. Application areas include: ac amplifiers, RC active filters, low frequency triangle, squarewave and pulse waveform generation circuits, tachometers and low speed, high voltage digital logic gates.

Features

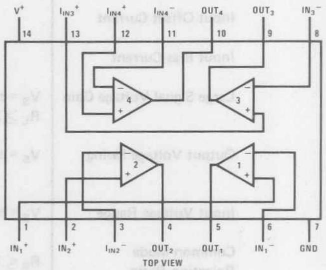
- Wide single supply voltage range or dual supplies — $4\ V_{DC}$ to $36\ V_{DC}$; $\pm 2\ V_{DC}$ to $\pm 18\ V_{DC}$
- Supply current drain independent of supply voltage
- Low input biasing current — 30 nA
- High open-loop gain — 70 dB
- Wide bandwidth — 2.5 MHz (Unity Gain)
- Large output voltage swing — $(V^+ -1)$ Vp-p
- Internally frequency compensated for unity gain
- Output short-circuit protection

Schematic and Connection Diagrams

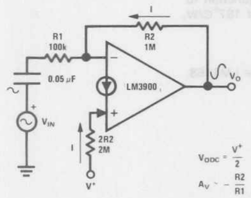


Order Number LM2900J
See NS Package J14A
Order Number LM2900N, LM3900N, LM3301N or LM3401N
See NS Package N14A

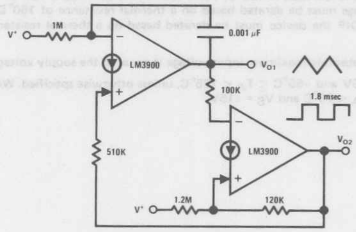
Dual-In-Line and Flat Package



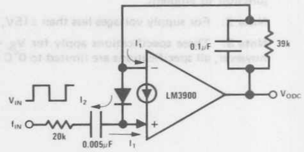
Typical Applications $(V^+ = 15\ V_{DC})$



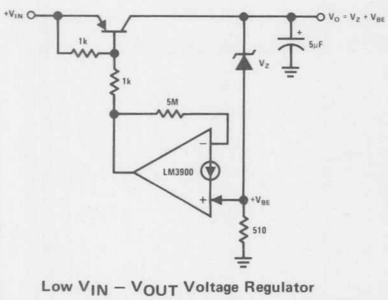
Inverting Amplifier



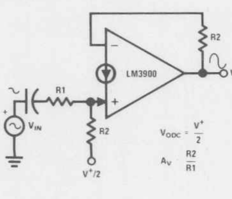
Triangle/Square Generator



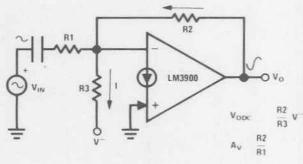
Frequency-Doubling Tachometer



Low $V_{IN} - V_{OUT}$ Voltage Regulator



Non-Inverting Amplifier



Negative Supply Biasing

Absolute Maximum Ratings

	LM2900/LM3900	LM3301	LM3401
Supply Voltage	32 V_{DC}	28 V_{DC}	18 V_{DC}
	±16 V_{DC}	±14 V_{DC}	±9 V_{DC}
Power Dissipation (T_A = 25°C) (Note 1)			
Cavity DIP	900 mW		
Flat Pack	800 mW		
Molded DIP	570 mW	570 mW	570 mW
Input Currents, I_{IN}^+ or I_{IN}^-	20 mA_{DC}	20 mA_{DC}	20 mA_{DC}
Output Short-Circuit Duration – One Amplifier	Continuous	Continuous	Continuous
T_A = 25°C (See Application Hints)			
Operating Temperature Range		−40°C to +85°C	0°C to +75°C
LM2900	−40°C to +85°C		
LM3900	0°C to +70°C		
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	300°C

Electrical Characteristics (Note 6)

PARAMETER	CONDITIONS	LM2900			LM3900			LM3301			LM3401		
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
Open Loop													
Voltage Gain											800		
Voltage Gain	T_A = 25°C, f = 100 Hz	1.2	2.8		1.2	2.8		1.2	2.8		1.2	2.8	
Input Resistance	T_A = 25°C, Inverting Input		1			1			1		0.1	1	
Output Resistance			8			8			8			8	
Unity Gain Bandwidth	T_A = 25°C, Inverting Input		2.5			2.5			2.5			2.5	
Input Bias Current	T_A = 25°C, Inverting Input		30	200		30	200		30	300		30	300
	Inverting Input												500
Slew Rate	T_A = 25°C, Positive Output Swing		0.5			0.5			0.5			0.5	
	T_A = 25°C, Negative Output Swing		20			20			20			20	
Supply Current	T_A = 25°C, R_L = ∞ On All Amplifiers		6.2	10		6.2	10		6.2	10		6.2	10
Output Voltage Swing	T_A = 25°C, R_L = 2k, V_{CC} = 15.0 V_{DC}												
V_{OUT} High	I_{IN}^- = 0, I_{IN}^+ = 0	13.5			13.5			13.5			13.5		
V_{OUT} Low	I_{IN}^- = 10μA, I_{IN}^+ = 0		0.09	0.2		0.09	0.2		0.09	0.2		0.09	0.2
V_{OUT} High	I_{IN}^- = 0, I_{IN}^+ = 0 R_L = ∞, V_{CC} = Absolute Maximum Ratings		29.5			29.5			25.5			15.5	
Output Current Capability	T_A = 25°C												
Source		6	18		6	10		5	18		5	10	
Sink	(Note 2)	0.5	1.3		0.5	1.3		0.5	1.3		0.5	1.3	
I_{SINK}	V_{OL} = 1V, I_{IN} = 5μA		5			5			5			5	

Electrical Characteristics (Continued) (Note 6)

PARAMETER	CONDITIONS	LM2900			LM3900			LM3301			LM3401			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Power Supply Rejection	$T_A = 25°C$, f = 100 Hz		70			70			70			70		dB
Mirror Gain	@ 20μA (Note 3)	0.90	1.0	1.1	0.90	1.0	1.1	0.90	1	1.10	0.90	1	1.10	μA/μA
	@ 200μA (Note 3)	0.90	1.0	1.1	0.90	1.0	1.1	0.90	1	1.10	0.90	1	1.10	μA/μA
ΔMirror Gain	@ 20μA To 200μA (Note 3)		2	5		2	5		2	5		2	5	%
Mirror Current	(Note 4)		10	500		10	500		10	500		10	500	μA_{DC}
Negative Input Current	$T_A = 25°C$ (Note 5)		1.0			1.0			1.0			1.0		mA_{DC}
Input Bias Current	Inverting Input		300			300								nA

Note 1: For operating at high temperatures, the device must be derated based on a 125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient.

Note 2: The output current sink capability can be increased for large signal conditions by overdriving the inverting input. This is shown in the section on Typical Characteristics.

Note 3: This spec indicates the current gain of the current mirror which is used as the non-inverting input.

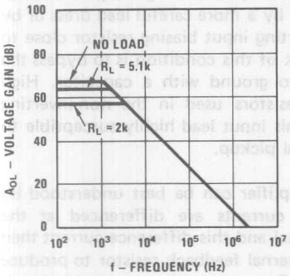
Note 4: Input V_{BE} match between the non-inverting and the inverting inputs occurs for a mirror current (non-inverting input current) of approximately 10μA. This is therefore a typical design center for many of the application circuits.

Note 5: Clamp transistors are included on the IC to prevent the input voltages from swinging below ground more than approximately −0.3 V_{DS}. The negative input currents which may result from large signal overdrive with capacitance input coupling need to be externally limited to values of approximately 1 mA. Negative input currents in excess of 4 mA will cause the output voltage to drop to a low voltage. This maximum current applies to any one of the input terminals. If more than one of the input terminals are simultaneously driven negative smaller maximum currents are allowed. Common-mode current biasing can be used to prevent negative input voltages; see for example, the "Differentiator Circuit" in the applications section.

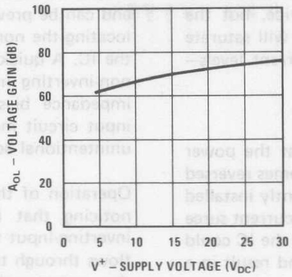
Note 6: These specs apply for $-55°C \leq T_A \leq +125°C$, unless otherwise stated.

Typical Performance Characteristics

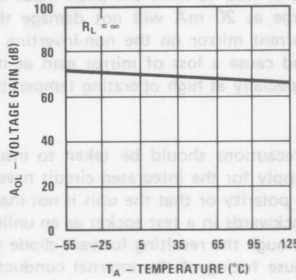
Open Loop Gain



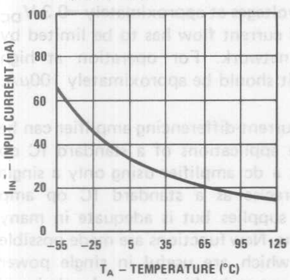
Voltage Gain



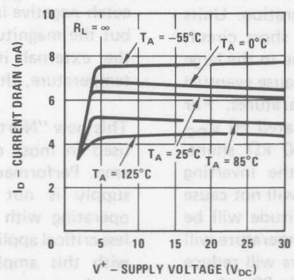
Voltage Gain



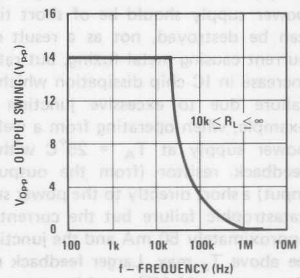
Input Current



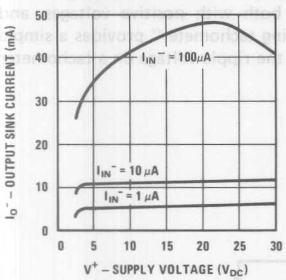
Supply Current



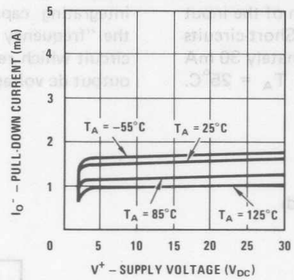
Large Signal Frequency Response



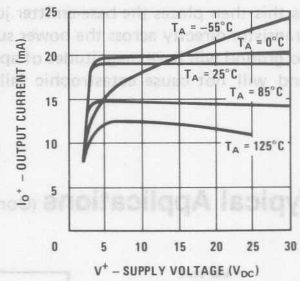
Output Sink Current



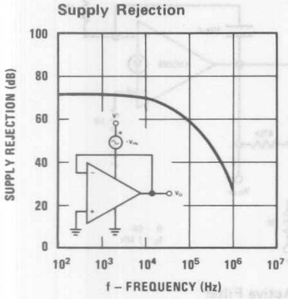
Output Class-A Bias Current



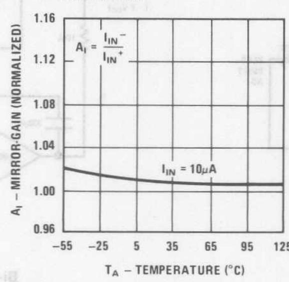
Output Source Current



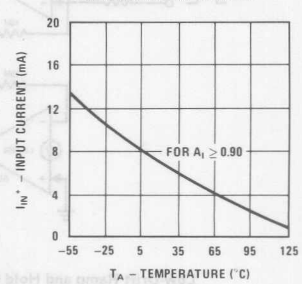
Supply Rejection



Mirror Gain



Maximum Mirror Current



input lead to limit the peak input current. Currents as large as 20 mA will not damage the device, but the current mirror on the non-inverting input will saturate and cause a loss of mirror gain at mA current levels—especially at high operating temperatures.

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fuzing of the internal conductors and result in a destroyed unit.

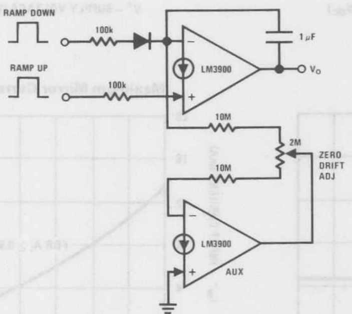
Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fuzing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. For example, when operating from a well-regulated +5 V_{DC} power supply at T_A = 25°C with a 100 kΩ shunt-feedback resistor (from the output to the inverting input) a short directly to the power supply will not cause catastrophic failure but the current magnitude will be approximately 50 mA and the junction temperature will be above T_J max. Larger feedback resistors will reduce the current, 11 MΩ provides approximately 30 mA, an open circuit provides 1.3 mA, and a direct connection from the output to the non-inverting input will result in catastrophic failure when the output is shorted to V^+ as this then places the base-emitter junction of the input transistor directly across the power supply. Short-circuits to ground will have magnitudes of approximately 30 mA and will not cause catastrophic failure at T_A = 25°C.

non-inverting input can cause oscillations. This is likely only in breadboard hook-ups with long component leads and can be prevented by a more careful lead dress or by locating the non-inverting input biasing resistor close to the IC. A quick check of this condition is to bypass the non-inverting input to ground with a capacitor. High impedance biasing resistors used in the non-inverting input circuit make this input lead highly susceptible to unintentional ac signal pickup.

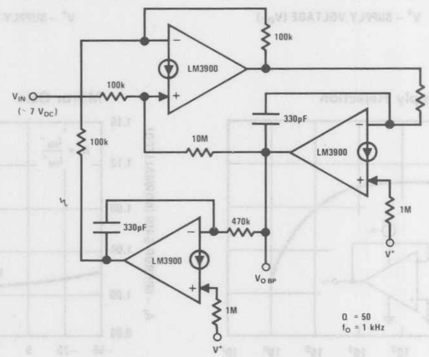
Operation of this amplifier can be best understood by noticing that input currents are differenced at the inverting-input terminal and this difference current then flows through the external feedback resistor to produce the output voltage. Common-mode current biasing is generally useful to allow operating with signal levels near ground or even negative as this maintains the inputs biased at $+V_{BE}$. Internal clamp transistors (see note 5) catch negative input voltages at approximately −0.3 V_{DC} but the magnitude of current flow has to be limited by the external input network. For operation at high temperature, this limit should be approximately 100μA.

This new "Norton" current-differencing amplifier can be used in most of the applications of a standard IC op amp. Performance as a dc amplifier using only a single supply is not as precise as a standard IC op amp operating with split supplies but is adequate in many less critical applications. New functions are made possible with this amplifier which are useful in single power supply systems. For example, biasing can be designed separately from the ac gain as was shown in the "inverting amplifier," the "difference integrator" allows controlling the charging and the discharging of the integrating capacitor both with positive voltages, and the "frequency doubling tachometer" provides a simple circuit which reduces the ripple voltage on a tachometer output dc voltage.

Typical Applications (Continued)

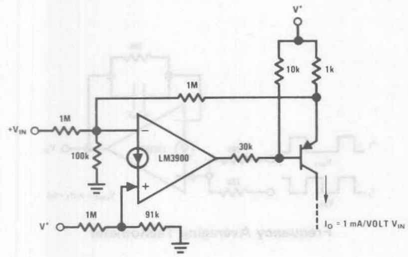


Low-Drift Ramp and Hold Circuit

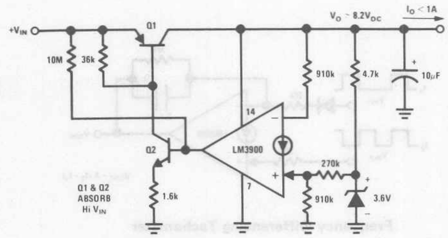


Bi-Quad Active Filter (2nd Degree State-Variable Network)

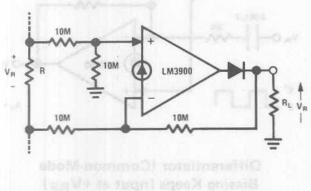
Typical Applications (Continued)



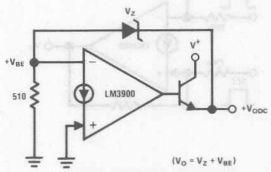
Voltage-Controlled Current Source
(Transconductance Amplifier)



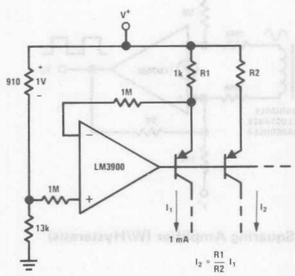
Hi V_{IN}, Lo ($V_{IN} - V_O$) Self-Regulator



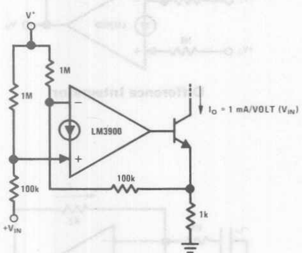
Ground-Referencing a
Differential Input Signal



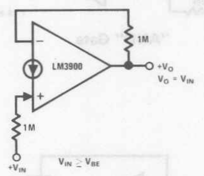
Voltage Regulator



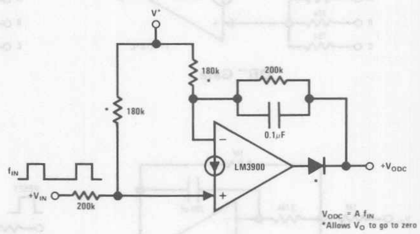
Fixed Current Sources



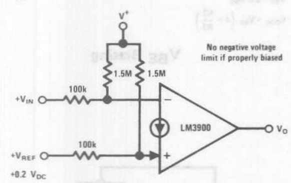
Voltage-Controlled Current Sink
(Transconductance Amplifier)



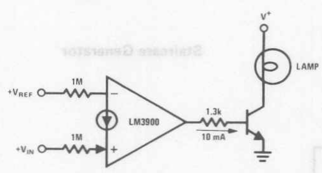
Buffer Amplifier



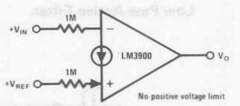
Tachometer



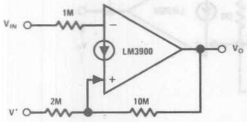
Low-Voltage Comparator



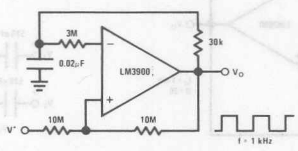
Power Comparator



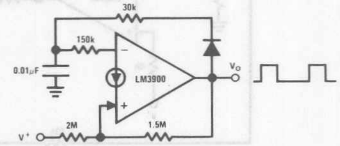
Comparator



Schmitt-Trigger

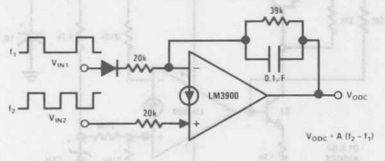


Square-Wave Oscillator

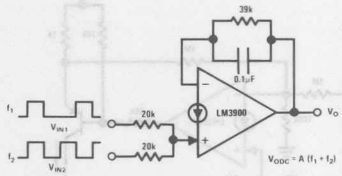


Pulse Generator

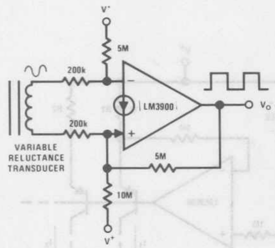
Typical Applications (Continued)



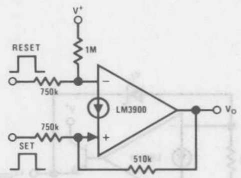
Frequency Differencing Tachometer



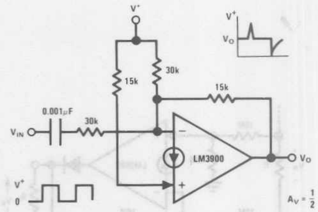
Frequency Averaging Tachometer



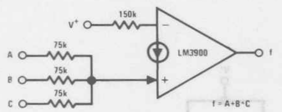
Squaring Amplifier (W/Hysteresis)



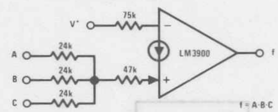
Bi-Stable Multivibrator



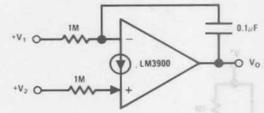
Differentiator (Common-Mode Biasing Keeps Input at $+V_{BE}$)



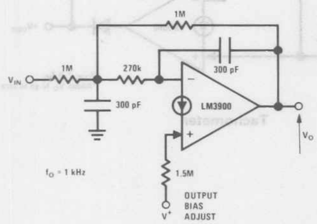
"OR" Gate



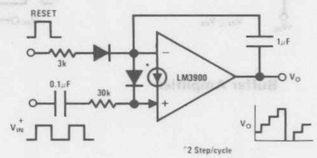
"AND" Gate



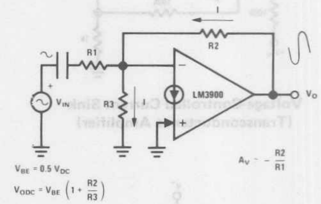
Difference Integrator



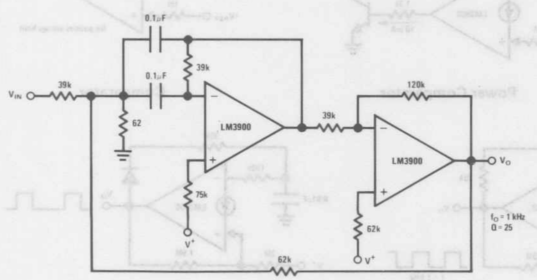
Low Pass Active Filter



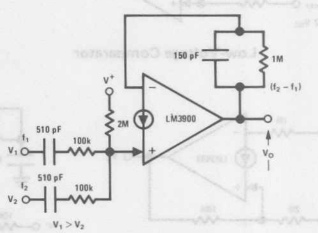
Staircase Generator



V_{BE} Biasing

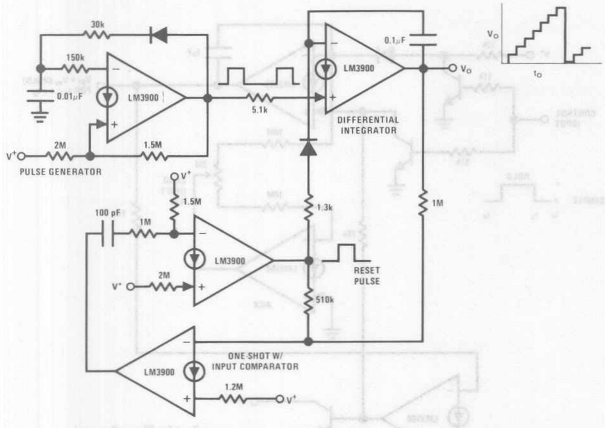


Bandpass Active Filter

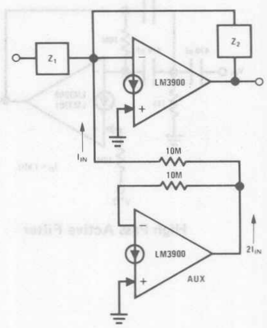


Low-Frequency Mixer

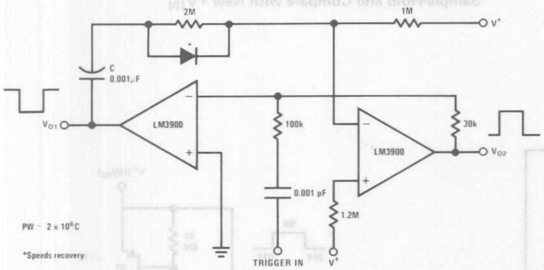
Typical Applications (Continued)



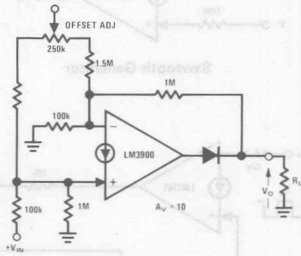
Free-Running Staircase Generator/Pulse Counter



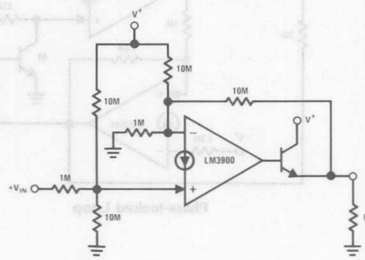
Supplying I_{IN} with Aux. Amp (to Allow Hi-Z Feedback Networks)



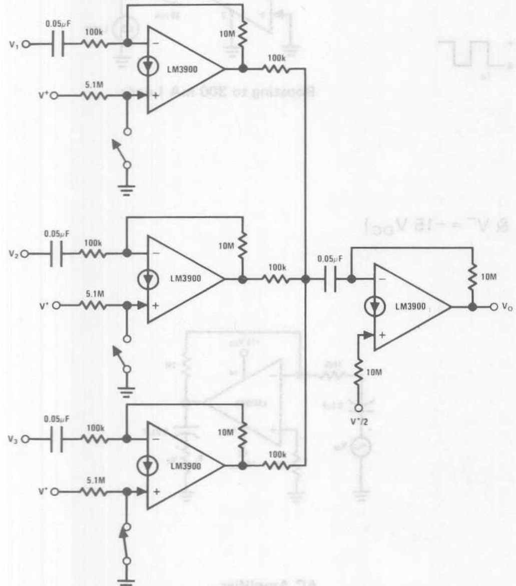
One-Shot Multivibrator



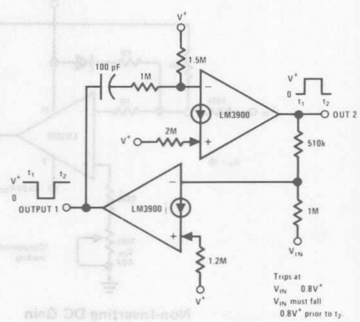
Non-Inverting DC Gain to (0,0)



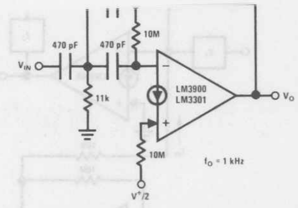
Power Amplifier



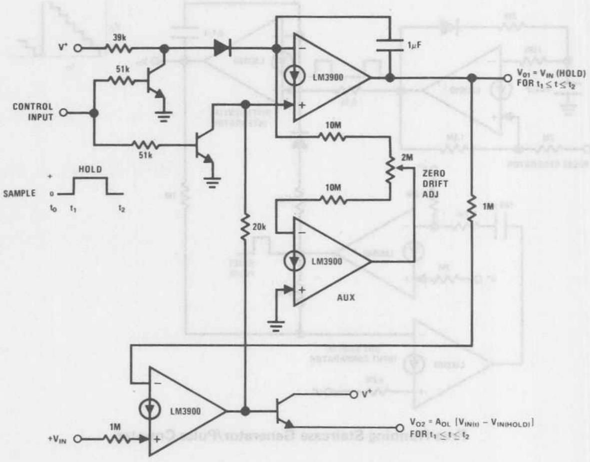
Channel Selection by DC Control (or Audio Mixer)



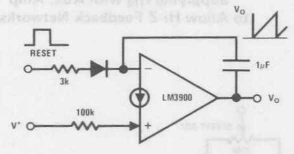
One-Shot with DC Input Comparator



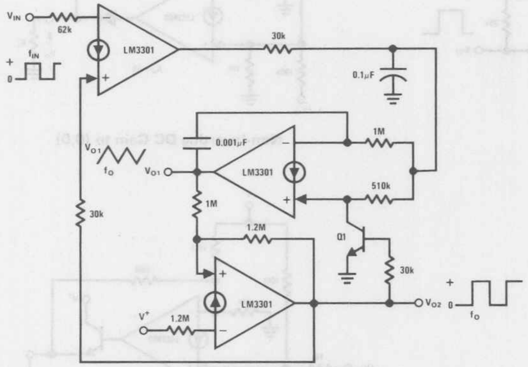
High Pass Active Filter



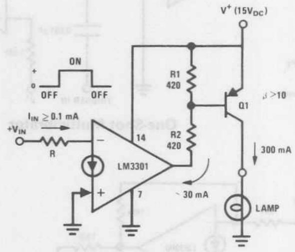
Sample-Hold and Compare with New $+V_{IN}$



Sawtooth Generator

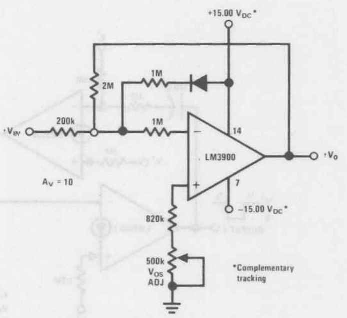


Phase-locked Loop

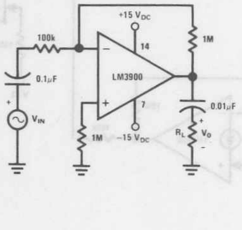


Boosting to 300 mA Loads

Split-Supply Applications ($V^+ = +15\ V_{DC}$ & $V^- = -15\ V_{DC}$)



Non-Inverting DC Gain



AC Amplifier

National Semiconductor

Operational Amplifiers/Buffers

LM4250/LM4250C Programmable Operational Amplifier

General Description

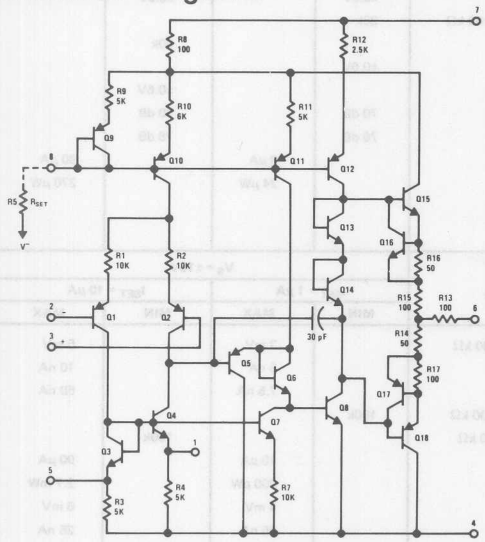
The LM4250 and LM4250C are extremely versatile programmable monolithic operational amplifiers. A single external master bias current setting resistor programs the input bias current, input offset current, quiescent power consumption, slew rate, input noise, and the gain-bandwidth product. The device is a truly general purpose operational amplifier.

Features

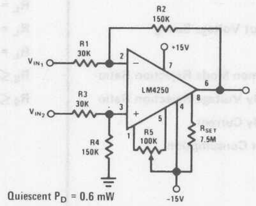
- ±1V to ±18V power supply operation
- 3 nA input offset current
- Standby power consumption as low as 500 nW
- No frequency compensation required
- Programmable electrical characteristics
- Offset Voltage nulling capability
- Can be powered by two flashlight batteries
- Short circuit protection

The LM4250C is identical to the LM4250 except that the LM4250C has its performance guaranteed over a 0°C to 70°C temperature range instead of the −55°C to +125°C temperature range of the LM4250.

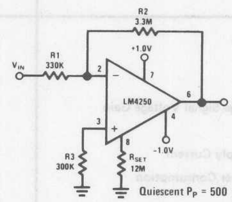
Schematic Diagrams



Typical Applications



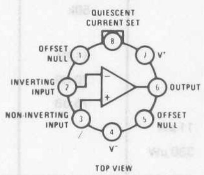
X5 Difference Amplifier



500 Nano-Watt X10 Amplifier

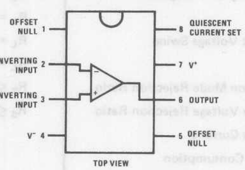
Connection Diagrams

Metal Can Package



Order Number LM4250H or LM4250CH
See NS Package H08C

Dual-In-Line Package



Order Number LM4250CN
See NS Package N08B
Order Number LM4250J
or LM4250CJ
See NS Package J08A

Absolute Maximum Ratings

Supply Voltage	±18V	Output Short-Circuit Duration		Indefinite
Power Dissipation (Note 1)	500 mW	Operating Temperature Range	LM4250	$-55^\circ C \leq T_A \leq 125^\circ C$
Differential Input Voltage	±30V		LM4250C	$0^\circ C \leq T_A \leq 70^\circ C$
Input Voltage (Note 2)	±15V	Storage Temperature Range		$-65^\circ C$ to $150^\circ C$
I_{SET} Current	150 µA	Lead Temperature (Soldering, 10 sec)		300°C

Electrical Characteristics LM4250 ($-55^\circ C \leq T_A \leq 125^\circ C$ unless otherwise specified)

PARAMETERS	CONDITIONS	$V_S = \pm 1.5V$, $I_{SET} = 1\ \mu A$ MIN	$I_{SET} = 1\ \mu A$ MAX	$I_{SET} = 10\ \mu A$ MIN	$I_{SET} = 10\ \mu A$ MAX
V_{OS}	$T_A = 25^\circ$ $R_S \leq 100\ k\Omega$		3 mV		5 mV
I_{OS}	$T_A = 25^\circ$		3 nA		10 nA
I_{bias}	$T_A = 25^\circ$		7.5 nA		50 nA
Large Signal Voltage Gain	$T_A = 25^\circ$ $R_L = 100\ k\Omega$	40k			
	$V_O = \pm 0.6$, $R_L = 10\ k\Omega$			50k	
Supply Current	$T_A = 25^\circ C$		7.5 µA		80 µA
Power Consumption	$T_A = 25^\circ C$		23 µW		240 µW
V_{OS}	$R_S \leq 100\ k\Omega$		4 mV		6 mV
I_{OS}	$T_A = 125^\circ C$		5 nA		10 nA
	$T_A = -55^\circ C$		3 nA		10 nA
I_{bias}			7.5 nA		50 nA
Input Voltage Range		±0.6V		±0.6V	
Large Signal Voltage Gain	$V_O = \pm 0.5V$, $R_L = 100\ k\Omega$	30k			
	$R_L = 10\ k\Omega$			30k	
Output Voltage Swing	$R_L = 100\ k\Omega$	±0.6V			
	$R_L = 10\ k\Omega$			±0.6V	
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70 dB		70 dB	
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$	76 dB		76 dB	
Supply Current			8 µA		90 µA
Power Consumption			24 µW		270 µW

PARAMETERS	CONDITIONS	$V_S = \pm 15V$, $I_{SET} = 1\ \mu A$ MIN	$I_{SET} = 1\ \mu A$ MAX	$I_{SET} = 10\ \mu A$ MIN	$I_{SET} = 10\ \mu A$ MAX
V_{OS}	$T_A = 25^\circ C$ $R_S \leq 100\ k\Omega$		3 mV		5 mV
I_{OS}	$T_A = 25^\circ C$		3 nA		10 nA
I_{bias}	$T_A = 25^\circ C$		7.5 nA		50 nA
Large Signal Voltage Gain	$T_A = 25^\circ C$ $R_L = 100\ k\Omega$	100k			
	$V_O = \pm 10V$ $R_L = 10\ k\Omega$			100k	
Supply Current	$T_A = 25^\circ C$		10 µA		90 µA
Power Consumption	$T_A = 25^\circ C$		300 µW		2.7 mW
V_{OS}	$R_S \leq 100\ k\Omega$		4 mV		6 mV
I_{OS}	$T_A = 125^\circ C$		25 nA		25 nA
	$T_A = -55^\circ C$		3 nA		10 nA
I_{bias}			7.5 nA		50 nA
Input Voltage Range		±13.5V		±13.5V	
Large Signal Voltage Gain	$V_O = \pm 10V$ $R_L = 100\ k\Omega$	50k			
	$R_L = 10\ k\Omega$			50k	
Output Voltage Swing	$R_L = 100\ k\Omega$	±12V			
	$R_L = 10\ k\Omega$			±12V	
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70 dB		70 dB	
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$	76 dB		76 dB	
Supply Current			11 µA		100 µA
Power Consumption			330 µW		3 mW

Note 1: The maximum junction temperature of the LM4250 is 150°C, while that of the LM4250C is 100°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W junction to ambient, or 45°C/W junction to case. The thermal resistance of the dual-in-line package is 125°C/W.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Electrical Characteristics LM4250C ($0^\circ C \leq T_A \leq 70^\circ C$ unless otherwise specified)

PARAMETERS	CONDITIONS	$V_S = \pm 1.5V$			
		$I_{SET} = 1\ \mu A$		$I_{SET} = 10\ \mu A$	
		MIN	MAX	MIN	MAX
V_{OS}	$T_A = 25^\circ C$ $R_S \leq 100\ k\Omega$		5 mV		6 mV
I_{OS}	$T_A = 25^\circ C$		6 nA		20 nA
I_{bias}	$T_A = 25^\circ C$		10 nA		75 nA
Large Signal Voltage Gain	$T_A = 25^\circ C$ $R_L = 100\ k\Omega$	25k			
	$V_O = \pm 0.6V$ $R_L = 10\ k\Omega$			25k	
Supply Current	$T_A = 25^\circ C$		8 μA		90 μA
Power Consumption	$T_A = 25^\circ C$		24 μW		270 μW
V_{OS}	$R_S \leq 10\ k\Omega$		6.5 mV		7.5 mV
I_{OS}			8 nA		25 nA
I_{bias}			10 nA		80 nA
Input Voltage Range		±0.6V		±0.6V	
Large Signal Voltage Gain	$V_O = \pm 0.5V$, $R_L = 100\ k\Omega$	25k			
	$R_L = 10\ k\Omega$			25k	
Output Voltage Swing	$R_L = 100\ k\Omega$	±0.6V			
	$R_L = 10\ k\Omega$			±0.6V	
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70 dB		70 dB	
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$	74 dB		74 dB	
Supply Current			8 μA		90 uA
Power Consumption			24 μW		270 uW

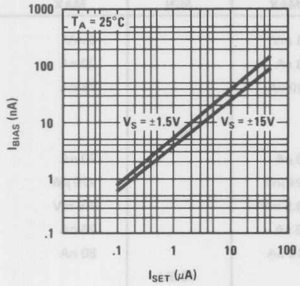
PARAMETERS	CONDITIONS	$V_S = \pm 15V$			
		$I_{SET} = 1\ \mu A$		$I_{SET} = 10\ \mu A$	
		MIN	MAX	MIN	MAX
V_{OS}	$T_A = 25^\circ C$ $R_S \leq 100\ k\Omega$		5 mV		6 mV
I_{OS}	$T_A = 25^\circ C$		6 nA		20 nA
I_{bias}	$T_A = 25^\circ C$		10 nA		75 nA
Large Signal Voltage Gain	$T_A = 25^\circ C$ $R_L = 100\ k\Omega$	60k			
	$V_O = \pm 10V$ $R_L = 10\ k\Omega$			60k	
Supply Current	$T_A = 25^\circ C$		11 μA		100 μA
Power Consumption	$T_A = 25^\circ C$		330 μW		3 mW
V_{OS}	$R_S \leq 10\ k\Omega$		6.5 mV		7.5 mV
I_{OS}			8 nA		25 nA
I_{bias}			10 nA		80 nA
Input Voltage Range		±13.5V		±13.5V	
Large Signal Voltage Gain	$V_O = \pm 10V$ $R_L = 100\ k\Omega$	50k			
	$R_L = 10\ k\Omega$			50k	
Output Voltage Swing	$R_L = 100\ k\Omega$	±12V			
	$R_L = 10\ k\Omega$			±12V	
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70 dB		70 dB	
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$	74 dB		74 dB	
Supply Current			11 uA		100 uA
Power Consumption			300 uW		3 mW

Resistor Biasing

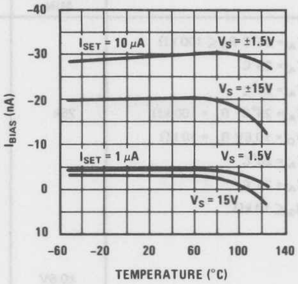
Set Current Setting Resistor to V^-

V_S	I_{SET}				
	0.1 μA	0.5 μA	1.0 μA	5 μA	10 μA
±1.5V	25.6 MΩ	5.04 MΩ	2.5 MΩ	492 kΩ	244 kΩ
±3.0V	55.6 MΩ	11.0 MΩ	5.5 MΩ	1.09 MΩ	544 kΩ
±6.0V	116 MΩ	23.0 MΩ	11.5 MΩ	2.29 MΩ	1.14 MΩ
±9.0V	176 MΩ	35.0 MΩ	17.5 MΩ	3.49 MΩ	1.74 MΩ
±12.0V	236 MΩ	47.0 MΩ	23.5 MΩ	4.69 MΩ	2.34 MΩ
±15.0V	296 MΩ	59.0 MΩ	29.5 MΩ	5.89 MΩ	2.94 MΩ

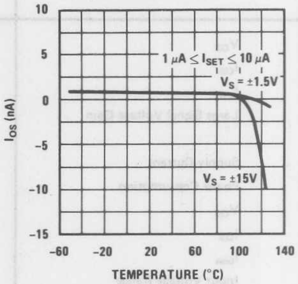
Input Bias Current vs I_{SET}



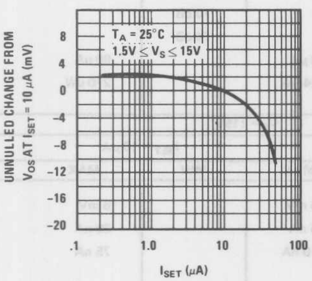
Input Bias Current vs Temperature



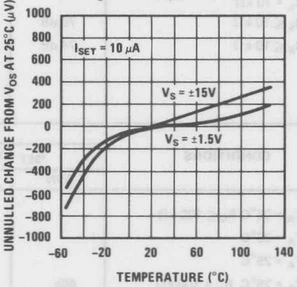
Input Offset Current vs Temperature



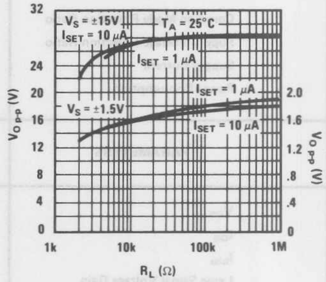
Unnulled Input Offset Voltage Change vs I_{SET}



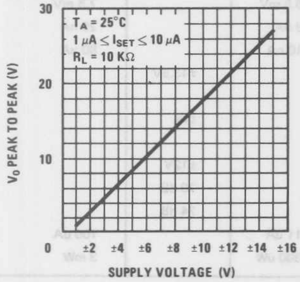
Unnulled Input Offset Voltage Change vs Temperature



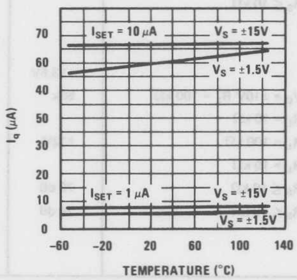
Peak to Peak Output Voltage Swing vs Load Resistance



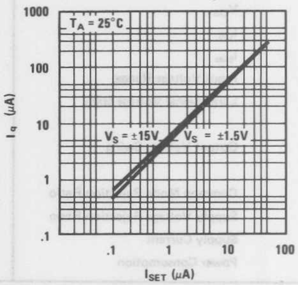
Peak to Peak Output Voltage Swing vs Supply Voltage



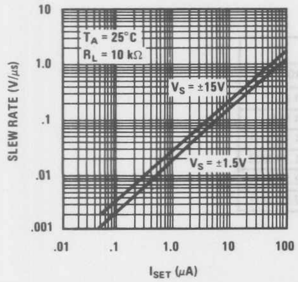
Quiescent Current (I_q) vs Temperature



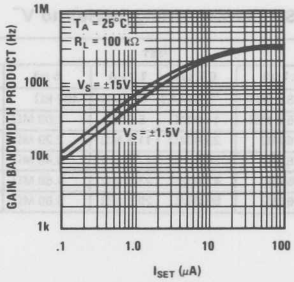
Quiescent Current (I_q) vs I_{SET}



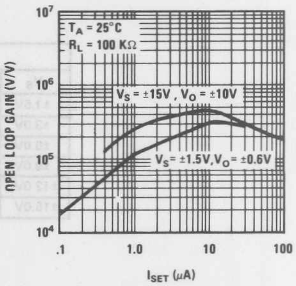
Slew Rate vs I_{SET}



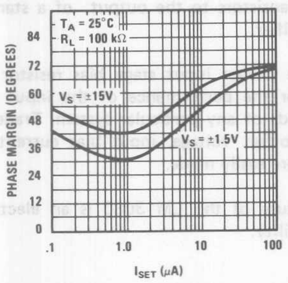
Gain Bandwidth Product vs I_{SET}



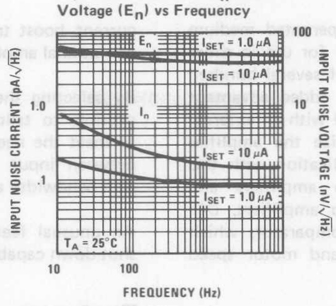
Open Loop Voltage Gain vs I_{SET}



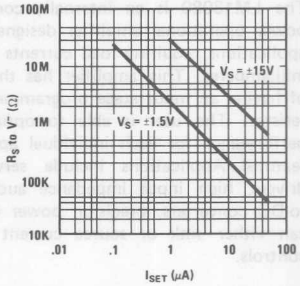
Phase Margin vs I_{SET}



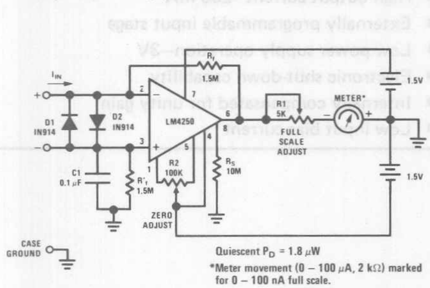
Input Noise Current (I_n) and Voltage (E_n) vs Frequency



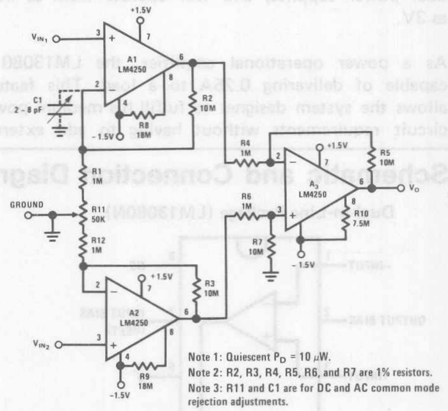
R_{SET} vs I_{SET}



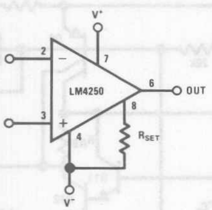
Typical Applications (Continued)



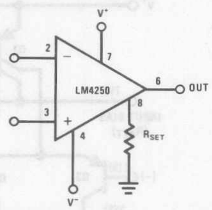
Floating Input Meter Amplifier 100 Nano-Ampere Full Scale



X100 Instrumentation Amplifier 10 µW



R_{SET} Connected to V^-

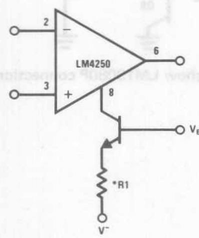


R_{SET} Connected to Ground

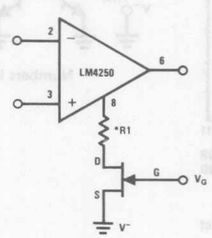
I_{SET} EQUATIONS:

$$I_{SET} \approx \frac{V^+ + |V^-| - 0.5}{R_{SET}}$$ where R_{SET} is connected to V^-.

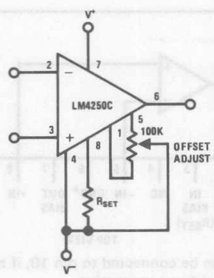
$$I_{SET} \approx \frac{V^+ - 0.5}{R_{SET}}$$ where R_{SET} is connected to ground.



Transistor Current Source Biasing



FET Current Source Biasing



Offset Null Circuit

*R1 limits I_{SET} maximum

National Semiconductor

Operational Amplifiers/Buffers

LM13080 Programmable Power Op Amp

General Description

The LM13080 is an internally compensated medium power operational amplifier designed for use in those applications requiring load currents of several hundred milliamperes. This amplifier has the added advantage of having an input stage programmed with an external resistor. The user is able to optimize the amplifier performance for each individual application with this feature. Applications include servo amplifiers and drivers, high input impedance audio amplifiers, DC-to-DC converters, precision power comparators which can either sink or source current and motor speed controls.

The LM13080 may be powered from either single or dual power supplies, and will operate from as little as 3V.

As a power operational amplifier, the LM13080 is capable of delivering 0.25A to a load. This feature allows the system designer to fulfill his medium power circuit requirements without having to add external current boost transistors to the output of a standard operational amplifier.

By selecting the proper input stage bias resistor it is possible to tailor the performance of the input stage to meet the needs of any particular system. Trade-offs between input offset voltage, input bias current and gain bandwidth are easily made.

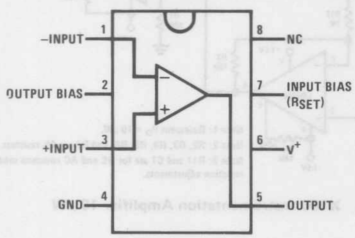
An unusual feature of the LM13080 is an electronic shut-down capability.

Features

- High output current—250 mA
- Externally programmable input stage
- Low power supply operation—3V
- Electronic shut-down capability
- Internally compensated for unity gain
- Low input bias current

Schematic and Connection Diagrams

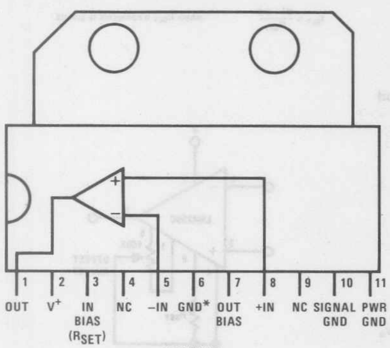
Dual-In-Line Package (LM13080N)



TOP VIEW

Order Number LM13080N
See NS Package N08A

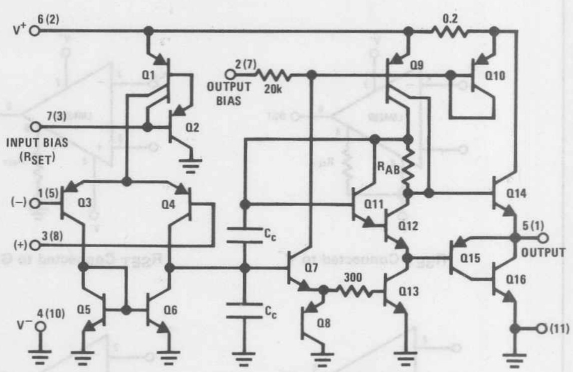
Single-In-Line Package (LM13080P)



TOP VIEW

*Pin 6 can be connected to pin 10, if not, pin 6 must be left with no connection.

Order Number LM13080P
See NS Package P11A



Numbers in parentheses show LM13080P connections

Absolute Maximum Ratings

Supply Voltage Operation Range	3V to 15V or ±1.5V to ±7.5V
Power Dissipation, (Note 1)	
Molded Dual-In-Line Package(LM13080N)	1000 mW
Molded Single-In-Line Package (LM13080P)	1900 mW
Differential Input Voltage, (Note 2)	15V
Input Voltage Range, (Note 3)	−0.3V to +15V
Input Current ($V_{IN} \leq -0.3V$), (Note 4)	20 mA
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (V_S = 12V, R_{SET} = 680k, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	T_A = 25°C, (Note 5)		±3	±7	mV
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$, T_A = 25°C		100	400	nA
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, T_A = 25°C		±30	±75	nA
Supply Current	$R_L = \infty$, T_A = 25°C, (Note 6)		3	6	mA
Output Voltage Swing	V_S = ±6V, T_A = 25°C, (Note 1)				
V_{OH}	$R_L = 50\Omega$	4.5	5		V
	$R_L = 8\Omega$	2			V
V_{OL}	$R_L = 50\Omega$		−5	−4.5	V
	$R_L = 8\Omega$			−2	V
Large Signal Voltage Gain	V_S = ±6V, $R_L = 50\Omega$, f = 100 Hz, T_A = 25°C	3	10		V/mV
Input Common-Mode Voltage Range	$V_S \leq$ 15V, T_A = 25°C, (Note 3)	1		V_S−1.5	V
Input Offset Voltage	(Note 5)			±10	mV
Input Offset Voltage Drift			5		μV/°C
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$			600	nA
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			±150	nA
Input Offset Current Drift			50		pA/°C
Supply Current	$R_L = \infty$, (Note 6)			8	mA
Output Voltage Swing	V_S = ±6V, (Note 1)				
V_{OH}	$R_L = 50\Omega$			4	V
	$R_L = 8\Omega$			1.6	V
V_{OL}	$R_L = 50\Omega$	−4			V
	$R_L = 8\Omega$	−1.6			V
Large Signal Voltage Gain	V_S = ±6V, $R_L = 50\Omega$, f = 100 Hz	1			V/mV
Input Common-Mode Voltage Range	$V_S \leq$ 15V, (Note 3)	1.25		V_S−1.75	V
Common-Mode Rejection Ratio		63	85		dB
Total Harmonic Distortion	$R_L = 8\Omega$, V_O = 2 Vrms, f = 1 kHz		0.5	5	%

Note 1: For operation at high temperatures, the LM13080 must be derated based upon a maximum junction temperature of 150°C and a thermal resistance of 120°C/W for the miniDIP package (LM13080N) or a thermal resistance as given by the curves for the single-in-line power package (LM13080P). The thermal resistance values given are for a still air ambient with the package soldered into a printed circuit board.

Note 2: Differential input voltages up to the magnitude of the power supply voltage will not damage the input circuitry. However, input voltages outside the input common-mode voltage range will not be able to properly control the output of the amplifier.

Note 3: The input voltage applied to either input should not be allowed to go more than 0.3V below the potential applied to pin 4; however, either input can be taken as high as 15V without causing damage to the circuit. Input voltages below the minimum common-mode voltage range may cause a phase reversal in the output.

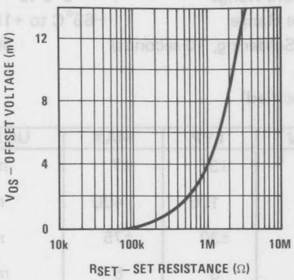
Note 4: This input current will exist only when the voltage at either input lead is driven negative. It is due to the base-isolation junction of the PNP transistor tub becoming forward biased and thereby acting as an input diode clamp. In addition to this diode action, there is also lateral NPN parasitic action on the IC chip. This transistor action can cause the output to take an undefined state for the time duration that an input is driven negative.

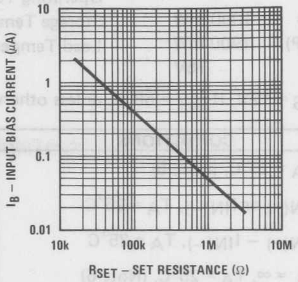
Note 5: V_O = 6V, $R_S = 0\Omega$, and over the full input common-mode voltage range.

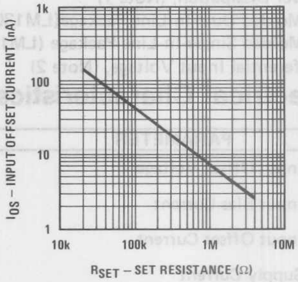
Note 6: Supply current is measured with the amplifier connected in a unity gain follower configuration and the positive input set to one-half of the supply voltage.

Input Bias Current

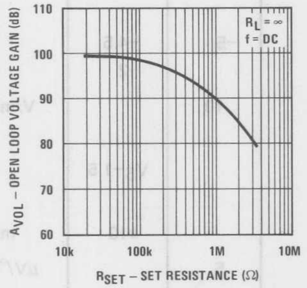
Offset Current



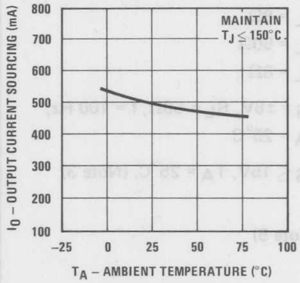




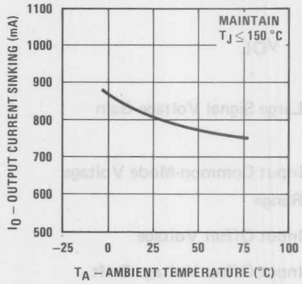
Voltage Gain as a Function of R_{SET}



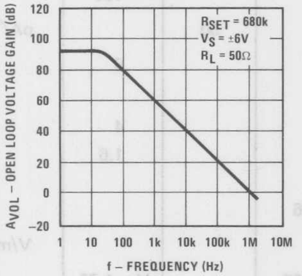
Output Current Sourcing



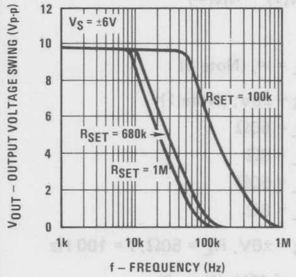
Output Current Sinking



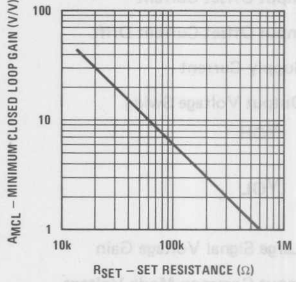
Small Signal Open Loop Frequency Response



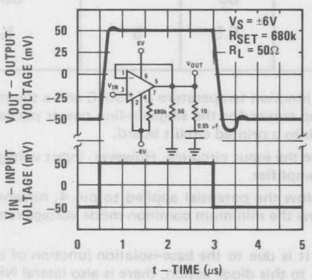
Large Signal Frequency Response



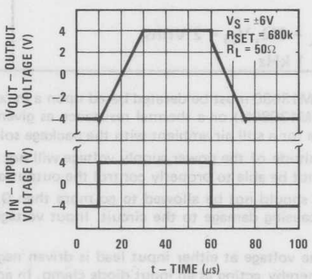
Minimum Stable Closed Loop Gain



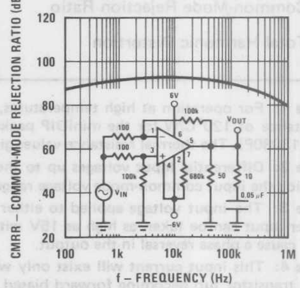
Voltage Follower Pulse Response (Small Signal)



Voltage Follower Pulse Response (Large Signal)

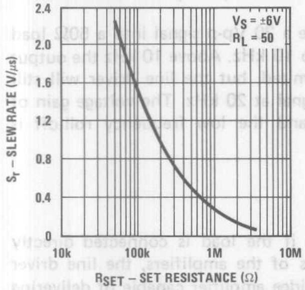


Common-Mode Rejection Ratio

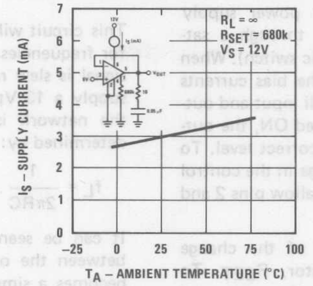


Typical Performance Characteristics (Continued)

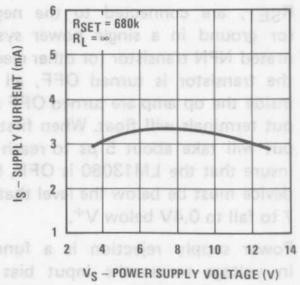
Slew Rate as Function of R_{SET}



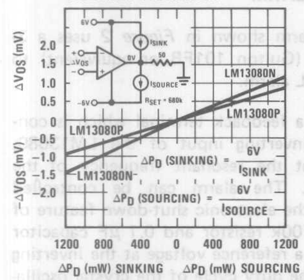
Supply Current



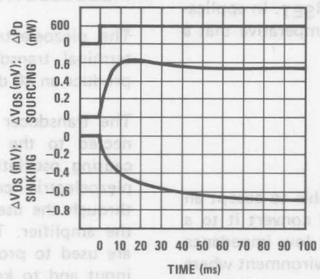
Supply Current



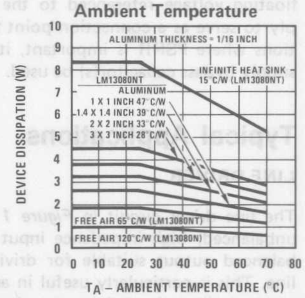
Offset Voltage Change vs Power Dissipation Due to Thermal Feedback



Thermal Feedback Time Constant



Device Dissipation vs Ambient Temperature



Application Hints

The LM13080 is a power op amp capable of sourcing or sinking more than 250 mA and does not include internal current limit or thermal shut-down. Therefore, the user must make sure that his application will not cause the power dissipation rating of the package to be exceeded. In the plastic miniDIP package the LM13080N is rated at a maximum dissipation of 1000 mW at 25°C; whereas the metal tab single-in-line (SIP) package (LM13080P) will handle 1900 mW in free air, also at 25°C. For operation at temperatures above 25°C, the maximum dissipation must be derated using the equation:

$$P_D = \frac{T_J - T_A}{\Theta_{JA}}$$

where P_D is the maximum allowable power dissipation, T_J is the maximum junction temperature (150°C), T_A is the ambient temperature and Θ_{JA} is the thermal resistance of the package operated in a still air environment. Θ_{JA} for the LM13080N is 120°C/W, whereas the Θ_{JA} of the LM13080P depends upon the heat sink used (see curve). For example, if the LM13080P is used in free air in a 70°C ambient, the maximum power that can be dissipated is:

$$P_D = \frac{150^\circ C - 70^\circ C}{65^\circ C/W} = 1230 \text{ mW}.$$

The LM13080 derives its ability to sink current through the use of a composite NPN/PNP output configuration. This local loop must be compensated by the series connection of a 0.05 μF capacitor and a 10Ω resistor between the output of the op amp (pin 5) and the negative power supply (pin 4). The RC does not just filter out the oscillation from the output waveform but actually stabilizes the loop.

If the inputs of the LM13080 are driven below the input common-mode voltage range, it is possible that the output will experience a phase reversal. This is particularly true for the non-inverting input ($V_{IN(+)}$). If either input is driven to a voltage level 0.3V below the substrate (pin 4) a parasitic NPN transistor will be turned ON. The emitter of this parasitic transistor is the normal input transistor epi (N-type, base) region, the base is the substrate (P-type) and the collector is every other epi region on the die. Circuit operation in this mode is unpredictable. If an input is forced below the substrate, the current flowing out of that input should be limited to 20 mA to insure that the amplifier will not be destroyed.

Programming the LM13080 is accomplished by selecting the value of R_{SET}, the input stage bias resistor, to optimize the amplifier for each particular application. An example would be an application with low source resistance which requires a low offset voltage to make a precise DC measurement. By selecting an R_{SET} of 100 kΩ, the normal offset voltage would be reduced to approximately one-fourth the value it would be if a 680k resistor was used. By studying the curves, it can be seen that the bias current will increase but an increase here has very little effect due to the small source impedance. It should also be noted that with a 100k input set resistor the gain bandwidth product will also increase, and in fact, the amplifier must be operated with a closed loop voltage gain of 6 to assure stability.

The effect of R_{SET} on the total quiescent supply current will be very small ($\Delta I_S < 5\% \ I_S$) as long as R_{SET} is 100k or greater.

Application Hints (Continued)

To employ electronic shut-down the output bias pin, pin 2, and the negative end of the input bias resistor, R_{SET}, are connected to the negative power supply (or ground in a single power system) through a saturated NPN transistor (or other electronic switch). When the transistor is turned OFF, all of the bias currents inside the op amp are turned OFF and all input and output terminals will float. When first turned ON, the output will take about 5 μs to reach the correct level. To insure that the LM13080 is OFF, leakage in the control device must be below the level that will allow pins 2 and 7 to fall to 0.4V below V^+.

Power supply rejection is a function of the change in voltage across the input bias resistor, R_{SET}. To improve the PSRR of the LM13080, the user must be careful to bypass pin 7 to pin 6 or to establish a floating voltage referenced to the positive power supply to serve as a connection point for R_{SET}. In applications where PSRR is important, it is imperative that a supply bypass capacitor(s) be used.

Typical Applications

LINE DRIVER

The line driver circuit in *Figure 1* is able to accept an unbalanced, high impedance input and convert it to a balanced output suitable for driving a low impedance line. This is particularly useful in an environment where magnetically induced hum or noise pickup is a problem.

The outputs of the 2 LM13080's are of opposite polarity; therefore, terminating the line with a balanced load (i.e., a differential amplifier or a transformer) will cause common-mode interference pickup to be cancelled.

This circuit will drive a 20 Vp-p signal into a 50Ω load for frequencies up to 10 kHz. Above 10 kHz the output signal is slew rate limited, but the line driver will still supply a 13 Vp-p signal at 20 kHz. The voltage gain of the network is 2, and the low frequency roll-off is determined by:

$$f_L = \frac{1}{2\pi RC}.$$

It can be seen that if the load is connected directly between the outputs of the amplifiers, the line driver becomes a simple bridge amplifier capable of delivering 2W into a 16Ω load.

PIEZOELECTRIC ALARM

The piezoelectric alarm shown in *Figure 2* uses a 3-terminal transducer (Gulton 101FB or equivalent) to produce an 80 dB SPL alarm.

The transducer has a feedback terminal which is connected to the non-inverting input of the LM13080, causing oscillation at the resonant frequency of the piezoelectric crystal. The alarm can be controlled through the use of the electronic shut-down feature of the amplifier. The 100k resistor and 0.1 μF capacitor are used to provide a reference voltage at the inverting input and to keep the duty cycle of the crystal oscillation close to 50%. The RC time constant of this feedback network should be much greater than the time constant of the transducer.

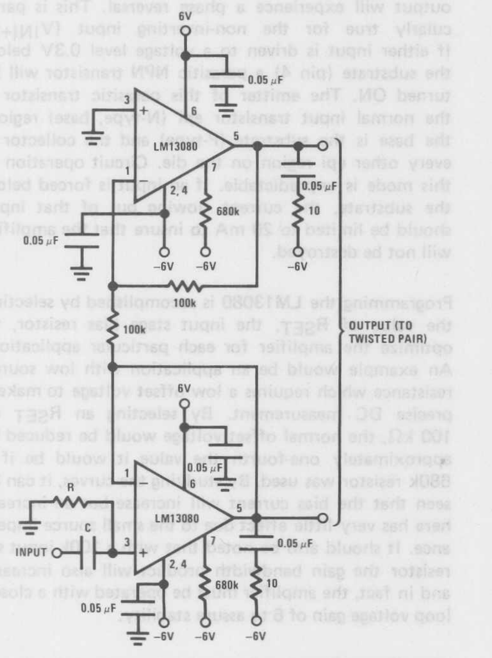


FIGURE 1. Line Driver — Unbalanced Input to Balanced Output

Note: Pin numbers apply to miniDIP.

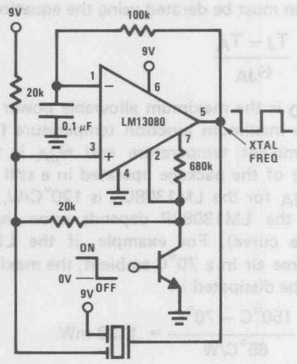


FIGURE 2. Piezoelectric Alarm

Typical Applications (Continued)

SIRENS

Two separate circuits for sirens are shown. The first, *Figure 3*, is a 2-state or ON-OFF type siren where the LM13080 oscillates at an audio frequency and drives an 8Ω speaker and the LM339 acts as a switch which controls the audio burst rate. The second siren, *Figure 4*, provides a constant audio output but alternates between 2 separate tones. The LM13080 is set to oscillate at one basic frequency and this frequency is changed by adding a 200 kΩ charging resistor in parallel with the feedback resistor, R2.

LAMP FLASHER – RELAY DRIVER

The LM13080 is easily adaptable to such applications as low frequency warning devices. The output of the oscillator is a squarewave that is used to drive lamps or small relays. As shown in *Figure 5*, the circuit alternately flashes 2 incandescent lamps.

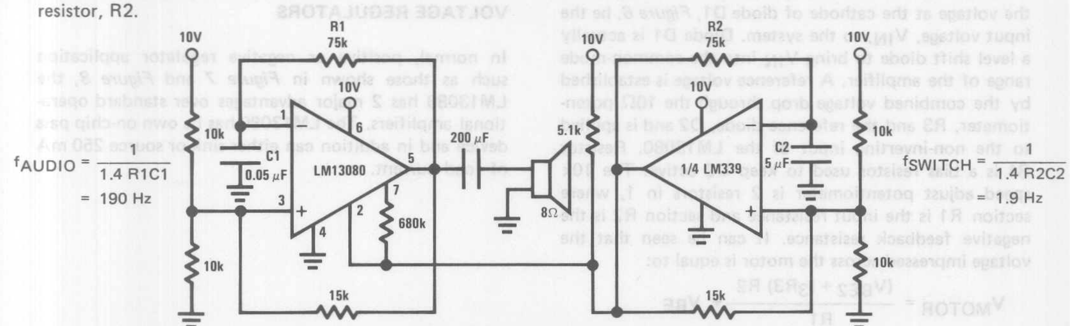


FIGURE 3. 2-State Siren

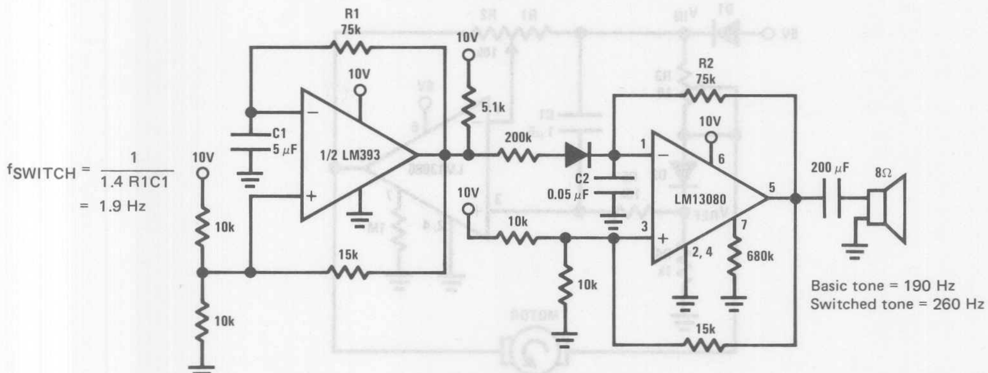
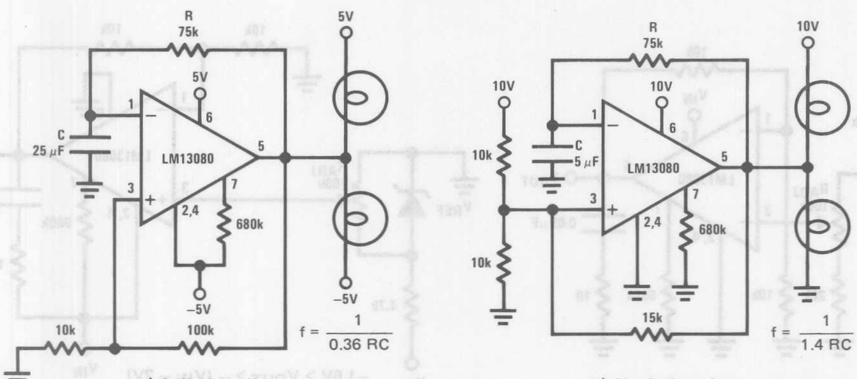


FIGURE 4. 2-Tone Siren



a) Split Supplies

b) Single Supply

FIGURE 5. Low Frequency Lamp Flasher/Relay Driver

Note: Pin numbers apply to miniDIP.

speed control for small motors requiring less than 0.5A start current. This circuit operates by impressing the multiple of a reference voltage across the motor, and then varying the reference by means of quasi-positive feedback to change the voltage across the motor any time the load on the motor changes.

To understand the circuit operation, it is easiest to let the voltage at the cathode of diode D1, *Figure 6*, be the input voltage, V_{IN}, to the system. Diode D1 is actually a level shift diode to bring V_{IN} into the common-mode range of the amplifier. A reference voltage is established by the combined voltage drop through the 10Ω potentiometer, R3 and the reference diode, D2 and is applied to the non-inverting input of the LM13080. Resistor R4 is a bias resistor used to keep D2 active. The 10k speed adjust potentiometer is 2 resistors in 1, where section R1 is the input resistance and section R2 is the negative feedback resistance. It can be seen that the voltage impressed across the motor is equal to:

$$V_{MOTOR} = \frac{(V_{BE2} + I_3R3)\ R2}{R1} + V_{BE}$$

The positive feedback is developed as a change in the voltage across R3 due to the change in the motor current caused by a variation in the motor's load. Resistor R3 is shown as a potentiometer so that the amount of positive feedback can be adjusted for smooth operation of the motor. Capacitor C1 and resistor R5 serve as a filter for the reference voltage at the non-inverting input of the amplifier.

VOLTAGE REGULATORS

In normal, positive or negative regulator application such as those shown in *Figure 7* and *Figure 8*, the LM13080 has 2 major advantages over standard operational amplifiers. The LM13080 has its own on-chip pass device and in addition can either sink or source 250 mA of load current.

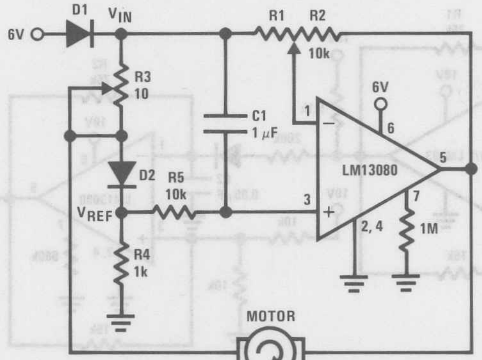
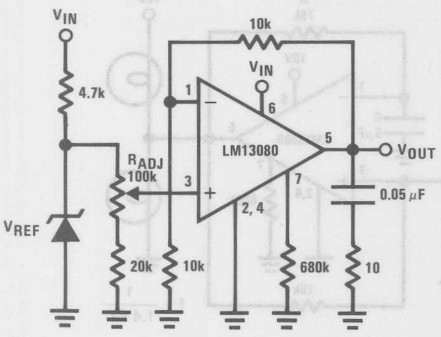
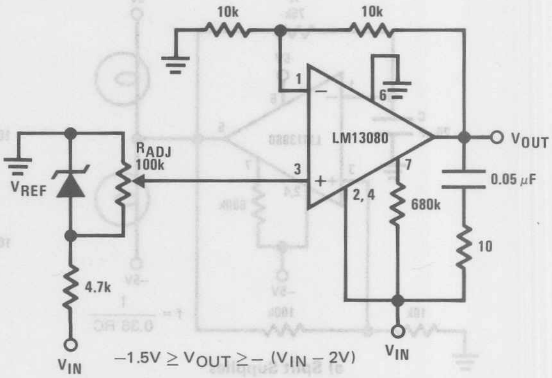


FIGURE 6. Motor Speed Control



$2V \leq V_{OUT} \leq (V_{IN} - 2V)$

FIGURE 7. Positive Variable Voltage Regulator



$-1.5V \geq V_{OUT} \geq -(V_{IN} - 2V)$

FIGURE 8. Negative Variable Voltage Regulator

Note: Pin numbers apply to miniDIP.

LH0002/LH0002C Current Amplifier

General Description

The LH0002/LH0002C is a general purpose thick film hybrid current amplifier that is built on a single substrate. The circuit features:

- High Input Impedance 400 kΩ
- Low Output Impedance 6Ω
- High Power Efficiency
- Low Harmonic Distortion
- DC to 30 MHz Bandwidth
- Output Voltage Swing that Approaches Supply Voltage
- 400 mA Pulsed Output Current
- Slew rate is typically 200V/μs
- Operation from ±5V to ±20V

These features make it ideal to integrate with an operational amplifier inside a closed loop configuration to increase current output. The symmetrical output portion of the circuit also provides a low output impedance for both the positive and negative slopes of output pulses.

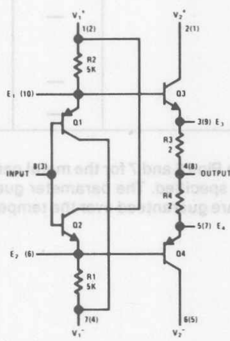
The LH0002 is available in an 8-lead low-profile TO-5 header; the LH0002C is also available in an 8-lead TO-5, and a 10-pin molded dual-in-line package.

The LH0002 is specified for operation over the −55°C to +125°C military temperature range. The LH0002C is specified for operation over the 0°C to +85°C temperature range.

Applications

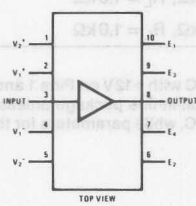
- Line driver
- 30 MHz buffer
- High speed D/A conversion
- Instrumentation buffer
- Precision current source

Schematic and Connection Diagrams



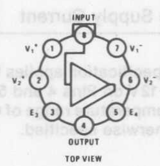
Pin numbers in parentheses denote pin connections for dual-in-line package.

Dual-In-Line Package



Order Number LH0002CN
See Package N10B

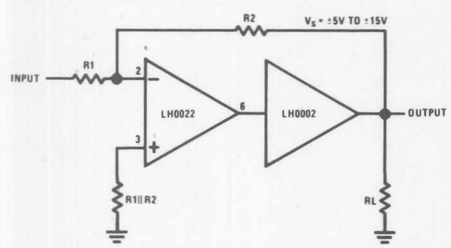
Metal Can Package



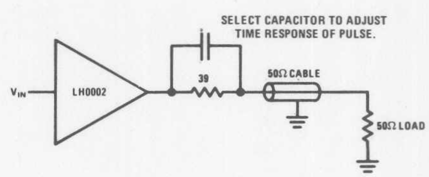
Order Number LH0002H or LH0002CH
See Package H08A

Typical Applications

High Current Operational Amplifier



Line Driver



*Previously called NH0002/NH0002C

Absolute Maximum Ratings

Supply Voltage	±22V
Power Dissipation Ambient	600 mW
Input Voltage (Equal to Power Supply Voltage)	
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
LH0002	−55°C to +125°C
LH0002C	0°C to +85°C
Steady State Output Current	±100 mA
Pulsed Output Current (50 ms On/1 sec. Off)	±400 mA

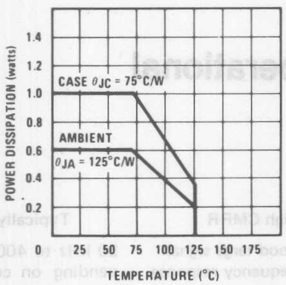
Electrical Characteristics (Note 1)

Parameter	Conditions	Min.	Typ.	Max.	Units
Voltage Gain	$R_S = 10\,k\Omega$, $R_L = 1.0\,k\Omega$, $V_{IN} = \pm 10\,V$	0.95	0.97		
AC Current Gain	$V_{IN} = 1.0\,V_{rms}$, $f = 1.0\,kHz$		40		A/ma
Input Impedance	$R_S = 200\,k\Omega$, $V_{IN} = \pm 1.0\,V$, $R_L = 1.0\,k\Omega$	180	400	—	kΩ
Output Impedance	$V_{IN} = \pm 1.0\,V$, $R_L = 50\,\Omega$, $R_S = 10\,k\Omega$	—	6.0	10	Ω
Output Voltage Swing	$R_L = 1.0\,k\Omega$, $V_{IN} = \pm 12\,V$	±10	±11	—	V
Output Voltage Swing	$V_S = \pm 15\,V$, $V_{IN} = \pm 12\,V$, $R_S = 50\,\Omega$, $R_L = 100\,\Omega$, $T_A = 25°C$	±10			V
DC Output Offset Voltage	$R_S = 300\,\Omega$, $R_L = 1.0\,k\Omega$	—	±10	±30	mV
DC Input Offset Current	$R_S = 10\,k\Omega$, $R_L = 1.0\,k\Omega$	—	±6.0	±10	μA
Harmonic Distortion	$V_{IN} = 5.0\,V_{rms}$, $f = 1.0\,kHz$	—	0.1	—	%
Rise Time	$R_L = 50\,\Omega$, $\Delta V_{IN} = 100\,mV$		7.0	12	ns
Positive Supply Current	$R_S = 10\,k\Omega$, $R_L = 1.0\,k\Omega$	—	+6.0	+10	mA
Negative Supply Current	$R_S = 10\,k\Omega$, $R_L = 1.0\,k\Omega$	—	−6.0	−10	mA

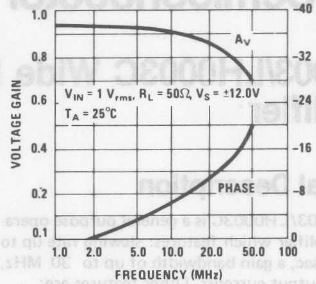
Note 1: Specification applies for $T_A = 25°C$ with +12V on Pins 1 and 2; −12V on Pins 6 and 7 for the metal can package and +12V on Pins 1 and 2; −12V on Pins 4 and 5 for the dual-in-line package unless otherwise specified. The parameter guarantees for LH0002C apply over the temperature range of 0°C to +85°C, while parameters for the LH0002 are guaranteed over the temperature range −55°C to 125°C unless otherwise specified.

Typical Performance

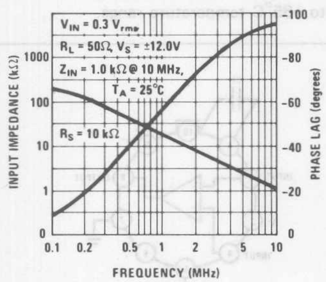
Maximum Power Dissipation



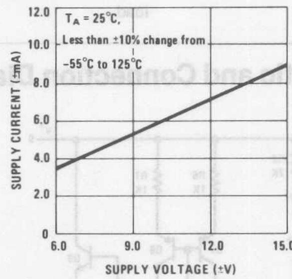
Frequency Response



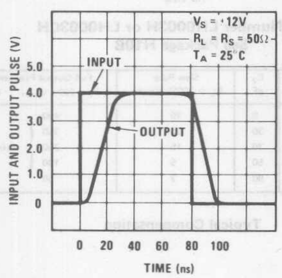
Input Impedance (Magnitude & Phase)



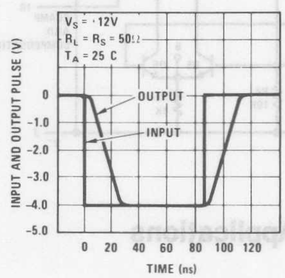
Supply Current



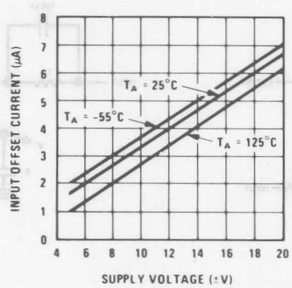
Positive Pulse



Negative Pulse



Input Offset Current



LH0003/LH0003C Wide Bandwidth Operational Amplifier

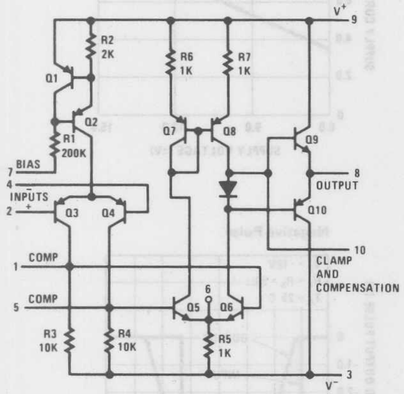
General Description

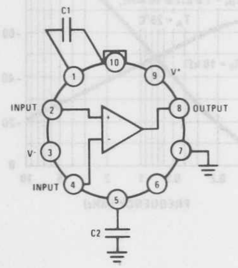
The LH0003/LH0003C is a general purpose operational amplifier which features: slewing rate up to 70 volts/μsec, a gain bandwidth of up to 30 MHz, and high output currents. Other features are:

- Very low offset voltage — Typically 0.4 mV
- Large output swing — > ±10V into 100Ω load
- High CMRR — Typically > 90 dB
- Good large signal frequency response — 50 kHz to 400 kHz depending on compensation

The LH0003 is specified for operation over the −55°C to +125°C military temperature range. The LH0003C is specified for operation over the 0°C to +85°C temperature range.

Schematic and Connection Diagrams





TOP VIEW

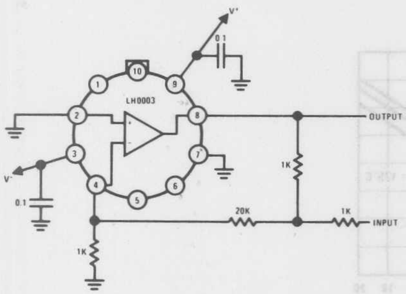
Order Number LH0003H or LH0003CH
See Package H10B

Circuit Gain	C_1 pF	C_2 pF	Slew Rate $R_L > 200\Omega$, V/μsec	Full Output Frequency $R_L \geq 200\Omega$ $V_{OUT} = \pm 10$ V
≥ 40	0	0	70	400 kHz
≥ 10	5	30	30	350 kHz
≥ 5	15	30	15	250 kHz
≥ 2	50	50	5	100 kHz
≥ 1	90	90	2	50 kHz

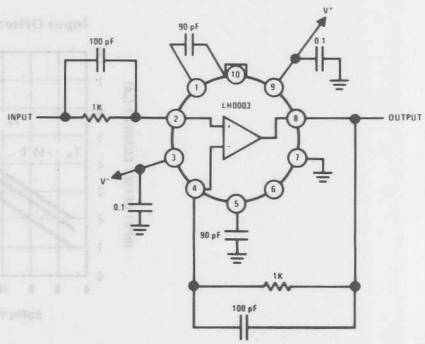
Typical Compensation

Typical Applications

High Slew Rate Unity Gain Inverting Amplifier



Unity Gain Follower



*Previously called NH0003/NH0003C

Absolute Maximum Ratings

Supply Voltage		±20V
Power Dissipation		See curve
Differential Input Voltage		±7V
Input Voltage		Equal to supply
Load Current		120 mA
Operating Temperature Range	LH0003	−55°C to +125°C
	LH0003C	0°C to +85°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

Electrical Characteristics (Notes 1 & 2)

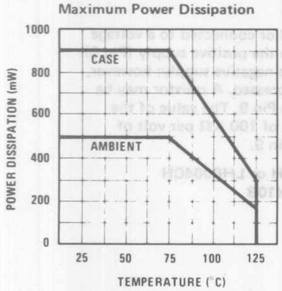
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S < 100\Omega$		0.4	3.0	mV
Input Offset Current			0.02	0.2	μA
Input Bias Current			0.4	2.0	μA
Supply Current	$V_S = \pm 20V$		1.2	3	mA
Voltage Gain	$R_L = 100k$, $V_S = \pm 15V$, $V_{OUT} = \pm 10V$	20	70		V/mV
Voltage Gain	$R_L = 2k$, $V_S = \pm 15V$, $V_{OUT} = \pm 10V$	15	40		V/mV
Output Voltage Swing	$V_S = \pm 15$, $R_L = 100\Omega$	±10	±12		V
Input Resistance			100		kΩ
Average Temperature Coefficient of Offset Voltage	$R_S < 100\Omega$		4		μV/°C
Average Temperature Coefficient of Bias Current			8		nA/°C
CMRR	$R_S < 100\Omega$, $V_S = \pm V$, $V_{IN} = \pm 10V$	70	90		dB
PSRR	$R_S < 100\Omega$, $V_S = \pm 15V$, $\Delta V = 5V$ to $20V$	70	90		dB
Equivalent Input Noise Voltage	$R_S = 100\Omega$, f = 10 kHz to 100 kHz $V_S = \pm 15V$ dc		1.8		μVrms

Note 1. These specifications apply for Pin 7 grounded, for $\pm 5V < V_S < \pm 20V$, with capacitor $C_1 = 90$ pF from Pin 1 to Pin 10 and $C_2 = 90$ pF from Pin 5 to ground, over the specified operating temperature range, unless otherwise specified.

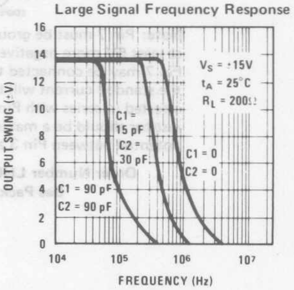
Note 2. Typical values are for $t_{AMBIENT} = 25°C$ unless otherwise specified.

Typical Performance

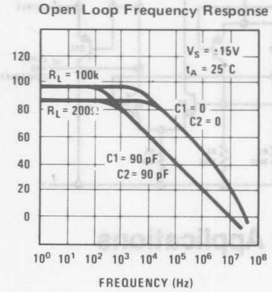
Maximum Power Dissipation



Large Signal Frequency Response



Open Loop Frequency Response



National Semiconductor

Operational Amplifiers/Buffers

LH0004/LH0004C High Voltage Operational Amplifier

General Description

The LH0004/LH0004C is a general purpose operational amplifier designed to operate from supply voltages up to ±40V. The device dissipates extremely low quiescent power, typically 8 mW at 25°C and V_S = ±40V. Additional features include:

- Capable of operation over the range of ±5V to ±40V
- Large output voltage typically ±35V for the LH0004 and ±33V for the LH0004C into a 2 KΩ load with ±40V supplies
- Low input offset current typically 20 nA for the LH0004 and 45 nA for the LH0004C
- Low input offset voltage typically 0.3 mV
- Frequency compensation with 2 small capacitors
- Low power consumption 8 mW at ±40V

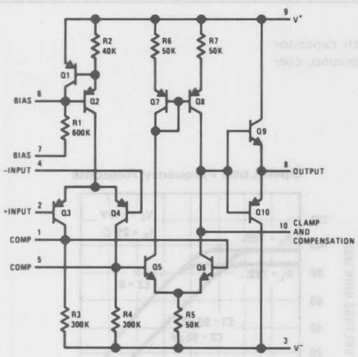
The LH0004's high gain and wide range of operating voltages make it ideal for applications requiring large output swing and low power dissipation.

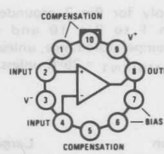
The LH0004 is specified for operation over the −55°C to +125°C military temperature range. The LH0004C is specified for operation over the 0°C to +85°C temperature range.

Applications

- Precision high voltage power supply
- Resolver excitation
- Wideband high voltage amplifier
- Transducer power supply

Schematic and Connection Diagrams



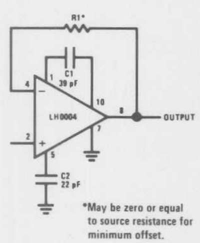


Note: Pin 7 must be grounded or connected to a voltage at least 5V more negative than the positive supply (Pin 9). Pin 7 may be connected to the negative supply; however, the standby current will be increased. A resistor may be inserted in series with Pin 7 to Pin 9. The value of the resistor should be a maximum of 100 KΩ per volt of potential between Pin 3 and Pin 9.

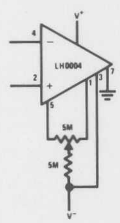
Order Number LH0004H or LH0004CH
See Package H10B

Typical Applications

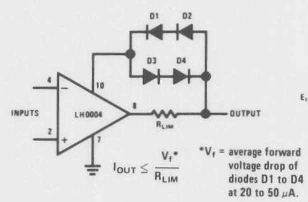
Voltage Follower



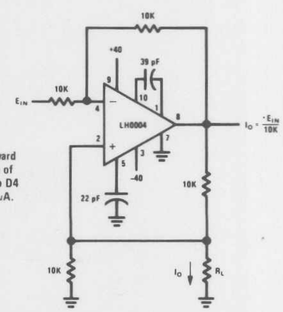
Input Offset Voltage Adjust



External Current Limiting Method



High Compliance Current Source



*Previously called NH0004/NH0004C

Absolute Maximum Ratings

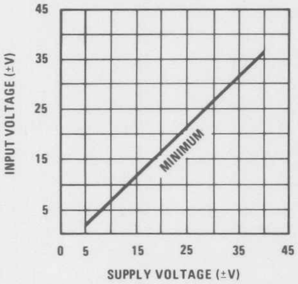
Supply Voltage, Continuous	±45V
Power Dissipation (See curve)	400 mW
Differential Input Voltage	±7V
Input Voltage	Equal to supply
Short Circuit Duration	3 sec
Operating Temperature Range LH0004	−55°C to +125°C
LH0004C	0°C to 85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics (Note 1)

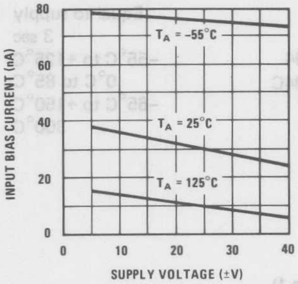
PARAMETER	CONDITIONS	LH0004			LH0004C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 100\,\Omega$, $T_A = 25°C$		0.3	1.0		0.3	1.5	mV
	$R_S \leq 100\,\Omega$			2.0			3.0	mV
Input Bias Current	$T_A = 25°C$		20	100		30	120	nA
				300			300	nA
Input Offset Current	$T_A = 25°C$		3	20		10	45	nA
				100			150	nA
Positive Supply Current	$V_S = \pm 40V$, $T_A = 25°C$		110	150		110	150	µA
	$V_S = \pm 40V$			175			175	µA
Negative Supply Current	$V_S = \pm 40V$, $T_A = 25°C$		80	100		80	100	µA
	$V_S = \pm 40V$			135			135	µA
Voltage Gain	$V_S = \pm 40V$, $R_L = 100k$, $T_A = 25°C$ $V_{OUT} = \pm 30V$	30	60		30	60		V/mV
	$V_S = \pm 40V$, $R_L = 100k$ $V_{OUT} = \pm 30V$	10			10			V/mV
Output Voltage	$V_S = \pm 40V$, $R_L = 10k$	±30	±35		±30	±33		V
CMRR	$V_S = \pm 40V$, $R_S \leq 5k$ $V_{IN} = \pm 33V$	70	90		70	90		dB
PSRR	$V_S = \pm 40V$, $R_S \leq 5k$ $\Delta V = 20V$ to $40V$	70	90		70	90		dB
Average Temperature Coefficient Offset Voltage	$R_S \leq 100\,\Omega$		4.0			4.0		µV/°C
Average Temperature Coefficient of Offset Current			0.4			0.4		nA/°C
Equivalent Input Noise Voltage	$R_S = 100\,\Omega$, $V_S = \pm 40V$ f = 500 Hz to 5 kHz, $T_A = 25°C$		3.0			3.0		µVrms

Note 1: These specifications apply for $\pm 5V \leq V_S \leq \pm 40V$, Pin 7 grounded, with capacitors C1 = 39 pF between Pin 1 and Pin 10, C2 = 22 pF between Pin 5 and ground, −55°C to +125°C for the LH0004, and 0°C to +85°C for the LH0004C unless otherwise specified.

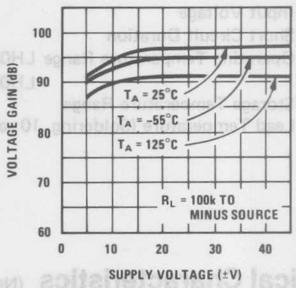
Input Voltage Range



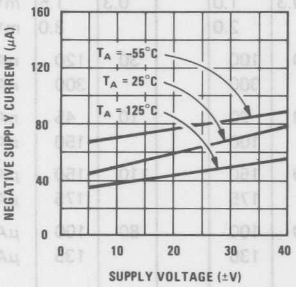
Input Bias Current



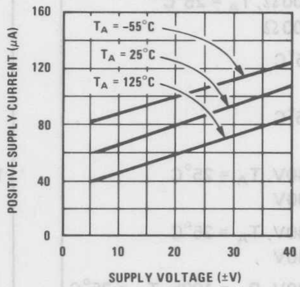
Voltage Gain



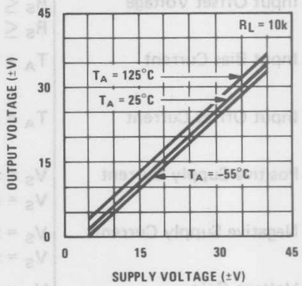
Negative Supply Current



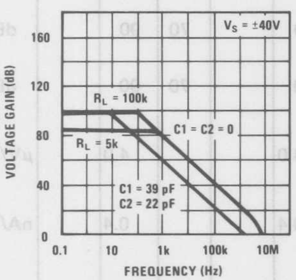
Positive Supply Current



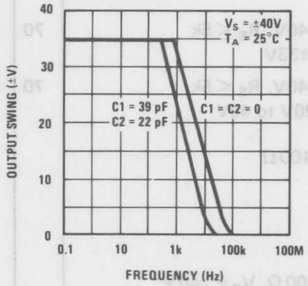
Output Voltage



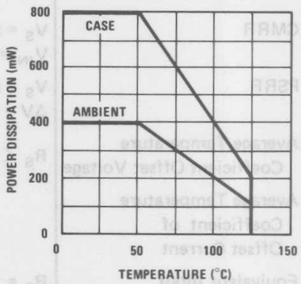
Open Loop Frequency Response



Large Signal Frequency Response



Package Power Dissipation



National Semiconductor

Operational Amplifiers/Buffers

LH0005/LH0005A Operational Amplifier

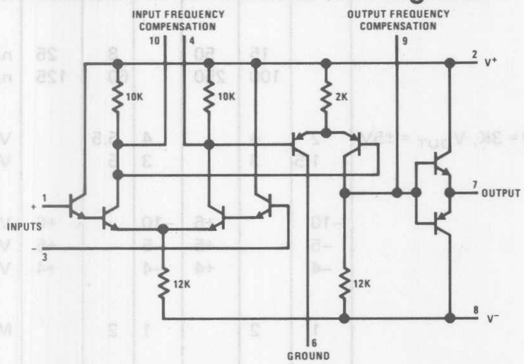
General Description

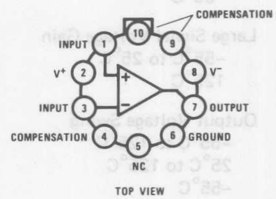
The LH0005/LH0005A is a hybrid integrated circuit operational amplifier employing thick film resistors and discrete silicon semiconductors in its design. The select matching of the input pairs of transistors results in low input bias currents and a very low input offset current, both of which exhibit excellent temperature tracking. In addition, the device features:

- Very high output current capability: ±50 mA into a 100 ohm load
- Low standby power dissipation: typically 60 mW at ±12V
- High input resistance: typically 2M at 25°C
- Full operating range: −55°C to +125°C
- Good high frequency response: unity gain at 30 MHz

With no external roll-off network, the amplifier is stable with a feedback ratio of 10 or greater. By adding a 200 pF capacitor between pins 9 and 10, and a 200 ohm resistor in series with a 75 pF capacitor from pin 4 to ground, the amplifier is stable to unity gain. The unity gain loop phase margin with the above compensation is typically 70 degrees. With a gain of 10 and no compensation the loop phase margin is typically 50 degrees.

Schematic and Connection Diagrams

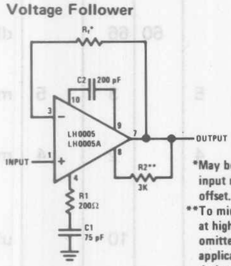




Order Number LH0005H or LH0005AH
See Package H10D

Typical Applications

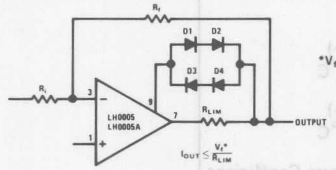
Voltage Follower



*May be zero or equal to the input resistance for minimum offset.

**To minimize crossover distortion at higher frequencies. May be omitted for low frequency application or selected to suit design requirements

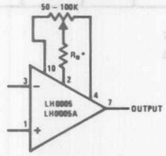
External Current Limiting



*V_f = Average forward voltage drop of diodes D_1 to D_4 at approx. 1 mA.

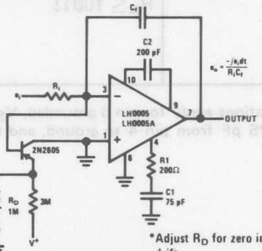
For continuous short circuit protection ($V_S = \pm 12V$, $-55°C < T_A < +100°C$) $R_{LIM} \geq 50\Omega$

Offset Balancing Circuit



*Typical value, R_B = 100K. R_B may be increased for greater sensitivity with reduction in range.

Integrator with Bias Current Compensation



*Adjust R_D for zero integration drift.

*Previously called NH0005/NH0005A

Absolute Maximum Ratings

Supply Voltage	±20V
Power Dissipation (see Curve)	400 mW
Differential Input Voltage	±15V
Input Voltage	Equal to supply voltages
Peak Load Current	±100 mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

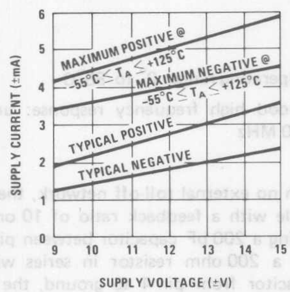
Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	LH0005 MIN	LH0005 TYP	LH0005 MAX	LH0005A MIN	LH0005A TYP	LH0005A MAX	UNITS
Input Offset Voltage								
25°C	$R_S \leq 100\,\Omega$		5	10		1	3	mV
−55°C, 125°C	$R_S \leq 100\,\Omega$			10			4	mV
Input Offset Current								
25°C to 125°C			10	20		2	5	nA
−55°C			25	75		10	25	nA
Input Bias Current								
25°C to 125°C			15	50		8	25	nA
−55°C			100	250		60	125	nA
Large Signal Voltage Gain								
−55°C to 25°C	R_L = 10K, R2 = 3K, V_{OUT} = ±5V	2	4		4	5.5		V/mV
125°C		1.5	3		3	5		V/mV
Output Voltage Swing								
−55°C to 125°C	$R_L = 10\,k\Omega$	−10		+6	−10		+6	V
25°C to 125°C	$R_L = 100\Omega$	−5		+5	−5		+5	V
−55°C	$R_L = 100\Omega$	−4		+4	−4		+4	V
Input Resistance								
25°C		1	2		1	2		MΩ
Common Mode Rejection Ratio								
25°C	V_{IN} = ±4V, $RS \leq 100\,\Omega$	55	60		60	66		dB
Power Supply Rejection Ratio								
25°C		55	60		60	66		dB
Supply Current (+)								
−55°C to 125°C			3	5		3	5	mA
Supply Current (−)								
−55°C to 125°C			2	4		2	4	mA
Average Temperature Coefficient of Input Offset Voltage								
−55°C to 125°C	$R_S \leq 100\,\Omega$		20			10		uV/°C
Output Resistance								
25°C			70			70		Ω

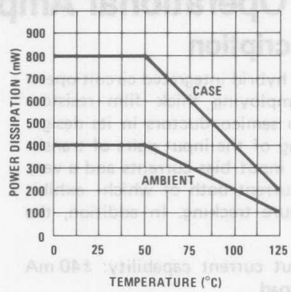
Note 1: These specifications apply for pin 6 grounded, V_S = ±12V, with Resistor R_1 = 200Ω in series with Capacitor C_1 = 75 pF from pin 4 to ground, and C_2 = 200 pF between pins 9 and 10 unless otherwise specified.

Guaranteed Performance Characteristics

Supply Current

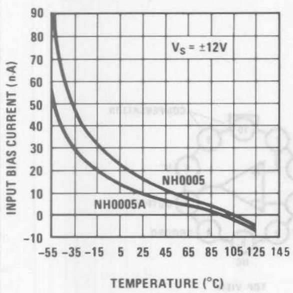


Maximum Power Dissipation

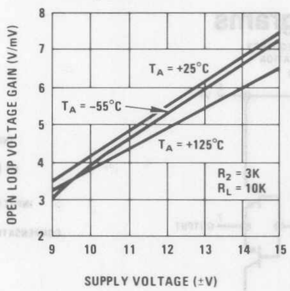


Typical Performance Characteristics

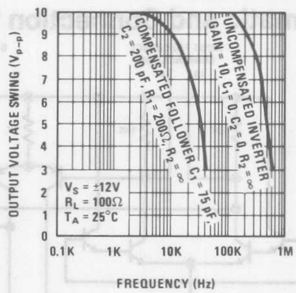
Input Bias Current



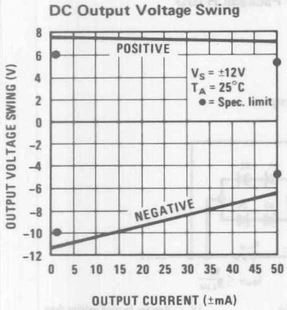
Voltage Gain



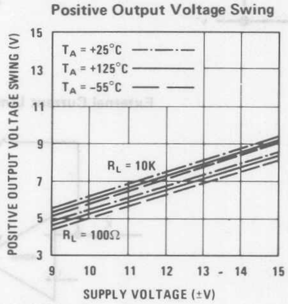
Loaded Output Voltage Swing



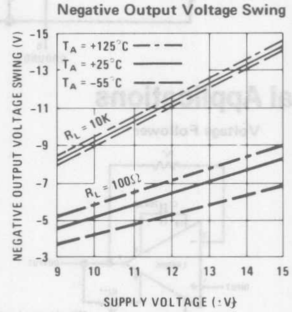
DC Output Voltage Swing



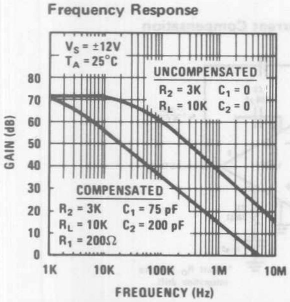
Positive Output Voltage Swing



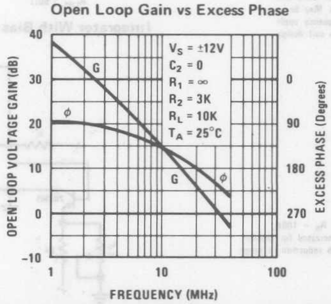
Negative Output Voltage Swing



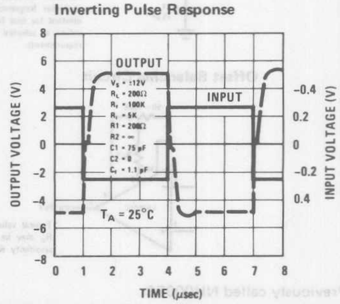
Frequency Response



Open Loop Gain vs Excess Phase



Inverting Pulse Response



LH0005C Operational Amplifier

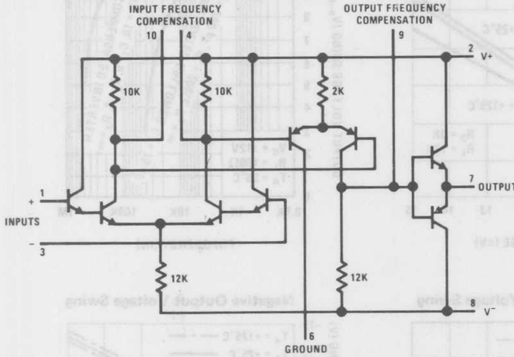
General Description

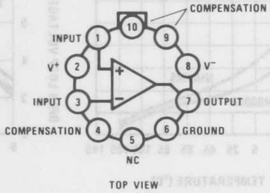
The LH0005C is a hybrid integrated circuit operational amplifier employing thick film resistors and discrete silicon semiconductors in its design. The select matching of the input pairs of transistors results in low input bias currents and a very low input offset current both of which exhibit excellent temperature tracking. In addition, the device features:

- Very high output current capability: ±40 mA into a 100 ohm load
- Low standby power dissipation: typically 60 mW at ±12V
- High input resistance: typically 2M at 25°C
- Operating range: 0° to 85°C
- Good high frequency response: unity gain at 30 MHz

With no external roll-off network, the amplifier is stable with a feedback ratio of 10 or greater. By adding a 200 pF capacitor between pins 9 and 10, and a 200 ohm resistor in series with a 75 pF capacitor from pin 4 to ground, the amplifier is stable to unity gain. The unity gain loop phase margin with the above compensation is typically 70 degrees. With a gain of 10 and no compensation the loop phase margin is typically 50 degrees.

Schematic and Connection Diagrams

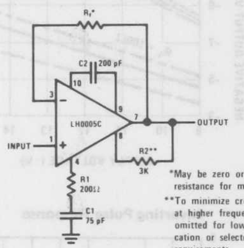




Order Number LH0005CH
See Package H10D

Typical Applications

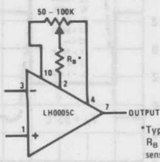
Voltage Follower



*May be zero or equal to the input resistance for minimum offset.

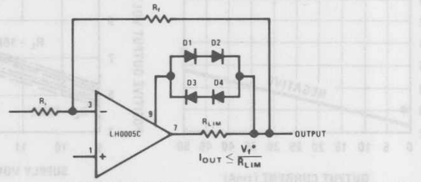
**To minimize crossover distortion at higher frequencies. May be omitted for low frequency application or selected to suit design requirements.

Offset Balancing Circuit



*Typical value, R_B = 100K. R_B may be increased for greater sensitivity with reduction in range.

External Current Limiting

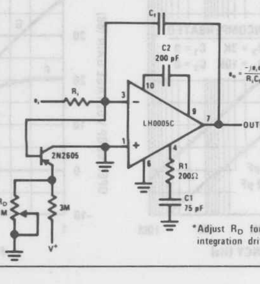


$I_{OUT} \le \frac{V_f^*}{R_{LIM}}$

For continuous short circuit protection (V_S = ±12V, 0°C ≤ T_A ≤ 70°C R_{LIM} ≥ 50Ω)

*V_f = Average forward voltage drop of diodes D_1 to D_4 at approx. 1 mA

Integrator With Bias Current Compensation



*Adjust R_D for zero integration drift.

*Previously called NH0005C

Absolute Maximum Ratings

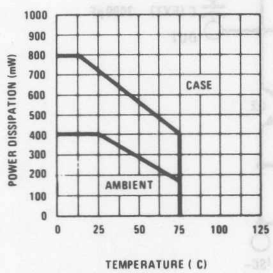
Supply Voltage	±20V
Power Dissipation (see Curve)	400 mW
Differential Input Voltage	±15V
Input Voltage	Equal to supply voltages
Peak Load Current	±100 mA
Storage Temperature Range	$-55^\circ C$ to $+125^\circ C$
Operating Temperature Range	$0^\circ C$ to $85^\circ C$
Lead Temperature (soldering, 10 sec)	$300^\circ C$

Electrical Characteristics

PARAMETER	CONDITIONS	LH0005C MIN	LH0005C TYP (Note 2)	LH0005C MAX	UNITS
Input Offset Voltage	$R_S \leq 100\,\Omega$		3	10	mV
Input Offset Current			5	25	nA
Input Bias Current			20	100	nA
Large Signal Voltage Gain	$R_L = 10K$, $R2 = 3K$, $V_{OUT} = \pm 5V$	2	5		V/mV
Output Voltage Swing	$R_L = 10\,k\Omega$	-10		+6	V
	$R_L = 100\Omega$	-4	±6	+4	V
Input Resistance	$T_A = 25^\circ C$	0.5	2		MΩ
Common Mode Rejection Ratio	$V_{IN} = \pm 4V$, $R_S \leq 100\,\Omega$, $T_A = 25^\circ C$	50	60		dB
Power Supply Rejection Ratio	$T_A = 25^\circ C$	50	60		dB
Supply Current (+)			3	5	mA
Supply Current (–)			2	4	mA

Note 1: These specifications apply for pin 6 grounded, $V_S = \pm 12V$, with Resistor R1 = 200Ω in series with Capacitor C1 = 75 pF from pin 4 to ground, and C2 = 200 pF between pins 9 and 10, over the temperature range of $0^\circ C$ to $+85^\circ C$ unless otherwise specified.

Note 2: Typical values are for $25^\circ C$ only.



Maximum Power Dissipation

National Semiconductor

Operational Amplifiers/Buffers

LH0021/LH0021C 1.0 Amp Power Operational Amplifier
LH0041/LH0041C 0.2 Amp Power Operational Amplifier

General Description

The LH0021/LH0021C and LH0041/LH0041C are general purpose operational amplifiers capable of delivering large output currents not usually associated with conventional IC Op Amps. The LH0021 will provide output currents in excess of one ampere at voltage levels of ±12V; the LH0041 delivers currents of 200 mA at voltage levels closely approaching the available power supplies. In addition, both the inputs and outputs are protected against overload. The devices are compensated with a single external capacitor and are free of any unusual oscillation or latch-up problems.

Features

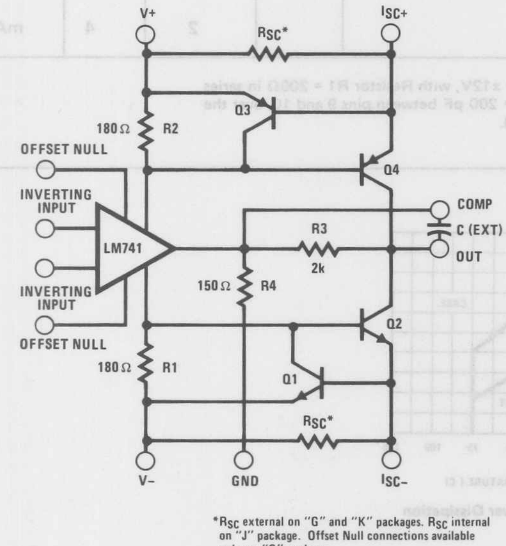
- Output current — 1.0 Amp (LH0021); 0.2 Amp (LH0041)
- Output voltage swing — ±12V into 10Ω (LH0021); ±14V into 100Ω (LH0041)
- Wide full power bandwidth — 15 kHz
- Low standby power — 100 mW at ±15V
- Low input offset voltage and current — 1 mV and 20 nA
- High slew rate — 3.0V/μs
- High open loop gain — 100 dB

The excellent input characteristics and high output capability of the LH0021 make it an ideal choice for power applications such as DC servos, capstan drivers, deflection yoke drivers, and programmable power supplies.

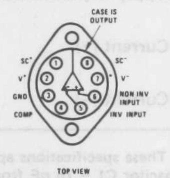
The LH0041 is particularly suited for applications such as torque driver for inertial guidance systems, diddle yoke driver for alpha-numeric CRT displays, cable drivers, and programmable power supplies for automatic test equipment.

The LH0021 is supplied in a 8 pin TO-3 package rated at 20 watts with suitable heatsink. The LH0041 is supplied in both 12 pin TO-8 (2.5 watts with clip on heatsink) and a power 8 pin ceramic DIP (2 watts with suitable heatsink). The LH0021 and LH0041 are guaranteed over the temperature range of −55°C to +125°C while the LH0021C and LH0041C are guaranteed from −25°C to +85°C

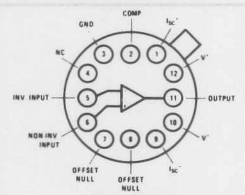
Schematic and Connection Diagrams



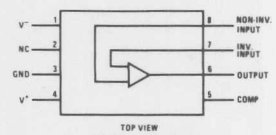
*RSC external on "G" and "K" packages. RSC internal on "J" package. Offset Null connections available only on "G" package.



Order Number LH0021K or LH0021CK
See Package K08A



Order Number LH0041G or LH0041CG
See Package H12B



Order Number LH0041CJ
See Package HY08A

Absolute Maximum Ratings

Supply Voltage		±18V
Power Dissipation		See curves
Differential Input Voltage		±30V
Input Voltage (Note 1)		±15V
Peak Output Current (Note 2)	LH0021/LH0021C	2.0 Amps
	LH0041/LH0041C	0.5 Amps
Output Short Circuit Duration (Note 3)		Continuous
Operating Temperature Range	LH0021/LH0041	−55°C to +125°C
	LH0021C/LH0041C	−25°C to +85°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

DC Electrical Characteristics for LH0021/LH0021C (Note 4)

PARAMETER	CONDITIONS	LIMITS LH0021 MIN	LH0021 TYP	LH0021 MAX	LH0021C MIN	LH0021C TYP	LH0021C MAX	UNITS
Input Offset Voltage	$R_S < 100\Omega$, $T_C = 25°C$		1.0	3.0		3.0	6.0	mV
	$R_S < 100\Omega$			5.0			7.5	mV
Voltage Drift with Temperature	$R_S < 100\Omega$		3	25		5	30	µV/°C
Offset Voltage Drift with Time			5			5		µV/week
Offset Voltage Change with Output Power			5	15		5	20	µV/watt
Input Offset Current	$T_C = 25°C$		30	100		50	200	nA
				300			500	nA
Offset Current Drift with Temperature			0.1	1.0		0.2	1.0	nA/°C
Offset Current Drift with Time			2			2		nA/week
Input Bias Current	$T_C = 25°C$		100	300		200	500	nA
				1.0			1.0	µA
Input Resistance	$T_C = 25°C$	0.3	1.0		0.3	1.0		MΩ
Input Capacitance			3			3		pF
Common Mode Rejection Ratio	$R_S < 100\Omega$, $\Delta V_{CM} = \pm 10V$	70	90		70	90		dB
Input Voltage Range	$V_S = \pm 15V$	±12			±12			V
Power Supply Rejection Ratio	$R_S < 100\Omega$, $\Delta V_S = \pm 10V$	80	96		70	90		dB
Voltage Gain	$V_S = \pm 15V$, $V_O = \pm 10V$ $R_L = 1\,k\Omega$, $T_C = 25°C$,	100	200		100	200		V/mV
	$V_S = \pm 15V$, $V_O = \pm 10V$ $R_L = 100\Omega$,	25			20			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 100\Omega$	±13.5	14		±13	±14		V
	$V_S = \pm 15V$, $R_L = 10\Omega$, $T_C = 25°C$	±11.0	±12		±10	±12		V
Output Short Circuit Current	$V_S = \pm 15V$, $T_C = 25°C$, $R_{SC} = 0.5\Omega$	0.8	1.2	1.6	0.8	1.2	1.6	Amps
Power Supply Current	$V_S = \pm 15V$, $V_{OUT} = 0$		2.5	3.5		3.0	4.0	mA
Power Consumption	$V_S = \pm 15V$, $V_{OUT} = 0$		75	105		90	120	mW

AC Electrical Characteristics for LH0021/LH0021C ($T_A = 25°C$, $V_S = \pm 15V$, $C_C = 3000\,pF$)

PARAMETER	CONDITIONS	LH0021 MIN	LH0021 TYP	LH0021 MAX	LH0021C MIN	LH0021C TYP	LH0021C MAX	UNITS
Slew Rate	$A_V = +1$, $R_L = 100\Omega$	0.8	3.0		1.0	3.0		V/µs
Power Bandwidth	$R_L = 100\Omega$		20			20		kHz
Small Signal Transient Response			0.3	1.0		0.3	1.5	µs
Small Signal Overshoot			5	20		10	30	%
Settling Time (0.1%)	$\Delta V_{IN} = 10V$, $A_V = +1$		4			4		µs
Overload Recovery Time			3			3		µs
Harmonic Distortion	$f = 1\,kHz$, $P_O = 0.5W$		0.2			0.2		%
Input Noise Voltage	$R_S = 50\Omega$, B.W. = 10 Hz to 10 kHz		5			5		µV rms
Input Noise Current	B.W. = 10 Hz to 10 kHz		0.05			0.05		nA rms

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0041			LH0041C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 100\Omega$, $T_A = 25^\circ C$		1.0	3.0		3.0	6.0	mV
	$R_S \leq 100\Omega$			5.0			7.5	mV
Voltage Drift with Temperature	$R_S \leq 100\Omega$		3			5		$\mu V/^\circ C$
Offset Voltage Drift with Time			5			5		μV/week
Offset Voltage Change with Output Power			15			15		μV/watt
Offset Voltage Adjustment Range	(Note 5)		20			20		mV
Input Offset Current	$T_A = 25^\circ C$		30	100		50	200	nA
				300			500	nA
Offset Current Drift with Temperature			0.1	1.0		0.2	1.0	$nA/^\circ C$
Offset Current Drift with Time			2			2		nA/week
Input Bias Current	$T_A = 25^\circ C$		100	300		200	500	nA
				1.0			1.0	μA
Input Resistance	$T_A = 25^\circ C$	0.3	1.0		0.3	1.0		$M\Omega$
Input Capacitance			3			3		pF
Common Mode Rejection Ratio	$R_S \leq 100\Omega$, $\Delta V_{CM} = \pm 10V$	70	90		70	90		dB
Input Voltage Range	$V_S = \pm 15V$	±12			±12			V
Power Supply Rejection Ratio	$R_S \leq 100\Omega$, $\Delta V_S = \pm 10V$	80	96		70	90		dB
Voltage Gain	$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 1\,k\Omega$, $T_A = 25^\circ C$	100	200		100	200		V/mV
	$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 100\Omega$	25			20			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 100\Omega$	±13.0	14.0		±13.0	±14.0		V
Output Short Circuit Current	$V_S = \pm 15V$, $T_A \cdot 25^\circ C$ (Note 6)		200	300		200	300	mA
Power Supply Current	$V_S = \pm 15V$, $V_{OUT} = 0$		2.5	3.5		3.0	4.0.	mA
Power Consumption	$V_S = \pm 15V$, $V_{OUT} = 0$		75	105		90	120	mW

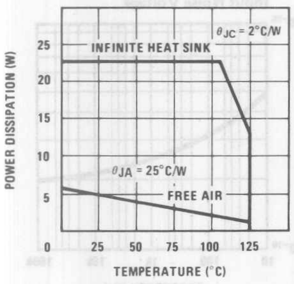
AC Electrical Characteristics for LH0041/LH0041C ($T_A = 25^\circ C$, $V_S = \pm 15V$, $C_C = 3000\,pF$)

Slew Rate	$A_V = +1$, $R_L = 100\Omega$	1.5	3.0		1.0	3.0		$V/\mu s$
Power Bandwidth	$R_L = 100\Omega$		20			20		kHz
Small Signal Transient Response			0.3	1.0		0.3	1.5	μs
Small Signal Overshoot			5	20		10	30	%
Settling Time (0.1%)	$\Delta V_{IN} = 10V$, $A_V = +1$		4			4		μs
Overload Recovery Time			3			3		μs
Harmonic Distortion	$f = 1\,kHz$, $P_O = 0.5W$		0.2			0.2		%
Input Noise Voltage	$R_S = 50\Omega$, B.W. = 10 Hz to 10 kHz		5			5		μV/rms
Input Noise Current	B.W. = 10 Hz to 10 kHz		0.05			0.05		nA/rms

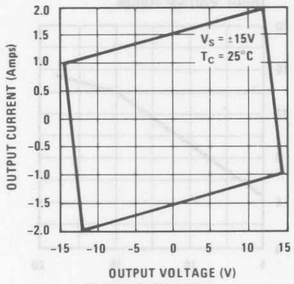
Note 1: Rating applies for supply voltages above ±15V. For supplies less than ±15V, rating is equal to supply voltage.
Note 2: Rating applies for LH0041G and LH0021K with $R_{SC} = 0\Omega$.
Note 3: Rating applies as long as package power rating is not exceeded.
Note 4: Specifications apply for $\pm 5V \leq V_S \pm 18V$, and $-55^\circ C \leq T_C = \leq 125^\circ C$ for LH0021K and LH0041G, and $-25^\circ C \leq T_C \leq +85^\circ C$ for LH0021CK, LH0041CG and LH0041CJ unless otherwise specified. Typical values are for 25°C only.
Note 5: TO-8 "G" packages only.
Note 6: Rating applies for "J" DIP package and for TO-8 "G" package with $R_{SC} = 3.3$ ohms.

Typical Performance Characteristics (Cont'd)

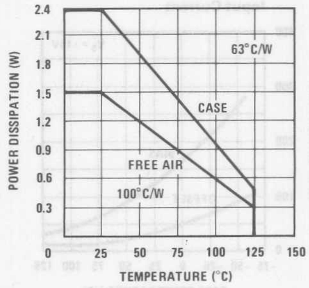
Power Derating-LH0021



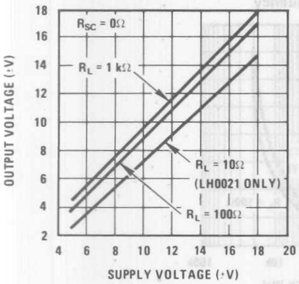
Safe Operating Area – LH0021



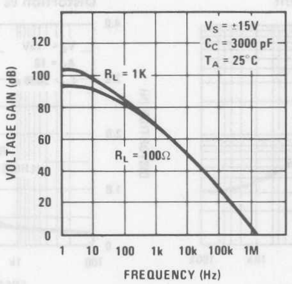
Package Power Dissipation LH0041/LH0041C



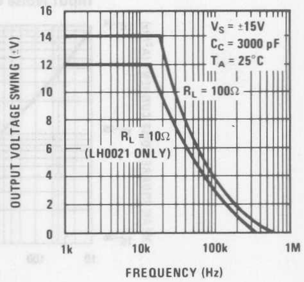
Output Voltage Swing



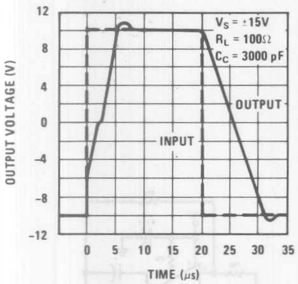
Open Loop Frequency Response



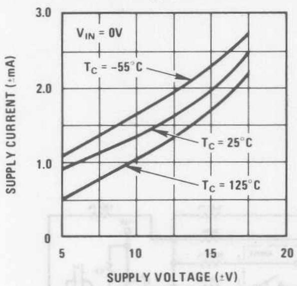
Large Signal Frequency Response



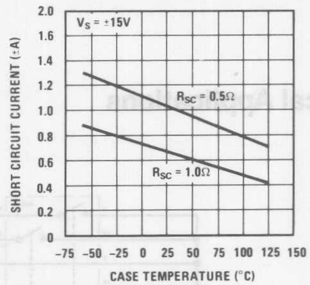
Voltage Follower Pulse Response



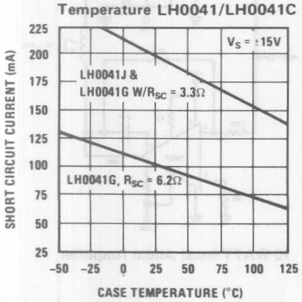
No Load Supply Current



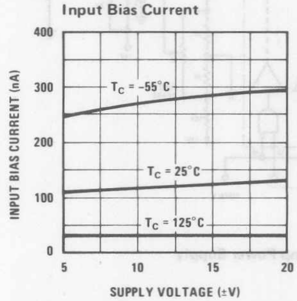
Short Circuit Current vs Temperature LH0021/LH0021C



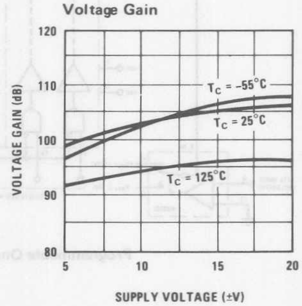
Short Circuit Current vs Temperature LH0041/LH0041C



Input Bias Current

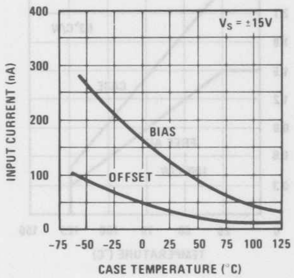


Voltage Gain

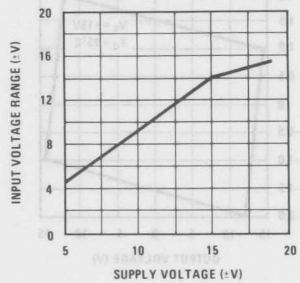


Typical Performance Characteristics (Cont'd)

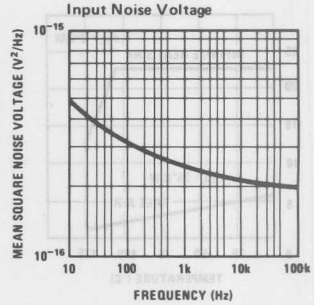
Input Current



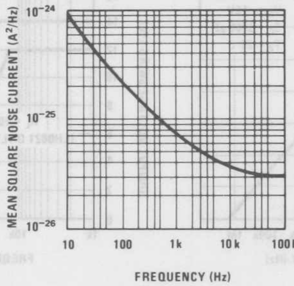
Input Voltage Range



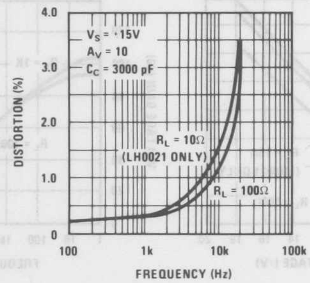
Input Noise Voltage



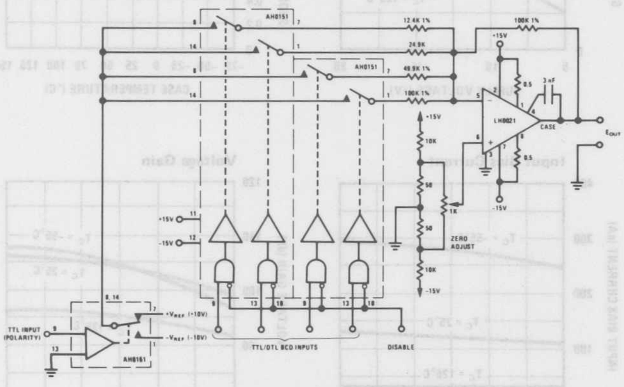
Input Noise Current



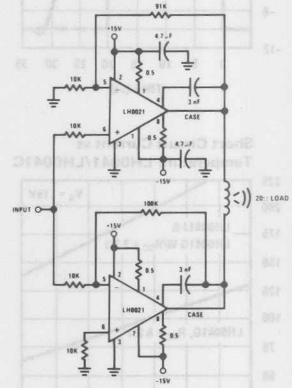
Distortion vs Frequency



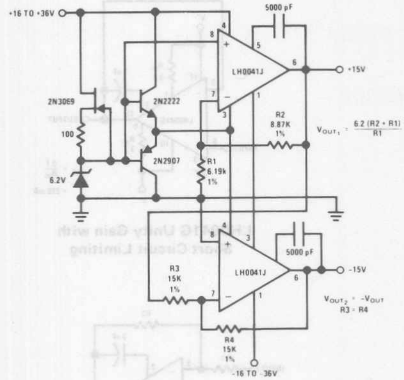
Typical Applications



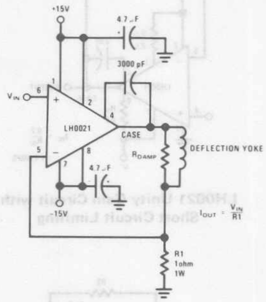
Programmable One Amp Power Supply



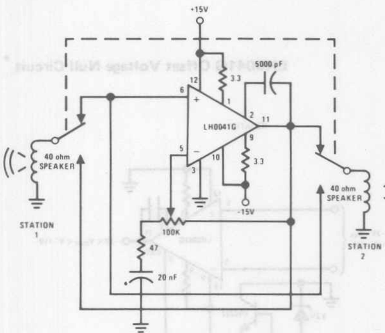
10 WATT (rms) Audio Amplifier



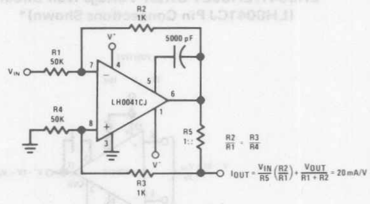
Dual Tracking One Amp Power Supply



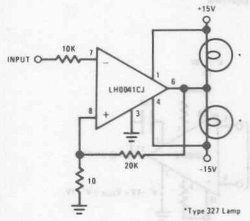
CRT Deflection Yoke Driver



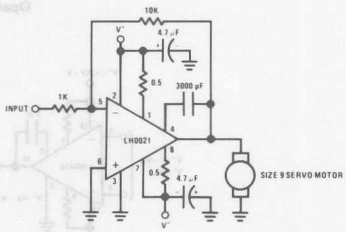
Two Way Intercom



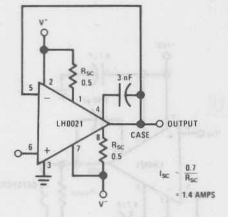
Programmable High Current Source/Sink



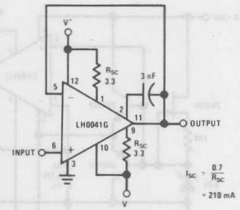
Power Comparator



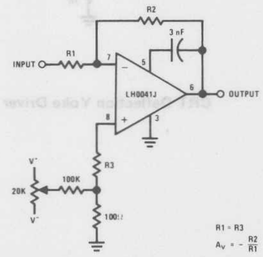
DC Servo Amplifier



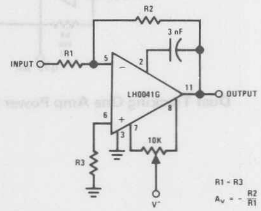
LH0021 Unity Gain Circuit with Short Circuit Limiting



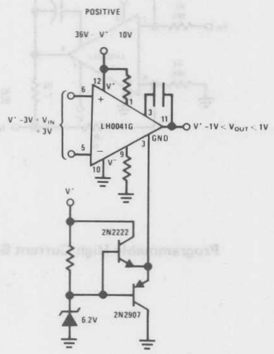
LH0041G Unity Gain with Short Circuit Limiting

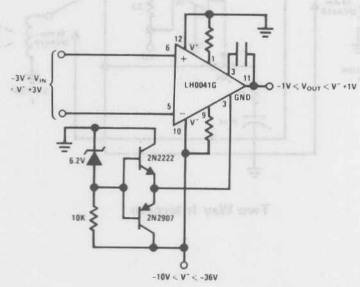


LH0041/LH0021 Offset Voltage Null Circuit (LH0041CJ Pin Connections Shown)*

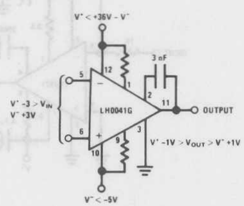


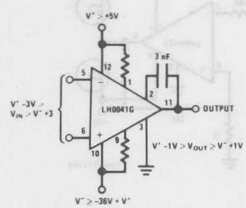
LH0041G Offset Voltage Null Circuit*





Operation from Single Supplies





Operation from Non-Symmetrical Supplies

*For additional offset null circuit techniques see National Linear Applications Handbook.

National Semiconductor

Operational Amplifiers/Buffers

LH0022/LH0022C High Performance FET Op Amp
LH0042/LH0042C Low Cost FET Op Amp
LH0052/LH0052C Precision FET Op Amp

General Description

The LH0022/LH0042/LH0052 are a family of FET input operational amplifiers with very closely matched input characteristics, very high input impedance, and ultra-low input currents with no compromise in noise, common mode rejection ratio, open loop gain, or slew rate. The internally laser nulled LH0052 offers 500 microvolts maximum offset and 5 μV/°C offset drift. Input offset current is less than 500 femtoamps at room temperature and 500 pA maximum at 125°C. The LH0022 and LH0042 are not internally nulled but offer comparable matching characteristics. All devices in the family are internally compensated and are free of latch-up and unusual oscillation problems. The devices may be offset nulled with a single 10k trimpot with neglible effect in CMRR.

The LH0022, LH0042 and LH0052 are specified for operation over the −55°C to +125°C military temperature range. The LH0022C, LH0042C and LH0052C are specified for operation over the −25°C to +85°C temperature range.

Features

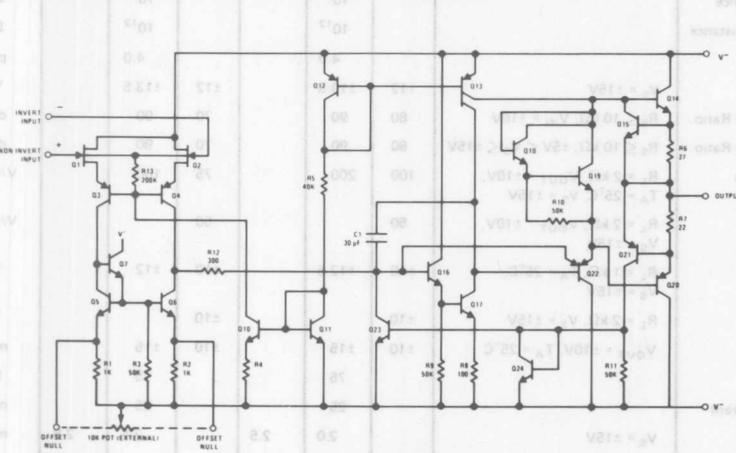
- Low input offset current − 500 femtoamps max. (LH0052)
- Low input offset drift − 5 μV/°C max (LH0052)
- Low input offset voltage − 100 microvolts-typ.
- High open loop gain − 100 dB typ.
- Excellent slew rate − 3.0 V/μs typ.
- Internal 6 dB/octave frequency compensation
- Pin compatible with standard IC op amps (TO-5 package)

The LH0022/LH0042/LH0052 family of IC op amps are intended to fulfill a wide variety of applications for process control, medical instrumentation, and other systems requiring very low input currents and tightly matched input offsets. The LH0052 is particularly suited for long term high accuracy integrators and high accuracy sample and hold buffer amplifiers. The LH0022 and LH0042 provide low cost high performance for such applications as electrometer and photocell amplification, pico-ammeters, and high input impedance buffers.

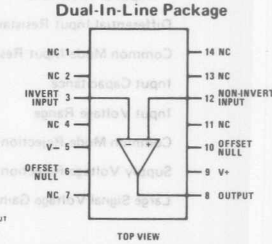
Special electrical parameter selection and custom built circuits are available on special request.

For additional application information and information on other National operational amplifiers, see *Available Linear Applications Literature.*

Schematic and Connection Diagrams



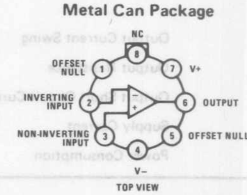
Dual-In-Line Package



TOP VIEW

Order Number LH0022D, LH0022CD, LH0042D, LH0042CD, LH0052D or LH0052CD
See Package D14E

Metal Can Package



TOP VIEW

Order Number LH0022H, LH0022CH, LH0042H, LH0042CH, LH0052H or LH0052CH
See Package H08A

*Previously Called NH0022/NH0022C

Absolute Maximum Ratings

Supply Voltage	±22V
Power Dissipation (see graph)	500 mW
Input Voltage (Note 1)	±15V
Differential Input Voltage (Note 2)	±30V
Voltage Between Offset Null and V^-	±0.5V
Short Circuit Duration	Continuous
Operating Temperature Range	
LH0022, LH0042, LH0052	−55°C to +125°C
LH0022C, LH0042C, LH0052C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

DC Electrical Characteristics for LH0022/LH0022C (Note 3)

PARAMETER	CONDITIONS	LIMITS LH0022 MIN	LH0022 TYP	LH0022 MAX	LH0022C MIN	LH0022C TYP	LH0022C MAX	UNITS
Input Offset Voltage	$R_S \leq 100\ k\Omega$; $T_A = 25°C$, $V_S = \pm15V$		2.0	4.0		3.5	6.0	mV
	$R_S \leq 100\ k\Omega$, $V_S = \pm15V$			5.0			7.0	mV
Temperature Coefficient of Input Offset Voltage	$R_S \leq 100\ k\Omega$		5	10		5	15	μV/°C
Offset Voltage Drift with Time			3			4		μV/week
Input Offset Current	(Note 4)		0.2	2.0		1.0	5.0	pA
				2.0			0.5	nA
Temperature Coefficient of Input Offset Current			Doubles every 10°C			Doubles every 10°C		
Offset Current Drift with Time			0.1			0.1		pA/week
Input Bias Current	(Note 4)		5	10		10	25	pA
				10			2.5	nA
Temperature Coefficient of Input Bias Current			Doubles every 10°C			Doubles every 10°C		
Differential Input Resistance			10^{12}			10^{12}		Ω
Common Mode Input Resistance			10^{12}			10^{12}		Ω
Input Capacitance			4.0			4.0		pF
Input Voltage Range	$V_S = \pm15V$	±12	±13.5		±12	±13.5		V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$, $V_{IN} = \pm10V$	80	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$, $\pm5V \leq V_S \leq \pm15V$	80	90		70	90		dB
Large Signal Voltage Gain	$R_L = 2\ k\Omega$, $V_{OUT} = \pm10V$, $T_A = 25°C$, $V_S = \pm15V$	100	200		75	160		V/mV
	$R_L = 2\ k\Omega$, $V_{OUT} = \pm10V$, $V_S = \pm15V$	50			50			V/mV
Output Voltage Swing	$R_L = 1\ k\Omega$, $T_A = 25°C$, $V_S = \pm15V$	±10	±12.5		±10	±12		V
	$R_L = 2\ k\Omega$, $V_S = \pm15V$	±10			±10			V
Output Current Swing	$V_{OUT} = \pm10V$, $T_A = 25°C$	±10	±15		±10	±15		mA
Output Resistance			75			75		Ω
Output Short Circuit Current			25			25		mA
Supply Current	$V_S = \pm15V$		2.0	2.5		2.4	2.8	mA
Power Consumption	$V_S = \pm15V$			75			85	mW

DC Electrical Characteristics for LH0042/LH0042C (Note 3)

Parameter	Conditions	LH0042 Min.	LH0042 Typ.	LH0042 Max.	LH0042C Min.	LH0042C Typ.	LH0042C Max.	Units
Input Offset Voltage	$R_S \leq 100 k\Omega$		5.0	20		6.0	20	mV
Temperature Coefficient of Input Offset Voltage	$R_S \leq 100 k\Omega$		5.0			10		μV/°C
Offset Voltage Drift with Time			7.0			10		μV/week
Input Offset Current	(Note 4)		1.0	5.0		2.0	10	pA
Temperature Coefficient of Input Offset Current		Doubles every 10°C			Doubles every 10°C			
Offset Current Drift with Time			0.1			0.1		pA/week
Input Bias Current	(Note 4)		10	25		15	50	pA
Temperature Coeffieient of Input Bias Current		Doubles every 10°C			Doubles every 19°C			
Differential Input Resistance			10^{12}			10^{12}		Ω
Common Mode Input Resistance			10^{12}			10^{12}		Ω
Input Capacitance			4.0			4.0		pF
Input Voltage Range		±12	±13.5		±12	±13.5		V
Common Mode Rejection Ratio	$R_S \leq 10 k\Omega$, $V_{IN} = \pm 10V$	70	86		70	80		dB
Supply Voltage Rejection Ratio	$R_S \leq 10 k\Omega$, $\pm 5V \leq V_S \leq \pm 15V$	70	86		70	80		dB
Large Signal Voltage Gain	$R_S \leq 2 k\Omega$, $V_{OUT} = \pm 10V$	50	150		25	100		V/mV
Output Voltage Swing	$R_L = 1 k\Omega$, $T_A = 25°C$	±10	±12.5		±10	±12		V
	$R_L = 2 k\Omega$	±10			±10			V
Output Current Swing	$V_{OUT} = \pm 10V$	±10	±15		±10	±15		mA
Output Resistance			75			75		Ω
Output Short Circuit Current			20			20		mA
Supply Current			2.5	3.5		2.8	4.0	mA
Power Consumption				105			120	mW

DC Electrical Characteristics For LH0052/LH0052C (Note 3)

Parameter	Conditions	LH0052 Min.	LH0052 Typ.	LH0052 Max.	LH0052C Min.	LH0052C Typ.	LH0052C Max.	Units
Input Offset Voltage	$R_S < 100 k\Omega$, $V_S = +15V$, $T_A = 25°C$		0.1	0.5		0.2	1.0	mV
	$R_S < 100 k\Omega$, $V_S = \pm 15V$			1.0			1.5	mV
Temperature Coefficient of Input Offset Voltage	$R_S \leq 100 k\Omega$, $V_S = \pm 15V$		2.0	5.0		5.0	10	μV/°C
Offset Voltage Drift with Time			2.0			4.0		μV/week
Input Offset Current	(Note 4)		0.01	5.0		0.02	1.0	pA
				500			100	pA
Temperature Coefficient of Input Offset Current		Doubles every 10°C			Doubles every 10°C			
Offset Current Drift with Time		<0.1			<0.1			pA/week
Input Bias Current	(Note 4)		0.5	2.5		1.0	5.0	pA
				2.5			0.5	nA
Temperature Coefficient of Input Bias Current		Doubles every 10°C			Doubles every 10°C			
Differential Input Resistance			10^{12}			10^{12}		Ω
Common Mode Input Resistance			10^{12}			10^{12}		Ω
Input Capacitance			4.0			4.0		pF
Input Voltage Range	$V_S = \pm 15V$	±12	±13.5		±12	±13.5		V
Common Mode Rejection Ratio	$R_S \leq 10 k\Omega$, $V_{IN} = \pm 10V$	74	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10 k\Omega$, $\pm 5V \leq V_S \leq \pm 15V$	74	90		70	90		dB
Large Signal Voltage Gain	$R_L = 2 K\Omega$, $V_{OUT} = \pm 10V$, $V_S = \pm 15V$, $T_A = 25°C$	100	200		75	160		V/mV
	$R_L = 2 k\Omega$, $V_{OUT} = \pm 10V$, $V_S = \pm 15V$	50			50			V/mV
Output Voltage Swing	$R_L = 1 k\Omega$, $T_A = 25°C$, $V_S = \pm 15V$	±10	±12.5		±10	±12		V
	$R_L = 2 k\Omega$, $V_S = \pm 15V$	±10			±10			V
Output Current Swing	$V_{OUT} = \pm 10V$, $t_A = 25°C$	±10	±15		±10	±15		mA
Output Resistance			75			75		Ω
Output Short Circuit Current			25			25		mA
Supply Current	$V_S = \pm 15V$		3.0	3.5		3.0	3.8	mA
Power Consumption	$V_S = \pm 15V$			105			114	mW

PARAMETER	CONDITIONS	LH0022/42/52 MIN	LH0022/42/52 TYP	LH0022/42/52 MAX	LH0022C/42C/52C MIN	LH0022C/42C/52C TYP	LH0022C/42C/52C MAX	UNITS
Slew Rate	Voltage Follower	1.5	3.0		1.0	3.0		V/μs
Large Signal Bandwidth	Voltage Follower		40			40		kHz
Small Signal Bandwidth			1.0			1.0		MHz
Rise Time			0.3	1.5		0.3	1.5	μs
Overshoot			10	30		15	40	%
Settling Time (0.1 %)	ΔV_{IN} = 10V		4.5			4.5		μs
Overload Recovery			4.0			4.0		μs
Input Noise Voltage	R_S = 10 kΩ, f_o = 10 Hz		150			150		nV/$\sqrt{Hz}$
Input Noise Voltage	R_S = 10 kΩ, f_o = 100 Hz		55			55		nV/$\sqrt{Hz}$
Input Noise Voltage	R_S = 10 kΩ, f_o = 1 kHz		35			35		nV/$\sqrt{Hz}$
Input Noise Voltage	R_S = 10 kΩ, f_o = 10 kHz		30			30		nV/$\sqrt{Hz}$
Input Noise Voltage	BW = 10 Hz to 10 kHz, R_S = 10 kΩ		12			12		μVrms
Input Noise Current	BW = 10 Hz to 10 kHz		<.1			<.1		pArms

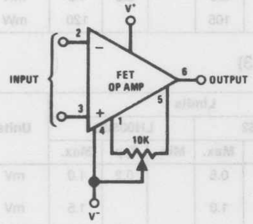
Note 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 2: Rating applies for minimum source resistance of 10 kΩ, for source resistances less than 10 kΩ, maximum differential input voltage is ±5V.

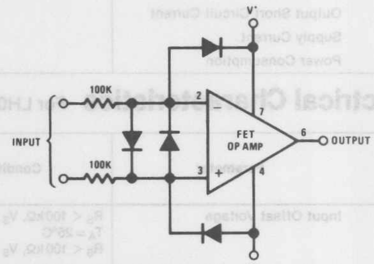
Note 3: Unless otherwise specified, these specifications apply for $\pm5V \leq V_S \leq \pm20V$ and $-55°C \leq T_A \leq +125°C$ for the LH0022 and LH0052 and $-25°C \leq T_A \leq +85°C$ for the LH0022C and LH0052C Typical values are given for $T_A = 25°C$.

Note 4: Input currents are a strong function of temperature. Due to high speed testing they are specified a junction temperature T_j = 25° C, self heating will cause an increase in current in manual tests.

Auxiliary Circuits (Shown for TO-5 pin out)

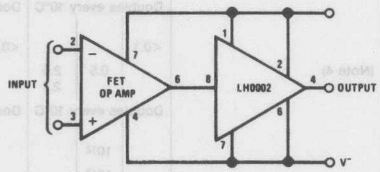


Offset Null



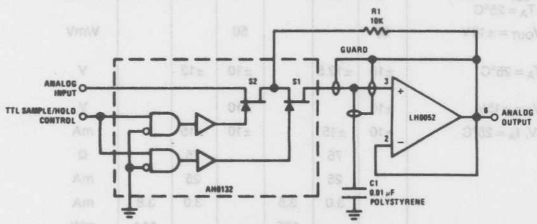
Note: All diodes are ultra low leakage

Protecting Inputs From ±150V Transients

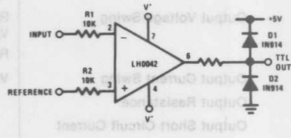


Boosting Output Drive to ±100 mA

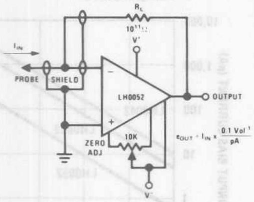
Typical Applications



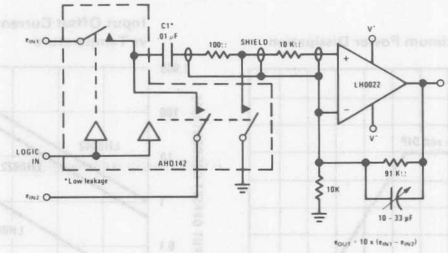
Low Drift Sample and Hold



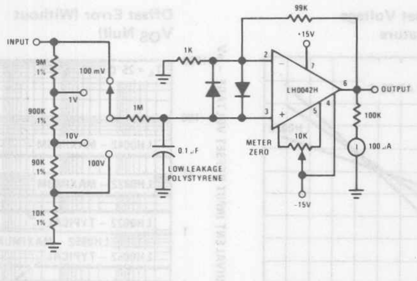
Precision Voltage Comparator



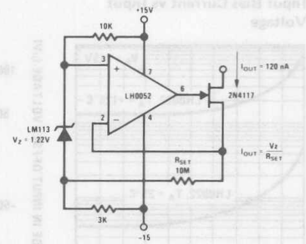
Picoamp Amplifier for pH Meters and Radiation Detectors



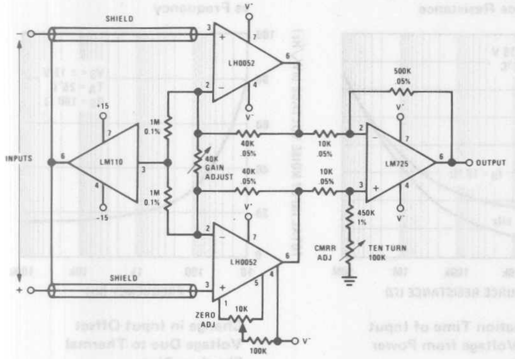
Precision Subtractor for Automatic Test Gear



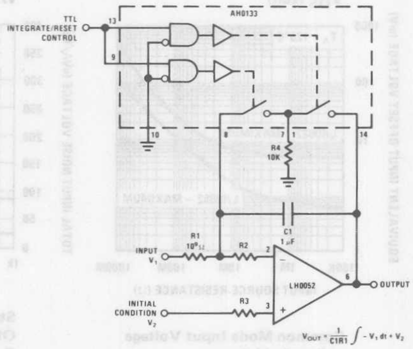
Sensitive Low Cost "VTVM"



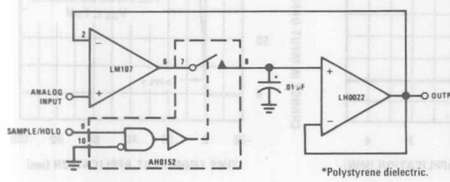
Ultra Low Level Current Source



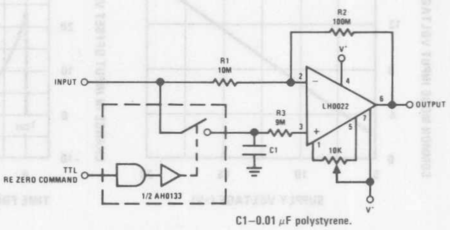
True Instrumentation Amplifier



Precision Integrator



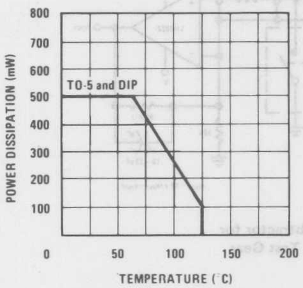
Precision Sample and Hold



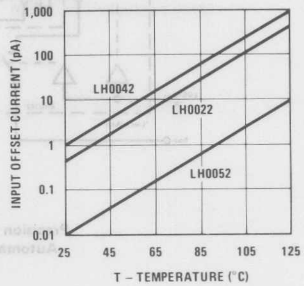
Re-Zeroing Amplifier

Typical Performance Characteristics

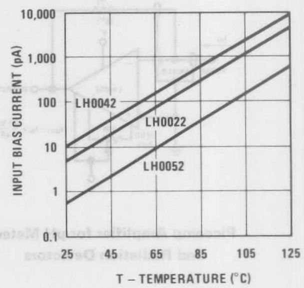
Maximum Power Dissipation



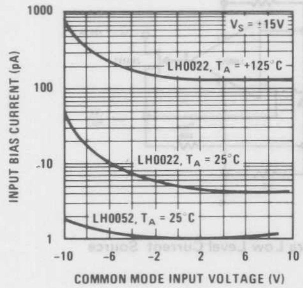
Input Offset Current vs Temperature



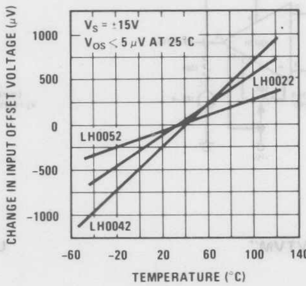
Input Bias Current vs Temperature



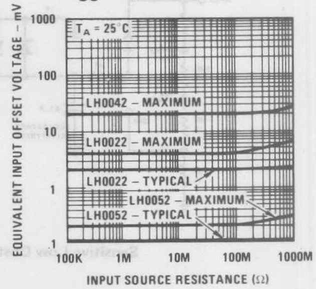
Input Bias Current vs Input Voltage



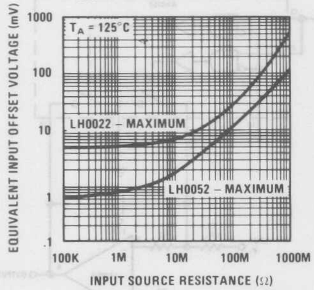
Input Offset Voltage vs Temperature



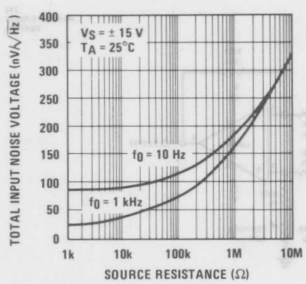
Offset Error (Without V_{OS} Null)



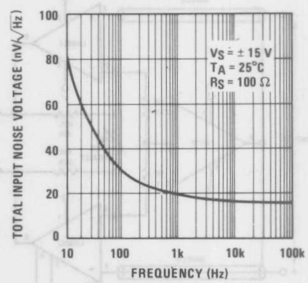
Offset Error (Without V_{OS} Null)



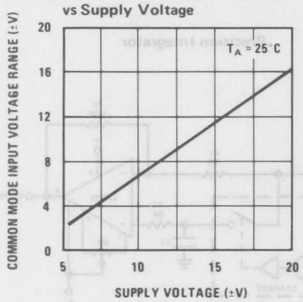
Total Input Noise Voltage* vs Source Resistance



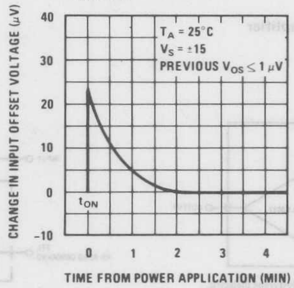
Total Input Noise Voltage* vs Frequency



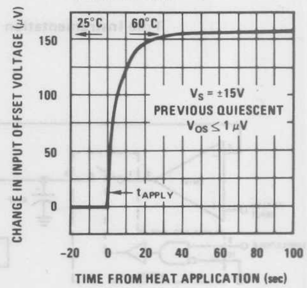
Common Mode Input Voltage vs Supply Voltage



Stabilization Time of Input Offset Voltage from Power Turn-On



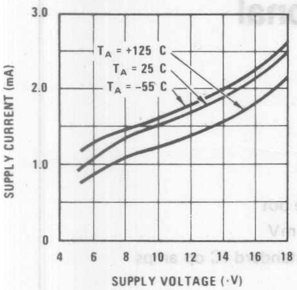
Change in Input Offset Voltage Due to Thermal Shock vs Time



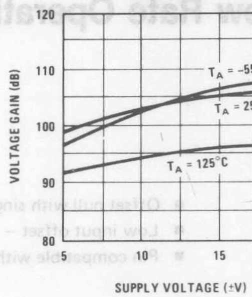
*Noise Voltage Includes Contribution from Source Resistance

Typical Performance Characteristics (Cont'd)

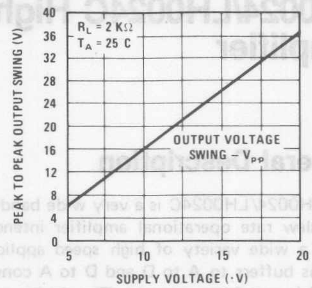
Supply Voltage vs Supply Current



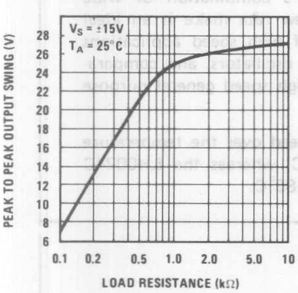
Voltage Gain



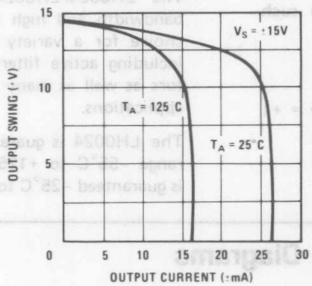
Output Swing vs Supply Voltage



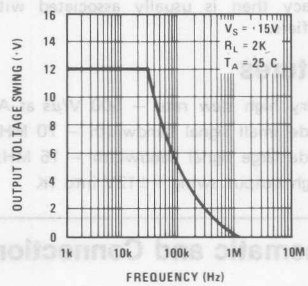
Output Voltage Swing vs Load Resistance



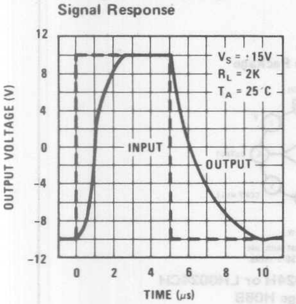
Current Limiting



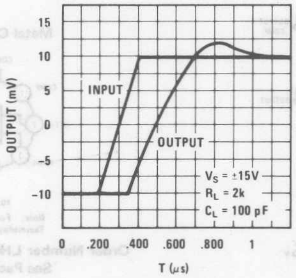
Output Voltage Swing vs Frequency



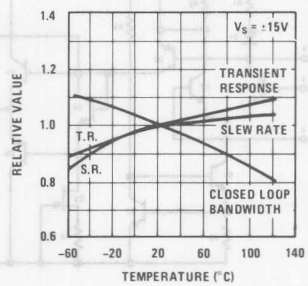
Voltage Follower Large Signal Response



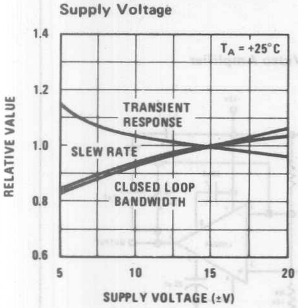
Transient Response



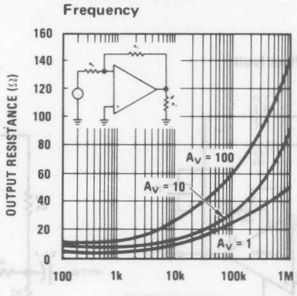
Frequency Characteristics vs Ambient Temperature



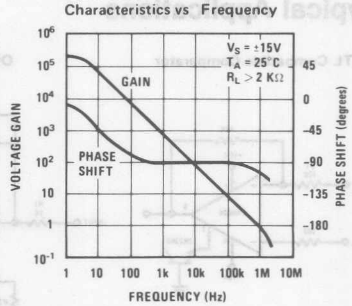
Frequency Characteristics vs Supply Voltage



Output Resistance vs Frequency



Open Loop Transfer Characteristics vs Frequency



LH0024/LH0024C High Slew Rate Operational Amplifier

General Description

The LH0024/LH0024C is a very wide bandwidth, high slew rate operational amplifier intended to fulfill a wide variety of high speed applications such as buffers to A to D and D to A converters and high speed comparators. The device exhibits useful gain in excess of 50 MHz making it possible to use in video applications requiring higher gain accuracy than is usually associated with such amplifiers.

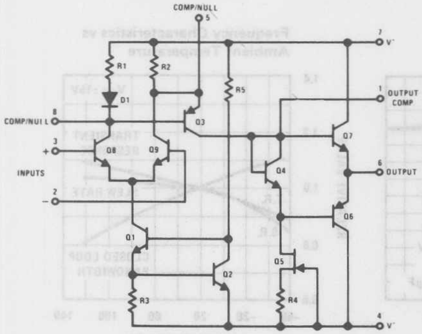
The LH0024/LH0024C's combination of wide bandwidth and high slew rate make it an ideal choice for a variety of high speed applications including active filters, oscillators, and comparators as well as many high speed general purpose applications.

The LH0024 is guaranteed over the temperature range -55°C to +125°C, whereas the LH0024C is guaranteed -25°C to +85°C.

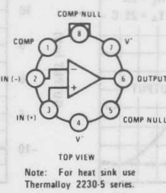
Features

- Very high slew rate — 500 V/μs at Av = +1
- Wide small signal bandwidth — 70 MHz
- Wide large signal bandwidth — 15 MHz
- High output swing — ±12V into 1K
- Offset null with single pot
- Low input offset — 2 mV
- Pin compatible with standard IC op amps

Schematic and Connection Diagrams



Metal Can Package

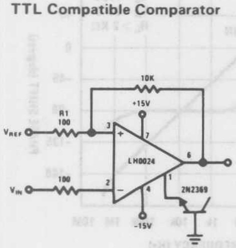


Note: For heat sink use Thermalloy 2230-5 series.

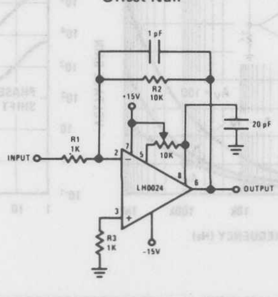
Order Number LH0024H or LH0024CH
See Package H08B

Typical Applications

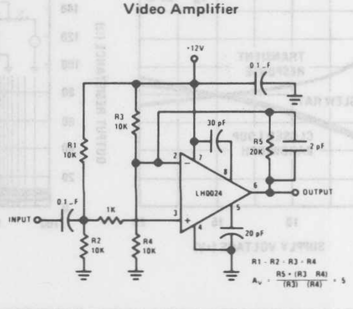
TTL Compatible Comparator



Offset Null



Video Amplifier



Supply Voltage		±18V
Input Voltage		Equal to Supply
Differential Input Voltage		±5V
Power Dissipation		600 mW
Operating Temperature Range	LH0024	-55°C to +125°C
	LH0024C	-25°C to +85°C
Storage Temperature Range		-65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

DC Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	LH0024			LH0024C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$		2.0	4.0		5.0	8.0	mV
	$R_S = 50\Omega$			6.0			10.0	mV
Average Temperature Coefficient of Input Offset Voltage	$V_S = \pm15V$, $R_S = 50\Omega$ -55°C to 125°C		−20			−25		μV/°C
Input Offset Current	$T_A = 25°C$		2.0	5.0		4.0	15.0	μA
				10.0			20.0	μA
Input Bias Current	$T_A = 25°C$		15	30		18	40	μA
				40			50	μA
Supply Current			12.5	15		12.5	15	mA
Large Signal Voltage Gain	$V_S = \pm15V$, $R_L = 1k$, $T_A = 25°C$	4	5		3	4		V/mV
	$V_S = \pm15V$, $R_L = 1k$	3			2.5			V/mV
Input Voltage Range	$V_S = \pm15V$	±12	±13		±12	±13		V
Output Voltage Swing	$V_S = \pm15V$, $R_L = 1k$, $T_A = 25°C$	±12	±13		±10	±13		V
	$V_S = \pm15V$, $R_L = 1k$	±10			±10			V
Slew Rate	$V_S = \pm15V$, $R_L = 1k$, $C_1 = C_2 = 30$ pF $A_V = +1$, $T_A = 25°C$	400	500		250	400		V/μs
Common Mode Rejection Ratio	$V_S = \pm15V$, $\Delta V_{IN} = \pm10V$ $R_S = 50\Omega$		60			60		dB
Power Supply Rejection Ratio	$\pm5V \le V_S \le \pm18V$ $R_S = 50\Omega$		60			60		dB

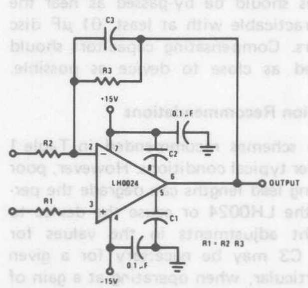
Note 1: These specifications apply for $V_S = \pm15V$ and −55°C to +125°C for the LH0024 and −25°C to +85°C for the LH0024C.

Frequency Compensation

TABLE I

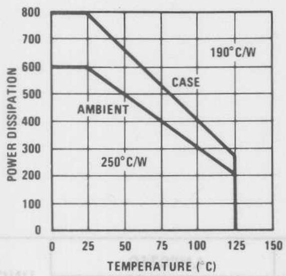
CLOSED LOOP GAIN	C_1	C_2	C_3
100	0	0	0
20	0	0	0
10	0	20 pF	1 pF
1	30 pF	30 pF	3 pF

Frequency Compensation Circuit

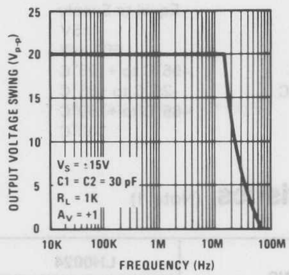


Typical Performance Characteristics

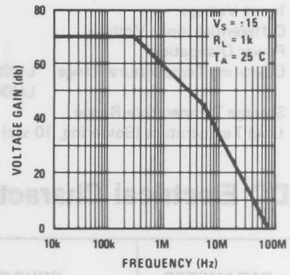
Maximum Power Dissipation



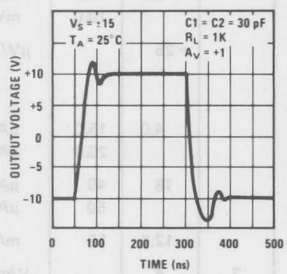
Large Signal Frequency Response



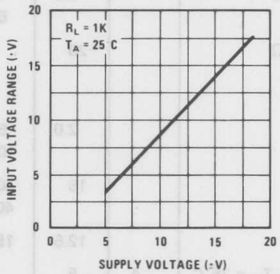
Open Loop Frequency Response



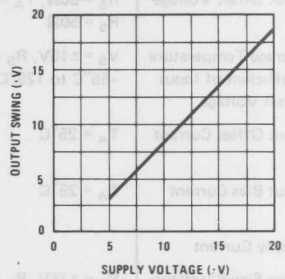
Voltage Follower Pulse Response



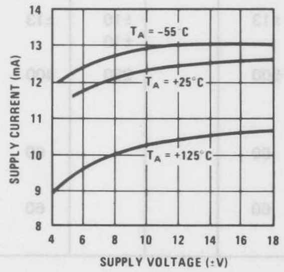
Input Voltage vs Supply Voltage



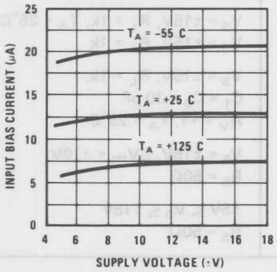
Output Voltage Swing



Supply Current vs Supply Voltage



Input Bias Current vs Voltage



Applications Information

1. Layout Considerations

The LH0024/LH0024C, like most high speed circuitry, is sensitive to layout and stray capacitance. Power supplies should be by-passed as near the device as is practicable with at least .01 μF disc type capacitors. Compensating capacitors should also be placed as close to device as possible.

2. Compensation Recommendations

Compensation schemes recommended in Table 1 work well under typical conditions. However, poor layout and long lead lengths can degrade the performance of the LH0024 or cause the device to oscillate. Slight adjustments in the values for C1, C2, and C3 may be necessary for a given layout. In particular, when operating at a gain of −1, C3 may require adjustment in order to perfectly cancel the input capacitance of the device.

When operating the LH0024/LH0024C at a gain of +1, the value of R1 should be at least 1K ohm.

The case of the LH0024 is electrically isolated from the circuit; hence, it may be advantageous to drive the case in order to minimize stray capacitances.

3. Heat Sinking

The LH0024/LH0024C is specified for operation without the use of an explicit heat sink. However, internal power dissipation does cause a significant temperature rise. Improved offset voltage drift can be obtained by limiting the temperature rise with a clip-on heat sink such as the Thermalloy 2228B or equivalent.

National Semiconductor

Operational Amplifiers/Buffers

LH0032/LH0032C Ultra Fast FET Operational Amplifier

General Description

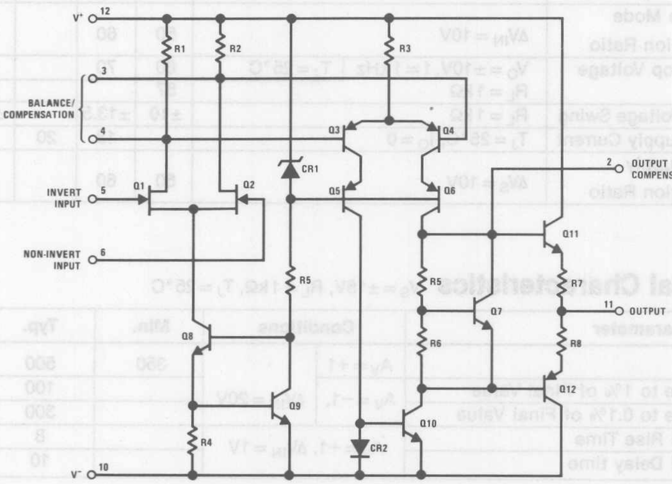
The LH0032/LH0032C is a high slew rate, high input impedance differential operational amplifier suitable for diverse application in fast signal handling. The high allowable differential input voltage, ease of output clamping, and high output drive capability particularly suit it for comparator applications. It may be used in applications normally reserved for video amplifiers allowing the use of operational gain setting and frequency response shaping into the megahertz region.

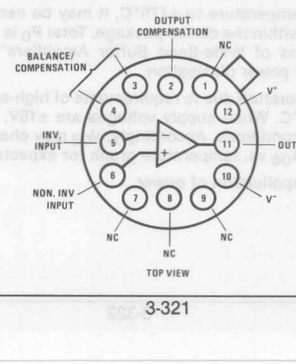
Features

- 500 V/μs slew rate
- 70 MHz bandwidth
- $10^{12}\Omega$ input impedance
- 5 mV max. input offset voltage
- FET input
- Offset null with single pot
- No compensation for gains above 50
- Peak output current to 100 mA

The LH0032's wide bandwidth, high input impedance and high output capacity make it an ideal choice for applications such as summing amplifiers in high speed D to A's, buffers in data acquisition systems, and sample and hold circuits. Additional applications include high speed integrators and video amplifiers. The LH0032 is guaranteed over the temperature range −55°C to +125°C and the LH0032C is guaranteed from −25°C to +85°C.

Schematic and Connection Diagrams





Order Number LH0032G or LH0032CG
See NS Package H12B

Differential Input Voltage	±30V or $\pm 2V_S$
Power Dissipation, P_D	
$T_A = 25°C$	1.5W, derate 100°C/W to 125°C (Note 1)
$T_C = 25°C$	2.2W, derate 70°C/W to 125°C (Note 1)
Operating Temperature Range, T_A	
LH0032G	−55°C to +125°C
LH0032CG	−25°C to +85°C
Operating Junction Temperature, T_J	175°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 seconds)	300°C

DC Electrical Characteristics $V_S = \pm 15V$, $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise noted

Parameter		Test Conditions		LH0032G			LH0032CG			Units
				Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OS}	Input Offset Voltage	$T_A = T_J = 25°C$ (Note 2)			2	5		2	15	mV
						10			20	
$\Delta V_{OS}/\Delta T$	Average Offset Voltage Drift				25			25		µV/°C
I_{OS}	Input Offset Current	$V_{IN} = 0$	$T_J = 25°C$ (Note 2)			25			50	pA
			$T_A = 25°C$ (Note 3)			250			500	pA
			$T_J = T_A = T_{MAX}$			25			5	nA
I_B	Input Bias Current		$T_J = 25°C$ (Note 2)			100			500	pA
			$T_A = 25°C$ (Note 3)			1			5	nA
			$T_J = T_A = T_{MAX}$			50			15	nA
V_{INCM}	Input Voltage Range			±10	±12		±10	±12		V
CMRR	Common Mode Rejection Ratio	$\Delta V_{IN} = 10V$		50	60		50	60		dB
A_{VOL}	Open-Loop Voltage Gain	$V_O = \pm 10V$, $f = 1\,kHz$	$T_J = 25°C$	60	70		60	70		dB
		$R_L = 1\,k\Omega$		57			57			
V_O	Output Voltage Swing	$R_L = 1\,k\Omega$		±10	±13.5		±10	±13		V
I_S	Power Supply Current	$T_J = 25°C$, $I_O = 0$			18	20		20	22	mA
PSRR	Power Supply Rejection Ratio	$\Delta V_S = 10V$		50	60		50	60		dB

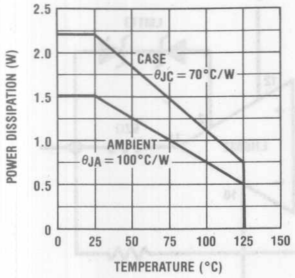
AC Electrical Characteristics $V_S = \pm 15V$, $R_L = 1\,k\Omega$, $T_J = 25°C$

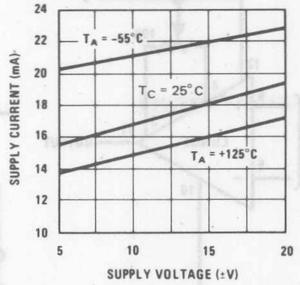
Parameter		Conditions		Min.	Typ.	Max.	Units
S_R	Slew Rate	$A_V = +1$	$\Delta V_{IN} = 20V$	350	500		V/µs
t_S	Settling Time to 1% of Final Value	$A_V = -1$,	$\Delta V_{IN} = 20V$		100		ns
t_S	Settling Time to 0.1% of Final Value	$A_V = -1$,	$\Delta V_{IN} = 20V$		300		ns
t_R	Small Signal Rise Time	$A_V = +1$, $\Delta V_{IN} = 1V$			8	20	ns
t_D	Small Signal Delay time	$A_V = +1$, $\Delta V_{IN} = 1V$			10	25	ns

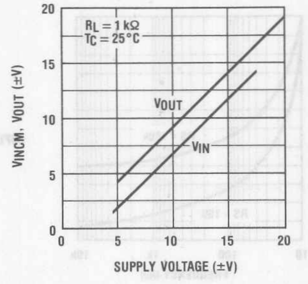
Note 1: In order to limit maximum junction temperature to +175°C, it may be necessary to operate with $V_S < \pm 15V$ when T_A or T_C exceeds specific values depending on the P_D within the device package. Total P_D is the sum of quiescent and load-related dissipation. See Applications Notes AN277, "Applications of Wide-Band Buffer Amplifiers" and AN253, "High-Speed Operational-Amplifier Applications" for a discussion of load-related power dissipation.

Note 2: Specification is at 25°C junction temperature due to requirements of high-speed automatic testing. Actual values at operating temperature will exceed the value at $T_J = 25°C$. When supply voltages are ±15V, no-load operating junction temperature may rise 40-60°C above ambient and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_B and I_{OS} will change significantly during warm-up. Refer to I_B and I_{OS} vs. temperature graph for expected values.

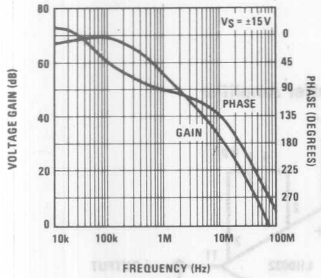
Note 3: Measured in still air 7 minutes after application of power.



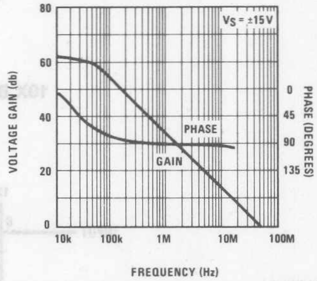




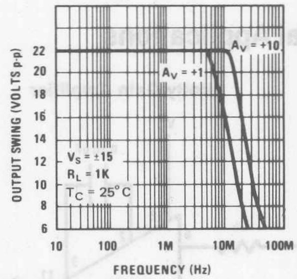
Bode Plot (Uncompensated)



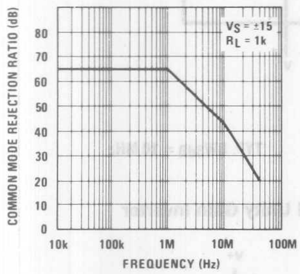
Bode Plot (Unity Gain Compensation)



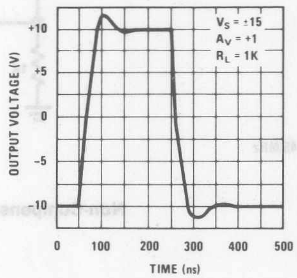
Large Signal Frequency Response



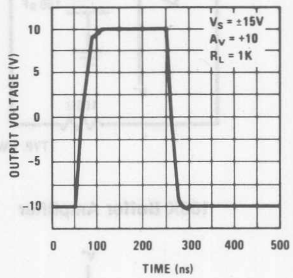
Common Mode Rejection Ratio vs. Frequency



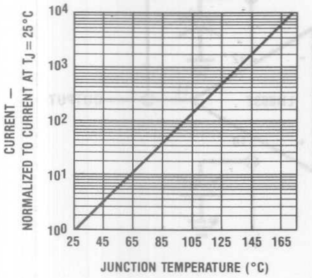
Large Signal Pulse Response



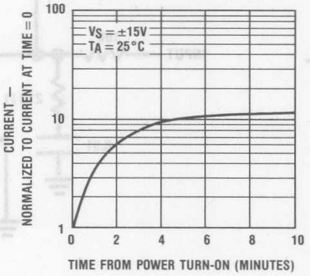
Large Signal Pulse Response



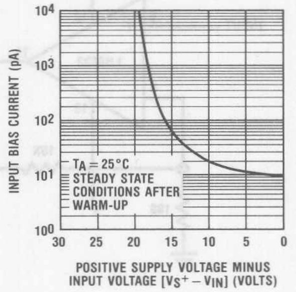
Normalized Input Bias and Offset Current vs. Junction Temperature



Normalized Input Bias Current During Warm-Up

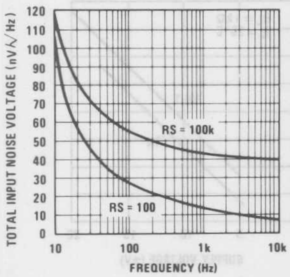


Input Bias Current vs. Input Voltage



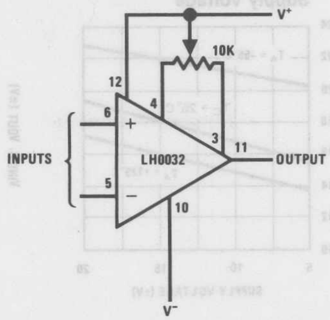
Auxiliary Circuits

Total Input Noise Voltage vs. Frequency*

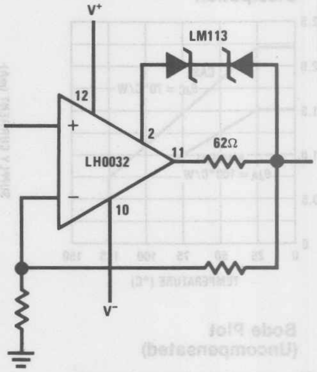


* Noise voltage includes contribution from source resistance.

Offset Null

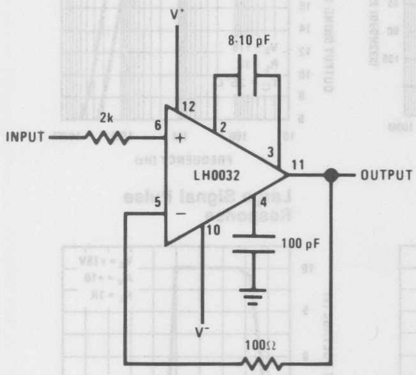


Output Short Circuit Protection



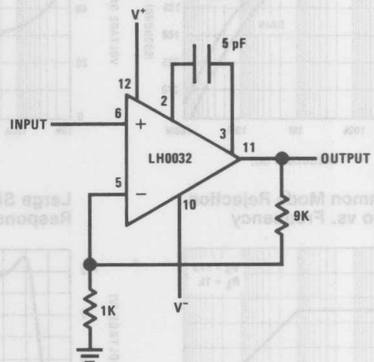
Typical Applications

Unity Gain Amplifier



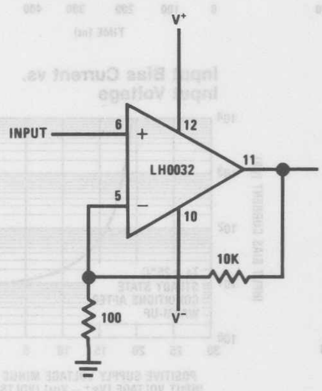
TYP. $BW_{3dB} = 45$ MHz

10X Buffer Amplifier



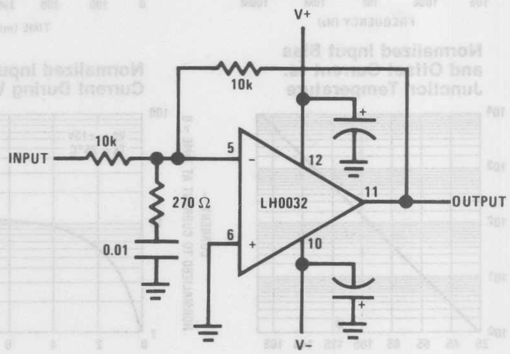
TYP. $BW_{3dB} = 10$ MHz

100X Buffer Amplifier



TYP. $BW_{3dB} = 5$ MHz

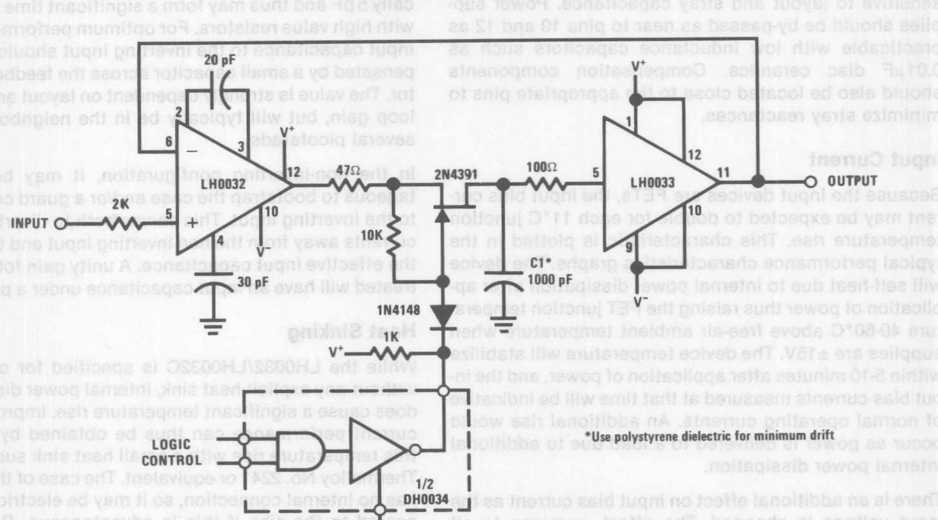
Non-Compensated Unity Gain Inverter



TYP. $BW_{3dB} = 70$ MHz

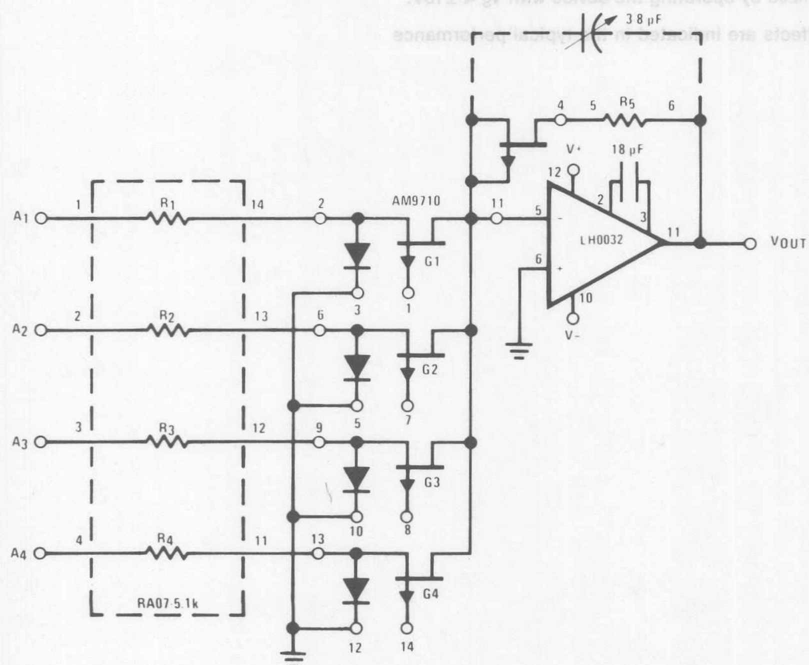
Typical Applications (cont'd)

High Speed Sample and Hold



*Use polystyrene dielectric for minimum drift

High Speed Current Mode MUX



Power Supply Decoupling

The LH0032/LH0032C, like most high speed circuits, is sensitive to layout and stray capacitance. Power supplies should be by-passed as near to pins 10 and 12 as practicable with low inductance capacitors such as 0.01 μF disc ceramics. Compensation components should also be located close to the appropriate pins to minimize stray reactances.

Input Current

Because the input devices are FETs, the input bias current may be expected to double for each 11°C junction temperature rise. This characteristic is plotted in the typical performance characteristics graphs. The device will self-heat due to internal power dissipation after application of power thus raising the FET junction temperature 40-60°C above free-air ambient temperature when supplies are ±15V. The device temperature will stabilize within 5-10 minutes after application of power, and the input bias currents measured at that time will be indicative of normal operating currents. An additional rise would occur as power is delivered to a load due to additional internal power dissipation.

There is an additional effect on input bias current as the input voltage is changed. The effect, common to all FETs, is an avalanche-like increase in gate current as the FET gate-to-drain voltage is increased above a critical value depending on FET geometry and doping levels. This effect will be noted as the input voltage of the LH0032 is taken below ground potential when the supplies are ±15V. All of the effects described here may be minimized by operating the device with $V_S \leqslant \pm 15V$.

These effects are indicated in the typical performance curves.

Input Capacitance

The input capacitance to the LH0032/LH0032C is typically 5 pF and thus may form a significant time constant with high value resistors. For optimum performance, the input capacitance to the inverting input should be compensated by a small capacitor across the feedback resistor. The value is strongly dependent on layout and closed loop gain, but will typically be in the neighborhood of several picofarads.

In the non-inverting configuration, it may be advantageous to bootstrap the case and/or a guard conductor to the inverting input. This serves both to divert leakage currents away from the non-inverting input and to reduce the effective input capacitance. A unity gain follower so treated will have an input capacitance under a picofarad.

Heat Sinking

While the LH0032/LH0032C is specified for operation without any explicit heat sink, internal power dissipation does cause a significant temperature rise. Improved bias current performance can thus be obtained by limiting this temperature rise with a small heat sink such as the Thermalloy No. 2241 or equivalent. The case of the device has no internal connection, so it may be electrically connected to the sink if this is advantageous. Be aware, however, that this will affect the stray capacitances to all pins and may thus require adjustment of circuit compensation values.

For additional applications information see Application Note AN-253.

National Semiconductor

Operational Amplifiers/Buffers

LH0033/LH0033C, LH0063/LH0063C Fast and Damn Fast Buffer Amplifiers

General Description

The LH0033/LH0033C and LH0063/LH0063C are high speed, FET input, voltage follower/buffers designed to provide high current drive at frequencies from DC to over 100 MHz. The LH0033/LH0033C will provide ±10 mA into 1 kΩ loads (±100 mA peak) at slew rates of 1500V/μs. The LH0063/LH0063C will provide ±250 mA into 50Ω loads (±500 mA peak) at slew rates of up to 6000V/μs. In addition, both exhibit excellent phase linearity up to 20 MHz.

Both are intended to fulfill a wide range of buffer applications such as high speed line drivers, video impedance transformation, nuclear instrumentation amplifiers, op amp isolation buffer for driving reactive loads and high impedance input buffers for high speed A to D's and comparators. In addition, the LH0063/LH0063C can continuously drive 50Ω coaxial cables or be used as a diddle yoke driver for high resolution CRT displays. For additional applications information, see AN-48.

Advantages

- Only +10V supply needed for 5 $V_{P\text{-}P}$ video out
- Speed does not degrade system performance
- Wide data rate range for phase encoded systems
- Output drive adequate for most loads
- Single pre-calibrated package

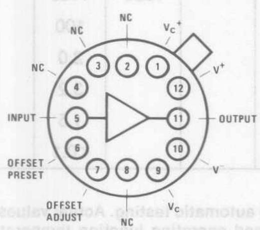
Features

- Damn fast (LH0063) 6000V/μs
- Wide range single or dual supply operation
- Wide power bandwidth DC to 100 MHz
- High output drive ±10V with 50Ω load
- Low phase non-linearity 2 degrees
- Fast rise times 2 ns
- High current gain 120 dB
- High input resistance 10^{10} Ω

These devices are constructed using specially selected junction FET's and active laser trimming to achieve guaranteed performance specifications. The LH0033 and LH0063 are specified for operation from −55°C to +125°C; whereas, the LH0033C and LH0063C are specified from −25°C to +85°C. The LH0033/LH0033C is available in a 1.5W metal TO-8 package and a special 1/2 x 1 inch 8 pin ceramic dual-in-line package while the LH0063/LH0063C is available in a 5W 8-pin TO-3 package.

Connection Diagrams

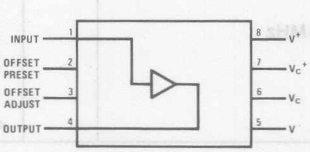
Metal Can Package



TOP VIEW
CASE IS ELECTRICALLY ISOLATED

Order Number LH0033G or LH0033CG
See Package H12B

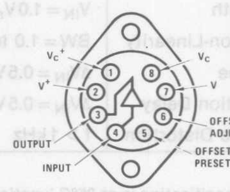
Dual-In-Line Package



TOP VIEW

Order Number LH0033J or LH0033CJ
See Package HY08A

Metal Can Package



TOP VIEW
CASE IS ELECTRICALLY ISOLATED

Order Number LH0063K or LH0063CK
See Package K08A

Absolute Maximum Ratings

Supply Voltage ($V^+ - V^-$)	40V
Maximum Power Dissipation (See Curves)	
LH0063/LH0063C	5W
LH0033/LH0033C	1.5W
Maximum Junction Temperature	175°C
Input Voltage	Equal to Supplies
Continuous Output Current	
LH0063/LH0063C	±250 mA
LH0033/LH0033C	±100 mA
Peak Output Current	
LH0063/LH0063C	±500 mA
LH0033/LH0033C	±250 mA
Operating Temperature Range	
LH0033 and LH0063	−55°C to +125°C
LH0033C and LH0063C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

DC Electrical Characteristics $V_S = \pm 15V$, $T_{MIN} \leqslant T_A \leqslant T_{MAX}$ unless otherwise specified

Parameter	Conditions	Limits LH0033 Min.	Typ.	Max.	LH0033C Min.	Typ.	Max.	Units
Output Offset Voltage	$R_S = 100\Omega$, $T_J = 25°C$, $V_{IN} = 0V$ (see note 1)		5.0	10		12	20	mV
	$R_S = 100\Omega$			15			25	mV
Average Temperature Coefficient of Offset Voltage	$R_S = 100\Omega$, $V_{IN} = 0V$		50			50		μV/°C
Input Bias Current	$V_{IN} = 0V$ $T_J = 25°C$ (Note 1)			250			500	pA
	$T_A = 25°C$ (Note 2)			2.5			5.0	nA
	$T_J = T_A = T_{MAX}$			10			20	nA
Voltage Gain	$V_O = \pm 10V$, $R_S = 100\Omega$, $R_L = 1.0k\Omega$	0.97	0.98	1.00	0.96	0.98	1.00	V/V
Input Impedance	$R_L = 1k\Omega$	10^{10}	10^{11}		10^{10}	10^{11}		Ω
Output Impedance	$V_{IN} = \pm 1.0V$, $R_L = 1.0k$		6.0	10		6.0	10	Ω
Output Voltage Swing	$V_I = \pm 14V$, $R_L = 1.0k$	±12			±12			V
	$V_I = \pm 10.5V$, $R_L = 100\Omega$, $T_A = 25°C$	±9.0			±9.0			V
Supply Current	$V_{IN} = 0V$		20	22		21	24	mA
Power Consumption	$V_{IN} = 0V$		600	660		630	720	mW

Note 1 is Note 2 of LH0032

Note 2 is Note 3 of LH0032

AC Electrical Characteristics $T_C = 25°C$, $V_S = \pm 15V$, $R_S = 50\Omega$, $R_L = 1.0k\Omega$

Parameter	Conditions	Limits LH0033 Min.	Typ.	Max.	LH0033C Min.	Typ.	Max.	Units
Slew Rate	$V_{IN} = \pm 10V$	1000	1500		1000	1400		V/μs
Bandwidth	$V_{IN} = 1.0V_{rms}$		100			100		MHz
Phase Non-Linearity	BW = 1.0 to 20 MHz		2.0			2.0		degrees
Rise Time	$\Delta V_{IN} = 0.5V$		2.9			3.2		ns
Propagation Delay	$\Delta V_{IN} = 0.5V$		1.2			1.5		ns
Harmonic Distortion	$f > 1kHz$		<0.1			<0.1		%

Note 1: Specification is at 25°C junction temperature due to requirements of high-speed automatic testing. Actual values at operating temperature will exceed the value at $T_J = 25°C$. When supply voltages are ±15V, no-load operating junction temperature may rise 40-60°C above ambient and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_B will change significantly during warm-up. Refer to I_B vs. temperature graph for expected values.

Note 2: Measured in still air 7 minutes after application of power.

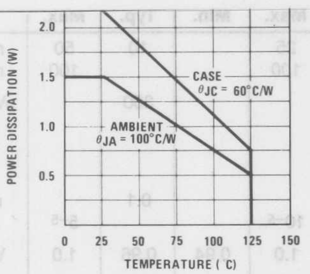
DC Electrical Characteristics $V_S = \pm 15V$, $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified

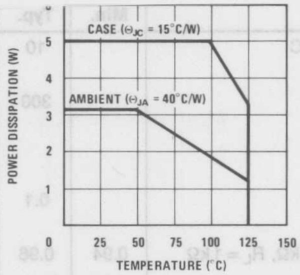
Parameter	Conditions	Limits LH0063 Min.	LH0063 Typ.	LH0063 Max.	LH0063C Min.	LH0063C Typ.	LH0063C Max.	Units
Output Offset	$R_S \leq 100\,k\Omega$, $T_J = 25°C$		10	25		10	50	mV
	$R_L = 100\,\Omega$			100			100	mV
Average Temperature Coefficient of Output Offset Voltage	$R_S \leq 100\,k\Omega$		300			300		μV/°C
Input Bias Current	$T_J = 25°C$		0.1	10^{-5}		0.1	5^{-5}	nA
Voltage Gain	$V_{IN} = \pm 10V$, $R_S \leq 100\,k\Omega$, $R_L = 1\,k\Omega$	0.94	0.96	1.0	0.94	0.96	1.0	V/V
Voltage Gain	$V_{IN} = \pm 10V$, $R_S \leq 100\,k\Omega$, $R_L = 50\,\Omega$, $T_J = 25°C$	0.92	0.93	0.98	0.91	0.93	0.98	V/V
Input Capacitance	Case Shorted to Output		8.0			8.0		pF
Output Impedance	$V_{OUT} = \pm 10V$, $R_S \leq 100\,k\Omega$, $R_L = 50\,\Omega$		1.0	4.0		1.0	4.0	Ω
Output Current Swing	$V_{IN} = \pm 10V$, $R_S \leq 100\,k\Omega$	0.2	0.25		0.2	0.25		Amps
Output Voltage Swing	$R_L = 50\,\Omega$	±10	±13		±10	±13		V
Output Voltage Swing	$V_S = \pm 5.0V$, $R_L = 50\,\Omega$, $T_J = 25°C$	5.0	7.0		5.09	7.0		V
Supply Current	$T_J = 25°C$, $R_L = \infty$, $V_S = \pm 15V$		35	65		35	65	mA
Supply Current	$V_S = \pm 5.0V$		50			50		mA
Power Consumption	$T_J = 25°C$, $R_L = \infty$, $V_S = \pm 15V$		1.05	1.95		1.05	1.95	W
Power Consumption	$V_S = \pm 5.0V$		500			500		mW

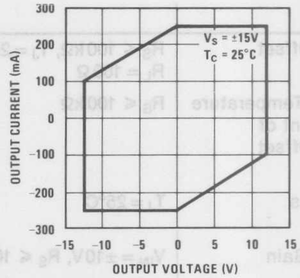
AC Electrical Characteristics LH0063/LH0063C ($T_J = 25°C$, $V_S = \pm 15V$, $R_S = 50\,k\Omega$, $R_L = 50\,\Omega$)

Parameter	Conditions	Limits LH0063 Min.	LH0063 Typ.	LH0063 Max.	LH0063C Min.	LH0063C Typ.	LH0063C Max.	Units
Slew Rate	$R_L = 1.0\,k\Omega$, $V_{IN} = \pm 10V$		6000			6000		V/μs
Slew Rate	$R_L = 50\,\Omega$, $V_{IN} = \pm 10V$, $T_J = 25°C$	2000	2400		2000	2400		V/μs
Bandwidth	$V_{IN} = 1.0\,V_{rms}$		200			200		MHz
Phase Non-Linearity	BW = 1.0 to 20 MHz		2.0			2.0		degrees
Rise Time	$\Delta V_{IN} = 0.5V$		1.6			1.9		ns
Propagation Delay	$\Delta V_{IN} = 0.5V$		1.9			2.1		ns
Harmonic Distortion			<0.1			<0.1		%

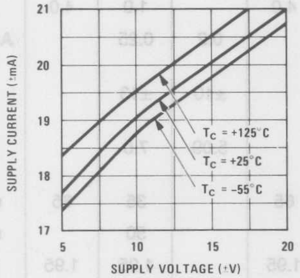
Note 1: Unless otherwise specified, these specifications apply for +15V applied to pins 1 and 12, −15V applied to pins 9 and 10, and pin 6 shorted to pin 7 for the LH0033/LH0033C. For the LH0063/LH0063C, specifiications apply for +15V applied to pins 1 and 2, −15V applied to pins 7 and 8, and pin 5 shorted to pin 6. Unless otherwise noted, specifications apply over a temperature range of $-55°C \leq T_J \leq +125°C$ for the LH0033 and LH0063; and $-25°C \leq T_J \leq +85°C$ for the LH0033C and LH0063C. Typical values shown are for $T_J = 25°C$.



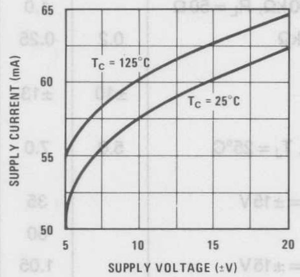




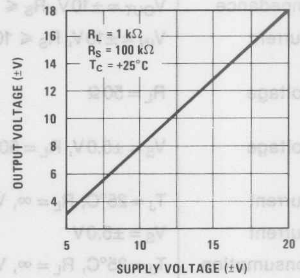
LH0033 Supply Current vs Supply Voltage



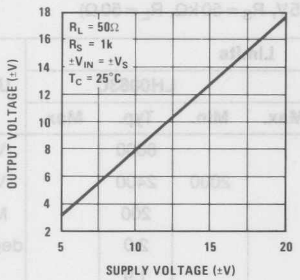
LH0063 Supply Current vs Supply Voltage



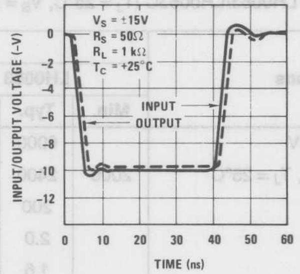
LH0033 Output Voltage vs Supply Voltage



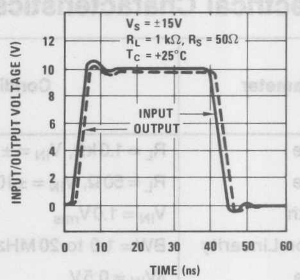
LH0063 Output Voltage vs Supply Voltage



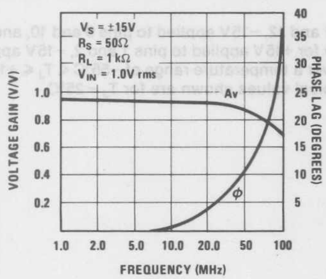
LH0033 Negative Pulse Response



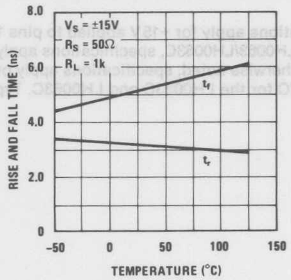
LH0033 Positive Pulse Response



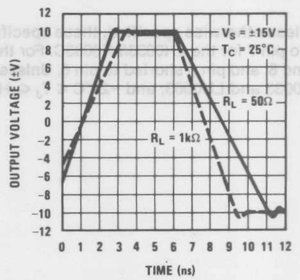
LH0033 Frequency Response



LH0033 Rise and Fall Time vs Temperature

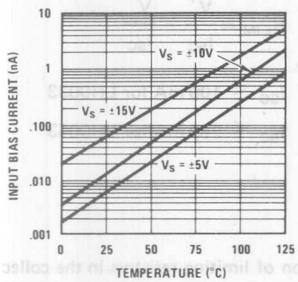


LH0063 Large Signal Pulse Response

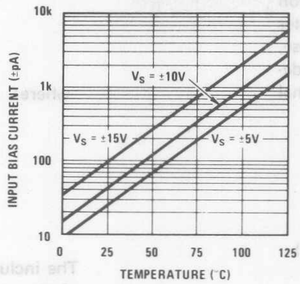


Typical Performance Characteristics (continued)

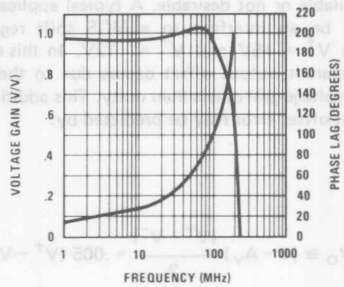
LH0033 Input Bias Current vs Temperature



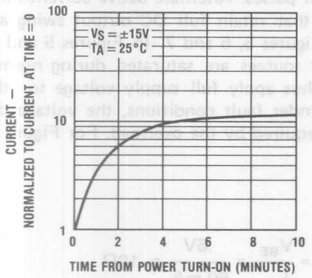
LH0063 Input Current



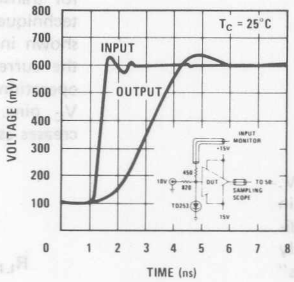
LH0063 Frequency Response



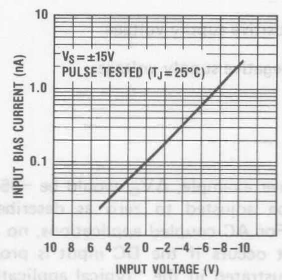
LH0033 Normalized Input Bias Current During Warm-up



LH0063 Small Signal Rise Time



LH0033 Input Bias Current vs Input Voltage



Application Hints

Recommended Layout Precautions: RF/video printed circuit board layout rules should be followed when using the LH0033 and LH0063 since they will provide power gain to frequencies over 100 MHz. Ground planes are recommended and power supplies should be decoupled at each device with low inductance capacitors. In addition, ground plane shielding may be extended to the metal case of the device since it is electrically isolated from internal circuitry. Alternatively the case should be connected to the output to minimize input capacitance.

Offset Voltage Adjustment: Both the LH0033's and LH0063's offset voltages have been actively trimmed by laser to meet guaranteed specifications when the offset preset pin is shorted to the offset adjust pin. This pre-calibration allows the devices to be used in most DC or AC applications without individually offset nulling each device. If offset null is desirable, it is simply obtained by leaving the offset preset pin open and connecting a trim pot of 100Ω for the LH0033 or 1 kΩ for the LH0063 between the offset adjust pin and V^- as illustrated in Figures 1 and 2.

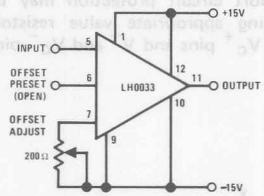


FIGURE 1. Offset Zero Adjust for LH0033 (Pin nos. shown for TO-8)

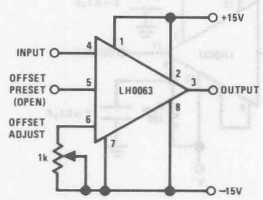


FIGURE 2. Offset Zero Adjust for LH0063

Applications Hints (Cont'd)

Operation from Single or Asymmetrical Power Supplies: Both device types may be readily used in applications where symmetrical supplies are unavailable or not desirable. A typical application might be an interface to a MOS shift register where $V^+ = +5V$ and $V^- = -12V$. In this case, an apparent output offset occurs due to the device's voltage gain of less than unity. This additional output offset error may be predicted by:

$$\Delta V_O \cong (1 - A_V) \frac{(V^+ - V^-)}{2} = .005\,(V^+ - V^-)$$

where:

A_V = No load voltage gain, typically .99

V^+ = Positive supply voltage

V^- = Negative supply voltage

For the above example, ΔV_O would be −35 mV. This may be adjusted to zero as described in Section 2. For AC coupled applications, no additional offset occurs if the DC input is properly biased as illustrated in the "typical applications" section.

Short Circuit Protection: In order to optimize transient response and output swing, output current limit has been omitted from the LH0033 and LH0063. Short circuit protection may be added by inserting appropriate value resistors between V^+ and $V_C{}^+$ pins and V^- and $V_C{}^-$ pins as illustrated in Figures 3 and 4. Resistor values may be predicted by:

$$R_{LIM} \cong \frac{V^+}{I_{SC}} = \frac{V^-}{I_{SC}}$$

where: $I_{SC} \leq 100$ mA for LH0033

$I_{SC} \leq 250$ mA for LH0063

The inclusion of limiting resistors in the collectors of the output transistors reduces output voltage swing. Decoupling $V_C{}^+$ and $V_C{}^-$ pins with capacitors to ground will retain full output swing for transient pulses. Alternate active current limit techniques that retain full DC output swing are shown in Figures 5, 6 and 7. In Figures 5 and 6, the current sources are saturated during normal operation thus apply full supply voltage to the V_C pins. Under fault conditions, the voltage decreases as required by the overload. For Figure 5:

$$R_{LIM} = \frac{V_{BE}}{I_{SC}} = \frac{.6V}{60\text{ mA}} = 10\Omega$$

In Figure 6, quad transistor arrays are used to minimize can count and:

$$R_{LIM} = \frac{V_{BE}}{1/3\,(I_{SC})} = \frac{.6V}{1/3\,(200\text{ mA})} = 8.2\Omega$$

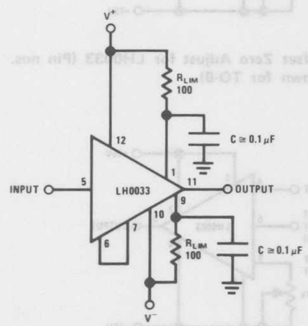


FIGURE 3. LH0033 Using Resistor Current Limiting

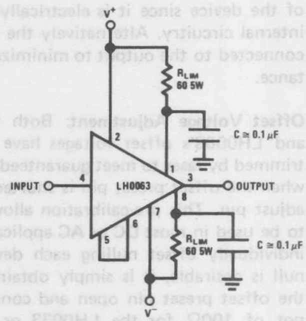


FIGURE 4. LH0063 Using Resistor Current Limiting

Applications Hints (Cont'd)

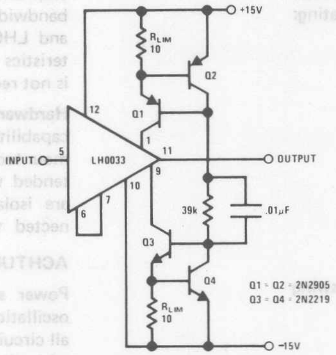


FIGURE 5. LH0033 Current Limiting Using Current Sources

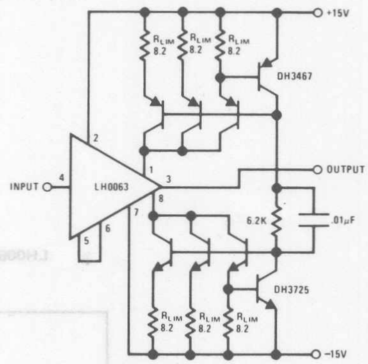


FIGURE 6. LH0063 Current Limiting Using Current Sources

Capacitive Loading: Both the LH0033 and LH0063 are designed to drive capacitive loads such as coaxial cables in excess of several thousand picofarads without susceptibility to oscillation. However, peak current resulting from $(C \times d_V/d_t)$ should be limited below absolute maximum peak current ratings for the devices.

Thus for the LH0033:

$$\left(\frac{\Delta V_{IN}}{\Delta t}\right) \times C_L \leq I_{OUT} \leq \pm 250\text{ mA}$$

and for the LH0063:

$$\left(\frac{\Delta V_{IN}}{\Delta t}\right) \times C_L \leq I_{OUT} \leq \pm 500\text{ mA}$$

should be kept below total package power rating:

$$P_{\substack{diss\\pkg}} \geq P_{DC} + P_{AC}$$

$$P_{\substack{diss\\pkg}} \geq (V^+ - V^-) \times I_S + P_{AC}$$

$$P_{AC} \cong (V_{P-P})^2 \times f \times C_L$$

where V_{P-P} = Peak-to-peak output voltage swing

f = frequency

C_L = Load Capacitance

Operation Within an Op Amp Loop: Both devices may be used as a current booster or isolation buffer within a closed loop with op amps such as LH0032, LH0062, or LM118. An isolation amp output and the input of LH0033. The wide bandwidths and high slew rates of the LH0033 and LH0063 assure that the loop has the characteristics of the op amp and that additional rolloff is not required.

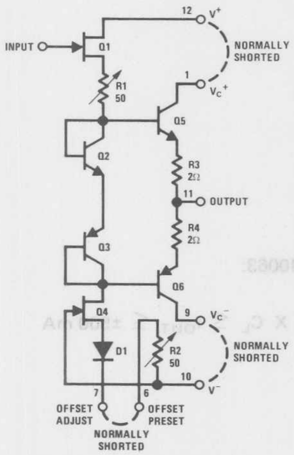
Hardware: In order to utilize the full drive capabilities of both devices, each should be mounted with a heat sink particularly for extended temperature operation. The cases of both are isolated from the circuit and may be connected to system chassis.

ACHTUNG!

Power supply bypassing is necessary to prevent oscillation with both the LH0033 and LH0063 in all circuits. Low inductance ceramic disc capacitors with the shortest practical lead lengths must be connected from each supply lead (within < ¼ to ½" of the device package) to a ground plane. Capacitors should be one or two 0.1μF in parallel for the LH0033; adding a 4.7μF solid tantalum capacitor will help in troublesome instances. For the LH0063, two 0.1μF ceramic and one 4.7μF solid tantalum capacitors in parallel will be necessary on each supply lead.

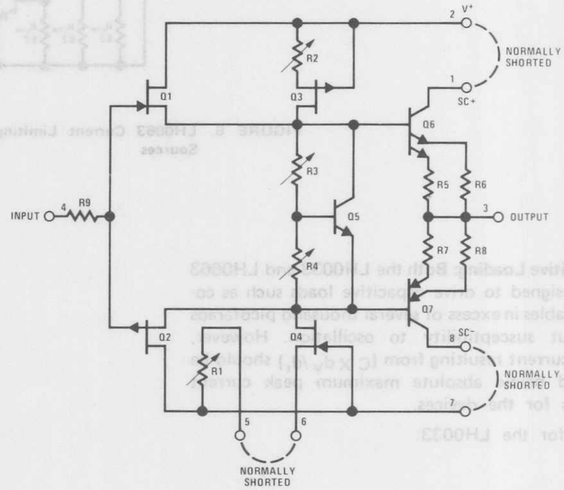
Schematic Diagrams

LH0033/LH0033C



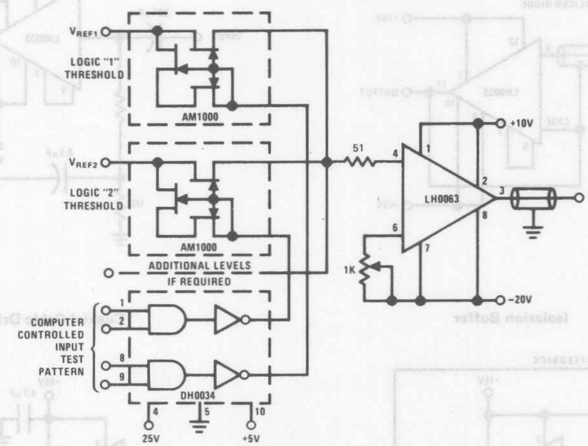
PIN NUMBERS SHOWN FOR TO-8 ("G") PACKAGE.

LH0063/LH0063C

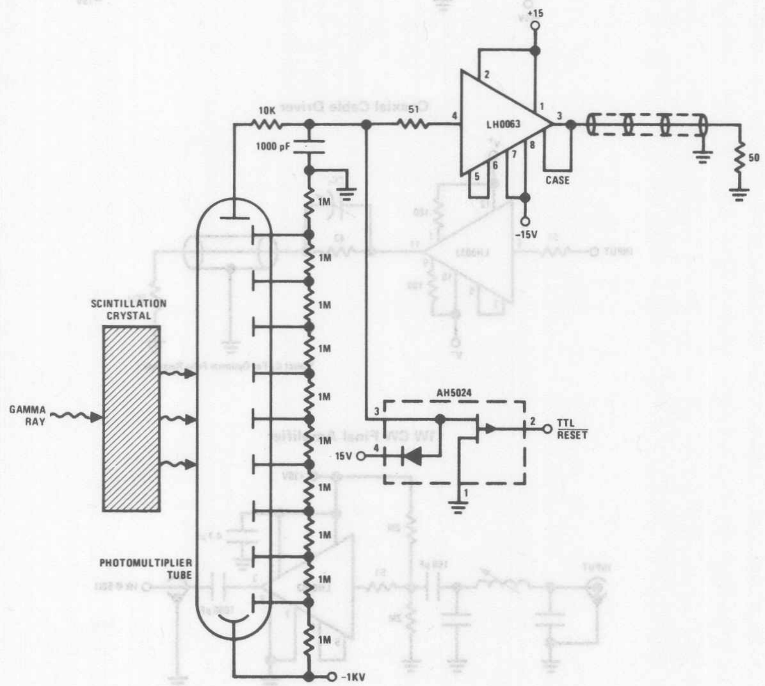


Typical Applications

High Speed Automatic Test Equipment Forcing Function Generator

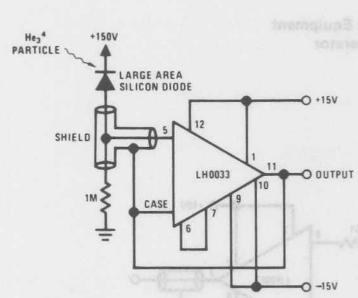


Gamma Ray Pulse Integrator

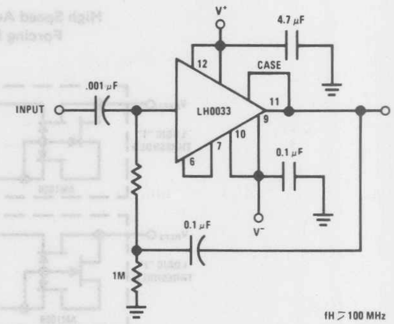


Typical Applications (Cont'd)

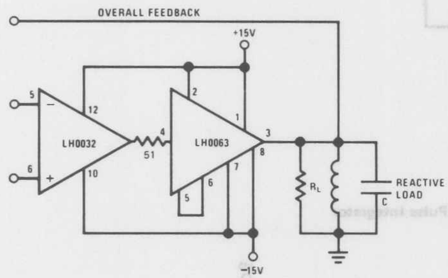
Nuclear Particle Detector



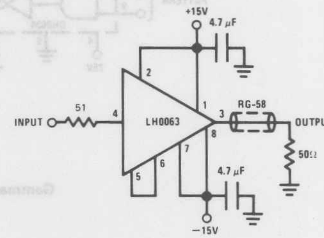
High Input Impedance AC Coupled Amplifier



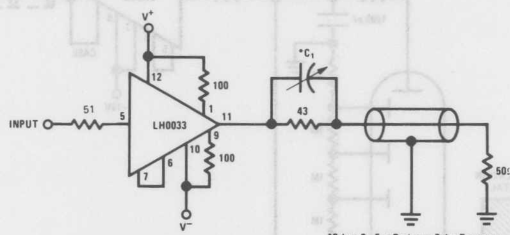
Isolation Buffer



Coaxial Cable Driver

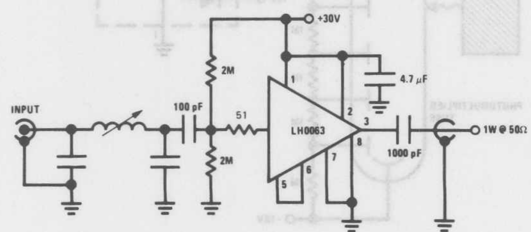


Coaxial Cable Driver



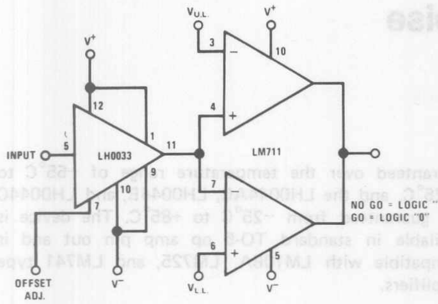
*Select C_1 For Optimum Pulse Response

1W CW Final Amplifier

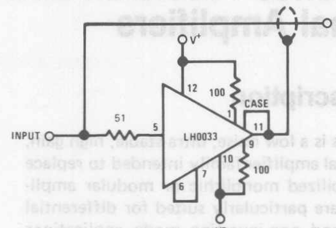


Typical Applications (Cont'd)

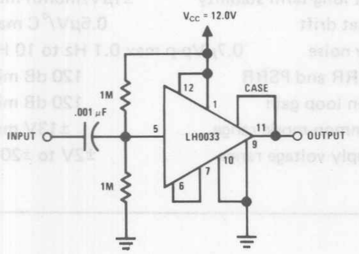
High Input Impedance Comparator With Offset Adjust



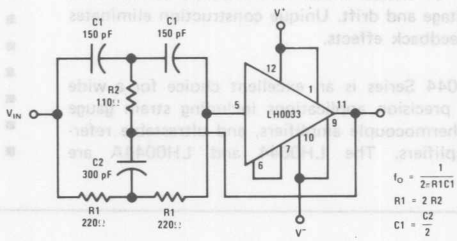
Instrumentation Shield/Line Driver



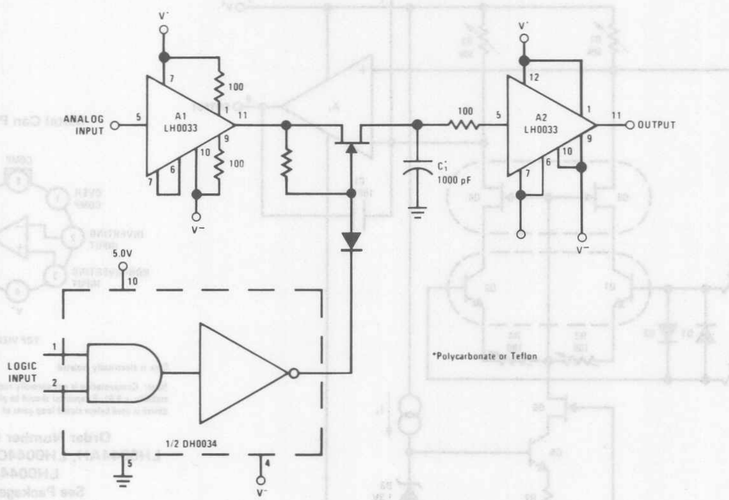
Single Supply AC Amplifier



4.5 MHz Notch Filter



High Speed Sample & Hold



*Polycarbonate or Teflon

LH0044 Series Precision Low Noise Operational Amplifiers

General Description

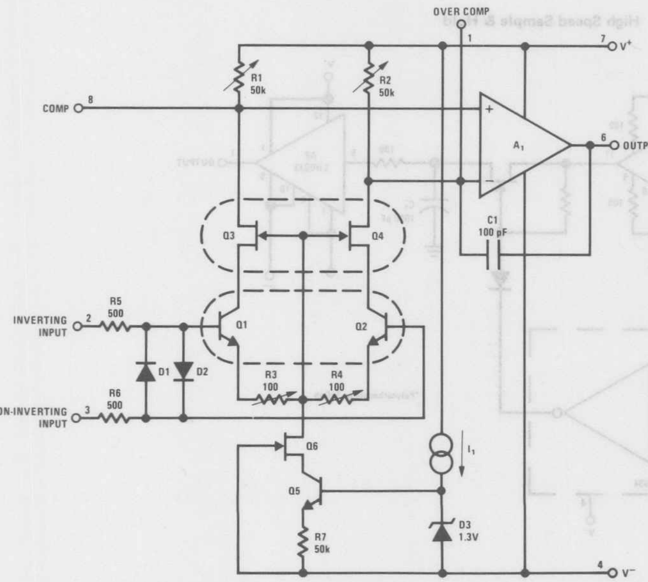
The LH0044 Series is a low noise, ultra-stable, high gain, precision operational amplifier family intended to replace either chopper-stabilized monolithic or modular amplifiers. The devices are particularly suited for differential mode, inverting, and non-inverting mode applications requiring very low initial offset, low offset drift, very high gain, high CMRR, and high PSRR. In addition, the LH0044 Series' low initial offset and offset drift eliminate costly and time consuming null adjustments at the systems level. The superior performance afforded by the LH0044 Series is made possible by advanced processing and testing techniques, as well as active laser trim of critical metal film resistors to minimize offset voltage and drift. Unique construction eliminates thermal feedback effects.

The LH0044 Series is an excellent choice for a wide range of precision applications including strain gauge bridges, thermocouple amplifiers, and ultrastable reference amplifiers. The LH0044 and LH0044A are guaranteed over the temperature range of −55°C to +125°C, and the LH0044AC, LH0044B, and LH0044C are guaranteed from −25°C to +85°C. The device is available in standard TO-5 op amp pin out and is compatible with LM108A, LM725, and LM741 type amplifiers.

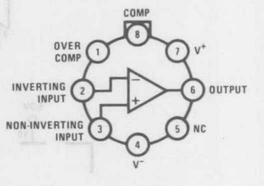
Features

- Low input offset voltage 25μV max
- Excellent long-term stability ±1μV/month max
- Low offset drift 0.5μV/°C max
- Very low noise 0.7μVp-p max 0.1 Hz to 10 Hz
- High CMRR and PSRR 120 dB min
- High open loop gain 120 dB min
- Wide common-mode range ±13V min
- Wide supply voltage range ±2V to ±20V

Equivalent Circuit and Connection Diagram



Metal Can Package



TOP VIEW

Case is electrically isolated

Note: Compensation is not normally required. However, for maximum stability, a 0.01μF capacitor should be placed between pins 7 and 8 when device is used below closed loop gains of 10.

Order Number LH0044H, LH0044AH, LH0044CH, LH0044ACH, LH0044BH
See Package H08B

Absolute Maximum Ratings

Supply Voltage	±20V
Power Dissipation	600 mW
Differential Input Voltage (Note 4)	±1V
Input Voltage (Note 5)	±15V
Output Short-Circuit Duration	Continuous
Operating Temperature Range	
LH0044, LH0044A	−55°C to +125°C
LH0044AC, LH0044B, LH0044C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	LIMITS LH0044A/LH0044AC MIN	TYP	MAX	LH0044/LH0044B/LH0044C MIN	TYP	MAX	UNITS
Input Offset Voltage	$T_A = 25°C$, $R_S = 50\Omega$, $V_{CM} = 0V$		8	25		12	50	μV
	LH0044C Only						100	μV
Input Offset Voltage	$R_S = 50\Omega$, $V_{CM} = 0V$			55			180	μV
	LH0044A and LH0044B Only			75			80	μV
Average Input Offset Voltage Drift	$T_{MIN} \leq T_A \leq T_{MAX}$		0.1	0.5		0.2	1.3	μV/°C
	LH0044B Only						0.5	μV/°C
Long-Term Stability	(Note 2)		0.2	1		0.3	2	μV/month
Input Noise Voltage (Note 3)	BW = 0.1 Hz to 10 Hz, $R_S = 50\Omega$		0.35	0.7		0.35	0.8	μVp-p
	$R_S = 10\ k\Omega$ Imbalance		0.50	0.9		0.50	1.0	μVp-p
Thermal Feedback Coefficient			0.005			0.005		μV/mW
Open Loop Voltage Gain	$R_L = 10\ k\Omega$	120	145		114	140		dB
Common-Mode Rejection Ratio	$-10V \leq V_{CM} \leq +10V$	120	145		114	140		dB
Power Supply Rejection Ratio	$\pm 3V \leq V_S \leq \pm 18V$	120	145		114	140		dB
Input Voltage Range		±13	±13.8		±12	±13.5		V
Output Voltage Swing	$R_L = 10\ k\Omega$	±13	±13.7		±12	±13.5		V
Input Offset Current	$25°C \leq T_A \leq T_{MAX}$		1.0	2.5		1.5	5.0	nA
	$T_{MIN} \leq T_A < 25°C$			5.0			10.0	nA
Average Input Offset Current Drift			5	40		15	80	pA/°C
Input Bias Current	$25°C \leq T_A \leq T_{MAX}$		8.5	15		10	30	nA
	$T_{MIN} \leq T_A < 25°C$			50			100	nA
Average Input Bias Current Drift			50	300		100	600	pA/°C
Differential Input Impedance		5	10		2.5	8		MΩ
Common-Mode Input Impedance			2×10^{11}			2×10^{11}		Ω
Supply Current	$I_L = 0$		0.9	3.0		1.0	4.0	mA
Power Dissipation			27	90		30	120	mW

AC Electrical Characteristics $T_A = 25°C$, $V_S = \pm 15V$

PARAMETER	CONDITIONS	TYP	UNITS
Input Noise Voltage	$R_S = 1\ k\Omega$, $f_O = 10$ Hz	11	$nV/\sqrt{Hz}$
	$R_S = 1\ k\Omega$, $f_O = 1$ kHz	9	$nV/\sqrt{Hz}$
Slew Rate	$A_V = +1$, $R_L = 10\ k\Omega$, $V_{IN} = \pm 10V$	0.06	V/μs
Large Signal Bandwidth	$A_V = +1$, $R_L = 10\ k\Omega$, $V_{IN} = \pm 10V$	1	kHz
Overload Recovery Time	$A_V = +100$, $V_{IN} = -100$ mV, $\Delta V_{IN} = 200$ mV	5	μs
Small Signal Bandwidth	$A_V = +1$, $R_L = 10\ k\Omega$	400	kHz
Small Signal Rise Time	$A_V = +1$, $R_L = 10\ k\Omega$, $V_{IN} = 10$ mV	2.5	μs
Overshoot	$A_V = +1$, $R_L = 10\ k\Omega$, $V_{IN} = 10$ mV, $C_L = 100$ pF	10	%

Note 1: All specifications apply for all device grades, at $V_S = \pm 15V$, and from T_{MIN} to T_{MAX} unless otherwise specified. T_{MIN} is −55°C and T_{MAX} is +125°C for the LH0044A and LH0044. T_{MIN} is −25°C and T_{MAX} is +85°C for the LH0044AC, LH0044B and LH0044C. Typicals are given for $T_A = 25°C$.

Note 2: This parameter is not 100% tested; however, 90% of the devices are guaranteed to meet this specification after one month of operation and after initial turn-on stabilization.

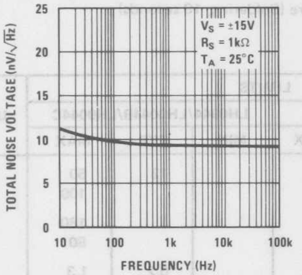
Note 3: Noise is 100% tested on the LH0044A, LH0044AC and LH0044B only. 90% of the LH0044 and LH0044C devices are guaranteed to meet this specification.

Note 4: The inputs are shunted by back-to-back diodes for over-voltage protection. Excessive current will flow for differential input voltages in excess of 1V. Input current should be limited to less than 1 mA.

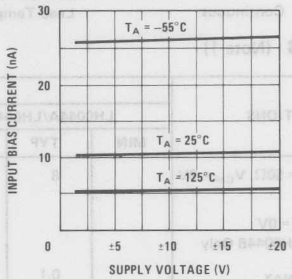
Note 5: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Typical Performance Characteristics

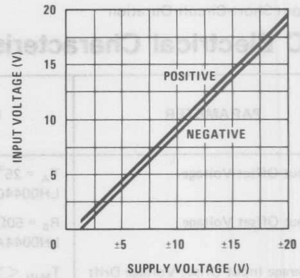
Total Input Noise Voltage vs Frequency



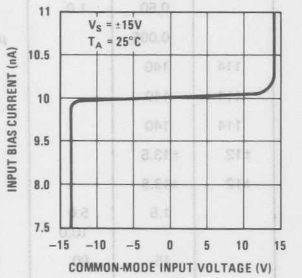
Input Bias Current



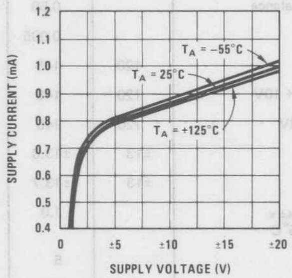
Input Voltage Range



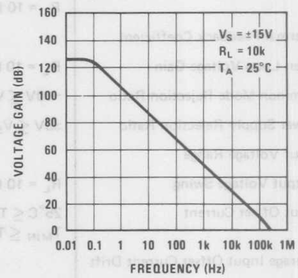
Input Bias Current vs Common-Mode Input Voltage



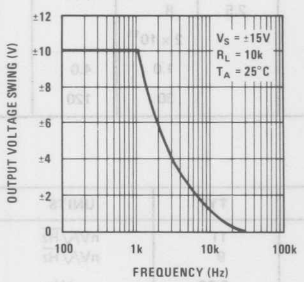
Supply Current vs Supply Voltage



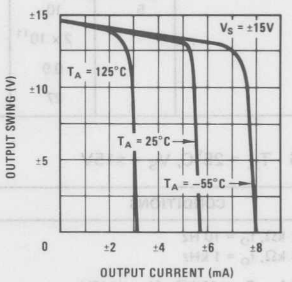
Open Loop Frequency Response



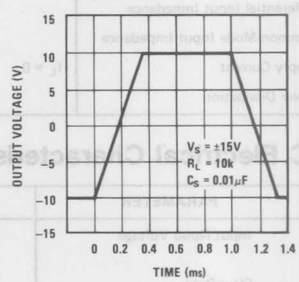
Large Signal Voltage Response



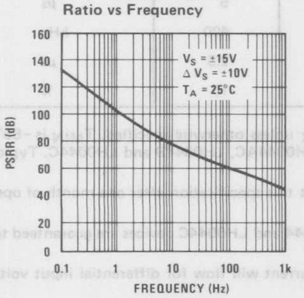
Output Swing



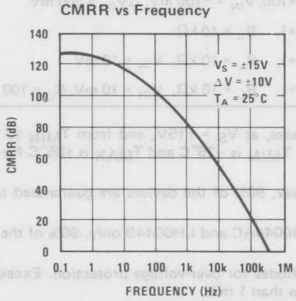
Large Signal Pulse Response



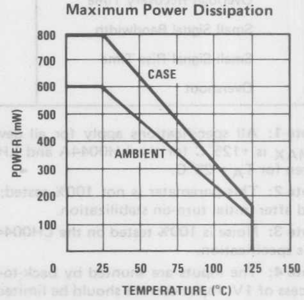
Power Supply Rejection Ratio vs Frequency



CMRR vs Frequency



Maximum Power Dissipation



Applications Information

LOW DRIFT CONSIDERATIONS

Achieving ultra-low drift in practical applications requires strict attention to board layout, thermocouple effects, and input guarding. For specific recommendations refer to AN-63 and AN-79.

A point worth stressing with regard to low drift specifications is testing of the LH0044. Simply stated—it is virtually impossible to test the device using a thermoprobe or other form of local heating. A one degree centigrade temperature gradient can account for tens of microvolts of virtual offset (or drift). The test circuit of *Figure 1* is recommended for use in a stabilized oven or continuously stirred oil bath with the entire circuit inside the oven or bath. Isothermal layout of the resistors is advised in order to minimize thermocouple induced EMF's.

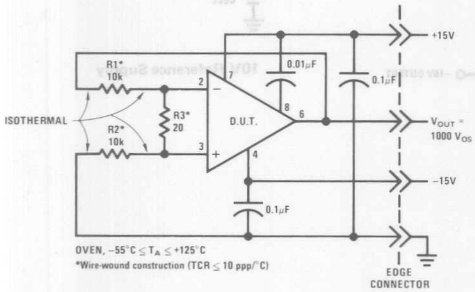


FIGURE 1. LH0044 Temperature Test Circuit

OVER COMPENSATION

The LH0044 may be overcompensated in order to minimize noise bandwidth by paralleling the internal 100 pF capacitor with an external capacitor connected between pins 1 and 6. Unity gain frequency may be predicted by:

$$f = \frac{4 \times 10^{-5}}{100\ \text{pF} + C_{ext}\ \text{pF}}\ \text{(Hz)}$$

COMPENSATION

For closed loop gains in excess of 10, no external components are required for frequency stability. However, for gains of 10 or less, a 0.01μF disc capacitor is recommended between pin 7 (V^+) and pin 8 (Comp). An improvement in ac PSRR will also be realized by use of the 0.01μF capacitor.

OFFSET NULL

In general, further nulling of LH0044 is neither necessary nor recommended. For most applications the specified initial offset is sufficient.

However, for those applications requiring additional null, an obvious temptation might be to place a pot between pins 1 and 8 with the wiper returned to V^+. This technique will usually result in reduced gain and increased offset drift due to mismatch in the TCR of the pot and R1 and R2. The technique is, therefore, not generally recommended.

The recommended technique for offset nulling the LH0044 is shown in *Figure 2*. Null is accomplished in A_2 and all errors are divided by the closed loop gain of the LH0044. Additional offset and drift incurred due to use of A_2 is less than 1μV/V for V^+ and V^- changes and 0.01μV/°C drift for the values shown in *Figure 2*.

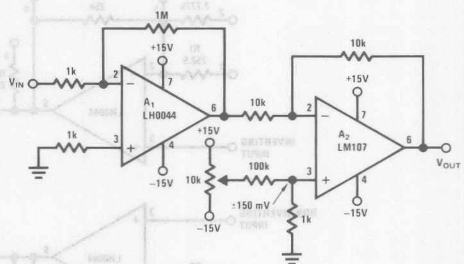
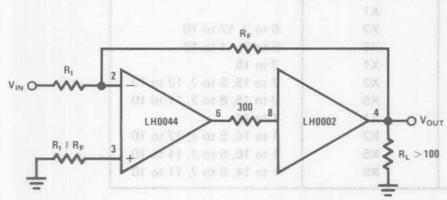
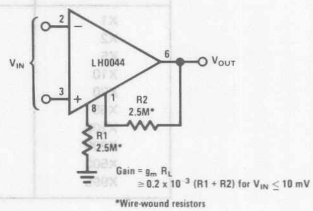


FIGURE 2. LH0044 Null Technique

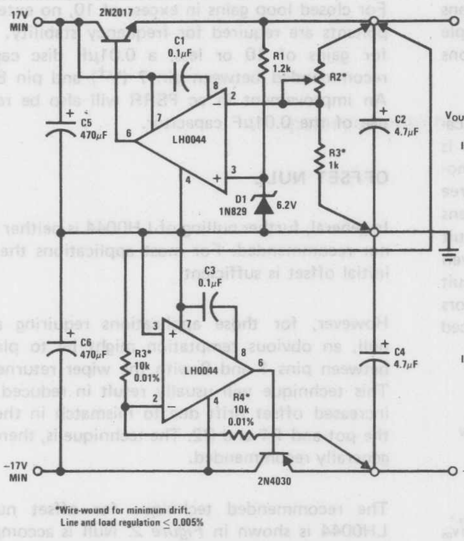
Typical Applications



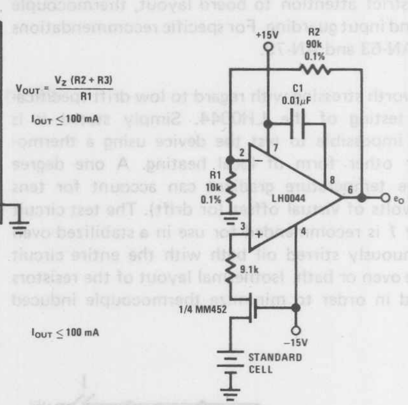
Buffered Output for Heavy Loads



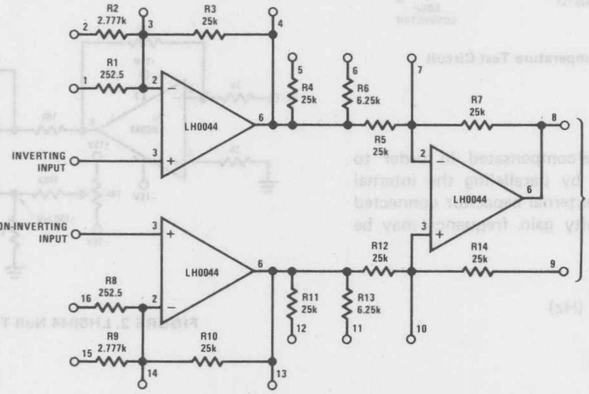
X1000 Instrumentation Amp



Precision Dual Tracking Regulator



10V Reference Supply

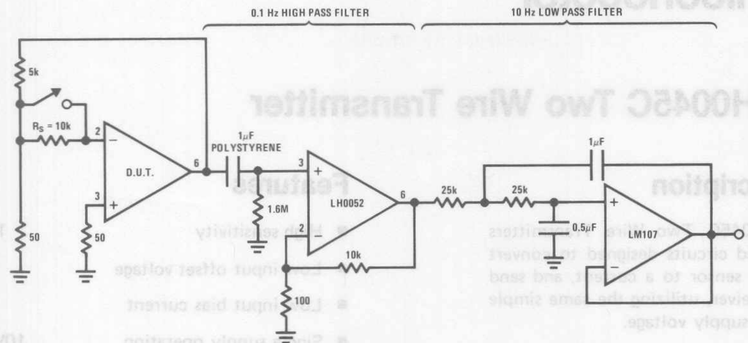


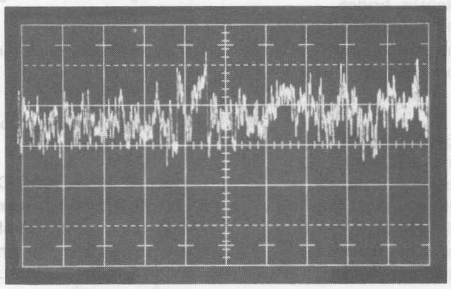
All resistors are part of National's RA201 resistor array.

OVERALL GAIN	INPUT STAGE GAIN	OUTPUT STAGE GAIN	JUMPER PINS ON RA201
X1	X1	X1	–
X2	X1	X2	5 to 7, 12 to 10
X5	X1	X5	6 to 7, 11 to 10
X10	X10	X1	2 to 15
X20	X10	X2	2 to 15, 5 to 7, 12 to 10
X50	X10	X5	2 to 15, 6 to 7, 11 to 10
X100	X100	X1	1 to 16
X200	X100	X2	1 to 16, 5 to 7, 12 to 10
X500	X100	X5	1 to 16, 6 to 7, 11 to 10
X995	X199	X5	1 to 14, 6 to 7, 11 to 10

Precision Instrumentation Amplifier

Noise Test Circuit





VERT: 200 nV/DIV
HORIZ: 5 SEC/DIV

National Semiconductor

Operational Amplifiers/Buffers

LH0045/LH0045C Two Wire Transmitter

General Description

The LH0045/LH0045C Two Wire Transmitters are linear integrated circuits designed to convert the voltage from a sensor to a current, and send it through to a receiver, utilizing the same simple twisted pair as the supply voltage.

The LH0045 and LH0045C contain an internal reference designed to power the sensor bridge, a sensitive input amplifier, and an output current source. The output current scale can be adjusted to match the industry standards of 4.0 mA to 20 mA or 10 mA to 50 mA.

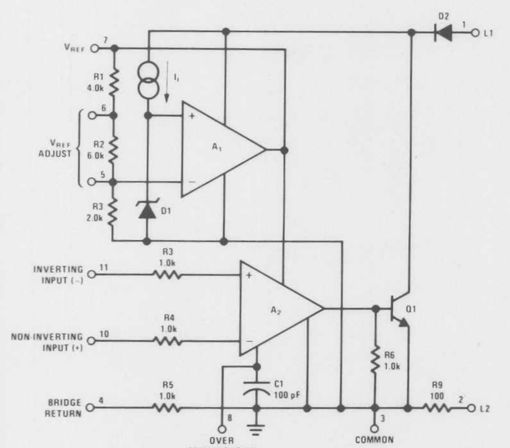
Designed for use with various sensors, the LH0045/LH0045C will interface with thermocouples, strain gauges, or thermistors. The use of the power supply leads as the signal output eliminates two or three extra wires in remote signal applications. Also, current output minimizes susceptibility to voltage noise spikes and eliminates line drop problems.

Features

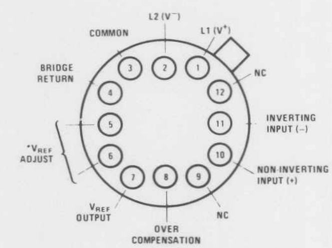
- High sensitivity $> 10\ \mu A/\mu V$
- Low input offset voltage 1.0 mV
- Low input bias current 2.0 nA
- Single supply operation 10V to 50V
- Programmable bridge reference (LH0045G) 5.0V to 30V
- Non-interactive span and null adjust
- Over compensation capability
- Supply reversal protection

The LH0045/LH0045C is intended to fulfill a wide variety of process control, instrumentation, and data acquisition applications. The LH0045 is guaranteed over the temperature range of −55°C to +125°C; whereas the LH0045C is guaranteed from −25°C to +85°C.

Equivalent Schematic and Connection Diagrams



*NOTE: PINS SHOWN ARE FOR THE 12 PIN TO-8 ("G") PACKAGE.



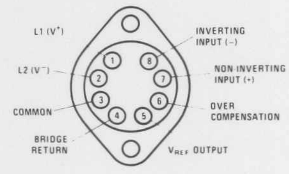
TOP VIEW

*NOTE: PIN 5 IS SHORTED TO PIN 6 TO OBTAIN A NOMINAL +5.1V, V_{REF}. LEFT OPEN V_{REF} = +10V.

THE CASE IS ISOLATED FROM THE CIRCUIT FOR BOTH TO-3 AND TO-8

Order Number LH0045G or LH0045CG
See Package H12B

TO-3



TOP VIEW

Order Number LH0045K or LH0045CK
See Package K08A

Absolute Maximum Ratings

Supply Voltage (L1 to common)	+50V
Input Current	±20 mA
Input Voltage (Either Input to Common)	0V to V_{REF}
Differential Input Voltage	±20 V
Output Current (Either L1 or L2)	50 mA
Reference Output Current	5.0 mA
Power Dissipation	
LH0045G	1.5W
LH0045K	3.0W
Operating Temperature Range	
LH0045	−55°C to +125°C
LH0045C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

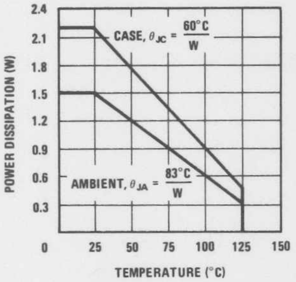
Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	LIMITS LH0045 MIN	LH0045 TYP	LH0045 MAX	LH0045C MIN	LH0045C TYP	LH0045C MAX	UNITS
Input Offset Voltage (V_{OS})	I_S = 4.0 mA, T_A = 25°C		0.7	2.0		2.0	7.5	mV
	I_S = 4.0 mA			3.0			10	mV
Offset Voltage Temperature Coefficient ($\Delta V_{OS}/\Delta T$)	I_S = 4.0 mA		3.0			6.0		µV/°C
Input Bias Current (I_B)	T_A = 25°C		0.8	2.0		1.5	7.0	nA
				3.0			10	nA
Input Offset Current (I_{OS})	T_A = 25°C		0.05	0.2		0.2	1.0	nA
				0.4			1.5	nA
Open Loop Transconductance (g_{MOL})	ΔI_S = 4.0 mA to 20 mA	10^6	10^7		10^6	10^7		µ℧
	ΔI_S = 10 mA to 50 mA	2×10^6	2×10^7		2×10^6	2×10^7		µ℧
Supply Voltage Range (V_S)		9.0		50	9.0		50	V
	LH0045G pins 5 and 6 open	15		50	15		50	V
Input Voltage Range (V_{IN})		1.0		3.3	1.0		3.3	V
	LH0045G pins 5 and 6 open	1.0		7.6	1.0		7.6	V
Open Loop Output Impedance (R_{OUT})	V_S = 10V to 45V, I_S = 4.0 mA, T_A = 25°C		1.0			1.0		MΩ
Common Mode Rejection Ratio (CMRR)	ΔV_{IN} = 1.0V to 3.3V, I_S = 12 mA	0.1	0.05		0.1	0.05		mV/V
Power Supply Rejection Ratio (PSRR)	ΔV_S = 10V to 45V, I_S = 12 mA	0.1	0.01		0.1	0.01		mV/V
Open Loop Supply Current (I_{SOL})	V_S = 50V		2.0	3.0		2.0	3.0	mA
Reference Voltage Load Regulation ($\Delta V_{REF}/\Delta I_{REF}$)	ΔI_{REF} = 0 mA to 2.0 mA, T_A = 25°C		0.05	0.2		0.05	0.2	%
Reference Voltage Line Regulation ($\Delta V_{REF}/\Delta V_S$)	ΔV_S = 10V to 45V, T_A = 25°C		0.3	0.5		0.3	0.7	mV/V
Reference Voltage Temperature Coefficient ($\Delta V_{REF}/\Delta T$)	I_{REF} = 2.0 mA		0.004			0.004		%/°C
Reference Voltage (V_{REF})	I_{REF} = 2.0 mA, T_A = 25°C	4.3	5.1	5.9	4.3	5.1	5.9	V
	I_{REF} = 2.0 mA, T_A = 25°C, LH0045G pins 5 and 6 open	8.6	10.3	12	8.6	10.3	12	V
Resistor R9	I_S = 12 mA, T_A = 25°C	95	100	105	95	100	105	Ω
Average Temperature Coefficient of R9 (TCR_9)	I_S = 12 mA		50	300		50	300	PPM/°C
Resistor R5	I_S = 1.0 mA, T_A = 25°C	950	1000	1050	950	1000	1050	Ω
Average Temperature Coefficient of R5 (TCR_5)	I_S = 1.0 mA		50	300		50	300	PPM/°C
Input Resistance (R_{IN})	T_A = 25°C		50			50		MΩ

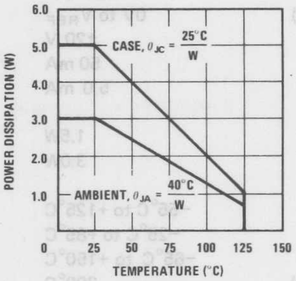
Note 1: Unless otherwise specified, these specifications apply for $+10V \le V_S \le +50V$, pin 5 shorted to pin 6 on the LH0045G, over the temperature range −55°C to +125°C for the LH0045 and −25°C to +85°C for the LH0045C.

LH0045/LH

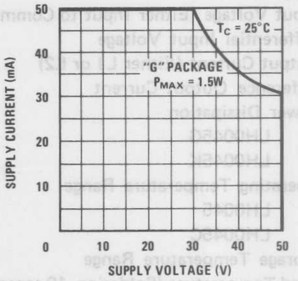
LH0045G Maximum Power Dissipation



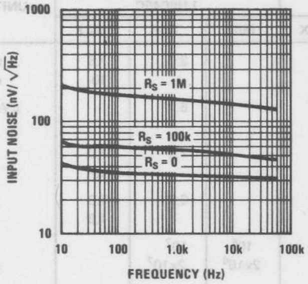
LH0045K Maximum Power Dissipation



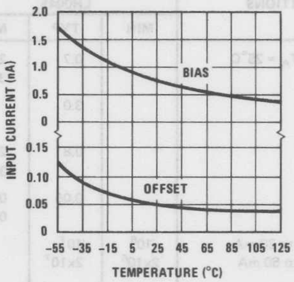
Safe Operating Area



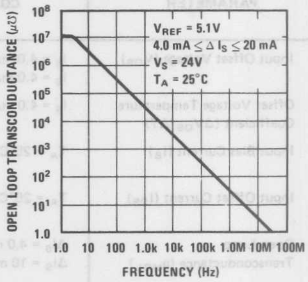
Input Noise Voltage



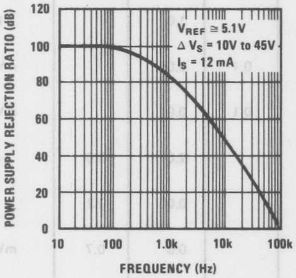
Input Currents



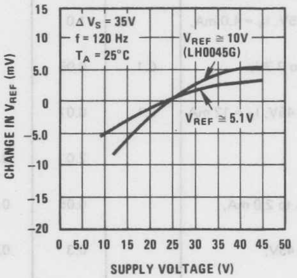
Open Loop Transconductance vs Frequency



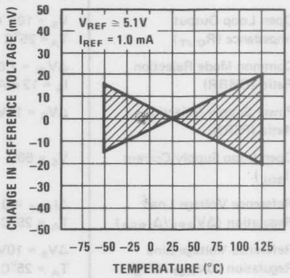
Power Supply Rejection Ratio vs Frequency



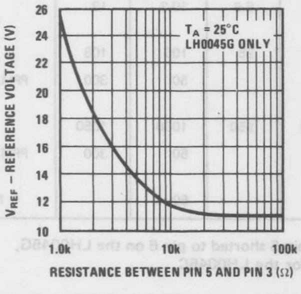
V_{REF} Line Regulation



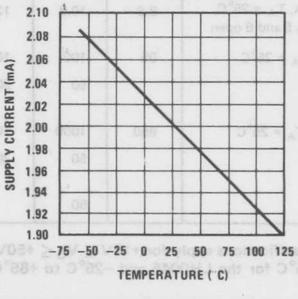
Variation of V_{REF} With Temperature Normalized to 25°C



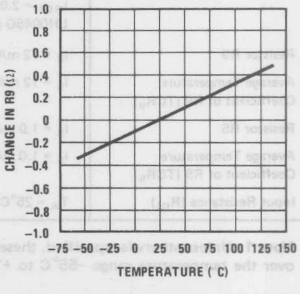
V_{REF} vs Resistance Between Pin 5 and Pin 3



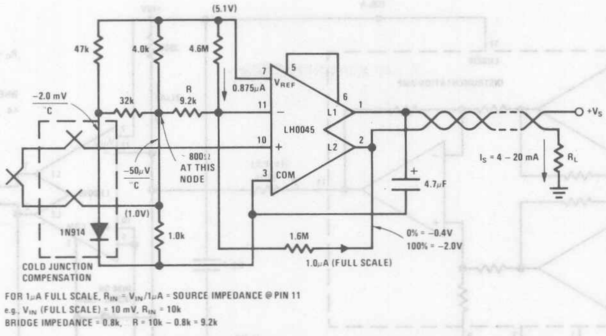
Open Loop Supply Current vs Temperature



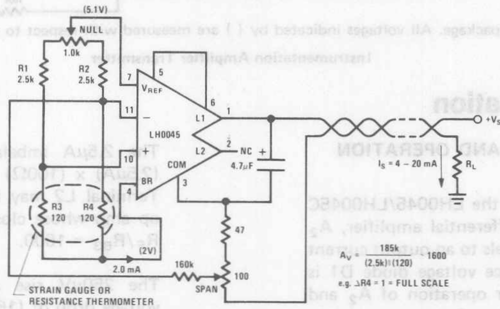
Change in R9 With Temperature Normalized to 25°C



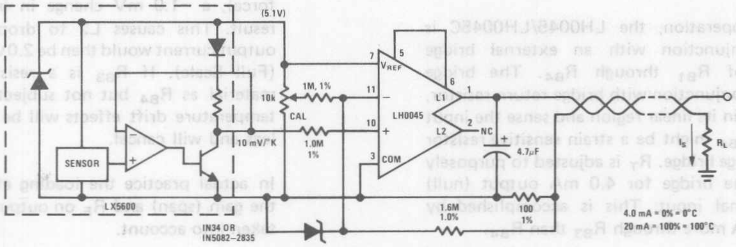
Typical Applications



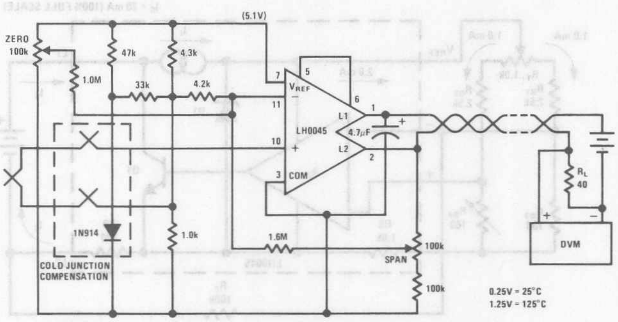
Thermocouple Input Transmitter



Resistance Bridge Input Transmitter



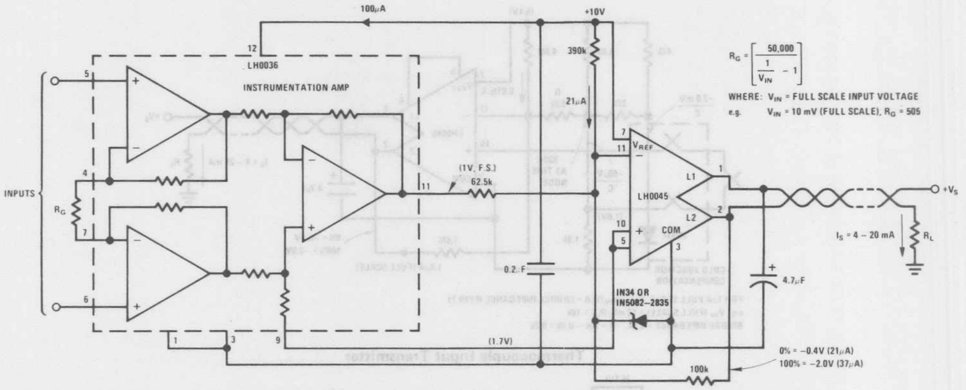
Electronic Temperature Sensor



Remote Sensing Digital Thermometer

*Pin numbers refer to 'G' package. All voltages indicated by ( ) are measured with respect to common, pin 3.

Typical Applications (Cont'd)



*Pin numbers refer to 'G' package. All voltages indicated by ( ) are measured with respect to common, pin 3.

Instrumentation Amplifier Transmitter

Applications Information

CIRCUIT DESCRIPTION AND OPERATION

A simplified schematic of the LH0045/LH0045C is shown in Figure 1. Differential amplifier, A_2 converts very low level signals to an output current via transistor Q1. Reference voltage diode D1 is used to supply voltage for operation of A_2 and to bias an external bridge. Current source I_1 minimizes fluctuation in the bridge reference voltage due to changes in V_S.

In normal operation, the LH0045/LH0045C is used in conjunction with an external bridge comprised of R_{B1} through R_{B4}. The bridge resistors in conjunction with bridge return resistor, R5, bias A_2 in its linear region and sense the input signal; e.g. R_{B4} might be a strain sensitive resistor in a strain gauge bridge. R_T is adjusted to purposely unbalance the bridge for 4.0 mA output (null) for zero signal input. This is accomplished by forcing 2.5μA more through R_{B3} than R_{B4}.

The 2.5μA imbalance causes a voltage rise of (2.5μA) x (100Ω) or 250μV at the top of R_{B3}. Terminal L2 may be viewed as the output of an op amp whose closed loop gain is approximately R_F/R_{B3} = 1600.

The 250μV rise at the top of R_{B3} causes a voltage drop of (1600) x (250μV) or −0.4V across R9. An output current, I_S, equal to 0.4V/R9 or 4.0 mA is thus established in Q1. If R_{B4} is now decreased by 1.0Ω (due to application of a strain force), a −1.0 mV change in input voltage will result. This causes L2 to drop to −2.0V. The output current would then be 2.0V/100Ω or 20 mA (Full Scale). If R_{B3} is a resistor of the same material as R_{B4} but not subjected to the strain, temperature drift effects will be equal in the two legs and will cancel.

In actual practice the loading effects of R_{B2} on the gain (span) and R_F on output current must be taken into account.

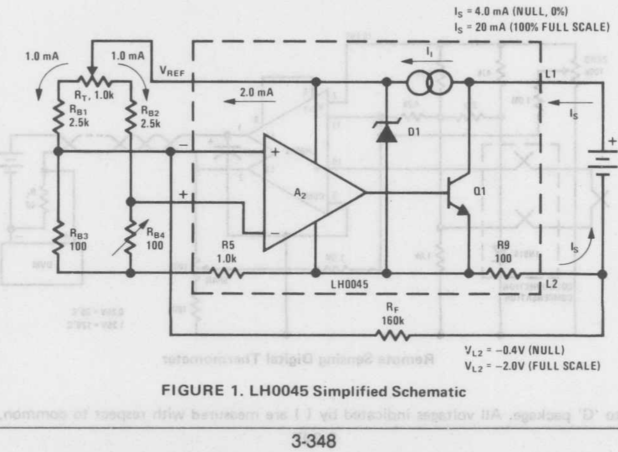


FIGURE 1. LH0045 Simplified Schematic

Applications Information (Cont'd)

THERMAL CONSIDERATIONS

The power output transistor of the LH0045 is thermally isolated from the signal amplifier, A_2. Nevertheless, a change in the power dissipation will cause a change in the temperature of the package and thus may cause amplifier drift. These temperature excursions may be minimized by careful heat sinking to hold the case temperature equal to the ambient. With the TO-8 (G) package this is best accomplished by a clip-on heat sink such as the Thermalloy #2240A or the Wakefield #215-CB. The 8 lead TO-3 is particularly convenient for heat sinking, in that it may be bolted directly to many commercial aluminum heat sink extrusions, or to the chassis. In both packages the case is electrically isolated from the circuit.

In addition, the power change can be minimized by operating the device from relatively high supply voltages in series with a relatively high load resistance. When the signal forces the supply current higher, the voltage across the device will be reduced and the internal power dissipation kept nearly equal to the low current, high voltage condition.

For example, take the case of a 4.0 mA to 20 mA transmitter with a 24V supply and a 100Ω load resistance. The power at 4.0 mA is (23.6V) x (4.0 mA) = 94.4 mW while at full scale the power is (22V) x (20 mA) = 440 mW. The net change in power is 345 mW. This change in power will cause a change in temperature and thus a change in offset voltage of A_2.

If the optimum load resistance of 800Ω (from Figure 2) is used, the power at null is [24V − (4.0 mA) x (800Ω)] (4.0 mA) = 83 mW. The power at full scale is [24V − (20 mA) x (800Ω)] (20 mA) = 160 mW. The net change is 77 mW. This change is significantly less than without the resistor.

If the supply voltage is increased to 48V and the load resistance chosen to be the optimum value from Figure 2 (1.95k), then the power at null is [48V − (4.0 mA) x (1.95k)] (4.0 mA) = 160.8 mW and the power at full scale is [48 − (20) x (1.95k)] (20 mA) = 180 mW for a net change of 19.2 mW.

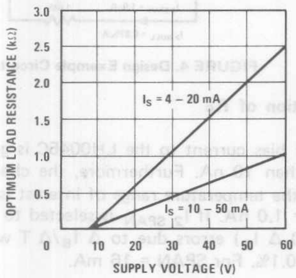


FIGURE 2. Optimum Load Resistance vs Supply Voltage

Note that the optimized load resistance is actually the sum of the line resistance, receiver resistances and added external load resistance. However, in many applications the line resistance and receiver resistances are negligible compared to the added external load resistance and thus may be omitted in calculations.

AUXILIARY PINS

The LH0045 has several auxiliary pins designed to provide the user with enhanced flexibility and performance. The following is a discussion of possible uses for these pins.

Programmable V_{REF} — Pins 5 and 6 (LH0045G Only)

The LH0045G provides pins 5 and 6 to allow the user to program the value of the reference voltage. The factory trimmed 10V value is obtained by leaving 5 and 6 open. A short between 5 and 6 will program the reference to a nominal 5.1V (equivalent to the fixed value used in the LH0045K).

A resistor or pot may be placed between pin 5 and common (pin 3) to obtain reference voltages between 10V and 30V or between pin 5 and pin 7 for reference voltages below 10V. Increased reference voltage might be useful to extend the positive common mode range or to accommodate transducers requiring higher supply voltage. A plot of resistance between pin 5 and pin 3 versus V_{REF} is given in the typical electrical characteristics section. V_{REF} may be adjusted about its nominal value by arranging a pot from V_{REF} to common and feeding a resistor from the wiper into pin 5 so that it may either inject or extract current. Lastly, pin 5 may be used as a nominal 1.7V reference point, if care is taken not to unduly load it with either dc current or capacitance. Obviously, higher supply voltages must be used to obtain the higher reference values. The minimum supply voltage to reference voltage differential is about 4.0V.

Bridge Return

An applications resistor is provided in the LH0045 with a nominal value of 1.0 kΩ. The primary application for the resistor is to maintain the minimum common mode input voltage (1.0V) required by the signal amplifier, A_2. A typical input application might utilize a strain gauge or thermistor bridge where the resistance of the sensor is 100Ω. Since only 1.0 mA may be drawn from V_{REF}, the 1.0 kΩ bridge return resistor is used to bias A_2 in its linear region as shown in Figure 3.

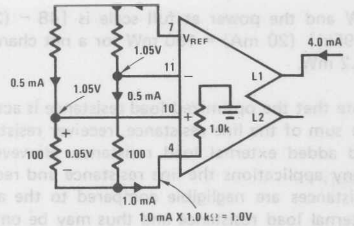


FIGURE 3. Use of Bridge Return

Over Compensation – Pin 8 (LH0045G), Pin 6 (LH0045K)

Over compensation of the signal amplifier, A_2 may be desirable in dc applications where the noise-bandwidth must be minimized. A capacitor should be placed between pin 8 (pin 6 on the LH0045K) and pin 3, common.

Typically,

$$f_{3db} = \frac{1}{2\pi R (C_1 + C_{EXT})}$$

where:

$R = 400\ M\Omega$

C1 = Internal Compensation Capacitor = 100 pF

C_{EXT} = External (over-compensation) Capacitor

Input Guard – Pins 9 and 12 (LH0045G)

Pins 9 and 12 have no internal connection whatever and thus need not be used. In some critical low current applications there may be an advantage to running a guard conductor between the inputs and the adjacent pins to intercept stray leakage currents. Pins 9 and 12 may be connected to this guard to simplify the PC board layout and allow the guard to continue under the device. (See AN-63 for further discussion of guarding techniques.)

NULL AND SPAN ADJUSTMENTS

Most applications of the LH0045 will require potentiometers to trim the initial tolerances of the sensor, the external resistors and the LH0045 itself. The preferred adjustment procedure is to stimulate the sensor, alternating between two known values, such as zero and full scale. The span and null are adjusted by monitoring the output current on a chart recorder, meter, or oscilloscope. A full scale stimulus is applied to the sensor and the span potentiometer adjusted for the desired full scale. Then, to adjust the null, apply a zero percent signal to the sensor and adjust the null potentiometer for the desired zero percent current indication.

If it is impractical to cycle the sensor during the calibration procedure, the signal may be simulated electrically with two cautions: 1) the calibration signal must be floating and 2) the calibration thus achieved does not account for sensor inaccuracies and/or errors in the signal generator.

SENSOR SELECTION

Generally it is easiest to use an insulated sensor. If it is necessary to use a grounded sensor, the power supply must be isolated from chassis ground to avoid extraneous circulating currents.

DESIGN EXAMPLE

There are numerous circuit configurations that may be utilized with the LH0045. The following is intended as a general design example which may be extended to specific cases.

Circuit Requirements

Output Characteristics

a. 0% = 4.0 mA (NULL)

b. 100% = 20 mA (SPAN = 16 mA)

c. Supply Voltage = 24V

Input (Sensor) Characteristics

a. V_{IN} = 100 mV (Full Scale)

b. V_{IN} = 0 mV (Zero Scale)

c. Source Impedance $\leq 1.0\Omega$

General Characteristics

a. $0°C \leq T_A \leq +75°C$

b. Overall Accuracy $\leq 0.5\%$

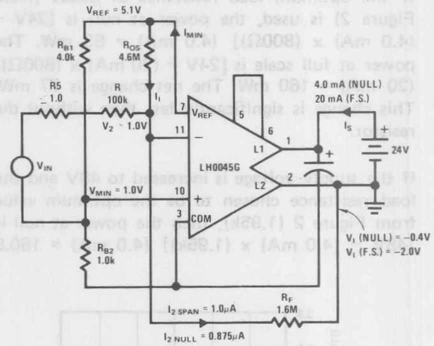


FIGURE 4. Design Example Circuit

Selection of R_F

Input bias current to the LH0045C is guaranteed less than 10 nA. Furthermore, the change in I_B over the temperature range of interest is typically under 1.0 nA. If $I_{2\ SPAN}$ is selected to be $1.0\mu A$ ($1000\ \Delta\ I_B$) errors due to $\Delta\ I_B/\Delta\ T$ will be less than 0.1%. For SPAN = 16 mA.

$$V_{SPAN} = \Delta V_1 = -(16\ mA)(R9) = -1.6V$$

Applications Information (Cont'd)

where R9 = Internal Current Set Resistor = 100Ω
For $I_{2\ SPAN} = 1.0\mu A$,

$$R_F = \frac{V_{SPAN}}{I_{2\ SPAN}} = \frac{-1.6V}{1.0\mu A} = 1.6M$$

$$R_F = 1.6\ M\Omega$$

NOTE: For applications with DC gain (ratio of feedback and input resistance) less than 8, it is recommended that a Schottky barrier diode be connected between pin 11 (cathode) and pin 3 (anode). This prevents the possibility of latch up resulting from the inverting input being forced beyond the amplifier supply voltage during power up.

Selection of R_{B1} and R_{B2}

The minimum input common mode voltage, V_{MIN} required at the pin 10 input of A_2 is 1.0V. Furthermore, the maximum open loop supply current (I_{SOL}) drawn by the LH0045 is 3.0 mA. That leaves I_{MIN} = 4.0 mA − 3.0 mA = 1.0 mA left to bias the bridge at null. Hence:

$$R_{B2} \geqq \frac{V_{MIN}}{I_{MIN}} = \frac{1.0V}{1.0\ mA} = 1.0\ k\Omega$$

And,

$$\frac{V_{REF}\ R_{B2}}{R_{B1} + R_{B2}} = 1.0V$$

$$R_{B1} = R_{B2}\ \frac{V_{REF} - 1.0V}{1.0V}$$

$$= 1.0k\ (5.1 - 1.0)$$

$$R_{B1} \cong 4.0\ k\Omega$$

Alternatively, an LM113, 1.22V reference diode, or an op amp such as the LM108 may be used to bias the signal amplifier, A_2 as shown in Figure 5. These techniques have the advantage of lowering the impedance seen at pin 10.

Selection of R_{OS}

R_{OS} is selected to provide the null current of 4.0 mA, $V_{1\ NULL}$ = 4.0 mA × 100Ω = 0.4V. From previous calculations we know that V_{MIN} = 1.0V. The voltage pin 11, V_2 is:

$$V_2 = V_{MIN} + V_{OS} \cong V_{MIN}$$

for V_{IN} = 0V

Hence, the current required to generate the null voltage, $I_{2\ NULL}$ is:

$$I_{2\ NULL} = \frac{V_{MIN} - V_{1\ NULL}}{R_F}$$

$$= \frac{1.0V - (-0.4V)}{1.6\ M\Omega} = 0.875\mu A$$

This current must be provided by R_{OS} from V_{REF}; hence:

$$R_{OS} = \frac{V_{REF} - V_{MIN}}{I_{2\ NULL}}$$

The nominal value for V_{REF} is 5.1V, therefore the nominal value for R_{OS} is:

$$\frac{5.1V - 1.0V}{0.875\mu A} \quad \text{or}$$

$$R_{OS} = 4.6\ M\Omega$$

It should be noted however, that the variation of V_{REF} may be as high as 5.9V or as low as 4.3V. Furthermore, the tolerances of R9 (100Ω), R_{B1}, R_{B2}, and the input V_{OS} of A_2 would predict values for R_{OS} as low as 3.98M and as high as 5.43M. The implication is that in the specific case, R_{OS} should be implemented with a pot, of appropriate value, in order to accommodate the tolerances of V_{REF}, R9, V_{OS}, R_{B1}, R_{B2}, etc.

Selection of R

SPAN is required to be 16 mA. From feedback theory and the gain equation we know:

$$I_{SPAN} = V_{IN}\ \frac{R_F}{R} \times \frac{1}{R9}$$

where:

R = total impedance in signal path between pin 10 and pin 11

R9 = Current setting resistor = 100Ω

V_{IN} = Full scale input voltage = 100 mV

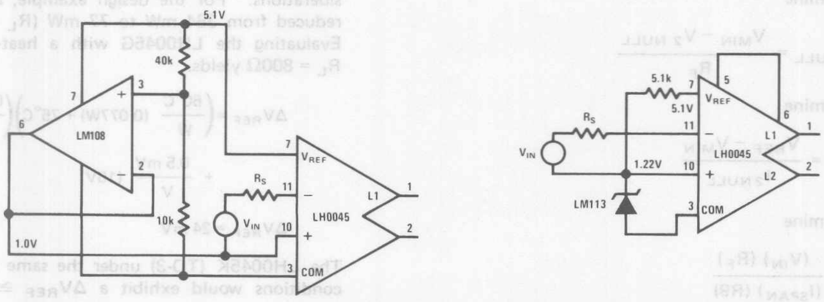


FIGURE 5. Alternate Biasing Techniques

Applications Information (Cont'd)

$$\therefore R = \frac{(V_{IN})(R_F)}{(I_{SPAN})(R9)}$$

$$R = \frac{(100\ mV)(1.6\ M\Omega)}{(16\ mA)(100\Omega)}$$

$$R = 100\ k\Omega$$

As before, uncertainties in device parameters might dictate that R_F be made a pot of appropriate value.

Summary of the Steps to Determine External Resistor Values

1. Select $I_{FULL\ SCALE} = I_{NULL} + I_{SPAN}$ for the desired application. (I_{NULL} is frequently 4.0 mA and $I_{FULL\ SCALE}$ is frequently 20 mA.)
2. Select $I_{2\ SPAN}$ so that it is large compared to ΔI_B. 1000 ΔI_B is a good value.
3. Determine $V_{SPAN} = \Delta V_2 = (I_{SPAN})(R9)$.
4. Determine $R_F = (V_{SPAN}/I_{2\ SPAN})$
5. Select

$$R_{B2} \geq \frac{V_{MIN}}{I_{MIN}}$$

$$R_{B2} \geq \frac{1\ VOLT}{I_{NULL} - I_{SOL}}$$

Where:

V_{MIN} = minimum common mode input voltage

I_{MIN} = minimum available bridge current

I_{SOL} = maximum open loop supply current

6. Determine

$$R_{B1} = R_{B2}\ \frac{V_{REF} - V_{MIN}}{V_{MIN}}$$

7. Determine $V_{2\ NULL} = I_{NULL}\ R9$
8. Determine

$$I_{2\ NULL} = \frac{V_{MIN} - V_{2\ NULL}}{R_F}$$

9. Determine

$$R_{OS} = \frac{V_{REF} - V_{MIN}}{I_{2\ NULL}}$$

10. Determine

$$R = \frac{(V_{IN})(R_F)}{(I_{SPAN})(R9)}$$

Where:

V_{IN} = Sensor full scale output voltage

ERROR BUDGET ANALYSIS

Errors Due to Change in V_{REF} (ΔV_{REF})

There are several factors which could cause a change in V_{REF}. First, as the ambient temperature changes, a V_{REF} drift of ±0.2 mV/°C might be expected. Secondly, supply voltage variations could cause a 0.5 mV/V change in V_{REF}. Lastly, self-heating due to power dissipation variations can cause drift of the reference.

An overall expression for change in V_{REF} is:

$$\Delta V_{REF} = \underbrace{[(\theta)(\Delta P_{DISS}) + \Delta T_A]\ \frac{\Delta V_{REF}}{\Delta T}}_{\text{Thermal Effects}}$$

$$+ \underbrace{\frac{\Delta V_{REF}}{\Delta V_S}\ (\Delta V_S)}_{\text{Supply Voltage Effects}}$$

Where:

θ = Thermal resistance, either junction-to-ambient to junction to case

ΔP_{DISS} = Change in avg. power dissipation

ΔT_A = Change in ambient temperature

$\frac{\Delta V_{REF}}{\Delta T}$ = Reference voltage drift (in mV/°C)

$\frac{\Delta V_{REF}}{\Delta V_S}$ = Line regulation of V_{REF}

Several steps may be taken to minimize the bracketed terms in the equation above. For example, operating the LH0045G with a heat-sink reduces the thermal resistance from θ_{JA} = 83°C/W to θ_{JC} = 60°C/W. For the LH0045K (TO-3) θ_{JA} = 40°C/W may be reduced to θ_{JC} = 25°C/W by using a heat sink. The ΔP_{DISS} term may be significantly reduced using the power minimization technique described under "Thermal Considerations." For the design example, ΔP_{DISS} is reduced from 384 mW to 77 mW (R_L = 800Ω.) Evaluating the LH0045G with a heat-sink and R_L = 800Ω yields.

$$\Delta V_{REF} = \left(\frac{60°C}{W}\ (0.077W) + 75°C\right)\left(\frac{0.2\ mV}{°C}\right)$$

$$+ \frac{0.5\ mV}{V}\ (16V)$$

$$\Delta V_{REF} = 24\ mV$$

The LH0045K (TO-3) under the same operating conditions would exhibit a $\Delta V_{REF} \cong 23$ mV.

Applications Information (Cont'd)

An expression for error in the output current due to ΔV_{REF} is:

$$\frac{\Delta I_S}{I_{SPAN}}(\%) = 100\frac{(K)(R_{OS})(\Delta V_{REF}) - (1-K)(\Delta V_{REF})(R_F)}{(R9)(R_{OS})(I_{SPAN})}$$

Where:

ΔV_{REF} = Total change in V_{REF}

$K = \dfrac{R_{B2}}{R_{B1} + R_{B2}}$

R9 = Current set resistor

I_{SPAN} = Change in output current from 0% to 100%

For example, ΔV_{REF} = 24 mV, K = 0.2, R9 = 100Ω, I_{SPAN} = 16 mA. Hence, a 0.12% worst case error might be expected in output currents due to ΔV_{REF} effects.

Error Due to V_{OS} Drift

One of the primary causes of error in I_S is caused by V_{OS} drift. Drift may be induced either by self heating of the device or ambient temperature changes. The input offset voltage drift, $\Delta V_{OS}/\Delta T$, is nominally 3.3μV/°C per millivolt of initial offset. An expression for the total temperature dependent drift is:

$$\Delta V_{OS} = [(\theta)(\Delta P_{DISS}) + \Delta T_A]\frac{\Delta V_{OS}}{\Delta T}$$

Where:

θ = Thermal resistance either junction-to-ambient or junction-to-case

ΔP_{DISS} = Change in average power dissipation

ΔT_A = Change in ambient temperature

The bracketed term may be minimized by heat sinking and using the power minimization technique described under "Thermal Considerations." For the LH0045G design example, ΔV_{OS} = 0.352 mV under ambient conditions and 0.263 mV using a heat-sink and R_L = 800Ω. Comparable V_{OS} for the LH0045K would be 0.254 mV.

The error in output current due to ΔV_{OS} is:

$$\frac{\Delta I_S}{I_{SPAN}}(\text{in }\%) = 100 \times \frac{\Delta V_{OS}}{V_{IN\ (FULL\ SCALE)}}$$

$$= 100 \times \frac{R_F}{(R)(R9)(I_{SPAN})}$$

For the design example, ΔV_{OS} = 0.263 mV, V_{IN} (Full Scale) = 100 mV. Hence, 0.26 mV ÷ 100 mV or 0.26% worst case error could be expected in output current effects.

Errors Due to Changes in R9

The temperature coefficient of R9 (TCR) will produce errors in the output current. Changes in R9 may be caused by self-heating of the device or by ambient temperature changes.

$$\frac{\Delta I_S}{I_{SPAN}}(\text{in }\%) = 100\,\frac{\Delta R9}{\Delta T}\,(\theta\, P_{DISS} + \Delta T_A)$$

Where:

θ = Thermal resistance either from junction-to-ambient or junction-to-case

ΔP_{DISS} = Change in average power dissipation

ΔT_A = Change in ambient temperature

$\dfrac{\Delta R9}{\Delta T}$ = TCR of R9

Using the LH0045G design example, $\Delta R9/\Delta T$ = 0.03%/°C, hence a 3.2% worst case error in output current might be expected for operation without a heat sink over the temperature range.

Heat sinking the device and using R_L = 800Ω, reduces $\Delta I_S/I_{SPAN}$ to 2.3%. Comparable error for the LH0045K would also be about 2.3%.

The error analysis indicates that the internal current set resistor, R9 is inadequate to satisfy high accuracy design criterion. In these instances, an external 100Ω resistor should be substituted for R9.

Obviously, the TCR of the resistor should be low. Metal film or wire-wound resistors are the best choice offering TCR's less than 10 ppm/°C versus 50 ppm/°C typical drift for R9.

External Causes of Error

The components external to the LH0045 are also critical in determining errors. Specifically, the composition of resistors R_{B1}, R_{OS}, R_F, R, etc. in the design example will influence both drift and long term stability.

In particular, resistors and potentiometers of wire wound construction are recommended. Also, metal-film resistors with low TCR (≤ 10 ppm/°C) may be used for fixed resistor applications.

Error Analysis Summary

The overall errors attributable to the LH0045 may be minimized using heat sinking, and utilization of an external load resistor. Although R_L reduces the compliance of the circuit, its use is generally advisable in precision applications. External components should be selected for low TCR and long-term stability.

The design example errors, using an external 100Ω wire wound resistor for R9 equal:

$$\frac{\Delta I_S}{I_{SPAN}} = \underbrace{0.12\%}_{\Delta V_{REF}} + \underbrace{0.26\%}_{\Delta V_{OS}} + \underbrace{0.08\%}_{\Delta R9} = 0.46\%$$

SOCKETS AND HEAT SINKS

Mounting sockets, test sockets, and heat sinks are available for the G package and K package.

The following or their equivalents are recommended:

Sockets:

G – 12 lead TO-8:	Barnes Corp. #MGX-12 Textool #212-100-323
K – 8 lead TO-3:	Robinson Nugent #0002011 Wells #6010–20811

Heat Sinks

G – 12 lead TO-8:	Thermalloy #2240A Wakefield #215-CB
K – 8 lead TO-3:	IERC #LAIC 3B4V

Definition of Terms

Input Offset Voltage, V_{OS}: The voltage which must be applied between the input terminals through equal resistances to obtain 4.0 mA of supply (output) current.

Input Bias Current, I_B: The average of the two input currents.

Input Offset Current, I_{OS}: The difference in the current into the two input terminals when the supply (output) current is 4.0 mA.

Input Resistance, R_{IN}: The ratio of the change in input voltage to the change in input current at either input with the other input connected to 1.0 Vdc.

Open Loop Transconductance, g_{MOL}: The ratio of the supply (output) current SPAN to the input voltage required to produce that SPAN.

Open Loop Output Resistance, R_{OUT}: The ratio of a specified supply (output) voltage change to the resulting change in supply (output) current at the specified current level.

Common Mode Rejection Ratio, CMRR: The ratio of the change in input offset voltage to the peak-to-peak input voltage range.

Power Supply Rejection Ratio, PSRR: The ratio of the change in input offset voltage to the change in supply (output) voltage producing it.

Input Voltage Range, V_{IN}: The range of voltages on the input terminals for which the device operates within specifications.

Open Loop Supply Current, I_S: The supply current required with the signal amplifier A_2 biased off (inverting input positive, non-inverting input negative) and no load on the V_{REF} terminal. This represents a measure of the minimum low end signal current.

Reference Voltage Line Regulation, $\Delta V_{REF}/\Delta V_S$: The ratio of the change in V_{REF} to the peak-to-peak change in supply (output) voltage producing it.

Reference Voltage Load Regulation, $\Delta V_{REF}/\Delta I_{REF}$: The change in V_{REF} for a stipulated change in I_{REF}.

National Semiconductor

Operational Amplifiers/Buffers

LH0061/LH0061C 0.5 Amp Wide Band Operational Amplifier

General Description

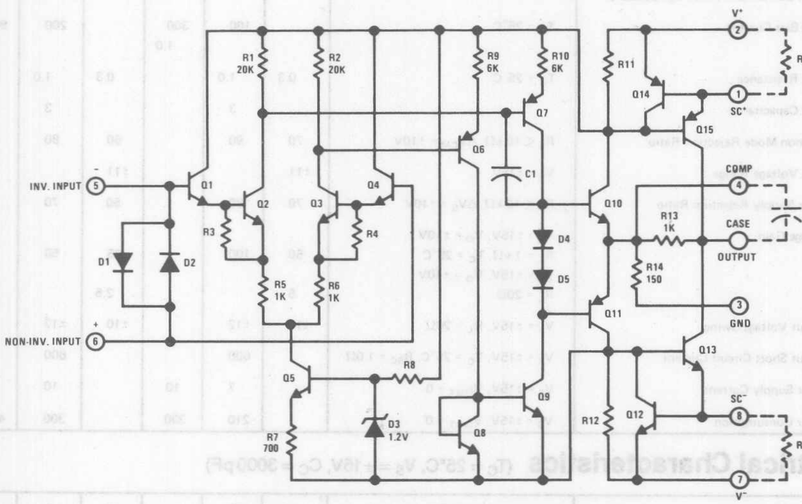
The LH0061/LH0061C is a wide band, high speed, operational amplifier capable of supplying currents in excess of 0.5 ampere at voltage levels of ±12V. Output short circuit protection is set by external resistors, and compensation is accomplished with a single external capacitor. With a suitable heat sink the device is rated at 20 Watts.

The wide bandwidth and high output power capabilities of the LH0061/LH0061C make it ideal for such applications as AC servos, deflection yoke drivers, capstan drivers, and audio amplifiers. The LH0061 is guaranteed over the temperature range -55°C to +125°C; whereas, the LH0061C is guaranteed from -25°C to +85°C.

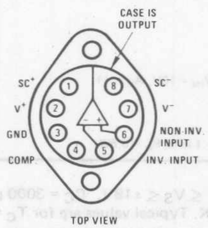
Features

- Output current — 0.5 Amp
- Wide large signal bandwidth — 1 MHz
- High slew rate — 70V/µs
- Low standby power — 240 mW
- Low input current — 300 nA Max

Schematic and Connection Diagrams



TO-3 Package



TOP VIEW

Order Numbers:
LH0061K (-55°C to +125°C)
LH0061CK (-25°C to +85°C)
See Package K08A

Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation	See Curve
Differential Input Current (Note 2)	±10 mA
Input Voltage (Note 3)	±15V
Peak Output Current	2A
Output Short Circuit Duration (Note 4)	Continuous
Operating Temperature Range LH0061	−55°C to +125°C
LH0061C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

DC Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	LIMITS LH0061 MIN	LH0061 TYP	LH0061 MAX	LH0061C MIN	LH0061C TYP	LH0061C MAX	UNITS
Input Offset Voltage	$R_S \leq 10\ k\Omega$, $T_C = 25°C$, $V_S = \pm 15V$		1.0	4.0		3.0	10	mV
	$R_S \leq 10\ k\Omega$, $V_S = \pm 15V$			6.0			15	mV
Voltage Drift with Temperature	$R_S \leq 10\ k\Omega$		5			5		µV/°C
Offset Voltage Change with Output Power			5			5		µV/watt
Input Offset Current	$T_C = 25°C$		30	100		50	200	nA
				300			500	nA
Offset Current Drift with Temperature			1			1		nA/°C
Input Bias Current	$T_C = 25°C$		100	300		200	500	nA
				1.0			1.0	µA
Input Resistance	$T_C = 25°C$	0.3	1.0		0.3	1.0		MΩ
Input Capacitance			3			3		pF
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$, $\Delta V_{CM} = \pm 10V$	70	90		60	80		dB
Input Voltage Range	$V_S = \pm 15V$	±11			±11			V
Power Supply Rejection Ratio	$R_S \leq 10\ k\Omega$, $\Delta V_S = \pm 10V$	70	80		50	70		dB
Voltage Gain	$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 1\ k\Omega$, $T_C = 25°C$	50	100		25	50		V/mV
	$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 20\Omega$	5			2.5			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 20\Omega$	±10	±12		±10	±12		V
Output Short Circuit Current	$V_S = \pm 15V$, $T_C = 25°C$, $R_{SC} = 1.0\Omega$		600			600		mA
Power Supply Current	$V_S = \pm 15V$, $V_{OUT} = 0$		7	10		10	15	mA
Power Consumption	$V_S = \pm 15V$, $V_{OUT} = 0$		210	300		300	450	mW

AC Electrical Characteristics ($T_C = 25°C$, $V_S = \pm 15V$, $C_C = 3000\ pF$)

PARAMETER	CONDITIONS	LH0061 MIN	LH0061 TYP	LH0061 MAX	LH0061C MIN	LH0061C TYP	LH0061C MAX	UNITS
Slew Rate	$A_V = +1$, $R_L = 100\Omega$	25	70		25	70		V/µs
Power Bandwidth	$R_L = 100\Omega$		1			1		MHz
Small Signal Transient Response			30			30		ns
Small Signal Overshoot			5	20		10	30	%
Settling Time (0.1%)	$\Delta V_{IN} = 10V$, $A_V = +1$		0.8			0.8		µs
Overload Recovery Time			1			1		µs
Harmonic Distortion	$f = 1\ kHz$, $P_O = 0.5W$		0.2			0.2		%

Note 1: Specifications apply for $\pm 5V \leq V_S \leq \pm 18V$, $C_C = 3000\ pF$, and $-55°C \leq T_C \leq +125°C$ for the LH0061K and $-25°C \leq T_C \leq +85°C$ for the LH0061CK. Typical values are for $T_C = 25°C$.

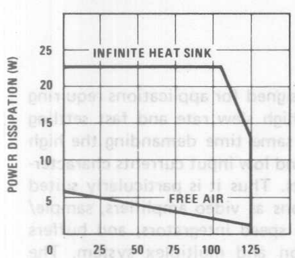
Note 2: The inputs are shunted with back-to-back diodes for overvoltage protection. Excessive current will flow if a differential voltage in excess of 1V is applied between the inputs without limiting resistors.

Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

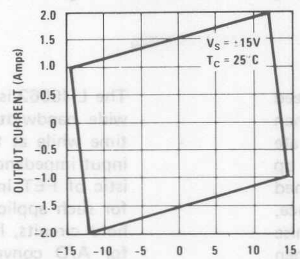
Note 4: Rating applies as long as package power rating is not exceeded.

Typical Performance Characteristics

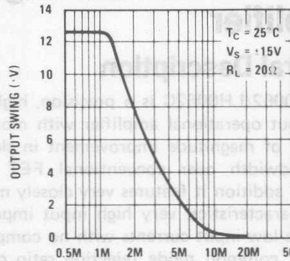
Power Derating



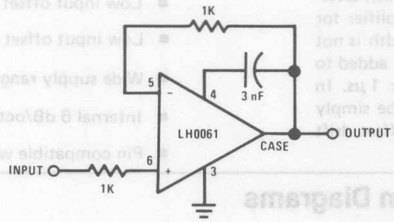
Safe Operating Area



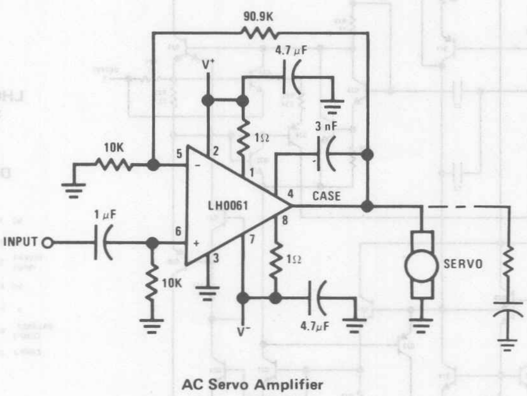
Large Signal Frequency Response



Typical Applications



Unity Gain Driver



AC Servo Amplifier

Semiconductor

LH0062/LH0062C High Speed FET Operational Amplifier

General Description

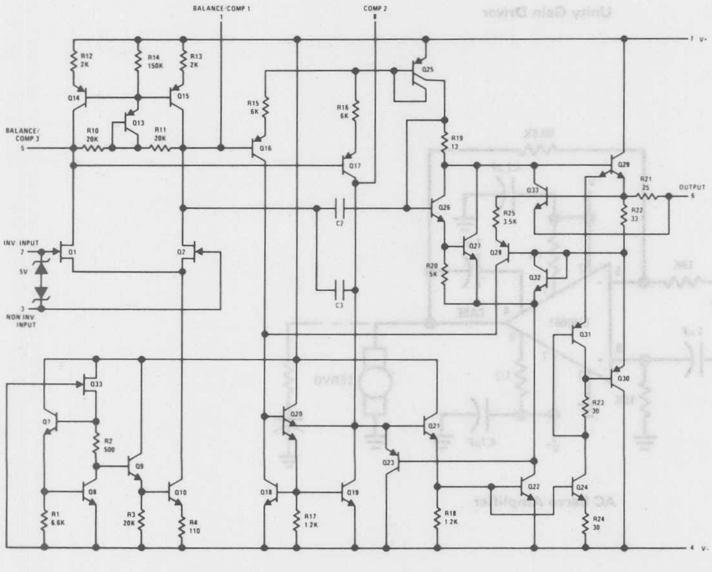
The LH0062/LH0062C is a precision, high speed FET input operational amplifier with more than an order of magnitude improvement in slew rate and bandwidth over conventional FET IC op amps. In addition it features very closely matched input characteristics, very high input impedance, and ultra low input currents with no compromise in noise, common mode rejection ratio or open loop gain. The device has internal unity gain frequency compensation, thus assuring stability in all normal applications. This considerably simplifies its application,. since no external components are necessary for operation. However, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. For inverting applications, feed-forward compensation will boost the slew rate to over 120 V/μs and almost double the bandwidth. (See LB-2, LB-14, and LB-17 for discussions of the application of feed-forward techniques). Overcompensation can be used with the amplifier for greater stability when maximum bandwidth is not needed. Further, a single capacitor can be added to reduce the 0.1% settling time to under 1 μs. In addition it is free of latch-up and may be simply offset nulled with negligible effect on offset drift or CMRR.

The LH0062 is designed for applications requiring wide bandwidth, high slew rate and fast settling time while at the same time demanding the high input impedance and low input currents characteristic of FET inputs. Thus it is particularly suited for such applications as video amplifiers, sample/hold circuits, high speed integrators, and buffers for A/D conversion and multiplex system. The LH0062 is specified for the full military temperature range of -55° to $+125^\circ$C while the LH0062C is specified to operate over a -25°C to $+85^\circ$C temperature range.

Features

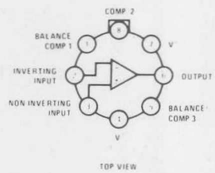
- High slew rate 70 V/μs
- Wide bandwidth 15 MHz
- Settling time (0.1%) 1μs
- Low input offset voltage 2 mV
- Low input offset current 1 pA
- Wide supply range ±5V to ±20V
- Internal 6 dB/octave frequency compensation
- Pin compatible with std IC op amps (TO-5 pkg)

Schematic and Connection Diagrams



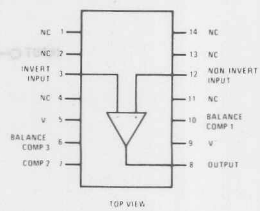
*Pin Numbers Shown for TO-5 Package

Metal Can Package



Order Number LH0062H or LH0062CH See Package H08A

Dual-In-Line Package



Order Number LH0062D or LH0062CD See Package D14E

Absolute Maximum Ratings

Supply Voltage	±20V	Operating Temperature	
Power Dissipation (see graph)	500 mW	LH0062,	−55°C to +125°C
Input Voltage (Note 1)	±5V	LH0062C,	−25°C to +85°C
Differential Input Voltage (Note 2)	±30V	Storage Temperature Range	−65°C to +150°C
Short Circuit Duration	Continuous	Lead Temperature (Soldering, 10 sec)	300°C

DC Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	LIMITS LH0062 MIN	LH0062 TYP	LH0062 MAX	LH0062C MIN	LH0062C TYP	LH0062C MAX	UNITS
Input Offset Voltage	$R_S \leq 100\ k\Omega$; $T_A = 25°C$		2	5		10	15	mV
	$R_S \leq 100\ k\Omega$			7			20	mV
Temperature Coefficient of Input Offset Voltage	$R_S \leq 100\ k\Omega$		5	25		10	35	μV/°C
Offset Voltage Drift with Time			4			5		μV/week
Input Offset Current	$T_A = 25°C$		0.2	2		1	5	pA
				2			0.2	nA
Temperature Coefficient of Input Offset Current			Doubles every 10°C			Doubles every 10°C		
Offset Current Drift with Time			0.1			0.1		pA/week
Input Bias Current	$T_A = 25°C$		5	10		10	65	pA
				10			2	nA
Temperature Coefficient of Input Bias Current			Doubles every 10°C			Doubles every 10°C		
Differential Input Resistance			10^{12}			10^{12}		Ω
Common Mode Input Resistance			10^{12}			10^{12}		Ω
Input Capacitance			4			4		pF
Input Voltage Range	$V_S = \pm 15V$	±10	±12		±10	±12		V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$, $V_{IN} = \pm 10V$	80	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$, $\pm 5V \leq V_S \leq \pm 15V$	80	90		70	90		dB
Large Signal Voltage Gain	$R_L = 2\ k\Omega$, $V_{OUT} = \pm 10V$, $T_A = 25°C$, $V_S = \pm 15V$	50	200		25	160		V/mV
	$R_L = 2\ k\Omega$, $V_{OUT} = \pm 10V$, $V_S = \pm 15V$	25			25			V/mV
Output Voltage Swing	$R_L = 2\ k\Omega$, $T_A = 25°C$, $V_S = \pm 15V$	±12	±13		±12	±13		V
	$R_L = 2\ k\Omega$, $V_S = \pm 15V$	±10			±10			V
Output Current Swing	$V_{OUT} = \pm 10V$, $T_A = 25°C$	±10	±15		±10	±15		mA
Output Resistance			75			75		Ω
Output Short Circuit Current	$T_A = 25°C$		25			25		mA
Supply Current	$V_S = \pm 15V$		5	8		7	12	mA
Power Consumption	$V_S = \pm 15V$			240			360	mW

AC Electrical Characteristics ($T_A = 25°C$, $V_S = \pm 15V$)

PARAMETER	CONDITIONS	LIMITS LH0062 MIN	LH0062 TYP	LH0062 MAX	LH0062C MIN	LH0062C TYP	LH0062C MAX	UNITS
Slew Rate	Voltage Follower	50	70		50	70		V/μs
Large Signal Bandwidth	Voltage Follower		2			2		MHz
Small Signal Bandwidth			15			15		MHz
Rise Time			25			25		ns
Overshoot			10			15		%
Settling Time (0.1%)	$\Delta V_{IN} = 10V$		1			1		μs
Overload Recovery			0.9			0.9		μs
Input Noise Voltage	$R_S = 10\ k\Omega$, $f_o = 10\ Hz$		150			150		$nV/\sqrt{Hz}$
Input Noise Voltage	$R_S = 10\ k\Omega$, $f_o = 100\ Hz$		55			55		$nV/\sqrt{Hz}$
Input Noise Voltage	$R_S = 10\ k\Omega$, $f_o = 1\ kHz$		35			35		$nV/\sqrt{Hz}$
Input Noise Voltage	$R_S = 10\ k\Omega$, $f_o = 10\ kHz$		30			30		$nV/\sqrt{Hz}$
Input Noise Voltage	BW = 10 Hz to 10 kHz, $R_S = 10\ k\Omega$		12			12		μVrms
Input Noise Current	BW = 10 Hz to 10 kHz		<.1			<.1		pArms

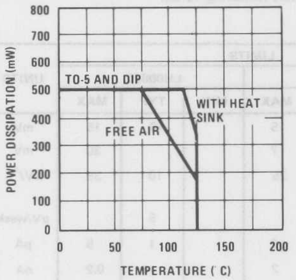
Note 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 2: Inputs are protected from excessive voltages by back-to-back diodes. Input currents should be limited to 1 mA.

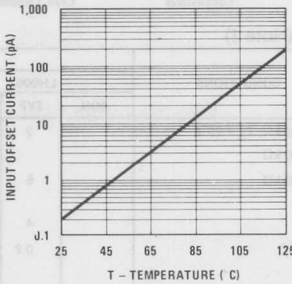
Note 3: Unless otherwise specified, these specifications apply for $\pm 5V \leq V_S \leq \pm 20V$ and $-55°C \leq T_A \leq +125°C$ for the LH0062 and $-25°C \leq T_A \leq +85°C$ for LH0062C. Typical values are given for $T_A = 25°C$. Power supplies should be bypassed with 0.1 μF ceramic capacitors.

Typical Performance Characteristics

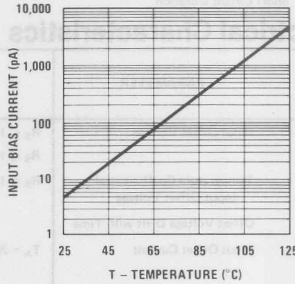
Maximum Power Dissipation



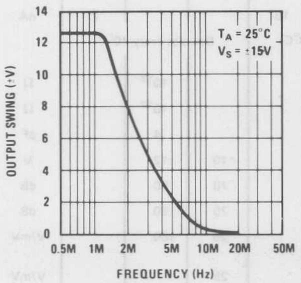
Input Offset Current vs Temperature



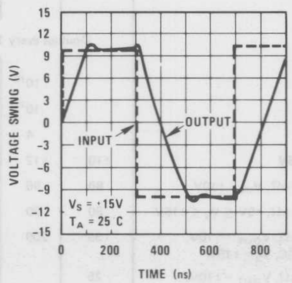
Input Bias Current vs Temperature



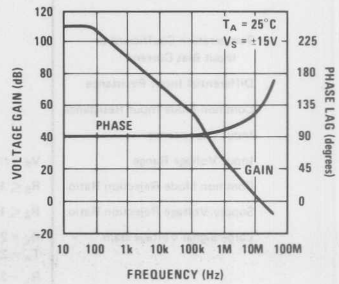
Large Signal Frequency Response



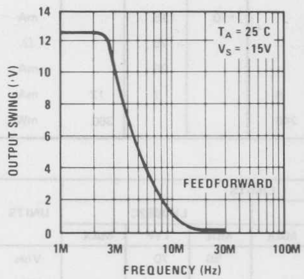
Voltage Follower Pulse Response



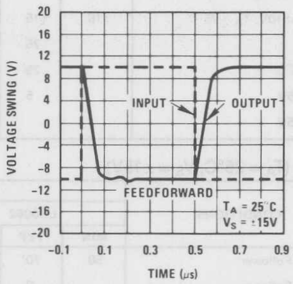
Open Loop Frequency Response



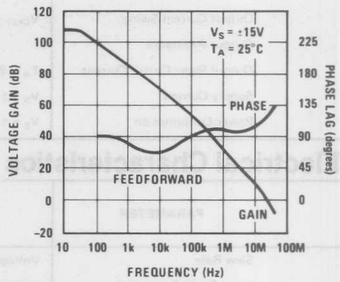
Large Signal Frequency Response



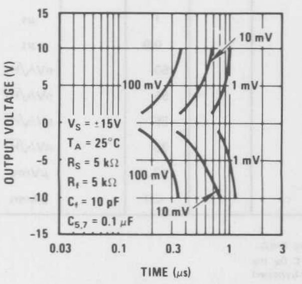
Inverter Pulse Response



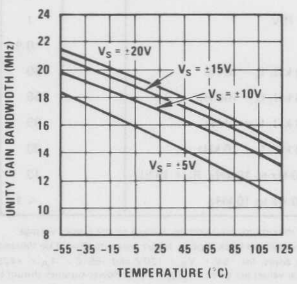
Open Loop Frequency Response



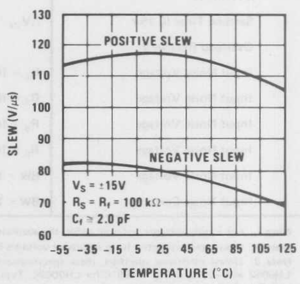
Inverter Settling Time



Unity Gain Bandwidth

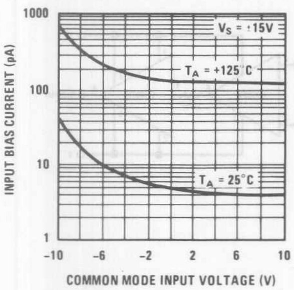


Voltage Follower Slew Rate

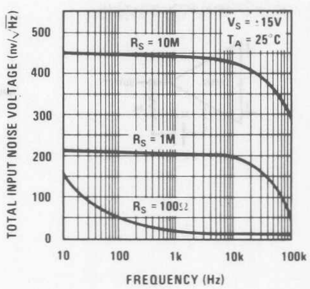


Typical Performance Characteristics (Cont'd)

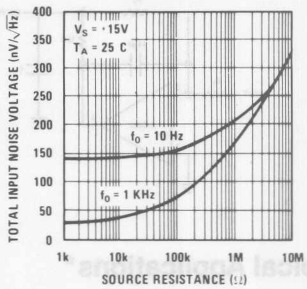
Input Bias Current vs Input Voltage



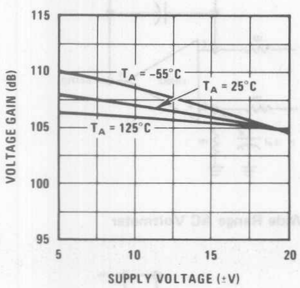
Total Input Noise Voltage* vs Frequency



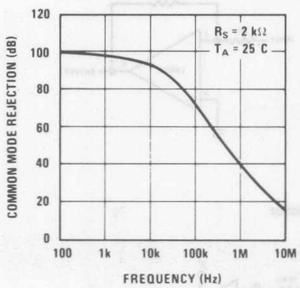
Total Input Noise Voltage* vs Source Resistance



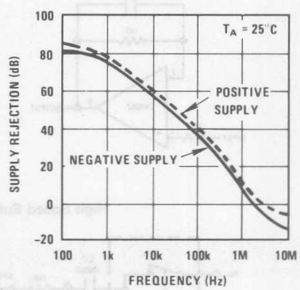
Voltage Gain



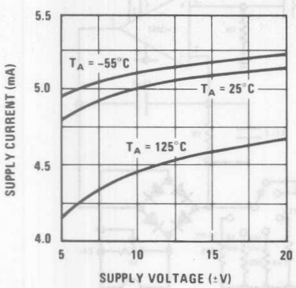
Common Mode Rejection



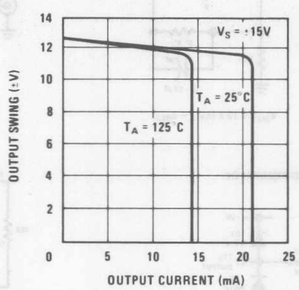
Power Supply Rejection



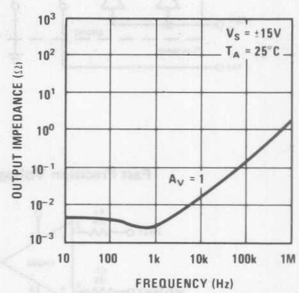
Supply Current



Current Limiting



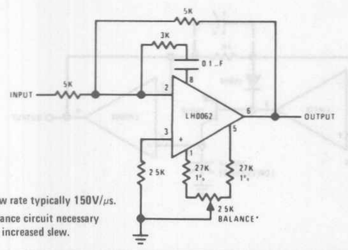
Closed Loop Output Impedance



*Noise Voltage Includes Contribution from Source Resistance

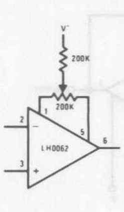
Auxiliary Circuits

Feedforward Compensation for Greater Inverting Slew Rate†

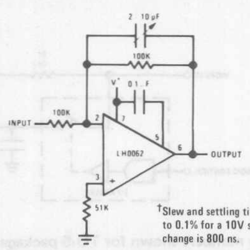


†Slew rate typically 150V/µs.
*Balance circuit necessary for increased slew.

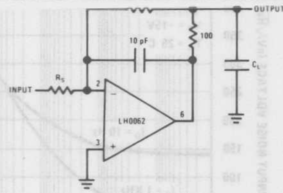
Offset Balancing

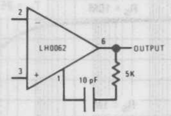


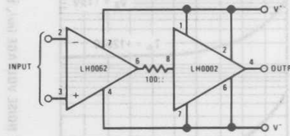
Compensation for Minimum Settling† Time



†Slew and settling time to 0.1% for a 10V step change is 800 ns.

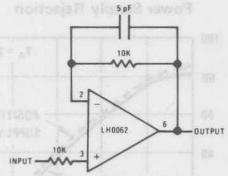




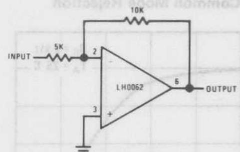


Typical Applications*

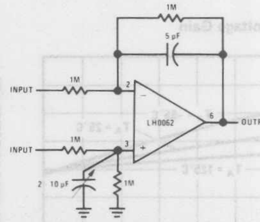
Fast Voltage Follower



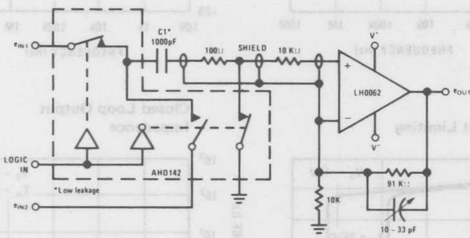
Fast Summing Amplifier



Differential Amplifier

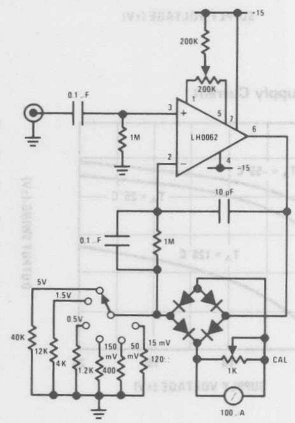


High Speed Subtractor

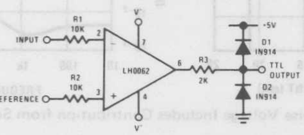


$e_{OUT} = 10 \times (e_{IN1} - e_{IN2})$

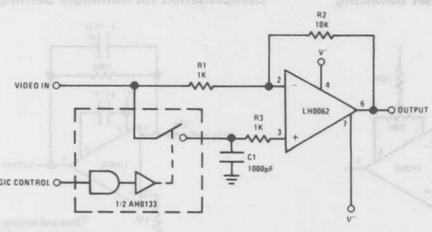
Wide Range AC Voltmeter



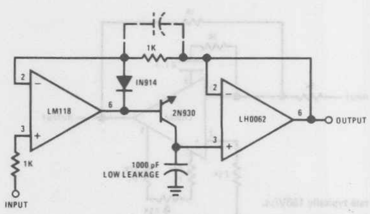
Fast Precision Voltage Comparator



Video DC Restoring Amplifier



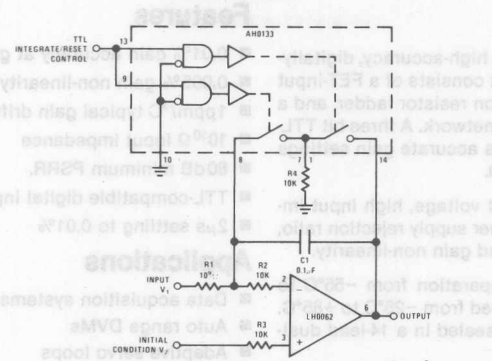
High Speed Positive Peak Detector



*Pin numbers shown for TO-5 package

Typical Applications* (Cont'd)

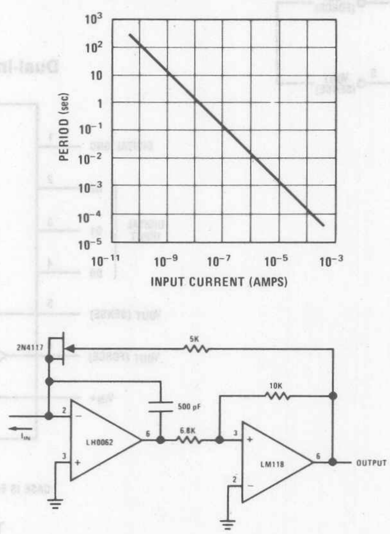
Precision Integrator



$$V_{OUT} = \frac{1}{C1R1} \int -V_1\,dt + V_2$$

*Pin numbers shown for TO-5 package

Precision Wide Range Current to Period Converter



National Semiconductor

LH0086/LH0086C Digitally-Programmable-Gain Amplifier

General Description

The LH0086 is a self-contained, high-accuracy, digitally-programmable-gain amplifier. It consists of a FET-input operational amplifier, a precision resistor ladder, and a digitally-programmable switch network. A three-bit TTL-compatible digital input selects accurate gain settings of 1, 2, 5, 10, 20, 50, 100, or 200.

The LH0086 exhibits low offset voltage, high input impedance, fast settling, high power supply rejection ratio, and excellent gain accuracy and gain non-linearity.

The LH0086 is specified for operation from −55°C to +125°C. The LH0086C is specified from −25°C to +85°C. Both devices are hermetically sealed in a 14-lead dual-in-line metal package.

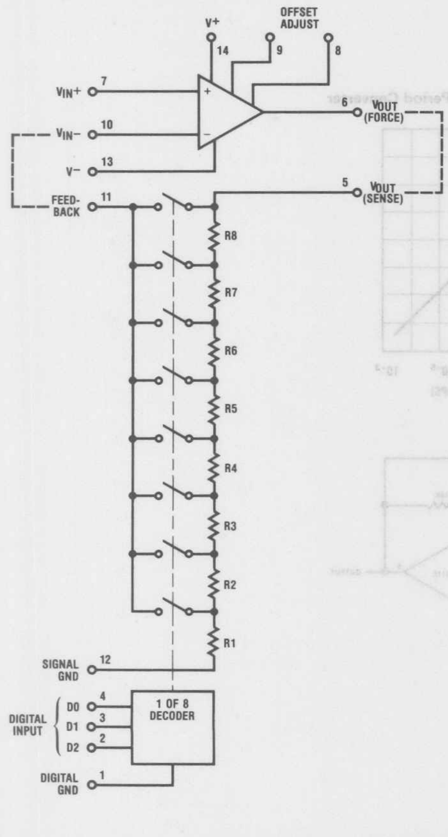
Features

- 0.01% gain accuracy at gain = 1
- 0.005% gain non-linearity
- 1 ppm/°C typical gain drift
- $10^{10}\,\Omega$ input impedance
- 80 dB minimum PSRR.
- TTL-compatible digital inputs
- 2 μs settling to 0.01%

Applications

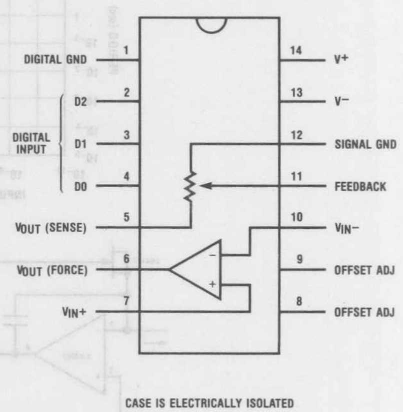
- Data acquisition systems
- Auto range DVMs
- Adaptive servo loops

Simplified Schematic



Connection Diagram

Dual-In-Line Package



Top View

Order Number LH0086D or LH0086CD
See NS Package D14F

Absolute Maximum Ratings

V_S	Supply Voltage (Note 1)	±18V
V_{IN}	Analog Input Voltage (Note 2)	±15V
$V_{IL(H)}$	Digital Input Voltage	−4V, $+V_S$
P_D	Power Dissipation	500 mW
	Output Short Circuit Duration	Continuous
T_A	Operating Temperature Range:	
	LH0086	−55°C to +125°C
	LH0086C	−25°C to +85°C
T_{STG}	Storage Temperature	−65°C to +150°C
	Lead Temperature (soldering, 20 seconds)	+300°C

DC Electrical Characteristics

$V_S = \pm 15V$, $R_L = 10\,k\Omega$, $T_{MIN} \leq T_A \leq T_{MAX}$, Pin 10 connected to Pin 11, Pin 5 connected to Pin 6 (Non-inverting)

	Parameter	Conditions		LH0086 Min.	LH0086 Typ.	LH0086 Max.	LH0086C Min.	LH0086C Typ.	LH0086C Max.	Units
V_{OS}	Input Offset Voltage		$T_J = 25°C$		0.3	5.0		0.3	10	mV
						7.0			13	
$V_{OS}/\Delta T$	Input Offset Voltage Change with Temperature	$V_{IN} = 0V$			10			10		µV/°C
I_B	Input Bias Current	(Notes 3, 4)	$T_J = 25°C$		100	500		100	500	pA
						500			100	nA
R_{IN}	Input Resistance				10			10		GΩ
V_{IN}	Input Voltage Range			±10	±11.5		±10	±11.5		V
A_V	Voltage Gain	See Table 1, p. 5, for Digital Gain-Control Codes			1.0			1.0		V/V
					2.0			2.0		
					5.0			5.0		
					10			10		
					20			20		
					50			50		
					100			100		
					200			200		
	Gain Error	$A_V = 1$	$T_A = 25°C$		0.003	0.01		0.003	0.03	%
		$A_V = 2,5$			0.03	0.05		0.05	0.1	
		$A_V = 10,20$			0.05	0.1		0.1	0.2	
		$A_V = 50,100,200$			0.1	0.2		0.15	0.3	
		$A_V = 1$			0.003	0.02		0.003	0.06	
		$A_V = 2,5$			0.03	0.1		0.05	0.2	
		$A_V = 10,20$			0.1	0.2		0.1	0.3	
		$A_V = 50,100,200$			0.15	0.3		0.15	0.4	
	Gain Non-Linearity	$A_V = 1$	$T_A = 25°C$		0.002			0.002		%
					0.005			0.005		
$\Delta A_V/\Delta T$	Gain Temperature Coefficient	$A_V = 1$			1.0			1.0		ppm/°C
PSRR	Power Supply Rejection Ratio	$\pm 8V \leq V_S \leq \pm 18V$		80	90		70	90		dB
V_O	Output Voltage Swing	$R_L \geq 10\,k\Omega$		±10	±12		±10	±12		V

Note 1: Improper supply power-on sequence may damage the device. See Power Supply Connection Section under Applications Information.

Note 2: For supply voltages less than ±15V the maximum input voltage is equal to the supply voltage.

Note 3: Due to short production test time, these parameters are specified at junction temperature, $T_J = 25°C$. In normal operation the junction temperature rises above the ambient temperature, T_A, as a result of the internal power dissipation, PD. $T_J = T_A + \theta_{jA} \times PD$ where θ_{jA} is the thermal resistance from junction to ambient (typically 65°C/W).

Note 4: The input bias currents are junction leakage currents which approximately double for every 10°C increase in junction temperature.

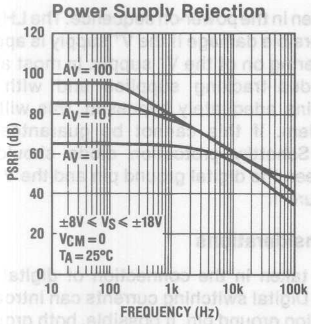
Parameter		Conditions	LH0086 Min.	LH0086 Typ.	LH0086 Max.	LH0086C Min.	LH0086C Typ.	LH0086C Max.	Units
I_{SC}	Output Short-Circuit Current	$T_A = 25°C$	±5	±18	±30	±5	±18	±30	mA
			±2		±30	±2		±30	mA
R_O	Output Resistance	$A_{VCL} = 1$		0.05			0.05		Ω
V_{IL}	Digital "0" Input Voltage				0.7			0.7	V
V_{IH}	Digital "1" Input Voltage		2.0			2.0			V
I_{IL}	Digital "0" Input Current	$V_{IN} = 0.4V$		1.5	4.0		1.5	4.0	μA
I_{IH}	Digital "1" Input Current	$V_{IN} = 2.4V$		0.01			0.01		μA
V_S	Supply Voltage Range		±8.0		±18	±8.0		±18	V
$I_S^{(+)}$	Positive Supply Current	$V_S = ±18V$		8.5	15.5		8.5	15.5	mA
$I_S^{(-)}$	Negative Supply Current	$V_S = ±18V$		−4.5	−8.5		−4.5	−8.5	mA

AC Electrical Characteristics

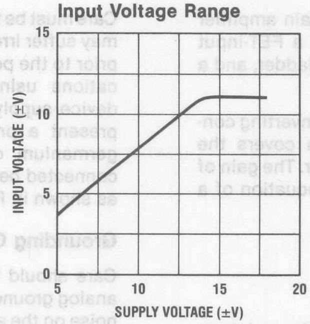
$V_S = ±15V$, $T_A = 25°C$, $R_L = 10 k\Omega$, Pin 10 connected to Pin 11, Pin 5 connected to Pin 6 (Non-inverting)

Parameter		Conditions		Min.	Typ.	Max.	Units
BW	Small Signal Bandwidth	−3dB	$A_V = 1$		3000		kHz
		−3dB	$A_V = 50$		60		kHz
		−3dB	$A_V = 200$		15		kHz
		−1%	$A_V = 1$		425		kHz
		−1%	$A_V = 50$		8.5		kHz
		−1%	$A_V = 200$		2		kHz
PBW	Power Bandwidth	$V_O = ±10V$			159		kHz
SR	Slew Rate	$V_O = ±10V$			10		V/μs
t_S	Settling Time (Figure 7) 0.01%	$\Delta V_O = 20V$	$A_V = 1$		2.5		μs
			$A_V = 50$		20		μs
			$A_V = 200$		75		μs
t_S	Settling Time After Gain Change				10		
$\overline{e}_N$	Equivalent Input Noise Voltage (Figure 6)	$R_S = 100\Omega$, $A_V = 100$	BW = 0.1–10Hz		3		$\mu V_{P\text{-}P}$
			f = 1kHz		25		$nV/\sqrt{Hz}$
$\overline{i}_N$	Equivalent Input Noise Current	$R_S = 100\Omega$, $A_V = 100$	f = 1kHz		0.01		$pA/\sqrt{Hz}$

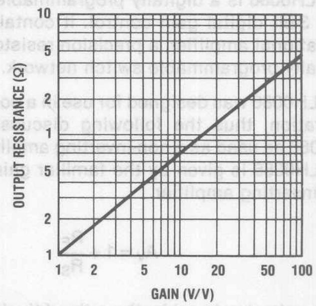
Power Supply Rejection



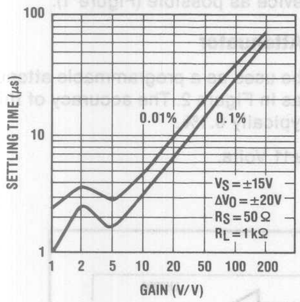
Input Voltage Range



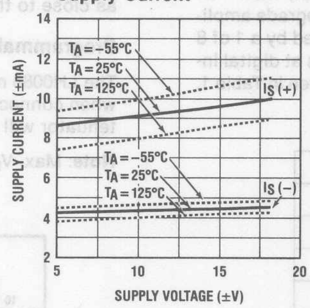
Closed Loop Output Resistance



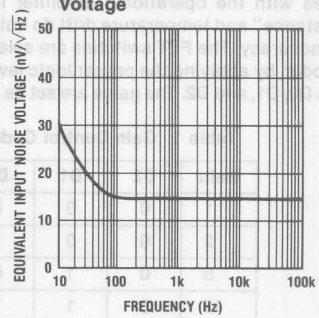
Settling Time



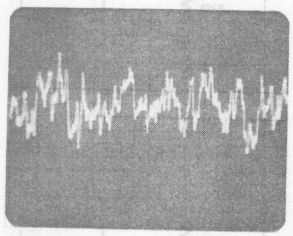
Supply Current



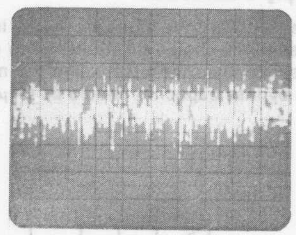
Equivalent Input Noise Voltage



Wideband Noise



$R_S = 50\Omega$. Bandwidth = 0.1 Hz to 10 Hz
1 μV/division Vertical, 5 seconds/division Horizontal



$R_S = 50\Omega$. Bandwidth = 10 Hz to 10 kHz
5 μV/division Vertical, 1 ms/division Horizontal

Applications Information

Theory of Operation

The LH0086 is a digitally programmable gain amplifier with 3-bit digital gain control. It contains a FET-input operational amplifier, a precision resistor ladder, and a digitally programmable switch network.

The LH0086 was designed for use in a non-inverting configuration, thus the following discussion covers the LH0086 as used as a non-inverting amplifier. The gain of the LH0086 is given by the familiar gain equation of a non-inverting amplifier.

$$A_V = 1 + \frac{R_F}{R_S}$$

Each gain step is set by the ratio of the ladder resistors. The resistor ladder is constructed with high stability, low temperature-coefficient resistors precision laser-trimmed to the required values. FET switches are used to select the desired ratio. Since the FET switches are in series with the operational amplifier input, their "on resistance" and temperature drift do not degrade amplifier accuracy. The FET switches are selected by a 1 of 8 decoder, by applying the proper logic levels at digital inputs D0, D1, and D2. The gains are set as given in Table 1.

Table 1. Gain-Control Codes

Gain	D2	D1	D0
1	0	0	0
2	0	0	1
5	0	1	0
10	0	1	1
20	1	0	0
50	1	0	1
100	1	1	0
200	1	1	1

Power Supply Connection

Proper power supply connections are shown in Figure 1. The power supplies should be bypassed to ground as close as possible to device supply pins. For most applications, the bypass capacitor should be 0.1μF.

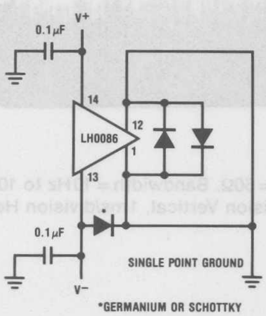


Figure 1. Power Supply and Ground Connections

Care must be taken in the power-on sequence. The LH0086 may suffer irreversible damage if the V^+ supply is applied prior to the powering on of the V^- supply. In most applications using dual-tracking supplies and with the device supply pins adequately bypassed, this will not present a problem. If this cannot be guaranteed, a germanium or Schottky protection diode should be connected between the digital ground pin and the V^- pin as shown in Figure 1.

Grounding Considerations

Care should be taken in the connection of digital and analog grounds. Digital switching currents can introduce noise on the analog ground pin. If possible, both grounds should go to a ground plane beneath the device, otherwise each ground should be run separately to a single point ground. The idea is to keep digital current from passing through the analog ground line. If long ground leads are used, diode clamps should be placed as close to the device as possible (Figure 1).

Programmable Attenuator

The LH0086 may be used as a programmable attenuator when connected as in Figure 2. The accuracy of this attenuator will be typically 0.1%.

Note: Max. $V_{IN} = \pm 11$ Volts.

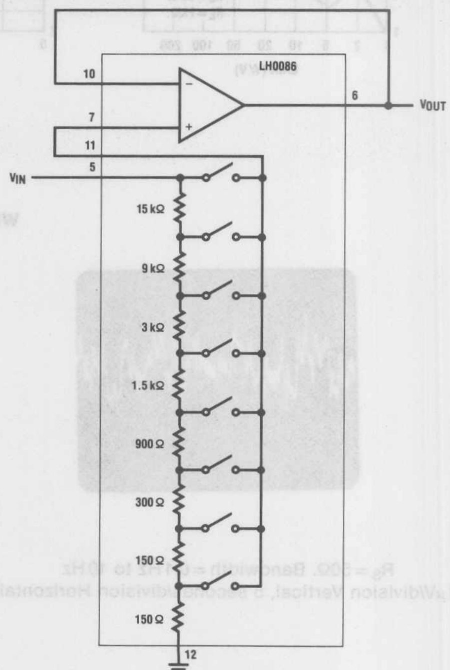


Figure 2. Programmable Attenuator

Table 2. Attenuator Codes

D2	D1	D0	Attenuation
0	0	0	1
0	0	1	2
0	1	0	5
0	1	1	10
1	0	0	20
1	0	1	50
1	1	0	100
1	1	1	200

Inverting Mode

The LH0086 may be used in the inverting mode, however, there are several design considerations.

1. Input resistance is low at high gains (see gain chart for input resistance at each gain).
2. Each gain step gets a one subtracted from the non-inverting gain. (See inverting gain chart for available gains.)
3. The first gain step (digital code of 000) cannot be used because the output will remain at virtual ground regardless of the input.

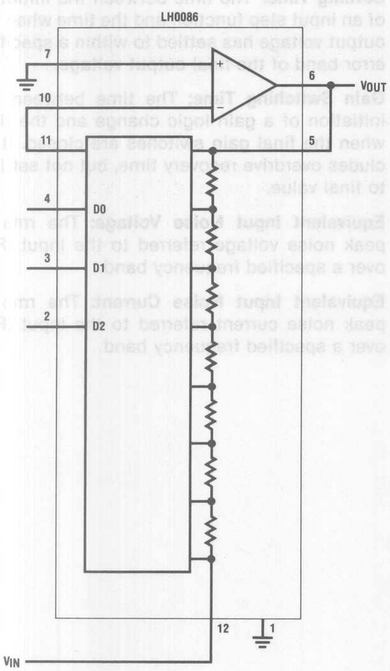


Figure 3. LH0086 Inverting Gain Configuration

Table 3. Inverting Gain Chart

D2	D1	D0	Gain	R_{IN} (Ω)
0	0	0	$A_V = 0$	30k
0	0	1	$A_V = 1$	15k
0	1	0	$A_V = 4$	6k
0	1	1	$A_V = 9$	3k
1	0	0	$A_V = 19$	1.5k
1	0	1	$A_V = 49$	600
1	1	0	$A_V = 99$	300
1	1	1	$A_V = 199$	150

Remote Output Sense

The V_{OUT} sense pin of the LH0086 should be connected at the load in order to eliminate errors due to lead resistance. In any case the output sense and output force must be tied together at some point. See Figure 4.

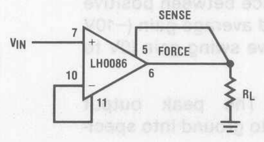


Figure 4. Remote Output Sense

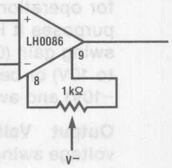


Figure 5. Offset Adjustment

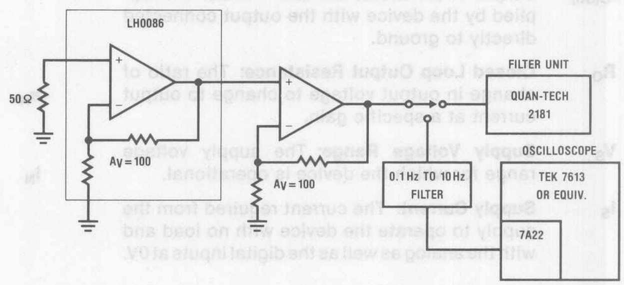


Figure 6. Noise Measurement Circuit

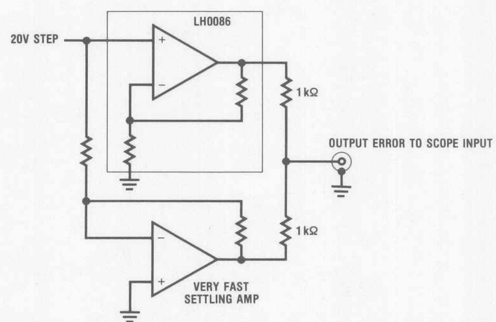


Figure 7. Settling Time Test Circuit

V_{OS} **Offset Voltage:** The voltage that must be applied to force the output to 0 volts.

I_B **Input Bias Current:** The current into Pin 7 with the device connected in the non-inverting configuration.

R_{IN} **Input Resistance:** The ratio of the change in input voltage to the change in input current on either input with the other grounded.

V_{IN} **Input Voltage Range:** The voltage range for which the device is operational.

PSRR **Power Supply Rejection Ratio:** The ratio of the specified change in supply voltage to the change in input offset voltage over this range.

A_V **Voltage Gain:** The ratio of output voltage change to the input voltage change producing it.

Gain Error: The deviation in percent between the ideal voltage gain and the value obtained when the device is configured for that gain.

Gain Non-Linearity: The deviation of the gain from a straight line drawn through the end-points expressed as a percent of full scale (10V for operation with ±15V supplies). For testing purposes it is the difference between positive swing gain (0V to 10V) and average gain (−10V to 10V) or between negative swing gain (0V to −10V) and average gain.

V_O **Output Voltage Swing:** The peak output voltage swing referenced to ground into specified load.

$I_{O(SC)}$ **Output Short-Circuit Current:** The current supplied by the device with the output connected directly to ground.

R_O **Closed Loop Output Resistance:** The ratio of change in output voltage to change to output current at a specific gain.

V_S **Supply Voltage Range:** The supply voltage range for which the device is operational.

I_S **Supply Current:** The current required from the supply to operate the device with no load and with the analog as well as the digital inputs at 0V.

P_D **Power Dissipation:** The power dissipated in the device with no load and with the analog as well as the digital inputs at 0V.

V_{IH} **Digital "1" Input Voltage:** Minimum voltage required at the digital input to guarantee a high logic state.

V_{IL} **Digital "0" Input Voltage:** The current into a digital input at specified logic level.

$\Delta V_{OS}/\Delta T$ **Average Input Offset Voltage Drift:** The ratio of input offset voltage change from 25°C to either temperature extreme divided by the temperature range.

$\Delta A_V/\Delta T$ **Average Gain Temperature Coefficient:** The ratio in gain from 25°C to either temperature extreme divided by the temperature range.

BW **Bandwidth:** The frequency at which the voltage gain is reduced to 3 dB below the low frequency value.

PBW **Power Bandwidth:** Maximum frequency for which the output swing is a large signal sine-wave without noticeable distortion.

SR **Slew Rate:** The internally limited rate of change in output voltage with a large amplitude step function applied at the input.

t_S **Settling Time:** The time between the initiation of an input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

Gain Switching Time: The time between the initiation of a gain logic change and the time when the final gain switches are closed. It includes overdrive recovery time, but not settling to final value.

e_N **Equivalent Input Noise Voltage:** The rms or peak noise voltage referred to the input (RTI) over a specified frequency band.

i_N **Equivalent Input Noise Current:** The rms or peak noise current referred to the input (RTI) over a specified frequency band.

LH0101/LH0101C, LH0101A/LH0101AC Power Operational Amplifier

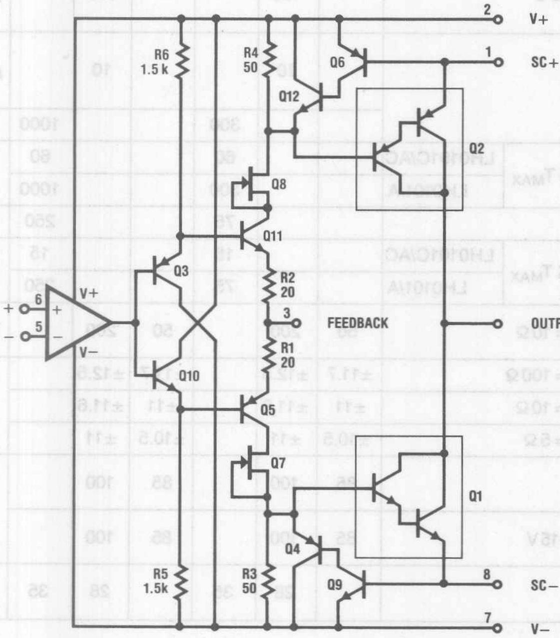
General Description

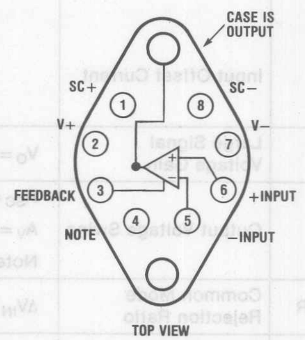
The LH0101 is a wideband power operational amplifier featuring FET inputs, internal compensation, virtually no crossover distortion, and rapid settling time. These features make the LH0101 an ideal choice for DC or AC servo amplifiers, deflection yoke drives, programmable power supplies, and disk head positioner amplifiers. The LH0101 is packaged in an 8 pin TO-3 hermetic package, rated at 20 watts with a suitable heat sink.

Features

- 5 Amp peak, 2 Amp continuous output current
- 300 kHz power bandwidth
- 850 mW standby power (±15V supplies)
- 300 pA input bias current
- 10 V/μS slew rate
- Virtually no crossover distortion
- 2μS settling time to 0.01%
- 5 MHz gain bandwidth

Schematic and Connection Diagrams





Order Numbers

LH0101CK

LH0101K

LH0101ACK

LH0101AK

See Package K08A

NOTE: ELECTRICALLY CONNECTED INTERNALLY, NO CONNECTION SHOULD BE MADE TO PIN.

Absolute Maximum Ratings

Supply Voltage, V_S	±22V
Power Dissipation at $T_A = 25°C$, P_D	5W
Derate linearly at 25°C/W to zero at 150°C,	
Power Dissipation at $T_C = 25°C$	62W
Derate linearly at 2°C/W to zero at 150°C	
Differential Input Voltage, V_{IN}	±40V but < ±V_S
Input Voltage Range, V_{CM}	±20V but < ±V_S
Peak Output Current (50ms pulse), $I_{O(PK)}$	5A
Output Short Circuit Duration (within rated power dissipation, $R_{SC} = 0.35\Omega$, $T_A = 25°C$)	Continuous
Operating Temperature Range, T_A	
LH0101, LH0101C	−25°C to +85°C
LH0101A, LH0101AC	−55°C to +125°C
Storage Temperature Range, T_{STG}	−65°C to +150°C
Maximum Junction Temperature, T_J	150°C
Lead Temperature (Soldering < 10 seconds)	300°C

DC Electrical Characteristics

(see Note 1) $V_S = \pm 15V$, $T_A = 25°C$ unless otherwise noted

Symbol	Parameter	Conditions	LH0101AC LH0101A Min.	Typ.	Max.	LH0101C LH0101 Min.	Typ.	Max.	Units
V_{OS}	Input Offset Voltage	$V_{CM} = 0$		1	3		5	10	mV
		$V_{CM} = 0$, $T_{MIN} \leq T_A \leq T_{MAX}$			7			15	mV
$\Delta V_{OS}/\Delta P_D$	Change in Input Offset Voltage with dissipated power	$V_{CM} = 0$, Note 2		150			300		μV/W
$\Delta V_{OS}/\Delta T$	Change in Input Offset Voltage with temperature	$V_{CM} = 0$		10			10		μV/°C
I_B	Input Bias Current	$V_{CM} = 0$			300			1000	pA
		$V_{CM} = 0$, $T_A \leq T_{MAX}$, LH0101C/AC			60			60	nA
		$V_{CM} = 0$, $T_A \leq T_{MAX}$, LH0101/A			300			1000	nA
I_{OS}	Input Offset Current	$V_{CM} = 0$			75			250	pA
		$V_{CM} = 0$, $T_A \leq T_{MAX}$, LH0101C/AC			15			15	nA
		$V_{CM} = 0$, $T_A \leq T_{MAX}$, LH0101/A			75			250	nA
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V$ $R_L = 10\Omega$	50	200		50	200		V/mV
V_O	Output Voltage Swing	$R_{SC} = 0$, $R_L = 100\Omega$	±11.7	±12.5		±11.7	±12.5		V
		$A_V = +1$, $R_L = 10\Omega$	±11	±11.6		±11	±11.6		V
		Note 3, $R_L = 5\Omega$	±10.5	±11		±10.5	±11		V
CMRR	Common Mode Rejection Ratio	$\Delta V_{IN} = \pm 10V$	85	100		85	100		dB
PSRR	Power Supply Rejection Ratio	$\Delta V_S = \pm 5V$ to $\pm 15V$	85	100		85	100		dB
I_S	Quiescent Supply Current			28	35		28	35	mA

AC Electrical Characteristics See Note 1, $V_S = \pm 15V$, $T_A = 25°C$

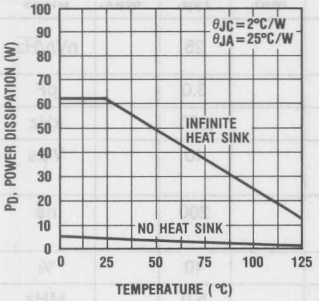
Symbol	Parameter	Conditions		LH0101AC LH0101A Min.	Typ.	Max.	LH0101C LH0101 Min.	Typ.	Max.	Units
e_n	Equivalent input noise voltage	f = 1 kHz			25			25		$nV/\sqrt{Hz}$
C_{in}	Input Capacitance	f = 1 MHz			3.0			3.0		pF
	Power Bandwidth, −3 dB	$R_L = 10\Omega$	$A_V = +1$		300			300		kHz
SR	Slew Rate	$R_L = 10\Omega$	$A_V = +1$	7.5 (note 4)	10			10		V/μs
t_r, t_f	Small Signal Rise or Fall Time	$R_L = 10\Omega$	$A_V = +1$		200			200		ns
	Small Signal Overshoot	$R_L = 10\Omega$	$A_V = +1$		10			10		%
GBW	Gain-Bandwidth Product	$R_L = \infty$	$A_V = +1$	4.0 (note 4)	5.0			5.0		MHz
t_s	Large Signal Settling Time to 0.01%	$R_L = \infty$	$A_V = +1$		2.0			2.0		μs
THD	Total Harmonic Distortion	$P_O = 0.5W$ f = 1 kHz $R_L = 10\Omega$			0.008			0.008		%

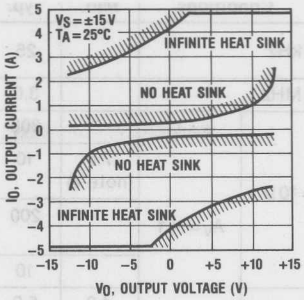
Note 1: Specification is at $T_A = 25°C$. Actual values at operating temperature may differ from the $T_A = 25°C$ value. When supply voltages are ±15V, quiescent operating junction temperature will rise approximately 20°C without heat sinking. Accordingly, V_{OS} may change 0.5 mV and I_B and I_{OS} will change significantly during warm-ups. Refer to the I_B vs. temperature and power dissipation graphs for expected values. Power supply voltage is ±15V. Temperature tests are made only at extremes.

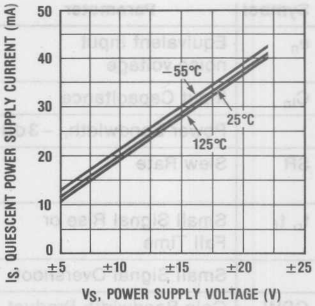
Note 2: Change in offset voltage with dissipated power is due entirely to average device temperature rise and not to differential thermal feedback effects. Test is performed without any heat sink.

Note 3: At light loads, the output swing may be limited by the second stage rather than the output stage. See the application section under "Output swing enhancement" for hints on how to obtain extended operation.

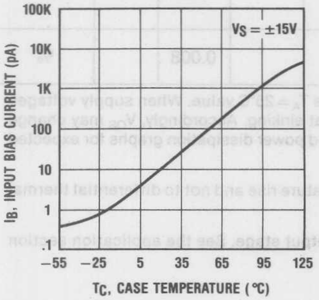
Note 4: These parameters are sample tested to 10% LTPD.



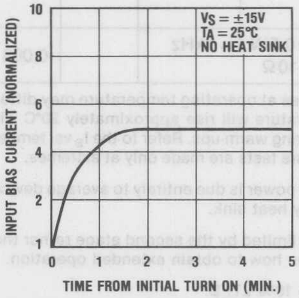




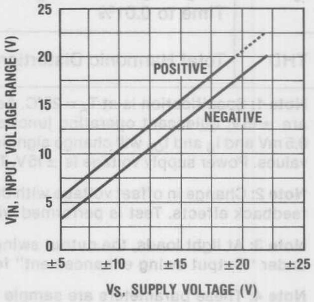
Input Bias Current



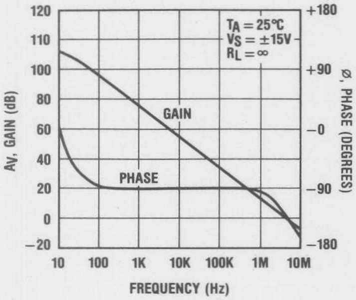
Input Bias Current after Warm-up



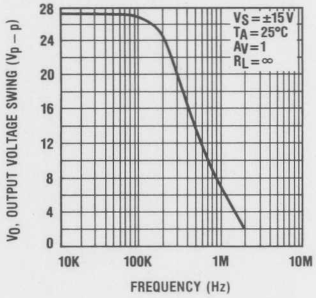
Input Common-Mode Voltage Range



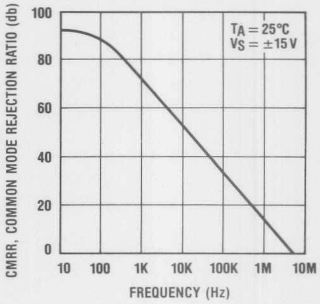
Small Signal Frequency Response (open loop)



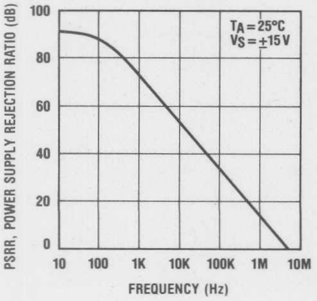
Output Voltage Swing vs. Frequency



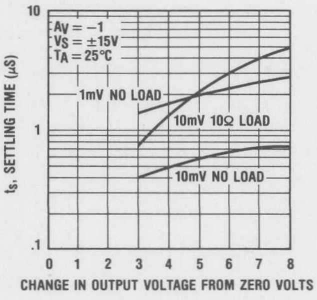
Common-Mode Rejection Ratio vs. Frequency



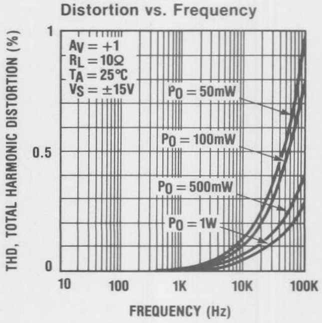
Power Supply Rejection Ratio vs. Frequency



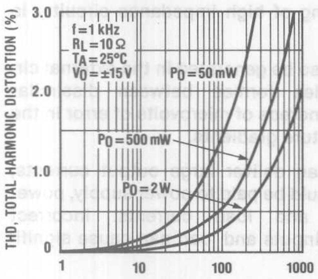
Settling Time



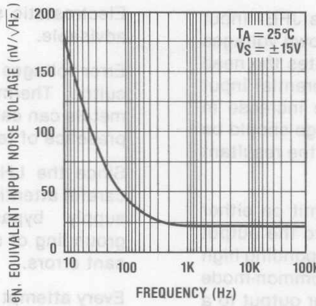
Total Harmonic Distortion vs. Frequency



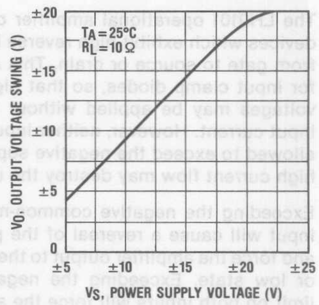
Total Harmonic Distortion vs. Gain



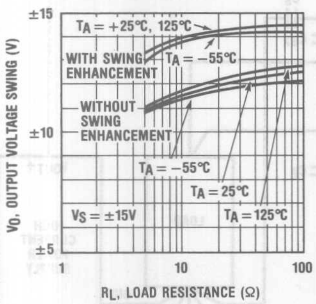
Equivalent Input Noise Voltage



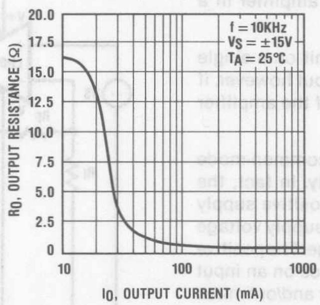
Output Voltage Swing with Swing Enhancement



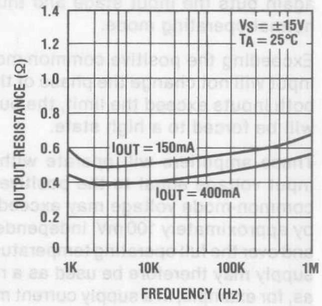
Output Voltage Swing vs. Load Resistance



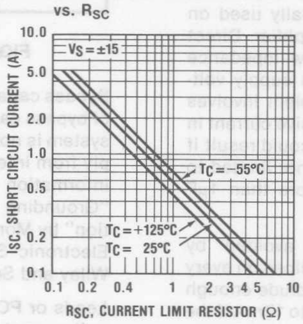
Open-Loop Output Resistance



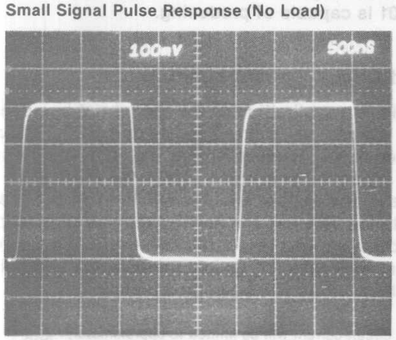
Open-Loop Output Resistance vs. Frequency



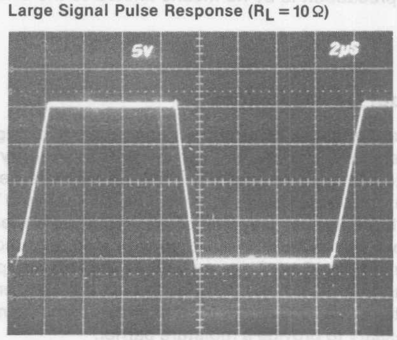
Short Circuit Current vs. R_{SC}



Small Signal Pulse Response (No Load)



Large Signal Pulse Response ($R_L = 10\Omega$)



Application Hints

Input Voltages

The LH0101 operational amplifier contains JFET input devices which exhibit high reverse breakdown voltages from gate to source or drain. This eliminates the need for input clamp diodes, so that high differential input voltages may be applied without a large increase in input current. However, neither input voltage should be allowed to exceed the negative supply as the resultant high current flow may destroy the unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage may exceed the positive supply by approximately 100 mV, independent of supply voltage and over the full operating temperature range. The positive supply may therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

With the LH0101 there is a temptation to remove the bias current compensation resistor normally used on the non-inverting input of a summing amplifier. Direct connection of the inputs to ground or a low-impedance voltage source is not recommended with supply voltages greater than 3V. The potential problem involves loss of one supply which can cause excessive current in the second supply. Destruction of the IC could result if the current to the inputs of the device is not limited to less than 100 mA or if there is much more than 1 μF bypass on the supply buss.

Although difficulties can be largely avoided by installing clamp diodes across the supply lines on every PC board, a conservative design would include enough resistance in the input lead to limit current to 10 mA if the input lead is pulled to either supply by internal currents. This precaution is by no means limited to the LH0101.

Layout Considerations

When working with circuitry capable of resolving picoampere level signals, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation is a must (Kel-F and Teflon rate high). Proper cleaning of all insulating surfaces to remove fluxes and other residues is also required. This includes the IC package as well as sockets and printed circuit boards. When operating in high humidity environments or near 0°C, some form of surface coating may be necessary to provide a moisture barrier.

The effects of board leakage can be minimized by encircling the input circuitry with a conductive guard ring operated at a potential close to that of the inputs.

Electrostatic shielding of high impedance circuitry is advisable.

Error voltages can also be generated in the external circuitry. Thermocouples formed between dissimilar metals can cause hundreds of microvolts of error in the presence of temperature gradients.

Since the LH0101 can deliver large output currents, careful attention should be paid to power supply, power supply bypassing and load currents. Incorrect grounding of signal inputs and load can cause significant errors.

Every attempt should be made to achieve a single point ground system as shown in the figure below.

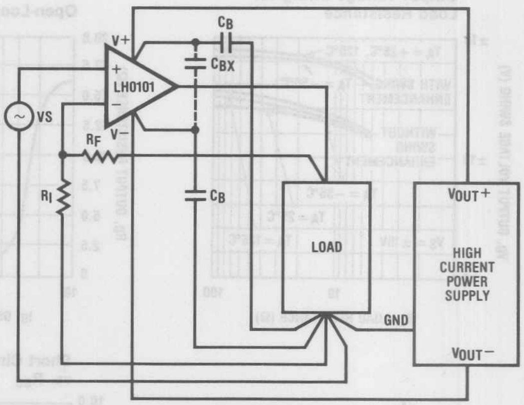


FIGURE 1. Single-Point Grounding

Bypass capacitor C_{BX} should be used if the lead lengths of bypass capacitors C_B are long. If a single point ground system is not possible, keep signal, load, and power supply from intermingling as much as possible. For further information on proper grounding techniques refer to "Grounding and Shielding Techniques in Instrumentation" by Morrison, and "Noise Reduction Techniques in Electronic Systems" by Ott (both published by John Wiley and Sons).

Leads or PC board traces to the supply pins, short-circuit current limit pins, and the output pin must be substantial enough to handle the high currents that the LH0101 is capable of producing.

Short Circuit Current Limiting

Should current limiting of the output not be necessary, SC+ should be shorted to V+ and SC− should be shorted to V−. Remember that the short circuit current limit is dependent upon the total resistance seen between the supply and current limit pins. This total resistance includes the desired resistor plus leads, PC Board traces, and solder joints.* Assuming a zero TCR current limit resistor, typical temperature coefficient of the short circuit will be approximately .3%.

*Short circuit current will be limited to approximately $\frac{0.6}{RSC}$.

Thermal Resistance

The thermal resistance between two points of a conductive system is expressed as:

$$\theta_{12} = \frac{T_1 - T_2}{P_D} \ {}^\circ C/W$$

where subscript order indicates the direction of heat flow. A simplified heat transfer circuit for a cased semiconductor and heat sink system is shown in the figure below.

The circuit is valid only if the system is in thermal equilibrium (constant heat flow) and there are, indeed, single specific temperatures T_J, T_C, and T_S (no temperature distribution in junction, case, or heat sink). Nevertheless, this is a reasonable approximation of actual performance.

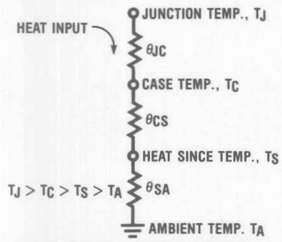


FIGURE 2. Semiconductor-Heat Sink Thermal Circuit

The junction-to-case thermal resistance θ_{JC} specified in the data sheet depends upon the material and size of the package, die size and thickness, and quality of the die bond to the case or lead frame. The case-to-heat sink thermal resistance θ_{CS} depends on the mounting of the device to the heat sink and upon the area and quality of the contact surface. Typical θ_{CS} for a TO-3 package is 0.5 to 0.7°C/W, and 0.3 to 0.5°C/W using silicone grease.

The heat sink to ambient thermal resistance θ_{SA} depends on the quality of the heat sink and the ambient conditions

Cooling is normally required to maintain the worst case operating junction temperature T_J of the device below the specified maximum value $T_{J(MAX)}$. T_J can be calculated from known operating conditions. Rewriting the above equation, we find:

$$\theta_{JA} = \frac{T_J - T_A}{P_D} \ {}^\circ C/W$$

$$T_J = T_A + P_D \theta_{JA} \ {}^\circ C$$

Where: $P_D = (V_S - V_{OUT}) I_{OUT} + |V+ - (V-)| I_Q$

$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$ and V_S = Supply Voltage

θ_{JC} for the LH0101 is about 2°C/W.

Stability and Compensation

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time consistant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Some inductive loads may cause output stage oscillation. A .01 μF ceramic capacitor in series with a 10Ω resistor from the output to ground will usually remedy this situation.

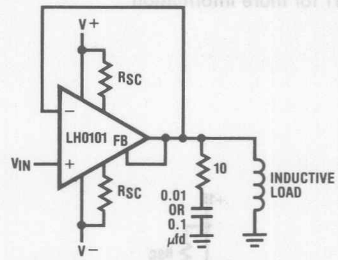


FIGURE 3. Driving Inductive Loads

Capacitive loads may be compensated for by traditional techniques. (See "Operational Amplifiers: Theory and Practice" by Roberge, published by Wiley):

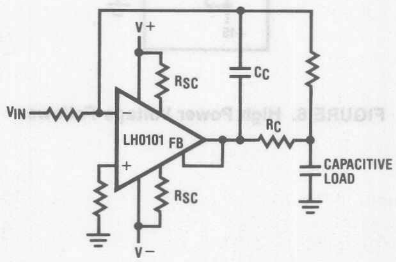


FIGURE 4. R_C and C_C Selected to Compensate for Capacitive Load

A similar but alternative technique may be used for the LH0101:

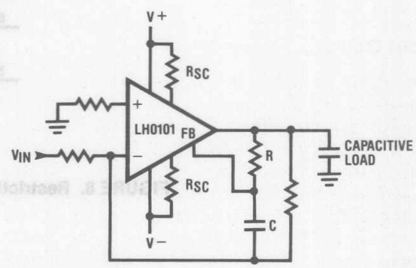


FIGURE 5. Alternate Compensation for Capacitive Load

stage and not by output saturation. Output swing can be increased as shown by taking gain in the output stage as shown in High Power Voltage Follower with Swing Enhancement below. Whenever gain is taken in the output stage, as in swing enhancement, either the output stage, or the entire op amp must be appropriately compensated to account for the additional loop gain.

Typical Applications

See AN261 for more information

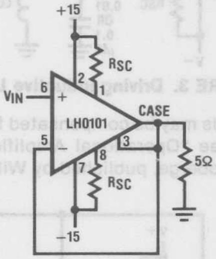


FIGURE 6. High Power Voltage Follower

approximately 10Ω. This decreases to under an ohm for load currents exceeding 100 mA.

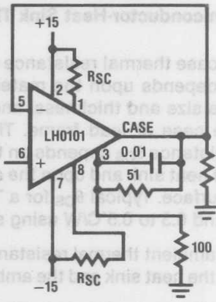


FIGURE 7. High Power Voltage Follower with Swing Enhancement

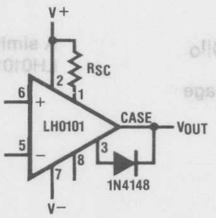


FIGURE 8. Restricting Outputs to Positive Voltages only

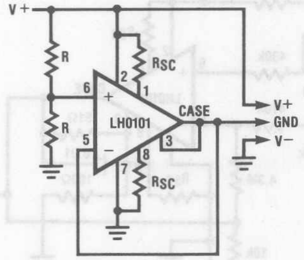


FIGURE 9. Generating a Split Supply from a Single Voltage Supply

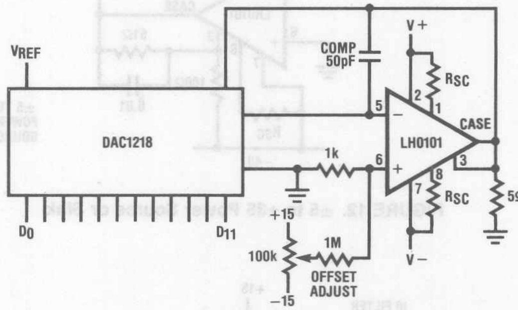


FIGURE 10. Power DAC

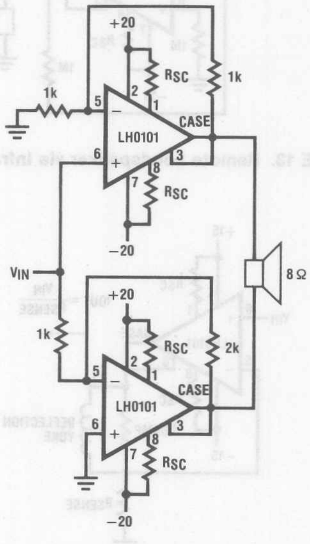


FIGURE 11. Bridge Audio Amplifier

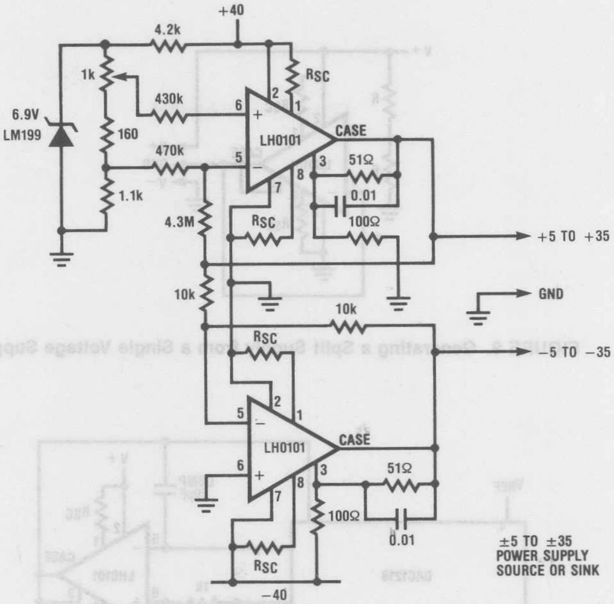


FIGURE 12. ±5 to ±35 Power Source or Sink

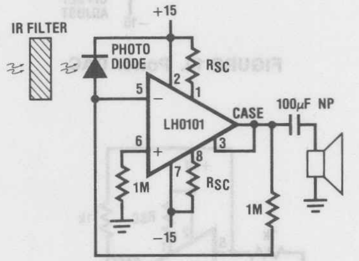


FIGURE 13. Remote Loudspeaker via Infrared Link

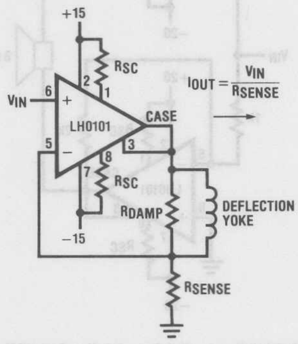


FIGURE 14. CRT Deflection Yoke Driver

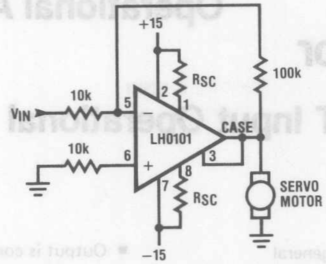


FIGURE 15. DC Servo Amplifier

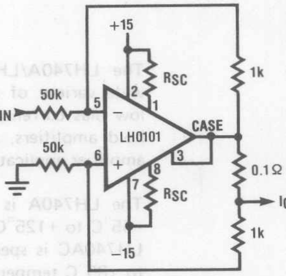


FIGURE 16. High Current Source/Sink

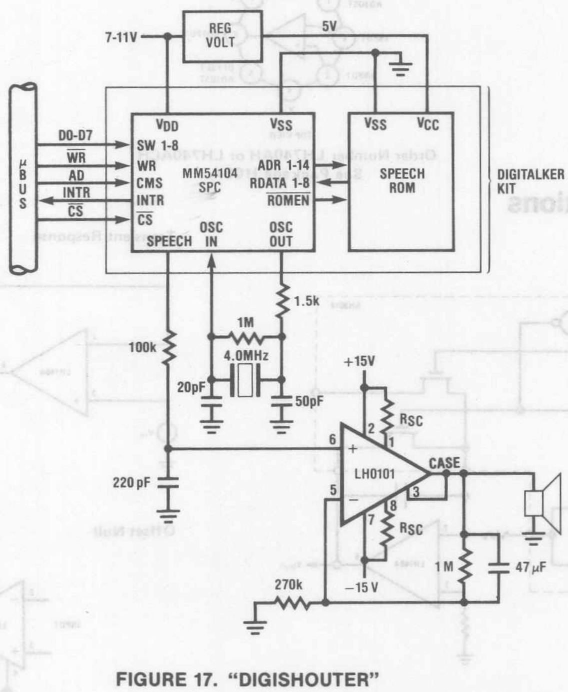


FIGURE 17. "DIGISHOUTER"

Semiconductor

LH740A/LH740AC FET Input Operational Amplifier

General Description

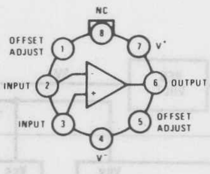
The LH740A/LH740AC is a FET input, general purpose operational amplifier with high input impedance, closely matched input characteristics, and good slew rates. Input offset voltage is typically 10.0 mV at 25°C, while input bias current is less than 100 pA at 25°C. Offset current is typically less than 40 pA at 25°C. Other important design features include:

- Internal 6 dB/octave frequency compensation
- Unity gain slew rate in excess of 6 V/µs
- Unity gain bandwidth of 1 MHz
- Input offset is adjustable with a single 10k pot
- **Pin compatible with LM741, LM709, LM101A.**
- Excellent offset current match over temperature, typically 100 pA
- Output is continuously short-circuit proof
- Excellent open loop gain, typically in excess of 100 dB
- Guaranteed over the full military temperature range

The LH740A/LH740AC is intended to fulfill a wide variety of applications requiring extremely low bias currents such as integrators, sample and hold amplifiers, and general purpose operational amplifier applications.

The LH740A is specified for operation over the –55°C to +125°C military temperature range. The LH740AC is specified for operation over the 0°C to +85°C temperature range.

Connection Diagram

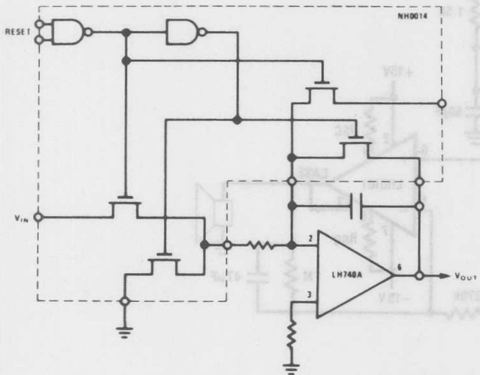


TOP VIEW

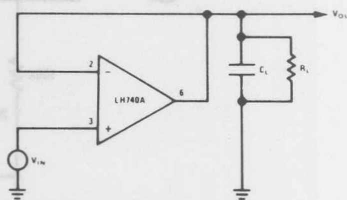
Order Number LH740AH or LH740ACH
See Package H08A

Typical Applications

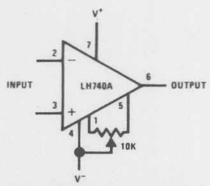
Integrator



Transient Response



Offset Null



Absolute Maximum Ratings

Supply Voltage		±22V
Maximum Power Dissipation		500 mW
Differential Input Voltage		±5V
Input Voltage		±15V
Short Circuit Duration		Continuous
Operating Temperature Range	LH740A	−55°C to +125°C
	LH740AC	0°C to +85°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (soldering, 10 sec.)		300°C

Electrical Characteristics (Note 1) ($V_S = \pm15V$, $T_A = 25°C$ unless otherwise noted)

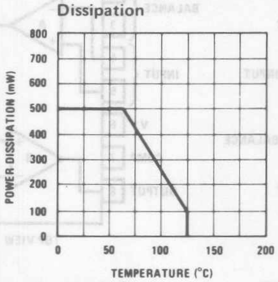
PARAMETER	CONDITIONS	LH740A MIN	LH740A TYP	LH740A MAX	LH740AC MIN	LH740AC TYP	LH740AC MAX	UNITS
Input Offset Voltage	$R_S \leq 100\ k\Omega$		10	15		10	20	mV
Input Offset Current	$T_J = 25°C$ (Note 2)		40	100		60	150	pA
Input Current (either input)	$T_J = 25°C$ (Note 2)		100	200		100	500	pA
Input Resistance	$T_J = 25°C$ (Note 2)		1,000,000			1,000,000		MΩ
Large Signal Voltage Gain	$R_L \geq 2\ k\Omega$, $V_{OUT} = \pm10V$	50,000	100,000		50,000	100,000		V/V
Output Resistance			75			75		Ω
Output Short-Circuit Current			20			20		mA
Common Mode Rejection Ratio		80			80			dB
Supply Voltage Rejection Ratio		80			80			dB
Supply Current			3.0	4.0		3.0	4.0	mA
Slew Rate			6.0			6.0		V/µs
Unity Gain Bandwidth			1.0			1.0		MHz
Transient Response (Unity Gain)	$C_L \leq 100\ pF$, $R_L = 2\ k\Omega$, $V_{IN} = 100\ mV$							
Risetime			110			300		ns
Overshoot			10	20		10		%
(These specifications apply for $-55°C \leq T_A \leq 125°C$ for the LH740A and $0°C \leq T_A \leq 85°C$ for the LH740AC unless otherwise noted.)								
Input Voltage Range		±12			±12			V
Common Mode Rejection Ratio		80			80			dB
Supply Voltage Rejection Ratio		80			80			dB
Large Signal Voltage Gain		40,000			40,000			V/V
Output Voltage Swing	$R_L \geq 10\ k\Omega$	±12	±14		±12	±14		V
	$R_L \geq 2\ k\Omega$	±10	±13		±10	±13		V
Input Offset Voltage			15	20		30		mV
Input Offset Current			100	500		60	500	pA
Input Current (either input)			2.5	4.0		1.1	5.0	nA
Offset Voltage Drift	$R_S \leq 100K$		5.0			5.0		µV/°C

Note 1: For supply voltages less than ±10V, the absolute maximum input voltage is equal to the supply voltage.

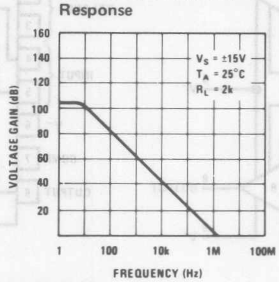
Note 2: Due to high speed automatic testing, these parameters are correlated to junction temperature.

Typical Performance Characteristics

Maximum Power Dissipation



Open Loop Frequency Response



National Semiconductor

Operational Amplifiers/Buffers

LH2011/LH2011B/LH2011C Dual Operational Amplifiers

General Description

The LH2011 series of dual operational amplifiers contain a pair of LM11 op amps in a single hermetic package, combining the best features of existing bipolar and FET op amps. The LH2011 is similar to the LH2108A, except that input currents have been reduced by more than a factor of ten. Offset voltage and drift have also been improved.

Compared to FETs, the device provides inherently lower offset voltage and offset voltage drift, along with at least an order of magnitude better long-term stability. Low frequency noise is also somewhat reduced. Bias current is significantly lower even under laboratory conditions, and the low drift makes compensation practical. Offset current is almost unmeasurable. Although not as fast as FETs, it does have a much lower power drain. This low dissipation has the added advantage of eliminating warm up time in critical applications.

Typical characteristics for 25°C (**−55°C** to **125°C**) are:

- Offset voltage: 100 μV (**200 μV**)
- Bias current: 25 pA (**65 pA**)
- Offset current: 0.5 pA (**3 pA**)
- Temperature drift: **1 μV/°C**
- Long-term stability: 10 μV/year

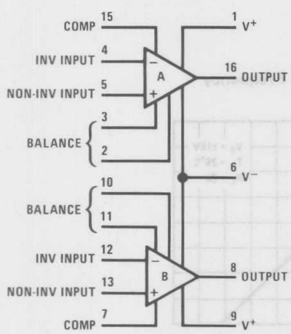
The LH2011 is internally compensated, but external compensation may be added for improved frequency stability, particularly with capacitive loads. Offset voltage balancing is also provided, with the balance range determined by a low-resistance potentiometer.

Otherwise, the device is the electrical equivalent of the LH2108, except that the negative common-mode limit is 0.6V less, performance is specified down to ±2.5V and the guaranteed output drive has been increased to ±2 mA. The input noise is somewhat higher, but amplifier noise is obscured by resistor noise with higher source resistances.

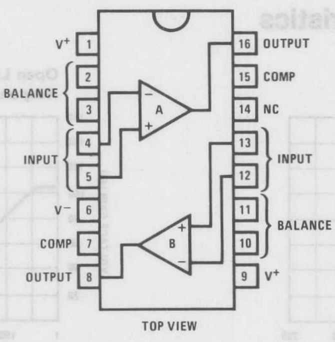
The LH2011 has applications as electrometer amplifiers, charge integrators, analog memories, low frequency active filters or for frequency shaping in slow servo loops. It can be substituted for existing circuits to provide improved performance or eliminate trimming operations. The greater precision can also be used to extend the dynamic range of logarithmic amplifiers, light meters and solid-state particle detectors.

The LH2011 is manufactured with standard bipolar processing using super-gain transistors.

Connection Diagrams

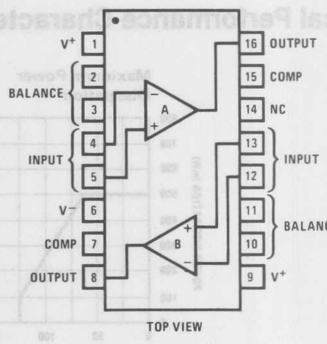


Dual-In-Line Package



Order Number LH2011D, LH2011BD, or LH2011CD
See Package D16C

Flat Package



Order Number LH2011F or LH2011BF
See Package F16B

Absolute Maximum Ratings

V_S	Total Supply Voltage	40V
I_{IN}	Input Current (Note 1)	± 10 mA
P_D	Power Dissipation at 25°C	500 mW
	Derate Linearly above 100°C at 100°C/W	
I_{SC}	Output Short-Circuit Duration (Note 2)	Indefinite
T_J	Junction Temperature	150°C
T_{stg}	Storage Temperature Range	− 65°C to + 150°C
T_A	Operating Temperature Range	
	LH2011CD	− 25°C to + 85°C
	LH2011D, LH2011F	− 55°C to + 125°C
	LH2011BD, LH2011BF	− 55°C to + 125°C
	Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics $V_S = \pm 15V$, $T_{MIN} \le T_J \le T_{MAX}$ unless noted.

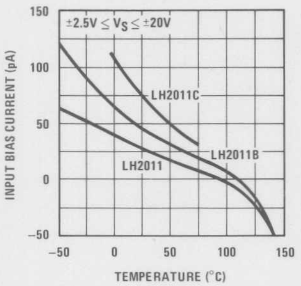
	Parameter	Conditions		LH2011 Min	LH2011 Typ	LH2011 Max	LH2011B Min	LH2011B Typ	LH2011B Max	LH2011C Min	LH2011C Typ	LH2011C Max	Units
V_{OS}	Input Offset Voltage	Note 3	$T_J = 25°C$		0.1	0.3		0.2	0.6		0.5	1	mV
						0.6			1.1			1.3	
I_{OS}	Input Offset Current	Note 3	$T_J = 25°C$		0.5	10		1	10		4	25	pA
						30			30			50	
I_B	Input Bias Current	Note 3	$T_J = 25°C$		25	50		40	100		70	180	pA
						150			300			400	
R_{IN}	Input Resistance				10^{11}			10^{11}			10^{11}		Ω
$\Delta V_{OS}/\Delta T$	Offset Voltage Drift				1	3		2	5		3		μV/°C
$\Delta I_B/\Delta T$	Bias Current Drift	Note 4			0.5	1.5		0.8	3		1.4		pA/°C
$\Delta I_{OS}/\Delta T$	Offset Current Drift				20			20			50		fA/°C
A_V	Large Signal Voltage Gain	$V_S = \pm 15V$, $I_O = \pm 2$ mA	$T_J = 25°C$, $V_O = \pm 12V$	100	300		100	300		50	300		V/mV
		$V_O = \pm 11.5V$		50			50			15			
		$V_S = \pm 15V$, $I_O = \pm 0.5$ mA	$T_J = 25°C$, $V_O = \pm 12V$	250	1200		250	1200		90	800		
		$V_O = \pm 11.5V$		100			100			30			
CMRR	Common-Mode Rejection		$T_J = 25°C$	110	130		110	130		96	110		dB
		$V_{CM} = -13V, +14V$		100			100			90			
PSRR	Power Supply Rejection Ratio		$T_J = 25°C$	100	118		100	118		84	100		dB
		$V_S = \pm 2.5V$ to $\pm 20V$		96			96			80			
I_S	Supply Current		$T_J = 25°C$		0.3	0.6		0.3	0.8		0.3	0.8	mA
						0.8			1			1	
I_{SC}	Output Short Circuit Current	$T_J = T_{MAX}$			±15			±15			±15		mA

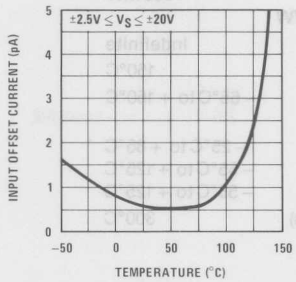
Note 1: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used. In addition, a 2 kΩ minimum resistance in each input is advised to avoid possible latch-up initiated by supply reversals.

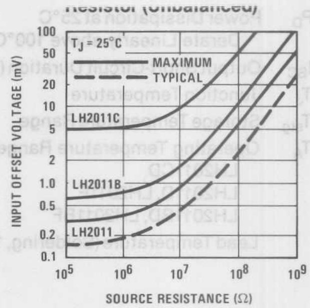
Note 2: Current limiting protects the output when it is shorted to ground or any voltage less than the supplies. With continuous overloads, package dissipation must be taken into account and heat sinking provided when necessary.

Note 3: These specifications apply for test at $V_S = \pm 15V$ and $V_{CM} = -12.5V$ (− 13V at 25°C), 14V; $V_S = \pm 20V$ and $V_{CM} = 0V$; in addition, V_{OS} is also tested at $V_S = \pm 2.5V$ and $V_{CM} = 0V$.

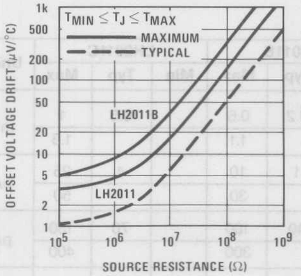
Note 4: Drift parameters are sample tested to 5% LTPD at the same conditions as Note 3. The values are average-calculated from measurements at 25°C and 125°C.



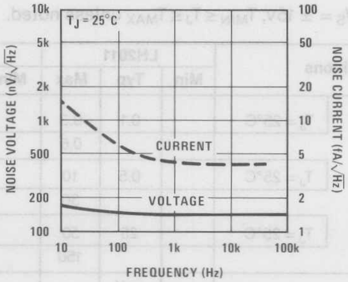




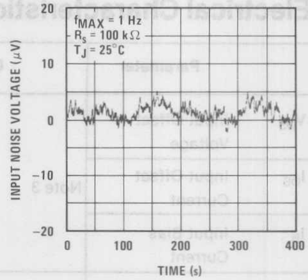
Drift: Single Source Resistor (Unbalanced)



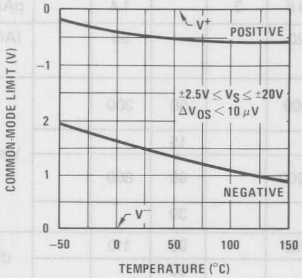
Equivalent Input Noise



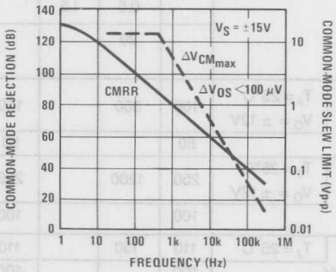
Input Noise



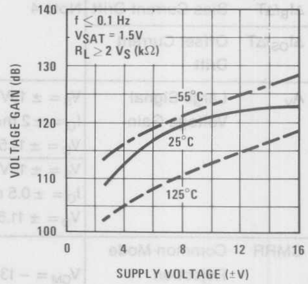
Input Common-Mode Limits



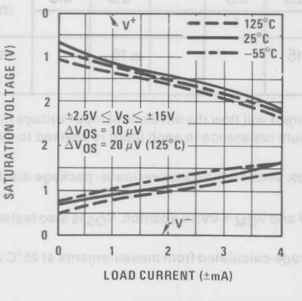
Common-Mode Rejection



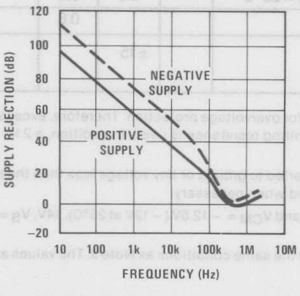
Large Signal Voltage Gain



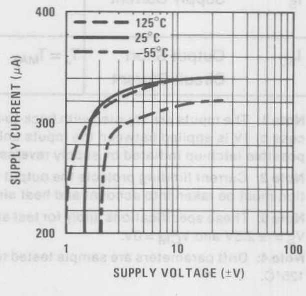
Output Saturation Threshold



Supply Rejection

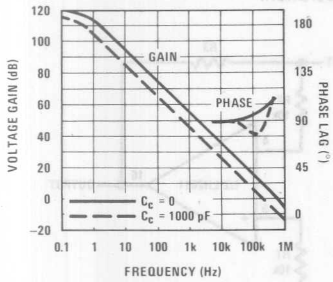


Supply Current (Each Amplifier)

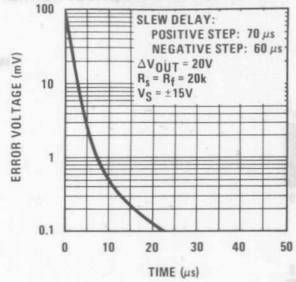


Typical Characteristics (Continued) (for single device)

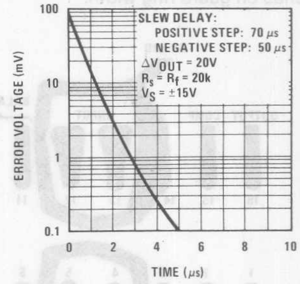
Open Loop Response



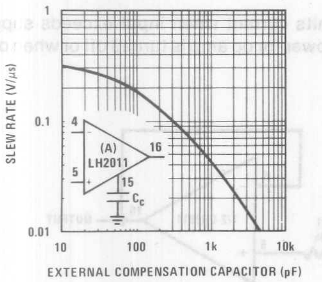
Follower Settling Time



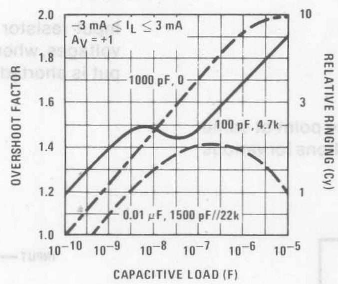
Inverter Settling Time



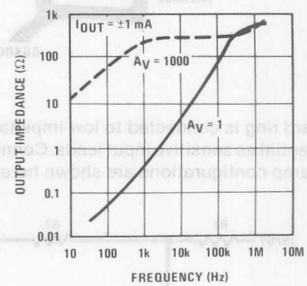
Slew Rate



Stability with Over-Compensation



Closed Loop Output Impedance



Application Hints

When working with circuitry capable of resolving picoampere level signals, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation is a must (Kel-F and Teflon rate high). Proper cleaning of all insulating surfaces to remove fluxes and other residues is also required. This includes the IC package as well as sockets and printed circuit boards. When operating in high humidity environments or near 0°C, some form of surface coating may be necessary to provide a moisture barrier.

The effects of board leakage can be minimized by encircling the input circuitry with a conductive guard ring operated at a potential close to that of the inputs. For critical applications, the floating metal lid is best connected to the guard. This might be accomplished with a dab of conductive paint connecting the metal lid to the "no-connection" pin 14.

Electrostatic shielding of high impedance circuitry is advisable.

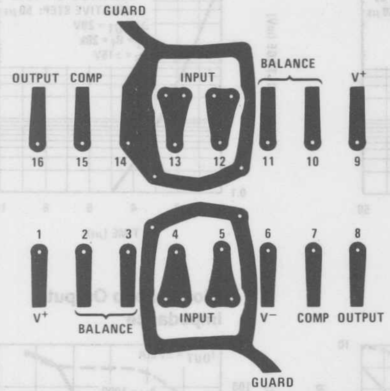
Error voltages can also be generated in the external circuitry. Thermocouples formed between dissimilar metals can cause hundreds of microvolts of error in the presence of temperature gradients. The most troublesome thermocouples are the junction of the IC package and the printed circuit board (35 μV/°C for copper-kovar) and internal resistor connections. Problems can be avoided by keeping low level circuitry away from heat generating elements. Mounting the IC directly to the PC board while keeping package leads short and the input leads close together can also help.

With the LH2011 there is a temptation to remove the bias-current-compensation resistor normally used on the non-inverting input of a summing amplifier. Direct connection of the inputs to ground or a low-impedance voltage source is not recommended with supply voltages greater than about 3V. The potential problem involves the loss of one supply which can cause excessive current in the second supply. Destruction of the IC could result if the current to the input of the device is not limited to less than 100 mA or if there is much more than 1 μF bypass on the supply buss.

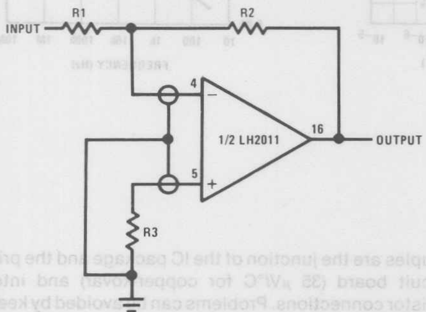
Although these difficulties can be largely avoided by installing clamp diodes across the supply lines on every PC board, a conservative design would include enough resistance in the input lead to limit current to 10 mA if the input lead is pulled to either supply by internal currents. This precaution is by no means limited to the LH2011.

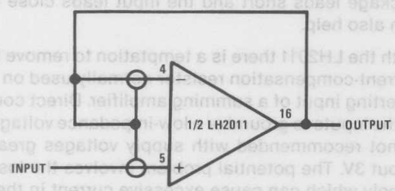
Input Guarding

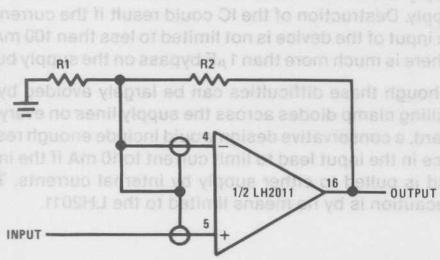
Input guarding can drastically reduce surface leakage. Layout for the LH2011 is shown here. Guarding both sides of board is required. Bulk leakage reduction is less and depends on guard ring width.



Guard ring is connected to low impedance point at same potential as sensitive input leads. Connections for various op amp configurations are shown here.

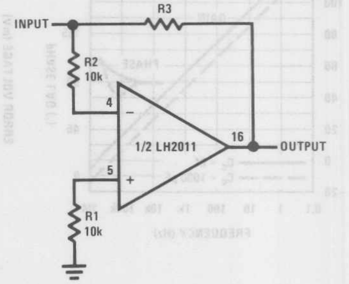




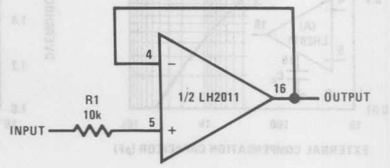


Input Protection

Current is limited by R2 even when input is connected to voltage source outside common-mode range. If one supply reverses, current is limited by R1. These resistors do not affect normal operation.

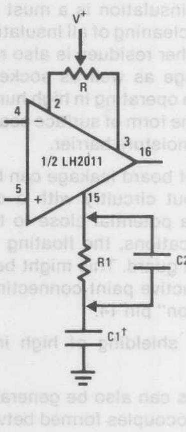


Input resistor limits current when input exceeds supply voltages, when power for op amp is turned off or when output is shorted.



Balancing and Over-Compensation

Over-compensation will improve stability with capacitive loading (see curves). Offset voltage adjustment range is determined by balance potentiometer resistance as indicated in the table.

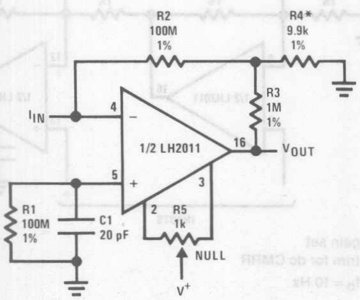


Min Adj Range	R
± 5 mV	100 kΩ
± 2	10k
± 1	3k
± 0.8	3k
± 0.4	1k

†See stability with over-compensation curve

Resistance Multiplication

Equivalent feedback resistance is 10 GΩ, but only standard resistors are used. Even though the offset voltage is multiplied by 100, output offset is actually reduced because error is dependent on offset current rather than bias current. Voltage on summing junction is less than 5 mV.

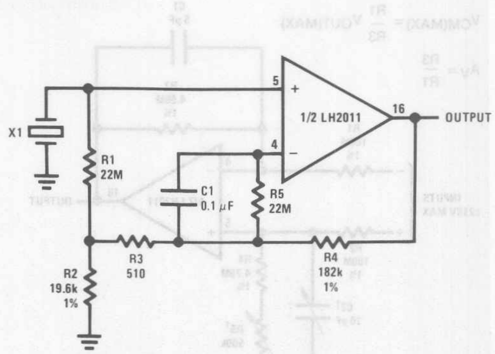


$R_f = R2\left(1 + \frac{R3}{R4}\right)$

R2>> R3 // R4

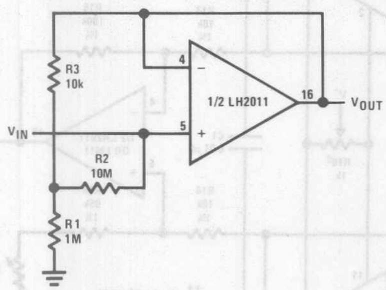
* gain trim

A high-input-impedance ac amplifier for a piezoelectric transducer. Input resistance of 880 MΩ and gain of 10 is obtained.



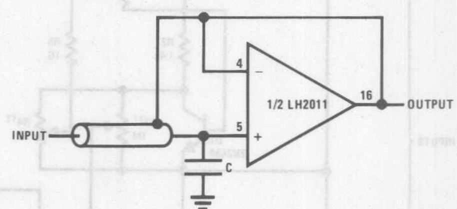
$R_{IN} = R1\left(1 + \frac{R2}{R3}\right) \quad A_V = \frac{R2 + R3 + R4}{R2 + R3}$

Follower input resistance is 1 GΩ. With the input open, offset voltage is multiplied by 100, but the added error is not significant because the op amp offset is low.



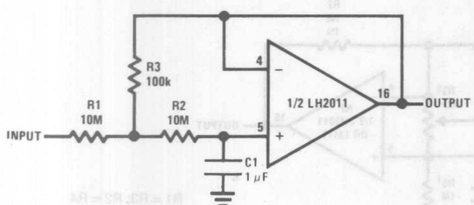
Cable Bootstrapping

Bootstrapping input shield for a follower reduces cable capacitance, leakage, and spurious voltages from cable flexing. Instability can be avoided with small capacitor on input.



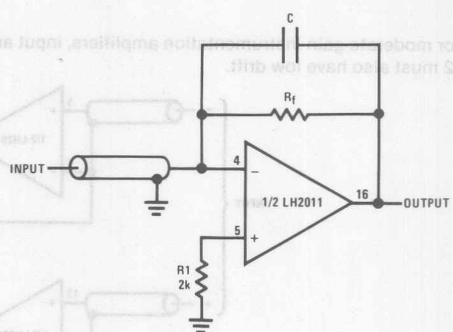
With summing amplifier, summing node is at virtual ground so input shield is best grounded. Small feedback capacitor insures stability.

This circuit multiplies RC time constant to 1000 seconds and provides low output impedance.



$\tau = \frac{R1\,C}{R3}(R2 + R3)$

$\Delta V_{OUT} = \frac{R1 + R3}{R3}(I_B R2 + V_{OS})$

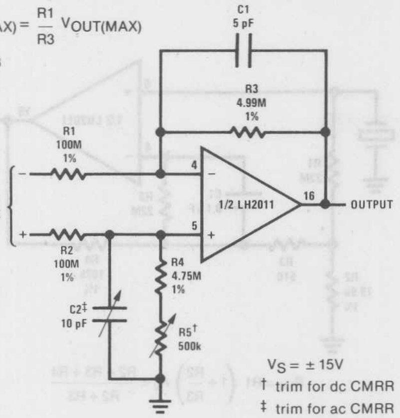


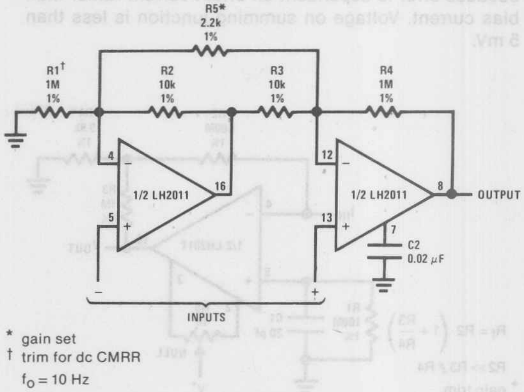
Resistor mismatches and stray capacitors should be balanced out for best common-mode rejection.

common-mode rejection. This can be improved at the expense of differential bandwidth with C2.

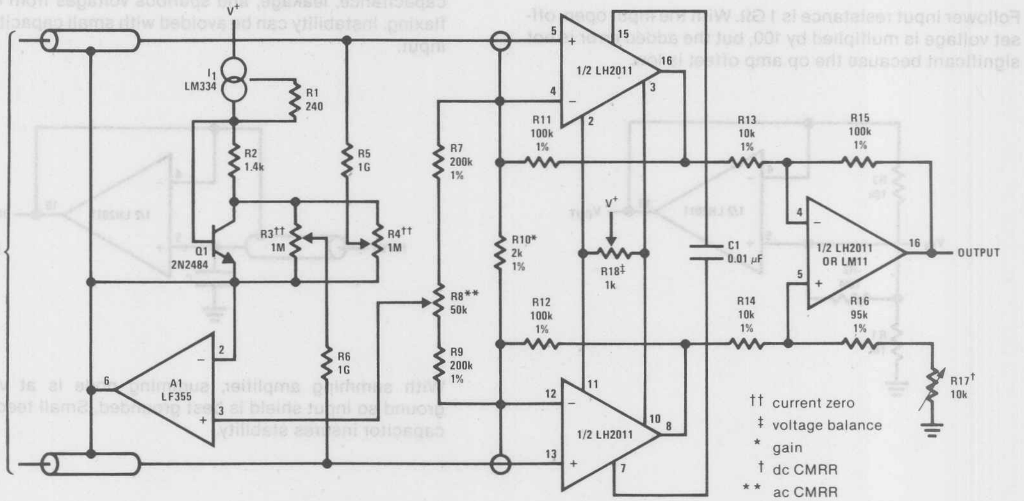
$$V_{CM(MAX)} = \frac{R1}{R3} V_{OUT(MAX)}$$

$$A_V = \frac{R3}{R1}$$

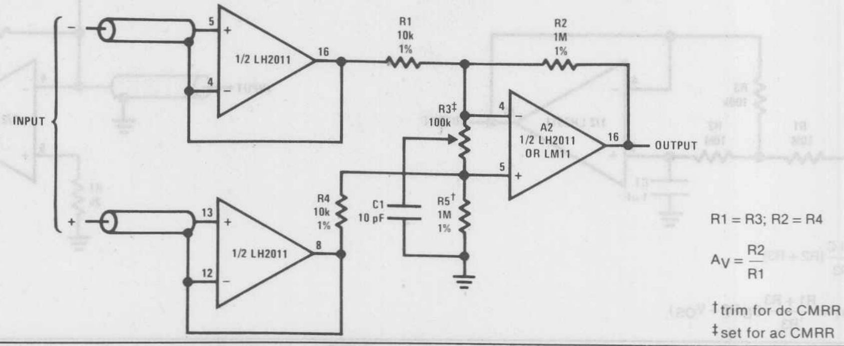




High gain differential instrumentation amplifier includes input guarding, cable bootstrapping and bias current compensation. Differential bandwidth is reduced by C1 which also makes common-mode rejection less dependent on matching of input amplifiers.



For moderate-gain instrumentation amplifiers, input amplifiers can be connected as followers. This simplifies circuitry, but A2 must also have low drift.



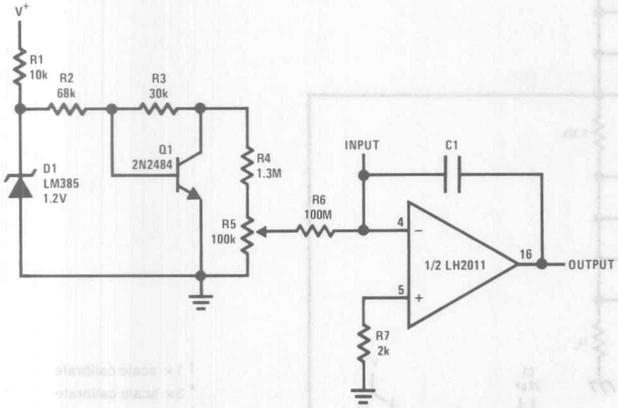
R1 = R3; R2 = R4

$$A_V = \frac{R2}{R1}$$

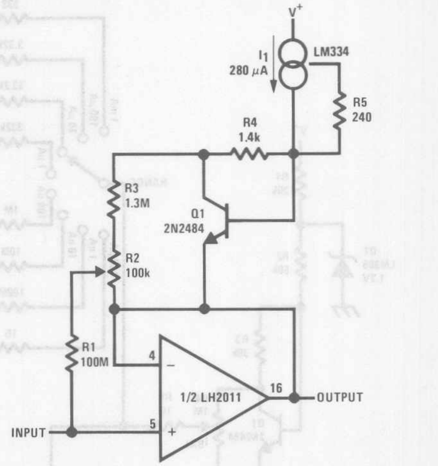
† trim for dc CMRR
‡ set for ac CMRR

Bias Current Compensation

Precise bias current compensation for use with unregulated supplies. Reference voltage is available for other circuitry.

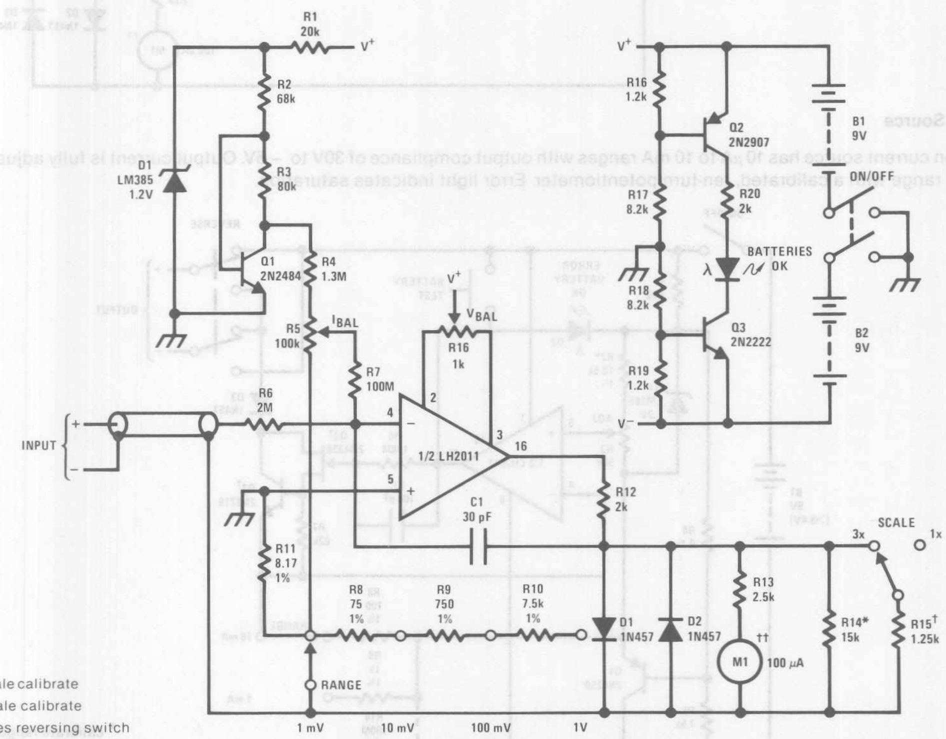


This circuit shows how bias current compensation can be used on a voltage follower.



Voltmeter

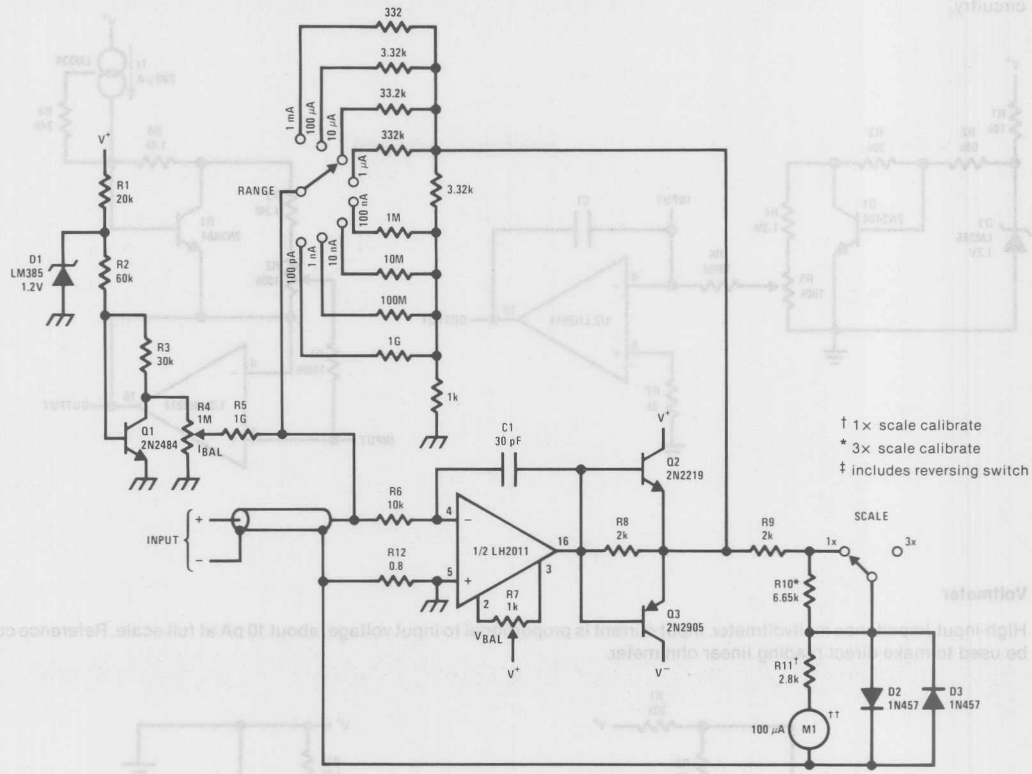
High-input-impedance millivoltmeter. Input current is proportional to input voltage, about 10 pA at full-scale. Reference could be used to make direct reading linear ohmmeter.



* 1× scale calibrate
† 3× scale calibrate
‡ includes reversing switch

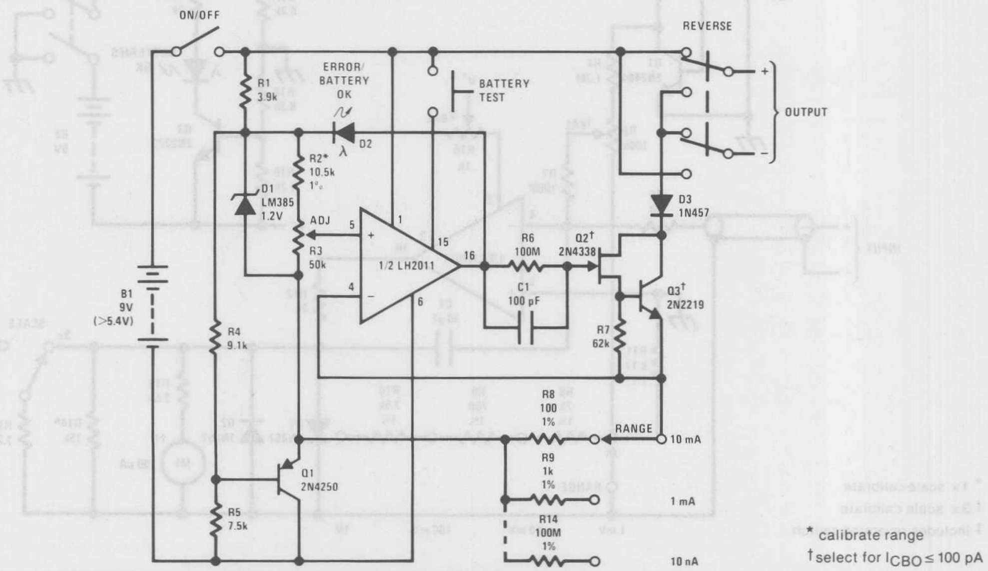
Ammeter

Current meter ranges from 100 pA to 3 mA full-scale. Voltage across input is 100 μV at lower ranges rising to 3 mV at 3 mA. Buffers on op amp are to remove ambiguity with high-current overload. Output can also drive DVM or DPM.



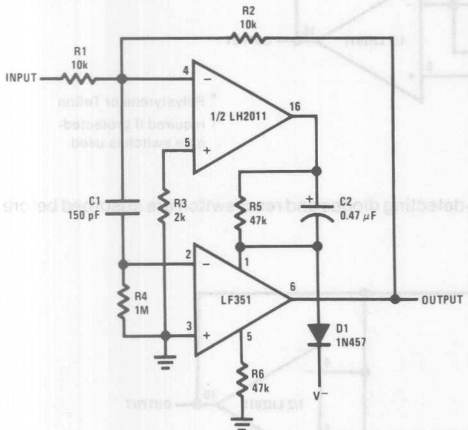
Current Source

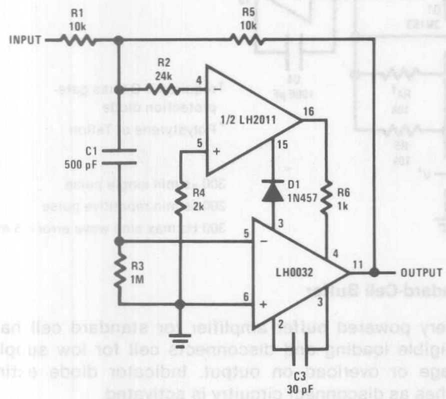
Precision current source has 10 μA to 10 mA ranges with output compliance of 30V to -5V. Output current is fully adjustable on each range with a calibrated, ten-turn potentiometer. Error light indicates saturation.



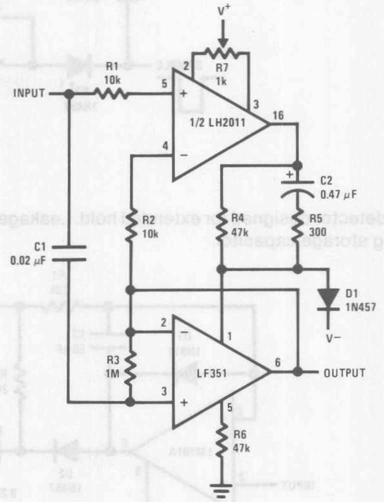
Fast Amplifiers

These inverters have bias current and offset voltage of LH2011 along with speed of the FET op amps. Open loop gain is about 140 dB and settling time to 1 mV about 8 μs. Overload-recovery delay can be eliminated by direct coupling the FET amplifier to summing node.

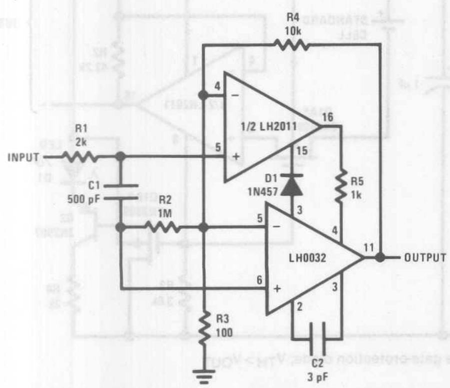




Follower has 10 μs settling to 1 mV, but signal repetition frequency should not exceed 10 kHz if the FET amplifier is ac coupled to input. The circuit does not behave well if common-mode range is exceeded.

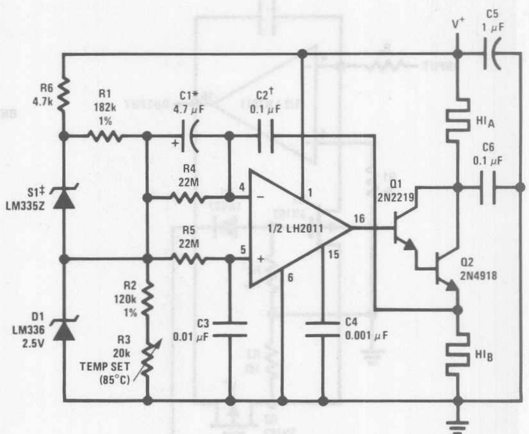


This 100× amplifier has small and large signal bandwidth of 1 MHz. The LH2011 greatly reduces offset voltage, bias current and gain error. Eliminating long recovery delay for greater than 100% overload requires direct coupling of A2 to input.

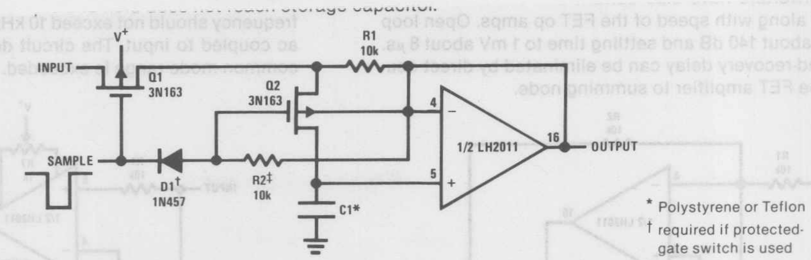


Heater Control

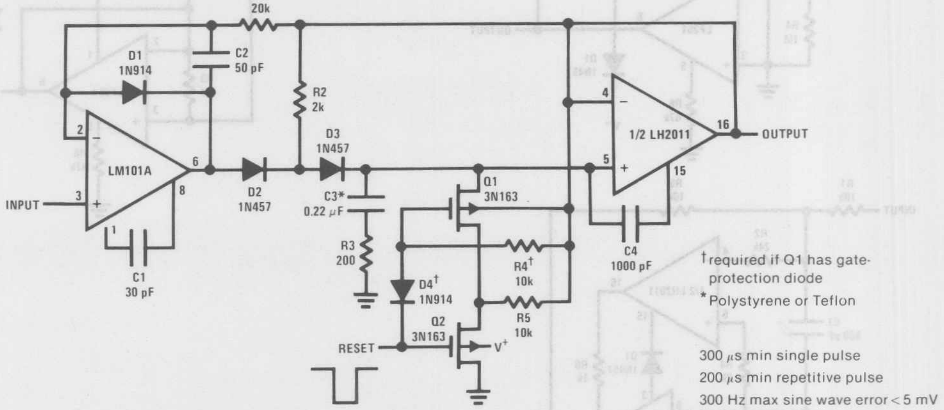
Proportional control crystal oven heater uses lead/lag compensation for fast settling. Time constant is changed with R4 and compensating resistor R5. If Q2 is inside oven, a regulated supply is recommended for 0.1°C control.



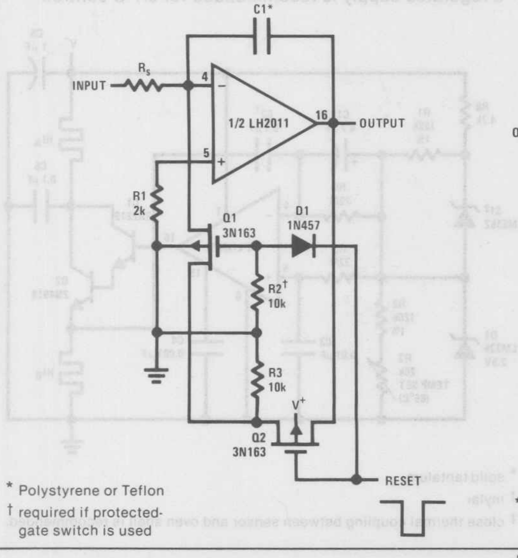
* solid tantalum
† mylar
‡ close thermal coupling between sensor and oven shell is recommended.



A peak detector designed for extended hold. Leakage currents of peak-detecting diodes and reset switch are absorbed before reaching storage capacitor.

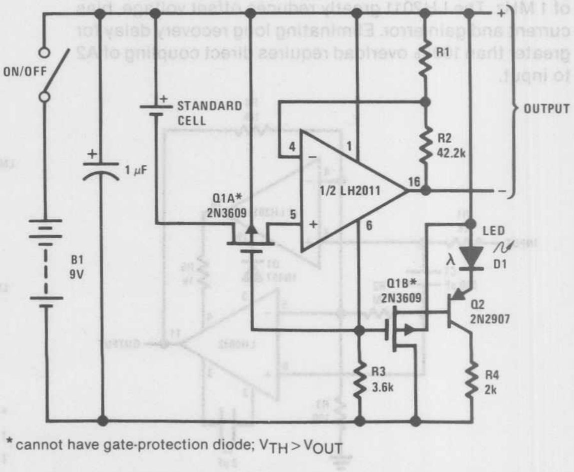


Reset is provided for this integrator and switch leakage is isolated from the summing junction. Greater precision can be provided if bias-current compensation is included.



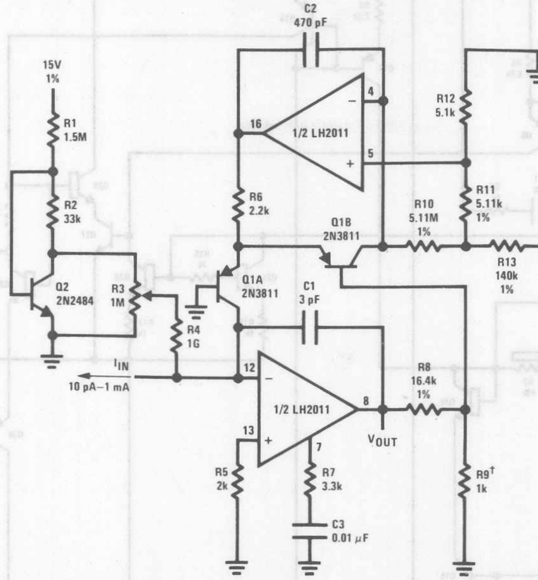
Standard-Cell Buffer

Battery powered buffer amplifier for standard cell has negligible loading and disconnects cell for low supply voltage or overload on output. Indicator diode extinguishes as disconnect circuitry is activated.



Logarithmic Amplifiers

Unusual frequency compensation gives this logarithmic converter a 100 μs time constant from 1 mA down to 100 μA, increasing from 200 μs to 200 ms from 10 nA to 10 pA. Optional bias current compensation can give 10 pA resolution from −55°C to 100°C. Scale factor is 1V/decade and temperature compensated.



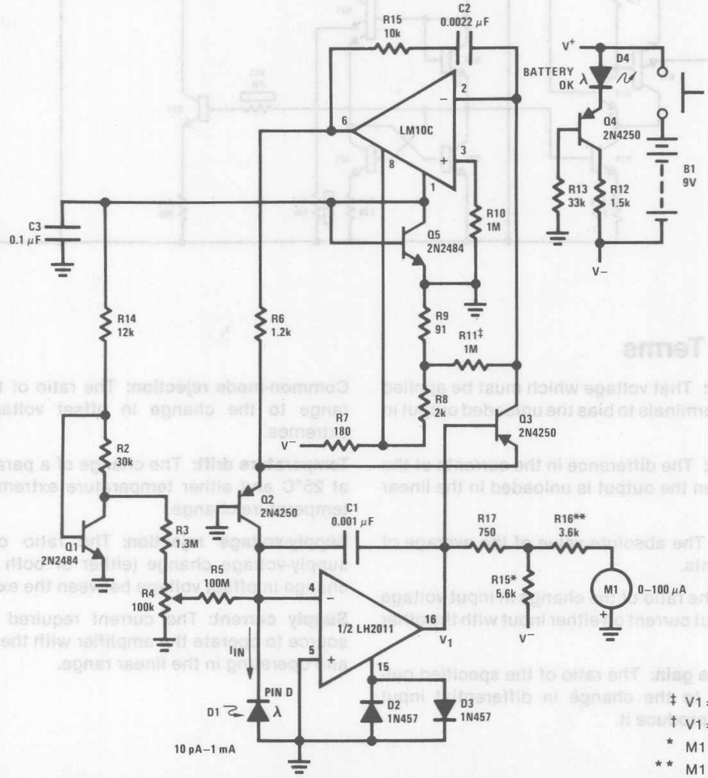
a. Set R11 for $V_{OUT} = 0$ at $I_{IN} = 100\ \mu A$

b. Set R8 for $V_{OUT} = 3V$ at $I_{IN} = 100\ \mu A$

c. Set R3 for $V_{OUT} = -4V$ at $I_{IN} = 10$ pA

† 3300 ppm/°C. Type Q209 available from Tel Labs, Inc., Manchester, N.H.

Light meter has eight-decade range. Bias current compensation can give input current resolution of better than ±2 pA over 15°C to 55°C.



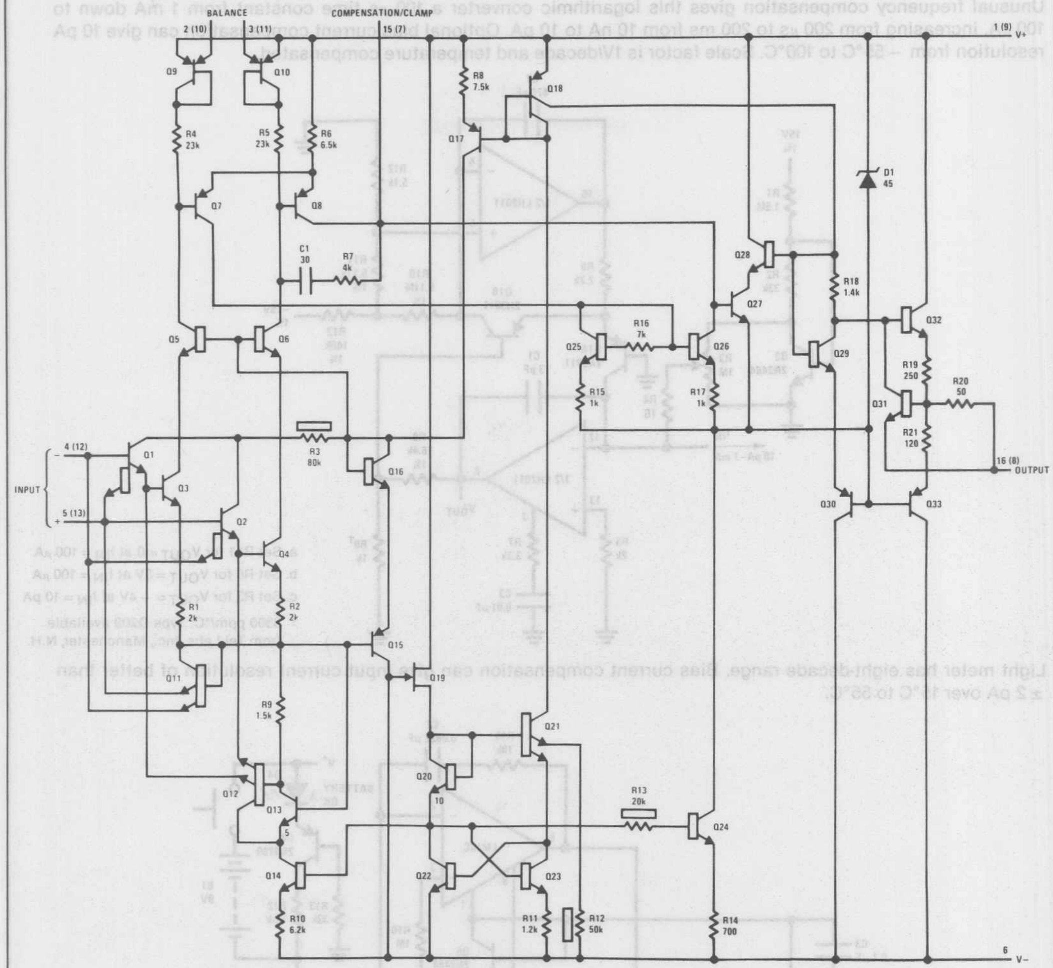
‡ $V1 = 0$ @ $I_{IN} = 100$ nA

$V1 = -0.24V$ @ $I_{IN} = 10$ pA

* $M1 = 0$ @ $I_{IN} = 10$ pA

** $M1 = f_S$ @ $I_{IN} = 1$ mA

Schematic Diagram (for single device)



Definition of Terms

Input offset voltage: That voltage which must be applied between the input terminals to bias the unloaded output in the linear region.

Input offset current: The difference in the currents at the input terminals when the output is unloaded in the linear region.

Input bias current: The absolute value of the average of the two input currents.

Input resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Large signal voltage gain: The ratio of the specified output voltage swing to the change in differential input voltage required to produce it.

Common-mode rejection: The ratio of the input voltage range to the change in offset voltage between the extremes.

Temperature drift: The change of a parameter measured at 25°C and either temperature extreme divided by the temperature change.

Supply-voltage rejection: The ratio of the specified supply-voltage change (either or both supplies) to the change in offset voltage between the extremes.

Supply current: The current required from the power source to operate the amplifier with the output unloaded and operating in the linear range.

National Semiconductor

Operational Amplifiers/Buffers

LH2101A/LH2201A/LH2301A Dual High Performance Op Amp

General Description

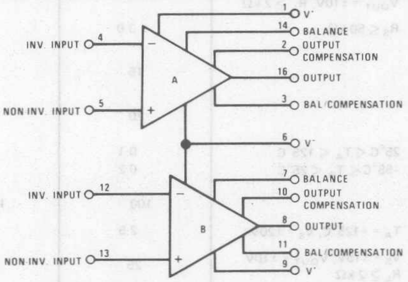
The LH2101A series of dual operational amplifiers are two LM101A type op amps in a single hermetic package. Featuring all the same performance characteristics of the single, these duals offer in addition closer thermal tracking, lower weight, reduced insertion cost, and smaller size than two singles. For additional information, see the LM101A data sheet and National's Linear Application Handbook.

The LH2101A is specified for operation over the −55°C to +125°C military temperature range. The LH2201A is specified for operation over the −25°C to +85°C temperature range. The LH2301A is specified for operation over the 0°C to +70°C temperature range.

Features

- Low offset voltage
- Low offset current
- Guaranteed drift characteristics
- Offsets guaranteed over entire common mode and supply voltage ranges
- Slew rate of 10V/μs as a summing amplifier

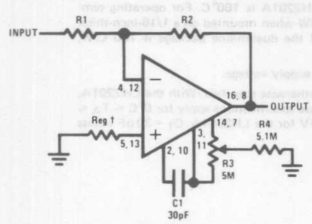
Connection Diagram



Order Number LH2101AD or LH2201AD or LH2301AD, see Package D16C
LH2101AF, LH2201AF, LH2301AF, see Package F16B
LH2101AJ, LH2201AJ, LH2301AJ, see Package J16A

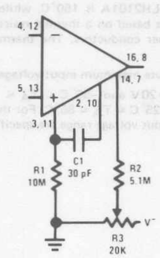
Auxiliary Circuits

Inverting Amplifier with Balancing Circuit

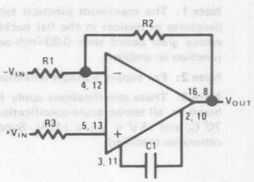


†May be zero or equal to parallel combination of R1 and R2 for minimum offset

Alternate Balancing Circuit



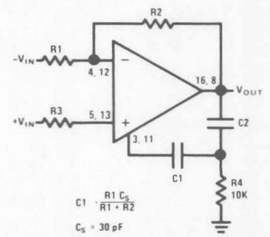
Single Pole Compensation



$C1 = \frac{R1\ C_S}{R1 + R2}$

$C_S = 30\ pF$

Two Pole Compensation

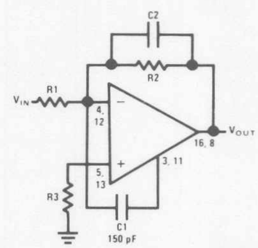


$C1 = \frac{R1\ C_S}{R1 + R2}$

$C_S = 30\ pF$

$C2 = 10\ C1$

Feedforward Compensation



$C2 = \frac{1}{2\pi f_o R2}$

$f_o = 3\ MHz$

Absolute Maximum Ratings

Supply Voltage	±22V	Operating Temperature Range	LH2101A	−55°C to 125°C
Power Dissipation (Note 1)	500 mW		LH2201A	−25°C to 85°C
Differential Input Voltage	±30V		LH2301A	0°C to 70°C
Input Voltage (Note 2)	±15V	Storage Temperature Range		−65°C to 150°C
Output Short-Circuit Duration	Continuous	Lead Temperature (Soldering, 10 sec)		300°C

Electrical Characteristics Each Side (Note 3)

PARAMETER	CONDITIONS	LIMITS LH2101A	LH2201A	LH2301A	UNITS
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 50\ k\Omega$	2.0	2.0	7.5	mV Max
Input Offset Current	$T_A = 25°C$	10	10	50	nA Max
Input Bias Current	$T_A = 25°C$	75	75	250	nA Max
Input Resistance	$T_A = 25°C$	1.5	1.5	0.5	MΩ Min
Supply Current	$T_A = 25°C$, $V_S = \pm 20V$	3.0	3.3	3.0	mA Max
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2\ k\Omega$	50	50	25	V/mV Min
Input Offset Voltage	$R_S \leq 50\ k\Omega$	3.0	3.0	10	mV Max
Average Temperature Coefficient of Input Offset Voltage		15	15	30	μV/°C Max
Input Offset Current		20	20	70	nA Max
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq 125°C$ $-55°C \leq T_A \leq 25°C$	0.1 0.2	0.1 0.2	0.3 0.6	nA/°C Max nA/°C Max
Input Bias Current		100	100	300	nA Max
Supply Current	$T_A = +125°C$, $V_S = \pm 20V$	2.5	2.5		mA Max
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2\ k\Omega$	25	25	15	V/mV Min
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$ $R_L = 2\ k\Omega$	±12 ±10	±12 ±10	±12 ±10	V Min V Min
Input Voltage Range	$V_S = \pm 20V$	±15	±15	±12	V Min
Common Mode Rejection Ratio	$R_S \leq 50\ k\Omega$	80	80	70	dB Min
Supply Voltage Rejection Ratio	$R_S \leq 50\ k\Omega$	80	80	70	dB Min

Note 1: The maximum junction temperature of the LH2101A is 150°C, while that of the LH2201A is 100°C. For operating temperatures of devices in the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: For supply voltages lens than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: These specifications apply for $\pm 5V \leq V_S \leq \pm 20V$ and $-55°C \leq T_A \leq 125°C$, unless otherwise specified. With the LH2201A, however, all temperature specifications are limited to $-25°C \leq T_A \leq 85°C$. For the LH2301A these specifications apply for $0°C \leq T_A \leq 70°C$, and $\pm 5V \leq V_S \leq \pm 15V$. Supply current and input voltage range are specified as $V_S = \pm 15V$ for the LH2301A. $C_1 = 30\ pF$ unless otherwise specified.

National Semiconductor

Operational Amplifiers/Buffers

LH2108/LH2208/LH2308, LH2108A/LH2208A/LH2308A Dual Super Beta Op Amp

General Description

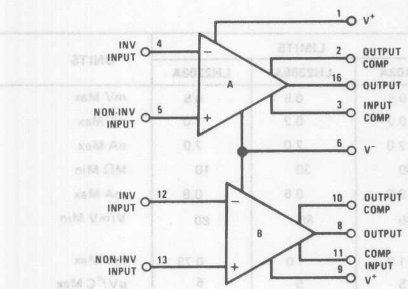
The LH2108A/LH2208A/LH2308A and LH2108/LH2208/LH2308 series of dual operational amplifiers are two LM108A or LM108 type op amps in a single hermetic package. Featuring all the same performance characteristics of the single device, these duals also offer closer thermal tracking, lower weight, reduced insertion cost, and smaller size than two single devices. For additional information see the LM108A or LM108 data sheet and National's Linear Application Handbook.

The LH2108A/LH2108 is specified for operation over the −55°C to +125°C military temperature range. The LH2208A/LH2208 is specified for operation over the −25°C to +85°C temperature range. The LH2308A/LH2308 is specified for operation over the 0°C to +70°C temperature range.

Features

- Low offset current — 50 pA
- Low offset voltage — 0.7 mV
- Low offset voltage — LH2108A 0.3 mV; LH2108 0.7 mV
- Wide input voltage range — ±15V
- Wide operating supply range — ±3V to ±20V

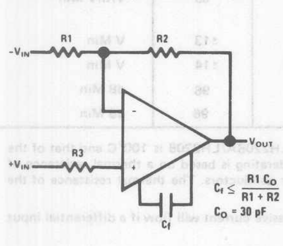
Connection Diagram



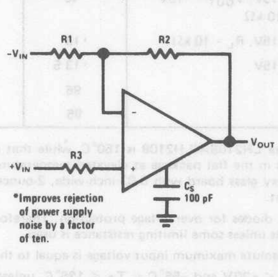
Order Number LH2108AD, LH2208AD, LH2308AD, LH2108D, LH2208D, or LH2308D
See Package D16C
Order Number LH2108AF, LH2208AF, LH2308AF, LH2108F, LH2208F, or LH2308F
See Package F16B
Order Number LH2108AJ, LH2208AJ, LH2308AJ, LH2108J, LH2208J, or LH2308J
See Package J16A

Auxiliary Circuits

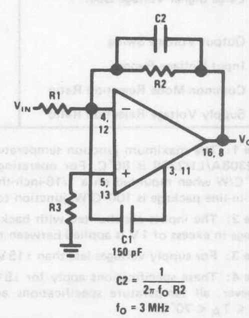
Standard Compensation Circuit



Alternate * Frequency Compensation



Feedforward Compensation



	±15V	LH2308A/LH2308	0°C to +70°C
Output Short Circuit Duration	Continuous	Storage Temperature Range	−65°C to +150°C
		Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics each side (Note 4)

PARAMETER	CONDITIONS	LIMITS			UNITS
		LH2108	LH2208	LH2308	
Input Offset Voltage	$T_A = 25°C$	2.0	2.0	7.5	mV Max
Input Offset Current	$T_A = 25°C$	0.2	0.2	1.0	nA Max
Input Bias Current	$T_A = 25°C$	2.0	2.0	7.0	nA Max
Input Resistance	$T_A = 25°C$	30	30	10	MΩ Min
Supply Current	$T_A = 25°C$	0.6	0.6	0.8	mA Max
Large Signal Voltage Gain	$T_A = 25°C$ $V_S = \pm15V$ $V_{OUT} = \pm10V$, $R_L > 10\ k\Omega$	50	50	25	V/mV Min
Input Offset Voltage		3.0	3.0	10	mV Max
Average Temperature Coefficient of Input Offset Voltage		15	15	30	μV/°C Max
Input Offset Current		0.4	0.4	1.5	nA Max
Average Temperature Coefficient of Input Offset Current		2.5	2.5	10	pA/°C Max
Input Bias Current		3.0	3.0	10	nA Max
Supply Current	$T_A = +125°C$	0.4	0.4		mA Max
Large Signal Voltage Gain	$V_S = \pm15V$, $V_{OUT} = \pm10V$ $R_L > 10\ k\Omega$	25	25	15	V/mV Min
Output Voltage Swing	$V_S = \pm15V$, $R_L = 10\ k\Omega$	±13	±13	±13	V Min
Input Voltage Range	$V_S = \pm15V$	±13.5	±13.5	±14	V Min
Common Mode Rejection Ratio		85	85	80	dB Min
Supply Voltage Rejection Ratio		80	80	80	dB Min

Electrical Characteristics each side (Note 4)

PARAMETER	CONDITIONS	LIMITS			UNITS
		LH2108A	LH2208A	LH2308A	
Input Offset Voltage	$T_A = 25°C$	0.5	0.5	0.5	mV Max
Input Offset Current	$T_A = 25°C$	0.2	0.2	1.0	nA Max
Input Bias Current	$T_A = 25°C$	2.0	2.0	7.0	nA Max
Input Resistance	$T_A = 25°C$	30	30	10	MΩ Min
Supply Current	$T_A = 25°C$	0.6	0.6	0.8	mA Max
Large Signal Voltage Gain	$T_A = 25°C$ $V_S = \pm15V$ $V_{OUT} = \pm10V$, $R_L > 10\ k\Omega$	80	80	80	V/mV Min
Input Offset Voltage		1.0	1.0	0.73	mV Max
Average Temperature Coefficient of Input Offset Voltage		5	5	5	μV/°C Max
Input Offset Current		0.4	0.4	1.5	nA Max
Average Temperature Coefficient of Input Offset Current		2.5	2.5	10	pA/°C Max
Input Bias Current		3.0	3.0	10	nA Max
Supply Current	$T_A = +125°C$	0.4	0.4	–	mA Max
Large Signal Voltage Gain	$V_S = \pm15V$, $V_{OUT} = \pm10V$ $R_L > 10\ k\Omega$	40	40	60	V/mV Min
Output Voltage Swing	$V_S = \pm15V$, $R_L = 10\ k\Omega$	±13	±13	±13	V Min
Input Voltage Range	$V_S = \pm15V$	±13.5	±13.5	±14	V Min
Common Mode Rejection Ratio		96	96	96	dB Min
Supply Voltage Rejection Ratio		96	96	96	dB Min

Note 1: The maximum junction temperature of the LH2108A/LH2108 is 150°C, while that of the LH2208A/LH2208 is 100°C and that of the LH2308A/LH2308 is 85°C. For operating devices in the flat package at elevated temperatures, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: These specifications apply for $\pm5V \leq V_S \leq \pm20V$ and $-55°C \leq T_A \leq 125°C$, unless otherwise specified. With the LH2208A/LH2208, however, all temperature specifications are limited to $-25°C \leq T_A \leq 85°C$ and with the LH2308A/LH2308 for $\pm5V \leq V_S \leq 15V$ and $0°C \leq T_A \leq 70°C$.

National Semiconductor

Operational Amplifiers/Buffers

LH2110/LH2210/LH2310 Dual Voltage Follower

General Description

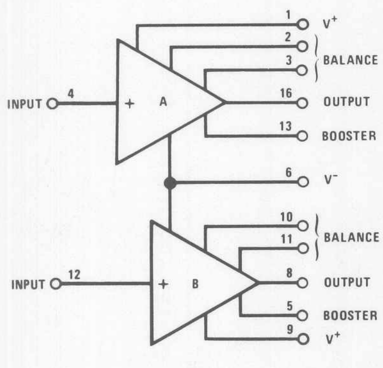
The LH2110 series of dual voltage followers are two LM110 type followers in a single hermetic package. Featuring all the same performance characteristics of the single, these duals offer in addition closer thermal tracking, lower weight, reduced insertion cost and smaller size than two singles. For additional information, see the LM110 data sheet and National's Linear Application Notebook.

The LH2110 is specified for operation over the −55°C to +125°C military temperature range. The LH2210 is specified for operation over the −25°C to +85°C temperature range. The LH2310 is specified for operation over the 0°C to +70°C temperature range.

Features

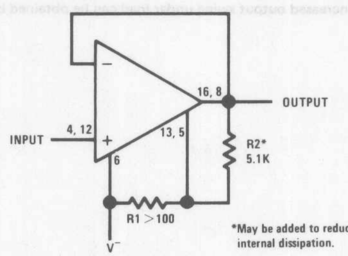
- Low input current 1 nA
- High input resistance 10^{10} ohms
- High slew rate 30V/µs
- Wide bandwidth 20 MHz
- Wide operating supply range ±5V to ±18V
- Output short circuit proof

Connection Diagram

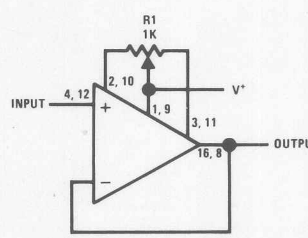


Order Number LH2110D, LH2210D or LH2310D, See Package D16C
Order Number LH2110F, LH2210F or LH2310F, See Package F16B
Order Number LH2110J, LH2210J or LH2310J, See Package J16A

Auxiliary Circuits



Increasing Negative Swing Under Load



Offset Balancing Circuit

Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation (Note 1)	500 mW
Input Voltage (Note 2)	±15V
Output Short Circuit Duration (Note 3)	Continuous
Operating Temperature Range LH2110	−55°C to 125°C
LH2210	−25°C to 85°C
LH2310	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics Each Side (Note 4)

PARAMETER	CONDITIONS	LIMITS			UNITS
		LH2110	LH2210	LH2310	
Input Offset Voltage	$T_A = 25°C$	4.0	4.0	7.5	mV Max
Input Bias Current	$T_A = 25°C$	3.0	3.0	7.0	nA Max
Input Resistance	$T_A = 25°C$	10^{10}	10^{10}	10^{10}	Ω Min
Input Capacitance		1.5	1.5	1.5	pF Typ
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm15V$ $V_{OUT} = \pm10V$, $R_L = 8\ k\Omega$	.999	.999	.999	V/V Min
Output Resistance	$T_A = 25°C$	2.5	2.5	2.5	Ω Max
Supply Current (Each Amplifier)	$T_A = 25°C$	5.5	5.5	5.5	mA Max
Input Offset Voltage		6.0	6.0	10	mV Max
Offset Voltage	$-55°C \leq T_A \leq 85°C$	6	6	10	µV/°C Typ
Temperature Drift	$T_A = 125°C$	12	12		µV/°C Typ
Input Bias Current		10	10	10	nA Max
Large Signal Voltage Gain	$V_S = \pm15V$, $V_{OUT} = \pm10V$ $R_L = 10\ k\Omega$	.999	.999	.999	V/V Min
Output Voltage Swing (Note 5)	$V_S = \pm15V$, $R_L = 10\ k\Omega$	±10	±10	±10	V Min
Supply Current (Each Amplifier)	$T_A = 125°C$	4.0	4.0	–	mA Max
Supply Voltage Rejection Ratio	$\pm5V \leq V_S \leq \pm18V$	70	70	70	dB Min

Note 1: The maximum junction temperature of the LH2110 is 150°C, while that of the LH2210 is 100°C and that of the LH2310 is 85°C. For operating devices in the flat package at elevated temperatures, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: Continuous short circuit is allowed for case temperatures to 125°C and ambient temperatures to 70°C. It is necessary to insert a resistor greater than 2 kΩ in series with the input when the amplifier is driven from low impedance sources to prevent damage when the output is shorted.

Note 4: These specifications apply for $\pm5V \leq V_S \leq \pm18V$ and $-55°C \leq T_A \leq 125°C$, unless otherwise specified. With the LM210, however, all temperature specifications are limited to $-25°C \leq T_A \leq 85°C$, and for the LH2310, all temperature specifications are limited to $0°C \leq T_A \leq 70°C$.

Note 5: Increased output swing under load can be obtained by connecting an external resistor between the booster and V^- terminals.

National Semiconductor

Operational Amplifiers/Buffers

LH24250/LH24250C Dual Programmable Micropower Op Amp

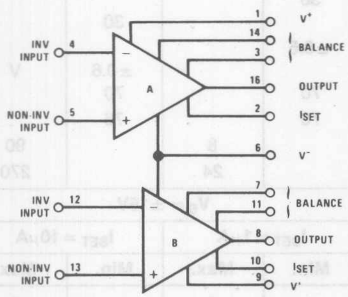
General Description

The LH24250/LH24250C series of dual programmable micropower operational amplifiers are two LM4250 type op amps in a single hermetic package. Featuring all the same performance characteristics of the LM4250, the LH24250/LH24250C duals also offer closer thermal tracking, lower weight, reduced insertion cost and smaller size than two single devices. For additional information, see the LM4250 data sheet and National's Linear Application Handbook.

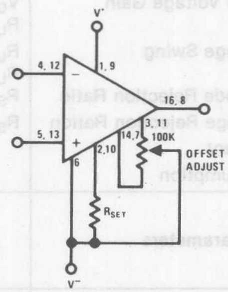
Features

- ±1V to ±18V power supply operation
- Standby power consumption as low as 20 μW
- Offset current programmable from less than 0.5 nA to 30 nA
- Programmable slew rate
- May be shut-down using standard open collector TTL
- Internally compensated and short circuit proof

Connection Diagram and Auxiliary Circuit



Offset Null Circuit



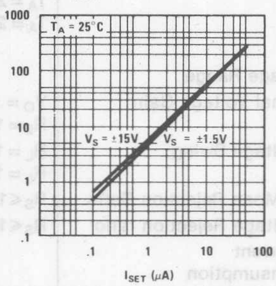
Ordering Information
Order Number LH24250D or LH24250CD, See Package D16C
LH24250F or LH24250CF, See Package F16B
LH24250J or LH24250CJ, See Package J16A

Typical Quiescent Current Setting Resistor

Set Current Setting Resistor to V−

	I_{SET}				
V_S	0.1 μA	0.5 μA	1.0 μA	5 μA	10 μA
±1.5V	25.6 MΩ	5.04 MΩ	2.5 MΩ	492 kΩ	244 kΩ
±3.0V	55.6 MΩ	11.0 MΩ	5.5 MΩ	1.09 MΩ	544 kΩ
±6.0V	116 MΩ	23.0 MΩ	11.5 MΩ	2.29 MΩ	1.14 MΩ
±9.0V	176 MΩ	35.0 MΩ	17.5 MΩ	3.49 MΩ	1.74 MΩ
±12.0V	236 MΩ	47.0 MΩ	23.5 MΩ	4.69 MΩ	2.34 MΩ
±15.0V	296 MΩ	59.0 MΩ	29.5 MΩ	5.89 MΩ	2.94 MΩ

Quiescent Current (I_Q) vs I_{SET}



Differential Input Voltage	±15V	Operating Temperature Range LH24250	−55°C to 125°C
Input Voltage (Note 2)	±15V	LH24250C	0°C to 70°C
I_{SET} Current	150µA	Storage Temperature Range	−65°C to 150°C
		Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics LH24250, each amplifier (−55°C ≤ T_A ≤ 125°C unless otherwise specified)

Parameters	Conditions	$V_S = \pm 1.5V$				Units
		$I_{SET} = 1\mu A$		$I_{SET} = 10\mu A$		
		Min.	Max.	Min.	Max.	
V_{OS}	$T_A = 25°C$, $R_S \leq 100k\Omega$		3		5	mV
I_{OS}	$T_A = 25°C$		3		10	nA
I_{bias}	$T_A = 25°C$		7.5		50	nA
Large Signal Voltage Gain	$T_A = 25°C$, $R_L = 100k\Omega$	40				k
	$V_O = \pm 0.6V$, $R_L = 10k\Omega$			50		k
Supply Current	$T_A = 25°C$		7.5		80	µA
Power Consumption	$T_A = 25°C$		23		240	µW
V_{OS}	$R_S \leq 10k\Omega$		4		6	mV
I_{OS}	$T_A = 25°C$		5		10	nA
	$T_A = 25°C$		3		10	nA
I_{bias}			7.5		50	nA
Input Voltage Range		±0.7		±0.7		V
Large Signal Voltage Gain	$V_O = \pm 0.6V$, $R_L = 100k\Omega$	30				k
	$R_L = 10k\Omega$			30		k
Output Voltage Swing	$R_L = 100k\Omega$	±0.6				V
	$R_L = 10k\Omega$			±0.6	V	
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70		70		dB
Supply Voltage Rejection Ration	$R_S \leq 10k\Omega$	76		76		dB
Supply Current			8		90	µA
Power Consumption			24		270	µW

Parameters	Conditions	$V_S = \pm 15V$				Units
		$I_{SET} = 1\mu A$		$I_{SET} = 10\mu A$		
		Min.	Max.	Min.	Max.	
V_{OS}	$T_A = 25°C$, $R_S \leq 10k\Omega$		3		5	mV
I_{OS}	$T_A = 25°C$		3		10	na
I_{bias}	$T_A = 25°C$		7.5		50	nA
Large Signal Voltage Gain	$T_A = 25°C$, $R_L = 100k\Omega$	100				k
	$V_O = \pm 10V$, $R_L = 10k\Omega$			100		k
Supply Current	$T_A = 25°C$		10		90	µA
Power Consumption	$T_A = 25°C$		300		2.7	µW/mW
V_{OS}	$R_S \leq 10k\Omega$		4		6	mV
I_{OS}	$T_A = 25°C$		25		25	nA
	$T_A = 25°C$		3		10	nA
I_{bias}			7.5		50	nA
Input Voltage Range		±13.5		±13.5		V
Large Signal Voltage Gain	$V_O = \pm 15V$, $R_L = 100\Omega$	50				k
	$R_L = 10k\Omega$			50		k
Output Voltage Swing	$R_L = 100k\Omega$	±12				V
	$R_L = 10k\Omega$			±12		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70		70		dB
Supply Voltage Rejection ratio	$R_S \leq 10k\Omega$	76		76		dB
Supply Current		11		100		µA
Power Consumption			330		3	µW/mW

Note 1: The maximum junction temperature of the LH24250 is 150°C, while that of the LH24250C is 100°C. The thermal resistance of the dual-in-line package is 100°C/W junction to ambient. For the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16 inch thick epoxy glass board with ten, 0.03 inch wide, 2 ounce copper conductors.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

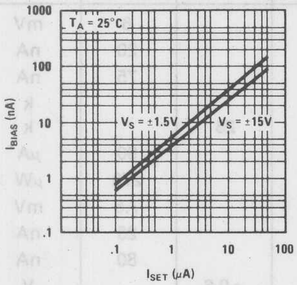
Electrical Characteristics LH24250C, each amplifier ($0°C \leq T_A \leq 70°C$ unless otherwise specified)

Parameters	Conditions	$V_S = \pm 1.5V$				Units
		$I_{SET} = 1\,\mu A$		$I_{SET} = 10\,\mu A$		
		Min.	Max.	Min.	Max.	
V_{OS}	$T_A = 25°C$, $R_S \leq 100\,k\Omega$		5		6	mV
I_{OS}	$T_A = 25°C$		6		20	nA
I_{bias}	$T_A = 25°C$		10		75	nA
Large Signal Voltage Gain	$T_A = 25°C$, $R_L = 100\,k\Omega$	25				k
	$V_O = \pm 0.6V$, $R_L = 10\,k\Omega$			25		k
Supply Current	$T_A = 25°C$		8		90	µA
Power Consumption	$T_A = 25°C$		24		270	µW
V_{OS}	$R_S \leq 10\,k\Omega$		6.5		7.5	mV
I_{OS}			8		25	nA
I_{bias}			10		80	nA
Input Voltage Range		±0.6		±0.6		V
Large Signal Voltage Gain	$V_O = \pm 0.6V$, $R_L = 100\,k\Omega$	25				k
	$R_L = 10\,k\Omega$			25		k
Output Voltage Swing	$R_L = 100\,k\Omega$	±0.6				V
	$R_L = 10\,k\Omega$			±0.6	V	
Common Mode Rejection Ratio	$R_S \leq 10\,k\Omega$	70		70	dB	
Supply Voltage Rejection Ratio	$R_S \leq 10\,k\Omega$	74		74	dB	
Supply Current			8		90	µA
Power Consumption			24		270	µW

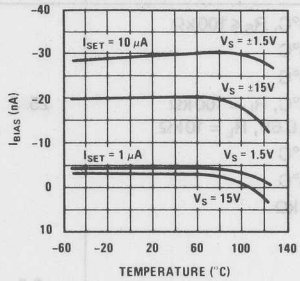
Parameters	Conditions	$V_S = \pm 15V$				Units
		$I_{SET} = 1\,\mu A$		$I_{SET} = 10\,\mu A$		
		Min.	Max.	Min.	Max.	
V_{OS}	$T_A = 25°C$, $R_S \leq 10\,k\Omega$		5		6	mV
I_{OS}	$T_A = 25°C$		6		20	na
I_{bias}	$T_A = 25°C$		10		75	nA
Large Signal Voltage Gain	$T_A = 25°C$, $R_L = 100\,k\Omega$	60				k
	$V_O = \pm 10V$, $R_L = 10\,k\Omega$			60		k
Supply Current	$T_A = 25°C$		11		100	µA
Power Consumption	$T_A = 25°C$		330		3	µW/mW
V_{OS}	$R_S \leq 10\,k\Omega$		6.5		7.5	mV
I_{OS}	$R_S \leq 10\,k\Omega$		8		25	nA
I_{bias}			10		80	nA
Input Voltage Range		±13.5		±13.5		V
Large Signal Voltage Gain	$V_O = \pm 15V$, $R_L = 100\,\Omega$	50				k
	$R_L = 10\,k\Omega$			50		k
Output Voltage Swing	$R_L = 100\,k\Omega$	±12				V
	$R_L = 10\,k\Omega$			±12		V
Common Mode Rejection Ratio	$R_S \leq 10\,k\Omega$	70		70		dB
Supply Voltage Rejection ratio	$R_S \leq 10\,k\Omega$	74		74		dB
Supply Current		11		100		µA
Power Consumption			300		3	µW/mW

Typical Performance Characteristics

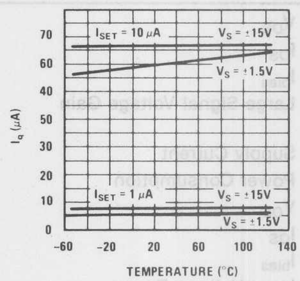
Input Bias Current vs I_{SET}



Input Bias Current vs Temperature



Quiescent Current (I_q) vs Temperature



Section 4

Instrumentation Amplifiers

4

Section Contents

Note. For additional information on instrumentation amplifiers, see National Semiconductor's Hybrid Products Databook.

All of the amplifiers in this guide are true differential input instrumentation amplifiers with very high common mode rejection and adjustable gain.

Features	Characteristics						Part Number		**
	I_B Max	V_{OS}in Max	$\frac{\Delta V_{OS}}{\Delta T}$	Gain Lin.	Gain Tempco	Gain Error	−25°C to 85°C	−55°C to 125°C	Page Number
90 μW dissipation, wide supply range, one external gain set resistor	125 nA 100 nA	2 mV 1 mV	10 μV/°C 10 μV/°C	0.03% 0.03%	*	3% max 1% max	LH0036C	LH0036	3-4
Low cost, one external gain set resistor	 500 nA	2 mV 1 mV	10 μV/°C 10 μV/°C	0.03% 0.03%	* *	1% 0.3%	LH0037C	LH0037	3-12
Ultra low drift, all gain set resistors internal, very low noise, very linear, guard drive amplifier included	100 nA	150 μV 100 μV	1 μV/°C max 0.25 μV/°C max	1 ppm 1 ppm	7 ppm/°C 7 ppm/°C	0.1% 0.1%	LH0038C	LH0038	3-15
Programmable gain fast settling	500 pA 500 pA	10 mV 5 mV	10 μV/°C 10 μV/°C	20 ppm 20 ppm	1 ppm/°C 1 ppm/°C	0.3% max 0.3% max	LH0084C	LH0084	3-26

*Dependent upon external resistors.

**Refers to Hybrid Products Databook, 1982 edition

National Semiconductor

Definition of Terms

Bandwidth: That frequency at which the voltage gain is reduced to $1/\sqrt{2}$ times the low frequency value.

Common-Mode Rejection Ratio: The ratio of the input common-mode voltage range to the peak-to-peak change in input offset voltage over this range.

Harmonic Distortion: That percentage of harmonic distortion being defined as one-hundred times the ratio of the root-mean-square (rms) sum of the harmonics to the fundamental. % harmonic distortion =

$$\frac{(V2^2 + V3^2 + V4^2 + \ldots)^{1/2}\ (100\%)}{V1}$$

where V1 is the rms amplitude of the fundamental and V2, V3, V4, . . . are the rms amplitudes of the individual harmonics.

Input Bias Current: The average of the two input currents.

Input Common-Mode Voltage Range: The range of voltages on the input terminals for which the amplifier is operational. Note that the specifications are not guaranteed over the full common-mode voltage range unless specifically stated.

Input Impedance: The ratio of input voltage to input current under the stated conditions for source resistance (R_S) and load resistance (R_L).

Input Offset Current: The difference in the currents into the two input terminals when the output is at zero.

Input Offset Voltage: That voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage.

Input Resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Input Voltage Range: The range of voltages on the input terminals for which the amplifier operates within specifications.

Large-Signal Voltage Gain: The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

Output Impedance: The ratio of output voltage to output current under the stated conditions for source resistance (R_S) and load resistance (R_L).

Output Resistance: The small signal resistance seen at the output with the output voltage near zero.

Output Voltage Swing: The peak output voltage swing, referred to zero, that can be obtained without clipping.

Offset Voltage Temperature Drift: The average drift rate of offset voltage for a thermal variation from room temperature to the indicated temperature extreme.

Power Supply Rejection: The ratio of the change in input offset voltage to the change in power supply voltages producing it.

Settling Time: The time between the initiation of the input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

Slew Rate: The internally-limited rate of change in output voltage with a large-amplitude step function applied to the input.

Supply Current: The current required from the power supply to operate the amplifier with no load and the output midway between the supplies..

Transient Response: The closed-loop step-function response of the amplifier under small-signal conditions.

Unity Gain Bandwidth: The frequency range from dc to the frequency where the amplifier open loop gain rolls off to one.

Voltage Gain: The ratio of output voltage to input voltage under the stated conditions for source resistance (R_S) and load resistance (R_L).

LM121/LM221/LM321, LM121A/LM221A/LM321A Precision Preamplifiers

General Description

The LM121 series are precision preamplifiers designed to operate with general purpose operational amplifiers to drastically decrease dc errors. Drift, bias current, common mode and supply rejection are more than a factor of 50 better than standard op amps alone. Further, the added dc gain of the LM121 decreases the closed loop gain error.

The LM121 series operates with supply voltages from ±3V to ±20V and has sufficient supply rejection to operate from unregulated supplies. The operating current is programmable from 5µA to 200µA so bias current, offset current, gain and noise can be optimized for the particular application while still realizing very low drift. Super-gain transistors are used for the input stage so input error currents are lower than conventional amplifiers at the same operating current. Further, the initial offset voltage is easily nulled to zero.

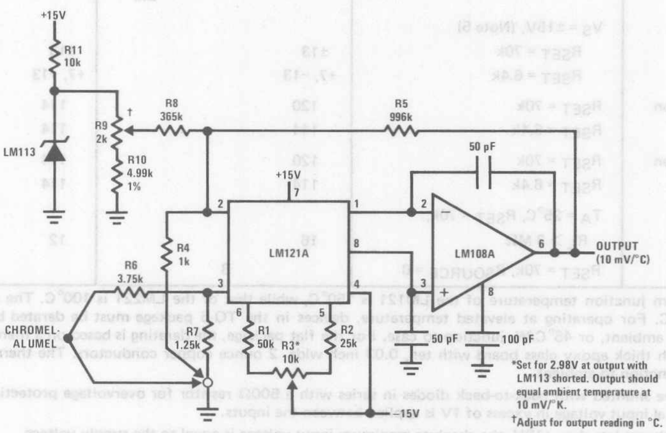
Features

- Guaranteed drift of LM121A series – 0.2µV/°C
- Guaranteed drift of LM121 series – 1µV/°C
- Offset voltage less than 0.4 mV
- Bias current less than 10 nA at 10µA operating current
- CMRR 126 dB minimum
- 120 dB supply rejection
- Easily nulled offset voltage

The extremely low drift of the LM121 will improve accuracy on almost any precision dc circuit. For example, instrumentation amplifier, strain gauge amplifiers and thermocouple amplifiers now using chopper amplifiers can be made with the LM121. The full differential input and high common-mode rejection are another advantage over choppers. For applications where low bias current is more important than drift, the operating current can be reduced to low values. High operating currents can be used for low voltage noise with low source resistance. The programmable operating current of the LM121 allows tailoring the input characteristics to match those of specialized op amps.

The LM121 is specified over a –55°C to +125°C temperature range, the LM221 over a –25°C to +85°C range and the LM321 over a 0°C to +70°C temperature range.

Typical Applications



Thermocouple Amplifier with Cold Junction Compensation

Input Voltage (Note 3)	±15V
Operating Temperature Range	
LM121	−55°C to +125°C
LM221	−25°C to +85°C
LM321	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 4) LM121, LM221, LM321

PARAMETER	CONDITIONS	LM121, LM221			LM321			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$, $6.4k \le R_{SET} \le 70k$			0.7			1.5	mV
Input Offset Current	$T_A = 25°C$,							
	$R_{SET} = 70k$			1			2	nA
	$R_{SET} = 6.4k$			10			20	nA
Input Bias Current	$T_A = 25°C$,							
	$R_{SET} = 70k$			10			18	nA
	$R_{SET} = 6.4k$			100			180	nA
Input Resistance	$T_A = 25°C$,							
	$R_{SET} = 70k$	4			2			MΩ
	$R_{SET} = 6.4k$	0.4			0.2			MΩ
Supply Current	$T_A = 25°C$, $R_{SET} = 70k$			1.5			2.2	mA
Input Offset Voltage	$6.4k \le R_{SET} \le 70k$			1.0			2.5	mV
Input Bias Current	$R_{SET} = 70k$			30			28	nA
	$R_{SET} = 6.4k$			300			280	nA
Input Offset Current	$R_{SET} = 70k$			3			4	nA
	$R_{SET} = 6.4k$			30			40	nA
Input Offset Current Drift	$R_{SET} = 70k$		3			3		pA/°C
Average Temperature Coefficient of Input Offset Voltage	$R_S \le 200\Omega$, $6.4k \le R_{SET} \le 70k$ Offset Voltage Nulled			1			1	µV/°C
Long Term Stability			5			5		µV/yr
Supply Current				2.5			3.5	mA
Input Voltage Range	$V_S = \pm 15V$, (Note 5)							
	$R_{SET} = 70k$	±13			±13			V
	$R_{SET} = 6.4k$	+7, −13			+7, −13			V
Common-Mode Rejection Ratio	$R_{SET} = 70k$	120			114			dB
	$R_{SET} = 6.4k$	114			114			dB
Supply Voltage Rejection Ratio	$R_{SET} = 70k$	120			114			dB
	$R_{SET} = 6.4k$	114			114			dB
Voltage Gain	$T_A = 25°C$, $R_{SET} = 70k$, $R_L > 3\ M\Omega$	16			12			V/V
Noise	$R_{SET} = 70k$, $R_{SOURCE} = 0$		8			8		$nV/\sqrt{Hz}$

Note 1: The maximum junction temperature of the LM121 is 150°C, while that of the LM221 is 100°C. The maximum junction temperature of the LM321 is 85°C. For operating at elevated temperature, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. For the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/6 inch thick epoxy glass board with ten, 0.03 inch wide, 2 ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W junction to ambient.

Note 2: The inputs are shunted with back-to-back diodes in series with a 500Ω resistor for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs.

Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: These specifications apply for $\pm 5 \le V_S \le \pm 20V$ and $-55°C \le T_A \le +125°C$, unless otherwise specified. With the LM221, however, all temperature specifications are limited to $-25°C \le T_A \le +85°C$, and for the LM321 the specifications apply over a 0°C to +70°C temperature range.

Note 5: External precision resistor — 0.1% — can be placed from pins 1 and 8 to 7 to increase positive common-mode range.

Absolute Maximum Ratings

Supply Voltage	±20V
Power Dissipation (Note 1)	500 mW
Differential Input Voltage (Notes 2 and 3)	±15V
Input Voltage (Note 3)	±15V
Operating Temperature Range	
LM121A	−55°C to +125°C
LM221A	−25°C to +85°C
LM321A	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 4) LM121A, LM221A, LM321A

PARAMETER	CONDITIONS	LM121A, LM221A			LM321A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$, $6.4k \le R_{SET} \le 70k$		0.2	0.4		0.2	0.4	mV
Input Offset Current	$T_A = 25°C$, $R_{SET} = 70k$		0.3	0.5		0.3	0.5	nA
	$R_{SET} = 6.4k$			5			5	nA
Input Bias Current	$T_A = 25°C$, $R_{SET} = 70k$		5	10		5	15	nA
	$R_{SET} = 6.4k$		50	100		50	150	nA
Input Resistance	$T_A = 25°C$, $R_{SET} = 70k$	4	8		2	8		MΩ
	$R_{SET} = 6.4k$	0.4			0.2			MΩ
Supply Current	$T_A = 25°C$, $R_{SET} = 70k$		0.8	1.5		0.8	2.2	mA
Input Offset Voltage	$6.4k \le R_{SET} \le 70k$		0.5	0.65		0.5	0.65	mV
Input Bias Current	$R_{SET} = 70k$		15	30		15	25	nA
	$R_{SET} = 6.4k$		150	300		150	250	nA
Input Offset Current	$R_{SET} = 70k$		0.5	1		0.5	1	nA
	$R_{SET} = 6.4k$		5	10		5	10	nA
Input Offset Current Drift	$R_{SET} = 70k$		3			3		pA/°C
Average Temperature Coefficient of Input Offset Voltage	$R_S \le 200\Omega$, $6.4k \le R_{SET} \le 70k$ Offset Voltage Nulled		0.07	0.2		0.07	0.2	µV/°C
Long Term Stability			3			3		µV/yr
Supply Current			1	2.5		1	3.5	mA
Input Voltage Range	$V_S = \pm 15V$, (Note 5) $R_{SET} = 70k$	±13			±13			V
	$R_{SET} = 6.4k$	+7, −13			+7, −13			V
Common-Mode Rejection Ratio	$R_{SET} = 70k$	126	140		126	140		dB
	$R_{SET} = 6.4k$	120	130		120	130		dB
Supply Voltage Rejection Ratio	$R_{SET} = 70k$	120	126		118	126		dB
	$R_{SET} = 6.4k$	114	120		114	120		dB
Voltage Gain	$T_A = 25°C$, $R_{SET} = 70k$, $R_L > 3 M\Omega$	16	20		12	20		V/V
Noise	$R_{SET} = 70k$, $R_{SOURCE} = 0$		8			8		$nV/\sqrt{Hz}$

Note 1: The maximum junction temperature of the LM121A is 150°C, while that of the LM221A is 100°C. The maximum junction temperature of the LM321A is 85°C. For operating at elevated temperature, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W junction to case. For the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/6 inch thick epoxy glass board with ten, 0.03 inch wide, 2 ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W junction to ambient.

Note 2: The inputs are shunted with back-to-back diodes in series with a 500Ω resistor for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs.

Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: These specifications apply for $\pm 5 \le V_S \le \pm 20V$ and $-55°C \le T_A \le +125°C$, unless otherwise specified. With the LM221A, however, all temperature specifications are limited to $-25°C \le T_A \le +85°C$, and for the LM321A the specifications apply over a 0°C to +70°C temperature range.

Note 5: External precision resistor – 0.1% – can be placed from pins 1 and 8 to 7 to increase positive common-mode range.

Frequency Compensation

UNIVERSAL COMPENSATION

The additional gain of the LM121 preamplifier when used with an operational amplifier usually necessitates additional frequency compensation. When the closed loop gain of the op amp with the LM121 is less than the gain of the LM121 alone, more compensation is needed. The worst case situation is when there is 100% feedback—such as a voltage follower or integrator—and the gain of the LM121 is high. When high closed loop gains are used—for example A_V = 1000—and only an addition gain of 200 is inserted by the LM121, the frequency compensation of the op amp will usually suffice.

The frequency compensation shown here is designed to operate with any unity-gain stable op amp. *Figure 1* shows the basic configuration of frequency stabilizing network. In operation the output of the LM121 is rendered single ended by a 0.01μF bypass capacitor to ground. Overall frequency compensation then is achieved by an integrating capacitor around the op amp.

$$\text{Bandwidth at unity-gain} \cong \frac{12}{2\pi R_{SET} C}$$

$$\text{for 0.5 MHz bandwidth } C = \frac{4}{10^6 R_{SET}}$$

For use with higher frequency op amps such as the LM118 the bandwidth may be increased to about 2 MHz.

If the closed loop gain is greater than unity, "C" may be decreased to:

$$C = \frac{4}{10^6\ A_{CL}\ R_{SET}}$$

ALTERNATE COMPENSATION

The two compensation capacitors can be made equal for improved power supply rejection. In this case the formula for the compensation capacitor is:

$$C = \frac{8}{10^6\ A_{CL}\ R_{SET}}$$

Table I shows typical values for the two compensating capacitors for various gains and operating currents.

TABLE I

CLOSED LOOP GAIN	CURRENT SET RESISTOR 120 kΩ	60 kΩ	30 kΩ	12 kΩ	6 kΩ
A_V = 1	68	130	270	680	1300
A_V = 5	15	27	56	130	270
A_V = 10	10	15	27	68	130
A_V = 50	1	3	5	15	27
A_V = 100	–	1	3	5	10
A_V = 500	–	–	1	1	3
A_V = 1000	–	–	–	–	–

This table applies for the LM108, LM101A, LM741, LM118. Capacitance is in pF.

DESIGN EQUATIONS FOR THE LM121 SERIES

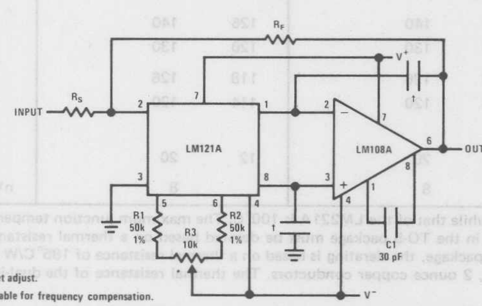
$$\text{Gain } A_V \approx \frac{1.2 \times 10^6}{R_{SET}}$$

Null Pot Value should be 10% of R_{SET}

$$\text{Operating Current} \approx \frac{2 \times 0.65V}{R_{SET}}$$

$$\text{Positive Common-Mode Limit} \approx V^+ - \left[0.6 - \frac{0.65V \times 50k}{R_{SET}}\right]$$

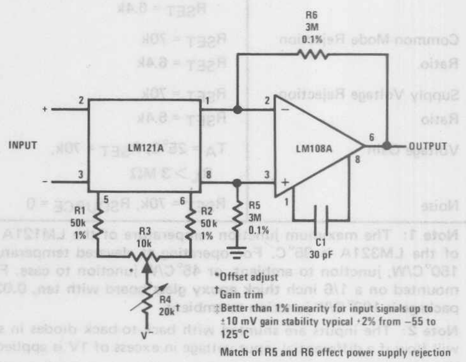
Typical Applications



*Offset adjust.

†See table for frequency compensation.

FIGURE 1. Low Drift Op Amp Using the LM121A as a Preamp



*Offset adjust

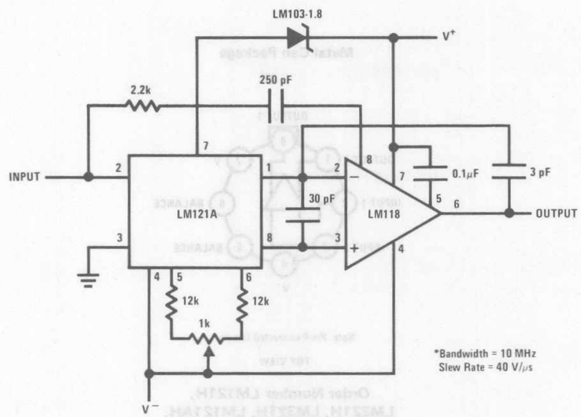
†Gain trim

‡Better than 1% linearity for input signals up to ±10 mV gain stability typical ·2% from −55 to 125°C

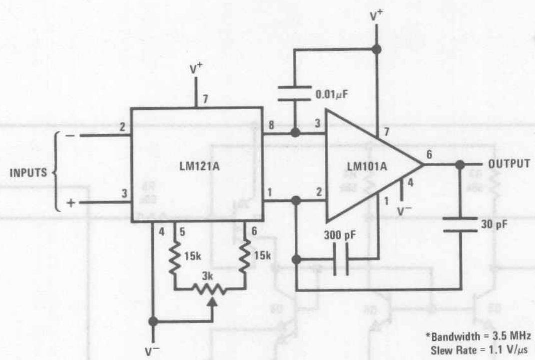
Match of R5 and R6 effect power supply rejection

Gain of 1000 Instrumentation Amplifier‡

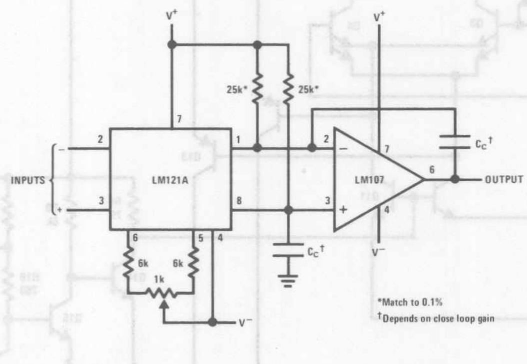
Typical Applications (Continued)



High Speed* Inverting Amplifier with Low Drift

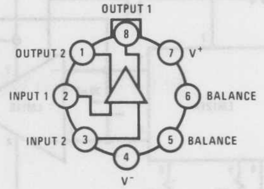


Medium Speed* General Purpose Amplifier



Increased Common-Mode Range at High Operating Currents

Metal Can Package



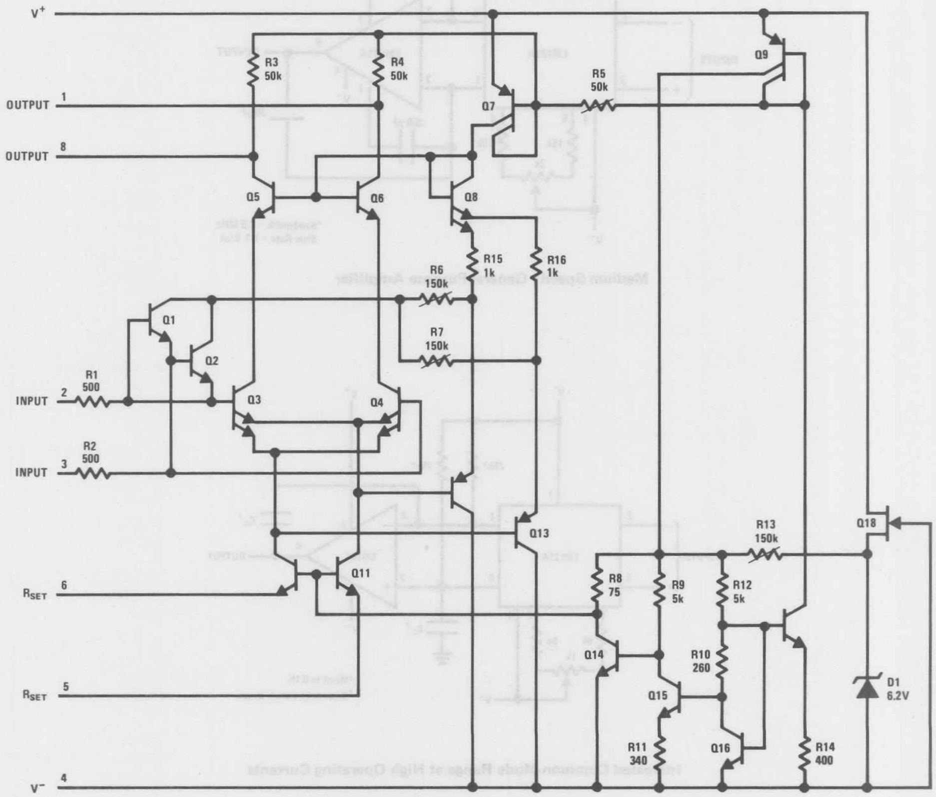
Note: Pin 4 connected to case.

TOP VIEW

Order Number LM121H, LM221H, LM321H, LM121AH, LM221AH or LM321AH
See NS Package H08C

Note: Outputs are inverting from the input of the same number.

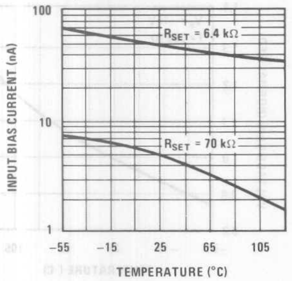
Schematic Diagram*



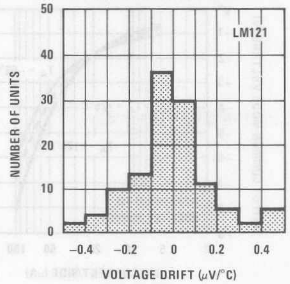
*Pin connections shown on schematic diagram and typical applications are for TO-5 package.

Typical Performance Characteristics

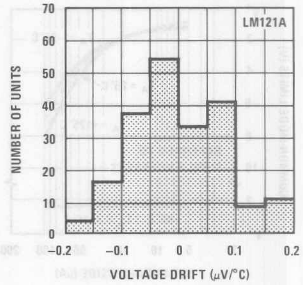
Input Bias Current



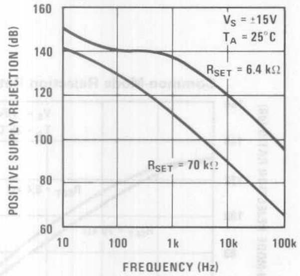
Distribution of Offset Voltage Drift (Nulled)



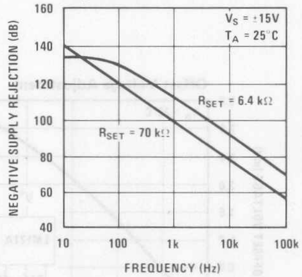
Distribution of Offset Voltage Drift (Nulled)



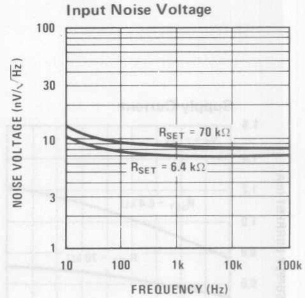
Positive Power Supply Rejection



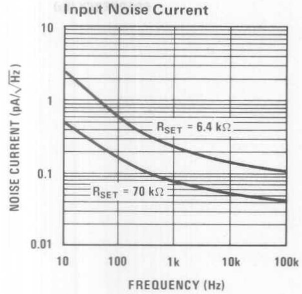
Negative Power Supply Rejection



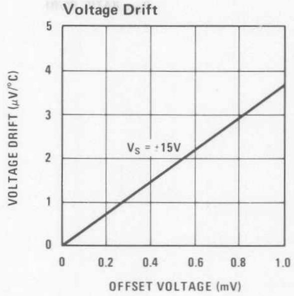
Input Noise Voltage



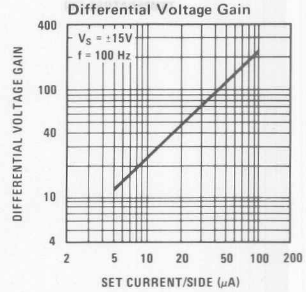
Input Noise Current



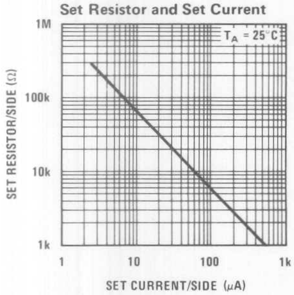
Voltage Drift



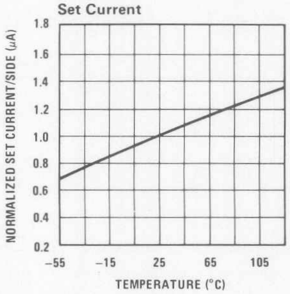
Differential Voltage Gain



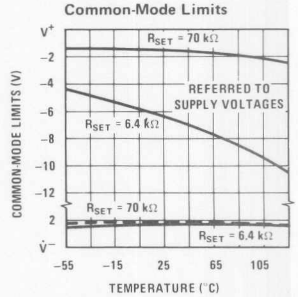
Set Resistor and Set Current



Set Current

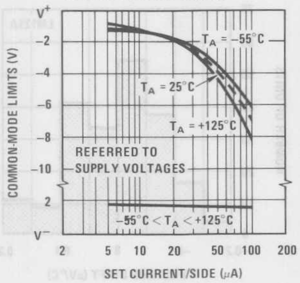


Common-Mode Limits

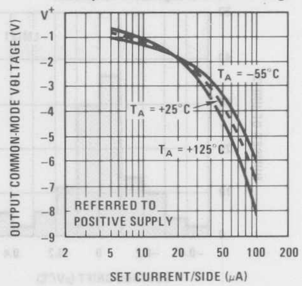


Typical Performance Characteristics (Continued)

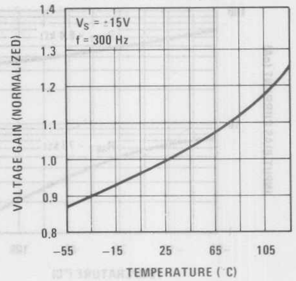
Common-Mode Limits



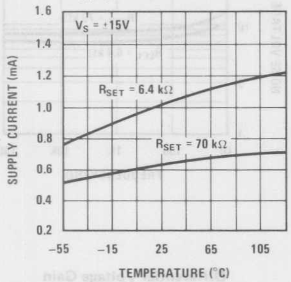
Output Common-Mode Voltage



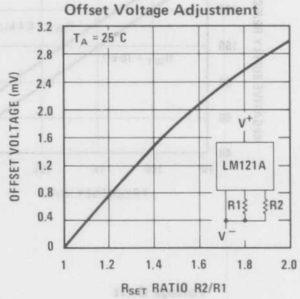
Differential Voltage Gain



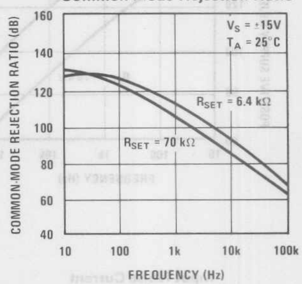
Supply Current



Offset Voltage Adjustment



Common-Mode Rejection Ratio



National Semiconductor

Instrumentation Amplifiers
PRELIMINARY

LM163/LM363 Precision Instrumentation Amplifier

General Description

The LM163 is a monolithic true instrumentation amplifier. It requires no external parts for fixed gains of 10, 100 and 1,000. High precision is attained by on-chip trimming of offset voltage and gain. A super beta bipolar input stage gives very low input voltage noise, extremely low offset voltage drift, and high common-mode rejection ratio. A new two-stage amplifier design yields an open loop gain of 10,000,000 and a gain bandwidth product of 30 MHz, yet remains stable for all closed loop gains, even with large capacitive loads. Supply voltage range is ±5V to ±18V.

The LM163 has separate force, sense, and reference pins to allow gain to be increased using external resistors. Twin differential shield drivers eliminate bandwidth loss due to shield capacitance. Compensation pins are available to allow simple low-pass filtering. The LM163 with all options is in a 16-pin dual-in-line package.

For less stringent applications requiring a single fixed gain, it is also available in an 8-pin TO-5 package. Shield drivers, pin-strapped gain options, and offset adjustment pins are eliminated on the 8-pin versions. Gain is internally set at 10, 100, or 500, but may be increased with the addition of external resistors.

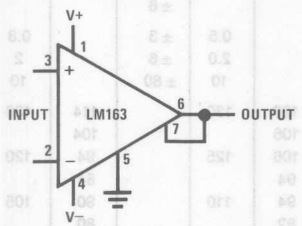
The LM163 is rated for −55°C to +125°C operation. The LM363 is rated for 0°C to 70°C operation.

Features

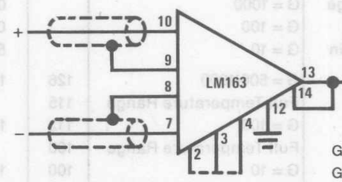
- Offset and gain pretrimmed
- 7 nV/$\sqrt{Hz}$ input noise
- 130 dB CMRR typical
- 2 nA bias current typical
- No external parts required
- Differential shield drivers
- Available at 0.5 μV/°C maximum drift
- Can be used as a high performance op-amp

Typical Connections

8-Pin Package



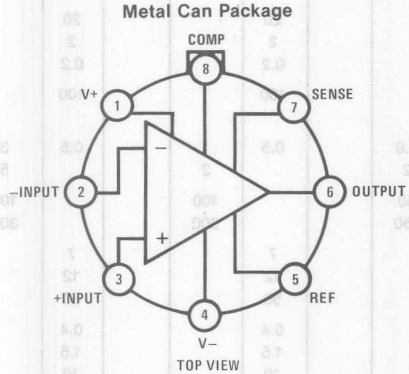
16-Pin Package



G = 10 2, 3, 4, open
G = 100 3–4 shorted
G = 1000 2–4 shorted

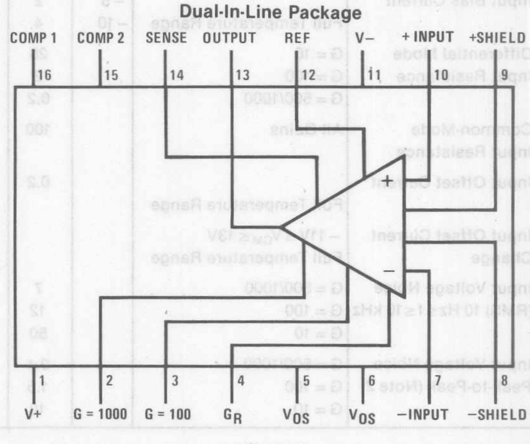
Connection Diagrams

Metal Can Package



Order Number LM163AH-10, LM163H-10, LM363AH-10, LM363H-10, LM163AH-100, LM163H-100, LM363AH-100, LM363H-100, LM163AH-500, LM163H-500, LM363AH-500 or LM363H-500
See NS Package H08C

Dual-In-Line Package



Order Number LM163AD, LM136D, LM363AD or LM363D
See NS Package D16C

Absolute Maximum Ratings

Supply Voltage	± 18V
Differential Input Voltage	± 10V
Differential Input Current	± 20 mA
Common-Mode Input Voltage	Equal to Supply Voltage
Reference and Sense Voltage	± 25V

Electrical Characteristics (Note 1)

Parameter	Conditions	LM163A/LM363A			LM163			LM363			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	T_A = 25°C, G = 500		10	± 30		20	± 50		30	± 100	μV
Fixed Gain	G = 100		25	± 75		35	± 100		50	± 200	μV
	G = 10		0.2	± 0.6		0.3	± 1.0		0.5	± 2.0	mV
	Full Temperature Range										
	G = 500			± 80			± 150			± 300	μV
	G = 100			± 200			± 400			± 500	μV
	G = 10			± 2			± 4			± 5	mV
Input Offset Voltage	G = 500		0.2	± 0.5			± 2			± 4	μV/°C
Temperature Drift	G = 100			± 2.0			± 5			± 8	μV/°C
Fixed Gain	G = 10			± 25			± 50			± 75	μV/°C
Input Offset Voltage	T_A = 25°C, G = 1000		10	± 50		25	± 100		50	± 200	μV
Programmable Gain	G = 100		25	± 150		50	± 300		100	± 400	μV
	G = 10		0.3	± 1		0.5	± 2		1.0	± 3	mV
	Full Temperature Range										
	G = 1000			± 100			± 200			± 400	μV
	G = 100			± 300			± 500			± 800	μV
	G = 10			± 3			± 6			± 7	mV
Input Offset Voltage	G = 1000		0.2	± 0.5		0.5	± 3		0.8	± 5	μV/°C
Temperature Drift	G = 100		0.5	± 2.0		2.0	± 6		2	± 10	μV/°C
Programmable Gain	G = 10		5.0	± 25		10	± 80		10	± 100	μV/°C
Common-Mode	G = 500/1000	126	140		120	130		114	130		dB
Rejection Ratio	Full Temperature Range	115			106			104			dB
	G = 100	112	130		106	125		94	120		dB
	Full Temperature Range	100			94			84			dB
	G = 10	100	115		94	110		90	105		dB
	Full Temperature Range	88			82			80			dB
Input Bias Current		− 5	2	5	− 5	2	5	− 10	2	10	nA
	Full Temperature Range	− 10	4	10	− 10	4	10	− 20		− 20	nA
Differential Mode	G = 10		20			20			20		GΩ
Input Resistance	G = 100		2			2			2		GΩ
	G = 500/1000		0.2			0.2			0.2		GΩ
Common-Mode Input Resistance	All Gains		100			100			100		GΩ
Input Offset Current			0.2	1.0		0.5	1		0.5	3	nA
	Full Temperature Range			2			2			5	nA
Input Offset Current	− 11V ≤ V_{CM} ≤ 13V			50			100			100	pA/V
Change	Full Temperature Range			150			300			300	pA/V
Input Voltage Noise	G = 500/1000		7			7			7		nV$\sqrt{Hz}$
(RMS) 10 Hz ≤ f ≤ 10 kHz	G = 100		12			12			12		nV$\sqrt{Hz}$
	G = 10		50			50			50		nV$\sqrt{Hz}$
Input Voltage Noise	G = 500/1000		0.4			0.4			0.4		μV
Peak-to-Peak (Note 2)	G = 100		1.5			1.5			1.5		μV
	G = 10		10			10			10		μV

Note 1: Unless otherwise noted, these conditions apply: $V^+ = V^- = 15V$, output load = 5 kΩ, $V_{CM} = 0$, reference pin is grounded, output sense is tied to output force, and junction temperature is 25°C.

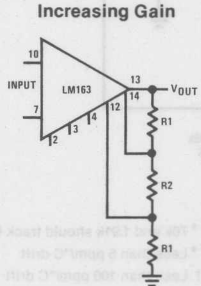
Note 2: Measured for 100 seconds at a bandwidth of 0.01 Hz to 10 Hz.

Electrical Characteristics (Continued) (Note 1)

Parameter	Conditions	LM163A/LM363A			LM163			LM363			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Current Noise (RMS)	10 Hz ≤ f ≤ 10 kHz		0.15			0.15			0.15		pA/√Hz
Input Current Noise Peak-to-Peak	0.01 Hz ≤ f ≤ 10 Hz		40			40			40		pA
Gain Error	Fixed G = 10, 100, 500		0.05	0.2		0.05	0.3		0.1	0.5	%
	Programmable G = 100		0.05	0.2		0.05	0.3		0.1	0.5	%
	Programmable G = 10		0.4	1.0		0.4	1.0		0.6	1.5	%
	Programmable G = 1000		0.4	1.0		0.4	1.0		0.4	1.5	%
Gain Non-Linearity	$-10V \le V_{OUT} \le +10V$,										
	G = 10, 100		0.005	0.01		0.005	0.02		0.01	0.03	%
	G = 500, 1000		0.007	0.02		0.007	0.03			0.05	%
Supply Voltage Rejection Ratio—Positive	G = 500, 1000	120	130		120	130		110	130		dB
	G = 100	105	120		105	120		100	120		dB
	G = 10	90	100		90	100		85	100		dB
Supply Voltage Rejection Ratio—Negative	G = 500, 1000	110	120		105	120		100	120		dB
	G = 100	96	106		90	106		85	106		dB
	G = 10	80	86		75	86		70	86		dB
Common-Mode Input Voltage Range	$V^+ = V^- = 15V$	−11.6		+13.8	−11.6		+13.8	−11.6		+13.8	V
	$V^+ = V^- = 5V$	−2.75		+3.8	−2.75		+3.8	−2.75		+3.8	V
Small Signal Bandwidth	G = 500, 1000		30			30			30		kHz
	G = 100		100			100			100		kHz
	G = 10		200			200			200		kHz
Settling Time to 0.1%	$\Delta V_{OUT} = 10V$, G = 500, 1000		70			70			70		μs
	G = 100		25			25			25		μs
	G = 10		20			20			20		μs
Open Loop Gain	G = 500, 1000	2×10^6	10^7		2×10^6	10^7		10^6	10^7		V/V
Gain Shift with Temperature	G = 500, 1000		15			15			15		ppm/°C
	G = 100		5			5			5		ppm/°C
	G = 10		5			5			5		ppm/°C
Supply Current Positive	Positive		1.2	1.8		1.2	1.8		1.2	2.2	mA
	Negative		1.6	2.2		1.6	2.2		1.6	2.5	mA
Reference and Feedback Resistance		35	50	70	35	50	70	30	50	80	kΩ

Typical Applications

Increasing Gain



R1 and R2 should be as low as possible to avoid errors due to 50kΩ input impedance of reference and sense pins. Total resistance (R2 + 2R1) should be above 4 kΩ, however, to prevent excessive load on the LM163 output. The exact formula for calculating gain (G) is:

$$G = G_O \left(1 + \frac{2R1}{R2} + \frac{R1}{50k}\right)$$

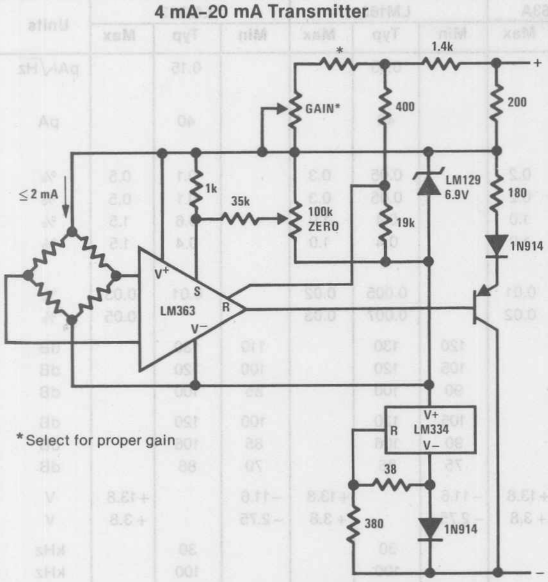
G_O = preset gain

The last term may be ignored in applications where gain accuracy is not critical. The table below gives suggested values for R1 and R2 along with the calculated error due to "closest value" standard 1% resistors.

Gain Increase	1.5	2	2.5	3	4	5	6	7	8	9	10
R1	1.2k	1.2k	2k	2k	1.78k	2k	2.49k	2.94k	3.48k	4.02k	4.53k
R2	5k	2.5k	2.74k	2.05k	1.2k	1k	1k	1k	1k	1k	1k
Error	+0.6%	−0.8%	0	−0.3%	+0.06%	+0.8%	+0.5%	−0.9%	+0.4%	−0.9%	−0.7%

Typical Applications (Continued)

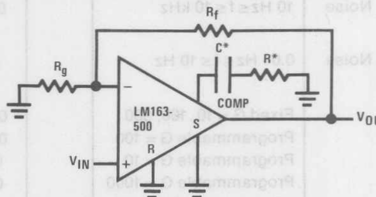
4 mA-20 mA Transmitter



*Select for proper gain

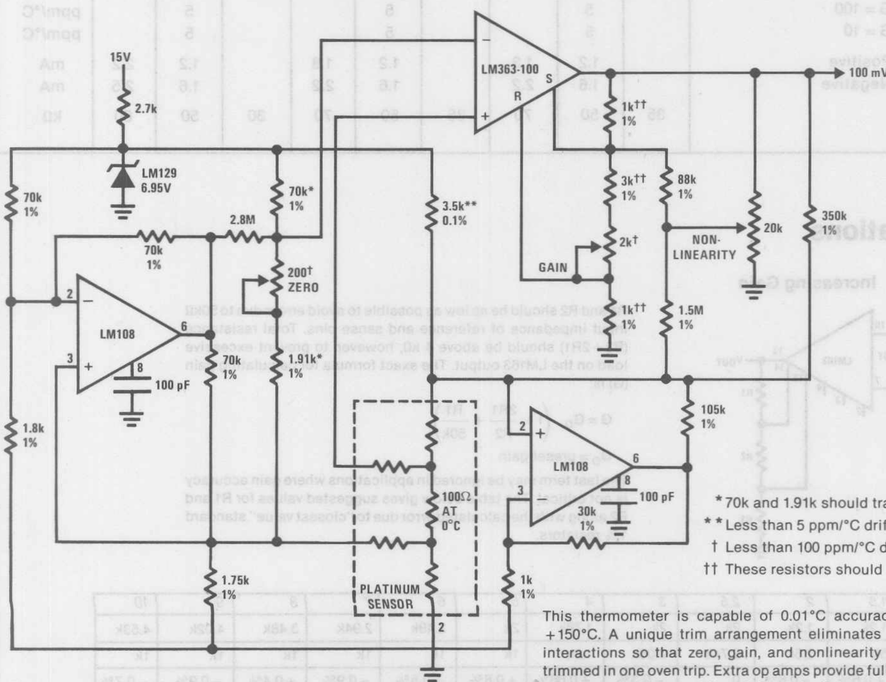
Current regulation is near perfect because the LM163 operates off the Zener reference. Circuitry is simplified by being able to drive the reference pin outside the power supply voltage. Gain and offset adjustments are non-interactive. 2 mA is available to drive the bridge.

LM163 Used as Precision Op Amp



*Select for optimum square wave response. Omit for closed loop gains above 100.

Curvature Corrected Platinum RTD Thermometer



*70k and 1.91k should track to 5 ppm/°C

**Less than 5 ppm/°C drift

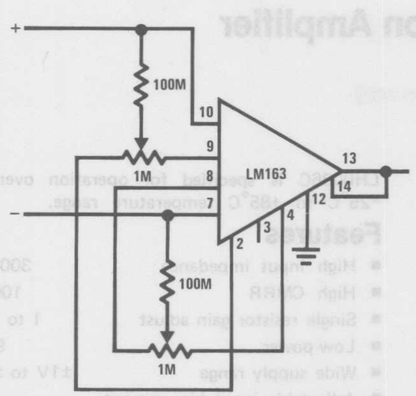
† Less than 100 ppm/°C drift

†† These resistors should track to 20 ppm/°C

This thermometer is capable of 0.01°C accuracy over −50°C to +150°C. A unique trim arrangement eliminates cumbersome trim interactions so that zero, gain, and nonlinearity correction can be trimmed in one oven trip. Extra op amps provide full Kelvin sensing on the sensor without adding drift and offset terms found in other designs.

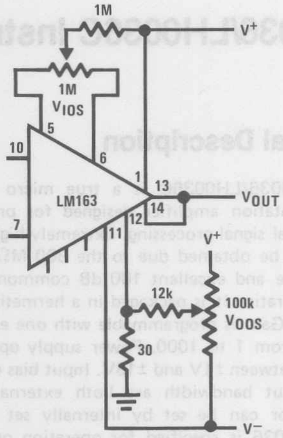
Typical Applications (Continued)

Zeroing Input Bias Current*

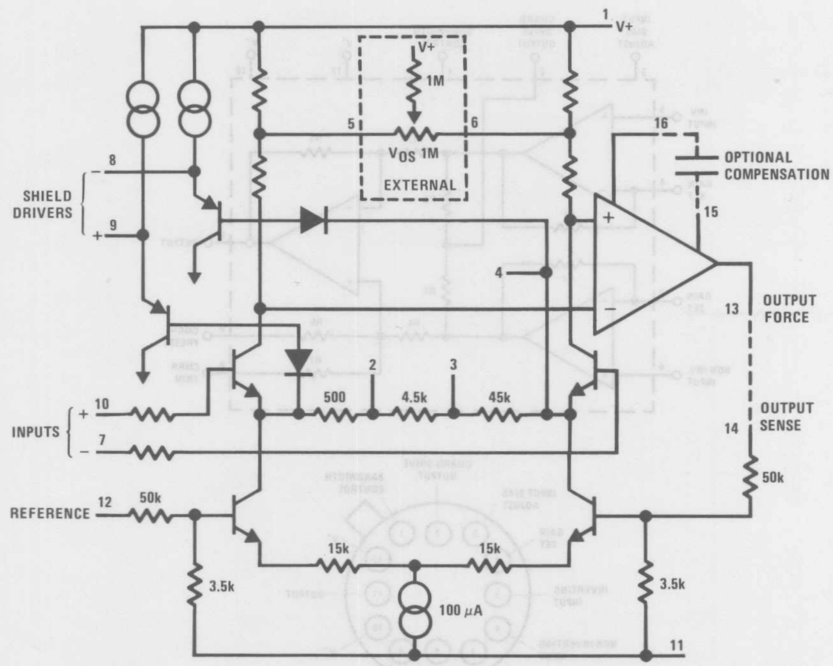


* For gains of 10 and 100

V_{IOS} and V_{OOS} Adjust



Simplified Schematic (for 16-pin dual-in-line package)



LH0036/LH0036C Instrumentation Amplifier

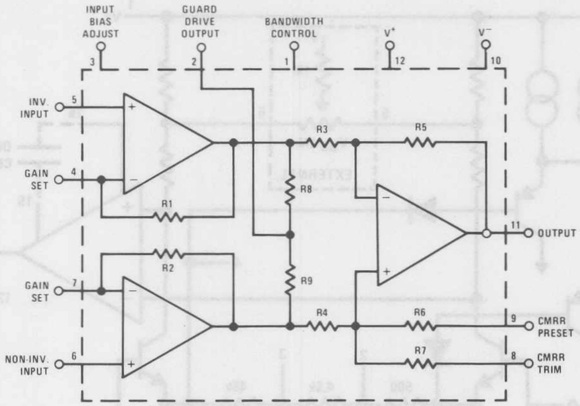
General Description

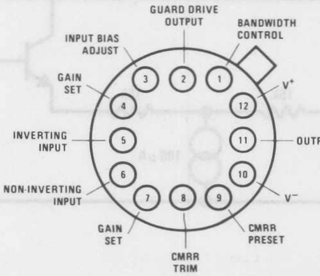
The LH0036/LH0036C is a true micro power instrumentation amplifier designed for precision differential signal processing. Extremely high accuracy can be obtained due to the 300 MΩ input impedance and excellent 100 dB common mode rejection ratio. It is packaged in a hermetic TO-8 package. Gain is programmable with one external resistor from 1 to 1000. Power supply operating range is between ±1V and ±18V. Input bias current and output bandwidth are both externally adjustable or can be set by internally set values. The LH0036 is specified for operation over the −55°C to +125°C temperature range and the LH0036C is specified for operation over the −25°C to +85°C temperature range.

Features

- High input impedance 300 MΩ
- High CMRR 100 dB
- Single resistor gain adjust 1 to 1000
- Low power 90μW
- Wide supply range ±1V to ±18V
- Adjustable input bias current
- Adjustable output bandwidth
- Guard drive output

Equivalent Circuit and Connection Diagrams





TOP VIEW

Order Number LH0036G or LH0036CG
See NS Package H12B

Absolute Maximum Ratings

Supply Voltage	±18V	Short Circuit Duration	Continuous
Differential Input Voltage	±30V	Operating Temperature Range	
Input Voltage Range	$\pm V_S$	LH0036	−55°C to +125°C
Shield Drive Voltage	$\pm V_S$	LH0036C	−25°C to +85°C
CMRR Preset Voltage	$\pm V_S$	Storage Temperature Range	−65°C to +150°C
CMRR Trim Voltage	$\pm V_S$	Lead Temperature, Soldering 10 seconds	300°C
Power Dissipation (Note 3)	1.5W		

Electrical Characteristics (Notes 1 and 2)

PARAMETER	CONDITIONS	LIMITS LH0036 MIN	LH0036 TYP	LH0036 MAX	LH0036C MIN	LH0036C TYP	LH0036C MAX	UNITS
Input Offset Voltage (V_{IOS})	R_S = 1.0kΩ, T_A = 25°C		0.5	1.0		1.0	2.0	mV
	R_S = 1.0kΩ			2.0			3.0	mV
Output Offset Voltage (V_{OOS})	R_S = 1.0kΩ, T_A = 25°C		2.0	5.0		5.0	10	mV
	R_S = 1.0kΩ			6.0			12	mV
Input Offset Voltage Tempco ($\Delta V_{IOS}/\Delta T$)	$R_S \leq$ 1.0kΩ		10			10		μV/°C
Output Offset Voltage Tempco ($\Delta V_{OOS}/\Delta T$)			15			15		μV/°C
Overall Offset Referred to Input (V_{OS})	A_V = 1.0		2.5			6.0		mV
	A_V = 10		0.7			1.5		mV
	A_V = 100		0.52			1.05		mV
	A_V = 1000		0.502			1.005		mV
Input Bias Current (I_B)	T_A = 25°C		40	100		50	125	nA
				150			200	nA
Input Offset Current (I_{OS})	T_A = 25°C		10	40		20	50	nA
				80			100	nA
Small Signal Bandwidth	A_V = 1.0, R_L = 10kΩ		350			350		kHz
	A_V = 10, R_L = 10kΩ		35			35		kHz
	A_V = 100, R_L = 10kΩ		3.5			3.5		kHz
	A_V = 1000, R_L = 10kΩ		350			350		Hz
Full Power Bandwidth	V_{IN} = ±10V, R_L = 10k, A_V = 1		5.0			5.0		kHz
Input Voltage Range	Differential	±10	±12		±10	±12		V
	Common Mode	±10	±12		±10	±12		V
Gain Nonlinearity			0.03			0.03		%
Deviation From Gain Equation Formula	A_V = 1 to 1000		±0.3	±1.0		±1.0	±3.0	%
PSRR	$\pm 5.0V \leq V_S \leq \pm 15V$, A_V = 1.0		1.0	2.5		1.0	5.0	mV/V
	$\pm 5.0V \leq V_S \leq \pm 15V$, A_V = 100		0.05	0.25		0.10	0.50	mV/V
CMRR	A_V = 1.0, DC to 100 Hz, ΔR_S = 1.0k		1.0	2.5		2.5	5.0	mV/V
	A_V = 10		0.1	0.25		0.25	0.50	mV/V
	A_V = 100		50	100		50	100	μV/V
Output Voltage	V_S = ±15V, R_L = 10kΩ,	±10	±13.5		±10	±13.5		V
	V_S = ±1.5V, R_L = 100kΩ	±0.6	±0.8		±0.6	±0.8		V
Output Resistance			0.5			0.5		Ω
Supply Current			300	400		400	600	μA
Equivalent Input Noise Voltage	0.1 Hz < f < 10 kHz, R_S < 50Ω		20			20		μV/p-p
Slew Rate	ΔV_{IN} = ±10V, R_L = 10kΩ, A_V = 1.0		0.3			0.3		V/μs
Settling Time	To ±10 mV, R_L = 10kΩ, ΔV_{OUT} = 1.0V, A_V = 1.0		3.8			3.8		μs
	A_V = 100		180			180		μs

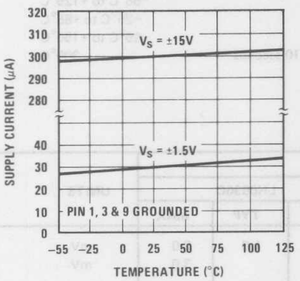
Note 1: Unless otherwise specified, all specifications apply for V_S = ±15V, Pins 1, 3, and 9 grounded, −25°C to +85°C for the LH0036C and −55°C to +125°C for the LH0036.

Note 2: All typical values are for T_A = 25°C.

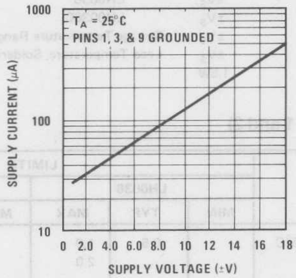
Note 3: The maximum junction temperature is 150°C. For operation at elevated temperature derate the G package on a thermal resistance of 90°C/W, above 25°C.

Typical Performance Characteristics

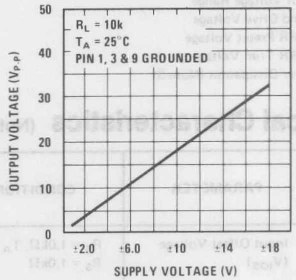
Supply Current vs Temperature



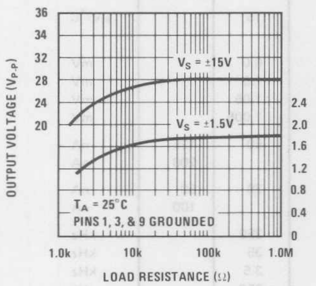
Supply Current vs Supply Voltage



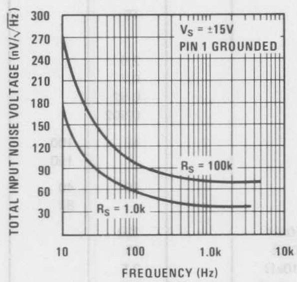
Output Voltage Swing vs Supply Voltage



Peak to Peak Output Voltage Swing vs R_L

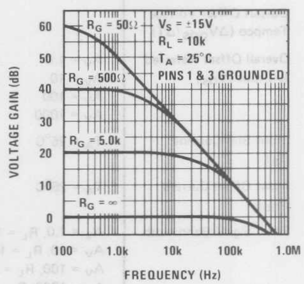


Total Input Noise Voltage* vs Frequency

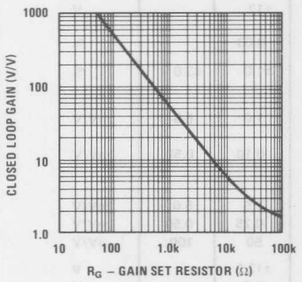


*Noise voltage includes contribution from source resistance

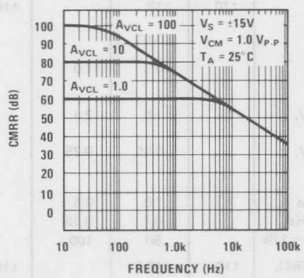
Closed Loop Voltage Gain vs Frequency



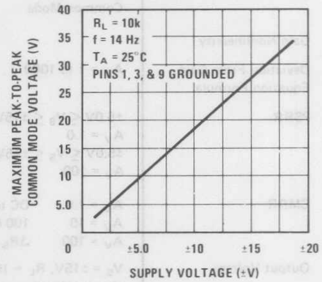
Closed Loop Voltage Gain



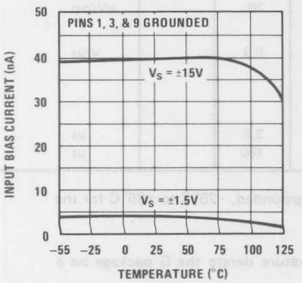
CMRR vs Frequency



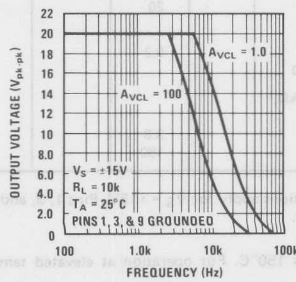
Common Mode Voltage vs Supply Voltage



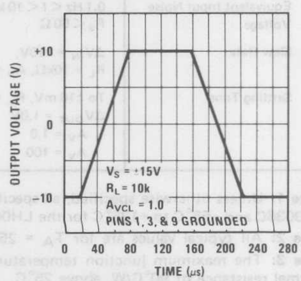
Input Bias Current



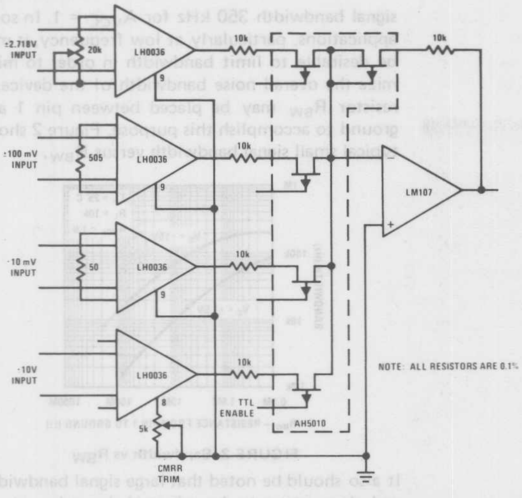
Output Voltage Swing vs Frequency



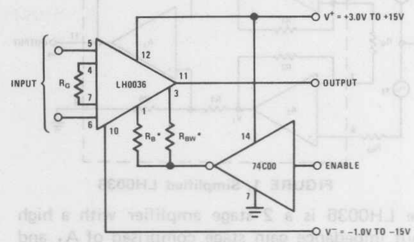
Large Signal Pulse Response



Typical Applications

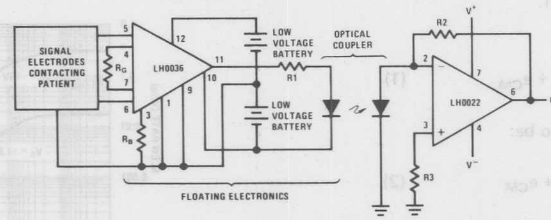


Pre MUX Signal Conditioning

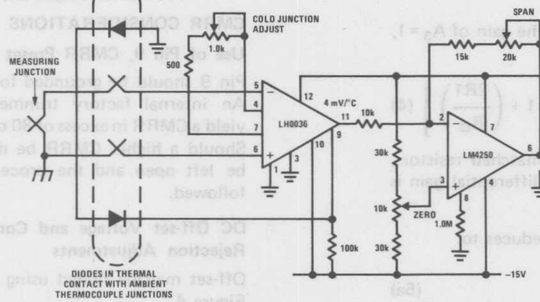


*R_BW AND R_B ARE OPTIONAL BANDWIDTH AND INPUT BIAS CURRENT CONTROLLING RESISTORS.

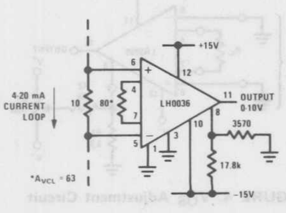
Instrumentation Amplifier with Logic Controlled Shut-Down



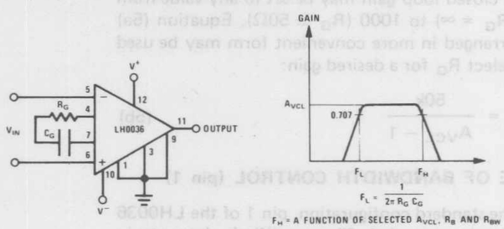
Isolation Amplifier for Medical Telemetry



Thermocouple Amplifier with Cold Junction Compensation



Process Control Interface



High Pass Filter

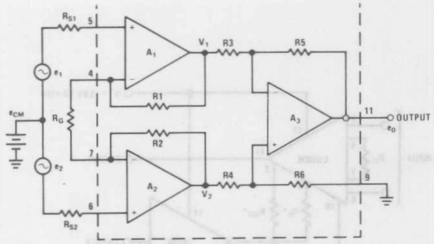


FIGURE 1. Simplified LH0036

The LH0036 is a 2 stage amplifier with a high input impedance gain stage comprised of A_1 and A_2 and a differential to single-ended unity gain stage, A_3. Operational amplifier, A_1, receives differential input signal, e_1, and amplifies it by a factor equal to $(R1 + R_G)/R_G$.

A_1 also receives input e_2 via A_2 and R2. e_2 is seen as an inverting signal with a gain of $R1/R_G$. A_1 also receives the common mode signal e_{CM} and processes it with a gain of +1.
Hence:

$$V_1 = \frac{R1 + R_G}{R_G} e_1 - \frac{R1}{R_G} e_2 + e_{CM} \qquad (1)$$

By similar analysis V_2 is seen to be:

$$V_2 = \frac{R2 + R_G}{R_G} e_2 - \frac{R2}{R_G} e_1 + e_{CM} \qquad (2)$$

For R1 = R2:

$$V_2 - V_1 = \left[\left(\frac{2R1}{R_G}\right) + 1\right](e_2 - e_1) \qquad (3)$$

Also, for R3 = R5 = R4 = R6, the gain of $A_3 = 1$, and:

$$e_0 = (1)(V_2 - V_1) = (e_2 - e_1)\left[1 + \left(\frac{2R1}{R_G}\right)\right] \qquad (4)$$

As can be seen for identically matched resistors, e_{CM} is cancelled out, and the differential gain is dictated by equation (4).

For the LH0036, equation (4) reduces to:

$$A_{VCL} = \frac{e_0}{e_2 - e_1} = 1 + \frac{50k}{R_G} \qquad (5a)$$

The closed loop gain may be set to any value from 1 ($R_G = \infty$) to 1000 ($R_G \cong 50\Omega$). Equation (5a) re-arranged in more convenient form may be used to select R_G for a desired gain:

$$R_G = \frac{50k}{A_{VCL} - 1} \qquad (5b)$$

USE OF BANDWIDTH CONTROL (pin 1)

In the standard configuration, pin 1 of the LH0036 is simply grounded. The amplifier's slew rate in this configuration is typically 0.3V/μs and small applications, particularly at low frequency, it may be desirable to limit bandwidth in order to minimize the overall noise bandwidth of the device. A resistor R_{BW} may be placed between pin 1 and ground to accomplish this purpose. Figure 2 shows typical small signal bandwidth versus R_{BW}.

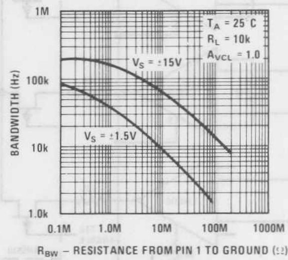


FIGURE 2. Bandwidth vs R_{BW}

It also should be noted that large signal bandwidth and slew rate may be adjusted down by use of R_{BW}. Figure 3 is plot of slew rate versus R_{BW}.

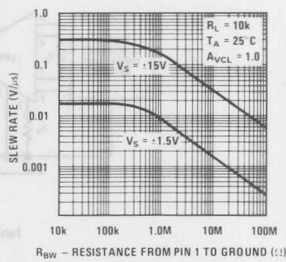


FIGURE 3. Output Slew Rate vs R_{BW}

CMRR CONSIDERATIONS

Use of Pin 9, CMRR Preset

Pin 9 should be grounded for nominal operation. An internal factory trimmed resistor, R6, will yield a CMRR in excess of 80 dB (for A_{VCL} = 100). Should a higher CMRR be desired, pin 9 should be left open and the procedure, in this section followed.

DC Off-set Voltage and Common Mode Rejection Adjustments

Off-set may be nulled using the circuit shown in Figure 4.

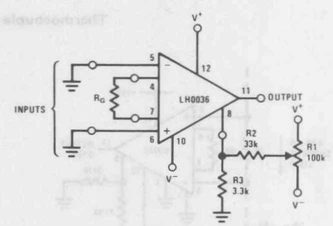


FIGURE 4. V_{OS} Adjustment Circuit

Pin 8 is also used to improve the common mode rejection ratio as shown in Figure 5. Null is

Applications Information (Cont'd)

achieved by alternately applying ±10V (for V^+ & V^- = 15V) to the inputs and adjusting R1 for minimum change at the output.

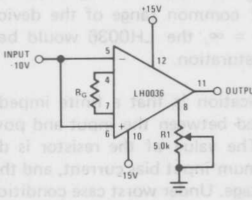


FIGURE 5. CMRR Adjustment Circuit

The circuits of Figure 4 and 5 may be combined as shown in Figure 6 to accomplish both V_{OS} and CMRR null. However, the V_{OS} and CMRR adjustment are interactive and several iterations are required. The procedure for null should start with the inputs grounded.

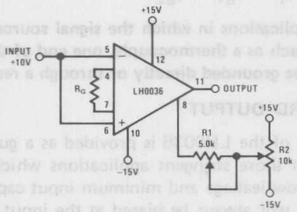
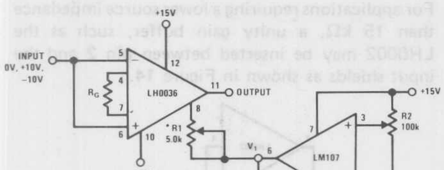


FIGURE 6. Combined CMRR, V_{OS} Adjustment Circuit

R2 is adjusted for V_{OS} null. An input of +10V is then applied and R1 is adjusted for CMRR null. The procedure is then repeated until the optimum is achieved.

A circuit which overcomes adjustment interaction is shown in Figure 7. In this case, R2 is adjusted first for output null of the LH0036. R1 is then adjusted for output null with +10V input. It is always a good idea to check CMRR null with a −10V input. The optimum null achievable will yield the highest CMRR over the amplifiers common mode range.



* NOTE: NOMINAL VALUE R1 TO ACHIEVE OPTIMUM CMRR IS 3.0 kΩ.

FIGURE 7. Improved V_{OS}, CMRR Nulling Circuit

AC CMRR Considerations

The ac CMRR may be improved using the circuit of Figure 8.

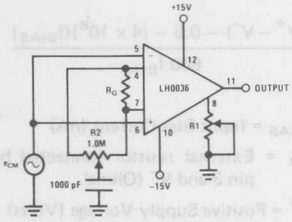


FIGURE 8. Improved AC CMRR Circuit

After adjusting R1 for best dc CMRR as before, R2 should be adjusted for minimum peak-to-peak voltage at the output while applying an ac common mode signal of the maximum amplitude and frequency of interest.

INPUT BIAS CURRENT CONTROL

Under nominal operating conditions (pin 3 grounded), the LH0036 requires input currents of 40 nA. The input current may be reduced by inserting a resistor (R_B) between 3 and ground or, alternatively, between 3 and V^-. For R_B returned to ground, the input bias current may be predicted by:

$$I_{BIAS} \cong \frac{V^+ - 0.5}{4 \times 10^8 + 800\, R_B} \qquad (6a)$$

or

$$R_B = \frac{V^+ - 0.5 - (4 \times 10^8)\,(I_{BIAS})}{800\, I_{BIAS}} \qquad (6b)$$

Where:

I_{BIAS} = Input Bias Current (nA)

R_B = External Resistor connected between pin 3 and ground (Ohms)

V^+ = Positive Supply Voltage (Volts)

Figure 9 is a plot of input bias current versus R_B.

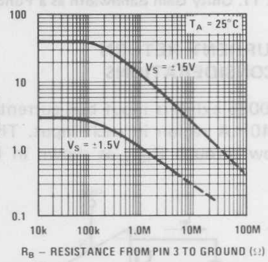


FIGURE 9. Input Bias Current as a Function of R_B

As indicated above, R_B may be returned to the negative supply voltage. Input bias current may then be predicted by:

$$I_{BIAS} \cong \frac{(V^+ - V^-) - 0.5}{4 \times 10^8 + 800 \cdot R_B}$$

Applications Information (Cont'd)

or

$$R_B \cong \frac{(V^+ - V^-) - 0.5 - (4 \times 10^8)(I_{BIAS})}{800\ I_{BIAS}} \qquad (8)$$

Where:

I_{BIAS} = Input Bias Current (nA)

R_B = External resistor connected between pin 3 and V^- (Ohms)

V^+ = Positive Supply Voltage (Volts)

V^- = Negative Supply Voltage (Volts)

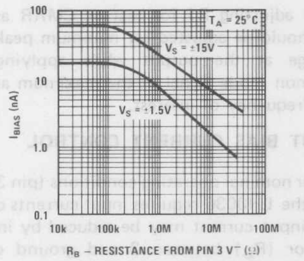


FIGURE 10. Input Bias Current as a Function of R_B

Figure 10 is a plot of input bias current versus R_B returned to V^- it should be noted that bandwidth is affected by changes in R_B. Figure 11 is a plot of bandwidth versus R_B.

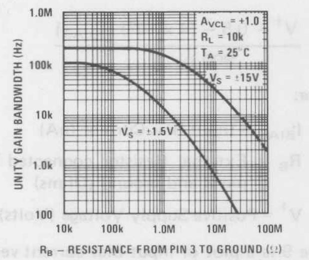


FIGURE 11. Unity Gain Bandwidth as a Function of R_B

BIAS CURRENT RETURN PATH CONSIDERATIONS

The LH0036 exhibits input bias currents typically in the 40 nA region in each input. This current must flow through R_{ISO} as shown in Figure 12.

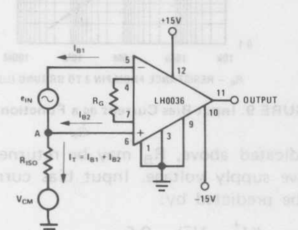


FIGURE 12. Bias Current Return Path

In a typical application, $V_S = \pm 15V$, $I_{B1} \cong I_{B2} \cong$ 40 nA, the total current, I_T, would flow through R_{ISO} causing a voltage rise at point A. For values of $R_{ISO} \geq 150\ M\Omega$, the voltage at point A exceeds the +12V common range of the device. Clearly, for $R_{ISO} = \infty$, the LH0036 would be driven to positive saturation.

The implication is that a finite impedance must be supplied between the input and power supply ground. The value of the resistor is dictated by the maximum input bias current, and the common mode voltage. Under worst case conditions:

$$R_{ISO} \leq \frac{V_{CMR} - V_{CM}}{I_T} \qquad (9)$$

Where:

V_{CMR} = Common Mode Range (10V for the LH0036)

V_{CM} = Common Mode Voltage

$I_T = I_{B1} + I_{B2}$

In applications in which the signal source is floating, such as a thermocouple, one end of the source may be grounded directly or through a resistor.

GUARD OUTPUT

Pin 2 of the LH0036 is provided as a guard drive pin in those stringent applications which require very low leakage and minimum input capacitance. Pin 2 will always be biased at the input common mode voltage. The source impedance looking into pin 2 is approximately 15 kΩ. Proper use of the guard/shield pin is shown in Figure 13.

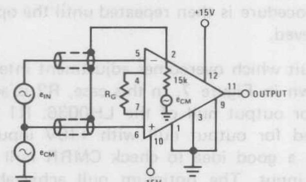


FIGURE 13. Use of Guard

For applications requiring a lower source impedance than 15 kΩ, a unity gain buffer, such as the LH0002 may be inserted between pin 2 and the input shields as shown in Figure 14.

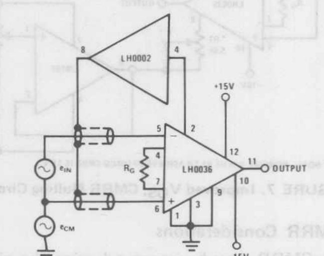


FIGURE 14. Guard Pin With Buffer

Definition of Terms

Bandwidth: The frequency at which the voltage gain is reduced to 0.707 of the low frequency (dc) value.

Closed Loop Gain, A_{VCL}: The ratio of the output voltage swing to the input voltage swing determined by $A_{VCL} = 1 + (50k/R_G)$. Where: R_G = Gain Set Resistor.

Common Mode Rejection Ratio: The ratio of input voltage range to the peak-to-peak change in offset voltage over this range.

Gain Equation Accuracy: The deviation of the actual closed loop gain from the predicted closed loop gain, $A_{VCL} = 1 + (50k/R_G)$ for the specified closed loop gain.

Input Bias Current: The current flowing at pin 5 and 6 under the specified operating conditions.

Input Offset Current: The difference between the input bias current at pins 5 and 6; i.e. $I_{OS} = |I_5 - I_6|$.

Input Stage Offset Voltage, V_{IOS}: The voltage which must be applied to the input pins to force the output to zero volts for $A_{VCL} = 100$.

Output Stage Offset Voltage, V_{OOS}: The voltage which must be applied to the input of the output stage to produce zero output voltage. It can be measured by measuring the overall offset at unity gain and subtracting V_{IOS}.

$$V_{OOS} = \left[V_{OS} \Big| A_{VCL} = 1 \right] - \left[V_{OS} \Big| A_{VCL} = 1000 \right]$$

Overall Offset Voltage:

$$V_{OS} = V_{IOS} + \frac{V_{OOS}}{A_{VCL}}$$

Power Supply Rejection Ratio: The ratio of the change in offset voltage, V_{OS}, to the change in supply voltage producing it.

Resistor, R_B: An optional resistor placed between pin 3 of the LH0036 and ground (or V^-) to reduce the input bias current.

Resistor, R_{BW}: An optional resistor placed between pin 1 of the LH0036 and ground (or V^-) to reduce the bandwidth of the output stage.

Resistor, R_G: A gain setting resistor connected between pins 4 and 7 of the LH0036 in order to program the gain from 1 to 1000.

Settling Time: The time between the initiation of an input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

LH0038/LH0038C True Instrumentation Amplifier

General Description

The LH0038/LH0038C is a precision true instrumentation amplifier (TIA) capable of amplifying very low level signals, such as thermocouple and low impedance strain guage outputs. Precision thin film gain setting resistors are included in the package to allow the user to set the closed-loop gain from 100 to 2000. Since the resistors are of a homogeneous single chip construction, they track almost perfectly so that temperature variations of closed loop gain are virtually eliminated.

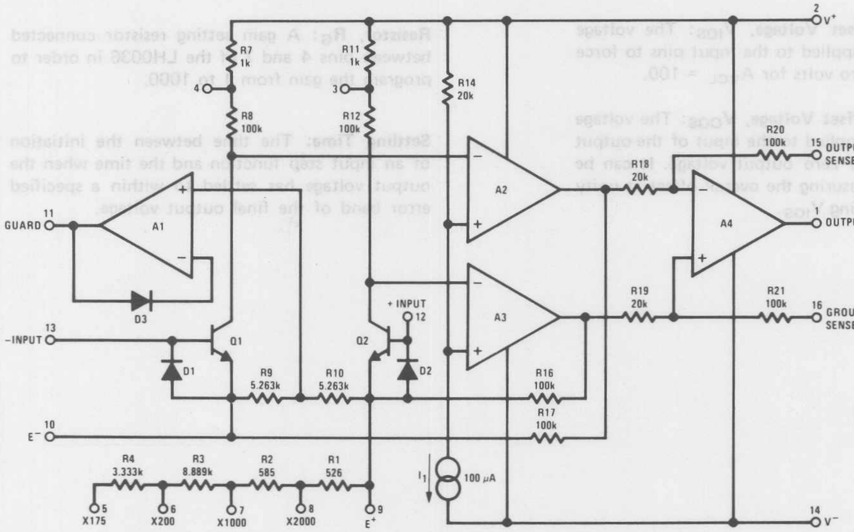
LH0038 exhibits excellent CMRR, PSRR, gain linearity, as well as extremely low input offset voltage, offset voltage drift and input noise voltage.

The devices are provided in a hermetically sealed 16-lead DIP. The LH0038 is guaranteed from −55°C to +125°C; whereas the LH0038C is guaranteed from −25°C to +85°C.

Features

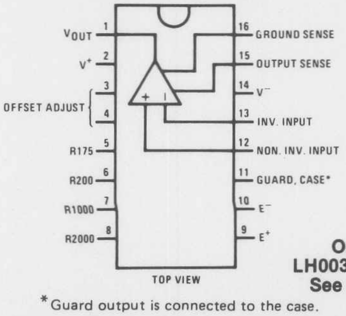
- Ultra-low offset voltage 25 μV typ., 100 μV max
- Ultra-low offset drift 0.25 μV/C max
- Ultra-low input noise 0.2 μVp-p
- Pin strap gain options 100, 200, 400, 500, 1k, 2k
- Excellent PSRR and CMRR 120 dB

Simplified Schematic Diagram



Connection Diagram

Dual-In-Line Package



Order Number
LH0038D or LH0038CD
See Package D16D

*Guard output is connected to the case.

Absolute Maximum Ratings

Supply Voltage	±18V
Differential Input Voltage (Note 1)	±1V
Input Voltage	$\pm V_S$
Power Dissipation (See Curve)	500 mW
Short Circuit Duration	Continuous
Operating Temperature Range	
LH0038	−55°C to +125°C
LH0038C	−25°C to +85°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 20 seconds)	300°C

DC Electrical Characteristics (Note 2)

PARAMETER		CONDITIONS		LH0038 MIN	LH0038 TYP	LH0038 MAX	LH0038C MIN	LH0038C TYP	LH0038C MAX	UNITS
V_{IOS}	Input Offset Voltage	$R_S = 50\Omega$, $V_{CM} = 0V$	$T_A = 25°C$		25	100		30	150	μV
						125			220	μV
$\Delta V_{IOS}/\Delta T$	Input Offset Voltage Tempco	$R_S = 50\Omega$, $V_{CM} = 0V$			0.1	0.25		0.2	1.0	μV/°C
V_{OOS}	Output Offset Voltage	$R_S = 50\Omega$, $V_{CM} = 0V$	$T_A = 25°C$		3	10		5	25	mV
						15			30	mV
$\Delta V_{OOS}/\Delta T$	Output Offset Voltage Tempco	$R_S = 50\Omega$, $V_{CM} = 0V$			25			25		μV/°C
I_B	Input Bias Current	$V_{CM} = 0V$	$T_A = 25°C$		50	100		50	100	nA
						200			200	nA
I_{OS}	Input Offset Current	$V_{CM} = 0V$	$T_A = 25°C$		2	5		7	10	nA
						8			15	nA
$\Delta I_B/\Delta T$	Input Bias Current Tempco	$V_{CM} = 0V$			500			500		pA/°C
A_{VCL}	Closed Loop Gain	Gain Pins Jumpered								V/V
		None			100			100		V/V
		6–10			200			200		V/V
		6–9, 10–5			400			400		V/V
		6–10, 5–9			500			500		V/V
		7–10			1000			1000		V/V
		8–10			2000			2000		V/V
	Closed Loop Gain Error	$A_{VCL} = 100, 200$			0.1	0.3		0.1	0.4	%
		$A_{VCL} = 400, 500$			0.2	0.3		0.2	0.6	%
		$A_{VCL} = 1000$			0.3	0.5		0.5	1.0	%
		$A_{VCL} = 2000$			1.0	2.0		1.5	3.0	%
	Gain Temperature Coefficient	$A_{VCL} = 1k$			7			7		ppm/°C
	Gain Nonlinearity	$100 \leq A_{VCL} \leq 2k$			1			1		ppm
V_{INCM}	Common-Mode Input Voltage Range			±10	±12		±10	±12		V
V_O	Output Voltage	$R_L \geq 10\ k\Omega$		±10	±12		±10	±12		V
V_S	Supply Voltage Range			±5		±18	±5		±18	
	Guard Voltage Error	$-10V < V_{CM} < +10V$			±10	±100		±10	±100	mV

DC Electrical Characteristics (Note 2) (Continued)

PARAMETER		CONDITIONS		LH0038 MIN	LH0038 TYP	LH0038 MAX	LH0038C MIN	LH0038C TYP	LH0038C MAX	UNITS
CMRR	Common-Mode Rejection Ratio	$V_{IN} = \pm 10V$	$A_{VCL} = 100$	94	110		86	110		dB
			$A_{VCL} = 1000$	114	120		106	110		dB
PSRR	Power Supply Rejection Ratio	$\pm 5V \le \Delta V_S \le \pm 15V$	$A_{VCL} = 100$	94	110		94	110		dB
			$A_{VCL} = 1000$	110	120		100	110		dB
I_{OSC}	Output Short Circuit Current	$T_A = 25°C$		±2	±5	±10	±2	±5	±10	mA
I_S	Supply Current	$T_A = 25°C$			1.6	2.0		1.6	3.0	mA
R_{IN} DIFF	Input Resistance	$A_{VCL} = 1000$, $T_A = 25°C$			5			5		MΩ
R_{IN} CM	Common-Mode Input Resistance				1			1		GΩ
R_{OUT}	Output Resistance				1			1		mΩ

AC Electrical Characteristics $V_S = \pm 15V$, $T_A = 25°C$

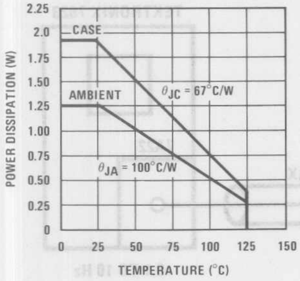
PARAMETER		COMMENT	CONDITIONS		TYP	UNITS
e_n	Equivalent Input Noise Voltage	*Figure 1*	$R_S = 0$, f = 0.1 to 10 Hz		0.2	μVp-p
$\overline{e_n}$	Equivalent Input Spot Noise Voltage	*Figure 1*	$R_S = 100\Omega$	f = 10 Hz	6.5	$nV/\sqrt{Hz}$
				f = 100 Hz	6.0	$nV/\sqrt{Hz}$
				f = 1 kHz	6.0	$nV/\sqrt{Hz}$
				f = 10 kHz	6.0	$nV/\sqrt{Hz}$
BW	Large Signal Bandwidth		$V_{OUT} = \pm 10V$		1.6	kHz
S_r	Slew Rate		$V_{OUT} = \pm 10V$		0.3	V/μs
t_s	Settling Time to 0.01%	*Figure 13*		20V Step	120	μs
				−10V Step	80	μs
				+10V Step	60	μs
t_r	Rise Time		$\Delta V_{OUT} = 100$ mV	$A_{VCL} = 100$	6	μs
				$A_{VCL} = 1000$	13	μs
$\overline{i_n}$	Equivalent Input Spot Noise Current		$R_S = 100$ MΩ	f = 10 Hz	0.1	$pA/\sqrt{Hz}$

Note 1: The inputs are protected by diodes for overvoltage protection. Excessive currents will flow for differential voltages in excess of ±1V. Input current should be limited to less than 10 mA.

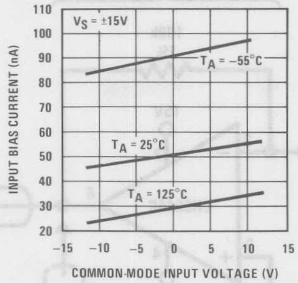
Note 2: Unless otherwise noted these specifications apply for $V_S = \pm 15.0V$, pin 15 connected to pin 1, pin 16 connected to ground, over the temperature range −55°C to +125°C for the LH0038 and −25°C to +85°C for LH0038C.

Typical Performance Characteristics

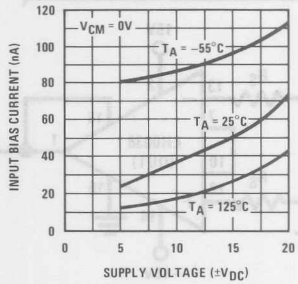
Power Dissipation



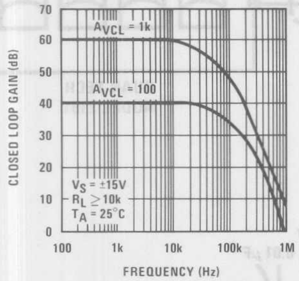
Input Bias Current



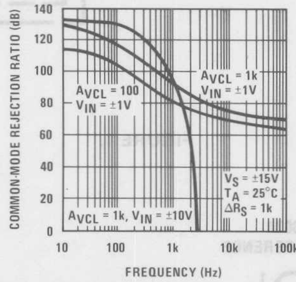
Input Bias Current



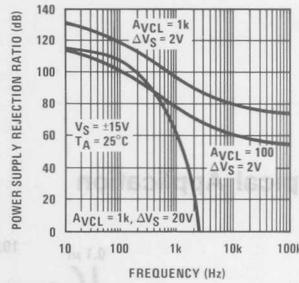
Closed Loop Frequency Response



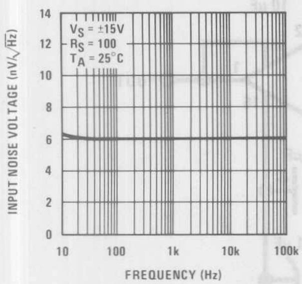
Common-Mode Rejection



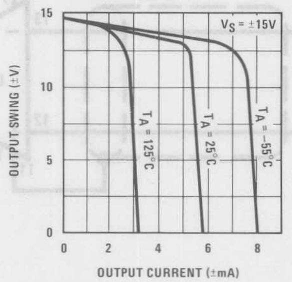
Power Supply Rejection



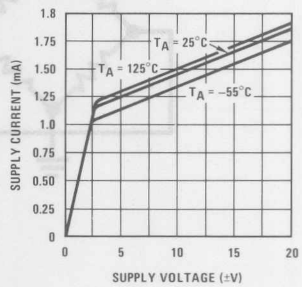
Input Noise Voltage (Includes Source Impedance)



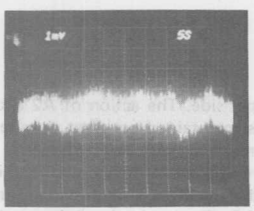
Output Swing



Supply Current

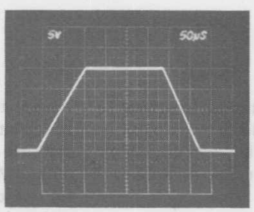


Wide Band Noise



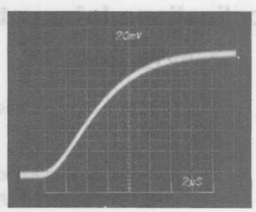
V_S = ±15V, R_S = 1kΩ, A_V = 10k, DUT = 1k
Vertical sensitivity: 0.1 μV/CM
Horizontal sensitivity: 5 sec/CM
Bandwidth: 0.1 Hz to 10 Hz

Pulse Response



V_S = ±15V
$R_L \geq$ 10kΩ
A_{VCL} = 1k

Rise Time



V_S = ±15V
$R_L \geq$ 10kΩ
A_{VCL} = 1k

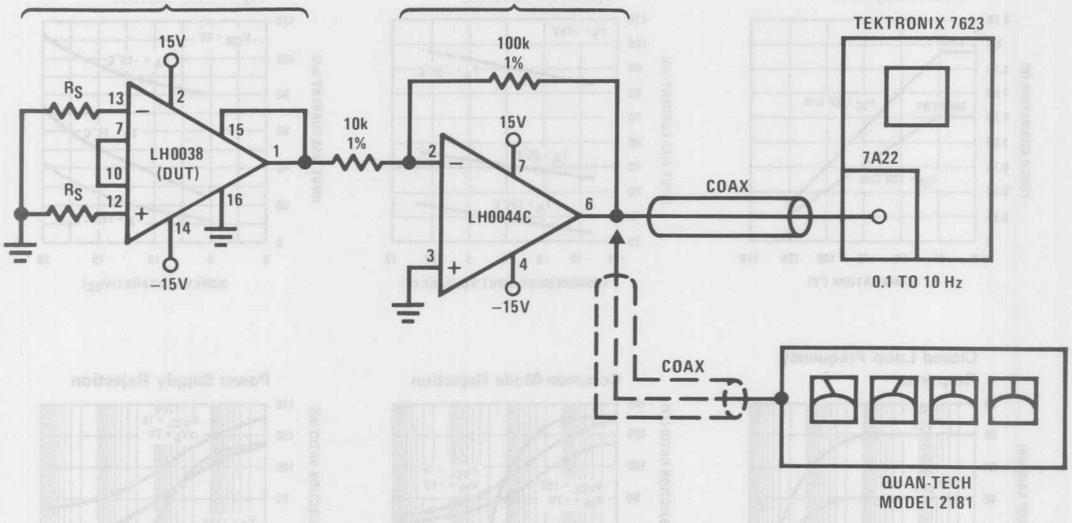


FIGURE 1.

Typical Application

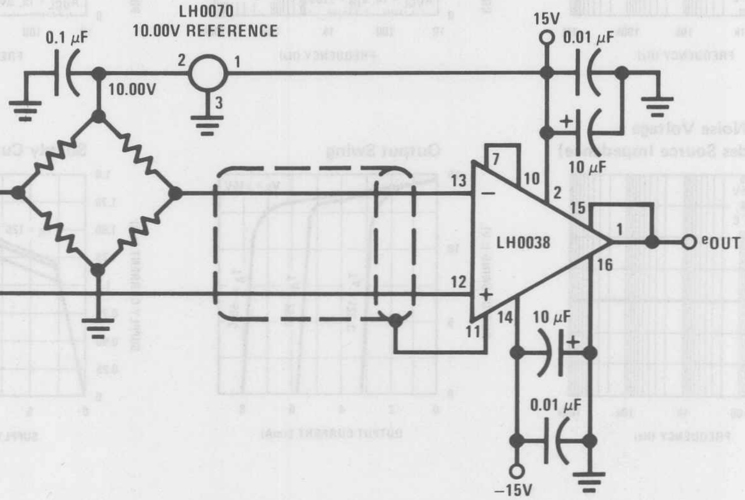


FIGURE 2. X1000 Bridge Amplifier

Applications Information

THEORY OF OPERATION

The LH0038 is a 3-stage, true instrumentation amplifier composed of a well matched transistor differential pair, Q1 and Q2, a common-mode loop amplifier, A2 and A3, and a differential to single ended amplifier, A4. A simplified schematic is shown in *Figure 3.*

Current source, I_A, establishes a voltage across R14 of approximately 2V, which results in a 2V drop across R8 and R12. This constant voltage forces the first stage current to be 20 μA per side. The action of A2 and A3 is such that 20 μA is maintained constant despite the presence of common-mode signals. The differential outputs of A2 and A3 are applied to differential amplifier, A4, which converts the signal to a single-ended output and provides a gain of 5. The total gain of the amplifier is, therefore, the fixed gain of 5 multiplied by the gain of the composite input stage.

Applications Information (Continued)

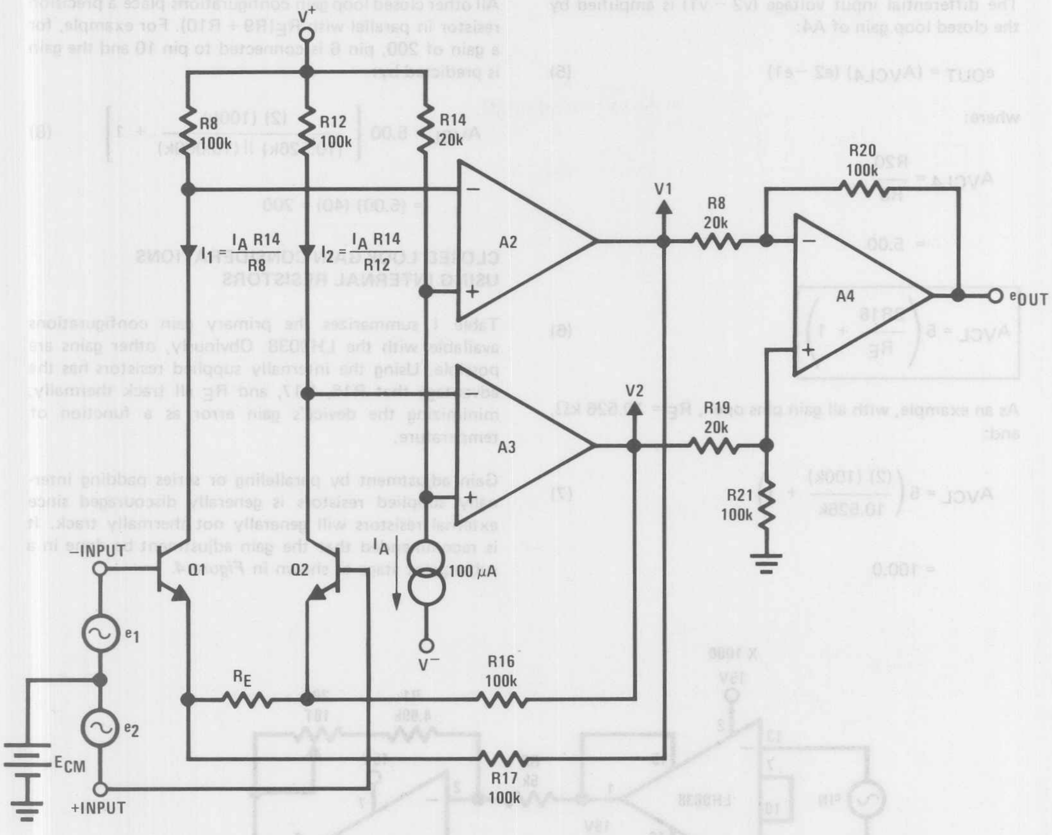


FIGURE 3. LH0038 Simplified Schematic

The closed loop gain of the composite amplifier may be better understood by referring to *Figure 3*. The Q1–A2 loop may be viewed as differential amplifier with the inverting input at the base and non-inverting input at the emitter. Combining small signal AC and large signal DC analysis =

$$v1 = e1\left(\frac{R17 + R_E}{R_E}\right) - e2\left(\frac{R17}{R_E}\right) \tag{1}$$

$$+ E_{CM} - V_{BE1} - I_1 R17$$

By similar analysis:

$$v2 = e2\left(\frac{R16 + R_E}{R_E}\right) - e1\left(\frac{R16}{R_E}\right) \tag{2}$$

$$+ E_{CM} - V_{BE2} - I_2 R16$$

For $I_1 \equiv I_2$, $R17 \equiv R16$, $V_{BE1} \equiv V_{BE2}$, subtracting equation (1) from (2) results in:

$$v2 - v1 = (e2 - e1)\left(\frac{R16 + R_E}{R_E}\right) \tag{3}$$

$$+ (e2 - e1)\left(\frac{R16}{R_E}\right)$$

$$\frac{v2 - v1}{e2 - e1} = \frac{2\,R16}{R_E} + 1 \tag{4}$$

Applications Information (Continued)

The differential input voltage (v2 − v1) is amplified by the closed loop gain of A4:

$$e_{OUT} = (A_{VCL4})\,(e2 - e1) \tag{5}$$

where:

$$A_{VCL4} = \frac{R20}{R8}$$

$$= 5.00$$

$$\boxed{A_{VCL} = 5\left(\frac{2R16}{R_E} + 1\right)} \tag{6}$$

As an example, with all gain pins open, $R_E = 10.526\ k\Omega$, and:

$$A_{VCL} = 5\left(\frac{(2)\,(100k)}{10.526k} + 1\right) \tag{7}$$

$$= 100.0$$

All other closed loop gain configurations place a precision resistor in parallel with R_E(R9 + R10). For example, for a gain of 200, pin 6 is connected to pin 10 and the gain is predicted by:

$$A_{VCL} = 5.00\left[\frac{(2)\,(100k)}{(10.526k)\,\|\,(10.000k)} + 1\right] \tag{8}$$

$$= (5.00)\,(40) = 200$$

CLOSED LOOP GAIN CONSIDERATIONS USING INTERNAL RESISTORS

Table I summarizes the primary gain configurations available with the LH0038. Obviously, other gains are possible. Using the internally supplied resistors has the advantage that R16, R17, and R_E all track thermally, minimizing the device's gain error as a function of temperature.

Gain adjustment by paralleling or series padding internally supplied resistors is generally discouraged since external resistors will generally not thermally track. It is recommended that the gain adjustment be done in a subsequent stage as shown in *Figure 4*.

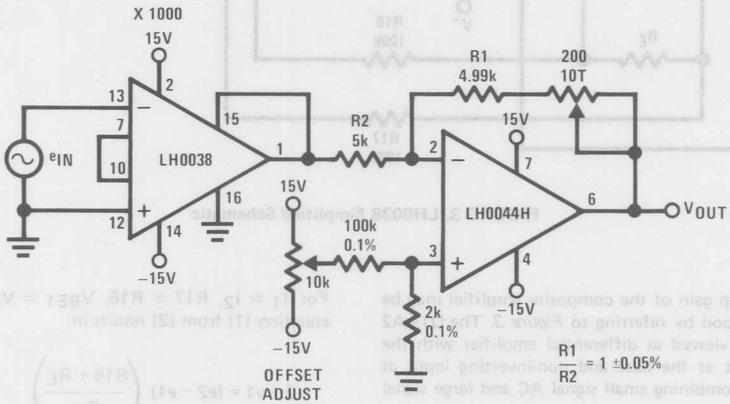


FIGURE 4. Recommended Gain Adjust Circuit

TABLE I. LH0038 INTERNAL GAIN CONFIGURATIONS

OVERALL GAIN	FIRST STAGE GAIN	PIN CONNECTIONS	EFFECTIVE R_E
100	20	All Gain Pins Open	10.5260 kΩ
200	40	Pin 6 to Pin 10	5.1281 kΩ
400	80	Pin 6 to Pin 9, Pin 10 to Pin 5	2.5316 kΩ
500	100	Pin 6 to Pin 10, Pin 9 to Pin 5	2.0202 kΩ
1000	200	Pin 7 to Pin 10	1.0050 kΩ
2000	400	Pin 8 to Pin 10	0.5013 kΩ

Applications Information (Continued)

GUARD DRIVE

The LH0038 is provided with a guard drive output, which will always be at the input common-mode voltage. The guard drive amplifier is short-circuit proof and is capable of driving several thousand pF without danger of latch-up or oscillation.

The guard drive tied to a shielded input cable will greatly reduce noise pick-up, and also improve AC CMRR by maintaining the shield at the common-mode voltage. *Figure 5* illustrates the proper use of the guard drive.

The guard drive output is also connected to the case to provide electrostatic shielding to the system.

REMOTE OUTPUT SENSE

The feedback network of the LH0038 may be closed directly at the load in order to eliminate errors due to lead resistance. Also, a unity gain buffer; e.g. LH0002, may be included within the feedback loop to increase output current capability as shown in *Figure 7.*

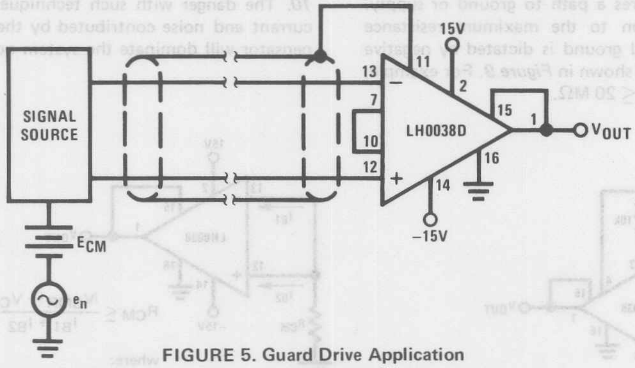


FIGURE 5. Guard Drive Application

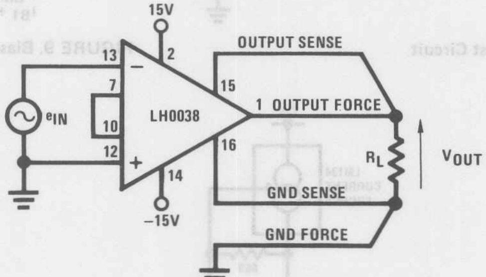


FIGURE 6. Remote Sense Connection

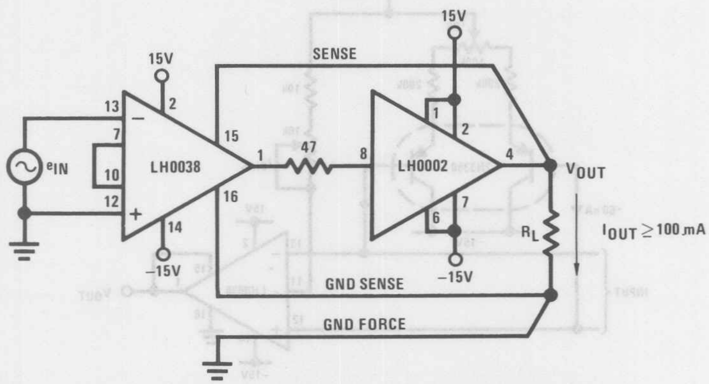


FIGURE 7. Output Buffer Connection

Offset of the LH0038 is trimmed by the factory to a very low value. The offset may be further trimmed using a 10 kΩ, 10 turn, 100 ppm/°C potentiometer as shown in *Figure 8.* However, a drift increase of 0.3 μV/°C will be caused for each 100 μV of offset adjusted. The recommended offset null is shown in *Figure 4* and is accomplished in the following stage.

BIAS CURRENT CONSIDERATIONS

The LH0038 exhibits bias current of approximately 50 nA per side, and requires a path to ground or supply. The practical limitation to the maximum resistance between the inputs and ground is dictated by negative common-mode range as shown in *Figure 9*. For example, for $V_{CM} = -10V$, $R_{CM} \leq 20\ M\Omega$.

The LH0038 input stage bias was optimized for minimum voltage noise so the input bias currents are higher than might otherwise be expected. Note, however, that the input currents are very well matched, resulting in an offset current value much lower than one might infer from the bias current. In order to take advantage of this low offset current, the source impedances at both inputs should be matched to minimize DC drift. Further, bias current is relatively constant with temperature (as opposed to an FET stage), so one can consider bias current compensation schemes such as shown in *Figure 10.* The danger with such techniques is that the offset current and noise contributed by the bias current compensator will dominate the system noise.

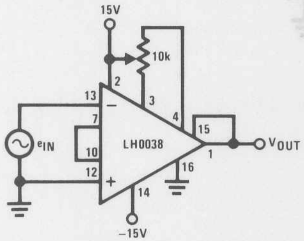
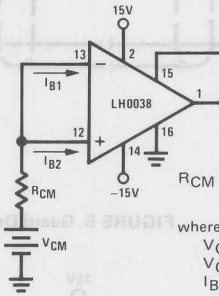


FIGURE 8. Offset Adjust Circuit (See also *Figure 4*)



$$R_{CM} \leq \frac{|V_{CMR}| - V_{CM}}{I_{B1} + I_{B2}}$$

where:
V_{CMR} = Common-Mode Range = ±12V
V_{CM} = Common-Mode Input Voltage
$I_{B1} + I_{B2}$ = Bias Current = 100 nA

FIGURE 9. Bias Current Return

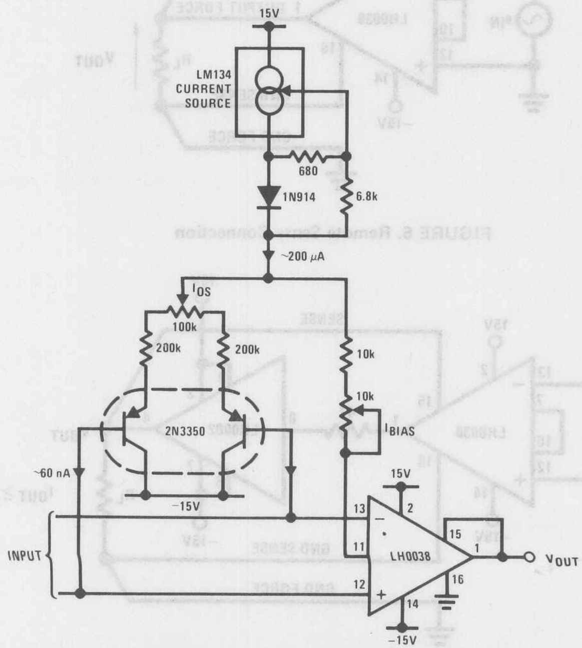


FIGURE 10. Bias Current Compensation

Applications Information (Continued)

SETTLING TIME

The LH0038 has been purposely over-compensated, and is therefore remarkably free from any undesirable transient response. Small signal settling time is governed by gain-bandwidth product; large signal settling time is dominated by slew rate.

Figure 11 shows an input voltage step of +10V to −10V applied, through a 1000 to 1 voltage divider, to the device configured for an inverting gain of 1000. The output of the device will therefore be equal to the negative of the input after the device is completely settled. By resistively subtracting the input before the divider from the device output, a pseudo summing node is generated. The voltage at this pseudo summing junction goes "off screen" on the photos, since in the first small time increment the input goes instantaneously to −10 mV and the output is still at +10V. About 130 µs after the input has gone negative, the output slews back in range and begins an exponential approach to the final value. *Figure 12* is the same set-up for a −10V to +10V input pulse. Note that there is no overshoot in either case. The test circuit is shown in *Figure 13*.

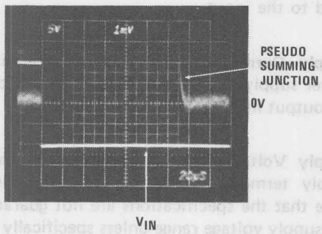
HIGH FREQUENCY CMRR

The LH0038 resistor ratios are carefully trimmed for optimum CMRR at DC through 60 Hz. Inevitably, this rejection will degrade at higher frequencies due to 2 separate effects: stray capacitance mismatch and slew rate limiting in the input stage. In most discrete instrumentation amplifier realizations, the stray capacitance mismatch dominates simply because the stray capacitances are relatively large (this can be trimmed out in a discrete amplifier). In a hybrid circuit such as the LH0038, stray capacitance is minimized, so the effects of mismatch are also minimized.

The response to a pulse or noise spike applied as a common-mode signal may be dominated by the slew characteristics of the input stage. Whenever the common-mode input slew rate exceeds 0.2 V/µs, the 2 input amplifiers will apply identical ramp signals to the final stage and cause its output to go to near 0V. Note that the amplifier is not really active under these conditions as normal mode signal variations will *not* be coupled to the output. Some time may be required for the amplifier to settle after a transient of this kind before the output can be considered representative of the input. Slew rate limiting will not normally be the limiting factor for sine wave common-mode signals as 0.2 V/µs corresponds to about 2 kHz (20 Vp-p).

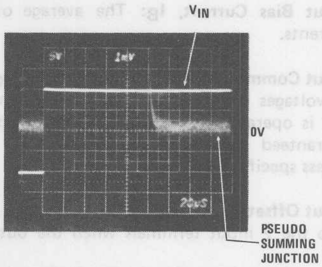
POWER SUPPLY DECOUPLING

Although the LH0038 exhibits in excess of 120 dB PSRR at DC, the figure degrades to 100 dB at 120 Hz. It is recommended that both V^+ and V^- leads be bypassed with 1 µF electrolytic in shunt with 0.01 µF ceramic disc no further than 1 inch from the device.



t_s, $A_V = 100$, $V_{IN} = -20V$

FIGURE 11. Settling Time



t_s, $A_V = 100$, $V_{IN} = 20V$

FIGURE 12. Settling Time

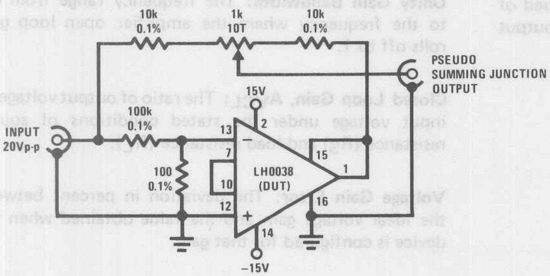


FIGURE 13. Settling Time Test Circuit

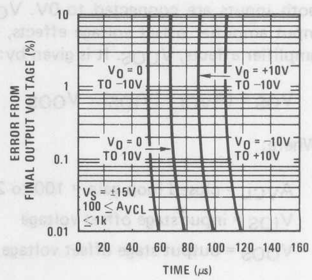


FIGURE 14. Settling Time

Definition of Terms

Bandwidth: That frequency at which the voltage gain is reduced to 3 dB below the low frequency value.

Common-Mode Rejection Ratio, CMRR: The ratio of the input common-mode voltage range to the peak-to-peak change in input offset voltage over this range.

Input Offset Voltage, V_{IOS}: The voltage which must be applied to the inputs to force the outputs of the input stage to 0V. V_{IOS} can be calculated by measuring V_{OS} at closed loop gains of 100 and 2000 and using the following equation:

$$V_{IOS} = \frac{(V_{OS})\ 2k - (V_{OS})\ 100}{1900}$$

Where:

$(V_{OS})2k$ = overall offset voltage for $A_{VCL} = 2k$.

$(V_{OS})100$ = overall offset voltage for $A_{VCL} = 100$.

Gain Non-Linearity: The deviation of the gain from a straight line drawn through the end points expressed as a percent of full-scale (10V for operations on ±15V supply). Note that this is a more stringent specification than deviation from the best straight line and is double the number that would be specified if the percentage were based on a 20V (±10V) range.

Guard Voltage Error: The voltage difference between the guard drive output and the average of the 2 input voltages.

Input Bias Current, I_B: The average of the 2 input currents.

Input Common-Mode Voltage Range, V_{INCM}: The range of voltages on the input terminals for which the amplifier is operational. Note that the specifications are not guaranteed over the full common-mode voltage range unless specifically stated.

Input Offset Current, I_{OS}: The difference in the currents into the 2 input terminals when the output is at zero.

Input Resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Overall Offset Voltage, V_{OS}: The output voltage when both inputs are connected to 0V. V_{OS} is composed of input amplifier offset voltage effects, V_{IOS}, and output amplifier effects, V_{OOS}. It is given by:

$$V_{OS} = (A_{VCL})\ (V_{IOS}) - V_{OOS}$$

Where:

A_{VCL} = closed loop gain = 100 to 2k

V_{IOS} = input stage offset voltage

V_{OOS} = output stage offset voltage

Output Offset Voltage, V_{OOS}: The output voltage when the outputs of the input stage are forced to 0V. V_{OOS} may be calculated by measuring V_{OS} at closed loop gains of 100 and 2000 and using the following equation:

$$V_{OOS} = \frac{(20)\ (V_{OS})\ 100 - (V_{OS})\ 2k}{19}$$

Where:

(V_{OS}) 100 = overall offset voltage for $A_{VCL} = 100$

(V_{OS}) 2k = overall offset voltage for A_{VCL}

Output Voltage, V_O: The peak output voltage swing, referred to zero.

Offset Voltage Temperature Drift, $\Delta V_{IOS}/\Delta T$: The average drift rate of offset voltage for a thermal variation from room temperature to the indicated temperature extreme.

Power Supply Rejection Ratio, PSRR: The ratio of the change in input offset voltage to the change in power supply voltages producing it.

Settling Times, t_s: The time between the initiation of the input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

Slew Rate, S_r: The internally-limited rate of change in output voltage with a large-amplitude step function applied to the input.

Supply Current, $\pm I_s$: The current required from the power supply to operate the amplifier with no load and the output midway between the supplies.

Supply Voltage Range: The range of voltages on the supply terminals for which the device is operational. Note that the specifications are not guaranteed over the full supply voltage range unless specifically stated.

Transient Response, t_r: The closed-loop step-function response of the amplifier under small-signal conditions.

Unity Gain Bandwidth: The frequency range from DC to the frequency where the amplifier open loop gain rolls off to 1.

Closed Loop Gain, A_{VCL}: The ratio of output voltage to input voltage under the stated conditions of source resistance (R_S) and load resistance (R_L).

Voltage Gain Error: The deviation in percent between the ideal voltage gain and the value obtained when the device is configured for that gain.

LH0084/LH0084C Digitally-Programmable-Gain Instrumentation Amplifier

General Description

The LH0084/LH0084C is a self-contained, high speed, high accuracy, digitally-programmable-gain instrumentation amplifier. It consists of paired FET-input variable-gain voltage-follower input stages followed by a differential-to-single-ended output stage. The input stage is programmable in accurate gain steps of 1, 2, 5, or 10 controlled by the logic levels of a 2-bit TTL-compatible digital input word. For additional flexibility, the output stage is pin-strappable to fixed gains of 1, 4, or 10 for an overall gain range of 1 to 100.

Applications include increased dynamic range A-to-D converters, test systems, and post multiplexer amplifier for data acquisition systems.

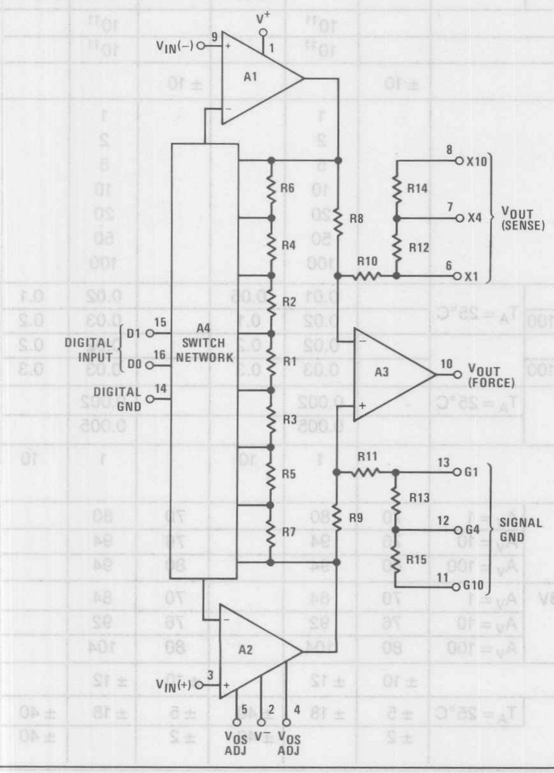
The device exhibits high input impedance, low offset voltage, high CMRR and PSRR, high speed, and excellent gain accuracy and gain non-linearity.

The LH0084 is guaranteed from −55°C to +125°C. The LH0084C is guaranteed from −25°C to +85°C. Both devices are provided in a hermetically sealed 16-lead dual-in-line metal package.

Features

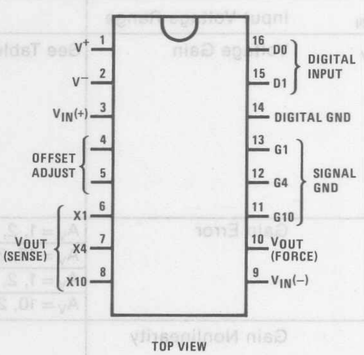
- Excellent gain accuracy — 0.05% max
- and low gain non-linearity — 0.01% typ
- Extremely low gain drift — 1 ppm/°C typ; 10 ppm/°C max
- High input impedance — $10^{11}\Omega$ typ
- High CMRR and PSRR — 70 dB min
- TTL compatible digital inputs
- High speed, settling to 0.1% — 4 μs max

Simplified Schematic



Connection Diagram

Dual-In-Line Package



Case is electrically isolated

Order Number LH0084D or LH0084CD
See NS Package D16D

Analog Input Voltage (Note 2)	±15V
Differential Input Voltage (Note 2)	±30V
Digital Input Voltage	−4V, +18V
Power Dissipation (See Curve)	2.5W
Operating Temperature Range	
LH0084	−55°C to +125°C
LH0084C	−25°C to +85°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 20 seconds)	+300°C

DC Electrical Characteristics $V_S = \pm 15V$, $R_L = 10\ k\Omega$, $T_{MIN} \le T_A \le T_{MAX}$ unless noted

	Parameter	Conditions		LH0084			LH0084C			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IOS}	Input Offset Voltage		$T_j = 25°C$		0.3	5		0.3	10	mV
						7			13	
$\Delta V_{IOS}/\Delta T$	Input Offset Voltage Change with Temperature	$R_S = 100\Omega$ $V_{CM} = 0$			10			10		μV/°C
V_{OOS}	Output Offset Voltage	(Note 3)	$T_j = 25°C$		0.6	5		0.6	10	mV
						7			13	
$\Delta V_{OOS}/\Delta T$	Output Offset Voltage Change with Temperature				20			20		μV/°C
I_B	Input Bias Current (Note 4)		$T_j = 25°C$		150	500		150	500	pA
						500			100	nA
I_{OS}	Input Offset Current		$T_j = 25°C$		50	200		50	200	pA
						200			50	nA
R_{IN}	Input Resistance	Differential			10^{11}			10^{11}		Ω
		Common-Mode			10^{11}			10^{11}		
V_{IN}	Input Voltage Range			±10			±10			V
A_V	Voltage Gain	See Table I			1			1		V/V
					2			2		
					5			5		
					10			10		
					20			20		
					50			50		
					100			100		
	Gain Error	$A_V = 1, 2, 5$	$T_A = 25°C$		0.01	0.05		0.02	0.1	%
		$A_V = 10, 20, 50, 100$			0.02	0.1		0.03	0.2	
		$A_V = 1, 2, 5$			0.02	0.2		0.02	0.2	
		$A_V = 10, 20, 50, 100$			0.03	0.3		0.03	0.3	
	Gain Nonlinearity		$T_A = 25°C$		0.002			0.002		
					0.005			0.005		
$\Delta A_V/\Delta T$	Gain Temperature Coefficient				1	10		1	10	ppm/°C
CMRR	Common-Mode Rejection Ratio	$V_{IN} = \pm 10V$	$A_V = 1$	70	80		70	80		dB
			$A_V = 10$	76	94		76	94		
			$A_V = 100$	80	94		80	94		
PSRR	Power Supply Rejection Ratio	$\pm 8V \le V_S \le \pm 18V$	$A_V = 1$	70	84		70	84		
			$A_V = 10$	76	92		76	92		
			$A_V = 100$	80	104		80	104		
V_O	Output Voltage Swing	$R_L \ge 10\ k\Omega$		±10	±12		±10	±12		V
I_C	Output Short-Circuit Current		$T_A = 25°C$	±5	±18	±40	±5	±18	±40	mA
				±2		±40	±2		±40	

DC Electrical Characteristics (Continued) $V_S = \pm 15V$, $R_L = 10\ k\Omega$, $T_{MIN} \le T_A \le T_{MAX}$ unless noted

	Parameter	Conditions	LH0084			LH0084C			Units
			Min	Typ	Max	Min	Typ	Max	
R_O	Output Resistance			0.05			0.05		Ω
V_{IL}	Digital "0" Input Voltage				0.7			0.7	V
V_{IH}	Digital "1" Input Voltage		2.0			2.0			V
I_{IL}	Digital "0" Input Current	$V_{IN} = 0.4V$		1.5	40		1.5	40	μA
I_{IH}	Digital "1" Input Current	$V_{IN} = 2.4V$		0.01			0.01		μA
V_S	Supply Voltage Range		±8		±18	±8		±18	V
$I_S(+)$	Positive Supply Current	$V_S \le \pm 18V$		12	18		12	26	mA
$I_S(-)$	Negative Supply Current	$V_S \le \pm 18V$		8	12		8	14	mA
P_D	Power Dissipation	$V_S = \pm 15V$		315	450		315	600	mW

AC Electrical Characteristics $V_S = \pm 15V$, $T_A = 25°C$, $R_L = 10\ k\Omega$

	Parameter	Conditions		Min	Typ	Max	Units
BW	Bandwidth (*Figure 1*)	Small Signal, −3 dB	$A_V = 1$		3250		kHz
			$A_V = 10$		500		kHz
			$A_V = 100$		350		kHz
		Small Signal, −1%	$A_V = 1$		300		kHz
			$A_V = 10$		75		kHz
			$A_V = 100$		55		kHz
PBW	Power Bandwidth	$V_o = \pm 10V$			200		kHz
SR	Slew Rate	$V_o = \pm 10V$		10	13		V/μs
t_S	Settling Time (*Figure 2*) ±0.1%	$\Delta V_o = \pm 20V$	$A_V = 1$		2.3	3.0	μs
			$A_V = 10$		2.7	3.5	μs
			$A_V = 100$		3.1	4.0	μs
	Gain Switching Time				3.5		μs
E_N	Equivalent Input Noise Voltage (*Figure 3*)	BW = 0.1 Hz-10 Hz	$A_V = 100$		7		μVp-p
		BW = 10 Hz-10 kHz	$A_V = 100$		1.4		μVrms
I_N	Equivalent Input Noise Current (*Figure 3*)	BW = 10 Hz-10 kHz	$A_V = 100$		30		pArms

Note 1: Improper supply power-on sequence may damage the device. See Power Supply Connection section under Applications Information.

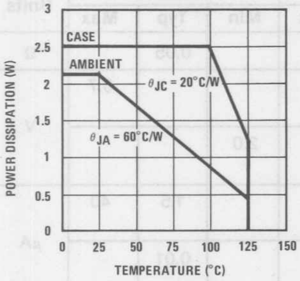
Note 2: For supply voltages less than ±15V the maximum input voltage is equal to the supply voltage.

Note 3: These parameters are specified at junction temperature, T_J. In normal operation the junction temperature rises above the ambient temperature, T_A, as a result of internal power dissipation, P_D. $T_J = T_A + \theta_{JA} P_D$ where θ_{JA} is the thermal resistance from junction to ambient.

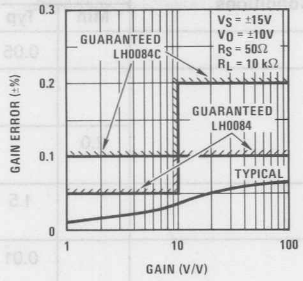
Note 4: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature.

Typical Performance Characteristics

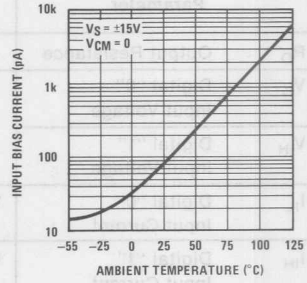
Power Dissipation



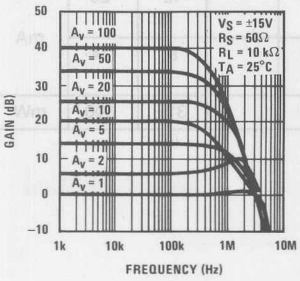
Gain Accuracy



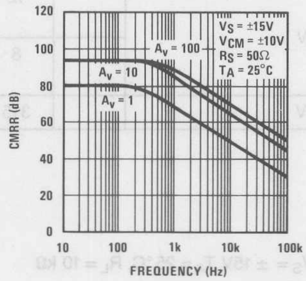
Input Bias Current



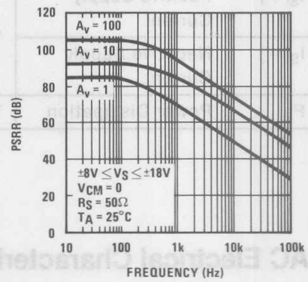
Small Signal Frequency Response



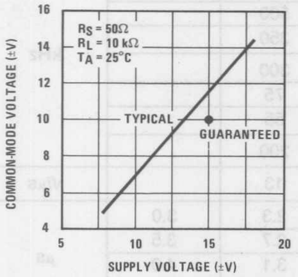
Common-Mode Rejection



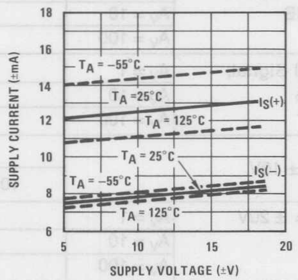
Power Supply Rejection



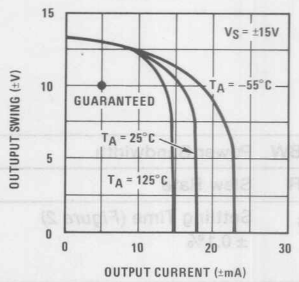
Input Common-Mode Range



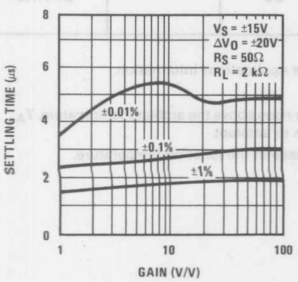
Supply Current



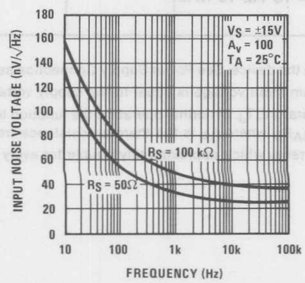
Output Swing



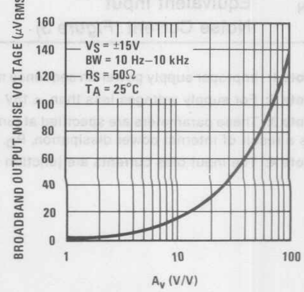
Settling Time



Equivalent Input Noise Voltage (Includes Source-Resistance Noise)



Broadband Output Noise Voltage



AC Test Circuits

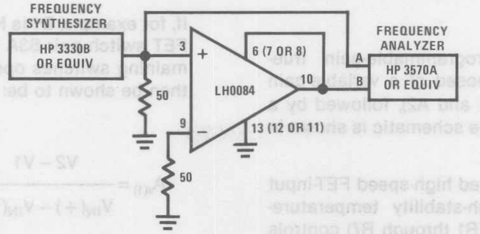


FIGURE 1. Frequency Response Measurement Circuit

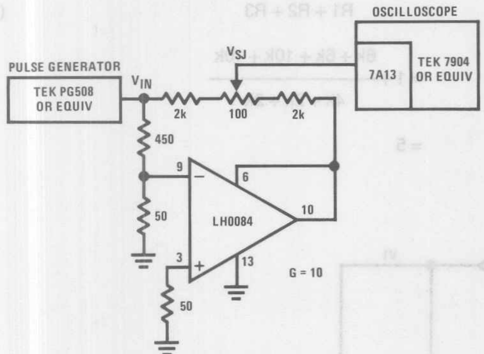
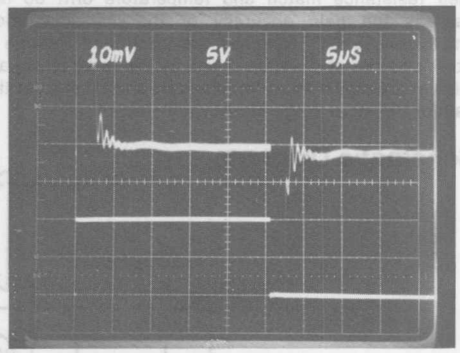


FIGURE 2. Settling Time Measurement Circuit

Settling Time



$A_V = 10$ Input Stage

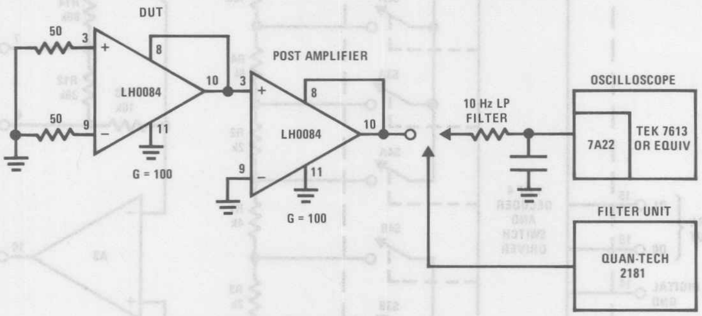
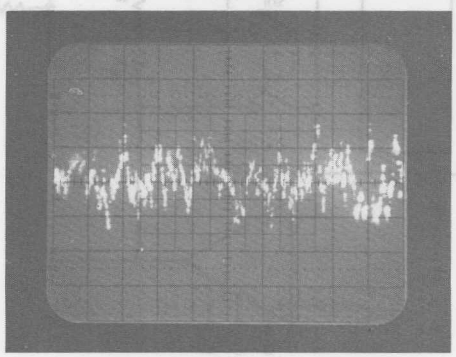


FIGURE 3. Noise Measurement Circuit

Wideband Noise



$R_S = 50\Omega$ Bandwidth 0.1 Hz to 10 Hz
1μV/Division Vertical 5 Seconds/Division Horizontal

instrumentation amplifier composed of a variable-gain voltage-follower input stage (A1 and A2), followed by a differential output stage (A3). The schematic is shown in *Figure 4*.

The input stage contains matched high-speed FET-input op amps (A1 and A2). A high-stability temperature-compensated resistor network (R1 through R7) controls feedback ratios at the inverting inputs of op amps A1 and A2 via FET switches S1A-S4A and S1B-S4B. Since the FET switches are in series with the op amp input impedance their resistance match and temperature drift do not degrade the gain accuracy of the instrumentation amplifier. The FET switches are controlled through a 1-of-4 decoder and switch driver, by the logic levels applied at the digital input terminals D1 and D0 and set the gain of the input stage as shown in Table I.

maining switches open). The input stage gain, $A_{V(1)}$, can then be shown to be:

$$A_{V(1)} = \frac{V2 - V1}{V_{IN}(+) - V_{IN}(-)}$$

$$= 1 + \frac{R4 + R5 + R6 + R7}{R1 + R2 + R3} \qquad (1)$$

$$= 1 + \frac{6k + 6k + 10k + 10k}{4k + 2k + 2k}$$

$$= 5$$

Schematic Diagram

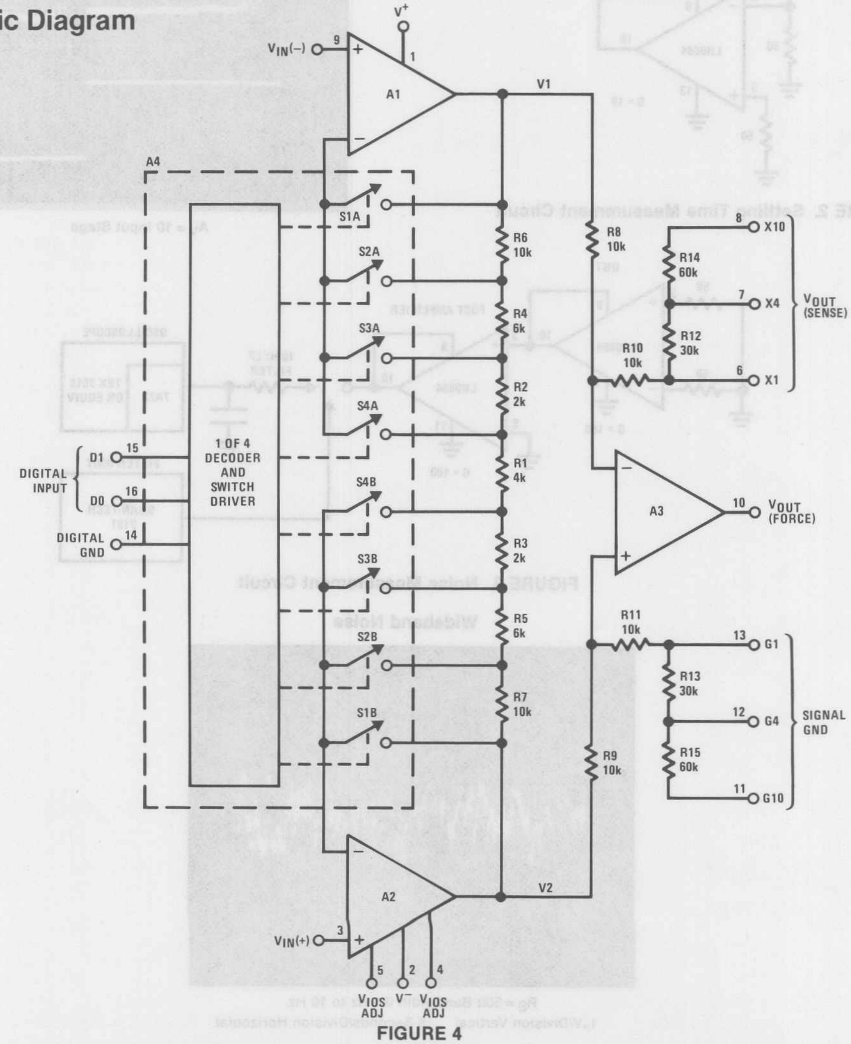


FIGURE 4

Applications Information (Continued)

TABLE I. GAIN TRUTH TABLE AND CONNECTION TABLE

Digital Inputs		1st Stage Gain	Pin Connections	2nd Stage Gain	Overall Gain
D1	D0	$A_{V(1)}$		$A_{V(2)}$	A_V
0	0	1	6-10, 13-GND	1	1
0	1	2			2
1	0	5			5
1	1	10			10
0	0	1	7-10, 12-GND	4	4
0	1	2			8
1	0	5			20
1	1	10			40
0	0	1	8-10, 11-GND	10	10
0	1	2			20
1	0	5			50
1	1	10			100

The output stage, consisting of op amp A3 and resistors R8 through R15, converts the voltage difference at the output of the input stage, V2 minus V1, to a single-ended output. For increased flexibility of the LH0084, the output stage gain is pin-strappable by selecting R10, R10 + R12, or R10 + R12 + R14 as feedback resistor for A3. The ratios of these resistors to the differential stage input resistor R3 are kept very accurate to maintain the excellent overall gain accuracy of the device. The output stage gain, $A_{V(2)}$, is equal to the feedback resistance divided by the input resistance. Thus with, for example, Pin 7 wired to Pin 10, that gain would be:

$$A_{V(2)} = \frac{V_{OUT}}{V2 - V1} = \frac{R10 + R12}{R8} = \frac{10k + 30k}{10k} = 4 \qquad (2)$$

To preserve the high common-mode rejection ratio of the output stage, the ground sense resistor, R11, R11 + R13 or R11 + R13 + R15, must match the feedback resistor used.

The overall gain of the LH0084 is therefore:

$$A_V = \frac{V_{OUT}}{V_{IN}(+) - V_{IN}(-)} = \frac{V2 - V1}{V_{IN}(+) - V_{IN}(-)} \cdot \frac{V_{OUT}}{V2 - V1} = A_{V(1)} \cdot A_{V(2)} \qquad (3)$$

The different gains available are in the range of 1 through 100 and are summarized in Table I.

POWER SUPPLY CONNECTIONS

Proper power supply connections are shown in *Figure 5*. The power supplies should be bypassed to ground as close as possible to device supply pins. For optimum high speed performance V^+ and V^- should be decoupled with a 0.01 μF ceramic disc in parallel with a 1 μF electrolytic capacitor.

The two ground pins, analog and digital grounds, should be connected together as close to the device as possible, preferably with a ground plane underneath the device. If this is not possible, the grounds should be connected together locally with back-to-back diodes and hard-wired together off-board. If a ground reference offset is used, it must be low impedance compared to the ground sense resistance to avoid CMRR degradation.

Care must be taken in the supply power-on sequence. The LH0084 may suffer irreversible damage if the V^+ supply is applied prior to the powering on of the V^- supply. In most applications using dual tracking supplies and with the device supply pins adequately bypassed, this will not present a problem. If this cannot be guaranteed, a germanium or Schottky protection diode should be connected between the digital ground pin and the V^- pin as shown in *Figure 5*.

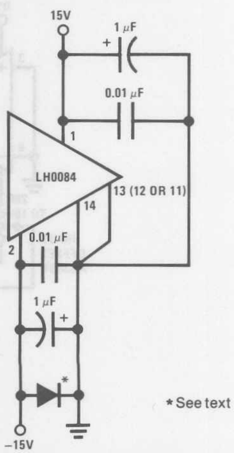


FIGURE 5. Power Supply Connections

Applications Information (Continued)

SIGNAL CONNECTIONS

The input signals should be connected as shown in *Figure 6.* To minimize errors, $R_S(+)$, $R_S(-)$ and R_{CM} should be kept as small as possible.

The output connections are also shown in *Figure 6.* The feedback leads should be kept short as should the ground sense in order to minimize lead resistance and parasitic capacitance.

OFFSET AND GAIN ADJUSTMENTS

Special care must be taken when using external offset adjustment. Since the LH0084 is a 2-stage amplifier with each stage contributing offset errors, and the amplifier presumably is used at several different gains, it is important to realize that the offsets of both the 1st and the 2nd stages must be nulled to maintain zero offset referred to output (RTO) at all gain settings.

In general, it is recommended that the input stage offset (V_{IOS}) be adjusted with a potentiometer as shown in *Figure 7.* The output stage offset (V_{OOS}) is ideally adjusted at a subsequent gain stage (i.e. sample-and-hold or A-to-D converter), but if this is impractical, it may also be done as shown in *Figure 7.*

Recommended offset adjust procedure is as follows: Initially set both pots to center positions and short both inputs of the LH0084 to ground.

a) Set the input stage gain to 1 (pull D1 and D0 low). Measure the output voltage, V_{OUT1}.

b) Set the input stage gain to 10 (pull D1 and D0 high). Measure the new output voltage, V_{OUT2}.

c) Calculate the portion of V_{OUT2} contributed by the output stage offset per the equation:

$$V_{OOS} = \frac{1}{9}(10 \cdot V_{OUT1} - V_{OUT2}) \qquad (4)$$

d) While maintaining an input stage gain of 10, adjust the input offset voltage (V_{IOS}) potentiometer until the output voltage is equal to the voltage calculated in Equation (4).

e) Change the input back to a gain of 1 and adjust the output offset voltage (V_{OOS}) potentiometer until the output voltage is zero.

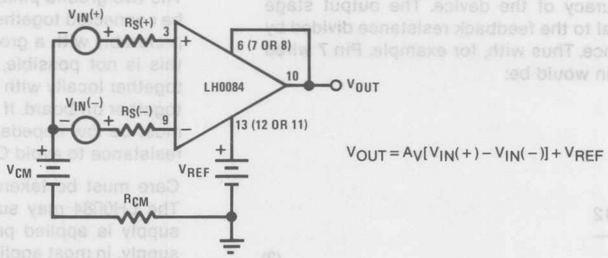


FIGURE 6. Signal Connections

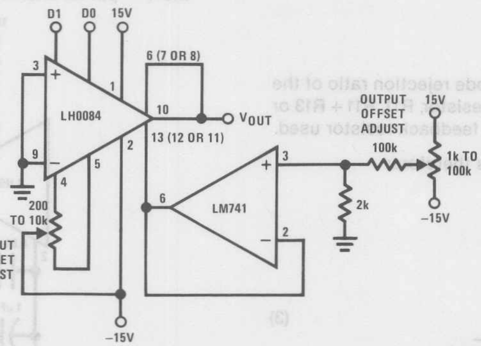


FIGURE 7. Offset Adjust Circuit

Applications Information (Continued)

An alternate offset adjust scheme is shown in *Figure 8*. The offset should be rezeroed after each time the gain is changed or when the op amp integrator drift warrants a new zero pulse. An additional advantage of this adjustment technique is that it can also be used to cancel out offset voltage drift and common-mode voltage error contributions.

External gain adjustment is generally discouraged since gain accuracy can be optimized for one gain setting only. If gain adjustment is required, however, it should be done at a subsequent gain stage.

LOGIC CONNECTIONS

The digital inputs D1 and D0 are referenced to the digital ground. The device interfaces directly to TTL and, with pull-down resistors, to CMOS.

Interfacing with microprocessors will usually require a latch. A circuit using full 6-bit wide address decode and write strobe is shown in *Figure 9*.

REMOTE OUTPUT SENSE

The feedback resistors of the LH0084 can be connected directly at the load in order to eliminate errors due to lead resistance (*Figure 10*).

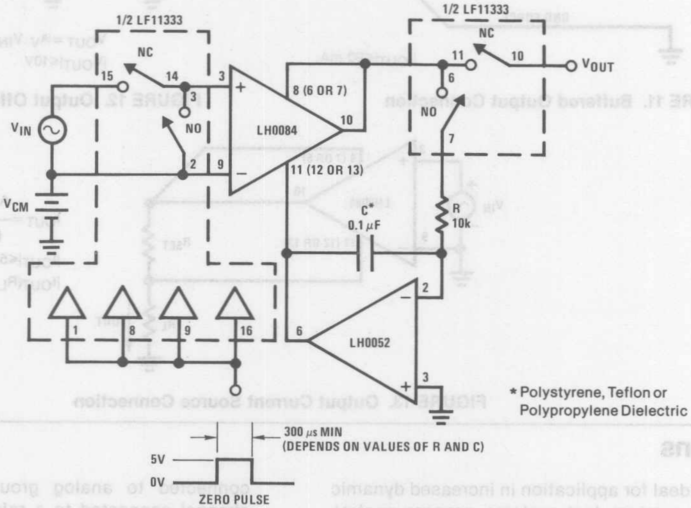


FIGURE 8. Auto Zero Circuit

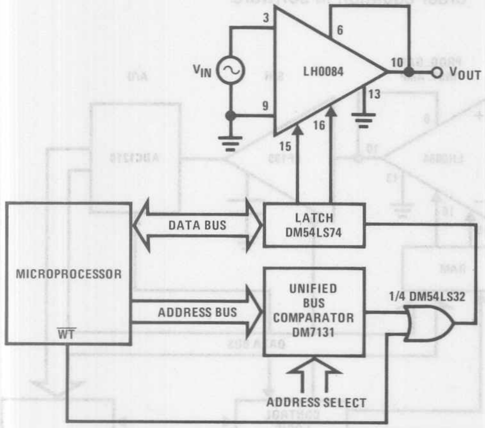


FIGURE 9. Typical Microprocessor Interface

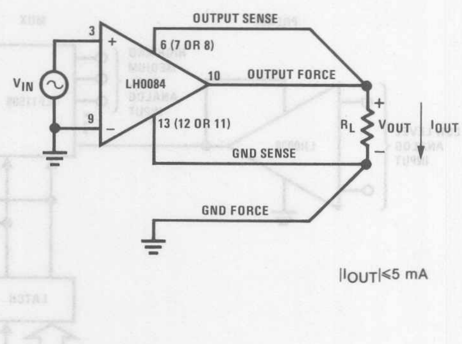
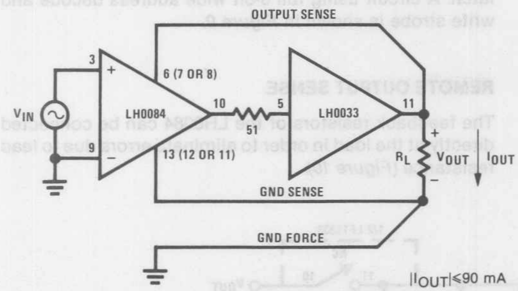


FIGURE 10. Remote Sense Connection

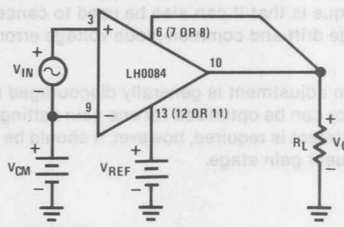
Also, a unity gain buffer, such as the LH0033, may be included in the feedback loop for increased current drive capability as shown in *Figure 11*.

The output sense feature can also be used in other ways such as output offset, *Figure 12*, or current source output, *Figure 13*.



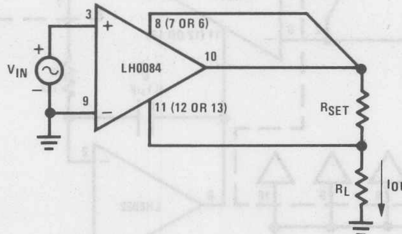
$|I_{OUT}| \leq 90$ mA

FIGURE 11. Buffered Output Connection



$V_{OUT} = A_V \cdot V_{IN} + V_{REF}$
$|V_{OUT}| \leq 10V$

FIGURE 12. Output Offset Connection



$$I_{OUT} = \frac{A_V \cdot V_{IN}}{R_{SET}}$$
$|I_{OUT}| \leq 5$ mA
$|I_{OUT}(R_L + R_{SET})| \leq 10V$

FIGURE 13. Output Current Source Connection

Applications

The LH0084 is ideal for application in increased dynamic range A-to-D converters, test systems, process control, and multi-channel data acquisition systems. *Figure 14* shows the device used in a typical data acquisition system.

A software offset and gain error correction scheme is shown in *Figure 15*. By first selecting a multiplexer input connected to analog ground, and then selecting a channel connected to a reference of known value, the overall system gain and offset errors can be calculated. For all subsequent readings, offset and gain corrections can be made mathematically by solving a simple first-order equation in software.

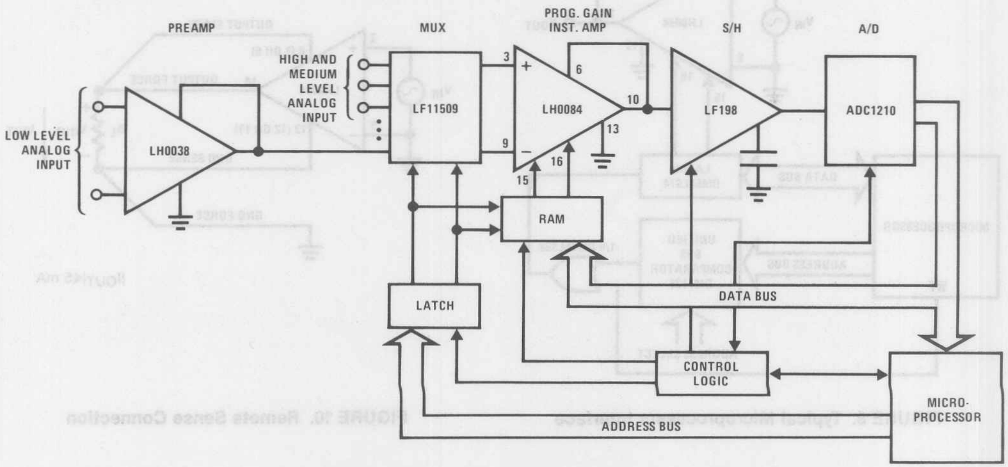


FIGURE 14. Typical Data Acquisition System

Applications (Continued)

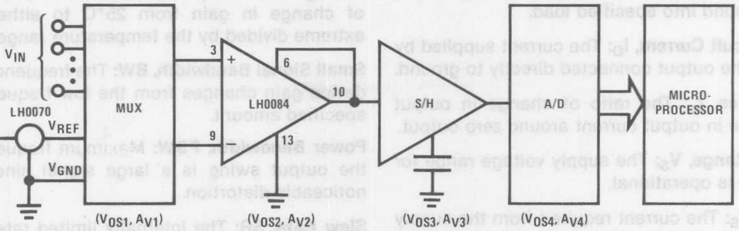


FIGURE 15. Software System Offset and Gain Calibration Circuit

Definition of Terms

Input Offset Voltage, V_{IOS}: The voltage which must be applied to the inputs to force the output of the input stage to 0V. V_{IOS} can be calculated by measuring V_{OS} (RTO) at input stage gains of 1 and 10 and using the following equation:

$$V_{IOS} = \frac{1}{9}\left(V_{OS}\Big|_{A_V=10} - V_{OS}\Big|_{A_V=1}\right)$$

where:

$$V_{OS}\Big|_{A_V=10} = \text{Overall offset (RTO) for } A_V = 10$$

$$V_{OS}\Big|_{A_V=1} = \text{Overall offset (RTO) for } A_V = 1$$

Input Offset Current, I_{OS}: The difference in the currents into the 2 analog input terminals at 0V.

Input Bias Current, I_B: The average of the currents into the 2 analog input terminals at 0V.

Input Resistance, R_{IN}: Common-mode input resistance is the change in input voltage range divided by the change in input bias current with both analog inputs at the same voltage. Differential input resistance is the change in input voltage at one input terminal divided by the change in input current at the other input terminal which is kept still at 0V.

Input Voltage Range, V_{IN}: The voltage range for which the device is operational.

Common-Mode Rejection Ratio, CMRR: The ratio of the input common-mode voltage range to the change in input offset voltage over this range.

Power Supply Rejection Ratio, PSRR: The ratio of the specified change in supply voltage to the change in input offset voltage over this range.

Voltage Gain, A_V: The ratio of output voltage change to the input voltage change producing it.

Gain Error: The deviation in percent between the ideal voltage gain and the value obtained when the device is configured for that gain.

Gain Non-Linearity: The deviation of the gain from a straight line drawn through the end-points expressed as a percent of full-scale (10V for operation with ±15V supply). For testing purposes it is the difference between positive swing gain (0V to 10V) and average gain (−10V to 10V) or between negative swing gain (0V to −10V) and average gain.

Output Stage Offset Voltage, V_{OOS}: The voltage which must be applied to the input of the output stage for the output to be forced to 0V. V_{OOS} can be calculated by measuring V_{OS} (RTO) at input stage gains of 1 and 10 and applying the following equation:

$$V_{OOS} = \frac{1}{9}\left(10 \cdot V_{OS}\Big|_{A_V=1} - V_{OS}\Big|_{A_V=10}\right)$$

where:

$$V_{OS}\Big|_{A_V=1} = \text{Overall offset (RTO) for } A_V = 1$$

$$V_{OS}\Big|_{A_V=10} = \text{Overall offset (RTO) for } A_V = 10$$

Offset Voltage (Referred to Output), $V_{OS(RTO)}$: The output voltage when both inputs are connected to 0V. V_{OS} is composed of input offset voltage, V_{IOS}, and output offset voltage, V_{OOS}, and is a function of amplifier gain. The overall offset voltage is given by:

$$V_{OS(RTO)} = A_{V(2)}(A_{V(1)}\, V_{IOS} + V_{OOS})$$

where:

V_{IOS} = Input offset voltage

V_{OOS} = Output stage offset voltage

$A_{V(1)}$ = Input stage gain

$A_{V(2)}$ = Output stage gain

Definition of Terms (Continued)

Output Voltage Swing, V_O: The peak output voltage swing referenced to ground into specified load.

Output Short-Circuit Current, I_O: The current supplied by the device with the output connected directly to ground.

Output Resistance, r_o: The ratio of change in output voltage to change in output current around zero output.

Supply Voltage Range, V_S: The supply voltage range for which the device is operational.

Supply Current, I_S: The current required from the supply to operate the device with zero load and with the analog as well as the digital inputs at 0V.

Power Dissipation, P_D: The power dissipated in the device with zero load and with the analog as well as the digital inputs at 0V.

Digital "1" Input Voltage, V_{IH}: Minimum voltage required at the digital input to guarantee a high logic state.

Digital "0" Input Voltage, V_{IL}: Maximum voltage required at the digital input to guarantee a low logic state.

Digital "1" Input Current, I_{IH}: The current into a digital input at specified logic level.

Digital "0" Input Current, I_{IL}: The current into a digital input at specified logic level.

Average Input Offset Voltage Drift, $\Delta V_{IOS}/\Delta T$: The ratio of input offset voltage change from 25°C to either temperature extreme divided by the temperature range.

Average Output Offset Voltage Drift, $\Delta V_{OOS}/\Delta T$: The ratio of output offset voltage change from 25°C to either temperature extreme divided by the temperature range.

Average Gain Temperature Coefficient, $\Delta A_V/\Delta T$: The ratio of change in gain from 25°C to either temperature extreme divided by the temperature range.

Small Signal Bandwidth, BW: The frequency at which the device gain changes from the low frequency gain by a specified amount.

Power Bandwidth, PBW: Maximum frequency for which the output swing is a large signal sinewave without noticeable distortion.

Slew Rate, SR: The internally limited rate of change in output voltage with a large amplitude step function applied at the input.

Settling Time, t_s: The time between the initiation of an input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

Gain Switching Time: The time between the initiation of a gain logic change and the time when the final gain switches are closed. It includes overdrive recovery time, but not settling to final value.

Equivalent Input Noise Voltage, E_N: The rms or peak noise voltage referred to the input (RTI) over a specified frequency band.

Equivalent Input Noise Current, I_N: The rms or peak noise current referred to the input (RTI) over a specified frequency band.

Section 5

Voltage Comparators

5

Section Contents

Voltage Comparator Guide

Device	Temperature Range*	DTL/TTL Fanout	Supply Voltage Typ (V)	Input Bias Current (25°C) Max (μA)	Input Offset Current (25°C) Max (μA)	Input Offset Voltage (25°C) Max (mV)	Response Time† Typ (ns)	Voltage Gain Typ	Package Type	Comments
LM106	Military	10	$V^+ = 12$	20	3	2	40 max	40k	TO-5	Single comparator with strobe, high speed and sensitivity, large fanout
LM206	Industrial	10	$V^- = -3$	20	3	2	40 max	40k	TO-5	
LM306	Commercial	10	To −12	25	5	5	40 max	40k	TO-5	
LF111	Military	2	36	0.05	0.000025	4	200	200k	TO-5	FET front-end inputs
LF211	Industrial	2	36	0.05	0.000025	4	200	200k	TO-5	
LF311	Commercial	2	36	0.15	0.000075	10	200	200k	TO-5	
LM111	Military	5	±15	0.1	0.04	0.7	200	200k	TO-5 DIP	Single, with strobe, will work from single supply, low bias current
LH2111 Dual (Note 1)	Military	5	±15	0.1	0.04	0.7	200	200k	TO-5 DIP F.P.	
LM211	Industrial	5	To 5	0.1	0.04	0.7	200	200k	To-5 DIP	
LH2211 Dual (Note 1)	Industrial	5	To 5	0.1	0.04	0.7	200	200k	TO-5 DIP F.P.	
LM311	Commercial	5	And GND	0.25	0.06	2	200	200k	TO-5 DIP	
LH2311 Dual (Note 1)	Commercial	5	And GND	0.25	0.06	2	200	200k	TO-5 DIP F.P.	
LM119	Military	2 (Each Side)	±15	0.5	0.075	4	80	40k	TO-5 DIP	High speed dual comparator
LM219	Industrial	2 (Each Side)	To 5	0.5	0.075	4	80	40k	TO-5 DIP	
LM319	Commercial	2 (Each Side)	And GND	1	0.2	8	80	40k	TO-5 DIP	
LM139 Quad	Military	1	±1	0.1	0.025	5	1.3μs	200k	DIP	Quad comparator designed for single supply operation; input common mode range includes ground
LM239 Quad	Industrial	1	To ±18	0.25	0.050	5	1.3μs	200k	DIP	
LM339 Quad	Commercial	1	Or From	0.25	0.050	5	1.3μs	200k	DIP	
LM139A Quad	Military	1	2	0.1	0.025	2	1.3μs	200k	DIP	Low offset voltage Quad comparator with DTL/TTL logic levels
LM239A Quad	Industrial	1	To 36	0.25	0.050	2	1.3μs	200k	DIP	
LM339A Quad	Commercial	1	And GND	0.25	0.050	2	1.3μs	200k	DIP	
LM160	Military	2	±4.5	10	2	2	16	3k	TO-5 DIP	Very high speed, outputs compatible with DTL/TTL logic levels
LM260	Industrial	2	To	10	2	2	16	3k	TO-5 DIP	
LM360	Commercial	2	±6.5	15	4	4	16	3k	TO-5 DIP	
LM161 (LM529)	Military	2	±5	10	2	2	12	3k	TO-5 DIP	Very high speed, with individual strobes, DTL/TTL compatible
LM261	Industrial	2	To ±15	10	2	2	12	3k	TO-5 DIP	
LM361 (LM529C)	Commercial	2	And 5	15	4	4	12	3k	TO-5 DIP	
LM193	Military	1	±1	0.1	0.025	5	1.3μs	200k	TO-5	Dual comparator designed for single supply operation; input common-mode range includes ground
LM293	Industrial	1	To ±18	0.25	0.050	5	1.3μs	200k	TO-5	
LM393	Commercial	1	Or From	0.25	0.050	5	1.3μs	200k	TO-5, DIP	
LM193A	Military	1	2	0.1	0.025	2	1.3μs	200k	TO-5	Low offset voltage dual comparator with DTL/TTL logic levels
LM293A	Industrial	1	To 36	0.25	0.050	2	1.3μs	200k	TO-5	
LM393A	Commercial	1	And Gnd	0.25	0.050	2	1.3μs	200k	TO-5, DIP	
LM710	Military	1	$V^+ = 12$	20	3	2	40	1750	TO-5	Single, differential in, single output
LM710C	Commercial	1	$V^- = -6$	25	5	5	40	1500	TO-5 DIP	
LM711 Dual	Military	1	$V^+ = 12$	75	10	3.5	40	1500	TO-5	Dual differential, common output, individual strobes
LM711C Dual	Commercial	1	$V^- = -6$	100	15	5	40	1500	TO-5 DIP	
LM1514 Dual	Military	1	$V^+ = 14$	20	3	3	30	1250	DIP	Dual LM710 with separate strobes, individual outputs
LM1414 Dual	Commercial	1	$V^- = -7$	25	5	4	30	1000	DIP	
LM2901 Quad	Industrial	1	±1 (2V) to ±18 (36)	0.25	0.05	7	1.3	200k	DIP	Quad comparator designed for single supply operation; input common-mode range includes ground
LM2903	Automotive	1	±1 (2V) to ±18 (36)	0.25	0.050	7	1.3μs	200k	DIP	Dual comparator designed for single supply operation; input common-mode range includes ground

Note 1: Dual version of device. †Response time is specified for 100 mV step input with 5 mV overdrive.

*Military: −55°C to +125°C; Industrial: −25°C to +85°C; Commercial: 0°C to +70°C; Automotive: −40°C to +85°C

National Semiconductor

Definition of Terms

Input Bias Current: The average of the two input currents.

Input Offset Current: The absolute value of the difference between the two input currents for which the output will be driven higher than or lower than specified voltages.

Input Offset Voltage: The absolute value of the voltage between the input terminals required to make the output voltage greater than or less than specified voltages.

Input Voltage Range: The range of voltage on the input terminals (common-mode) over which the offset specifications apply.

Logic Threshold Voltage: The voltage at the output of the comparator at which the loading logic circuitry changes its digital state.

Negative Output Level: The negative dc output voltage with the comparator saturated by a differential input equal to or greater than a specified voltage.

Output Leakage Current: The current into the output terminal with the output voltage within a given range and the input drive equal to or greater than a given value.

Output Resistance: The resistance seen looking into the output terminal with the dc output level at the logic threshold voltage.

Output Sink Current: The maximum negative current that can be delivered by the comparator.

Positive Output Level: The high output voltage level with a given load and the input drive equal to or greater than a specified value.

Power Consumption: The power required to operate the comparator with no output load. The power will vary with signal level, but is specified as a maximum for the entire range of input signal conditions.

Response Time: The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

Saturation Voltage: The low-output voltage level with the input drive equal to or greater than a specified value.

Strobe Current: The current out of the strobe terminal when it is at the zero logic level.

Strobed Output Level: The dc output voltage, independent of input conditions, with the voltage on the strobe terminal equal to or less than the specified low state.

Strobe "ON" Voltage: The maximum voltage on either strobe terminal required to force the output to the specified high state independent of the input voltage.

Strobe "OFF" Voltage: The minimum voltage on the strobe terminal that will guarantee that it does not interfere with the operation of the comparator.

Strobe Release Time: The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from zero to the one logic level.

Supply Current: The current required from the positive or negative supply to operate the comparator with no output load. The power will vary with input voltage, but is specified as a maximum for the entire range of input voltage conditions.

Voltage Gain: The ratio of the change in output voltage to the change in voltage between the input terminals producing it.

National Semiconductor

Voltage Comparators

LF111/LF211/LF311 Voltage Comparators

General Description

The LF111, LF211 and LF311 are FET input voltage comparators that virtually eliminate input current errors. Designed to operate over a 5.0V to ±15V range the LF111 can be used in the most critical applications.

The extremely low input currents of the LF111 allows the use of a simple comparator in applications usually requiring input current buffering. Leakage testing, long time delay circuits, charge measurements, and high source impedance voltage comparisons are easily done.

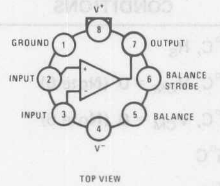
Further, the LF111 can be used in place of the LM111 eliminating errors due to input currents. See the "application hints" of the LM311 for application help.

Advantages

- Eliminates input current errors
- Interchangeable with LM111
- No need for input current buffering

Connection Diagram

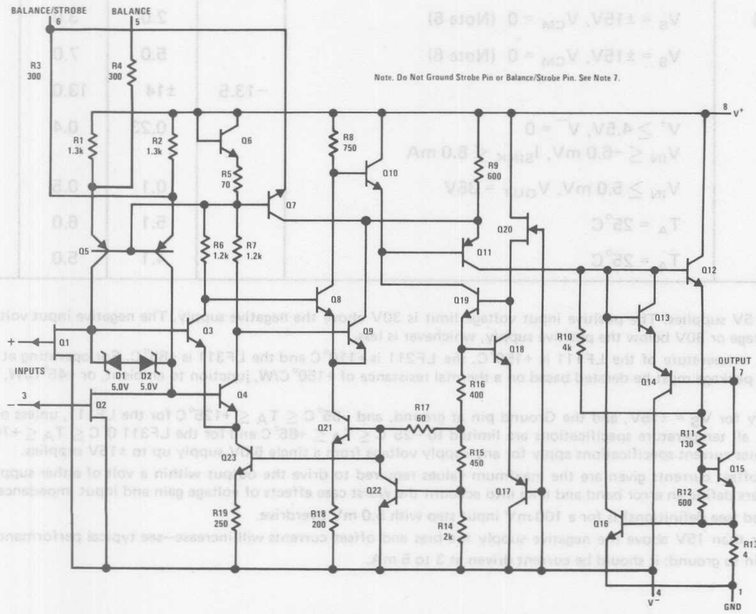
Metal Can Package

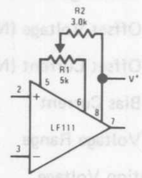


Order Number LF111H, LF211H or LF311H
See NS Package H08C

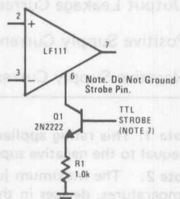
Schematic Diagram and Auxiliary Circuits

Note. Do Not Ground Strobe Pin or Balance/Strobe Pin. See Note 7.

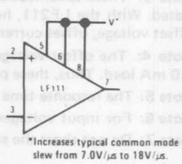




Offset Balancing



Strobing



*Increases typical common mode slew from 7.0V/μs to 18V/μs.

Increasing Input Stage Current*

Total Supply Voltage (V_{84})	36V	36V
Output to Negative Supply Voltage (V_{74})	50V	40V
Ground to Negative Supply Voltage (V_{14})	30V	30V
Differential Input Voltage	±30V	±30V
Input Voltage (Note 1)	±15V	±15V
Power Dissipation (Note 2)	500 mW	500 mW
Output Short Circuit Duration	10 seconds	10 seconds
Operating Temperature Range		
LF111	−55°C to +125°C	
LF211	−25°C to +85°C	
LF311		0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

Electrical Characteristics (LF111/LF211) (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 4)	T_A = 25°C, R_S		0.7	4.0	mV
Input Offset Current (Note 4)	T_A = 25°C, V_{CM} = 0 (Note 6)		5.0	25	pA
Input Bias Current	T_A = 25°C, V_{CM} = 0 (Note 6)		20	50	pA
Voltage Gain	T_A = 25°C	40	200		V/mV
Response Time (Note 5)	T_A = 25°C		200		ns
Saturation Voltage	$V_{IN} \leq -5.0$ mV, I_{OUT} = 50 mA, T_A = 25°C		0.75	1.5	V
Strobe On Current	T_A = 25°C		3.0		mA
Output Leakage Current	$V_{IN} \geq 5.0$ mV, V_{OUT} = 35V, T_A = 25°C		0.2	10	nA
Input Offset Voltage (Note 4)				6.0	mV
Input Offset Current (Note 4)	V_S = ±15V, V_{CM} = 0 (Note 6)		2.0	3.0	nA
Input Bias Current	V_S = ±15V, V_{CM} = 0 (Note 6)		5.0	7.0	nA
Input Voltage Range		−13.5	±14	13.0	V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -6.0$ mV, $I_{SINK} \leq 8.0$ mA		0.23	0.4	V
Output Leakage Current	$V_{IN} \geq 5.0$ mV, V_{OUT} = 35V		0.1	0.5	µA
Positive Supply Current	T_A = 25°C		5.1	6.0	mA
Negative Supply Current	T_A = 25°C		4.1	5.0	mA

Note 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LF111 is +150°C, the LF211 is +110°C and the LF311 is +85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of +150°C/W, junction to ambient, or +45°C/W, junction to case.

Note 3: These specifications apply for V_S = ±15V, and the Ground pin at ground, and $-55°C \leq T_A \leq +125°C$ for the LF111, unless otherwise stated. With the LF211, however, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$ and for the LF311 $0°C \leq T_A \leq +70°C$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5.0V supply up to ±15V supplies.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1.0 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

Note 5: The response time specified (see definitions) is for a 100 mV input step with 5.0 mV overdrive.

Note 6: For input voltages greater than 15V above the negative supply the bias and offset currents will increase—see typical performance curves.

Note 7: Do not short the strobe pin to ground; it should be current driven at 3 to 5 mA.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 4)	$T_A = 25^\circ C$, $R_S \leq 50k$		2.0	10	mV
Input Offset Current (Note 4)	$T_A = 25^\circ C$, $V_{CM} = 0$ (Note 6)		5.0	75	pA
Input Bias Current	$T_A = 25^\circ C$, $V_{CM} = 0$ (Note 6)		25	150	pA
Voltage Gain	$T_A = 25^\circ C$		200		V/mV
Response Time (Note 5)	$T_A = 25^\circ C$		200		ns
Saturation Voltage	$V_{IN} \leq -10$ mV, $I_{OUT} = 50$ mA, $T_A = 25^\circ C$		0.75	1.5	V
Strobe On Current	$T_A = 25^\circ C$		3.0		mA
Output Leakage Current	$V_{IN} \geq 10$ mV, $V_{OUT} = 35V$, $T_A = 25^\circ C$		0.2	10	nA
Input Offset Voltage (Note 4)	$R_S \leq 50k$			15	mV
Input Offset Current (Note 4)	$V_S = \pm 15V$, $V_{CM} = 0$ (Note 6)		1.0		nA
Input Bias Current	$V_S = \pm 15V$, $V_{CM} = 0$ (Note 6)		3.0		nA
Input Voltage Range			+14 −13.5		V V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -10$ mV, $I_{SINK} \leq 8.0$ mA		0.23	0.4	V
Positive Supply Current	$T_A = 25^\circ C$		5.1	7.5	mA
Negative Supply Current	$T_A = 25^\circ C$		4.1	5.0	mA

Note 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LF111 is +150°C, the LF211 is +110°C and the LF311 is +85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of +150°C/W, junction to ambient, or +45°C/W, junction to case.

Note 3: These specifications apply for $V_S = \pm 15V$ and $-55^\circ C \leq T_A \leq +125^\circ C$ for the LF111, unless otherwise stated. With the LF211, however, all temperature specifications are limited to $-25^\circ C \leq T_A \leq +85^\circ C$ and for the LF311 $0^\circ C \leq T_A \leq +70^\circ C$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5.0 mV supply up to ±15V supplies.

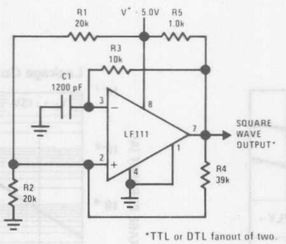
Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1.0 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

Note 5: The response time specified (see definitions) is for a 100 mV input step with 5.0 mV overdrive.

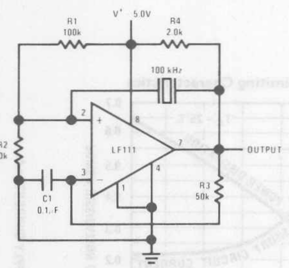
Note 6: For input voltages greater than 15V above the negative supply the bias and offset currents will increase—see typical performance curves.

Note 7: Do not short the strobe pin to ground; it should be current driven at 3 to 5 mA.

Typical Applications

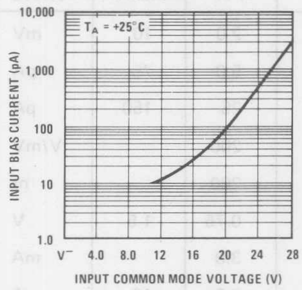


100 kHz Free Running Multivibrator

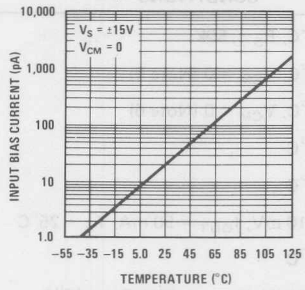


Crystal Oscillator

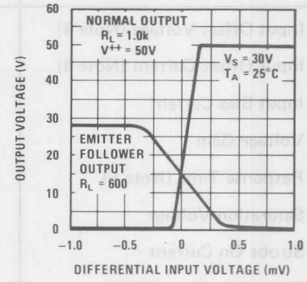
Typical Performance



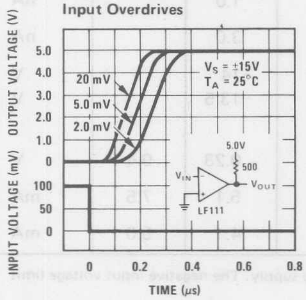
Input Bias Current vs Common Mode



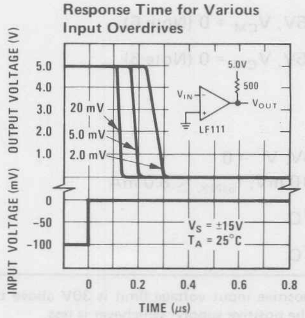
Input Bias Current vs Temperature



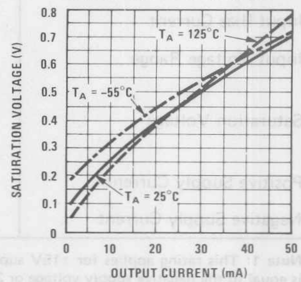
Transfer Function



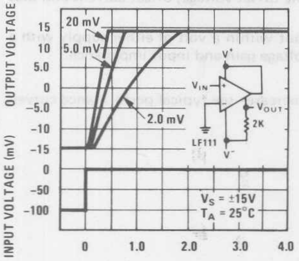
Response Time for Various Input Overdrives



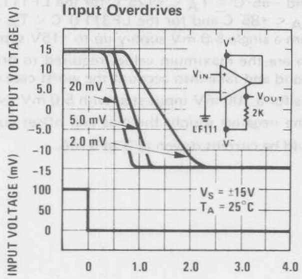
Response Time for Various Input Overdrives



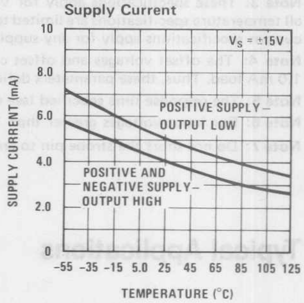
Output Saturation Voltage



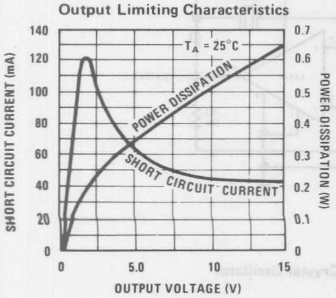
Response Time for Various Input Overdrives



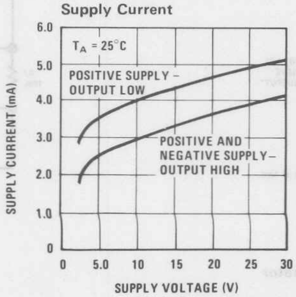
Response Time for Various Input Overdrives



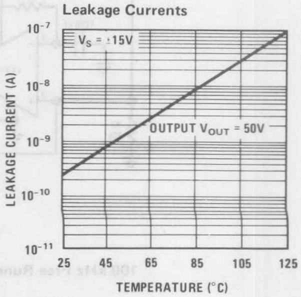
Supply Current



Output Limiting Characteristics

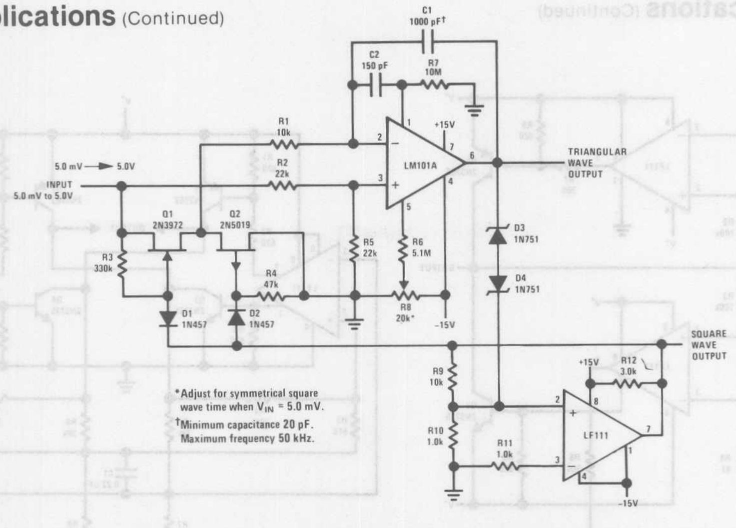


Supply Current

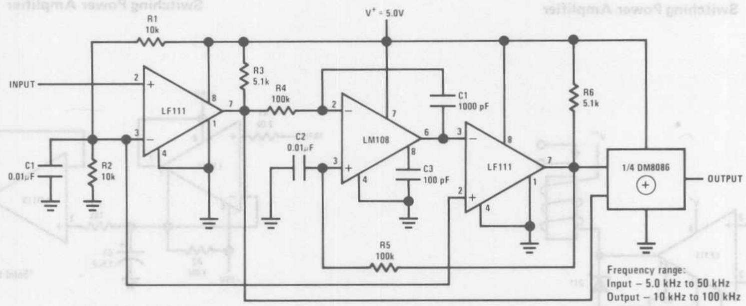


Leakage Currents

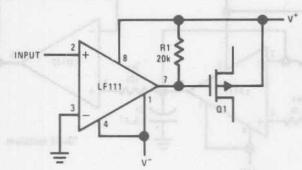
Typical Applications (Continued)



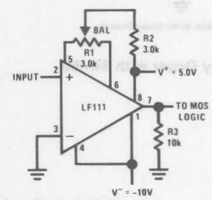
10 Hz to 10 kHz Voltage Controlled Oscillator



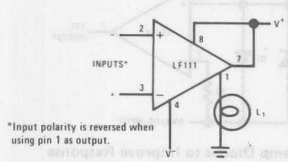
Frequency Doubler



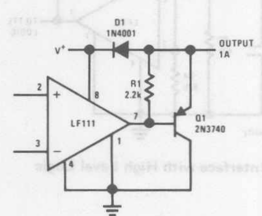
Zero Crossing Detector Driving MOS Switch



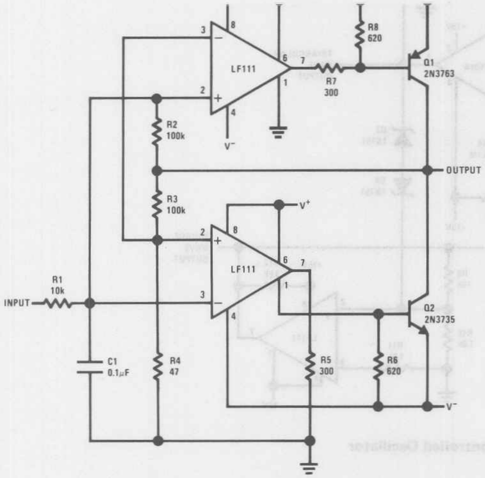
Zero Crossing Detector Driving MOS Logic



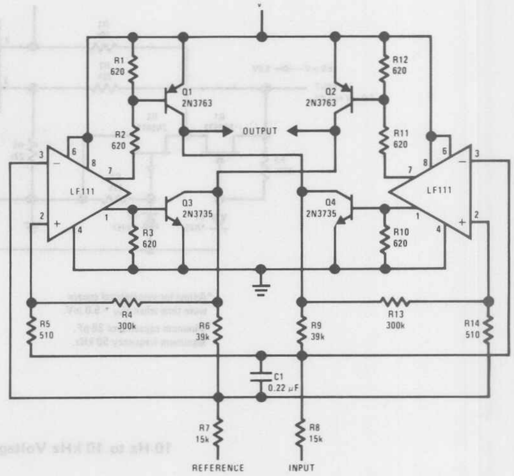
Driving Ground-Referred Load



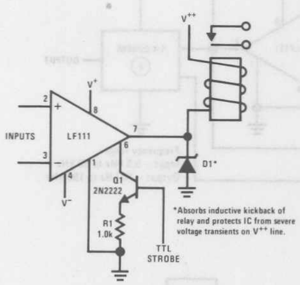
Comparator and Solenoid Driver



Switching Power Amplifier

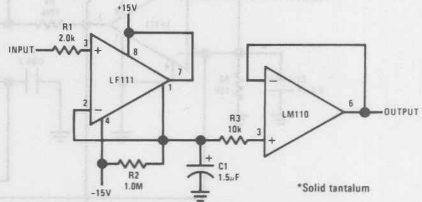


Switching Power Amplifier

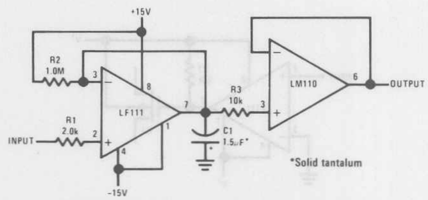


Note. Do Not Ground Strobe Pin.

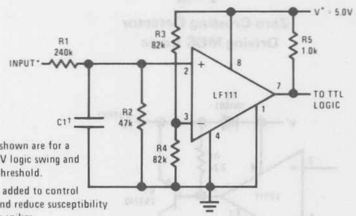
Relay Driver with Strobe



Positive Peak Detector



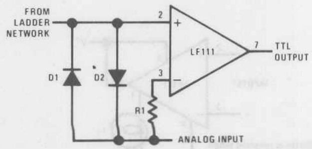
Negative Peak Detector



*Values shown are for a 0 to 30V logic swing and a 15V threshold.

†May be added to control speed and reduce susceptibility to noise spikes.

TTL Interface with High Level Logic



Using Clamp Diodes to Improve Response

LH2111/LH2211/LH2311 Dual Voltage Comparator

General Description

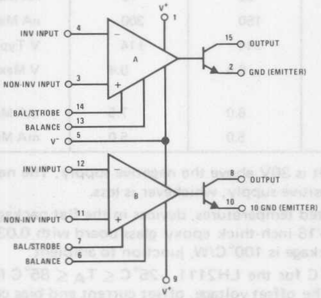
The LH2111 series of dual voltage comparators are two LM111 type comparators in a single hermetic package. Featuring all the same performance characteristics of the single, these duals offer in addition closer thermal tracking, lower weight, reduced insertion cost and smaller size than two singles. For additional information see the LM111 data sheet and National's Linear Application Handbook.

The LH2111 is specified for operation over the −55°C to +125°C military temperature range. The LH2211 is specified for operation over the −25°C to +85°C temperature range. The LH2311 is specified for operation over the 0°C to 70°C temperature range.

Features

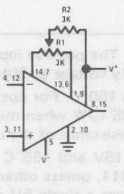
- Wide operating supply range ±15V to a single +5V
- Low input currents 6 nA
- High sensitivity 10 μV
- Wide differential input range ±30V
- High output drive 50 mA, 50V

Connection Diagram

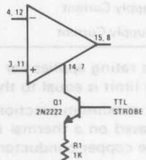


Order Number LH2111D or LH2211D or LH2311D
See Package D16C
LH2111F or LH2211F or LH2311F,
See Package F16B
LH2111J or LH2211J or LH2311J,
See Package J16A

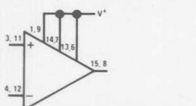
Auxiliary Circuits



Offset Balancing

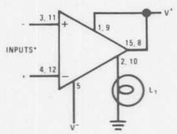


Strobing

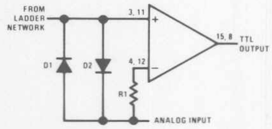


*Increases typical common mode slew from 7.0V/μs to 18V/μs.

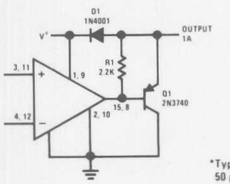
Increasing Input Stage Current*



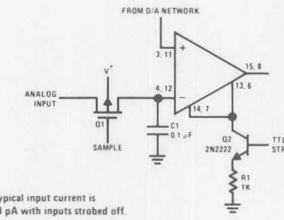
Driving Ground-Referred Load



Using Clamp Diodes to Improve Responses

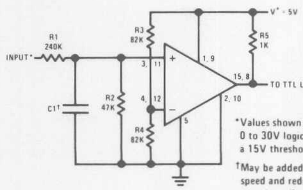


Comparator and Solenoid Driver



*Typical input current is 50 pA with inputs strobed off.

Strobing off Both Input* and Output Stages



*Values shown are for a 0 to 30V logic swing and a 15V threshold.

†May be added to control speed and reduce susceptibility to noise spikes.

TTL Interface with High Level Logic

Absolute Maximum Ratings

Total Supply Voltage ($V^+ - V^-$)	36V
Output to Negative Supply Voltage ($V_{OUT} - V^-$)	50V
Ground to Negative Supply Voltage (GND $- V^-$)	30V
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 sec
Operating Temperature Range LH2111	−55°C to 125°C
LH2211	−25°C to 85°C
LH2311	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics Each Side (Note 3)

PARAMETER	CONDITIONS	LIMITS			UNITS
		LH2111	LH2211	LH2311	
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50k$	3.0	3.0	7.5	mV Max
Input Offset Current (Note 4)	$T_A = 25°C$	10	10	50	nA Max
Input Bias Current	$T_A = 25°C$	100	100	250	nA Max
Voltage Gain	$T_A = 25°C$	200	200	200	V/mV Typ
Response Time (Note 5)	$T_A = 25°C$	200	200	200	ns Typ
Saturation Voltage	$V_{IN} \leq -5$ mV, $I_{OUT} = 50$ mA, $T_A = 25°C$	1.5	1.5	1.5	V Max
Strobe On Current	$T_A = 25°C$	3.0	3.0	3.0	mA Typ
Output Leakage Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$, $T_A = 25°C$	10	10	50	nA Max
Input Offset Voltage (Note 4)	$R_S \leq 50k$	4.0	4.0	10	mV Max
Input Offset Current (Note 4)		20	20	70	nA Max
Input Bias Current		150	150	300	nA Max
Input Voltage Range		±14	±14	±14	V Typ
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$, $V_{IN} \leq -5$ mV, $I_{SINK} \leq 8$ mA	0.4	0.4	0.4	V Max
Positive Supply Current	$T_A = 25°C$	6.0	6.0	7.5	mA Max
Negative Supply Current	$T_A = 25°C$	5.0	5.0	5.0	mA Max

Note 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature is 150°C. For operating at elevated temperatures, devices in the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with 0.03-inch-wide, 2 ounce copper conductor. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 3: These specifications apply for $V_S = \pm 15V$ and $-55°C \leq T_A \leq 125°C$ for the LH2111, $-25°C \leq T_A \leq 85°C$ for the LH2211, and $0°C \leq T_A \leq 70°C$ for the LH2311, unless otherwise stated. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies. For the LH2311, $V_{IN} = \pm 10$ mV.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

Note 5: The response time specified is for a 100 mV input step with 5 mV overdrive.

National Semiconductor

LM106/LM206/LM306 Voltage Comparator

General Description

The LM106 series are high-speed voltage comparators designed to accurately detect low-level analog signals and drive a digital load. They are equivalent to an LM710, combined with a two input NAND gate and an output buffer. The circuits can drive RTL, DTL or TTL integrated circuits directly. Furthermore, their outputs can switch voltages up to 24V at currents as high as 100 mA.

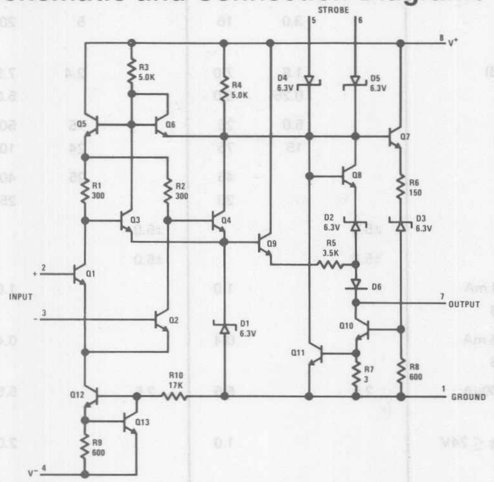
The devices have short-circuit protection which limits the inrush current when it is used to drive incandescent lamps, in addition to preventing damage from accidental shorts to the positive supply. The speed is equivalent to that of an LM710. However, they are even faster where buffers and additional logic circuitry can be eliminated by the increased flexibility of the LM106 series. They can also be operated from any negative supply voltage between −3V and −12V with little effect on performance.

The LM106 is specified for operation over the −55°C to +125°C military temperature range. The LM206 is specified for operation over the −25°C to +85°C temperature range. The LM306 is specified for operation over 0°C to +70°C temperature range.

Features

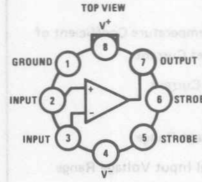
- Improved accuracy
- Fan-out of 10 with DTL or TTL
- Added logic or strobe capability
- Useful as a relay or lamp driver
- Plug-in replacement for the LM710
- 40 ns maximum response time

Schematic and Connection Diagrams **



Metal Can

TOP VIEW

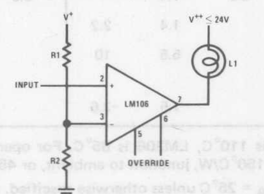


Note: Pin 4 connected to case.

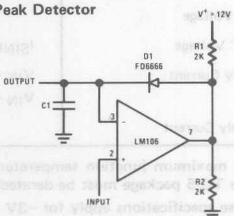
Order Number LM106H, LM206H or LM306H
See NS Package H08C

Typical Applications **

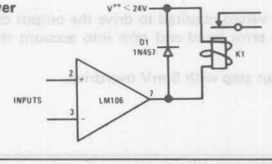
Level Detector and Lamp Driver



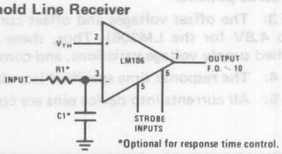
Fast Response Peak Detector



Relay Driver



Adjustable Threshold Line Receiver



*Optional for response time control.

Output Voltage	24V
Output to Negative Supply Voltage	30V
Differential Input Voltage	±5V
Input Voltage	±7V

Operating Temperature Range	T_{MIN}	T_{MAX}
LM106	−55°C to	+125°C
LM206	−25°C to	+85°C
LM306	0°C to	+70°C
Storage Temperature Range	−65°C to	+150°C
Lead Temperature (Soldering, 10 seconds)		300°C

Electrical Characteristics (Note 2)

PARAMETER	CONDITIONS	LM106/LM206 MIN	LM106/LM206 TYP	LM106/LM206 MAX	LM306 MIN	LM306 TYP	LM306 MAX	UNITS
Input Offset Voltage	(Note 3)		0.5	2.0		1.6	5.0	mV
Input Offset Current	(Note 3)		0.7	3.0		1.8	5.0	μA
Input Bias Current			10	20		16	25	μA
Response Time	$R_L = 390\Omega$ to 5V $C_L = 15$ pF, (Note 4)		28	40		28	40	ns
Saturation Voltage	$V_{IN} \leq -5$ mV, $I_{OUT} = 100$ mA		1.0	1.5				V
	$V_{IN} \leq -7$ mV, $I_{OUT} = 100$ mA					0.8	2.0	V
Output Leakage Current	$V_{IN} \geq 5$ mV, $8V \leq V_{OUT} \leq 24V$		0.02	1.0				μA
	$V_{IN} \geq 7$ mV, $8V \leq V_{OUT} \leq 24V$					0.02	2.0	μA
The following specifications apply for $T_{MIN} \leq T_A \leq T_{MAX}$ (Note 5)								
Input Offset Voltage	(Note 3)			3.0			6.5	mV
Average Temperature Coefficient of Input Offset Voltage			3.0	10		5	20	μV/°C
Input Offset Current	$T_L \leq T_A \leq 25°C$, (Note 3)		1.8	7.0		2.4	7.5	μA
	$25°C \leq T_A \leq T_H$		0.25	3.0			5.0	μA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq T_H$		5.0	25		15	50	nA/°C
	$T_L \leq T_A \leq 25°C$		15	75		24	100	nA/°C
Input Bias Current	$T_L \leq T_A \leq 25°C$			45		25	40	μA
	$25°C \leq T_A \leq T_H$			20			25	μA
Input Voltage Range	$-7V \geq V^- \geq -12V$	±5.0			±5.0			V
Differential Input Voltage Range		±5.0			±5.0			V
Saturation Voltage	$V_{IN} \leq -5$ mV, $I_{OUT} = 50$ mA $V_{IN} \leq -8$ mV For LM306			1.0			1.0	V
Saturation Voltage	$V_{IN} \leq -5$ mV, $I_{OUT} = 16$ mA $V_{IN} \leq -8$ mV For LM306			0.4			0.4	V
Positive Output Level	$V_{IN} \geq 5$ mV, $I_{OUT} = -400\mu A$ $V_{IN} \geq 8$ mV For LM306	2.5		5.5	2.5		5.5	V
Output Leakage Current	$V_{IN} \geq 5$ mV, $8V \leq V_{OUT} \leq 24V$ $V_{IN} \geq 8$ mV For LM306 $T_L \leq T_A \leq 25°C$			1.0			2.0	μA
	$25°C < T_A \leq T_H$			100			100	μA
Strobe Current	$V_{STROBE} = 0.4V$		−1.7	−3.2		−1.7	−3.2	mA
Strobe "ON" Voltage		0.9	1.4		0.9	1.4		V
Strobe "OFF" Voltage	$I_{SINK} \leq 16$ mA		1.4	2.2		1.4	2.2	V
Positive Supply Current	$V_{IN} = -5$ mV $V_{IN} = -8$ mV For LM306		5.5	10		5.5	10	mA
Negative Supply Current			−1.5	−3.6		−1.5	−3.6	mA

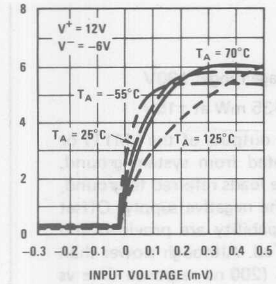
Note 1: The maximum junction temperature of LM106 is 150°C, LM206 is 110°C, LM306 is 85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case.

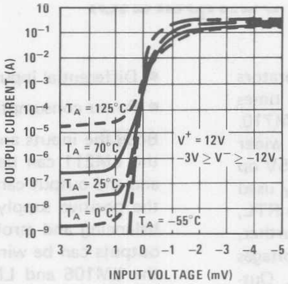
Note 2: These specifications apply for $-3V \geq V^- \geq -12V$, $V^+ = 12V$ and $T_A = 25°C$ unless otherwise specified. All currents into device pins are considered positive.

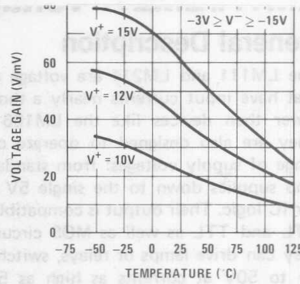
Note 3: The offset voltages and offset currents given are the maximum values required to drive the output down to 0.5V or up to 4.4V (0.5V or up to 4.8V for the LM306). Thus, these parameters actually define an error band and take into account the worst-case effects of voltage gain, specified supply voltage variations, and common mode voltage variations.

Note 4: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

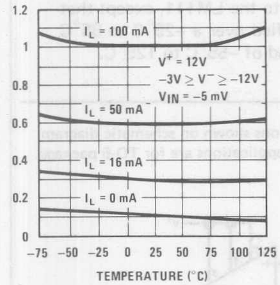
Note 5: All currents into device pins are considered positive.



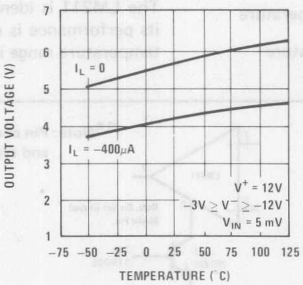




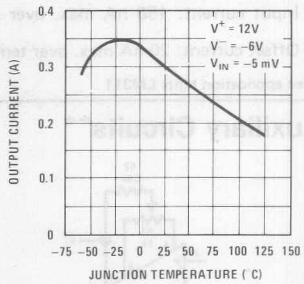
Saturation Voltage



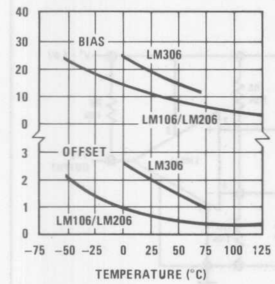
Positive Output Level



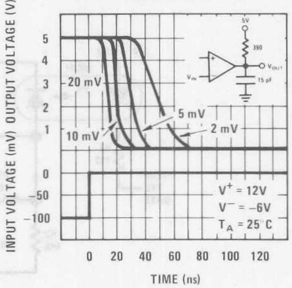
Short Circuit Output Current



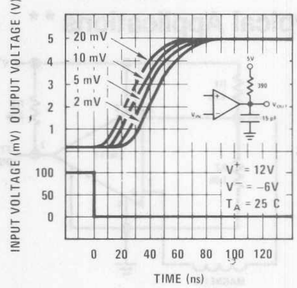
Input Current



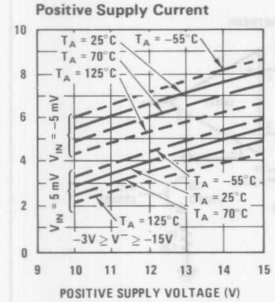
Response Time For Various Input Overdrives



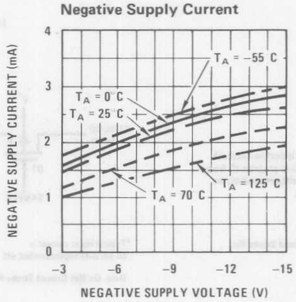
Response Time For Various Input Overdrives



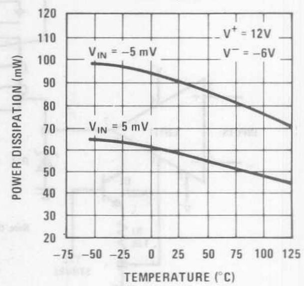
Positive Supply Current



Negative Supply Current



Power Consumption



National Semiconductor

Voltage Comparators

LM111/LM211 Voltage Comparator†

General Description

The LM111 and LM211 are voltage comparators that have input currents nearly a thousand times lower than devices like the LM106 or LM710. They are also designed to operate over a wider range of supply voltages: from standard ±15V op amp supplies down to the single 5V supply used for IC logic. Their output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, they can drive lamps or relays, switching voltages up to 50V at currents as high as 50 mA. Outstanding characteristics include:

- Operates from single 5V supply
- Input current: 150 nA max. over temperature
- Offset current: 20 nA max. over temperature
- Differential input voltage range: ±30V
- Power consumption: 135 mW at ±15V

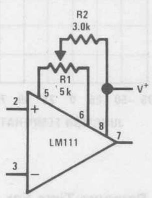
Both the inputs and the outputs of the LM111 or the LM211 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the LM106 and LM710 (200 ns response time vs 40 ns) the devices are also much less prone to spurious oscillations. The LM111 has the same pin configuration as the LM106 and LM710.

The LM211 is identical to the LM111, except that its performance is specified over a −25°C to 85°C temperature range instead of −55°C to 125°C.

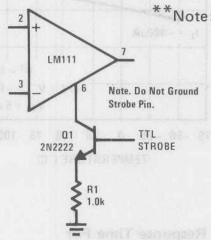
†See application hints LM311

Auxiliary Circuits**

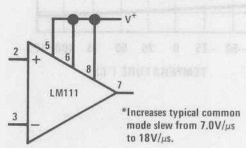
**Note: Pin connections shown on schematic diagram and typical applications are for TO-5 package.



Offset Balancing

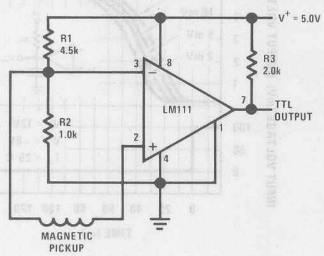


Strobing

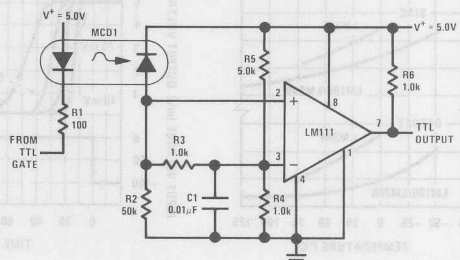


Increasing Input Stage Current*

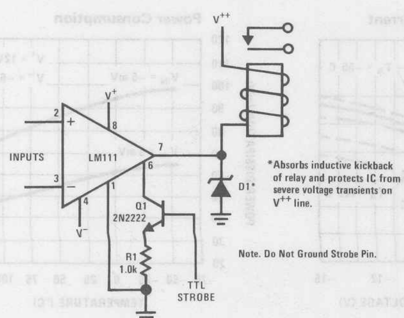
Typical Applications **



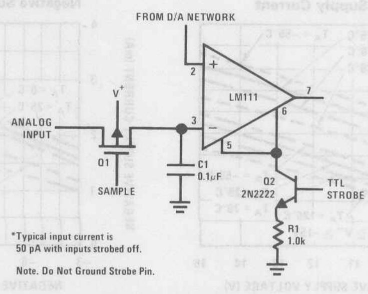
Detector for Magnetic Transducer



Digital Transmission Isolator



Relay Driver with Strobe*



Strobing off Both Input* and Output Stages

Absolute Maximum Ratings

Total Supply Voltage (V_{84})		36V
Output to Negative Supply Voltage (V_{74})		50V
Ground to Negative Supply Voltage (V_{14})		30V
Differential Input Voltage		±30V
Input Voltage (Note 1)		±15V
Power Dissipation (Note 2)		500 mW
Output Short Circuit Duration		10 sec
Operating Temperature Range	LM111	−55°C to 125°C
	LM211	−25°C to 85°C
Storage Temperature Range		−65°C to 150°C
Lead Temperature (soldering, 10 sec)		300°C
Voltage at Strobe Pin		V^+−5V

Electrical Characteristics (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50k$		0.7	3.0	mV
Input Offset Current (Note 4)	$T_A = 25°C$		4.0	10	nA
Input Bias Current	$T_A = 25°C$		60	100	nA
Voltage Gain	$T_A = 25°C$	40	200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200		ns
Saturation Voltage	$V_{IN} \leq -5$ mV, $I_{OUT} = 50$ mA $T_A = 25°C$		0.75	1.5	V
Strobe ON Current (Note 6)	$T_A = 25°C$		3.0		mA
Output Leakage Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$ $T_A = 25°C$, $I_{STROBE} = 3$ mA		0.2	10	nA
Input Offset Voltage (Note 4)	$R_S \leq 50k$			4.0	mV
Input Offset Current (Note 4)				20	nA
Input Bias Current				150	nA
Input Voltage Range	$V^+ = 15V$, $V^- = -15V$, Pin 7 Pull-Up May Go To 5V	−14.5	13.8,−14.7	13.0	V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -6$ mV, $I_{SINK} \leq 8$ mA		0.23	0.4	V
Output Leakage Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$		0.1	0.5	µA
Positive Supply Current	$T_A = 25°C$		5.1	6.0	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

Note 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

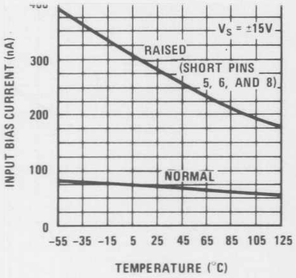
Note 2: The maximum junction temperature of the LM111 is 150°C, while that of the LM211 is 110°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

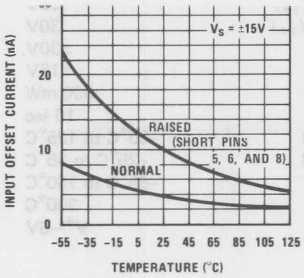
Note 3: These specifications apply for $V_S = \pm15V$ and Ground pin at ground, and $-55°C \leq T_A \leq +125°C$, unless otherwise stated. With the LM211, however, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.

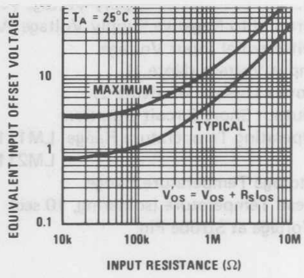
Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.

Note 5: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

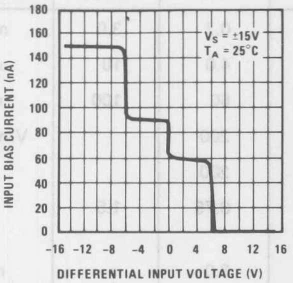
Note 6: Do not short the strobe pin to ground; it should be current driven at 3 to 5 mA.



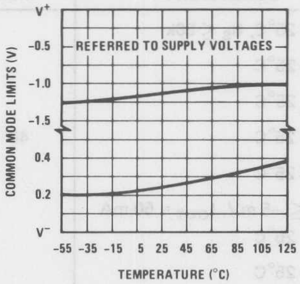




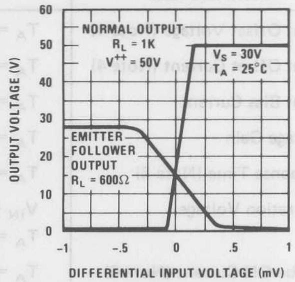
Input Characteristics



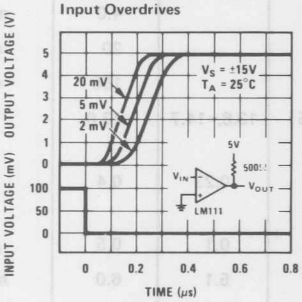
Common Mode Limits



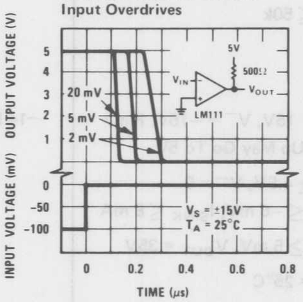
Transfer Function



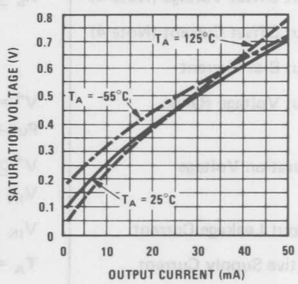
Response Time for Various Input Overdrives



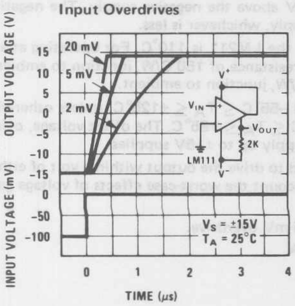
Response Time for Various Input Overdrives



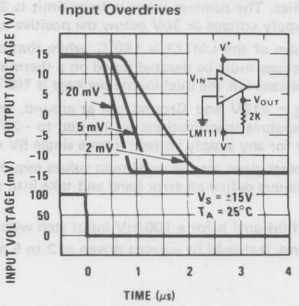
Output Saturation Voltage



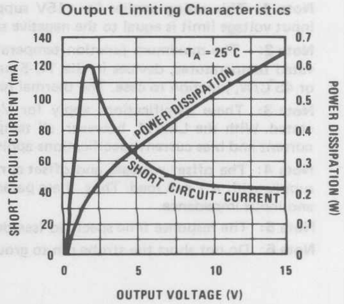
Response Time for Various Input Overdrives



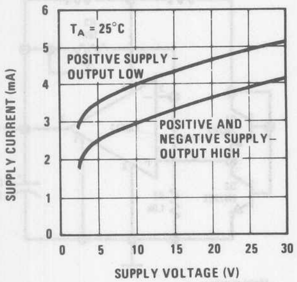
Response Time for Various Input Overdrives



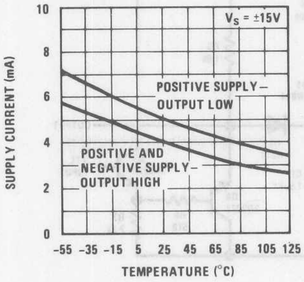
Output Limiting Characteristics



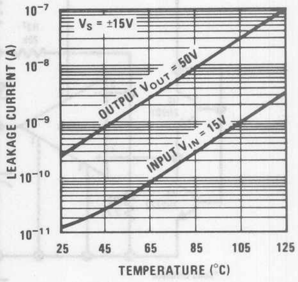
Supply Current



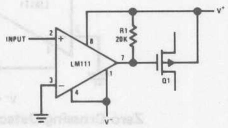
Supply Current



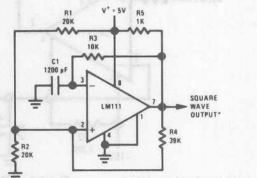
Leakage Currents



Typical Applications (Continued)

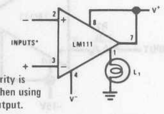


Zero Crossing Detector Driving MOS Switch



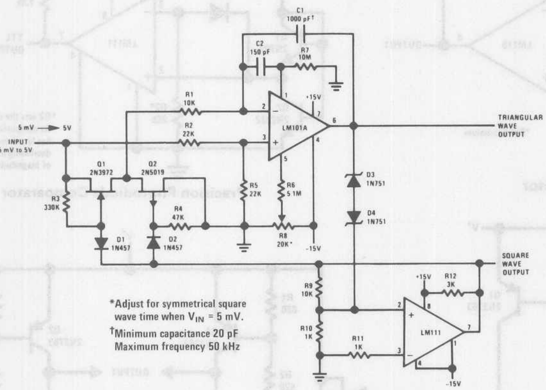
*TTL or DTL fanout of two.

100 kHz Free Running Multivibrator



*Input polarity is reversed when using pin 1 as output.

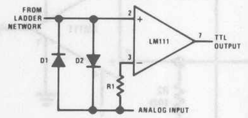
Driving Ground-Referred Load



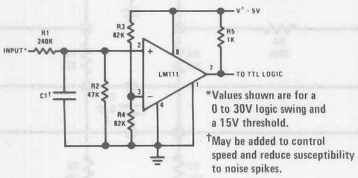
*Adjust for symmetrical square wave time when V_{IN} = 5 mV.

†Minimum capacitance 20 pF Maximum frequency 50 kHz

10 Hz to 10 kHz Voltage Controlled Oscillator



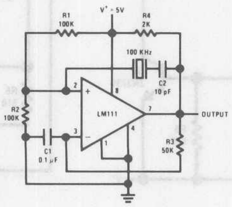
Using Clamp Diodes to Improve Response



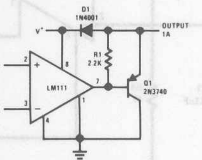
*Values shown are for a 0 to 30V logic swing and a 15V threshold.

†May be added to control speed and reduce susceptibility to noise spikes.

TTL Interface with High Level Logic

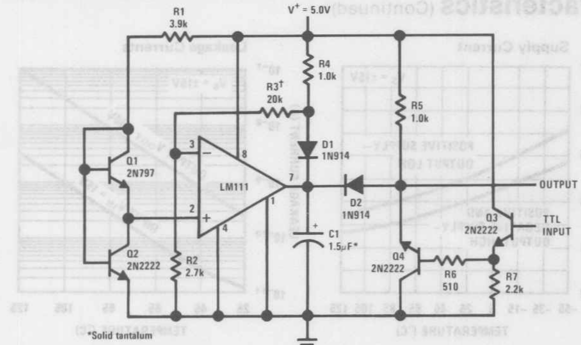


Crystal Oscillator



Comparator and Solenoid Driver

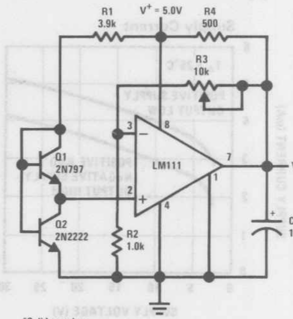
Typical Applications (Continued)



*Solid tantalum

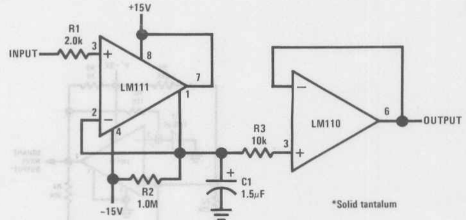
†Adjust to set clamp level

Precision Squarer



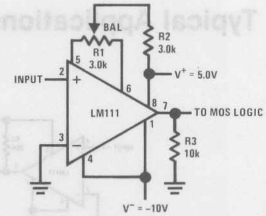
*Solid tantalum

Low Voltage Adjustable Reference Supply

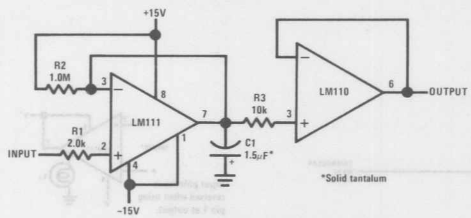


*Solid tantalum

Positive Peak Detector

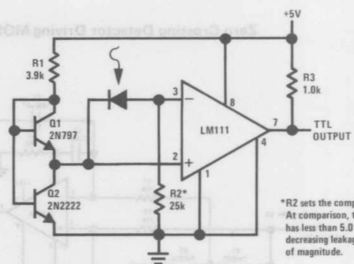


Zero Crossing Detector driving MOS logic



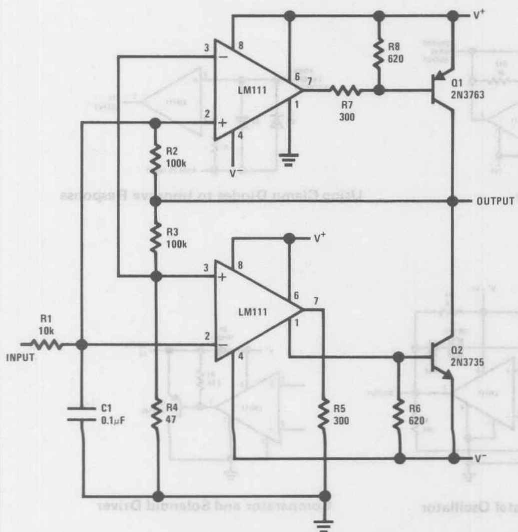
*Solid tantalum

Negative Peak Detector

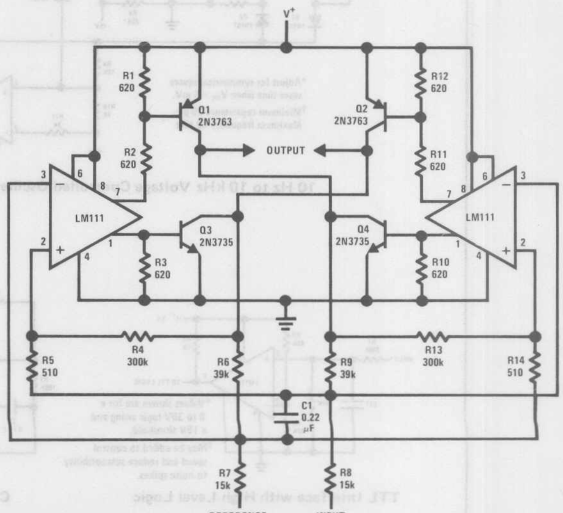


*R2 sets the comparison level. At comparison, the photodiode has less than 5.0 mV across it, decreasing leakages by an order of magnitude.

Precision Photodiode Comparator

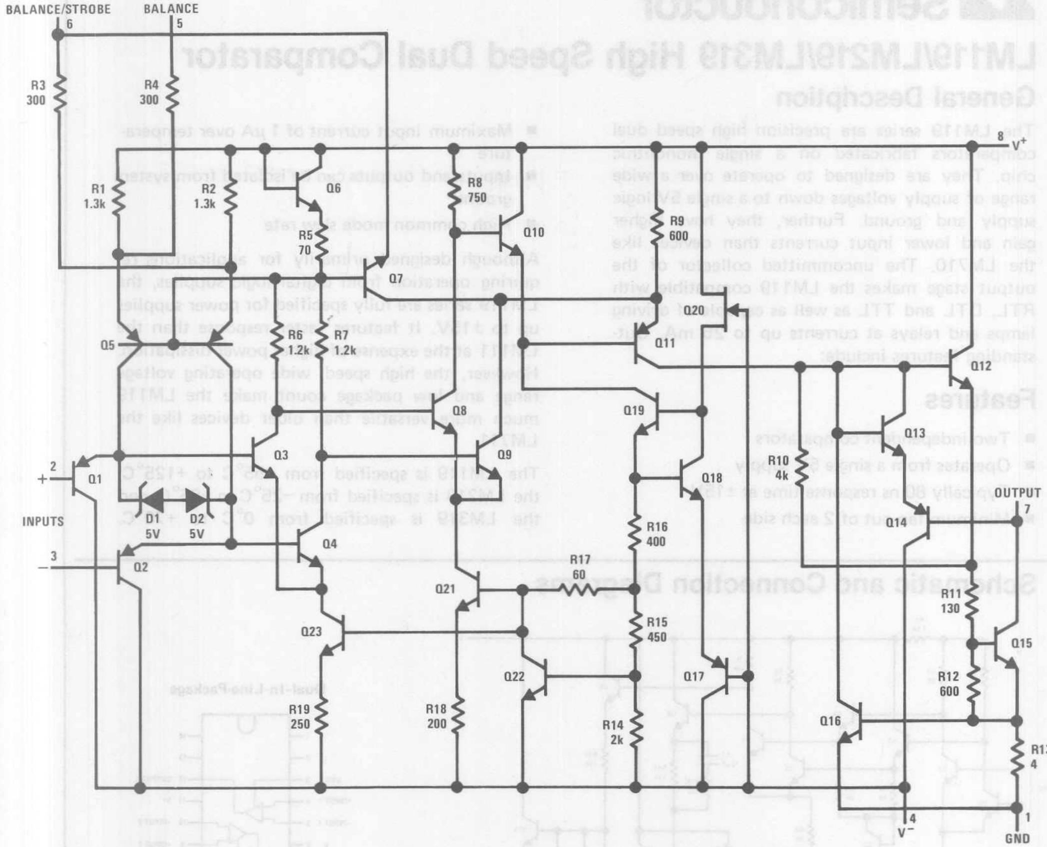


Switching Power Amplifier



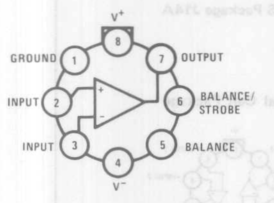
Switching Power Amplifier

Schematic Diagram



Connection Diagrams *

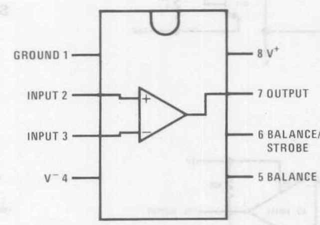
Metal Can Package



TOP VIEW

Order Number LM111H or LM211H
See NS Package H08C

Dual-In-Line Package

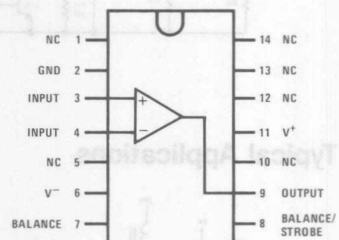


NOTE: Pin 4 connected to case.

TOP VIEW

Order Number LM111J-8
See NS Package J08A

14-Pin Dual-In-Line Package



Note: Pin 6 connected to bottom of package.

TOP VIEW

Order Number LM111J or LM211J
See NS Package J14A

*Pin connections shown are for metal can.

LM119/LM219/LM319 High Speed Dual Comparator

General Description

The LM119 series are precision high speed dual comparators fabricated on a single monolithic chip. They are designed to operate over a wide range of supply voltages down to a single 5V logic supply and ground. Further, they have higher gain and lower input currents than devices like the LM710. The uncommitted collector of the output stage makes the LM119 compatible with RTL, DTL and TTL as well as capable of driving lamps and relays at currents up to 25 mA. Outstanding features include:

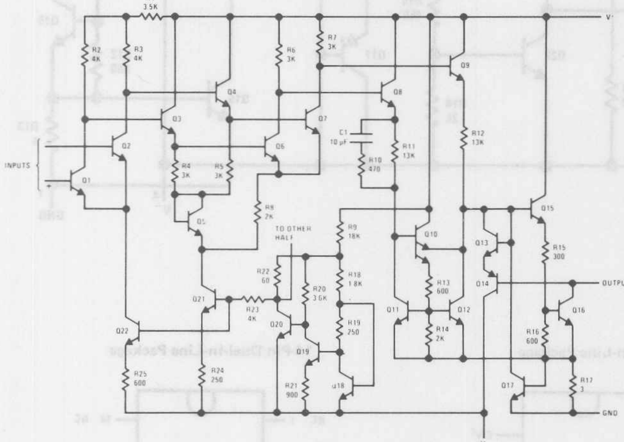
Features

- Two independent comparators
- Operates from a single 5V supply
- Typically 80 ns response time at ±15V
- Minimum fan-out of 2 each side
- Maximum input current of 1 μA over temperature
- Inputs and outputs can be isolated from system ground
- High common mode slew rate

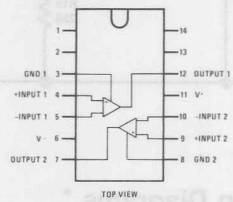
Although designed primarily for applications requiring operation from digital logic supplies, the LM119 series are fully specified for power supplies up to ±15V. It features faster response than the LM111 at the expense of higher power dissipation. However, the high speed, wide operating voltage range and low package count make the LM119 much more versatile than older devices like the LM711.

The LM119 is specified from −55°C to +125°C, the LM219 is specified from −25°C to +85°C, and the LM319 is specified from 0°C to +70°C.

Schematic and Connection Diagrams



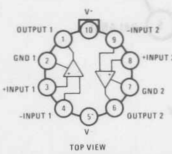
Dual-In-Line-Package



Order Number LM319N
See NS Package N14A

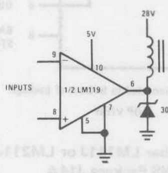
Order Number LM119J, LM219J or LM319J
See NS Package J14A

Metal Can Package

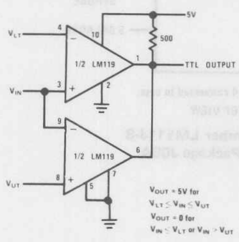


Order Number LM119H, LM219H or LM319H
See NS Package H10C

Typical Applications



Relay Driver



Window Detector

Ground to Negative Supply Voltage	25V	Operating Temperature Range LM119	−55°C to 125°C
Ground to Positive Supply Voltage	18V	LM219	−25°C to 85°C
Differential Input Voltage	±5V	Storage Temperature Range	−65°C to 150°C
Input Voltage (Note 1)	±15V	Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \le 5k$		0.7	4.0	mV
Input Offset Current (Note 4)	$T_A = 25°C$		30	75	nA
Input Bias Current	$T_A = 25°C$		150	500	nA
Voltage Gain	$T_A = 25°C$	10	40		V/mV
Response Time (Note 5)	$T_A = 25°C$ $V_S = \pm 15V$		80		ns
Saturation Voltage	$V_{IN} \le -5$ mV, $I_{OUT} = 25$ mA $T_A = 25°C$		0.75	1.5	V
Output Leakage Current	$V_{IN} \ge 5$ mV, $V_{OUT} = 35V$ $T_A = 25°C$		0.2	2	μA
Input Offset Voltage (Note 4)	$R_S \le 5k$			7	mV
Input Offset Current (Note 4)				100	nA
Input Bias Current				1000	nA
Input Voltage Range	$V_S = \pm 15V$ $V^+ = 5V$, $V^- = 0$	−12 1	±13	+12 3	V V
Saturation Voltage	$V^+ \ge 4.5V$, $V^- = 0$ $V_{IN} \le -6$ mV, $I_{SINK} \le 3.2$ mA $T_A \ge 0°C$ $T_A \le 0°C$		0.23	0.4 0.6	V
Output Leakage Current	$V_{IN} \ge 5$ mV, $V_{OUT} = 35V$, $V_{GND} = 0V$		1	10	μA
Differential Input Voltage				±5	V
Positive Supply Current	$T_A = 25°C$, $V^+ = 5V$, $V^- = 0$		4.3		mA
Positive Supply Current	$T_A = 25°C$ $V_S = \pm 15V$		8	11.5	mA
Negative Supply Current	$T_A = 25°C$ $V_S = \pm 15V$		3	4.5	mA

Note 1: For supply voltages less than ±15V the absolute maximum input voltage is equal to the supply voltage.

Note 2: The maximum junction temperature of the LM119 is 150°C, while that of the LM219 is 110°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 3: These specifications apply for $V_S = \pm 15V$, and the Ground pin at ground, and $-55°C \le T_A \le +125°C$, unless otherwise stated. With the LM219, however, all temperature specifications are limited to $-25°C \le T_A \le +85°C$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

Note 5: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

Absolute Maximum Ratings LM319

Total Supply Voltage	36V
Output to Negative Supply Voltage	36V
Ground to Negative Supply Voltage	25V
Ground to Positive Supply Voltage	18V
Differential Input Voltage	±5V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 sec
Operating Temperature Range LM319	0°C to 70°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 5k$		2.0	8.0	mV
Input Offset Current (Note 4)	$T_A = 25°C$		80	200	nA
Input Bias Current	$T_A = 25°C$		250	1000	nA
Voltage Gain	$T_A = 25°C$	8	40		V/mV
Response Time (Note 5)	$T_A = 25°C$ $V_S = \pm15V$		80		ns
Saturation Voltage	$V_{IN} \leq -10$ mV, $I_{OUT} = 25$ mA $T_A = 25°C$		0.75	1.5	V
Output Leakage Current	$V_{IN} \geq 10$ mV, $V_{OUT} = 35V$, $V^- = V_{GND} = 0V$, $T_A = 25°C$		0.2	10	µA
Input Offset Voltage (Note 4)	$R_S \leq 5k$			10	mV
Input Offset Current (Note 4)				300	nA
Input Bias Current				1200	nA
Input Voltage Range	$V_S = \pm15V$		±13		V
	$V^+ = 5V$, $V^- = 0$	1		3	V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -10$ mV, $I_{SINK} \leq 3.2$ mA		0.3	0.4	V
Differential Input Voltage				±5	V
Positive Supply Current	$T_A = 25°C$, $V^+ = 5V$, $V^- = 0$		4.3		mA
Positive Supply Current	$T_A = 25°C$ $V_S = \pm15V$		8	12.5	mA
Negative Supply Current	$T_A = 25°C$ $V_S = \pm15V$		3	5	mA

Note 1: For supply voltages less than ±15V the absolute maximum input voltage is equal to the supply voltage.

Note 2: The maximum junction temperature of the LM319 is 85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

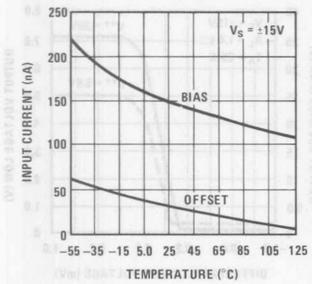
Note 3: These specifications apply for $V_S = \pm15V$ and $0°C \leq T_A \leq 70°C$, unless otherwise stated. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

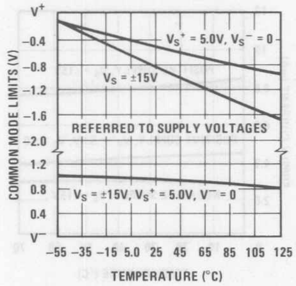
Note 5: The response time specified is for a 100 mV input step with 5 mV overdrive.

Typical Performance Characteristics LM119/LM219

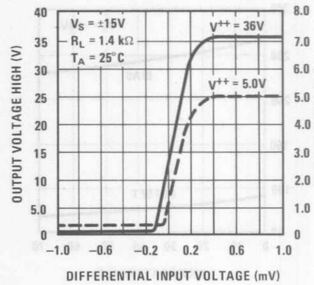
Input Currents



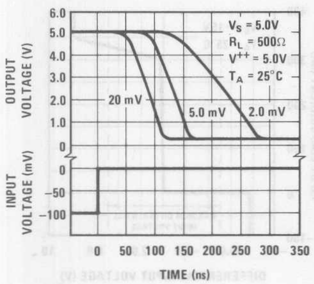
Common Mode Limits



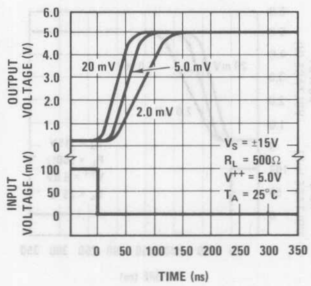
Transfer Function



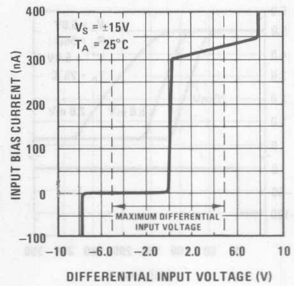
Response Time for Various Input Overdrives



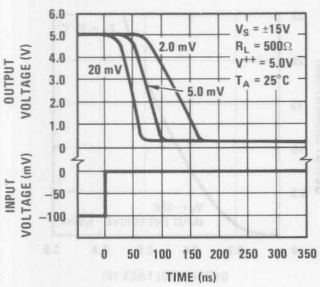
Response Time for Various Input Overdrives



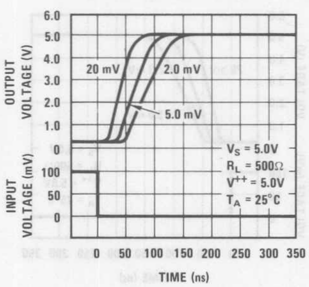
Input Characteristics



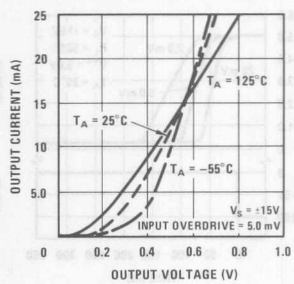
Response Time for Various Input Overdrives



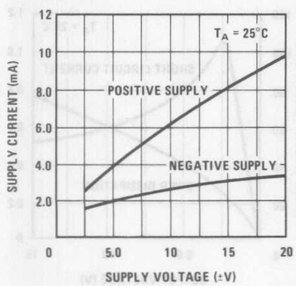
Response Time for Various Input Overdrives



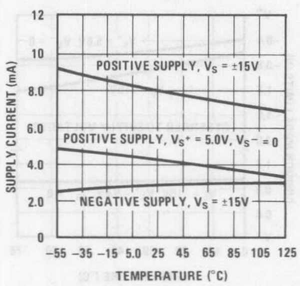
Output Saturation Voltage



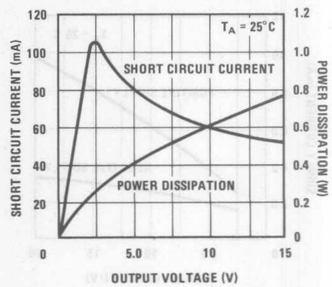
Supply Current



Supply Current

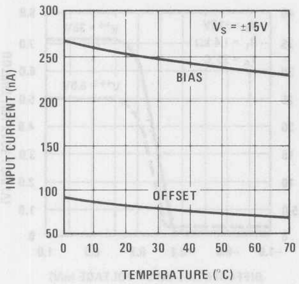


Output Limiting Characteristics

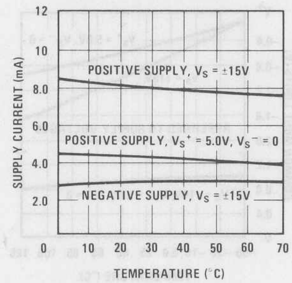


Typical Performance Characteristics LM319

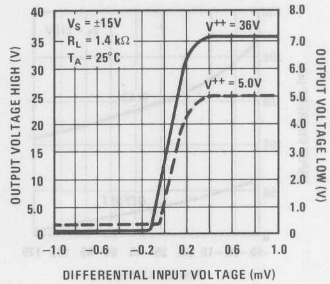
Input Currents



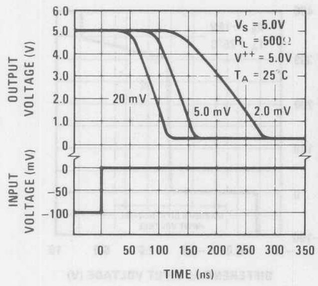
Supply Currents



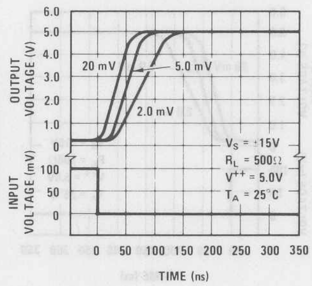
Transfer Function



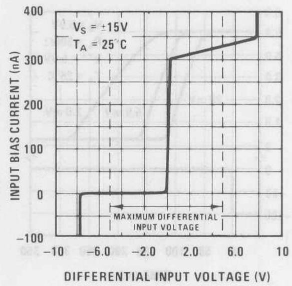
Response Time for Various Input Overdrives



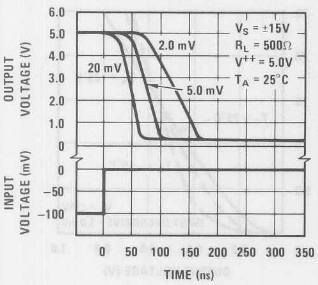
Response Time for Various Input Overdrives



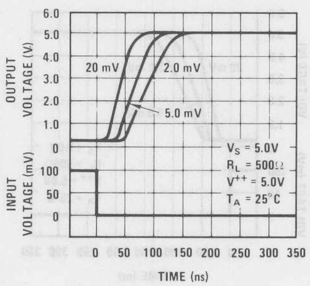
Input Characteristics



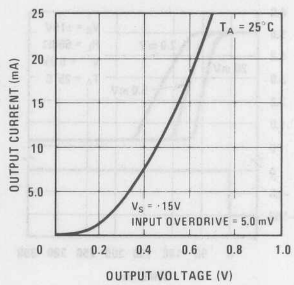
Response Time for Various Input Overdrives



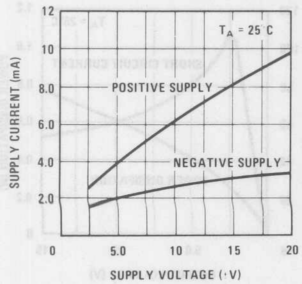
Response Time for Various Input Overdrives



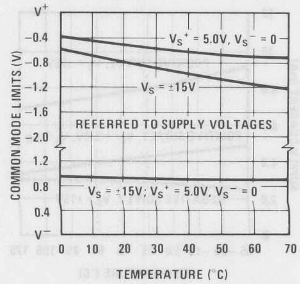
Output Saturation Voltage



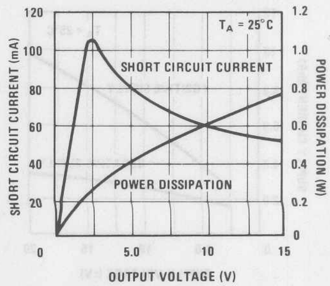
Supply Current



Common Mode Limits



Output Limiting Characteristics



Low Power Low Offset Voltage Quad Comparators

General Description

The LM139 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2 mV max for all four comparators. These were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, they will directly interface with MOS logic— where the low power drain of the LM339 is a distinct advantage over standard comparators.

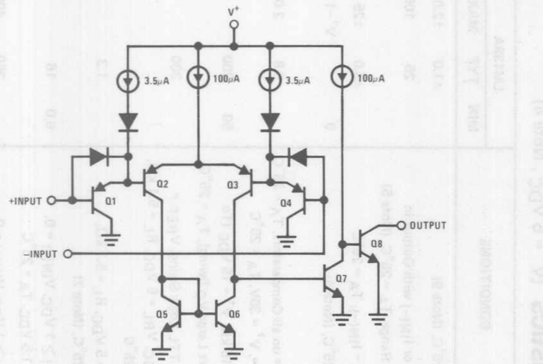
Advantages

- High precision comparators
- Reduced V_{OS} drift over temperature
- Eliminates need for dual supplies
- Allows sensing near gnd
- Compatible with all forms of logic
- Power drain suitable for battery operation

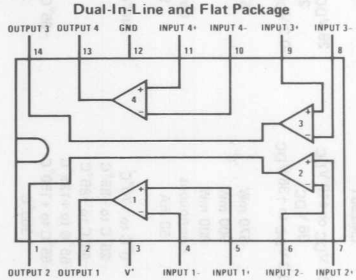
Features

- Wide single supply voltage range or dual supplies
  - LM139 series, 2 V_{DC} to 36 V_{DC} or
  - LM139A series, LM2901 ±1 V_{DC} to ±18 V_{DC}
  - LM3302 2 V_{DC} to 28 V_{DC} or ±1 V_{DC} to ±14 V_{DC}
- Very low supply current drain (0.8 mA) – independent of supply voltage (2 mW/comparator at +5 V_{DC})
- Low input biasing current 25 nA
- Low input offset current ±5 nA and offset voltage ±3 mV
- Input common-mode voltage range includes gnd
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage 250 mV at 4 mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

Schematic and Connection Diagrams



Dual-In-Line and Flat Package

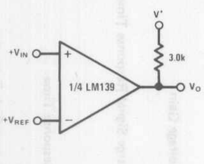


TOP VIEW

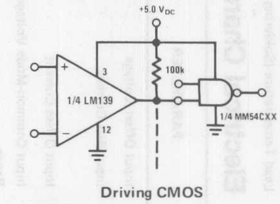
Order Number LM139J, LM139AJ, LM239J, LM239AJ, LM339J, LM339AJ, LM2901J or LM3302J
See NS Package J14A

Order Number LM339N, LM339AN, LM2901N or LM3302N
See NS Package N14A

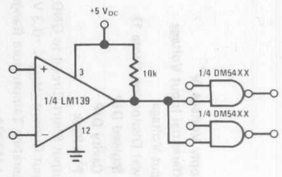
Typical Applications ($V^+ = 5.0\ V_{DC}$)



Basic Comparator



Driving CMOS



Driving TTL

Absolute Maximum Ratings

	LM139/LM239/LM339 LM139A/LM239A/LM339A LM2901	LM3302
Supply Voltage, V^+	36 V_{DC} or ±18 V_{DC}	28 V_{DC} or ±14 V_{DC}
Differential Input Voltage	36 V_{DC}	28 V_{DC}
Input Voltage	−0.3 V_{DC} to +36 V_{DC}	−0.3 V_{DC} to +28 V_{DC}
Power Dissipation (Note 1)		
Molded DIP	570 mW	570 mW
Cavity DIP	900 mW	
Flat Pack	800 mW	
Output Short-Circuit to GND, (Note 2)	Continuous	Continuous
Input Current ($V_{IN} < -0.3\ V_{DC}$), (Note 3)	50 mA	50 mA
Operating Temperature Range		
LM339A	0°C to +70°C	−40°C to +85°C
LM239A	−25°C to +85°C	
LM2901	−40°C to +85°C	
LM139A	−55°C to +125°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

Electrical Characteristics ($V^+ = 5\ V_{DC}$, Note 4)

PARAMETER	CONDITIONS	LM139A			LM239A, LM339A			LM139			LM239, LM339			LM2901			LM3302			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$, (Note 9)		±1.0	±2.0		±1.0	±2.0		±2.0	±5.0		±2.0	±5.0		±2.0	±7.0		±3	±20	mV_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, $T_A = 25°C$, (Note 5)		25	100		25	250		25	100		25	250		25	250		25	500	nA_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $T_A = 25°C$		±3.0	±25		±5.0	±50		±3.0	±25		±5.0	±50		±5	±50		±3	±100	nA_{DC}
Input Common-Mode Voltage Range	$T_A = 25°C$, (Note 6)	0		V^+−1.5	0		V^+−1.5	0		V^+−1.5	0		V^+−1.5	0		V^+−1.5	0		V^+−1.5	V_{DC}
Supply Current	$R_L = \infty$ on all Comparators, $T_A = 25°C$		0.8	2.0		0.8	2.0		0.8	2.0		0.8	2.0		0.8	2.0		0.8	2	mA_{DC}
	$R_L = \infty$, $V^+ = 30V$, $T_A = 25°C$														1	2.5				mA_{DC}
Voltage Gain	$R_L \geq 15\ k\Omega$, $V^+ = 15\ V_{DC}$ (To Support Large V_O Swing), $T_A = 25°C$	50	200		50	200			200			200		25	100		2	30		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, $V_{REF} = 1.4\ V_{DC}$, $V_{RL} = 5\ V_{DC}$, $R_L = 5.1\ k\Omega$, $T_A = 25°C$		300			300			300			300			300			300		ns
Response Time	$V_{RL} = 5\ V_{DC}$, $R_L = 5.1\ k\Omega$, $T_A = 25°C$, (Note 7)		1.3			1.3			1.3			1.3			1.3			1.3		µs
Output Sink Current	$V_{IN(-)} \geq 1\ V_{DC}$, $V_{IN(+)} = 0$, $V_O \leq 1.5\ V_{DC}$, $T_A = 25°C$	6.0	16		6.0	16		6.0	16		6.0	16		6.0	16		6.0	16		mA_{DC}
Saturation Voltage	$V_{IN(-)} \geq 1\ V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4$ mA, $T_A = 25°C$		250	400		250	400		250	400		250	400			400		250	500	mV_{DC}
Output Leakage Current	$V_{IN(+)} \geq 1\ V_{DC}$, $V_{IN(-)} = 0$, $V_O = 5\ V_{DC}$, $T_A = 25°C$		0.1			0.1			0.1			0.1			0.1			0.1		nA_{DC}

Electrical Characteristics (Continued)

PARAMETER	CONDITIONS	LM139A			LM239A, LM339A			LM139			LM239, LM339			LM2901			LM3302			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	(Note 9)			4.0			4.0			9.0			9.0		9	15			40	mV_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			±100			±150			±100			±150		50	200			300	nA_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range			300			400			300			400		200	500			1000	nA_{DC}
Input Common-Mode Voltage Range		0		V^+–2.0	0		V^+–2.0	0		V^+–2.0	0		V^+–2.0	0		V^+–2.0	0		V^+–2.0	V_{DC}
Saturation Voltage	$V_{IN(-)} \geq 1\ V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4$ mA			700			700			700			700		400	700			700	mV_{DC}
Output Leakage Current	$V_{IN(+)} \geq 1\ V_{DC}$, $V_{IN(-)} = 0$, $V_O = 30\ V_{DC}$			1.0			1.0			1.0			1.0			1.0			1.0	μA_{DC}
Differential Input Voltage	Keep all V_{IN}'s $\geq 0\ V_{DC}$ (or V^-, if used), (Note 8)			36			36			36			36	0		36			28	V_{DC}

Note 1: For operating at high temperatures, the LM339/LM339A, LM2901, LM3302 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM239 and LM139 must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small ($P_D \leq 100$ mW), provided the output transistors are allowed to saturate.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA independent of the magnitude of V^+.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3\ V_{DC}$ (at 25°C).

Note 4: These specifications apply for $V^+ = 5\ V_{DC}$ and $-55°C \leq T_A \leq +125°C$, unless otherwise stated. With the LM239/LM239A, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$, the LM339/LM339A temperature specifications are limited to $0°C \leq T_A \leq +70°C$, and the LM2901, LM3302 temperature range is $-40°C \leq T_A \leq +85°C$.

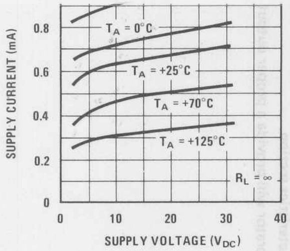
Note 5: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

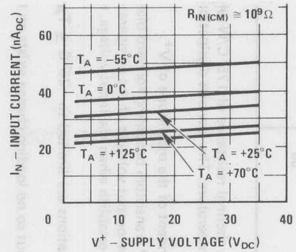
Note 6: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V^+ –1.5V, but either or both inputs can go to +30 V_{DC} without damage (25V for LM3302).

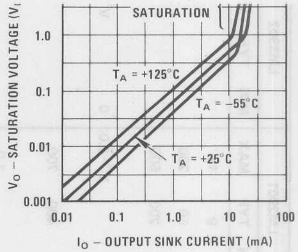
Note 7: The response time specified is a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section.

Note 8: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3\ V_{DC}$ (or 0.3 V_{DC} below the magnitude of the negative power supply, if used) (at 25°C).

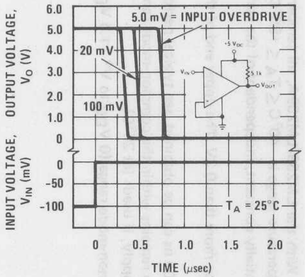
Note 9: At output switch point, $V_O \cong 1.4\ V_{DC}$, $R_S = 0\Omega$ with V^+ from 5 V_{DC}; and over the full input common-mode range (0 V_{DC} to V^+ –1.5 V_{DC}).



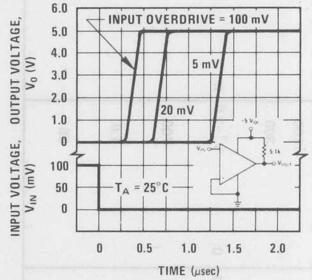




Response Time for Various Input Overdrives — Negative Transition

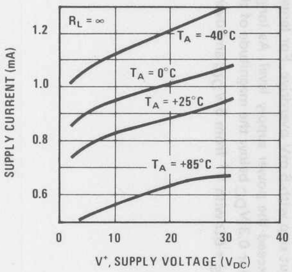


Response Time for Various Input Overdrives — Positive Transition

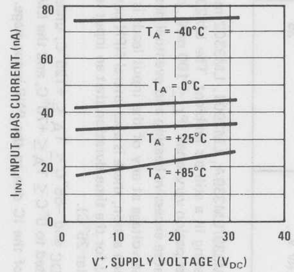


Typical Performance Characteristics LM2901

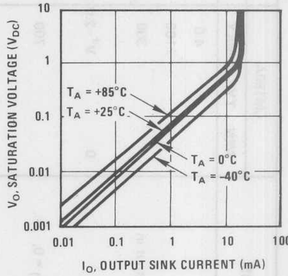
Supply Current



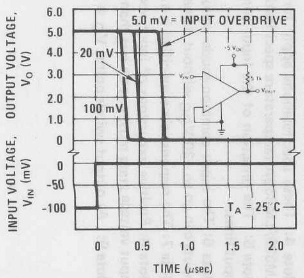
Input Current



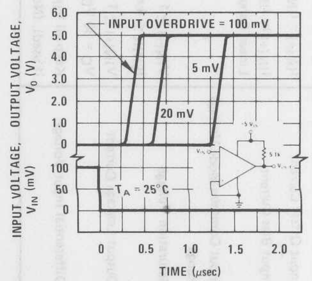
Output Saturation Voltage



Response Time for Various Input Overdrives—Negative Transition



Response Time for Various Input Overdrives—Positive Transition



The LM139 series are high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to $< 10\ k\Omega$ reduces the feedback signal levels and finally, adding even a small amount (1 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be grounded.

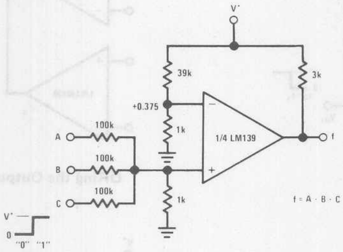
The bias network of the LM139 series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2 V_{DC} to 30 V_{DC}.

It is usually unnecessary to use a bypass capacitor across the power supply line.

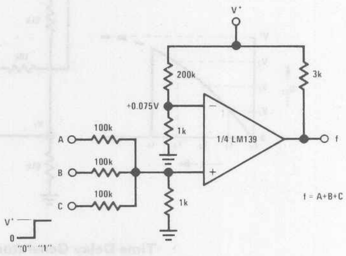
The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than $-0.3\ V_{DC}$ (at 25°C). An input clamp diode can be used as shown in the applications section.

The output of the LM139 series is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the LM139A package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60Ω r_{sat} of the output transistor. The low offset voltage of the output transistor (1 mV) allows the output to clamp essentially to ground level for small load currents.

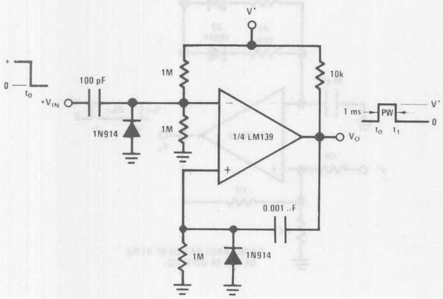
Typical Applications ($V^+ = 15\ V_{DC}$)



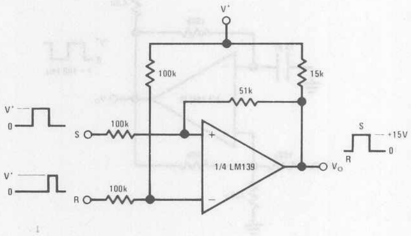
AND Gate



OR Gate

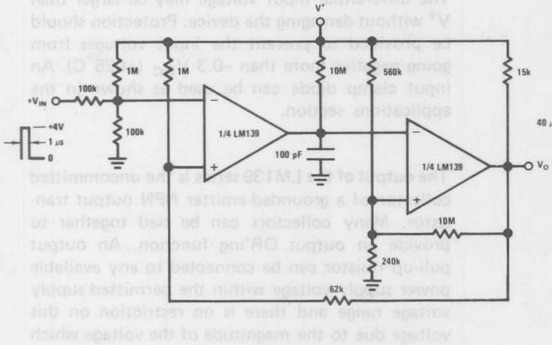


One-Shot Multivibrator

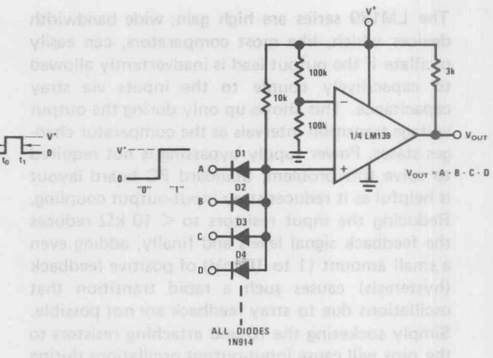


Bi-Stable Multivibrator

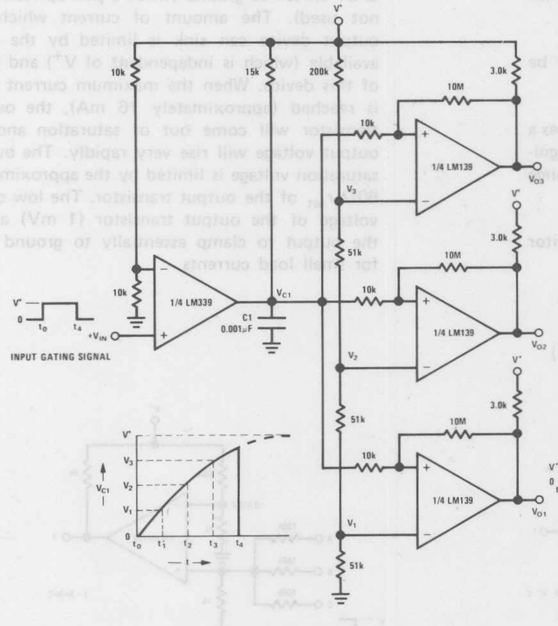
Typical Applications (Continued) ($V^+ = 15\ V_{DC}$)



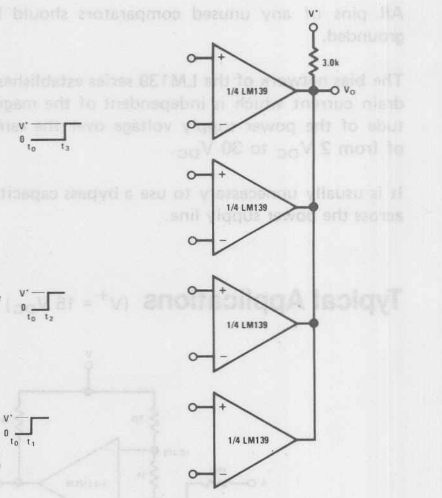
One-Shot Multivibrator with Input Lock Out



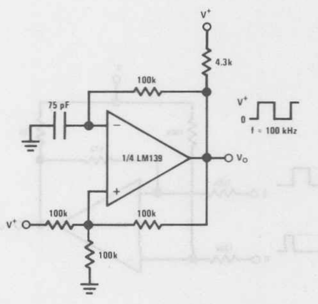
Large Fan-in AND Gate



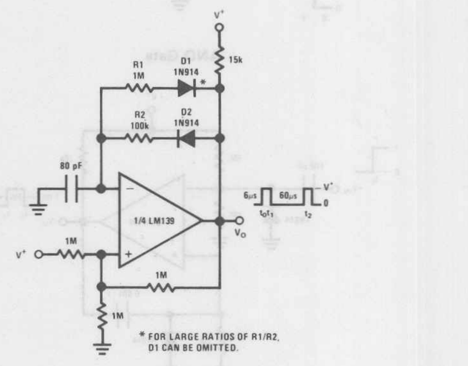
Time Delay Generator



ORing the Outputs

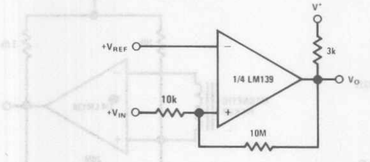


Squarewave Oscillator

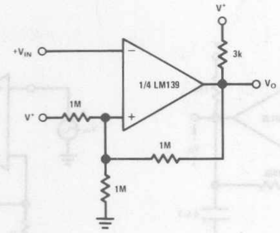


Pulse Generator

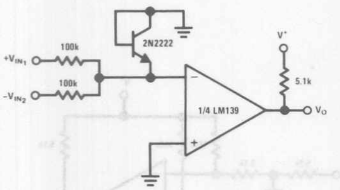
Typical Applications (Continued) ($V^+ = 5\ V_{DC}$)



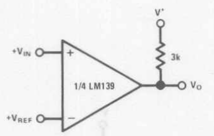
Non-Inverting Comparator with Hysteresis



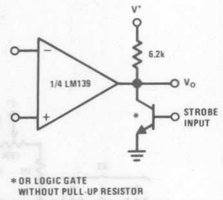
Inverting Comparator with Hysteresis



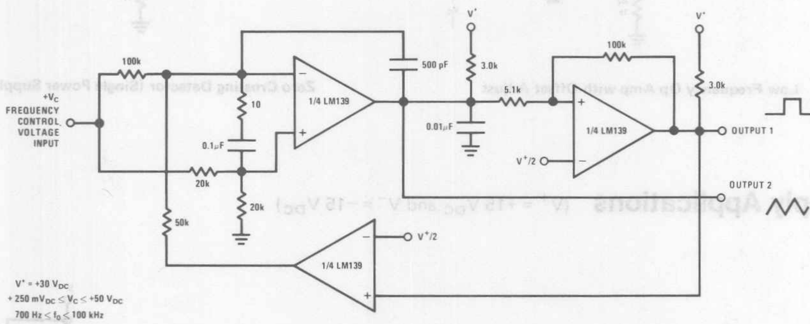
Comparing Input Voltages of Opposite Polarity



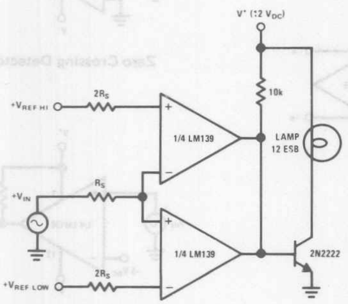
Basic Comparator



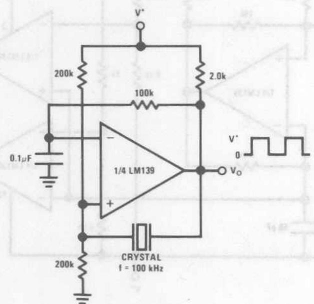
Output Strobing



Two-Decade High-Frequency VCO

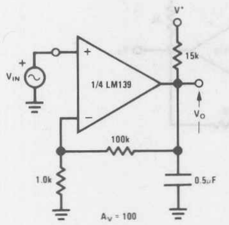


Limit Comparator

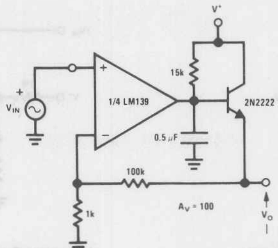


Crystal Controlled Oscillator

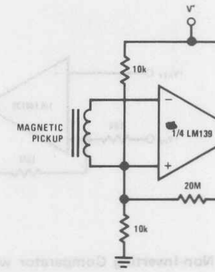
Typical Applications (Continued) ($V^+ = 5\ V_{DC}$)



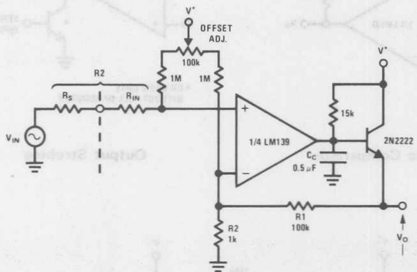
Low Frequency Op Amp



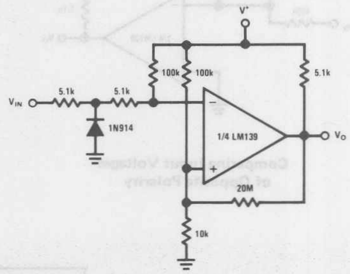
Low Frequency Op Amp (V_O = 0V for V_{IN} = 0V)



Transducer Amplifier

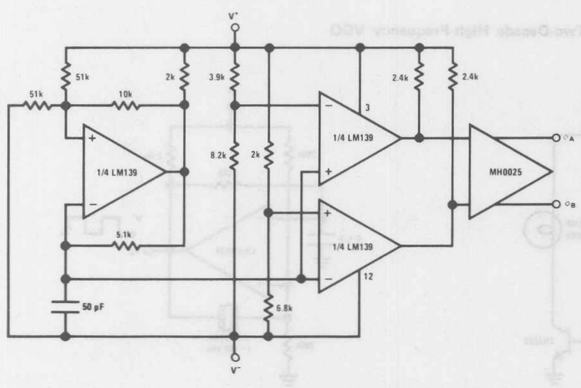


Low Frequency Op Amp with Offset Adjust

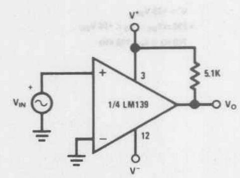


Zero Crossing Detector (Single Power Supply)

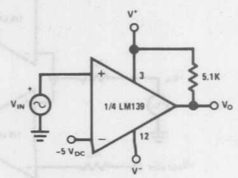
Split-Supply Applications ($V^+ = +15\ V_{DC}$ and $V^- = -15\ V_{DC}$)



MOS Clock Driver



Zero Crossing Detector



Comparator With a Negative Reference

LM160/LM260/LM360 High Speed Differential Comparator

General Description

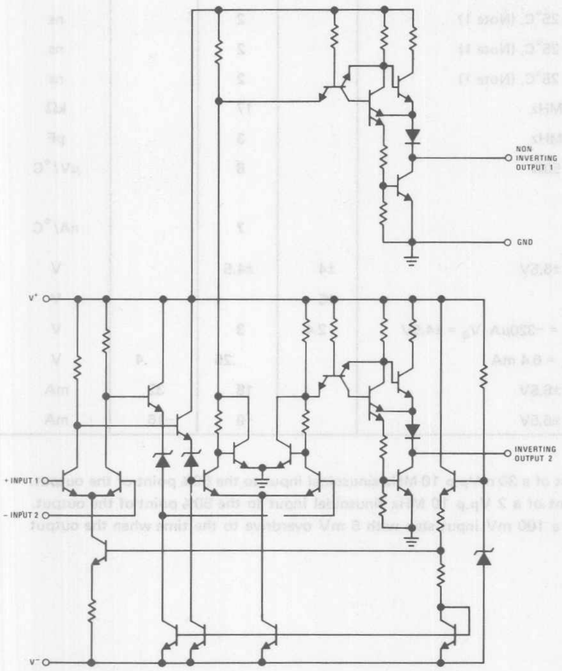
The LM160/LM260/LM360 is a very high speed differential input, complementary TTL output voltage comparator with improved characteristics over the μA760/μA760C, for which it is a pin-for-pin replacement. The device has been optimized for greater speed, input impedance and fan-out, and lower input offset voltage. Typically delay varies only 3 ns for overdrive variations of 5 mV to 500 mV.

Complementary outputs having minimum skew are provided. Applications involve high speed analog to digital convertors and zero-crossing detectors in disc file systems.

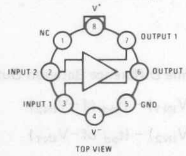
Features

- Guaranteed high speed 20 ns max
- Tight delay matching on both outputs
- Complementary TTL outputs
- High input impedance
- Low speed variation with overdrive variation
- Fan-out of 4
- Low input offset voltage
- Series 74 TTL compatible

Schematic and Connection Diagrams

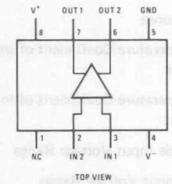


Metal Can Package



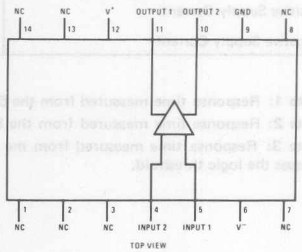
Order Number LM160H, LM260H or LM360H
See NS Package H08C

Dual-In-Line Package



Order Number LM360N
See NS Package N08B

Dual-In-Line Package



Order Number LM360N-14
See NS Package N14A
Order Number LM160J-14, LM260J-14
See NS Package J14A

Positive Supply Voltage	+8V
Negative Supply Voltage	−8V
Peak Output Current	20 mA
Differential Input Voltage	±5V
Input Voltage	$V^+ \geq V_{IN} \geq V^-$
Operating Temperature Range	
LM160	−55°C to +125°C
LM260	−25°C to +85°C
LM360	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics ($T_{MIN} \leq T_A \leq T_{MAX}$)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Conditions					
Supply Voltage $V_{CC}{}^+$		4.5	5	6.5	V
Supply Voltage $V_{CC}{}^-$		−4.5	−5	−6.5	V
Input Offset Voltage	$R_S \leq 200\Omega$		2	5	mV
Input Offset Current			.5	3	μA
Input Bias Current			5	20	μA
Output Resistance (Either Output)	$V_{OUT} = V_{OH}$		100		Ω
Response Time	$T_A = 25°C, V_S = \pm5V$ (Note 1)		13	25	ns
	$T_A = 25°C, V_S = \pm5V$ (Note 2)		12	20	ns
	$T_A = 25°C, V_S = \pm5V$ (Note 3)		14		ns
Response Time Difference Between Outputs					
(t_{pd} of $+V_{IN1}$) − (t_{pd} of $-V_{IN2}$)	$T_A = 25°C$, (Note 1)		2		ns
(t_{pd} of $+V_{IN2}$) − (t_{pd} of $-V_{IN1}$)	$T_A = 25°C$, (Note 1)		2		ns
(t_{pd} of $+V_{IN1}$) − (t_{pd} of $+V_{IN2}$)	$T_A = 25°C$, (Note 1)		2		ns
(t_{pd} of $-V_{IN1}$) − (t_{pd} of $-V_{IN2}$)	$T_A = 25°C$, (Note 1)		2		ns
Input Resistance	f = 1 MHz		17		kΩ
Input Capacitance	f = 1 MHz		3		pF
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\Omega$		8		μV/°C
Average Temperature Coefficient of Input Offset Current			7		nA/°C
Common Mode Input Voltage Range	$V_S = \pm6.5V$	±4	±4.5		V
Differential Input Voltage Range		±5			V
Output High Voltage (Either Output)	$I_{OUT} = -320\mu A, V_S = \pm4.5V$	2.4	3		V
Output Low Voltage (Either Output)	$I_{SINK} = 6.4$ mA		.25	.4	V
Positive Supply Current	$V_S = \pm6.5V$		18	32	mA
Negative Supply Current	$V_S = \pm6.5V$		−9	−16	mA

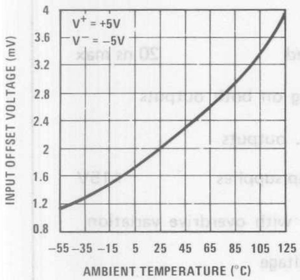
Note 1: Response time measured from the 50% point of a 30 mV$_{P-P}$ 10 MHz sinusoidal input to the 50% point of the output.

Note 2: Response time measured from the 50% point of a 2 V$_{P-P}$ 10 MHz sinusoidal input to the 50% point of the output.

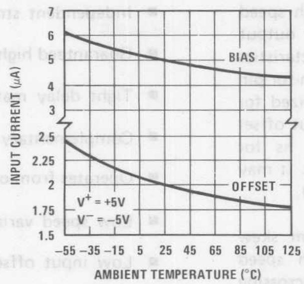
Note 3: Response time measured from the start of a 100 mV input step with 5 mV overdrive to the time when the output crosses the logic threshold.

Typical Performance Characteristics

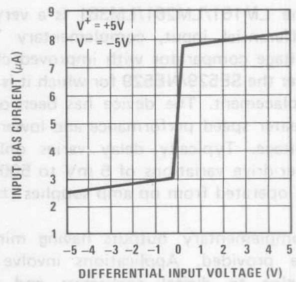
Offset Voltage



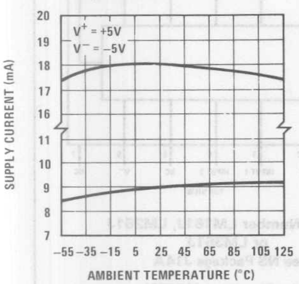
Input Currents vs Ambient Temperature



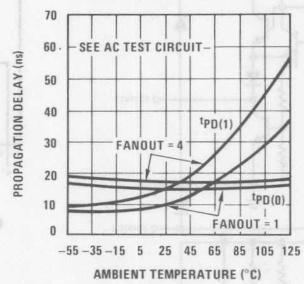
Input Characteristics



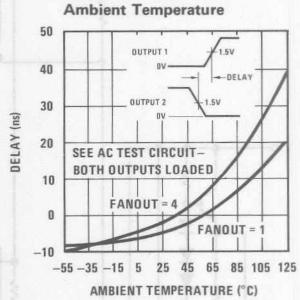
Supply Current vs Ambient Temperature



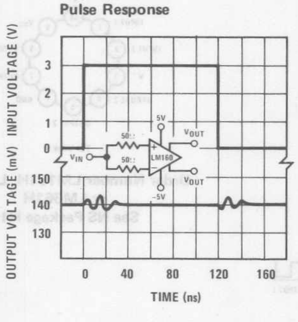
Propagation Delay vs Ambient Temperature



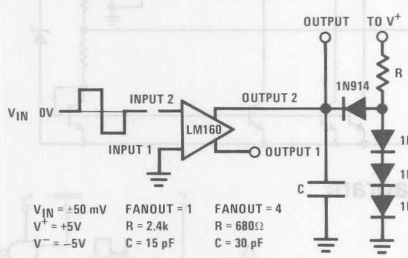
Delay of Output 1 With Respect to Output 2 vs Ambient Temperature



Common-Mode Pulse Response



AC Test Circuit



National Semiconductor

Voltage Comparators

LM161/LM261/LM361 High Speed Differential Comparators

General Description

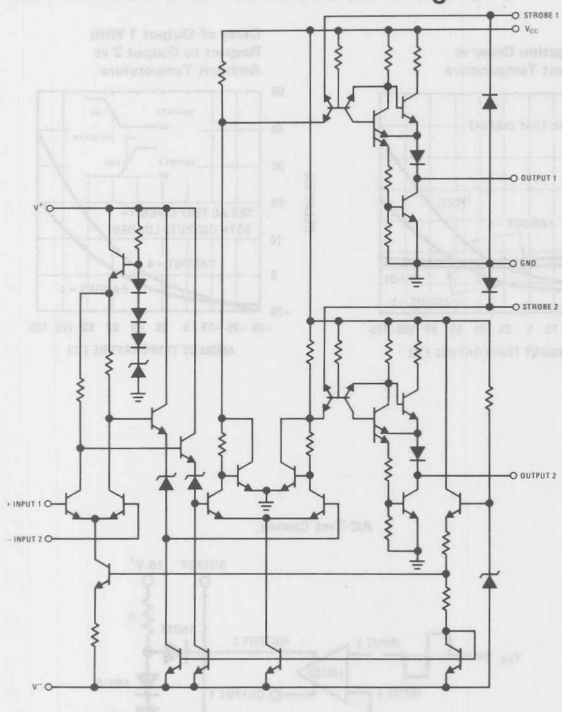
The LM161/LM261/LM361 is a very high speed differential input, complementary TTL output voltage comparator with improved characteristics over the SE529/NE529 for which it is a pin-for-pin replacement. The device has been optimized for greater speed performance and lower input offset voltage. Typically delay varies only 3 ns for over-drive variations of 5 mV to 500 mV. It may be operated from op amp supplies (±15V).

Complementary outputs having minimum skew are provided. Applications involve high speed analog to digital converters and zero-crossing detectors in disc file systems.

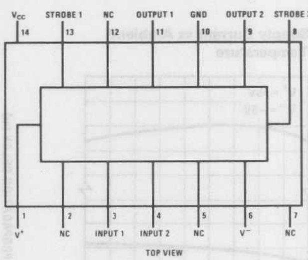
Features

- Independent strobes
- Guaranteed high speed 20 ns max
- Tight delay matching on both outputs
- Complementary TTL outputs
- Operates from op amp supplies ±15V
- Low speed variation with overdrive variation
- Low input offset voltage
- Versatile supply voltage range

Schematic and Connection Diagrams

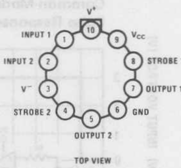


Dual-In-Line Package



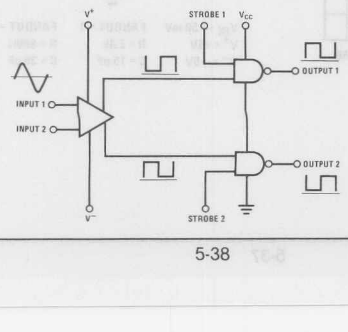
Order Number LM161J, LM261J or LM361J
See NS Package J14A
Order Number LM361N
See NS Package N14A

Metal Can Package



Order Number LM161H, LM261H or LM361H
See NS Package H10C

Logic Diagram



Absolute Maximum Ratings

Positive Supply Voltage, V^+	+16V
Negative Supply Voltage, V^-	−16V
Gate Supply Voltage, V_{CC}	+7V
Output Voltage	+7V
Differential Input Voltage	±5V
Input Common Mode Voltage	±6V
Power Dissipation	600 mW
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	T_{MIN} T_{MAX}
LM161	−55°C to +125°C
LM261	−25°C to +85°C
LM361	0°C to +70°C
Lead Temperature (Soldering, 10 sec)	300°C
For Any Device Lead Below V^-	0.3V

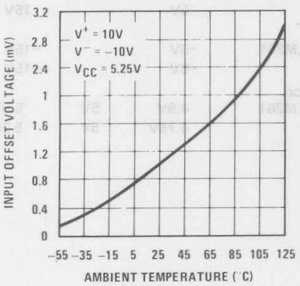
Operating Conditions

	MIN	TYP	MAX
Supply Voltage V^+			
LM161/LM261	5V		15V
LM361	5V		15V
Supply Voltage V^-			
LM161/LM261	−6V		−15V
LM361	−6V		−15V
Supply Voltage V_{CC}			
LM161/LM261	4.5V	5V	5.5V
LM361	4.75V	5V	5.25V

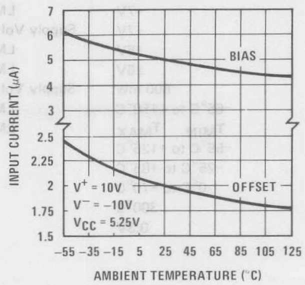
Electrical Characteristics ($V^+ = +10V$, $V_{CC} = +5V$, $V^- = -10V$, $T_{MIN} \leq T_A \leq T_{MAX}$, unless noted)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LM161/LM261			LM361			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage			1	3		1	5	mV
Input Bias Current	$T_A = 25°C$		5	20		10	30	μA μA
Input Offset Current	$T_A = 25°C$		2	3		2	5	μA μA
Voltage Gain	$T_A = 25°C$		3			3		V/mV
Input Resistance	$T_A = 25°C$, f = 1 kHz		20			20		kΩ
Logical "1" Output Voltage	$V_{CC} = 4.75V$, $I_{SOURCE} = -.5$ mA	2.4	3.3		2.4	3.3		V
Logical "0" Output Voltage	$V_{CC} = 4.75V$, $I_{SINK} = 6.4$ mA			.4			.4	V
Strobe Input "1" Current	$V_{CC} = 5.25V$, $V_{STROBE} = 2.4V$			200			200	μA
Strobe Input "0" Current	$V_{CC} = 5.25V$, $V_{STROBE} = .4V$			−1.6			−1.6	mA
Strobe Input "0" Voltage	$V_{CC} = 4.75V$			.8			.8	V
Strobe Input "1" Voltage	$V_{CC} = 4.75V$	2			2			V
Output Short Circuit Current	$V_{CC} = 5.25V$, $V_{OUT} = 0V$	18		55	18		55	mA
Supply Current I^+	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $-55°C \leq T_A \leq 125°C$			4.5				mA
Supply Current I^+	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $0°C \leq T_A \leq 70°C$						5	mA
Supply Current I^-	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $55°C \leq T_A \leq 125°C$			10				mA
Supply Current I^-	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $0°C \leq T_A \leq 70°C$						10	mA
Supply Current I_{CC}	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $-55°C \leq T_A \leq 125°C$			18				mA
Supply Current I_{CC}	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $0°C \leq T_A \leq 70°C$						20	mA
TRANSIENT RESPONSE	$V_{IN} = 50$ mV Overdrive							
Propagation Delay Time ($t_{pd(0)}$)	$T_A = 25°C$		14	20		14	20	ns
Propagation Delay Time ($t_{pd(1)}$)	$T_A = 25°C$		14	20		14	20	ns
Delay Between Output A and B	$T_A = 25°C$		2	5		2	5	ns
Strobe Delay Time ($t_{pd(0)}$)	$T_A = 25°C$		8			8		ns
Strobe Delay Time ($t_{pd(1)}$)	$T_A = 25°C$		8			8		ns

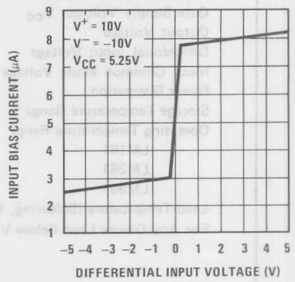
Offset Voltage



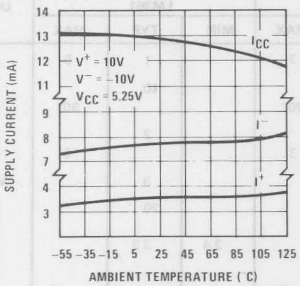
Temperature



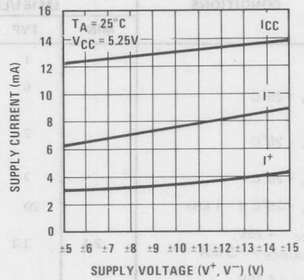
Input Characteristics



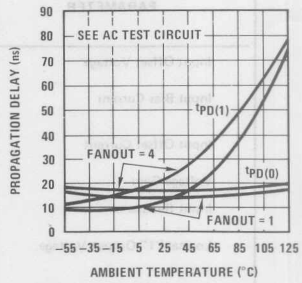
Supply Current vs Ambient Temperature



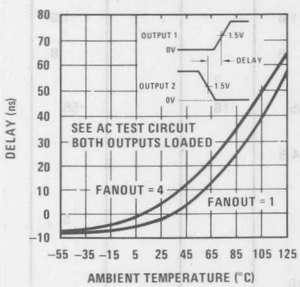
Supply Current vs Supply Voltage



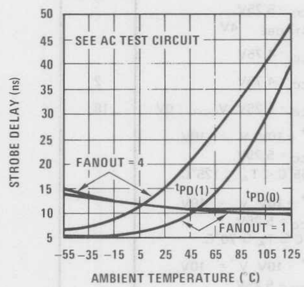
Propagation Delay vs Ambient Temperature



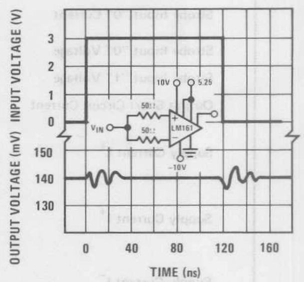
Delay of Output 1 With Respect to Output 2 vs Ambient Temperature



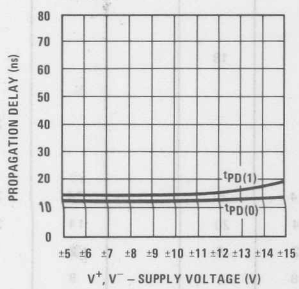
Strobe Delay vs Ambient Temperature



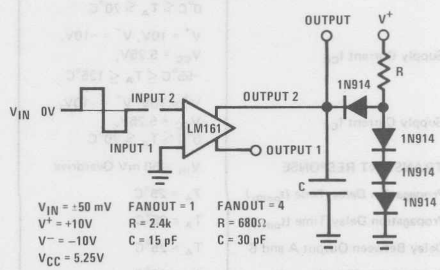
Common-Mode Pulse Response



Propagation Delay vs Supply Voltage



AC Test Circuit



National Semiconductor

Voltage Comparators

LM193/LM293/LM393, LM193A/LM293A/LM393A, LM2903 Low Power Low Offset Voltage Dual Comparators

General Description

The LM193 series consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0 mV max for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM193 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM193 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

Advantages

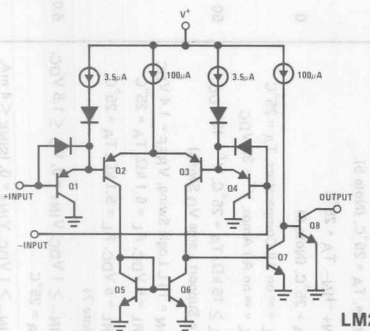
- High precision comparators
- Reduced V_{OS} drift over temperature
- Eliminates need for dual supplies
- Allows sensing near ground
- Compatible with all forms of logic
- Power drain suitable for battery operation

Features

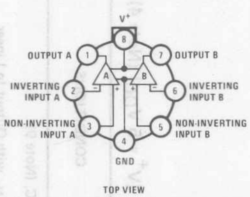
- Wide single supply
  Voltage range $2.0\ V_{DC}$ to $36\ V_{DC}$
  or dual supplies $\pm 1.0\ V_{DC}$ to $\pm 18\ V_{DC}$
- Very low supply current drain (0.8 mA)—independent of supply voltage (1.0 mW/comparator at $5.0\ V_{DC}$)
- Low input biasing current 25 nA
- Low input offset current ±5 nA
  and maximum offset voltage ±3 mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage 250 mV at 4 mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

5

Schematic and Connection Diagrams

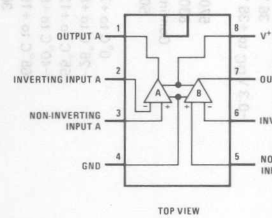


Metal Can Package



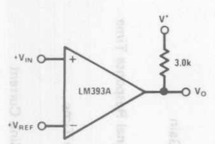
Order Number LM193H, LM193AH, LM293H, LM293AH, LM393H or LM393AH
See NS Package H08C

Dual-In-Line Package

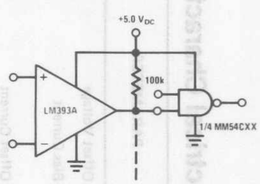


Order Number LM393N, LM393AN, or LM2903N
See NS Package N08B

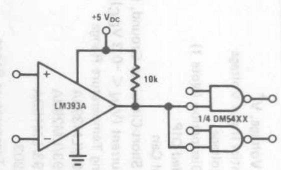
Typical Applications ($V^+ = 5.0\ V_{DC}$)



Basic Comparator



Driving CMOS



Driving TTL

Absolute Maximum Ratings

Supply Voltage, V^+	36 V_{DC} or ±18 V_{DC}
Differential Input Voltage	36 V_{DC}
Input Voltage	−0.3 V_{DC} to +36 V_{DC}
Power Dissipation (Note 1)	
Molded DIP	570 mW
Metal Can	830 mW
Output Short-Circuit to Ground, (Note 2)	Continuous
Input Current ($V_{IN} < -0.3\ V_{DC}$), (Note 3)	50 mA
Operating Temperature Range	
LM393/LM393A	0°C to +70°C
LM293/LM293A	−25°C to +85°C
LM193/LM193A	−55°C to +125°C
LM2903	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics ($V^+ = 5\ V_{DC}$) (Note 4)

PARAMETER	CONDITIONS	LM193A			LM293A, LM393A			LM193			LM293, LM393			LM2903			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$, (Note 9)		±1.0	±2.0		±1.0	±2.0		±1.0	±5.0		±1.0	±5.0		±2.0	±7.0	mV_{DC}
Input Bias Current	I_{IN+} or I_{IN-} with Output In Linear Range, $T_A = 25°C$, (Note 5)		25	100		25	250		25	100		25	250		25	250	nA_{DC}
Input Offset Current	$I_{IN+} - I_{IN-}$, $T_A = 25°C$		±3.0	±25		±5.0	±50		±3.0	±25		±5.0	±50		±5.0	±50	nA_{DC}
Input Common-Mode Voltage Range	$T_A = 25°C$, (Note 6)	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	V_{DC}
Supply Current	$R_L = \infty$ on All Comparators, $T_A = 25°C$		0.4	1		0.4	1		0.4	1		0.4	1		0.4	1.0	mA_{DC}
	$R_L = \infty$ on All Amps, $V^+ = 30\ V_{DC}$		1	2.5		1	2.5			2.5			2.5		1	2.5	mA_{DC}
Voltage Gain	$R_L \geq 15\ k\Omega$, $T_A = 25°C$, $V^+ = 15\ V_{DC}$ (To Support Large V_O Swing)	50	200		50	200		50	200		50	200		25	100		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, $V_{REF} = 1.4\ V_{DC}$, $V_{RL} = 5\ V_{DC}$, $R_L = 5.1\ k\Omega$, $T_A = 25°C$		300			300			300			300			300		ns
Response Time	$V_{RL} = 5\ V_{DC}$, $R_L = 5.1\ k\Omega$, $T_A = 25°C$, (Note 7)		1.3			1.3			1.3			1.3			1.5		µs
Output Sink Current	$V_{IN-} \geq 1\ V_{DC}$, $V_{IN+} = 0$, $V_O \leq 1.5\ V_{DC}$, $T_A = 25°C$	6.0	16		6.0	16		6.0	16		6.0	16		6	16		mA_{DC}
Saturation Voltage	$V_{IN-} \geq 1\ V_{DC}$, $V_{IN+} = 0$, $I_{SINK} \leq 4$ mA, $T_A = 25°C$		250	400		250	400		250	400		250	400			400	mV_{DC}
Output Leakage Current	$V_{IN-} = 0$, $V_{IN+} \geq 1\ V_{DC}$, $V_O = 5\ V_{DC}$, $T_A = 25°C$		0.1			0.1			0.1			0.1			0.1		nA_{DC}

Electrical Characteristics (Continued)

PARAMETER	CONDITIONS	LM193A			LM293A, LM393A			LM193			LM293, LM393			LM2903			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	(Note 9)			4.0			4.0			9			9		9	15	mV_{DC}
Input Offset Current	$I_{IN+} - I_{IN-}$			±100			±150			±100			±150		50	200	nA_{DC}
Input Bias Current	I_{IN+} or I_{IN-} with Output in Linear Range			300			400			300			400		200	500	nA_{DC}
Input Common-Mode Voltage Range		0		$V^+-2.0$	0		$V^+-2.0$	0		$V^+-2.0$	0		$V^+-2.0$	0		V^+-20	V_{DC}
Saturation Voltage	$V_{IN-} \geq 1\ V_{DC}$, $V_{IN+} = 0$, $I_{SINK} \leq 4$ mA,			700			700			700			700		400	700	mV_{DC}
Output Leakage Current	$V_{IN-} = 0$, $V_{IN+} \geq 1\ V_{DC}$, $V_O = 30\ V_{DC}$,			1.0			1.0			1.0			1.0			1.0	μA_{DC}
Differential Input Voltage	Keep All V_{IN}'s $\geq 0\ V_{DC}$ (or V^-, if Used), (Note 8)			36			36			36			36			28	V_{DC}

Note 1: For operating at high temperatures, the LM393/LM393A and LM2903 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM193/LM193A/LM293/LM293A must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small ($P_D \leq 100$ mW), provided the output transistors are allowed to saturate.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA independent of the magnitude of V^+.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3\ V_{DC}$.

Note 4: These specifications apply for $V^+ = 5\ V_{DC}$ and $-55°C \leq T_A \leq +125°C$, unless otherwise stated. With the LM293/LM293A all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$ and the LM393/LM393A temperature specifications are limited to $0°C \leq T_A \leq +70°C$. The LM2903 is limited to $-40°C \leq T_A \leq +85°C$.

Note 5: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

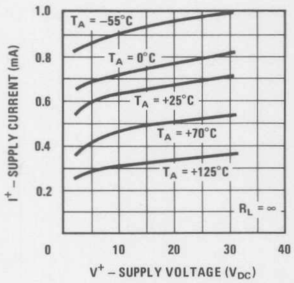
Note 6: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+ -1.5V$, but either or both inputs can go to 30 V_{DC} without damage.

Note 7: The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section.

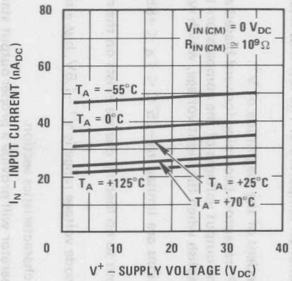
Note 8: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3\ V_{DC}$ (or 0.3 V_{DC} below the magnitude of the negative power supply, if used).

Note 9: At output switch point, $V_O \cong 1.4\ V_{DC}$, $R_S = 0\Omega$ with V^+ from 5 V_{DC} to 30 V_{DC}; and over the full input common-mode range (0 V_{DC} to $V^+ -1.5\ V_{DC}$).

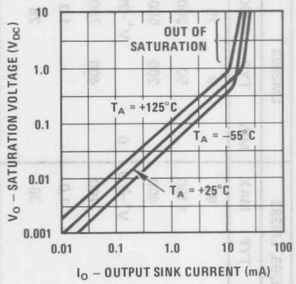
Supply Current



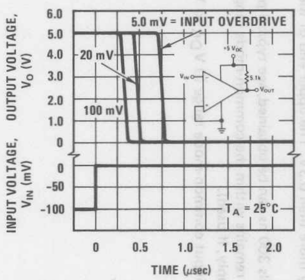
Input Current



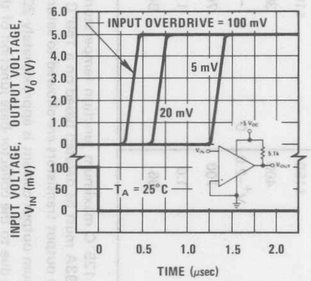
Output Saturation Voltage



Response Time for Various Input Overdrives – Negative Transition

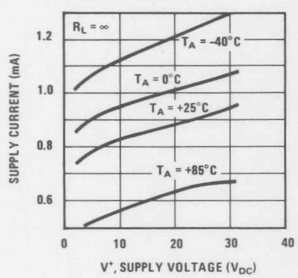


Response Time for Various Input Overdrives – Positive Transition

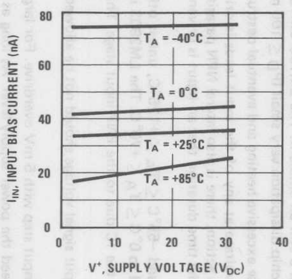


Typical Performance Characteristics LM2903

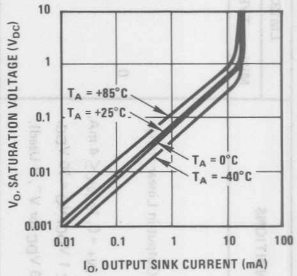
Supply Current



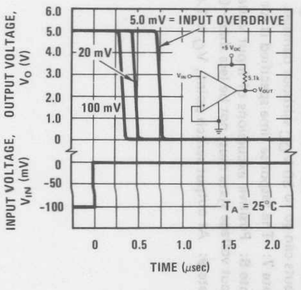
Input Current



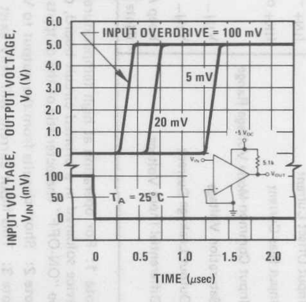
Output Saturation Voltage



Response Time for Various Input Overdrives–Negative Transition



Response Time for Various Input Overdrives–Positive Transition



Application Hints

The LM193 series are high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to $< 10\ k\Omega$ reduces the feedback signal levels and finally, adding even a small amount (1.0 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be grounded.

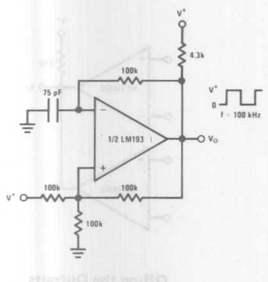
The bias network of the LM193 series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2.0 V_{DC} to 30 V_{DC}.

It is usually unnecessary to use a bypass capacitor across the power supply line.

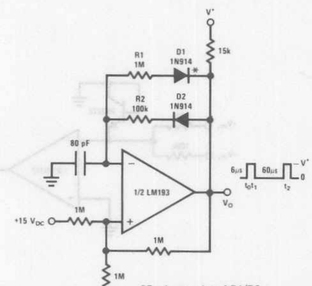
The differential input voltage may be larger than V^+ without damaging the device (see Note 8). Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode can be used as shown in the applications section.

The output of the LM193 series is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the LM193 package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60Ω r_{SAT} of the output transistor. The low offset voltage of the output transistor (1.0 mV) allows the output to clamp essentially to ground level for small load currents.

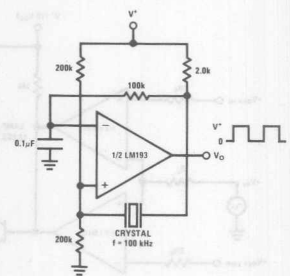
Typical Applications (Continued) ($V^+ = 15\ V_{DC}$)



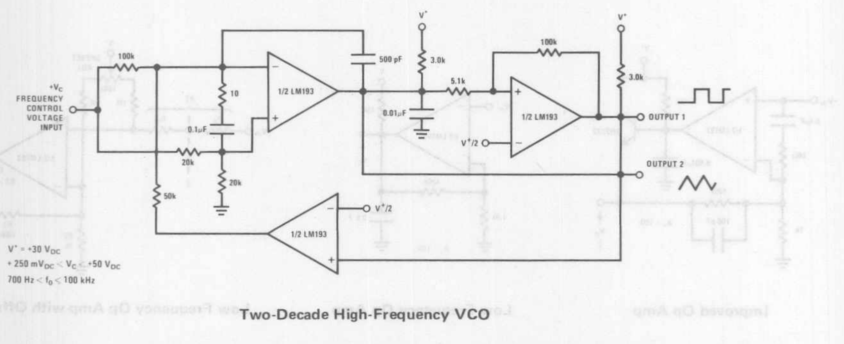
Squarewave Oscillator



Pulse Generator

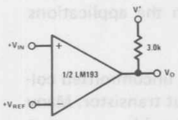


Crystal Controlled Oscillator

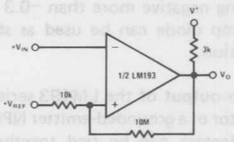


Two-Decade High-Frequency VCO

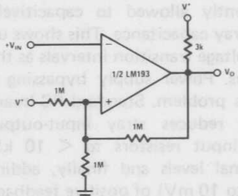
Typical Applications (Continued) ($V^+ = 15\ V_{DC}$)



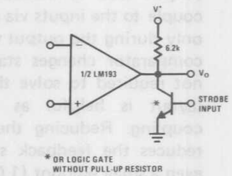
Basic Comparator



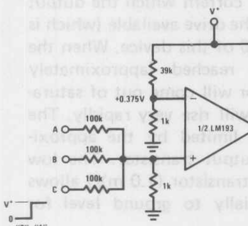
Non-Inverting Comparator with Hysteresis



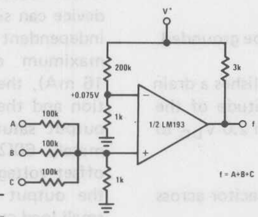
Inverting Comparator with Hysteresis



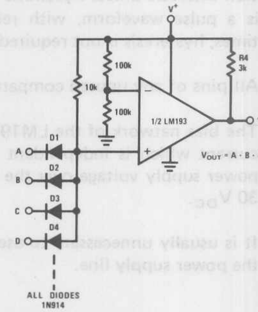
Output Strobing



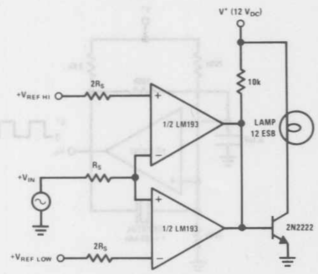
AND Gate



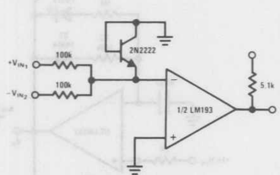
OR Gate



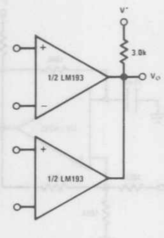
Large Fan-in AND Gate



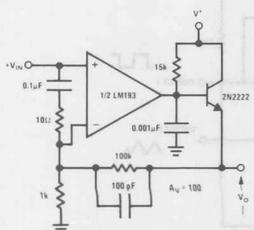
Limit Comparator



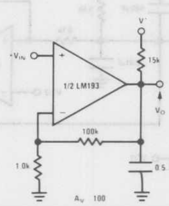
Comparing Input Voltages of Opposite Polarity



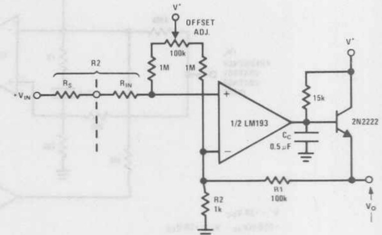
ORing the Outputs



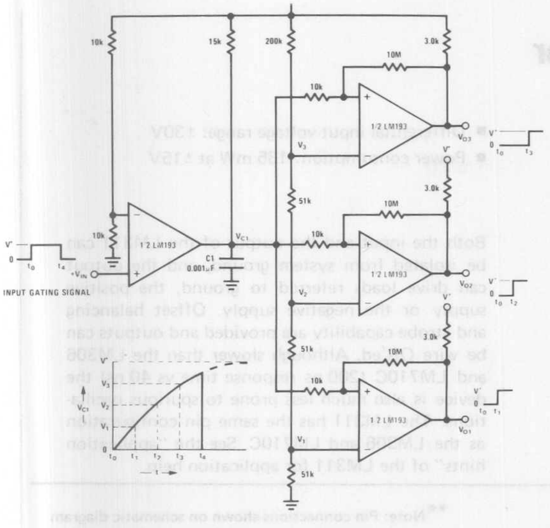
Improved Op Amp



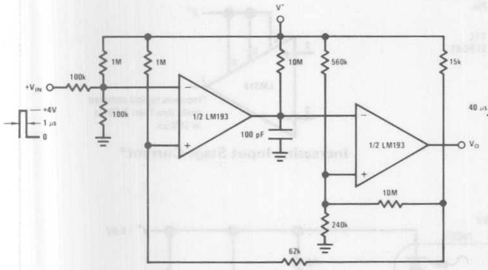
Low Frequency Op Amp



Low Frequency Op Amp with Offset Adjust

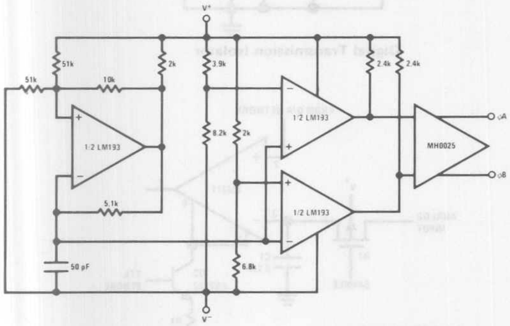


Time Delay Generator

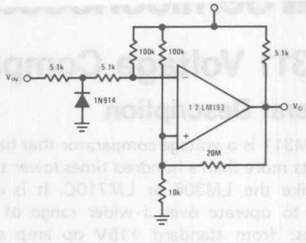


One-Shot Multivibrator with Input Lock Out

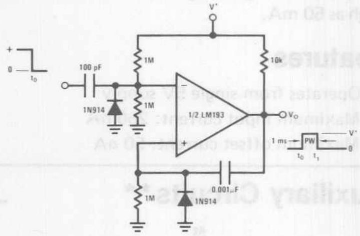
Split-Supply Applications ($V^+ = +15\ V_{DC}$ and $V^- = -15\ V_{DC}$)



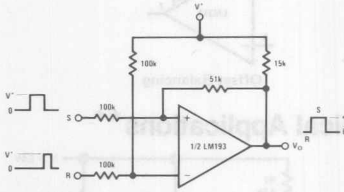
MOS Clock Driver



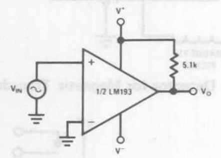
Zero Crossing Detector (Single Power Supply)



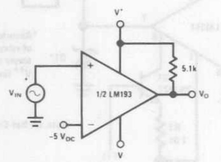
One-Shot Multivibrator



Bi-Stable Multivibrator



Zero Crossing Detector



Comparator With a Negative Reference

LM311 Voltage Comparator

General Description

The LM311 is a voltage comparator that has input currents more than a hundred times lower than devices like the LM306 or LM710C. It is also designed to operate over a wider range of supply voltages: from standard ±15V op amp supplies down to the single 5V supply used for IC logic. Its output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, it can drive lamps or relays, switching voltages up to 40V at currents as high as 50 mA.

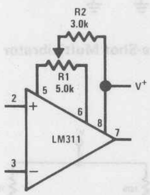
Features

- Operates from single 5V supply
- Maximum input current: 250 nA
- Maximum offset current: 50 nA
- Differential input voltage range: ±30V
- Power consumption: 135 mW at ±15V

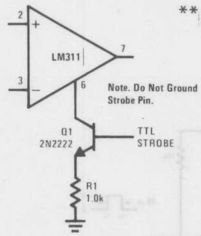
Both the input and the output of the LM311 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the LM306 and LM710C (200 ns response time vs 40 ns) the device is also much less prone to spurious oscillations. The LM311 has the same pin configuration as the LM306 and LM710C. See the "application hints" of the LM311 for application help.

Auxiliary Circuits**

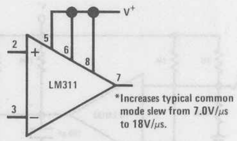
**Note: Pin connections shown on schematic diagram and typical applications are for TO-5 package.



Offset Balancing

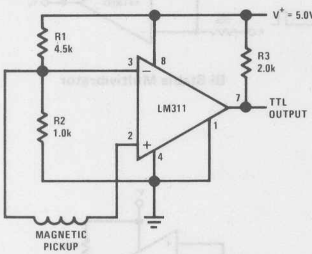


Strobing

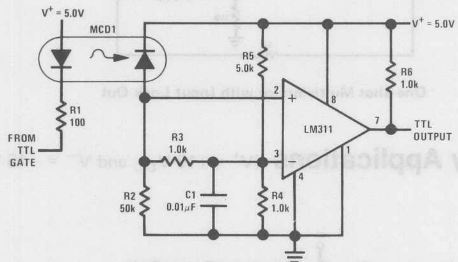


Increasing Input Stage Current*

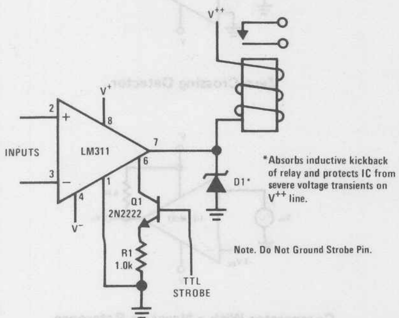
Typical Applications**



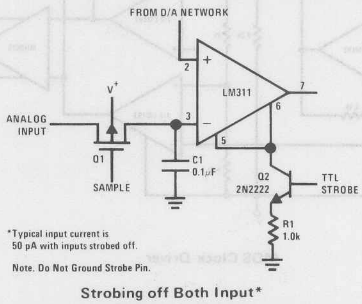
Detector for Magnetic Transducer



Digital Transmission Isolator



Relay Driver with Strobe



Strobing off Both Input* and Output Stages

Absolute Maximum Ratings

Total Supply Voltage (V_{84})	36V
Output to Negative Supply Voltage (V_{74})	40V
Ground to Negative Supply Voltage (V_{14})	30V
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 sec
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	–65°C to 150°C
Lead Temperature (soldering, 10 sec)	300°C
Voltage at Strobe Pin	V^+–5V

Electrical Characteristics (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50k$		2.0	7.5	mV
Input Offset Current (Note 4)	$T_A = 25°C$		6.0	50	nA
Input Bias Current	$T_A = 25°C$		100	250	nA
Voltage Gain	$T_A = 25°C$	40	200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200		ns
Saturation Voltage	$V_{IN} \leq -10$ mV, $I_{OUT} = 50$ mA $T_A = 25°C$		0.75	1.5	V
Strobe ON Current	$T_A = 25°C$		3.0		mA
Output Leakage Current	$V_{IN} \geq 10$ mV, $V_{OUT} = 35V$ $T_A = 25°C$, $I_{STROBE} = 3$ mA		0.2	50	nA
Input Offset Voltage (Note 4)	$R_S \leq 50k$			10	mV
Input Offset Current (Note 4)				70	nA
Input Bias Current				300	nA
Input Voltage Range		–14.5	13.8,–14.7	13.0	V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -10$ mV, $I_{SINK} \leq 8$ mA		0.23	0.4	V
Positive Supply Current	$T_A = 25°C$		5.1	7.5	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

Note 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LM311 is 110°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 3: These specifications apply for $V_S = \pm15V$ and the Ground pin at ground, and $0°C < T_A < +70°C$, unless otherwise specified. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.

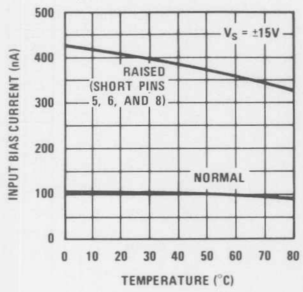
Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with 1 mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.

Note 5: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

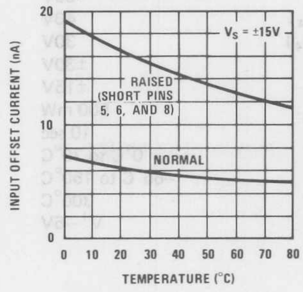
Note 6: Do not short the strobe pin to ground; it should be current driven at 3 to 5 mA.

Typical Performance Characteristics

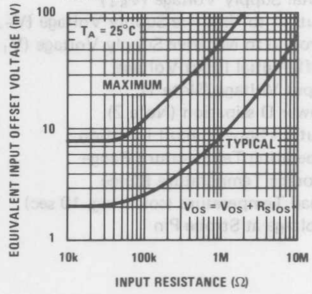
Input Bias Current



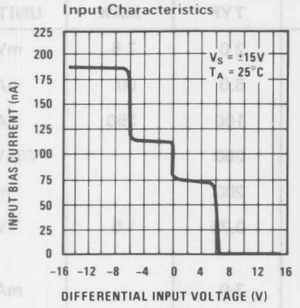
Input Offset Current



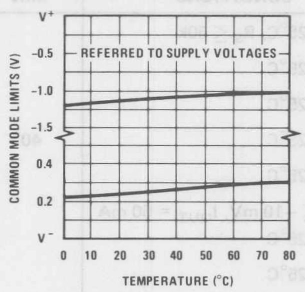
Offset Error



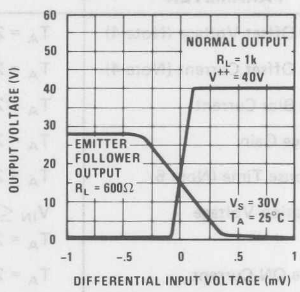
Input Characteristics



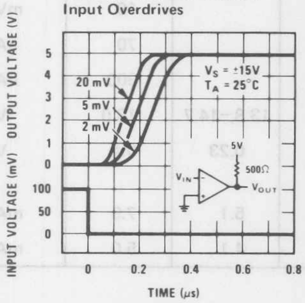
Common Mode Limits



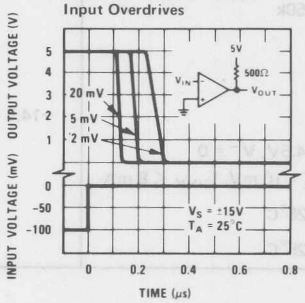
Transfer Function



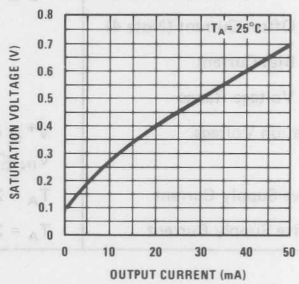
Response Time for Various Input Overdrives



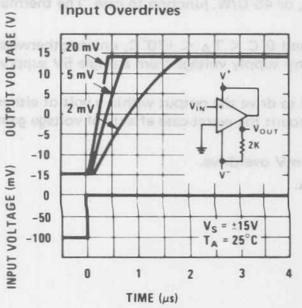
Response Time for Various Input Overdrives



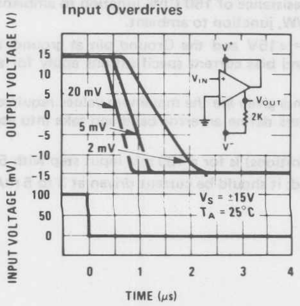
Output Saturation Voltage



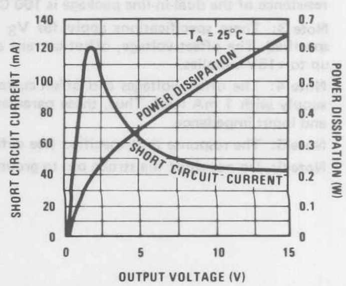
Response Time for Various Input Overdrives



Response Time for Various Input Overdrives

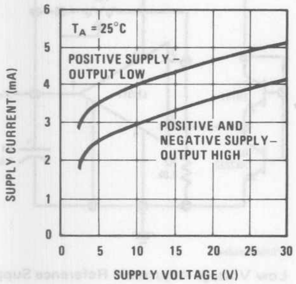


Output Limiting Characteristics

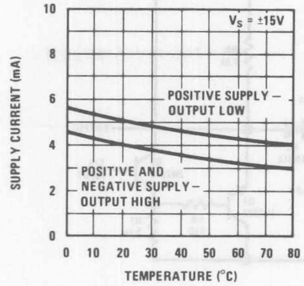


Typical Performance Characteristics (Continued)

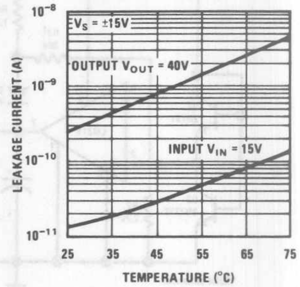
Supply Current



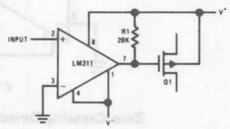
Supply Current



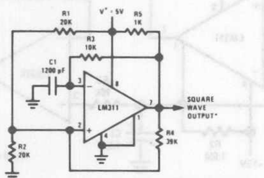
Leakage Currents



Typical Applications

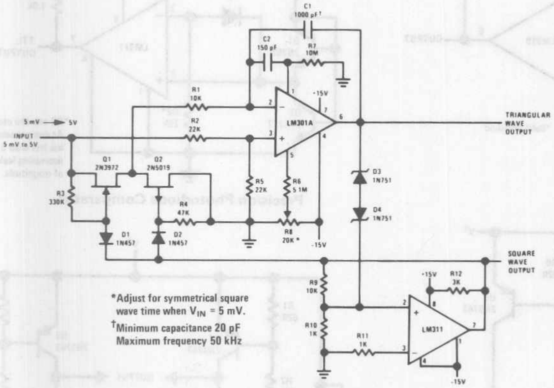


Zero Crossing Detector Driving MOS Switch



*TTL or DTL fanout of two.

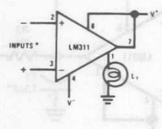
100 kHz Free Running Multivibrator



*Adjust for symmetrical square wave time when V_{IN} = 5 mV.

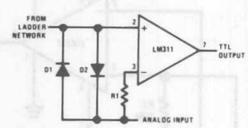
†Minimum capacitance 20 pF Maximum frequency 50 kHz

10 Hz to 10 kHz Voltage Controlled Oscillator

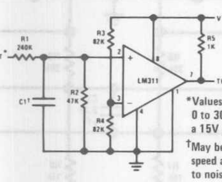


*Input polarity is reversed when using pin 1 as output.

Driving Ground-Referred Load



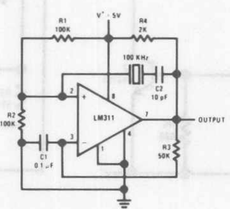
Using Clamp Diodes to Improve Response



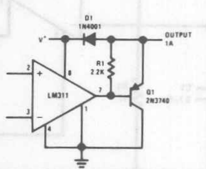
*Values shown are for a 0 to 30V logic swing and a 15V threshold.

†May be added to control speed and reduce susceptibility to noise spikes.

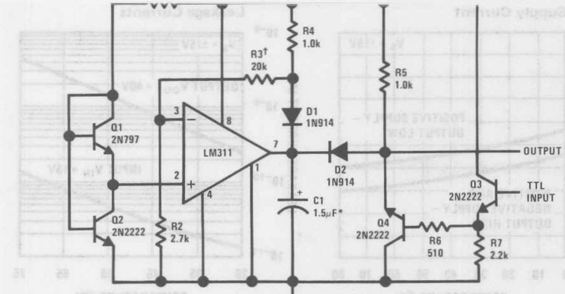
TTL Interface with High Level Logic



Crystal Oscillator

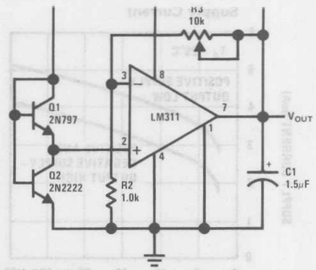


Comparator and Solenoid Driver



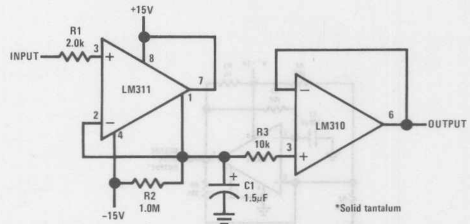
*Solid tantalum.
†Adjust to set clamp level.

Precision Squarer



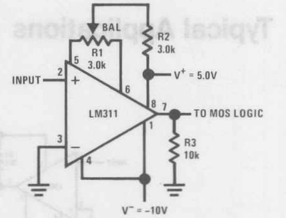
*Solid tantalum

Low Voltage Adjustable Reference Supply

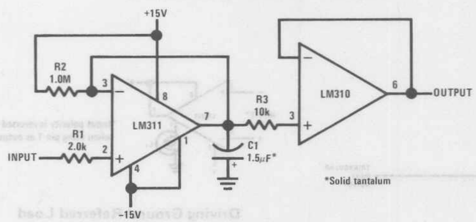


*Solid tantalum

Positive Peak Detector

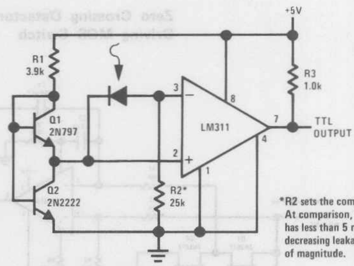


Zero Crossing Detector driving MOS logic



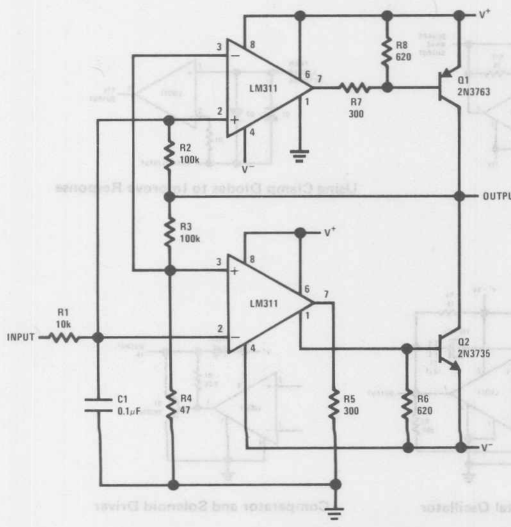
*Solid tantalum

Negative Peak Detector

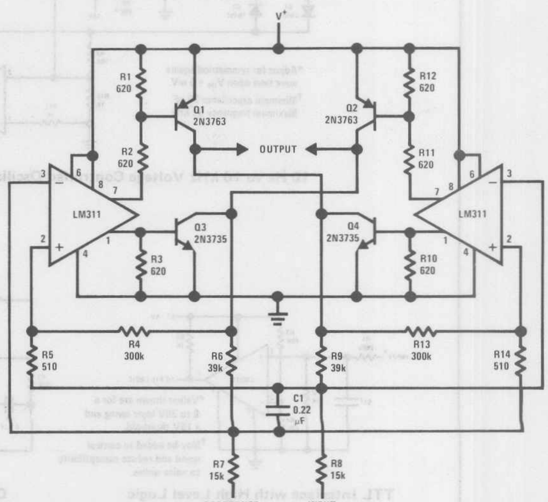


*R2 sets the comparison level. At comparison, the photodiode has less than 5 mV across it, decreasing leakages by an order of magnitude.

Precision Photodiode Comparator

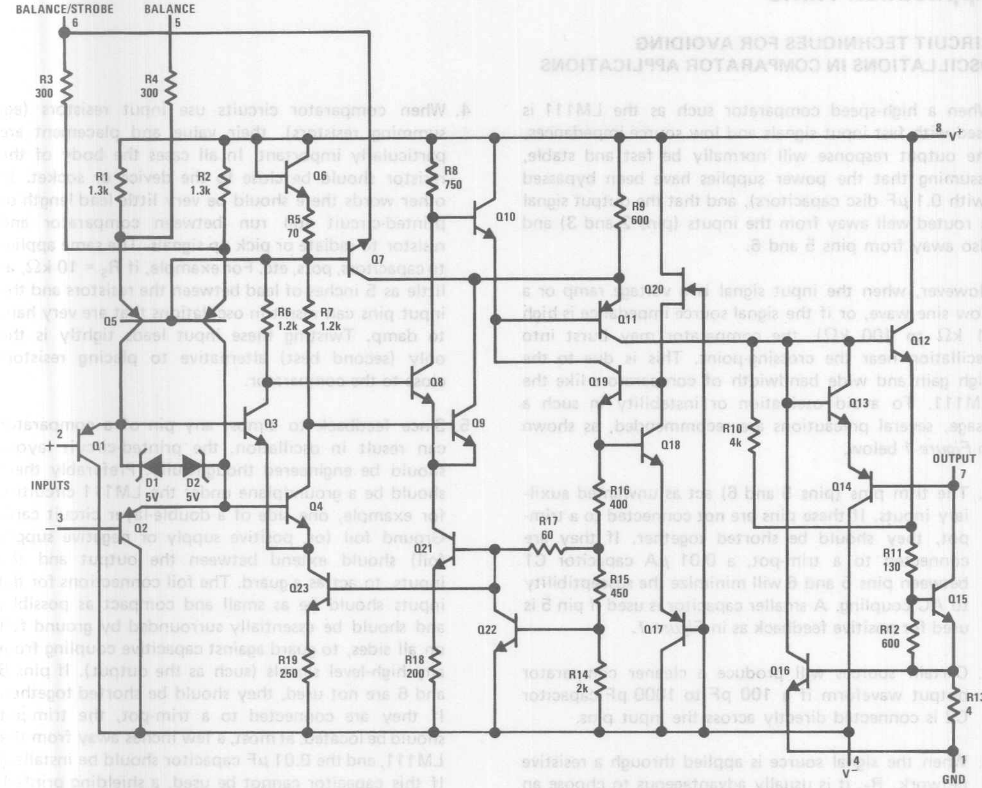


Switching Power Amplifier



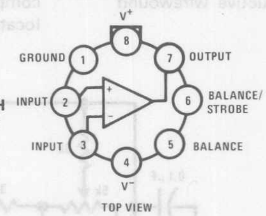
Switching Power Amplifier

Schematic Diagram



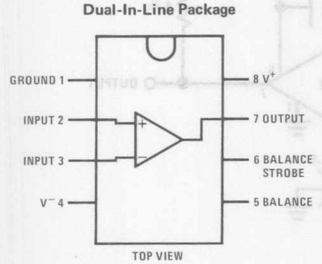
Connection Diagrams*

Metal Can Package



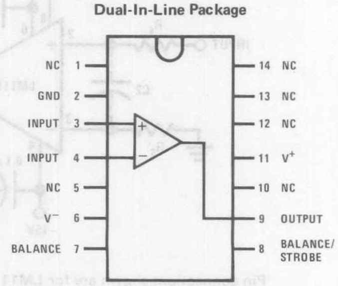
Order Number LM311H
See NS Package H08C

Dual-In-Line Package



Order Number LM311N
See NS Package N08B
Order Number LM311J-8
See NS Package J08A

Dual-In-Line Package



Note: Pin 6 connected to bottom of package.

Order Number LM311N-14
See NS Package N14A
Order Number LM311J
See NS Package J14A

*Pin connections shown on schematic diagram and typical applications are for TO-5 package.

Application Hints

CIRCUIT TECHNIQUES FOR AVOIDING OSCILLATIONS IN COMPARATOR APPLICATIONS

When a high-speed comparator such as the LM111 is used with fast input signals and low source impedances, the output response will normally be fast and stable, assuming that the power supplies have been bypassed (with 0.1 μF disc capacitors), and that the output signal is routed well away from the inputs (pins 2 and 3) and also away from pins 5 and 6.

However, when the input signal is a voltage ramp or a slow sine wave, or if the signal source impedance is high (1 kΩ to 100 kΩ), the comparator may burst into oscillation near the crossing-point. This is due to the high gain and wide bandwidth of comparators like the LM111. To avoid oscillation or instability in such a usage, several precautions are recommended, as shown in *Figure 1* below.

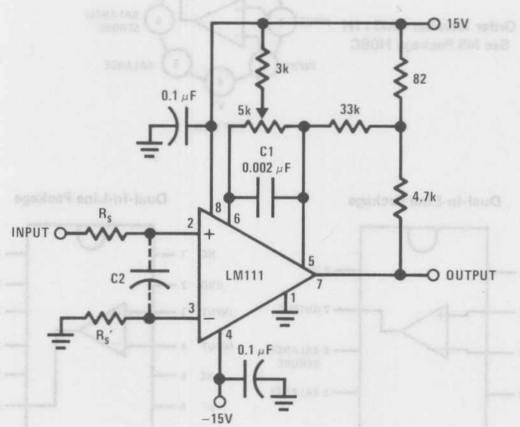
1. The trim pins (pins 5 and 6) act as unwanted auxiliary inputs. If these pins are not connected to a trim-pot, they should be shorted together. If they are connected to a trim-pot, a 0.01 μA capacitor C1 between pins 5 and 6 will minimize the susceptibility to AC coupling. A smaller capacitor is used if pin 5 is used for positive feedback as in *Figure 1*.

2. Certain sources will produce a cleaner comparator output waveform if a 100 pF to 1000 pF capacitor C2 is connected directly across the input pins.

3. When the signal source is applied through a resistive network, R_S, it is usually advantageous to choose an R_S' of substantially the same value, both for DC and for dynamic (AC) considerations. Carbon, tin-oxide, and metal-film resistors have all been used successfully in comparator input circuitry. Inductive wirewound resistors are not suitable.

4. When comparator circuits use input resistors (eg. summing resistors), their value and placement are particularly important. In all cases the body of the resistor should be close to the device or socket. In other words there should be very little lead length or printed-circuit foil run between comparator and resistor to radiate or pick up signals. The same applies to capacitors, pots, etc. For example, if R_S = 10 kΩ, as little as 5 inches of lead between the resistors and the input pins can result in oscillations that are very hard to damp. Twisting these input leads tightly is the only (second best) alternative to placing resistors close to the comparator.

5. Since feedback to almost any pin of a comparator can result in oscillation, the printed-circuit layout should be engineered thoughtfully. Preferably there should be a groundplane under the LM111 circuitry, for example, one side of a double-layer circuit card. Ground foil (or, positive supply or negative supply foil) should extend between the output and the inputs, to act as a guard. The foil connections for the inputs should be as small and compact as possible, and should be essentially surrounded by ground foil on all sides, to guard against capacitive coupling from any high-level signals (such as the output). If pins 5 and 6 are not used, they should be shorted together. If they are connected to a trim-pot, the trim-pot should be located, at most, a few inches away from the LM111, and the 0.01 μF capacitor should be installed. If this capacitor cannot be used, a shielding printed-circuit foil may be advisable between pins 6 and 7. The power supply bypass capacitors should be located within a couple inches of the LM111. (Some other comparators require the power-supply bypass to be located immediately adjacent to the comparator.)



Pin connections shown are for LM111H in 8-lead TO-5 hermetic package

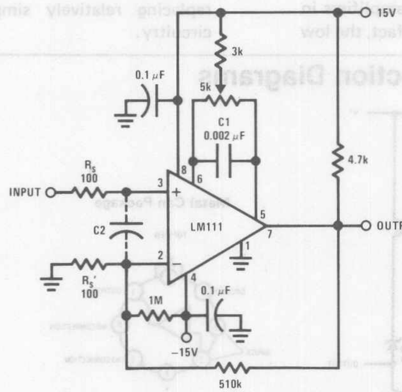
FIGURE 1. Improved Positive Feedback

Application Hints (Continued)

6. It is a standard procedure to use hysteresis (positive feedback) around a comparator, to prevent oscillation, and to avoid excessive noise on the output because the comparator is a good amplifier for its own noise. In the circuit of *Figure 2,* the feedback from the output to the positive input will cause about 3 mV of hysteresis. However, if R_S is larger than 100Ω, such as 50 kΩ, it would not be reasonable to simply increase the value of the positive feedback resistor above 510 kΩ. The circuit of *Figure 3* could be used, but it is rather awkward. See the notes in paragraph 7 below.

7. When both inputs of the LM111 are connected to active signals, or if a high-impedance signal is driving the positive input of the LM111 so that positive feedback would be disruptive, the circuit of *Figure 1* is ideal. The positive feedback is to pin 5 (one of the offset adjustment pins). It is sufficient to cause 1 to 2 mV hysteresis and sharp transitions with input triangle waves from a few Hz to hundreds of kHz. The positive-feedback signal across the 82Ω resistor swings 240 mV below the positive supply. This signal is centered around the nominal voltage at pin 5, so this feedback does not add to the V_{OS} of the comparator. As much as 8 mV of V_{OS} can be trimmed out, using the 5 kΩ pot and 3 kΩ resistor as shown.

8. These application notes apply specifically to the LM111, LM211, LM311, and LF111 families of comparators, and are applicable to all high-speed comparators in general, (with the exception that not all comparators have trim pins).



Pin connections shown are for LM111H in 8-lead TO-5 hermetic package

FIGURE 2. Conventional Positive Feedback

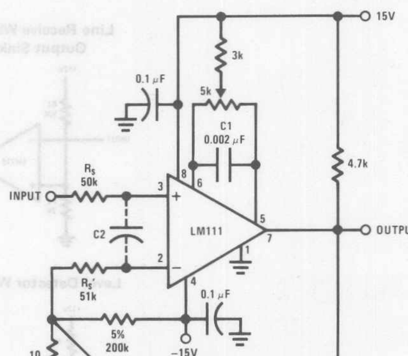


FIGURE 3. Positive Feedback With High Source Resistance

LM710/LM710C Voltage Comparator

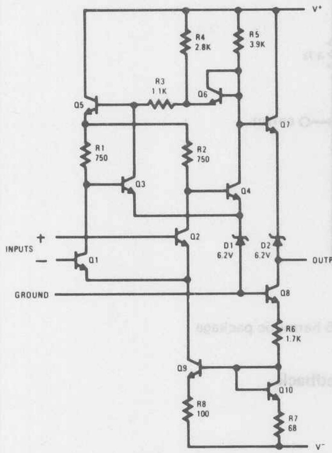
General Description

The LM710 series are a high-speed voltage comparators intended for use as an accurate, low-level digital level sensor or as a replacement for operational amplifiers in comparator applications where speed is of prime importance. The circuit has a differential input and a single-ended output, with saturated output levels compatible with practically all types of integrated logic.

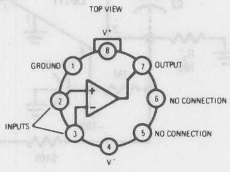
The device is built on a single silicon chip which insures low offset and thermal drift. The use of a minimum number of stages along with minority-carrier lifetime control (gold doping) makes the circuit much faster than operational amplifiers in saturating comparator applications. In fact, the low stray and wiring capacitances that can be realized with monolithic construction make the device difficult to duplicate with discrete components operating at equivalent power levels.

The LM710 series are useful as pulse height discriminators, voltage comparators in high-speed A/D converters or go, no-go detectors in automatic test equipment. They also have applications in digital systems as an adjustable-threshold line receiver or an interface between logic types. In addition, the low cost of the units suggests it for applications replacing relatively simple discrete component circuitry.

Schematic* and Connection Diagrams



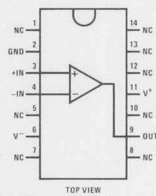
Metal Can Package



Note: Pin 4 connected to case.

Order Number LM710H or LM710CH See NS Package H08C

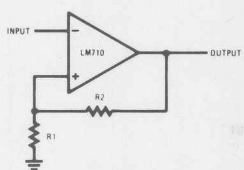
Dual-In-Line Package



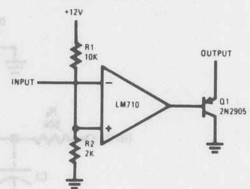
Order Number LM710N or LM710CN See NS Package N14A

Typical Applications *

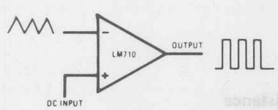
Schmitt Trigger



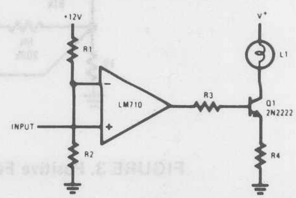
Line Receive With Increased Output Sink Current



Pulse Width Modulator



Level Detector With Lamp Driver



*Pin connections shown are for metal can.

Absolute Maximum Ratings

Positive Supply Voltage	+14V
Negative Supply Voltage	−7V
Peak Output Current	10 mA
Output Short Circuit Duration	10 seconds
Differential Input Voltage	±5V
Input Voltage	±7V
Power Dissipation	
TO-99, (Note 1)	300 mW
Flat Package, (Note 2)	200 mW

	T_{MIN} T_{MAX}
Operating Temperature Range	
LM710	−55°C to +125°C
LM710C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	300°C

Electrical Characteristics (Note 3)

PARAMETER	CONDITIONS	LM710 MIN	LM710 TYP	LM710 MAX	LM710C MIN	LM710C TYP	LM710C MAX	UNITS
Input Offset Voltage	$R_S \leq 200\Omega$, $V_{CM} = 0V$, $T_A = 25°C$		0.6	2.0		1.6	5.0	mV
Input Offset Current	$V_{OUT} = 1.4V$, $T_A = 25°C$		0.75	3.0		1.8	5.0	μA
Input Bias Current	$T_A = 25°C$		13	20		16	25	μA
Voltage Gain	$T_A = 25°C$	1250	1700		1000	1500		
Output Resistance	$T_A = 25°C$		200			200		Ω
Output Sink Current	$V_{OUT} = 0$, $T_A = 25°C$							
	$\Delta V_{IN} \geq 5$ mV	2.0	2.5					mA
	$\Delta V_{IN} \geq 10$ mV				1.6	2.5		mA
Response Time	$T_A = 25°C$, (Note 4)		40			40		ns
Input Offset Voltage	$R_S \leq 200\Omega$, $V_{CM} = 0V$			3.0			6.5	mV
Average Temperature Coefficient of Input Offset Voltage	$T_{MIN} \leq T_A \leq T_{MAX}$ $R_S \leq 50\Omega$		3.0	10		5.0	20	μV/°C
Input Offset Current	$T_A = T_{A\,MAX}$		0.25	3.0			7.5	μA
	$T_A = T_{A\,MIN}$		1.8	7.0			7.5	μA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq T_{MAX}$		5.0	25		15	50	nA/°C
	$T_{MIN} \leq T_A \leq 25°C$		15	75		24	100	nA/°C
Input Bias Current	$T_A = T_{MIN}$		27	45		25	40	μA
Input Voltage Range	$V^- = -7V$	±5.0			±5.0			V
Common-Mode Rejection Ratio	$R_S \leq 200\Omega$	80	100		70	98		dB
Differential Input Voltage Range		±5.0			±5.0			V
Voltage Gain		1000			800			V/V
Positive Output Level	-5 mA $\leq I_{OUT} \leq 0$							
	$V_{IN} \geq 5$ mV	2.5	3.2	4.0				V
	$V_{IN} \geq 10$ mV				2.5	3.2	4.0	V
Negative Output Level	$V_{IN} \geq 5$ mV	−1.0	−0.5	0				V
	$V_{IN} \geq 10$ mV				−1.0	−0.5	0	V
Output Sink Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 0$							
	$T_A = 125°C$	0.5	1.7					mA
	$T_A = -55°C$	1.0	2.3					mA
	$V_{IN} \geq 10$ mV, $V_{OUT} = 0$							
	$0°C \leq T_A \leq +70°C$				0.5			mA
Positive Supply Current	$V_{IN} \geq 5$ mV		5.2	9.0				mA
	$V_{IN} \geq 10$ mV					5.2	9.0	mA
Negative Supply Current	$V_{IN} \geq 5$ mV		4.6	7.0				mA
	$V_{IN} \geq 10$ mV					4.6	7.0	mA
Power Consumption	$I_{OUT} = 0$							
	$V_{IN} \geq 5$ mV		90	150				mW
	$V_{IN} \geq 10$ mV						150	mW

Note 1: Rating applies for case temperatures to 125°C for LM710 and to 70°C for LM710C; derate linearly at 5.6 mW/°C for ambient temperatures above 105°C.

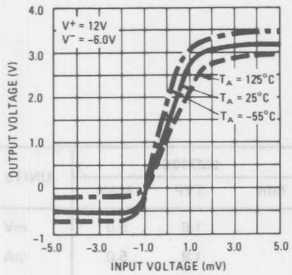
Note 2: Derate linearly at 4.4 mW/°C for ambient temperatures above 100°C.

Note 3: These specifications apply for $V^+ = 12V$, $V^- = -6V$, $-55°C \leq T_A \leq +125°C$ for LM710 and $0°C \leq T_A \leq +70°C$ for LM710C unless otherwise specified. The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1.8V at −55°C, 1.4V at 25°C, and 1V at 125°C for LM710 and 1.5V at 0°C, 1.4V at 25°C and 1.2V at 70°C for LM710C.

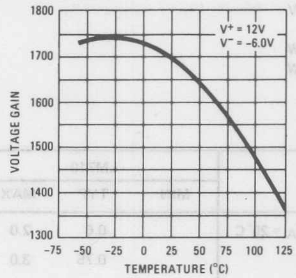
Note 4: The response time specified (see definitions) is a 100 mV input step with 5 mV overdrive (LM710) or a 10 mV overdrive (LM710C).

Typical Performance Characteristics

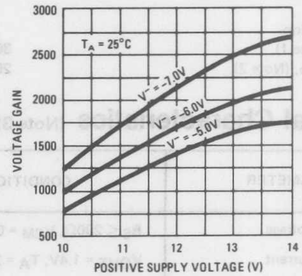
Transfer Function



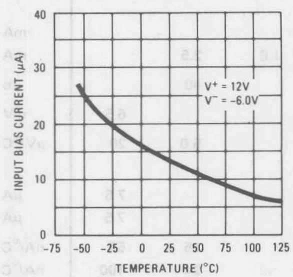
Voltage Gain



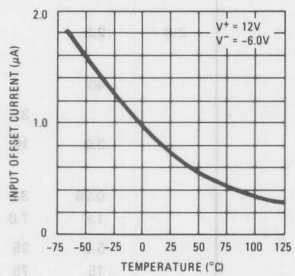
Voltage Gain



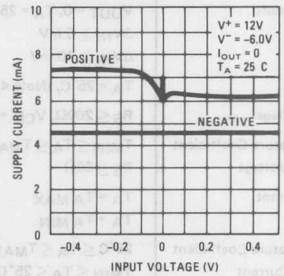
Input Bias Current



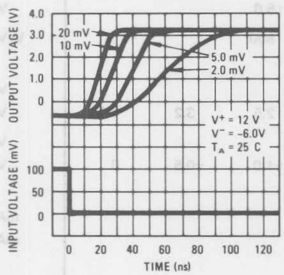
Input Offset Current



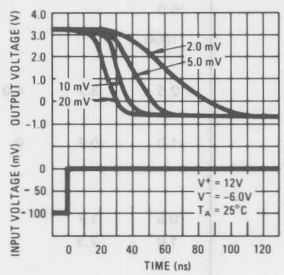
Supply Current



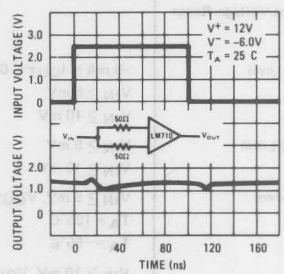
Response Time For Various Input Overdrives



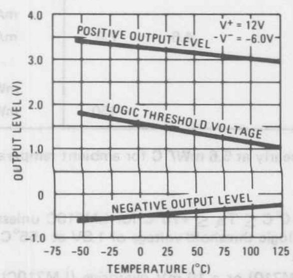
Response Time For Various Input Overdrives



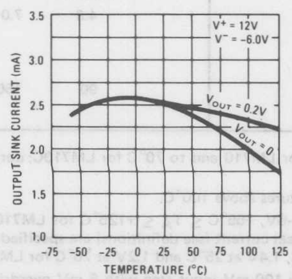
Common Mode Pulse Response



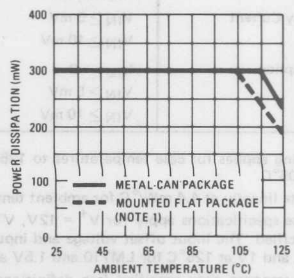
Output Voltage Level



Output Sink Current



Maximum Power Dissipation



National Semiconductor

Voltage Comparators

LM711/LM711C Dual Comparator

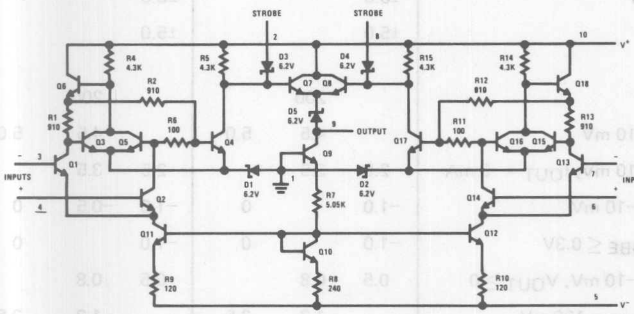
General Description

The LM711 series contains two voltage comparators with separate differential inputs, a common output and provision for strobing each side independently. Similar to the LM710, the device features low offset and thermal drift, a large input voltage range, low power consumption, fast recovery from large overloads and compatibility with most integrated logic circuits.

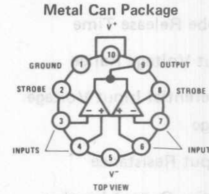
With the addition of an external resistor network, the LM711 series can be used as a sense amplifier for core memories. The input thresholding, combined with the high gain of the comparator, eliminates many of the inaccuracies encountered with conventional sense amplifier designs. Further, it has the speed and accuracy needed for reliably detecting the outputs of cores as small as 20 mils.

The LM711 series are also useful in other applications where a dual comparator with OR'ed outputs is required, such as a double-ended limit detector. By using common circuitry for both halves, the device can provide high speed with lower power dissipation than two single comparators. The LM711C is the commercial/industrial version of the LM711. With operation specified over 0°C to +70°C temperature range.

Schematic** and Connection Diagrams



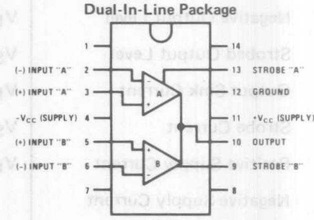
Metal Can Package



Note: Pin 5 connected to case.

Order Number LM711H or LM711CH
See NS Package H10C

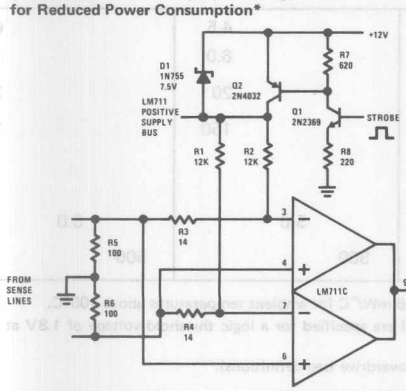
Dual-In-Line Package



Order Number LM711CN
See NS Package N14A

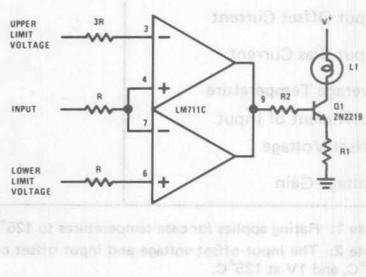
Typical Applications**

Sense Amplifier With Supply Strobing for Reduced Power Consumption*



*Standby dissipation is about 40 mW.

Double-Ended Limit Detector With Lamp Driver



**Pin connections shown are for metal can.

Negative Supply Voltage	−7V
Peak Output Current	25 mA
Differential Input Voltage	±5V
Input Voltage	±7V
Strobe Voltage	0 to +6V
Internal Power Dissipation (Note 1)	300 mW
LM711	−55°C to +125°C
LM711C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (These specifications apply for $T_A = 25°C$, $V^+ = 12V$, $V^- = -6V$)

PARAMETER	CONDITIONS (Note 2)	LM711			LM711C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 200\Omega$, $V_{CM} = 0$		1.0	3.5		1.0	5.0	mV
	$R_S \leq 200\Omega$, $-5V \leq V_{CM} \leq +5V$		1.0	5.0		1.0	7.5	mV
Input Offset Current			0.5	10.0		0.5	15	μA
Input Bias Current			25	75		25	100	μA
Voltage Gain		750	1500		700	1500		
Response Time (Note 3)			40			40		ns
Strobe Release Time			12			12		ns
Input Voltage Range	$V^- = 7V$	±5.0			±5.0			V
Differential Input Voltage Range		±5.0			±5.0			V
Output Resistance			200			200		Ω
Positive Output Level	$V_{IN} \geq 10$ mV		4.5	5.0		4.5	5.0	V
Loaded Positive Output Level	$V_{IN} \geq 10$ mV, $I_{OUT} = -5$ mA	2.5	3.5		2.5	3.5		V
Negative Output Level	$V_{IN} \leq -10$ mV	−1.0		0	−1.0	−0.5	0	V
Strobed Output Level	$V_{STROBE} \leq 0.3V$	−1.0		0	−1.0		0	V
Output Sink Current	$V_{IN} \leq -10$ mV, $V_{OUT} \geq 0$	0.5	0.8		0.5	0.8		mA
Strobe Current	$V_{STROBE} = 100$ mV		1.2	2.5		1.2	2.5	mA
Positive Supply Current	$V_{IN} \leq -10$ mV		8.6			8.6		mA
Negative Supply Current			3.9			3.9		mA
Power Consumption			130	200		130	230	mW
The following specifications apply for $T_{MIN} \leq T_A \leq T_{MAX}$:								
Input Offset Voltage	$R_S \leq 200\Omega$, $V_{CM} = 0$			4.5			6.0	mV
	$R_S \leq 200\Omega$			6.0			10	mV
Input Offset Current				20			25	μA
Input Bias Current				150			150	μA
Average Temperature Coefficient of Input Offset Voltage			5.0			5.0		μV/°C
Voltage Gain		500			500			

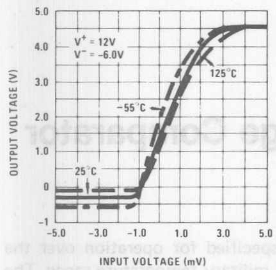
Note 1: Rating applies for case temperatures to 125°C; derate linearly at 5.6 mW/°C for ambient temperatures above 105°C.

Note 2: The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1.8V at −55°C, 1.4V at 25°C, and 1V at 125°C.

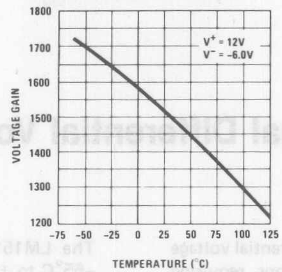
Note 3: The response time specified is for a 100 mV input step with 5 mV overdrive (see definitions).

Typical Performance Characteristics

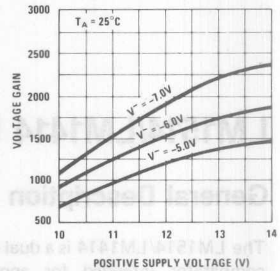
Transfer Function



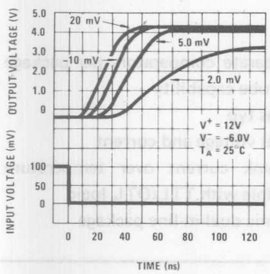
Voltage Gain



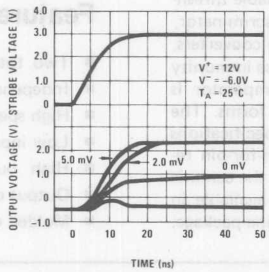
Voltage Gain



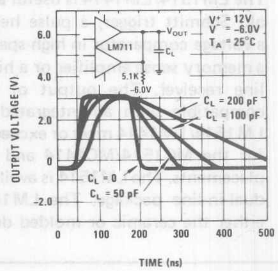
Response Time for Various Input Overdrives



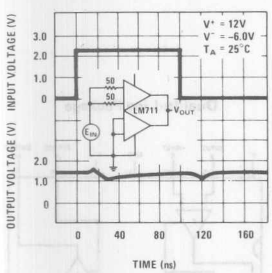
Strobe Release Time for Various Input Overdrives



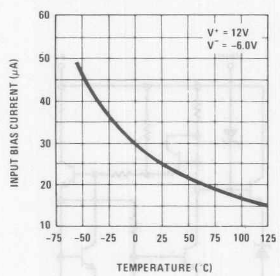
Output Pulse Stretching With Capacitive Loading



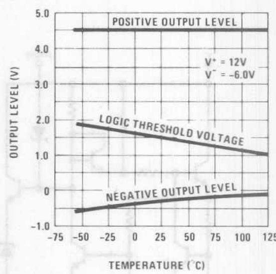
Common Mode Pulse Response



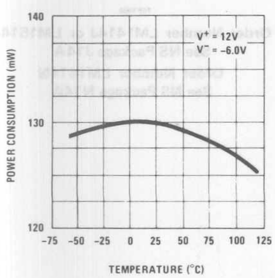
Input Bias Current



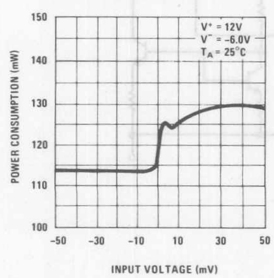
Output Voltage Level



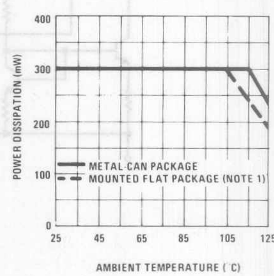
Power Consumption



Power Consumption



Maximum Power Dissipation



National Semiconductor

LM1514/LM1414 Dual Differential Voltage Comparator

General Description

The LM1514/LM1414 is a dual differential voltage comparator intended for applications requiring high accuracy and fast response times. The device is constructed on a single monolithic silicon chip.

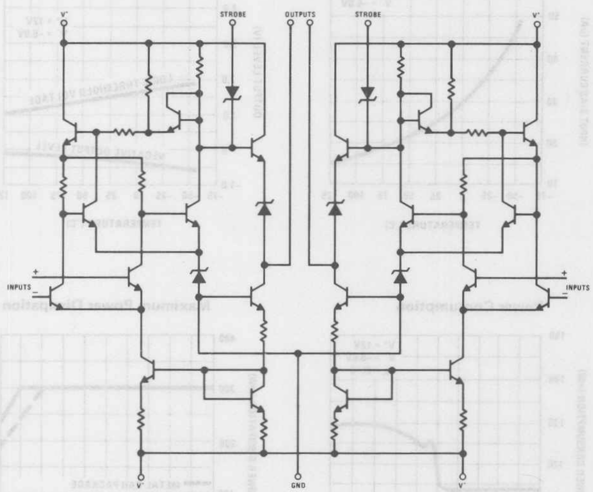
The LM1514/LM1414 is useful as a variable threshold Schmitt trigger, a pulse height discriminator, a voltage comparator in high-speed A-D converters, a memory sense amplifier or a high noise immunity line receiver. The output of the comparator is compatible with all integrated logic forms. The LM1514/LM1414 meet or exceed the specifications for the MC1514/MC1414 and are pin-for-pin replacements. The LM1514 is available in the ceramic dual-in-line package. The LM1414 is available in either the ceramic or molded dual-in-line package.

The LM1514 is specified for operation over the −55°C to +125°C military temperature range. The LM1414 is specified for operation over the 0°C to +70°C temperature range.

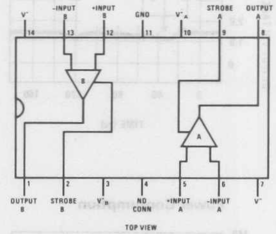
Features

- Two totally separate comparators per package
- Independent strobe capability
- High speed 30 ns typ
- Low input offset voltage and current
- High output sink current over temperature
- Output compatible with TTL/DTL logic
- Molded or ceramic dual-in-line package

Schematic and Connection Diagrams



Dual-In-Line Package



Order Number LM1414J or LM1514J
See NS Package J14A
Order Number LM1414N
See NS Package N14A

Absolute Maximum Ratings (Note 1)

Positive Supply Voltage		+14.0V
Negative Supply Voltage		−7.0V
Peak Output Current		10 mA
Differential Input Voltage		±5.0V
Input Voltage		±7.0V
Power Dissipation (Note 2)		600 mW
Operating Temperature Range	LM1514	−55°C to +125°C
	LM1414	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)		300°C

Electrical Characteristics for T_A = 25°C, V^+ = +12V, V^- = −6V, unless otherwise specified

PARAMETER	CONDITIONS	LM1514			LM1414			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 200\Omega$, V_{CM} = 0V, V_{OUT} = 1.4V		0.6	2.0		1.0	5.0	mV
Input Offset Current	V_{CM} = 0V, V_{OUT} = 1.4V		0.8	3.0		1.2	5.0	μA
Input Bias Current				20			25	μA
Voltage Gain		1250			1000			
Output Resistance			200			200		Ω
Differential Input Voltage Range		±5.0			±5.0			V
Input Voltage Range	V^- = −7.0V	±5.0			±5.0			V
Common Mode Rejection Ratio	$R_S \leq 200\Omega$, V^- = −7.0V	80	100		70	100		dB
Positive Output Voltage	$V_{IN} \geq 7.0$ mV, $0 \leq I_{OUT} \leq -5.0$ mA	2.5	3.2	4.0	2.5	3.2	4.0	V
Negative Output Voltage	$V_{IN} \leq -7.0$ mV	−1.0	−0.5	0	−1.0	−0.5	0	V
Strobed Output Voltage	$V_{STROBE} \leq 0.3$V	−1.0	−0.5	0	−1.0	−0.5	0	V
Strobe "0" Current	V_{STROBE} = 100 mV		−1.2	−2.5		−1.2	−2.5	mA
Positive Supply Current	$V_{IN} \leq -7$ mV			18			18	mA
Negative Supply Current	$V_{IN} \leq -7$ mV			−14			−14	mA
Power Consumption			180	300		180	300	mW
Response Time	(Note 3)		30			30		ns
LM1514/LM1414: The following apply for $T_L \leq T_A \leq T_H$ (Note 4) unless otherwise specified								
Input Offset Voltage	$R_S \leq 200\Omega$, V_{OUT} = 1.8V for $T_A = T_L$			3.0			6.5	mV
	V_{CM} = 0V, V_{OUT} = 1.0V for $T_A = T_H$			3.0			6.5	mV
Input Bias Current				45			40	μA
Temperature Coefficient of Input Offset Voltage			3.0			5.0		μV/°C
Input Offset Current	V_{CM} = 0V, V_{OUT} = 1.8V, $T_A = T_L$			7.0			7.5	μA
	V_{CM} = 0V, V_{OUT} = 1.0V, $T_A = T_H$			3.0			7.5	μA
Voltage Gain		1000			800			
Output Sink Current	$V_{IN} \leq -9.0$ mV, $V_{OUT} \geq 0$V	2.8	4.0		1.6	2.5		mA

Note 1: Voltage values are with respect to network ground terminal. Positive current is defined as current into the referenced pin.

Note 2: LM1514 ceramic package: The maximum junction temperature is +150°C, for operating at elevated temperatures, devices must be derated linearly at 12.5 mW/°C. LM1414 ceramic package: The maximum junction temperature is +95°C for operating at elevated temperatures, devices must be derated linearly at 12.5 mW/°C. LM1414 molded package: The maximum junction temperature is +115°C, for operating at elevated temperatures, devices must be derated linearly at 6.7 mW/°C.

Note 3: The response time specified (see definitions) for a 100 mV input step with 5 mV overdrive.

Note 4: For LM1514, T_L = −55°C, T_H = +125°C. For LM1414, T_L = 0°C, T_H = +70°C.

Section 6

Analog Switches

6

Analog Switches

Section Contents

Note. For additional information on analog switches, see National Semiconductor's Hybrid Products Databook and FET Databook.

R_{ON} (Ω)*	$V_{A/I}$ (V)†	Part Number	Logic Input	V_S (V) Typ	t_{ON}/t_{OFF} Typ
QUAD SPST					
100	15 mA	AH5011	15V TTL, CMOS		150/300 ns
150	5 mA	AH5012	TTL, CMOS		150/300 ns
200	± 10	LF11201	TTL	± 15	90/500 ns
200	± 10	LF11202	TTL	± 15	90/500 ns
200	± 10	LF11331	TTL	± 15	90/500 ns
200	± 10	LF11332	TTL	± 15	90/500 ns
200	± 10	LF11333	TTL	± 15	90/500 ns
250	± 10	LF13201	TTL	± 15	90/500 ns
250	± 10	LF13202	TTL	± 15	90/500 ns
250	± 10	LF13331	TTL	± 15	90/500 ns
250	± 10	LF13332	TTL	± 15	90/500 ns
250	± 10	LF13333	TTL	± 15	90/500 ns
280	± 7.5	CD4066	CMOS	± 7.5	50/50 ns
850	± 7.5	CD4016	CMOS	± 7.5	20/20 ns
TRIPLE SPDT					
280	± 7.5	CD4053	CMOS	± 7.5	150/150 ns
4-CHANNEL					
100	15 mA	AH5009	15V TTL, CMOS		150/300 ns
150	5 mA	AH5010	TTL, CMOS		150/300 ns
4-CHANNEL DIFFERENTIAL					
280	± 7.5	CD4052	CMOS	± 7.5	150/150 ns
350	12, − 15	LF11509	TTL	± 15	1/0.2 μs
270	± 7.5	CD4529B	CMOS	± 7.5	50/50 ns
8-CHANNEL					
250-400	± 5	AM3705	TTL	− 15, 5	300/600 ns
350	12, − 15	LF11508	TTL	± 15	1/0.2 μs
270	± 7.5	CD4529B	CMOS	± 7.5	50/50 ns
280	± 7.5	CD4501	CMOS	± 7.5	150/150 ns

*R_{ON} max @ $T_A = 25°C$
†$V_{A/I}$ = maximum voltage or current to be safely switched

Definition of Terms

R_{ON}: Resistance between the output and the input of an addressed channel.

I_S: Current at any switch input. This is leakage current when the switch is ON.

I_D: Current at any switch input going into the switch. This is leakage current when the switch is OFF.

C_S: Capacitance between any open terminal "S" and ground.

C_D: Capacitance between any open terminal "D" and ground.

I_D–I_S: Leakage current that flows from the closed switch into the body. This leakage is the difference between the current I_D going into the switch and the current I_S going out of the switch.

t_{RAN}: Delay time when switching from one address state to another.

t_{ON}: Delay time between the 50% points of an enable input and the switch ON condition.

t_{OFF}: Delay time between the 50% points of the enable input and the switch OFF condition.

AH5009, AH5010, AH5011, AH5012 Monolithic Analog Current Switches

General Description

A versatile family of monolithic JFET analog switches economically fulfills a wide variety of multiplexing and analog switching applications.

Even numbered switches may be driven directly from standard 5V logic, whereas the odd numbered switches are intended for applications utilizing 10V or 15V logic. The monolithic construction guarantees tight resistance match and track.

Applications

- AD/DA converters
- Micropower converters
- Industrial controllers
- Position controllers
- Data acquisition
- Active filters
- Signal multiplexers/demultiplexers
- Multiple channel AGC
- Quad compressors/expanders
- Choppers/demodulators
- Programmable gain amplifiers
- High impedance voltage buffer
- Sample and hold

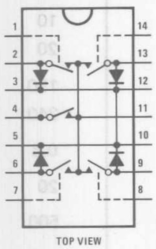
For voltage switching applications see LF13331, LF13332, and LF13333 Analog Switch Family.

Features

■ Interfaces with standard TTL and CMOS	
■ "ON" resistance match	2 ohms
■ Low "ON" resistance	100 ohms
■ Very low leakage	50 pA
■ Large analog signal range	±10V peak
■ High switching speed	150 ns
■ Excellent isolation between channels	80 dB at 1 kHz

Connection and Schematic Diagrams

Dual-In-Line Package

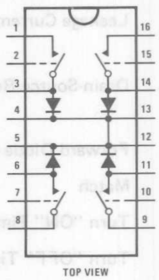


AH5009C and AH5010C MUX Switches (4-Channel Version Shown)

Order Number AH5009CN or AH5010CN NS Package Number N14A

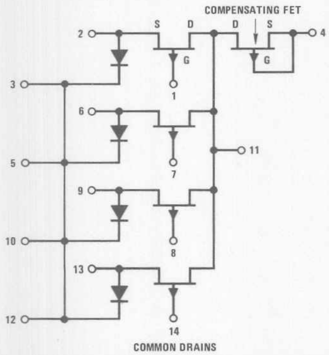
LOGIC DRIVE	4 CHANNEL MUX	4 SPST SWITCHES
5V TTL	AH5010CN	AH5012CN
15V TTL	AH5009CN	AH5011CN

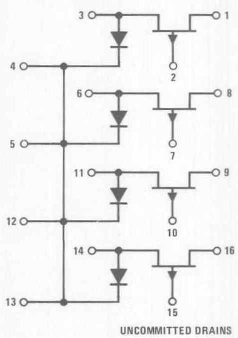
Dual-In-Line Package



AH5011C and AH5012C SPST Switches (Quad Version Shown)

Order Number AH5011CN or AH5012CN NS Package Number N16A





Note: All diode cathodes are internally connected to the substrate.

Absolute Maximum Ratings

Input Voltage	
AH5009/AH5010/AH5011/AH5012	30V
Positive Analog Signal Voltage	30V
Negative Analog Signal Voltage	−15V
Diode Current	10 mA
Drain Current	30 mA
Power Dissipation	500 mW
Operating Temperature Range	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

AH5010 and AH5012 (Notes 1 and 2)

	PARAMETER	CONDITIONS	TYP	MAX	UNITS
I_{GSX}	Input Current "OFF"	$4.5V \leq V_{GD} \leq 11V$, $V_{SD} = 0.7V$	0.01	0.2	nA
		$T_A = 85°C$		10	nA
$I_{D(OFF)}$	Leakage Current "OFF"	$V_{SD} = 0.7V$, $V_{GS} = 3.8V$	0.01	0.2	nA
		$T_A = 85°C$		10	nA
$I_{G(ON)}$	Leakage Current "ON"	$V_{GD} = 0V$, $I_S = 1$ mA	0.08	1	nA
		$T_A = 85°C$		200	nA
$I_{G(ON)}$	Leakage Current "ON"	$V_{GD} = 0V$, $I_S = 2$ mA	0.13	5	nA
		$T_A = 85°C$		10	μA
$I_{G(ON)}$	Leakage Current "ON"	$V_{GD} = 0V$, $I_S = -2$ mA	0.1	10	nA
		$T_A = 85°C$		20	μA
$r_{DS(ON)}$	Drain-Source Resistance	$V_{GS} = 0.35V$, $I_S = 2$ mA	90	150	Ω
		$T_A = +85°C$		240	Ω
V_{DIODE}	Forward Diode Drop	$I_D = 0.5$ mA		0.8	V
$r_{DS(ON)}$	Match	$V_{GS} = 0$, $I_D = 1$ mA	4	20	Ω
T_{ON}	Turn "ON" Time	See ac Test Circuit	150	500	ns
T_{OFF}	Turn "OFF" Time	See ac Test Circuit	300	500	ns
CT	Cross Talk	See ac Test Circuit	120		dB

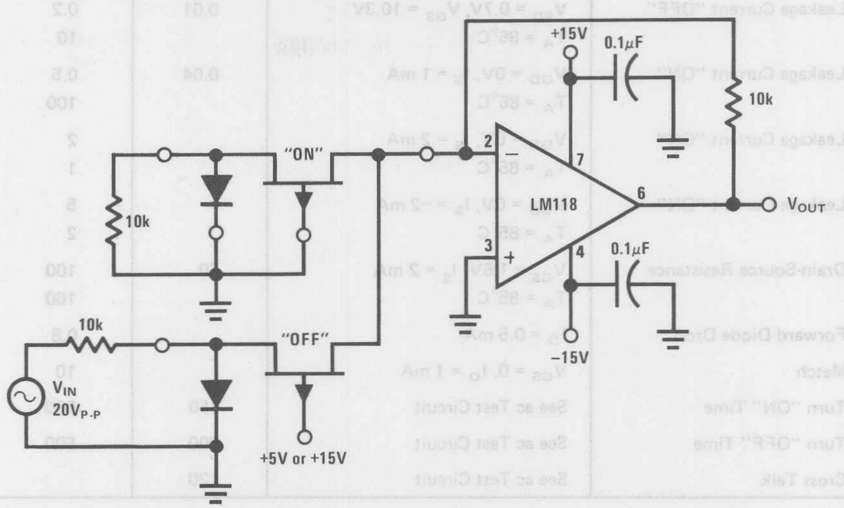
Note 1: Test conditions 25°C unless otherwise noted.

Note 2: "OFF" and "ON" notation refers to the conduction state of the FET switch.

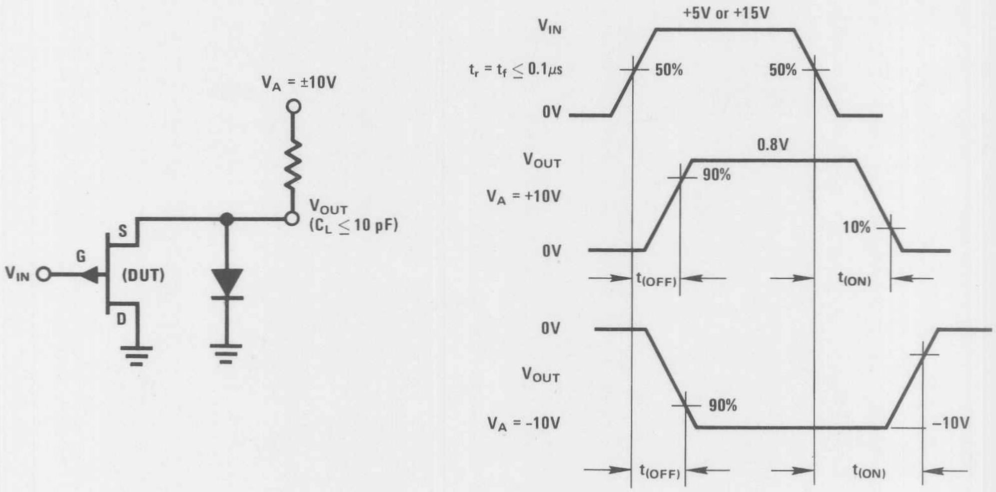
Electrical Characteristics AH5009 and AH5011

	PARAMETER	CONDITIONS	TYP	MAX	UNITS
I_{GSX}	Input Current "OFF"	$11V \leq V_{GD} \leq 15V$, $V_{SD} = 0.7V$	0.01	0.2	nA
		$T_A = 85°C$		10	nA
$I_{D(OFF)}$	Leakage Current "OFF"	$V_{SD} = 0.7V$, $V_{GS} = 10.3V$	0.01	0.2	nA
		$T_A = 85°C$		10	nA
$I_{G(ON)}$	Leakage Current "ON"	$V_{GD} = 0V$, $I_S = 1$ mA	0.04	0.5	nA
		$T_A = 85°C$		100	nA
$I_{G(ON)}$	Leakage Current "ON"	$V_{GD} = 0V$, $I_S = 2$ mA		2	nA
		$T_A = 85°C$		1	μA
$I_{G(ON)}$	Leakage Current "ON"	$V_{GD} = 0V$, $I_S = -2$ mA		5	nA
		$T_A = 85°C$		2	μA
$r_{DS(ON)}$	Drain-Source Resistance	$V_{GS} = 1.5V$, $I_S = 2$ mA	60	100	Ω
		$T_A = 85°C$		160	Ω
V_{DIODE}	Forward Diode Drop	$I_D = 0.5$ mA		0.8	V
$r_{DS(ON)}$	Match	$V_{GS} = 0$, $I_D = 1$ mA		10	Ω
T_{ON}	Turn "ON" Time	See ac Test Circuit	150	500	ns
T_{OFF}	Turn "OFF" Time	See ac Test Circuit	300	500	ns
CT	Cross Talk	See ac Test Circuit	120		dB

Cross Talk Test Circuit

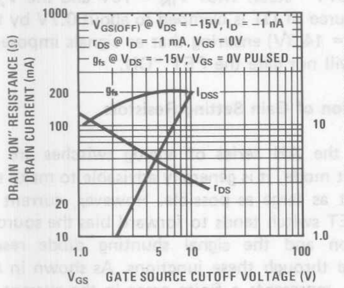


ac Test Circuit

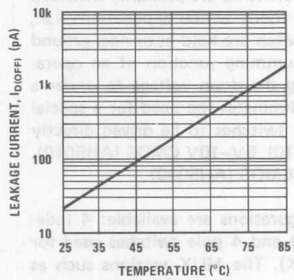


Typical Performance Characteristics

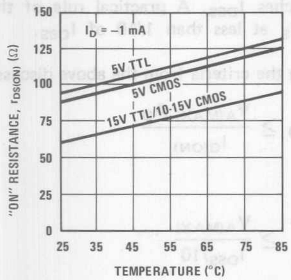
Parameter Interaction



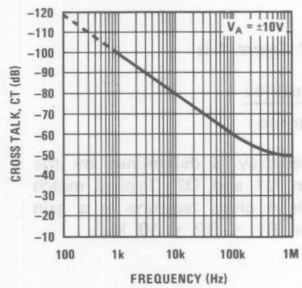
Leakage Current, $I_{D(OFF)}$ vs Temperature



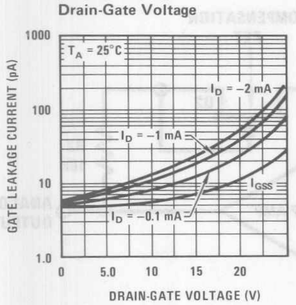
"ON" Resistance, $r_{DS(ON)}$ vs Temperature



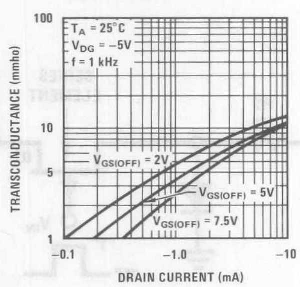
Cross Talk, CT vs Frequency



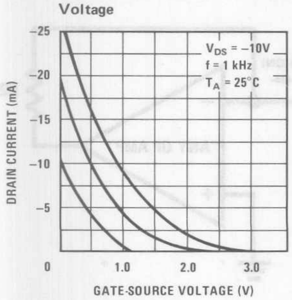
Leakage Current vs Drain-Gate Voltage



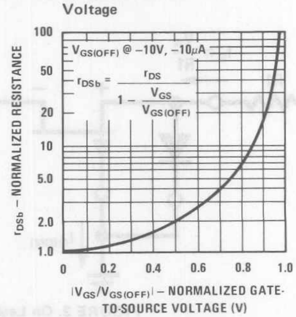
Transconductance vs Drain Current



Drain Current vs Bias Voltage



Normalized Drain Resistance vs Bias Voltage



Applications Information

Theory of Operation

The AH series of analog switches are primarily intended for operation in current mode switch applications; i.e., the drains of the FET switch are held at or near ground by operating into the summing junction of an operational amplifier. Limiting the drain voltage to under a few hundred millivolts eliminates the need for a special gate driver, allowing the switches to be driven directly by standard TTL (AH5010), 5V–10V CMOS (AH5010), open collector 15V TTL/CMOS (AH5009).

Two basic switch configurations are available: 4 independent switches (SPST) and 4 pole switches used for multiplexing (4 PST-MUX). The MUX versions such as the AH5009 offer common drains and include a series FET operated at V_{GS} = 0V. The additional FET is placed in the feedback path in order to compensate for the "ON" resistance of the switch FET as shown in *Figure 1.*

The closed-loop gain of *Figure 1* is:

$$A_{VCL} = \frac{R2 + r_{DS(ON)Q2}}{R1 + r_{DS(ON)Q1}}$$

For R1 = R2, gain accuracy is determined by the $r_{DS(ON)}$ match between Q1 and Q2. Typical match between Q1 and Q2 is 4 ohms resulting in a gain accuracy of 0.05% (for R1 = R2 = 10 kΩ).

Noise Immunity

The switches with the source diodes grounded exhibit improved noise immunity for positive analog signals in the "OFF" state. With V_{IN} = 15V and the V_A = 10V, the source of Q1 is clamped to about 0.7V by the diode (V_{GS} = 14.3V) ensuring that ac signals imposed on the 10V will not gate the FET "ON."

Selection of Gain Setting Resistors

Since the AH series of analog switches are operated current mode, it is generally advisable to make the signal current as large as possible. However, current through the FET switch tends to forward bias the source to gate junction and the signal shunting diode resulting in leakage through these junctions. As shown in *Figure 2,* $I_{G(ON)}$ represents a finite error in the current reaching the summing junction of the op amp.

Secondly, the $r_{DS(ON)}$ of the FET begins to "round" as I_S approaches I_{DSS}. A practical rule of thumb is to maintain I_S at less than 1/10 of I_{DSS}.

Combining the criteria from the above discussion yields:

$$R1_{(MIN)} \geq \frac{V_{A(MAX)}\,A_D}{I_{G(ON)}} \qquad (2a)$$

or:

$$\geq \frac{V_{A(MAX)}}{I_{DSS}/10} \qquad (2b)$$

whichever is larger.

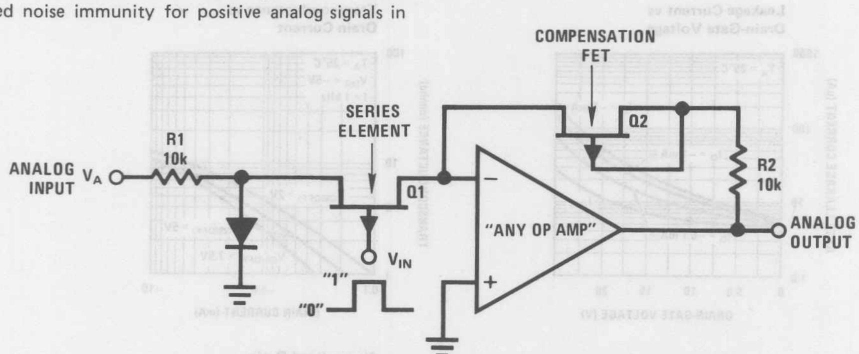


FIGURE 1. Use of Compensation FET

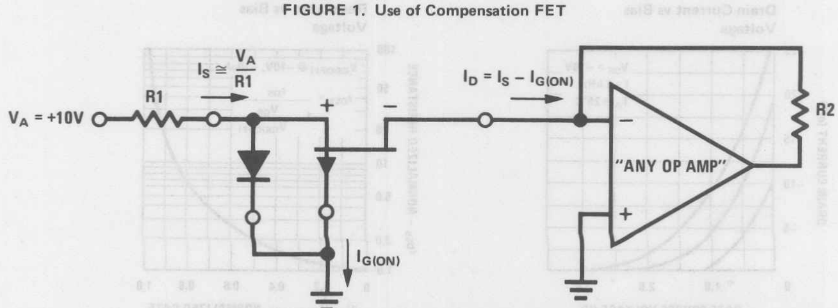


FIGURE 2. On Leakage Current, $I_{G(ON)}$

Applications Information (Continued)

Where: $V_{A(MAX)}$ = Peak amplitude of the analog input signal

A_D = Desired accuracy

$I_{G(ON)}$ = Leakage at a given I_S

I_{DSS} = Saturation current of the FET switch

$\cong$ 20 mA

In a typical application, V_A might = ±10V, A_D = 0.1%, $0°C \le T_A \le 85°C$. The criterion of equation (2b) predicts:

$$R1_{(MIN)} \ge \frac{10V}{\dfrac{20\ mA}{10}} = 5\ k\Omega$$

For R1 = 5k, $I_S \cong$ 10V/5k or 2 mA. The electrical characteristics guarantee an $I_{G(ON)} \le 1\mu A$ at 85°C for the AH5010. Per the criterion of equation (2a):

$$R1_{(MIN)} \ge \frac{(10V)(10^{-3})}{1 \times 10^{-6}} \ge 10\ k\Omega$$

Since equation (2a) predicts a higher value, the 10k resistor should be used.

The "OFF" condition of the FET also affects gain accuracy. As shown in *Figure 3,* the leakage across Q2, $I_{D(OFF)}$ represents a finite error in the current arriving at the summing junction of the op amp.

Accordingly:

$$R1_{(MAX)} \le \frac{V_{A(MIN)}\ A_D}{(N)\ I_{D(OFF)}}$$

Where: $V_{A(MIN)}$ = Minimum value for the analog input signal

A_D = Desired accuracy

N = Number of channels

$I_{D(OFF)}$ = "OFF" leakage of a given FET switch

As an example, if N = 10, A_D = 0.1%, and $I_{D(OFF)} \le$ 10 nA at 85°C for the AH5009. $R1_{(MAX)}$ is:

$$R1_{(MAX)} \le \frac{(1V)(10^{-3})}{(10)(10 \times 10^{-9})} = 10k$$

Selection of R2, of course, depends on the gain desired and for unity gain R1 = R2.

Lastly, the foregoing discussion has ignored resistor tolerances, input bias current and offset voltage of the op amp—all of which should be considered in setting the overall gain accuracy of the circuit.

TTL Compatibility

Two input logic drive versions of AH series are available: the even numbered part types are specified to be driven from standard 5V TTL logic and the odd numbered types from 15V open collector TTL.

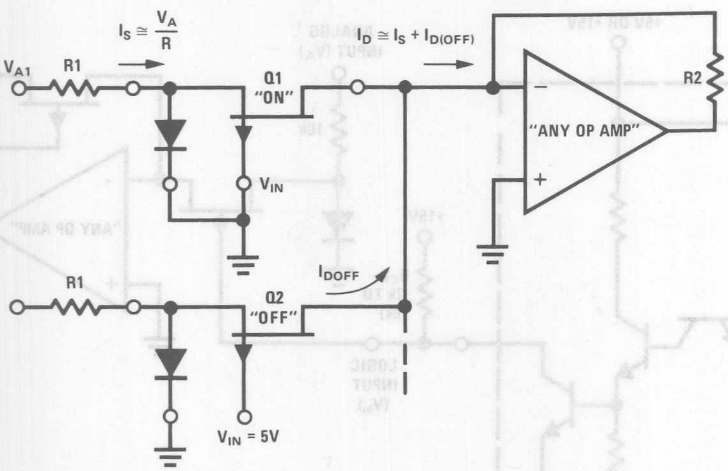


FIGURE 3.

Standard TTL gates pull-up to about 3.5V (no load). In order to ensure turn-off of the even numbered switches such as AH5010, a pull-up resistor, R_{EXT}, of at least 10 kΩ should be placed between the 5V V_{CC} and the gate output as shown in *Figure 4.*

Likewise, the open-collector, high voltage TTL outputs should use a pull-up resistor as shown in *Figure 5.* In

at the expense of power dissipation in the low state.

Definition of Terms

The terms referred to in the electrical characteristics tables are as defined in *Figure 6.*

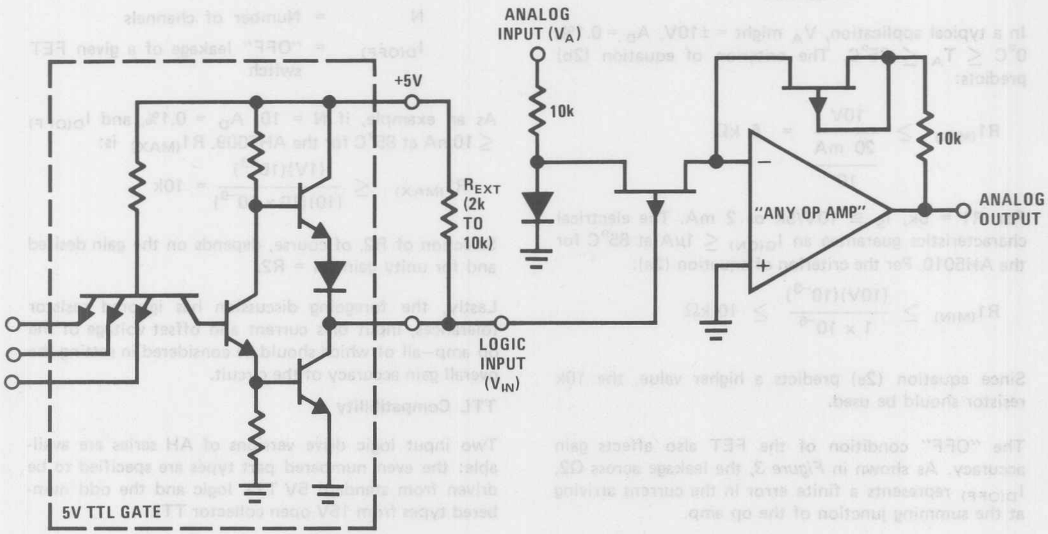


FIGURE 4. Interfacing with +5V TTL

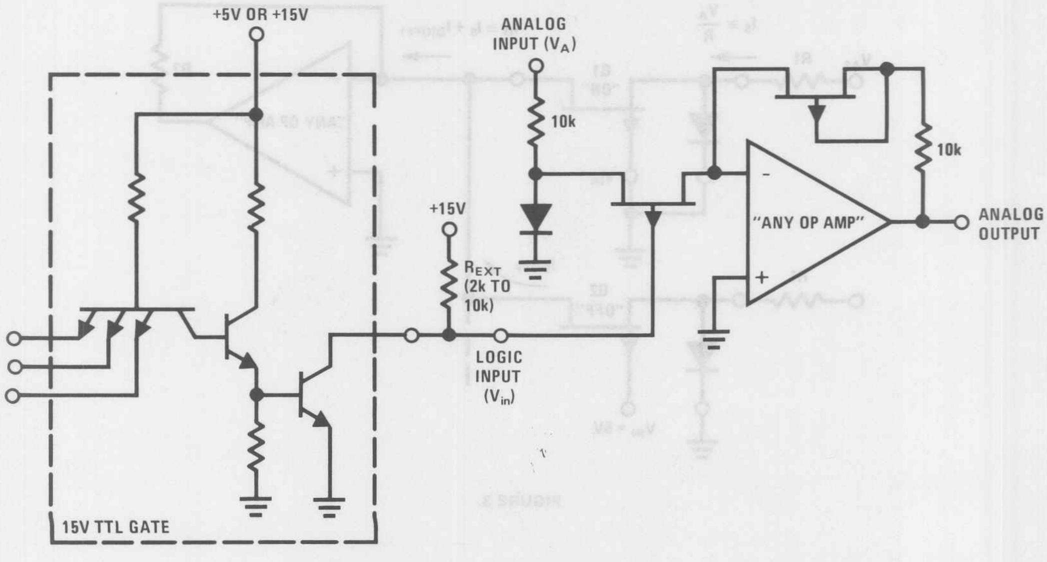


FIGURE 5. Interfacing with +15V Open Collector TTL

Applications Information (Continued)

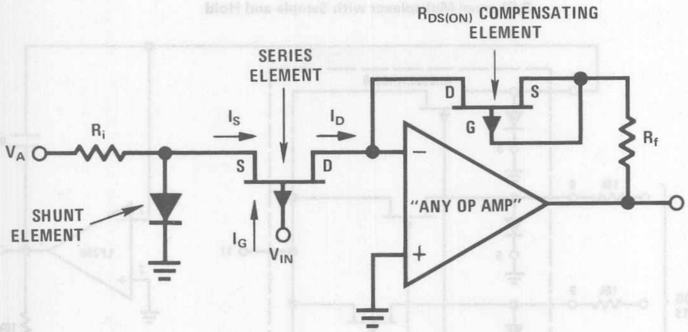
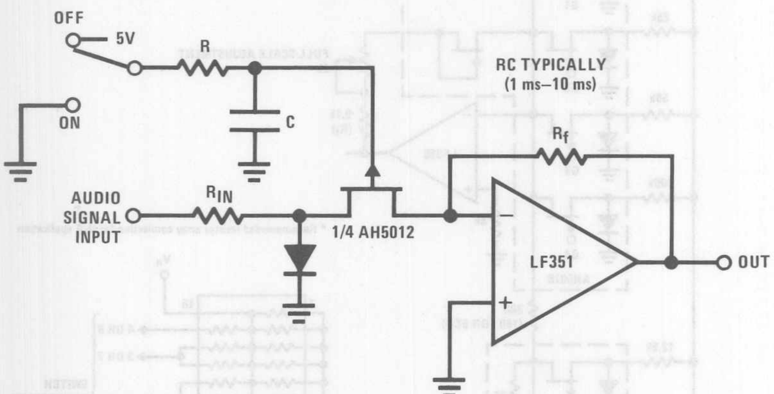


FIGURE 6. Definition of Terms

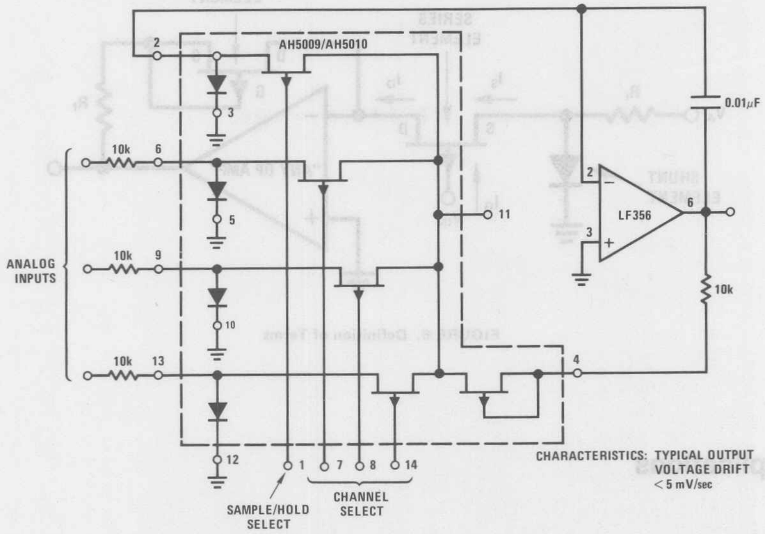
Typical Applications

De-Glitched Switch for Noiseless Audio Switching

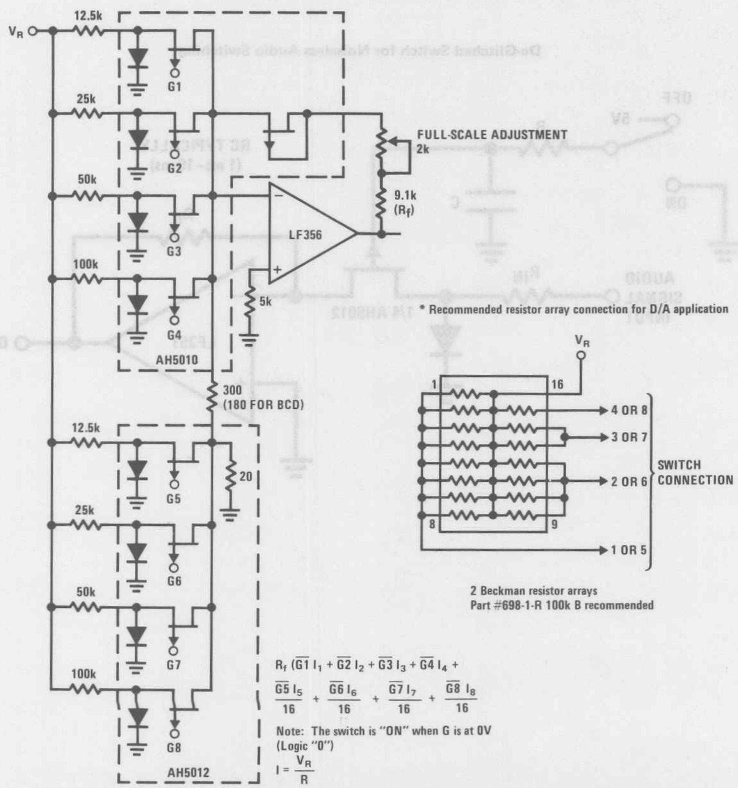


Typical Applications (Continued)

3-Channel Multiplexer with Sample and Hold



8-Bit Binary (BCD) Multiplying D/A Converter*



* Recommended resistor array connection for D/A application

2 Beckman resistor arrays
Part #698-1-R 100k B recommended

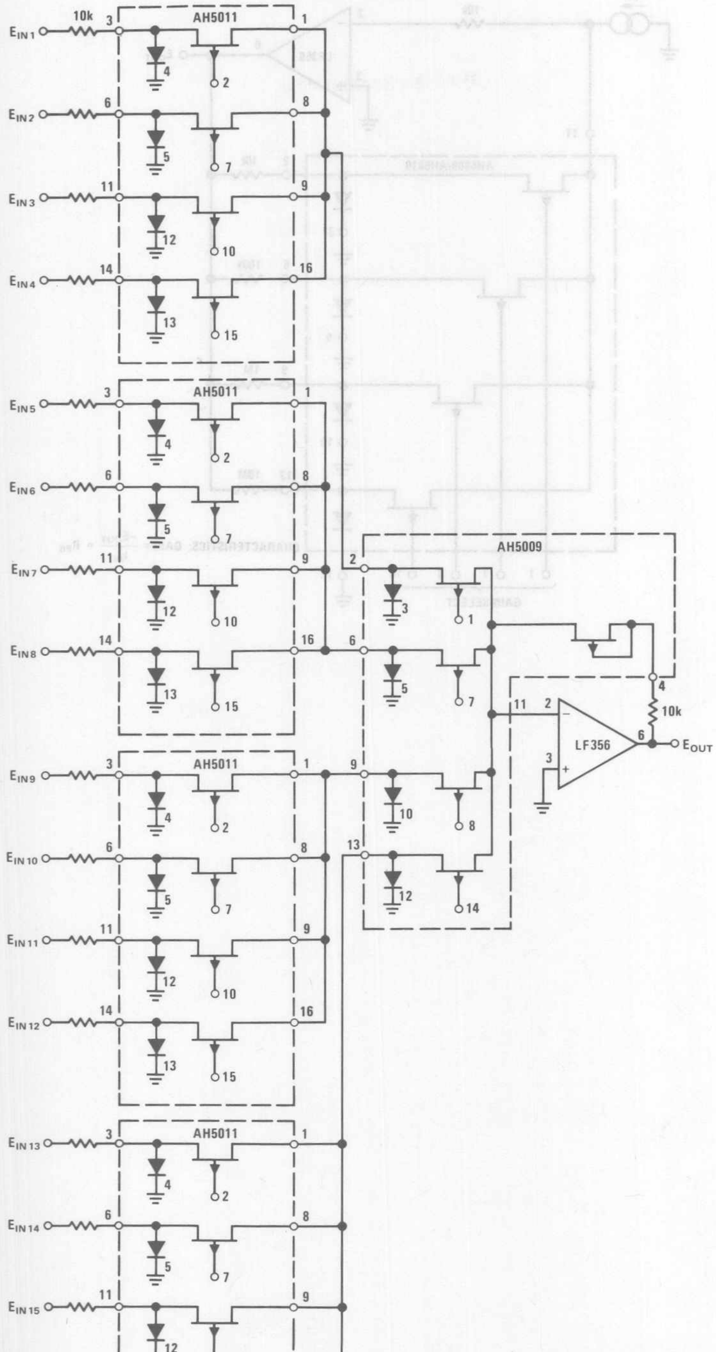
$R_f\,(\overline{G1}\,I_1 + \overline{G2}\,I_2 + \overline{G3}\,I_3 + \overline{G4}\,I_4 + \frac{\overline{G5}\,I_5}{16} + \frac{\overline{G6}\,I_6}{16} + \frac{\overline{G7}\,I_7}{16} + \frac{\overline{G8}\,I_8}{16}$

Note: The switch is "ON" when G is at 0V (Logic "0")

$I = \frac{V_R}{R}$

Typical Applications (Continued)

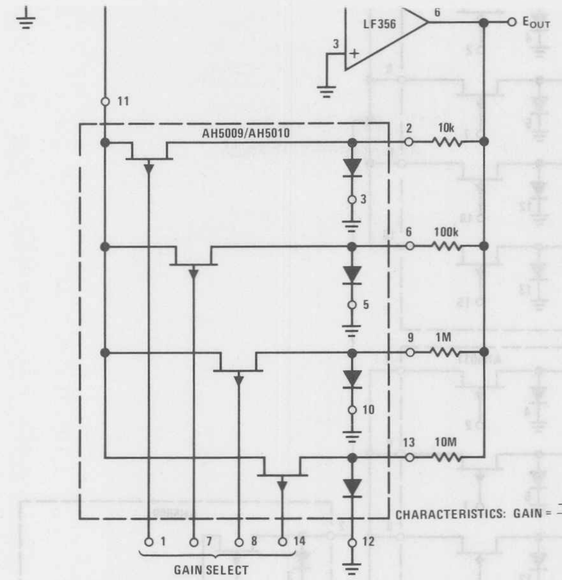
16-Channel Multiplexer



CHARACTERISTICS: ERROR = 0.4μV TYPICAL @ 25°C
10μV TYPICAL @ 70°C

Note: The analog switch between the op amp and the 16 input switches reduces the errors due to leakage.

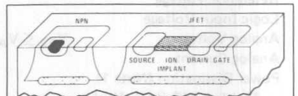
All resistors are 10k



CHARACTERISTICS: GAIN = $\frac{-E_{OUT}}{I_{IN}}$ = R_{FB}

National Semiconductor

Analog Switches



BI-FET Technology

Quad SPST JFET Analog Switches

LF11331/LF13331 4 Normally Open Switches with Disable
LF11332/LF13332 4 Normally Closed Switches with Disable
LF11333/LF13333 2 Normally Closed Switches and 2 Normally Open Switches with Disable
LF11201/LF13201 4 Normally Closed Switches
LF11202/LF13202 4 Normally Open Switches

General Description

These devices are a monolithic combination of bipolar and JFET technology producing the industry's first one chip quad JFET switch. A unique circuit technique is employed to maintain a constant resistance over the analog voltage range of ±10V. The input is designed to operate from minimum TTL levels, and switch operation also ensures a break-before-make action.

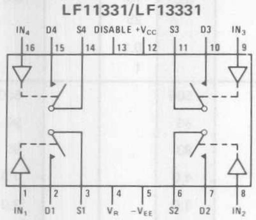
Features

- Analog signals are not loaded
- Constant "ON" resistance for signals up to ±10V and 100 kHz
- Pin compatible with CMOS switches with the advantage of blow out free handling
- Small signal analog signals to 50 MHz
- Break-before-make action $t_{OFF} < t_{ON}$
- High open switch isolation at 1.0 MHz −50 dB
- Low leakage in "OFF" state <1.0 nA
- TTL, DTL, RTL compatibility
- Single disable pin opens all switches in package on LF11331, LF11332, LF11333
- LF11201 is pin compatible with DG201

These devices operate from ±15V supplies and swing a ±10V analog signal. The JFET switches are designed for applications where a dc to medium frequency analog signal needs to be controlled.

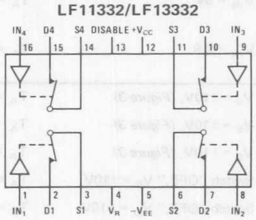
Connection Diagrams (Dual-In-Line Packages) (All Switches Shown are For Logical "0")

LF11331/LF13331



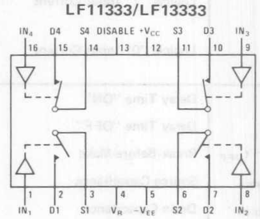
TOP VIEW

LF11332/LF13332



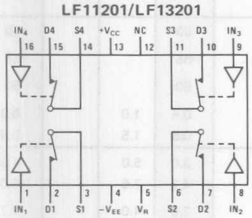
TOP VIEW

LF11333/LF13333



TOP VIEW

LF11201/LF13201

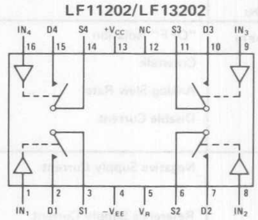


TOP VIEW

Order Number LF11201D, LF13201D, LF11202D, LF13202D, LF11331D, LF13331D, LF11332D, LF13332D, LF11333D, or LF13333D
See NS Package D16C

Order Number LF13201N, LF13202N, LF13331N, LF13332N, or LF13333N
See NS Package N16A

LF11202/LF13202



TOP VIEW

Test Circuit and Schematic Diagram

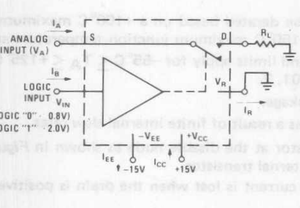


FIGURE 1. Typical Circuit for One Switch

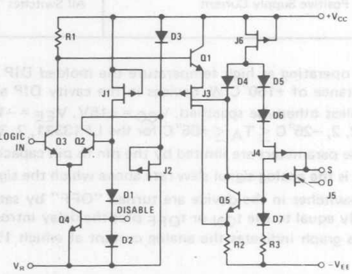


FIGURE 2. Schematic Diagram (Normally Open)

Absolute Maximum Ratings

Positive Supply – Negative Supply (V_{CC}–V_{EE})	36V
Reference Voltage	$V_{EE} \leq V_R \leq V_{CC}$
Logic Input Voltage	V_R –4.0V $\leq V_{IN} \leq V_R$ +6.0V
Analog Voltage	$V_{EE} \leq V_A \leq V_{CC}$ +6V; $V_A \leq V_{EE}$ +36V
Analog Current	$\lvert I_A \rvert$ < 20 mA
Power Dissipation (Note 1)	
Molded DIP (N Suffix)	500 mW
Cavity DIP (D Suffix)	900 mW
Operating Temperature Range	
LF11201, 2 and LF11331, 2, 3	–55°C to +125°C
LF13201, 2 and LF13331, 2, 3	0°C to +70°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 2)

SYMBOL	PARAMETER	CONDITIONS		LF11331/2/3 LF11201/2 MIN	TYP	MAX	LF13331/2/3 LF13201/2 MIN	TYP	MAX	UNITS
R_{ON}	"ON" Resistance	V_A = 0, I_D = 1 mA	T_A = 25°C		150	200		150	250	Ω
					200	300		200	350	Ω
R_{ON} Match	"ON" Resistance Matching		T_A = 25°C		5	20		10	50	Ω
V_A	Analog Range			±10	±11		±10	±11		V
$I_{S(ON)}$ + $I_{D(ON)}$	Leakage Current in "ON" Condition	Switch "ON," V_S = V_D = ±10V	T_A = 25°C		0.3	5		0.3	10	nA
					3	100		3	30	nA
$I_{S(OFF)}$	Source Current in "OFF" Condition	Switch "OFF," V_S = +10V, V_D = –10V	T_A = 25°C		0.4	5		0.4	10	nA
					3	100		3	30	nA
$I_{D(OFF)}$	Drain Current in "OFF" Condition	Switch "OFF," V_S = +10V, V_D = –10V	T_A = 25°C		0.1	5		0.1	10	nA
					3	100		3	30	nA
V_{INH}	Logical "1" Input Voltage			2.0			2.0			V
V_{INL}	Logical "0" Input Voltage					0.8			0.8	V
I_{INH}	Logical "1" Input Current	V_{IN} = 5V	T_A = 25°C		3.6	10		3.6	40	μA
						25			100	μA
I_{INL}	Logical "0" Input Current	V_{IN} = 0.8	T_A = 25°C			0.1			0.1	μA
						1			1	μA
t_{ON}	Delay Time "ON"	V_S = ±10V, *(Figure 3)*	T_A = 25°C		500			500		ns
t_{OFF}	Delay Time "OFF"	V_S = ±10V, *(Figure 3)*	T_A = 25°C		90			90		ns
$t_{ON} - t_{OFF}$	Break-Before-Make	V_S = ±10V, *(Figure 3)*	T_A = 25°C		80			80		ns
$C_{S(OFF)}$	Source Capacitance	Switch "OFF," V_S = ±10V	T_A = 25°C		4.0			4.0		pF
$C_{D(OFF)}$	Drain Capacitance	Switch "OFF," V_D = ±10V	T_A = 25°C		3.0			3.0		pF
$C_{S(ON)}$ + $C_{D(ON)}$	Active Source and Drain Capacitance	Switch "ON," V_S = V_D = 0V	T_A = 25°C		5.0			5.0		pF
$I_{SO(OFF)}$	"OFF" Isolation	*(Figure 4)*, (Note 3)	T_A = 25°C		–50			–50		dB
CT	Crosstalk	*(Figure 4)*, (Note 3)	T_A = 25°C		–65			–65		dB
SR	Analog Slew Rate	(Note 4)	T_A = 25°C		50			50		V/μs
I_{DIS}	Disable Current	*(Figure 5)*, (Note 5)	T_A = 25°C		0.4	1.0		0.6	1.5	mA
					0.6	1.5		0.9	2.3	mA
I_{EE}	Negative Supply Current	All Switches "OFF," V_S = ±10V	T_A = 25°C		3.0	5.0		4.3	7.0	mA
					4.2	7.5		6.0	10.5	mA
I_R	Reference Supply Current	All Switches "OFF," V_S = ±10V	T_A = 25°C		2.0	4.0		2.7	5.0	mA
					2.8	6.0		3.8	7.5	mA
I_{CC}	Positive Supply Current	All Switches "OFF," V_S = ±10V	T_A = 25°C		4.5	6.0		7.0	9.0	mA
					6.3	9.0		9.8	13.5	mA

Note 1: For operating at high temperature the molded DIP products must be derated based on a +100°C maximum junction temperature and a thermal resistance of +150°C/W, devices in the cavity DIP are based on a +150°C maximum junction temperature and are derated at +100°C/W.

Note 2: Unless otherwise specified, V_{CC} = +15V, V_{EE} = –15V, V_R = 0V, and limits apply for $-55°C \leq T_A \leq +125°C$ for the LF11331, 2, 3 and the LF11202, 2, $-25°C \leq T_A \leq +85°C$ for the LF13331, 2, 3 and the LF13201, 2.

Note 3: These parameters are limited by the pin to pin capacitance of the package.

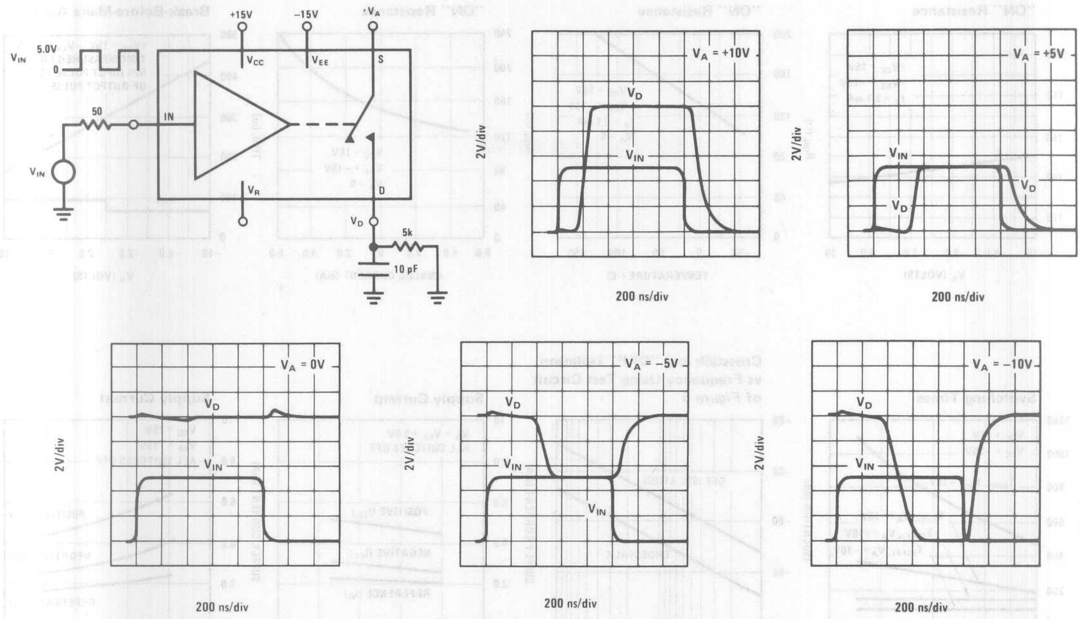
Note 4: This is the analog signal slew rate above which the signal is distorted as a result of finite internal slew rates.

Note 5: All switches in the device are turned "OFF" by saturating a transistor at the disable node as shown in *Figure 5.* The delay times will be approximately equal to the t_{ON} or t_{OFF} plus the delay introduced by the external transistor.

Note 6: This graph indicates the analog current at which 1% of the analog current is lost when the drain is positive with respect to the source.

Test Circuit and Typical Performance Curves

Delay Time, Rise Time, Settling Time, and Switching Transients



Additional Test Circuits

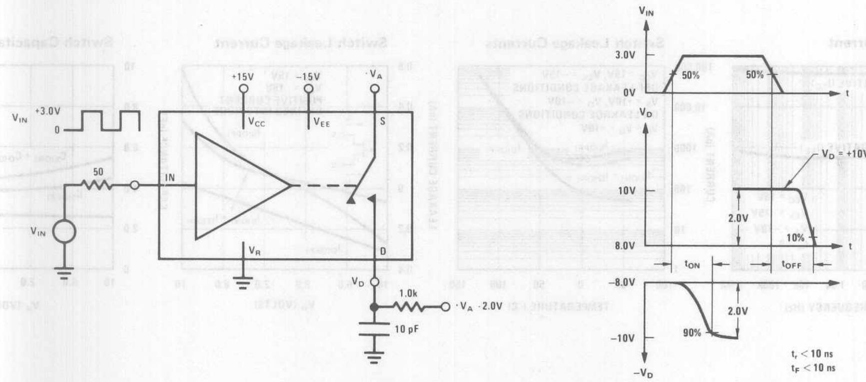
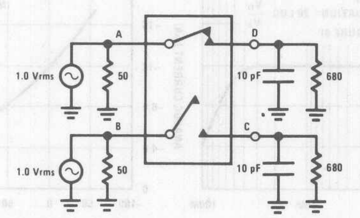


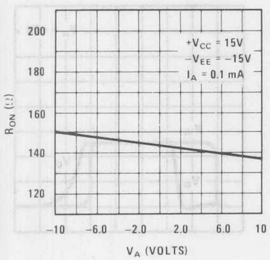
FIGURE 3. t_{ON}, t_{OFF} Test Circuit and Waveforms for a Normally Open Switch



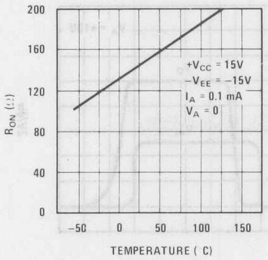
OFF ISOLATION = 20 log $\frac{|V_C|}{|V_B|}$ CROSSTALK = 20 log $\frac{|V_C|}{|V_A|}$

FIGURE 4. "OFF" Isolation, Crosstalk, Small Signal Response

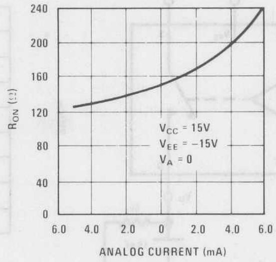
"ON" Resistance



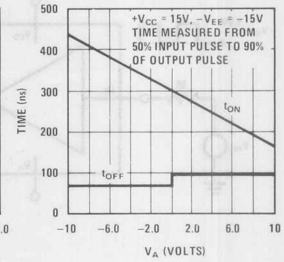
"ON" Resistance



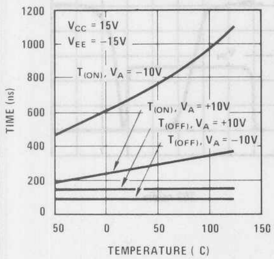
"ON" Resistance



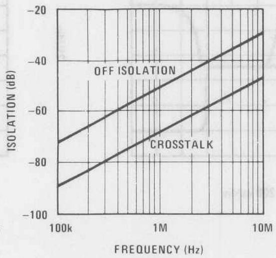
Break-Before-Make Action



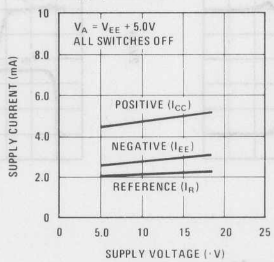
Switching Times



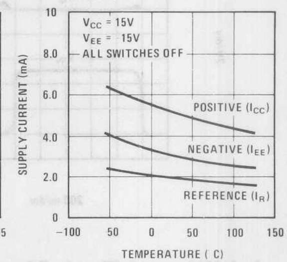
Crosstalk and "OFF" Isolation vs Frequency Using Test Circuit of *Figure 5*



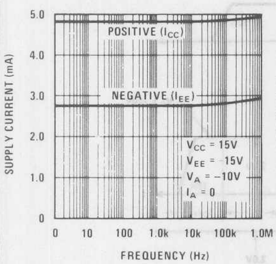
Supply Current



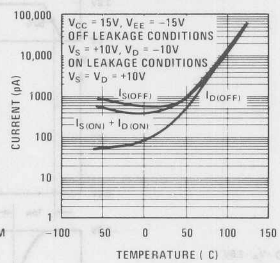
Supply Current



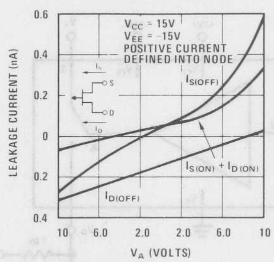
Supply Current



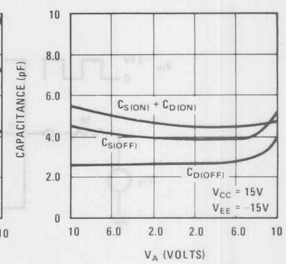
Switch Leakage Currents



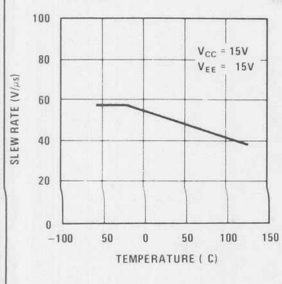
Switch Leakage Current



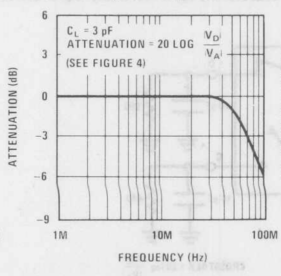
Switch Capacitances



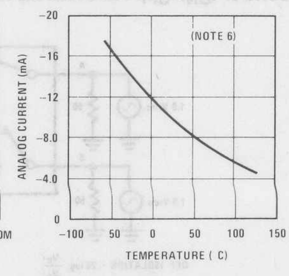
Slew Rate of Analog Voltage Above Which Signal Loading Occurs



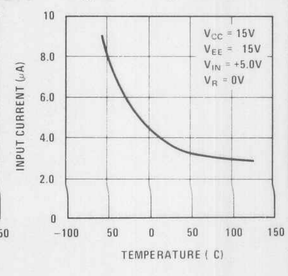
Small Signal Response



Maximum Accurate Analog Current vs Temperature



Logical "1" Input Bias Current



Application Hints

GENERAL INFORMATION

These devices are monolithic quad JFET analog switches with "ON" resistances which are essentially independent of analog voltage or analog current. The leakage currents are typically less than 1 nA at 25°C in both the "OFF" and "ON" switch states and introduce negligible errors in most applications. Each switch is controlled by minimum TTL logic levels at its input and is designed to turn "OFF" faster than it will turn "ON." This prevents two analog sources from being transiently connected together during switching. The switches were designed for applications which require break-before-make action, no analog current loss, medium speed switching times and moderate analog currents.

Because these analog switches are JFET rather than CMOS, they do not require special handling.

LOGIC INPUTS

The logic input (IN), of each switch, is referenced to two forward diode drops (1.4V at 25°C) from the reference supply (V_R) which makes it compatible with DTL, RTL, and TTL logic families. For normal operation, the logic "0" voltage can range from 0.8V to −4.0V with respect to V_R and the logic "1" voltage can range from 2.0V to 6.0V with respect to V_R, provided V_{IN} is not greater than (V_{CC} − 2.5V). If the input voltage is greater than (V_{CC} − 2.5V), the input current will increase. If the input voltage exceeds 6.0V or −4.0V with respect to V_R, a resistor in series with the input should be used to limit the input current to less than 100μA.

ANALOG VOLTAGE AND CURRENT

Analog Voltage

Each switch has a constant "ON" resistance (R_{ON}) for analog voltages from (V_{EE} + 5V) to (V_{CC} − 5V). For analog voltages greater than (V_{CC} − 5V), the switch will remain ON independent of the logic input voltage. For analog voltages less than (V_{EE} + 5V), the ON resistance of the switch will increase. Although the switch will not operate normally when the analog voltage is out of the previously mentioned range, the source voltage can go to either (V_{EE} + 36V) or (V_{CC} + 6V), whichever is more positive, and can go as negative as V_{EE} without destruction. The drain (D) voltage can also go to either (V_{EE} + 36V) or (V_{CC} + 6V), whichever is more positive, and can go as negative as (V_{CC} − 36V) without destruction.

Analog Current

With the source (S) positive with respect to the drain (D), the R_{ON} is constant for low analog currents, but will increase at higher currents (>5 mA) when the FET enters the saturation region. However, if the drain is positive with respect to the source and a small analog current loss at high analog currents (Note 6) is tolerable, a low R_{ON} can be maintained for analog currents greater than 5 mA at 25°C.

LEAKAGE CURRENTS

The drain and source leakage currents, in both the ON and the OFF states of each switch, are typically less than 1 nA at 25°C and less than 100 nA at 125°C. As shown in the typical curves, these leakage currents are dependent on power supply voltages, analog voltage, analog current and the source to drain voltage.

DELAY TIMES

The delay time OFF (t_{OFF}) is essentially independent of both the analog voltage and temperature. The delay time ON (t_{ON}) will decrease as either (V_{CC} − V_A) decreases or the temperature decreases.

POWER SUPPLIES

The voltage between the positive supply (V_{CC}) and either the negative supply (V_{EE}) or the reference supply (V_R) can be as much as 36V. To accommodate variations in input logic reference voltages, V_R can range from V_{EE} to (V_{CC} − 4.5V). Care should be taken to ensure that the power supply leads for the device never become reversed in polarity or that the device is never inadvertantly installed backwards in a test socket. If one of these conditions occurs, the supplies would zener an interal diode to an unlimited current; and result in a destroyed device.

SWITCHING TRANSIENTS

When a switch is turned OFF or ON, transients will appear at the load due to the internal transient voltage at the gate of the switch JFET being coupled to the drain and source by the junction capacitances of the JFET. The magnitude of these transients is dependent on the load. A lower value R_L produces a lower transient voltage. A negative transient occurs during the delay time ON, while a positive transient occurs during the delay time OFF. These transients are relatively small when compared to faster switch families.

DISABLE NODE

This node can be used, as shown in *Figure 5,* to turn all the switches in the unit off independent of logic inputs. Normally, the node floats freely at an internal diode drop (≈ 0.7V) above V_R. When the external transistor in *Figure 5* is saturated, the node is pulled very close to V_R and the unit is disabled. Typically, the current from the node will be less than 1 mA. This feature is not available on the LF11201 or LF11202 series.

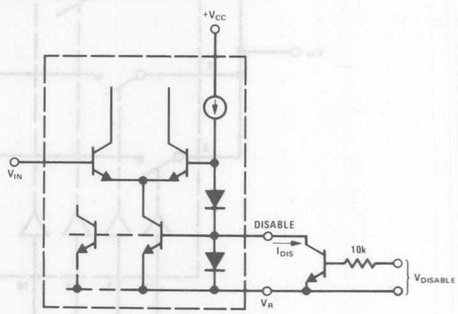
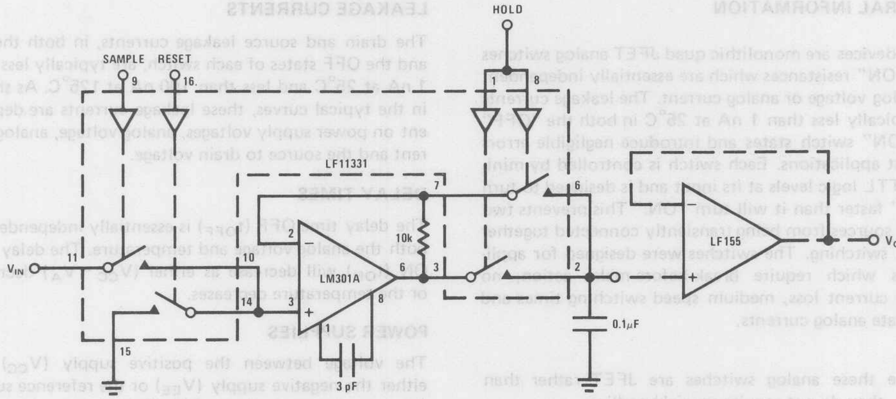


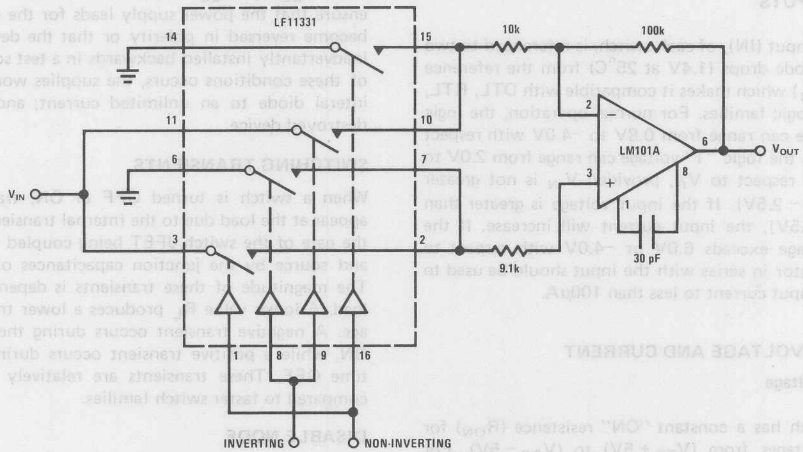
FIGURE 5. Disable Function

Typical Applications

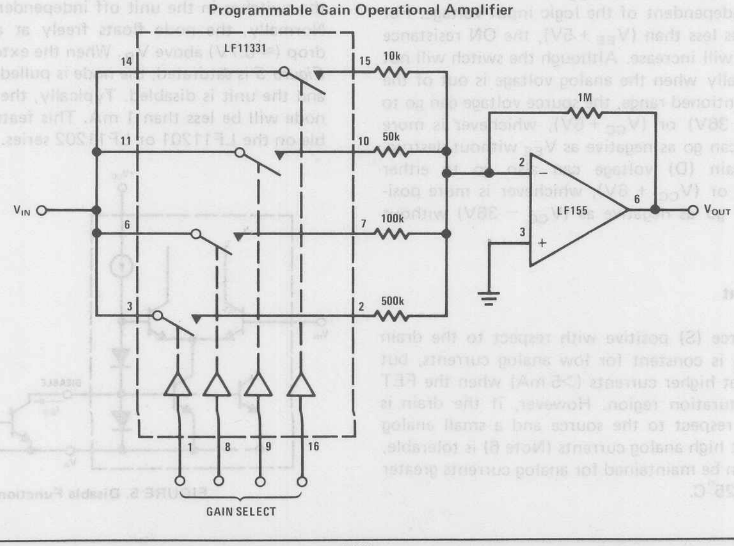
Sample and Hold with Reset



Programmable Inverting Non-Inverting Operational Amplifier

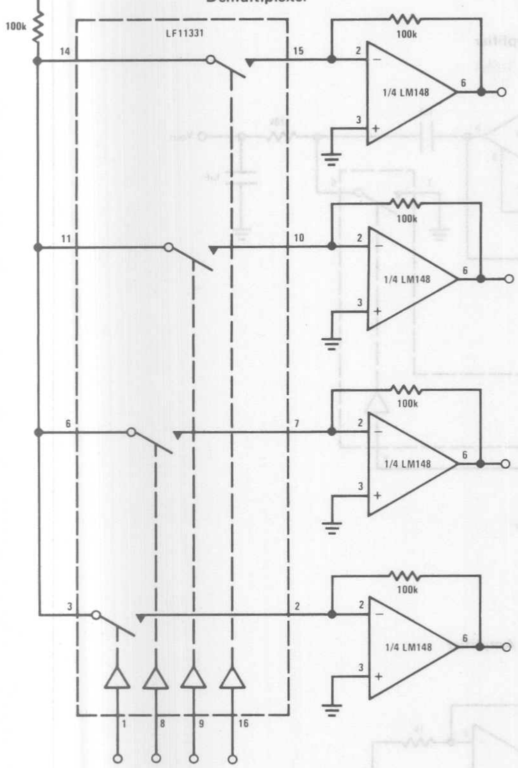


Programmable Gain Operational Amplifier

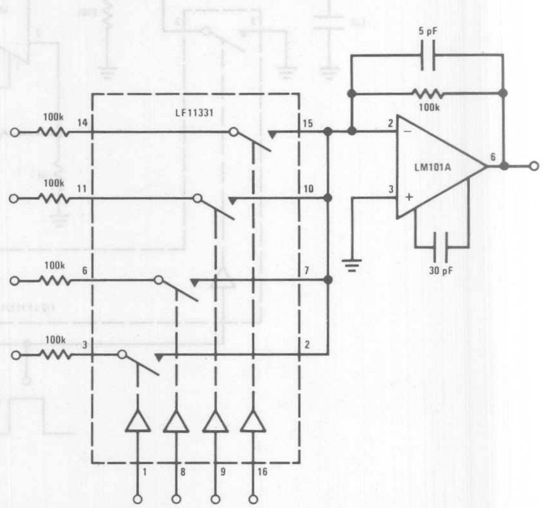


Typical Applications (Continued)

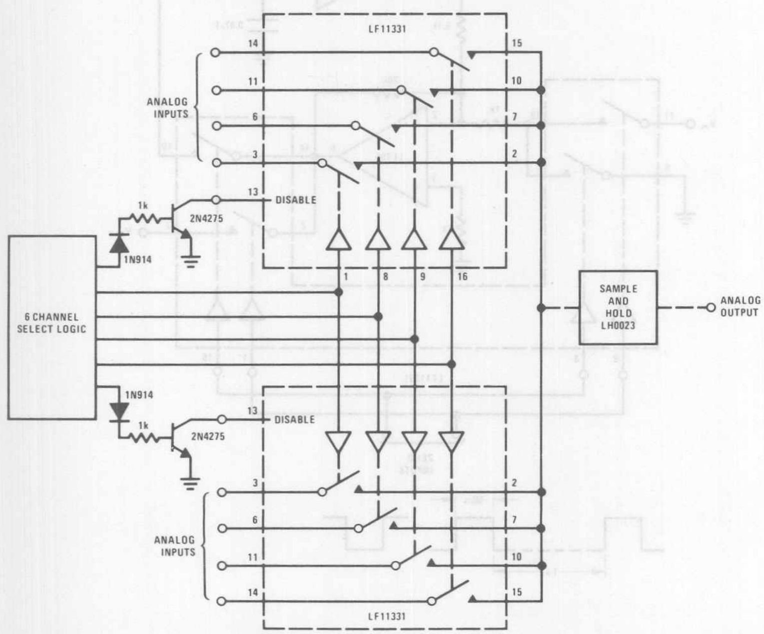
Demultiplexer



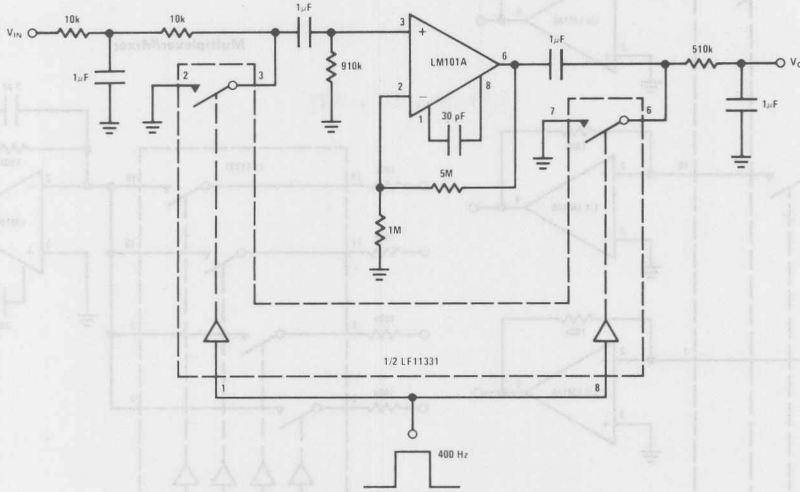
Multiplexer/Mixer



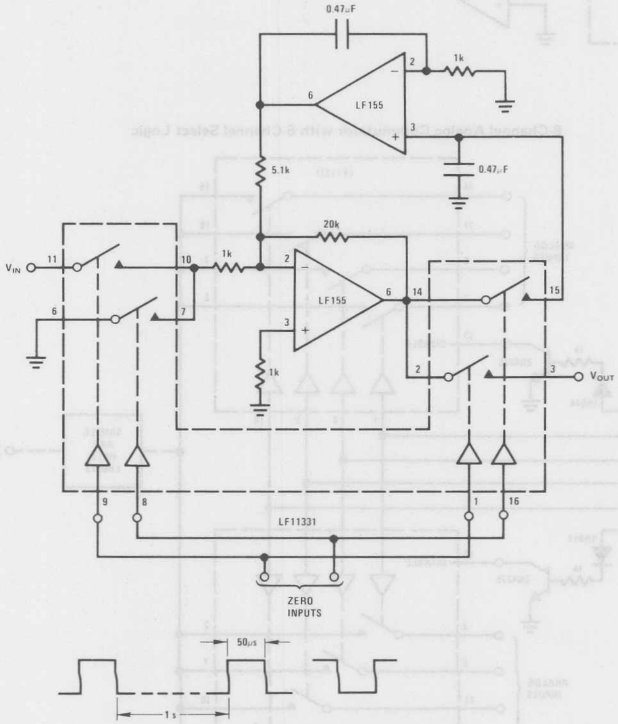
8-Channel Analog Commutator with 6-Channel Select Logic



Chopper Channel Amplifier

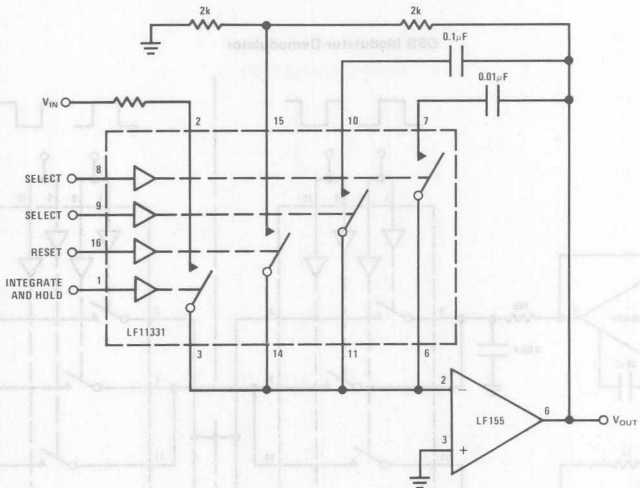


Self-Zeroing Operational Amplifier

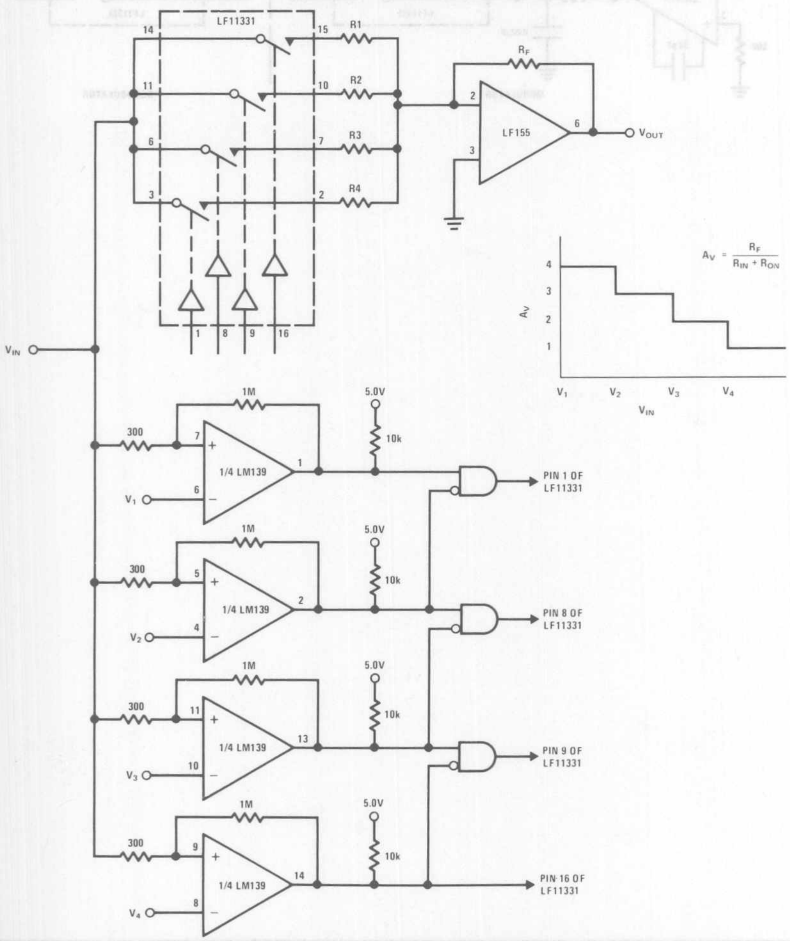


Typical Applications (Continued)

Programmable Integrator with Reset and Hold

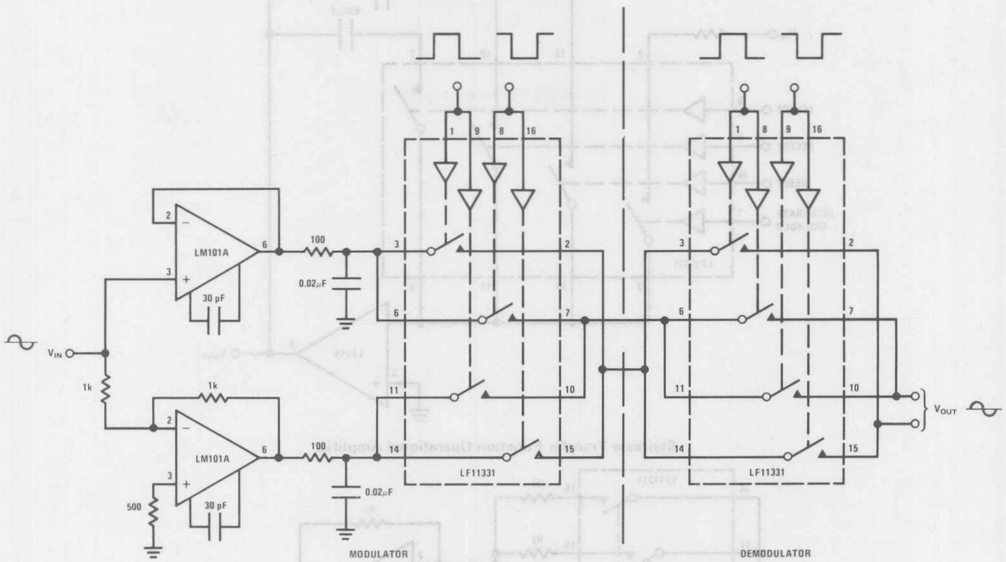


Staircase Transfer Function Operational Amplifier



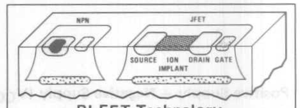
Typical Applications (Continued)

DSB Modulator-Demodulator



National Semiconductor

Analog Switches



BI-FET Technology

LF11508/LF13508 8-Channel Analog Multiplexer
LF11509/LF13509 4-Channel Differential Analog Multiplexer

General Description

The LF11508/LF13508 is an 8-channel analog multiplexer which connects the output to 1 of the 8 analog inputs depending on the state of a 3-bit binary address. An enable control allows disconnecting the output, thereby providing a package select function.

This device is fabricated with National's BI-FET technology which provides ion-implanted JFETs for the analog switch on the same chip as the bipolar decode and switch drive circuitry. This technology makes possible low constant "ON" resistance with analog input voltage variations. This device does not suffer from latch-up problems or static charge blow-out problems associated with similar CMOS parts. The digital inputs are designed to operate from both TTL and CMOS levels while always providing a definite break-before-make action.

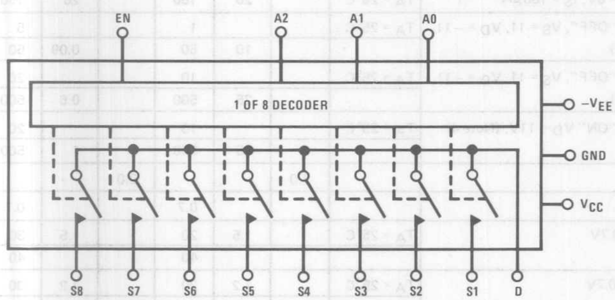
The LF11509/LF13509 is a 4-channel differential analog multiplexer. A 2-bit binary address will connect a pair of independent analog inputs to one of any 4 pairs of independent analog outputs. The device has all the features of the LF11508 series and should be used whenever differential analog inputs are required.

Features

- JFET switches rather than CMOS
- No static discharge blow-out problem
- No SCR latch-up problems
- Analog signal range 11V, −15V
- Constant "ON" resistance for analog signals between −11V and 11V
- "ON" resistance 380 Ω typ
- Digital inputs compatible with TTL and CMOS
- Output enable control
- Break-before-make action: t_{OFF} = 0.2 μs; t_{ON} = 2 μs typ
- Lower leakage devices available

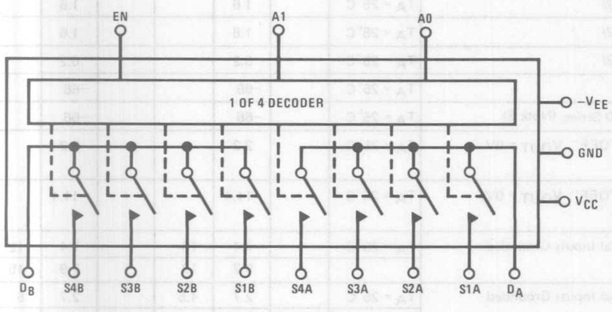
Functional Diagrams and Truth Tables

LF11508/LF13508



EN	A2	A1	A0	SWITCH ON
H	L	L	L	S1
H	L	L	H	S2
H	L	H	L	S3
H	L	H	H	S4
H	H	L	L	S5
H	H	L	H	S6
H	H	H	L	S7
H	H	H	H	S8
L	X	X	X	NONE

LF11509/LF13509



EN	A1	A0	SWITCH PAIR ON
L	X	X	None
H	L	L	S1
H	L	H	S2
H	H	L	S3
H	H	H	S4

	LF11508, LF11509	LF13508, LF13509
Positive Supply — Negative Supply ($V_{CC} - V_{EE}$)	36V	36V
Positive Analog Input Voltage (Note 1)	V_{CC}	V_{CC}
Negative Analog Input Voltage (Note 1)	$-V_{EE}$	$-V_{EE}$
Positive Digital Input Voltage	V_{CC}	V_{CC}
Negative Digital Input Voltage	$-5V$	$-5V$
Analog Switch Current	$\|I_S\| < 10$ mA	$\|I_S\| < 10$ mA
Power Dissipation (P_D at 25°C) and Thermal Resistance (θ_{jA}), (Note 2)		
Molded DIP (N) P_D	—	500 mW
Molded DIP (N) θ_{jA}	—	150°C/W
Cavity DIP (D) P_D	900 mW	900 mW
Cavity DIP (D) θ_{jA}	100°C/W	100°C/W
Maximum Junction Temperature (T_{jMAX})	150°C	100°C
Operating Temperature Range	$-55°C \leq T_A \leq +125°C$	$0°C \leq T_A \leq +70°C$
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	300°C	300°C

Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LF11508, LF11509 MIN	TYP	MAX	LF13508, LF13509 MIN	TYP	MAX	UNITS
R_{ON}	"ON" Resistance	$V_{OUT} = 0V$, $I_S = 100\,\mu A$	$T_A = 25°C$		380	500		380	650	Ω
					600	750		500	850	Ω
ΔR_{ON}	ΔR_{ON} with Analog Voltage Swing	$-10V \leq V_{OUT} \leq +10V$, $I_S = 100\,\mu A$	$T_A = 25°C$		0.01	1		0.01	1	%
R_{ON} Match	R_{ON} Match Between Switches	$V_{OUT} = 0V$, $I_S = 100\,\mu A$	$T_A = 25°C$		20	100		20	150	Ω
$I_{S(OFF)}$	Source Current in "OFF" Condition	Switch "OFF", $V_S = 11$, $V_D = -11$, (Note 4)	$T_A = 25°C$			1			5	nA
					10	50		0.09	50	nA
$I_{D(OFF)}$	Drain Current in "OFF" Condition	Switch "OFF", $V_S = 11$, $V_D = -11$, (Note 4)	$T_A = 25°C$			10			20	nA
					25	500		0.6	500	nA
$I_{D(ON)}$	Leakage Current in "ON" Condition	Switch "ON" $V_D = 11V$, (Note 4)	$T_A = 25°C$			10			20	nA
					35	500		1	500	nA
V_{INH}	Digital "1" Input Voltage			2.0			2.0			V
V_{INL}	Digital "0" Input Voltage					0.7			0.7	V
I_{INL}	Digital "0" Input Current	$V_{IN} = 0.7V$	$T_A = 25°C$		1.5	20		1.5	30	μA
						40			40	μA
$I_{INL(EN)}$	Digital "0" Enable Current	$V_{EN} = 0.7V$	$T_A = 25°C$		1.2	20		1.2	30	μA
						40			40	μA
t_{TRAN}	Switching Time of Multiplexer	*(Figure 1)*, (Note 5)	$T_A = 25°C$		2.0	3		1.8		μs
t_{OPEN}	Break-Before-Make	*(Figure 3)*	$T_A = 25°C$		1.6			1.6		μs
$t_{ON(EN)}$	Enable Delay "ON"	*(Figure 2)*	$T_A = 25°C$		1.6			1.6		μs
$t_{OFF(EN)}$	Enable Delay "OFF"	*(Figure 2)*	$T_A = 25°C$		0.2			0.2		μs
$I_{SO(OFF)}$	"OFF" Isolation	(Note 6)	$T_A = 25°C$		−66			−66		dB
CT	Crosstalk	LF11509 Series, (Note 6)	$T_A = 25°C$		−66			−66		dB
$C_{S(OFF)}$	Source Capacitance ("OFF")	Switch "OFF", $V_{OUT} = 0V$, $V_S = 0V$	$T_A = 25°C$		2.2			2.2		pF
$C_{D(OFF)}$	Drain Capacitance ("OFF")	Switch "OFF", $V_{OUT} = 0V$, $V_S = 0V$	$T_A = 25°C$		11.4			11.4		pF
I_{CC}	Positive Supply Current	All Digital Inputs Grounded	$T_A = 25°C$		7.4	10		7.4	12	mA
					9.2	13		7.9	15	mA
I_{EE}	Negative Supply Current	All Digital Inputs Grounded	$T_A = 25°C$		2.7	4.5		2.7	5	mA
					2.9	5.5		2.8	6	mA

Notes

Note 1: If the analog input voltage exceeds this limit, the input current should be limited to less than 10 mA.

Note 2: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{jMAX}, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_D = (T_{jMAX} - T_A)/\theta_{jA}$ or the 25°C P_{DMAX}, whichever is less.

Note 3: These specifications apply for $V_S = \pm 15V$ and over the absolute maximum operating temperature range ($T_L \leq T_A \leq T_H$) unless otherwise noted.

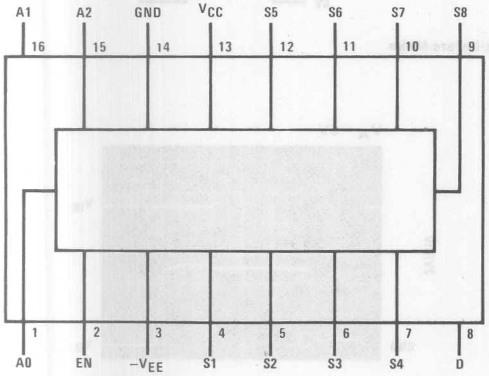
Note 4: Conditions applied to leakage tests insure worse case leakages. Exceeding 11V on the analog input may cause an "OFF" channel to turn "ON".

Note 5: Lots are sample tested to this parameter. The measurement conditions of *Figure 1* insure worse case transition time.

Note 6: "OFF" isolation is measured with all switches "OFF" and driving a source. Crosstalk is measured with a pair of switches "ON", driving channel A and measuring channel B. $R_L = 200$, $C_L = 7$ pF, $V_S = 3$ Vrms, f = 500 kHz.

Connection Diagrams

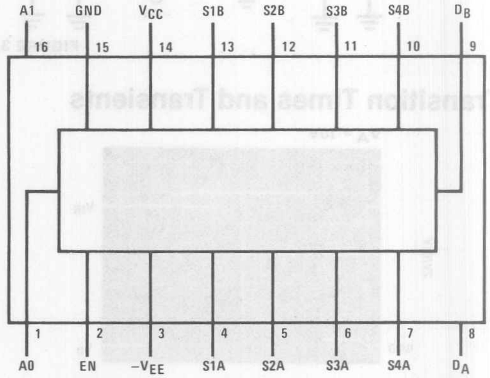
LF11508/LF13508
Dual-In-Line Package



TOP VIEW

Order Number LF11508D or LF13508D
See NS Package D16C
Order Number LF13508N
See NS Package N16A

LF11509/LF13509
Dual-In-Line Package



TOP VIEW

Order Number LF11509D or LF13509D
See NS Package D16C
Order Number LF13509N
See NS Package N16A

AC Test Circuits and Switching Time Waveforms

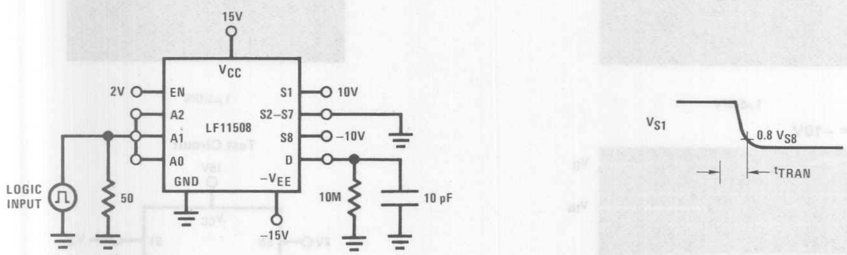


FIGURE 1. Transition Time

AC Test Circuit and Switching Time Waveforms (Continued)

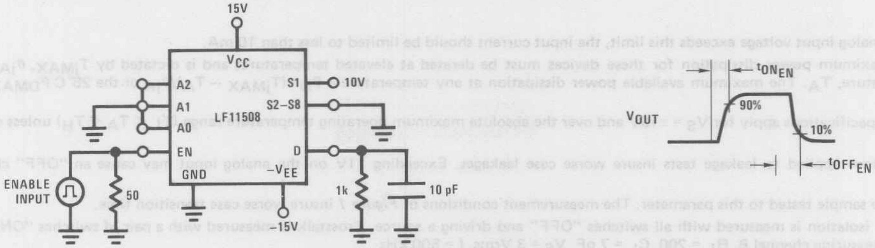


FIGURE 2. Enable Times

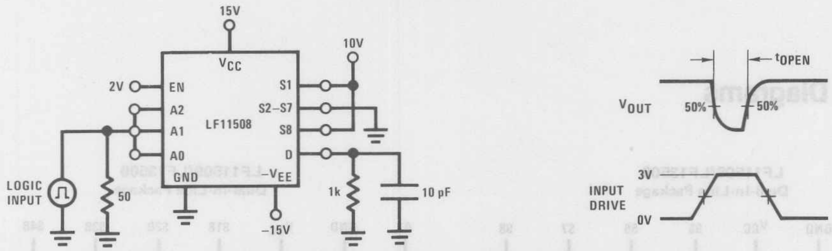
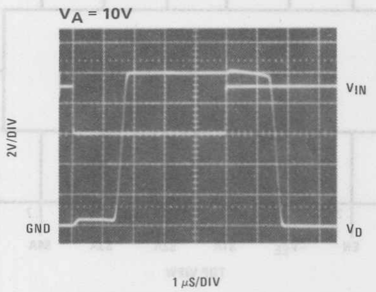
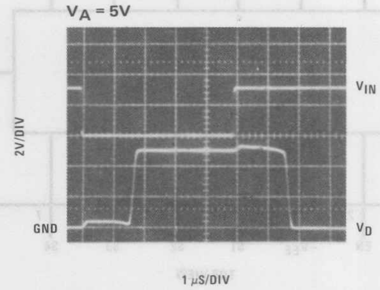
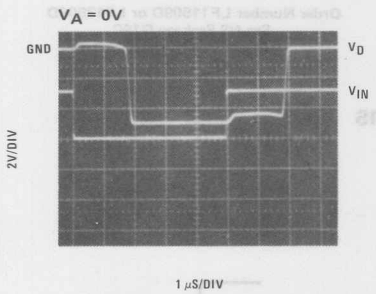


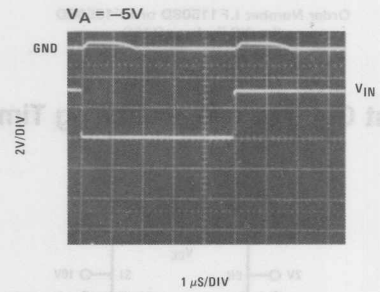
FIGURE 3. Break-Before-Make

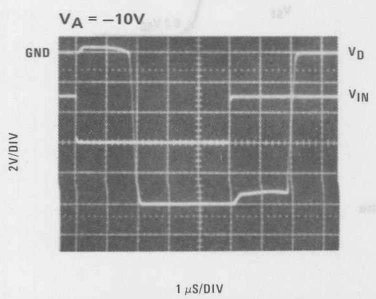
Transition Times and Transients



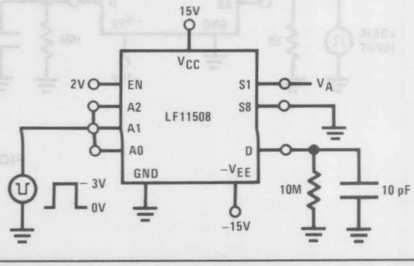






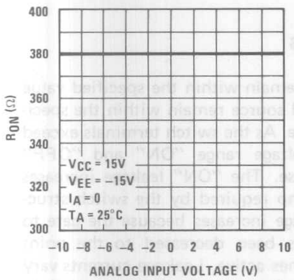


Test Circuit

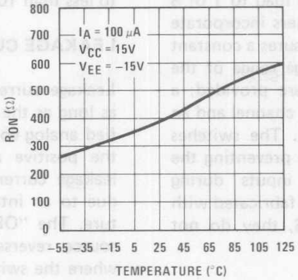


Typical Performance Characteristics

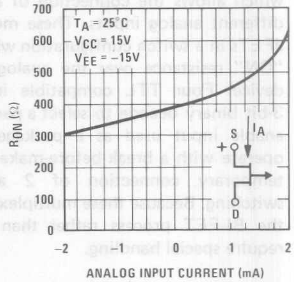
“ON” Resistance



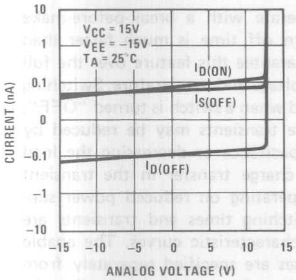
“ON” Resistance



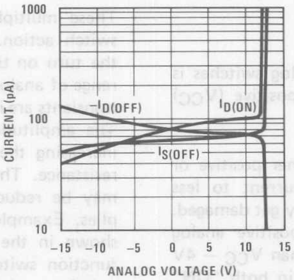
“ON” Resistance



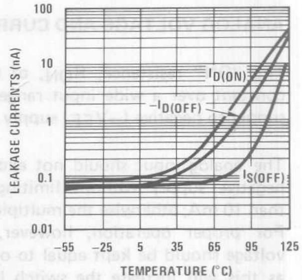
Switch Leakage Currents



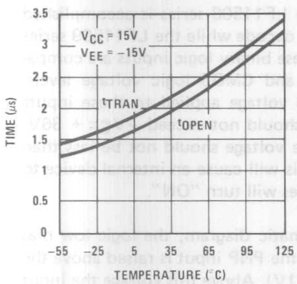
Switch Leakage Currents



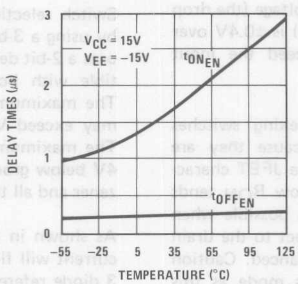
Switch Leakage Currents



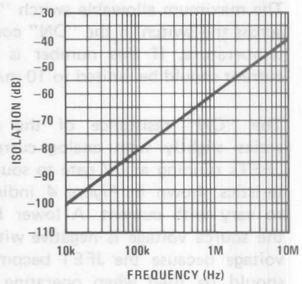
Switching Times (Figures 1 and 3)



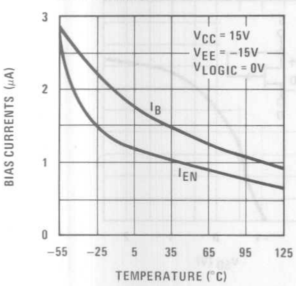
Enable Delay Times (Figure 2)



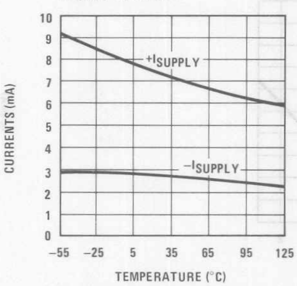
“OFF” Isolation and Crosstalk



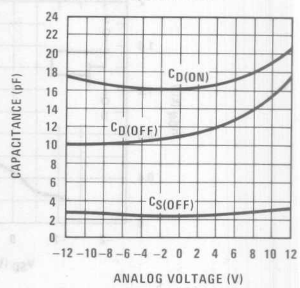
Bias Currents



Supply Currents



Switch Capacitances



JFETs in a switch configuration which insures a constant "ON" resistance over the analog voltage range of the device. Four TTL compatible inputs are provided; a 3-bit binary decode to select a particular channel and an enable input used as a package select. The switches operate with a break-before-make action preventing the temporary connection of 2 analog inputs during switching. Because these multiplexers are fabricated with the BI-FET process rather than CMOS, they do not require special handling.

The LF11509 series is a 4-channel differential multiplexer which allows two loads to be connected to 1 of 4 different pairs of analog inputs. The LF11509 series also has all the features of the LF11508.

ANALOG VOLTAGE AND CURRENT

The "ON" resistance, R_{ON}, of the analog switches is constant over a wide input range from positive (V_{CC}) supply to negative ($-V_{EE}$) supply.

The analog input should not exceed either positive or negative supply without limiting the current to less than 10 mA; otherwise the multiplexer may get damaged. For proper operation, however, the positive analog voltage should be kept equal to or less than $V_{CC} - 4V$ as this will increase the switch leakage in both "ON" and "OFF" state and it may also cause a false turn "ON" of a normally "OFF" switch. This limit applies over the full temperature range.

The maximum allowable switch "ON" voltage (the drop across the switch in the "ON" condition) is ±0.4V over temperature. If this number is to exceed the input current should be limited to 10 mA.

The "ON" resistance of the multiplexing switches varies slightly with analog current because they are JFETs running at 0V gate to source. The JFET characteristics shown in *Figure 4* indicates how R_{ON} tends to vary with current. A lower R_{ON} is possible when the source voltage is negative with respect to the drain voltage because the JFET becomes enhanced. Caution should be used when operating in this mode as this may forward-bias an internal transistor and cause high currents to flow in the switches. Thus, the drain voltage should never be greater than 0.4V positive with respect

LEAKAGE CURRENTS

Leakage currents will remain within the specified value as long as the drain and source remain within the specified analog voltage range. As the switch terminals exceed the positive analog voltage range "ON" and "OFF" leakage currents increase. The "ON" leakage increases due to an internal clamp required by the switch structure. The "OFF" leakage increases because the gate to source reverse bias has been decreased to the point where the switch becomes active. Leakage currents vary slightly with analog voltage and will approximately double for every 10°C rise in temperature.

SWITCHING TIMES AND TRANSIENTS

These multiplexers operate with a break-before-make switch action. The turn off time is much faster than the turn on time to guarantee this feature over the full range of analog input voltage and temperature. Switching transients are introduced when a switch is turned "OFF". The amplitude of these transients may be reduced by increasing the load capacitance or decreasing the load resistance. The actual charge transfer in the transient may be reduced by operating on reduced power supplies. Examples of switching times and transients are shown in the typical characteristic curves. The enable function switching times are specified separately from switch-to-switch transition times and may be thought of as package-to-package transition times.

LOGIC INPUTS AND ENABLE INPUT

Switch selection in the LF11508 series is accomplished by using a 3-bit binary decode while the LF11509 series uses a 2-bit decode. These binary logic inputs are compatible with both TTL and CMOS logic voltage levels. The maximum positive voltage applied to these inputs may exceed V_{CC} but should not exceed $-V_{EE} + 36V$. The maximum negative voltage should not be less than 4V below ground as this will cause an internal device to zener and all the switches will turn "ON".

As shown in the schematic diagram, the logic low bias current will flow until the PNP input is raised above the 3 diode reference (≈ 2.1V). Above this voltage the input device becomes reverse biased and the input current drops to the leakage of the reverse biased junction (< 0.1 μA).

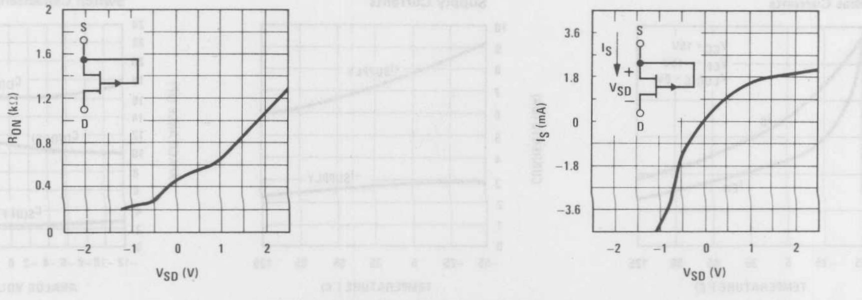


FIGURE 4. JFET Characteristics

Typical Applications

DATA ACQUISITION SYSTEM

A SIMPLIFIED SYSTEM DISCUSSION

Analog multiplexers (MUX) are usually used for multi-channel Data Acquisition Units (DAU). *Figure 5* shows a system in which 8 different analog inputs are sampled and converted into digital words for further processing. The sample and hold circuit is optional, depending on input speed requirements and on A/D converter speed.

Parameters characterizing the system are:

System Channels: The number of multiplexer channels.

Accuracy: The conversion accuracy of each individual sample with the system operating at the throughput rate.

Speed or Throughput Rate: Number of samples/second/channel the system can handle.

For a discussion on system structure, addressing mode and processor interfacing, see application note AN-159.

A. ACCURACY CONSIDERATIONS

1. Multiplexer's Influence on System Accuracy *(Figure 6).*

a. The error, (E), caused by the finite "ON" resistance, R_{ON}, of the multiplexing switches is given by:

$$E(\%) = \frac{100}{1 + R_{IN}/(R_{ON} + R_S + \Delta R_{ON})} \quad \text{where:}$$

R_{IN} = following stage input impedance

ΔR_{ON} = "ON" resistance modulation which is negligible for JFET switches like the LF11508

Example: Let $R_{ON} = 450\ \Omega$, $\Delta R_{ON} = 0$, $R_S = 0$, $T_A = 25^\circ C$ and allowable $E = 0.01\%$ which is equivalent to 1/2 LSB in a 12-bit system:

$$R_{IN}\Big|_{min} = \frac{R_{ON}(100-E)}{E} = 4.5\ M\Omega$$

Note that if temperature effects are included, some gain (or full scale) drift will occur; but effects on linearity are small.

b. Multiplexer settling time (t_s):

$t_s(ON)$: is the time required for the MUX output to settle within a predetermined accuracy, as shown in Table I.

C_S *(Figure 6):* MUX output capacitance + following stage input capacitance + any stray capacitance at this node.

TABLE I.

ERROR %	BITS	t_s(ON) TO 1/2 LSB
0.2	8	6.2t
0.05	10	7.6t
0.01	12	9t
0.0008	16	11.8t

$t = C_S\ (R_{ON} + R_S) \| R_{IN}$

$t_s(OFF)$: is the time it takes to discharge C_S within a tolerable error. The "OFF" settling time should be taken into account for bipolar inputs where its effects will appear as a worse case doubling of the $t_s(ON)$.

2. Sample and Hold Influence on System Accuracy

The sample and hold, if used, also introduces errors into the system accuracy due to:

- Offset voltage of sample and hold
- Droop rate in the Hold mode
- T_A: Aperture time or time delay between the time of a digital Hold command and the actual Hold occurance
- Taq: Acquisition time or time it takes to acquire an analog input and settle within a predetermined error band
- Hold step: Error created during the Sample to Hold mode caused by an undesirable charge injected into the Hold capacitor C_h.

For more details on sample and hold errors, see the LF198/LF298/LF398 data sheet.

3. A/D Converter Influence on System Accuracy

The "accuracy" of the A/D converter is the best possible system accuracy. In most data acquisition systems, the A/D converter is the most expensive single component, so its error will often dominate system error. Care should be taken that MUX, S/H and input source errors do not exceed system error requirements when *added* to A/D errors. For instance, if an 8-bit accuracy system is desired and an 8-bit A/D converter is used, the accuracy of the MUX and S/H should be far better than 8 bits.

For details on A/D converter specifications, see AN-156.

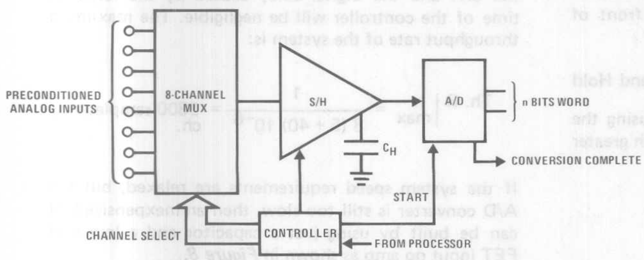


FIGURE 5. Random-Addressed, Multiplexed DAU

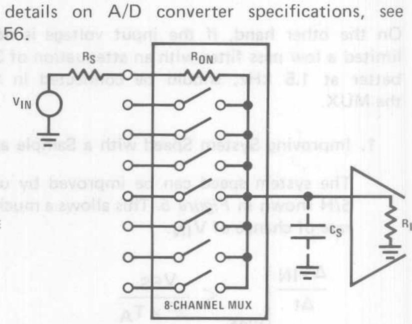


FIGURE 6. 8-Channel MUX

Typical Applications (Continued)

B. SPEED CONSIDERATIONS

In the system of *Figure 5* with the S/H omitted, if n-bit accuracy is desired, the change of the analog input voltage should be less than ±1/2 LSB over the A/D conversion time T_C. In other words, the analog input slew rate, (rate of change of input voltage), will cause a slew-induced error and its magnitude, with respect to the total system error, will depend on the particular application.

$$\left.\frac{\Delta V_{IN}}{\Delta t}\right|_{max} < \frac{\pm 1/2\ LSB}{T_C} = \frac{V_{FS}}{2^n \times T_C}$$

where V_{FS} is the full scale voltage of the A/D. Note that slew induced errors are not affected by the MUX switch time since we can let the unit settle before starting conversion.

Example: Let $T_C = 40\ \mu s$ (MM4357), $V_{FS} = 10V$ and $n = 8$.

$$\left.\frac{\Delta V_{IN}}{\Delta t}\right|_{max} < \frac{1\ mV}{\mu s}$$

which is a very small number. A 10 Vp-p sine wave of a frequency greater than 32 Hz will have higher slew rate than this. The maximum throughput rate of the above 8-channel system would be calculated using both the A/D conversion time and the sum of MUX switch "ON" time and settling time, i.e.:

$$Th.\ R\Big|_{max} = \frac{1}{8\ (T_C + T_{MUX})} = 3k\ \text{samples/sec/channel}$$

$$T_{MUX} = T_{ON} + T_{S(ON)}$$

Also notice that Nyquist sampling criteria would allow each channel to have a signal bandwidth of 1.5 kHz max, while the slew limit dictates a maximum frequency of 32 Hz. If the input signal has a peak-to-peak voltage less than 10V, the allowable maximum input frequency can be calculated by:

$$f_{MAX} = \frac{(\text{Slew Rate})max}{\pi\ Vp\text{-}p}$$

On the other hand, if the input voltage is not band-limited a low pass filter with an attenuation of 30 dB or better at 1.5 kHz, should be connected in front of the MUX.

1. Improving System Speed with a Sample and Hold

   The system speed can be improved by using the S/H shown in *Figure 5*. This allows a much greater rate of change of V_{IN}.

$$\left.\frac{\Delta V_{IN}}{\Delta t}\right|_{max} < \frac{V_{FS}}{2^n \times T_A}$$

where T_A is the aperture time of the S/H. This represents an input slew rate improvement by a factor: T_C/T_A. Here again, the slew rate error is not affected by the acquisition time of the Sample and Hold since conversion will start after the S/H has settled. *An important thing to notice is that the sample and hold errors will add to the total system error budget; therefore, the inequality of the $\Delta V_{IN}/\Delta t$ expression should become more stringent.*

Example: $T_C = 40\ \mu s, T_A = 0.5\ \mu s, n = 8: T_C/T_A = 80$

So the use of a S/H allows a speed improvement by nearly two orders of magnitude.

The maximum throughput rate can be calculated by:

$$Th.\ R\Big|_{max} = \frac{1}{8\ (T_A + Taq + T_C)}$$

Notice that T_{MUX} does not affect the $\Delta V_{IN}/\Delta t$ expression *nor the throughput rate* of the system since it may be switched and settled while the Sample and Hold is in the Hold mode. This is true, provided that: $T_{MUX} < T_A + T_C$.

C. SYSTEM EXAMPLE *(Figure 7)*

The LF398 S/H with a 1000 pF hold capacitor, has an acquisition time of 4 μs to 0.1% (1/4 LSB error for 8 bits) and an aperture time of less than 200 μs. On the other hand, after the hold command, the output will settle to ±0.05 mV in 1 μs. This, together with the acquisition time, introduces approximately a ±1/4 LSB error. Allowing another 1/4 LSB error for hold step and gain non-linearity, the maximum slew error ($\Delta V_{IN}/\Delta t$) should not exceed 1/4 LSB or:

$$\frac{\Delta V_{IN}}{\Delta t} \leq \frac{1}{4} \times \frac{1}{256} \times \frac{1}{T_A} \approx 5\ mV/\mu s$$

(which is the maximum slew rate of a 5 V peak sine wave. Also notice that, due to the above input slew restrictions, the analog delay caused by the finite BW of the S/H and the digital delay caused by the response time of the controller will be negligible. The maximum throughput rate of the system is:

$$Th.\ R\Big|_{max} = \frac{1}{8\ (5 + 40)\ 10^{-6}} = 2800\ \text{samples/sec/ch.}$$

If the system speed requirements are relaxed, but the A/D converter is still too slow, then an inexpensive S/H can be built by using just a capacitor and a low cost FET input op amp as shown in *Figure 8*.

Typical Applications (Continued)

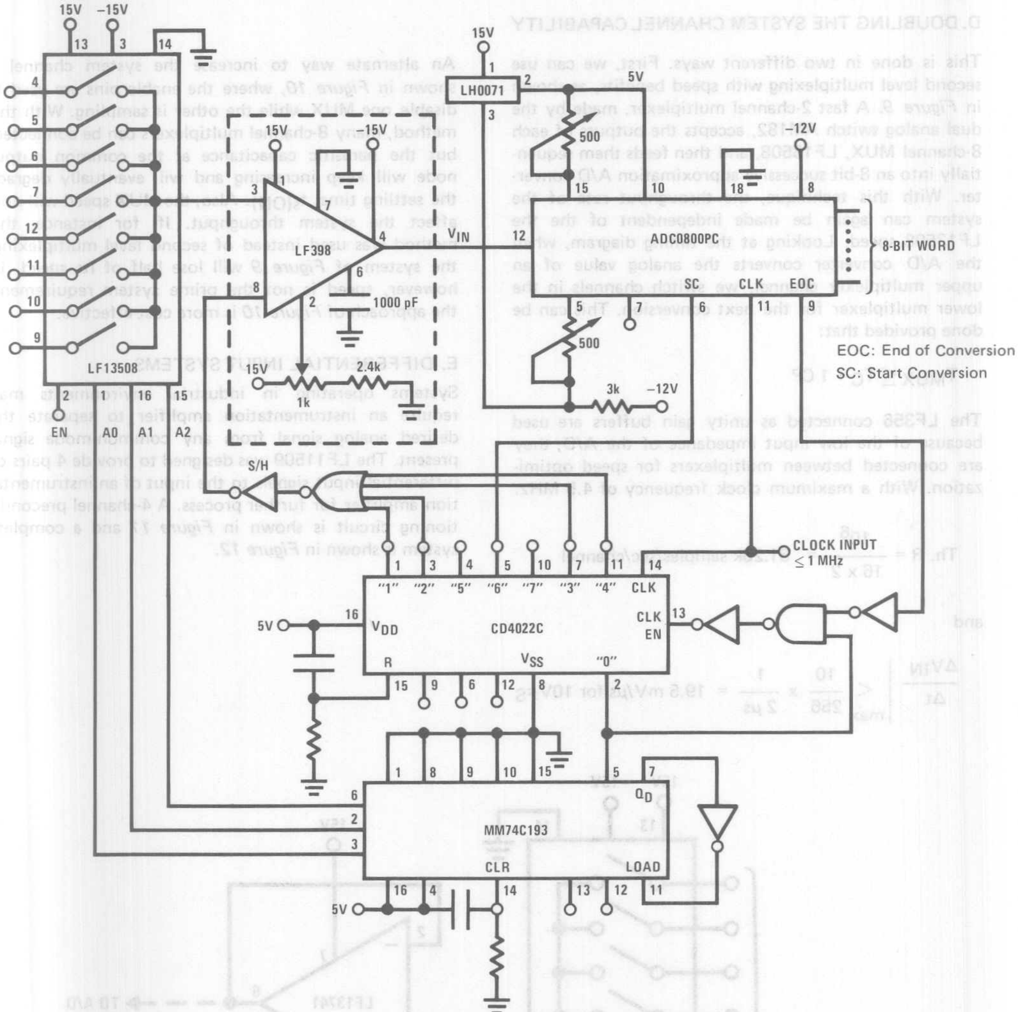


FIGURE 7a. Sequentially Multiplexed DAU with Sample and Hold

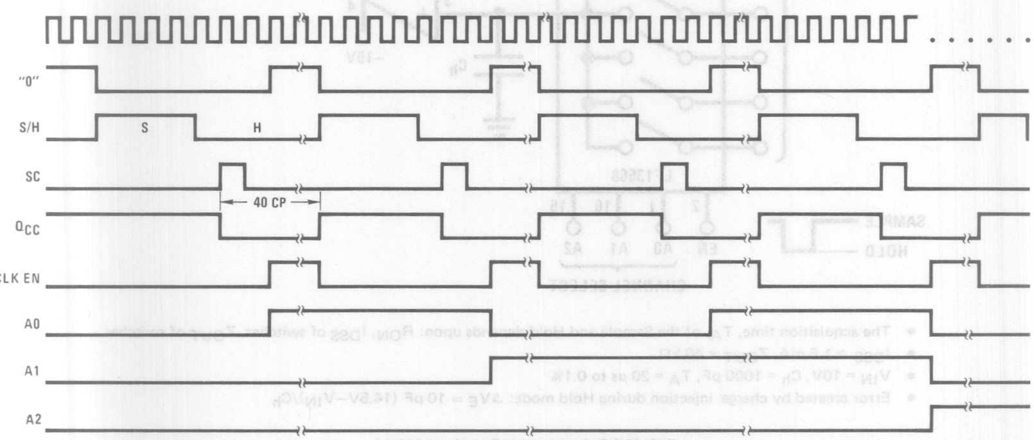


FIGURE 7b. Timing Diagram

This is done in two different ways. First, we can use second level multiplexing with speed benefits, as shown in *Figure 9*. A fast 2-channel multiplexer, made by the dual analog switch AM182, accepts the outputs of each 8-channel MUX, LF13508, and then feeds them sequentially into an 8-bit successive approximation A/D converter. With this technique, the throughput rate of the system can again be made independent of the the LF13508 speed. Looking at the timing diagram, when the A/D converter converts the analog value of an upper multiplexer channel, we switch channels in the lower multiplexer for the next conversion. This can be done provided that:

$$T_{MUX} \leq T_C + 1\ CP$$

The LF356 connected as unity gain buffers are used because of the low input impedance of the A/D; they are connected between multiplexers for speed optimization. With a maximum clock frequency of 4.5 MHz:

$$\text{Th. R} = \frac{10^6}{16 \times 2} = 31.25\text{k samples/sec/channel}$$

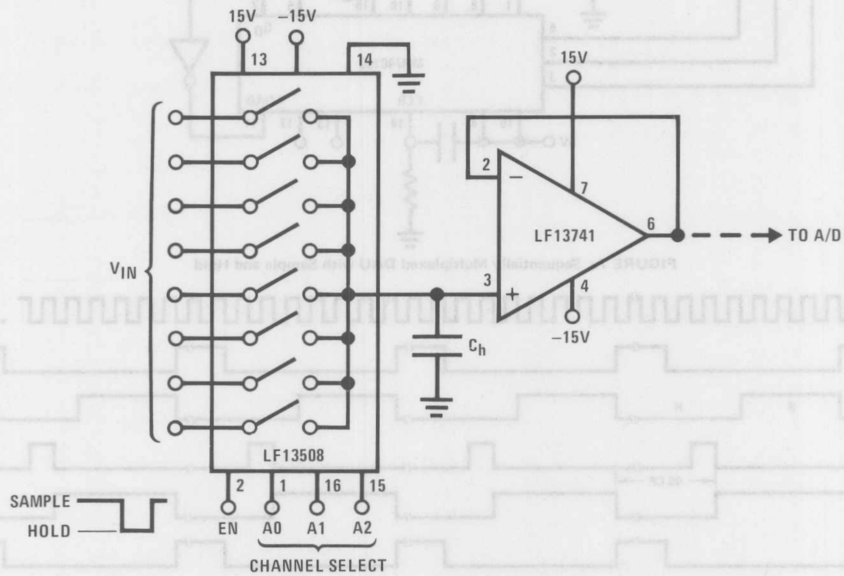
and

$$\left.\frac{\Delta V_{IN}}{\Delta t}\right|_{max} < \frac{10}{256} \times \frac{1}{2\ \mu s} = 19.5\ \text{mV}/\mu\text{s for } 10V_{FS}$$

An alternate way to increase the system channel is shown in *Figure 10*, where the enable pins are used to disable one MUX while the other is sampling. With this method, many 8-channel multiplexers can be connected, but the parasitic capacitance at the common output node will keep increasing and will eventually degrade the settling time, $t_{s(ON)}$. Also, the MUX speed will now affect the system throughput. If, for instance, this method was used instead of second level multiplexing, the system of *Figure 9* will lose half of its speed. If, however, speed is not the prime system requirement, the approach of *Figure 10* is more cost effective.

E. DIFFERENTIAL INPUT SYSTEMS

Systems operating in industrial environments may require an instrumentation amplifier to separate the desired analog signal from any common-mode signal present. The LF11509 was designed to provide 4 pairs of differential input signals to the input of an instrumentation amplifier for further process. A 4-channel preconditioning circuit is shown in *Figure 11* and a complete system is shown in *Figure 12*.



- The acquisition time, T_A, of the Sample and Hold depends upon: R_{ON}, I_{DSS} of switches, Z_{OUT} of switches
- $I_{DSS} \cong 1.5$ mA, $Z_{OUT} = 40\ k\Omega$
- $V_{IN} = 10V$, $C_h = 1000$ pF, $T_A = 20\ \mu s$ to 0.1%
- Error created by charge injection during Hold mode: $\Delta V_E \simeq 10\ \text{pF}\ (14.5V - V_{IN})/C_h$

FIGURE 8. Inexpensive Sample and Hold

Typical Applications (Continued)

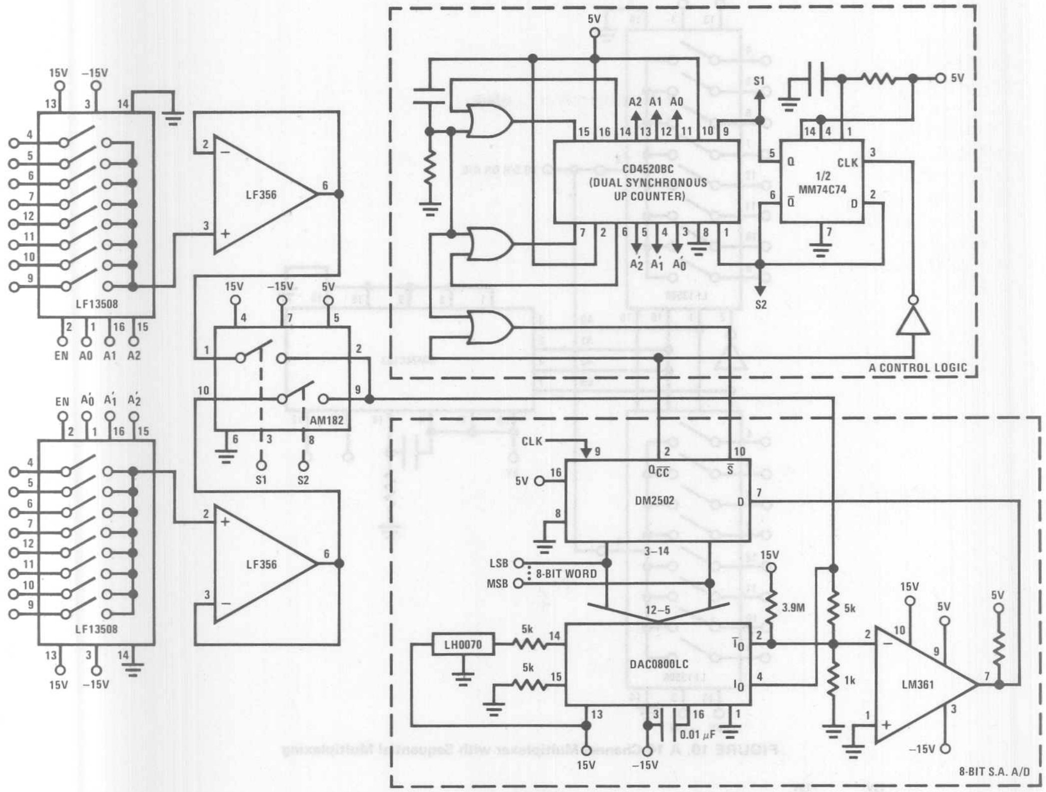


FIGURE 9a. A Fast 16-Channel DAU with Second Level Multiplexing

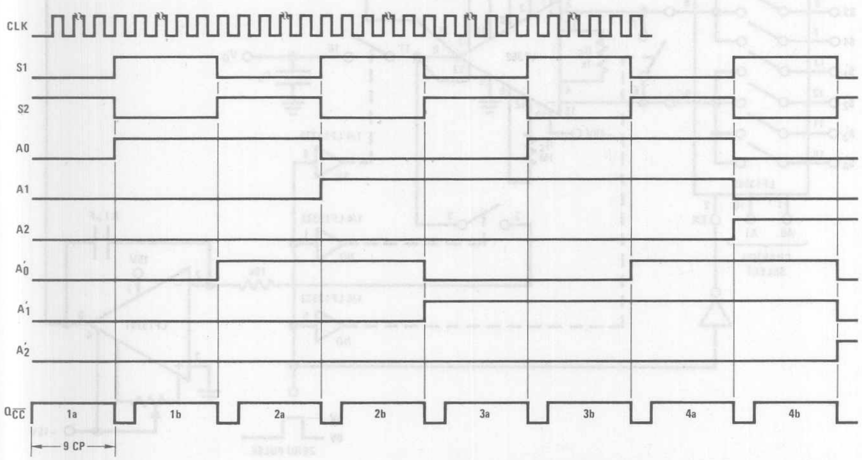


FIGURE 9b. Timing Diagram

Typical Applications (Continued)

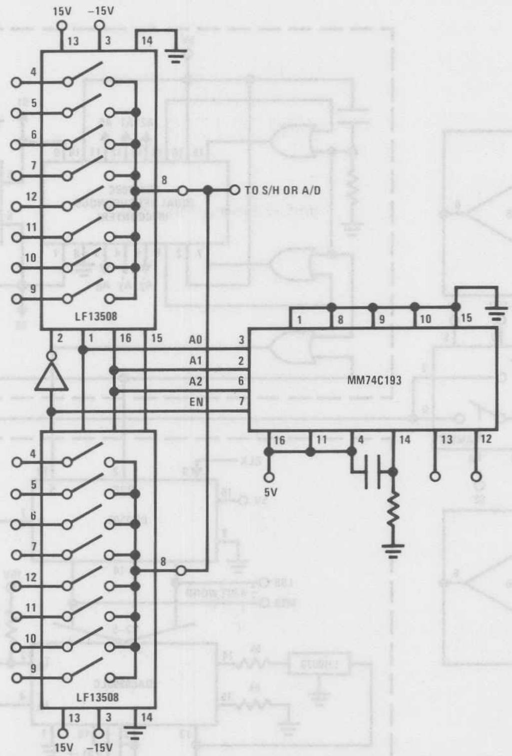
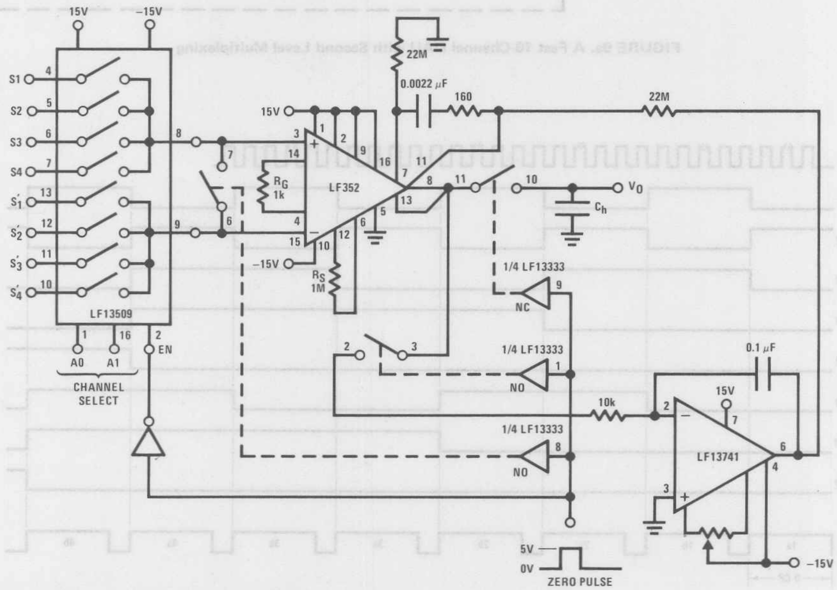


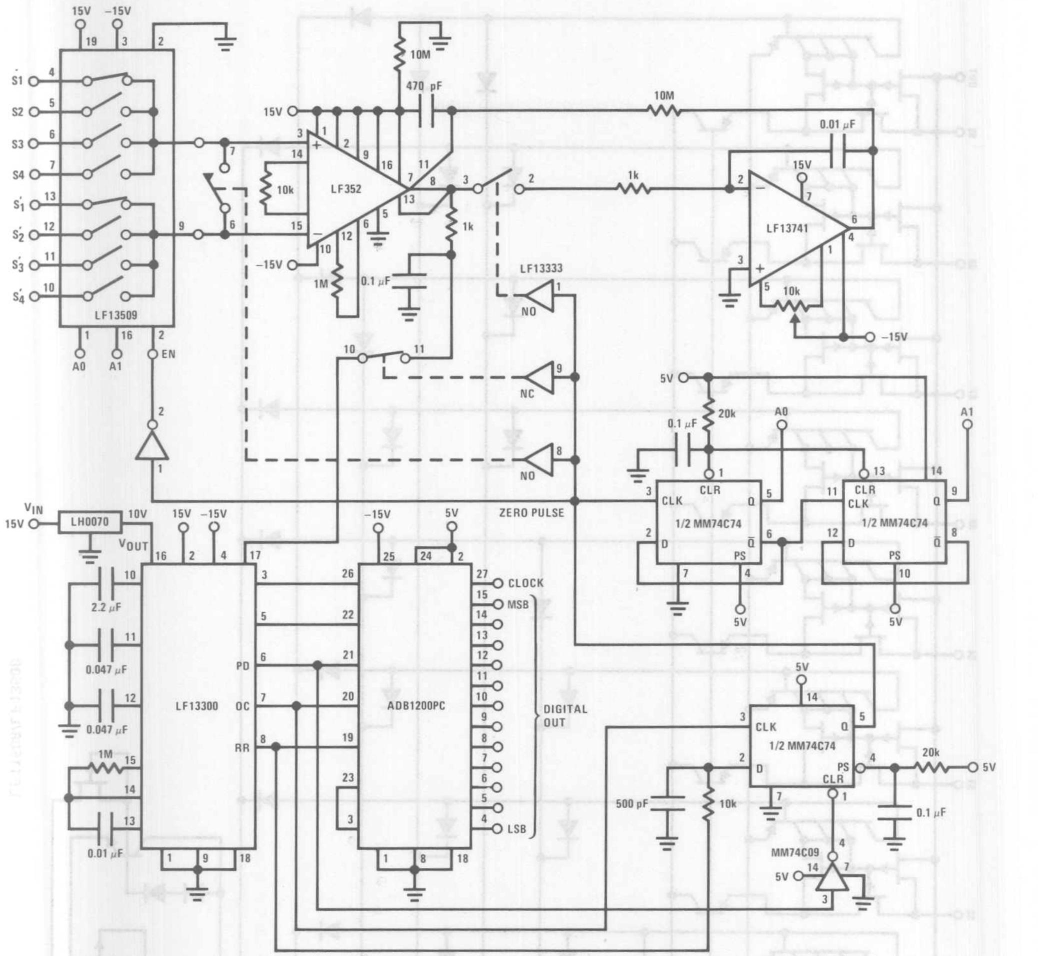
FIGURE 10. A 16-Channel Multiplexer with Sequential Multiplexing



- Differential multiplexer disabled during auto zeroing
- Minimum zeroing pulse width will depend upon the integrator R1C
- This scheme provides input offset adjust especially useful with high gain connections. The device, LF352, provides pins for output offset adjust. For more details, see LF352 data sheet.

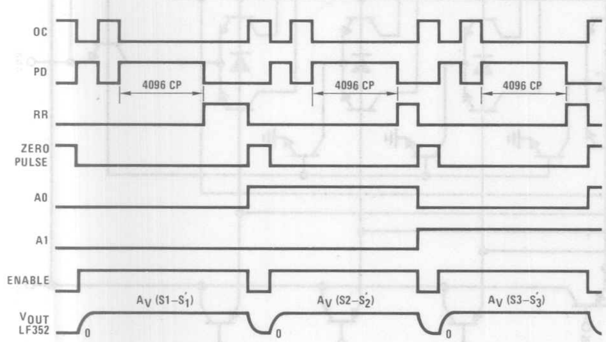
FIGURE 11. 4-Channel Differential Multiplexer with Auto Zeroed Instrumentation Amplifier

Typical Applications (Continued)



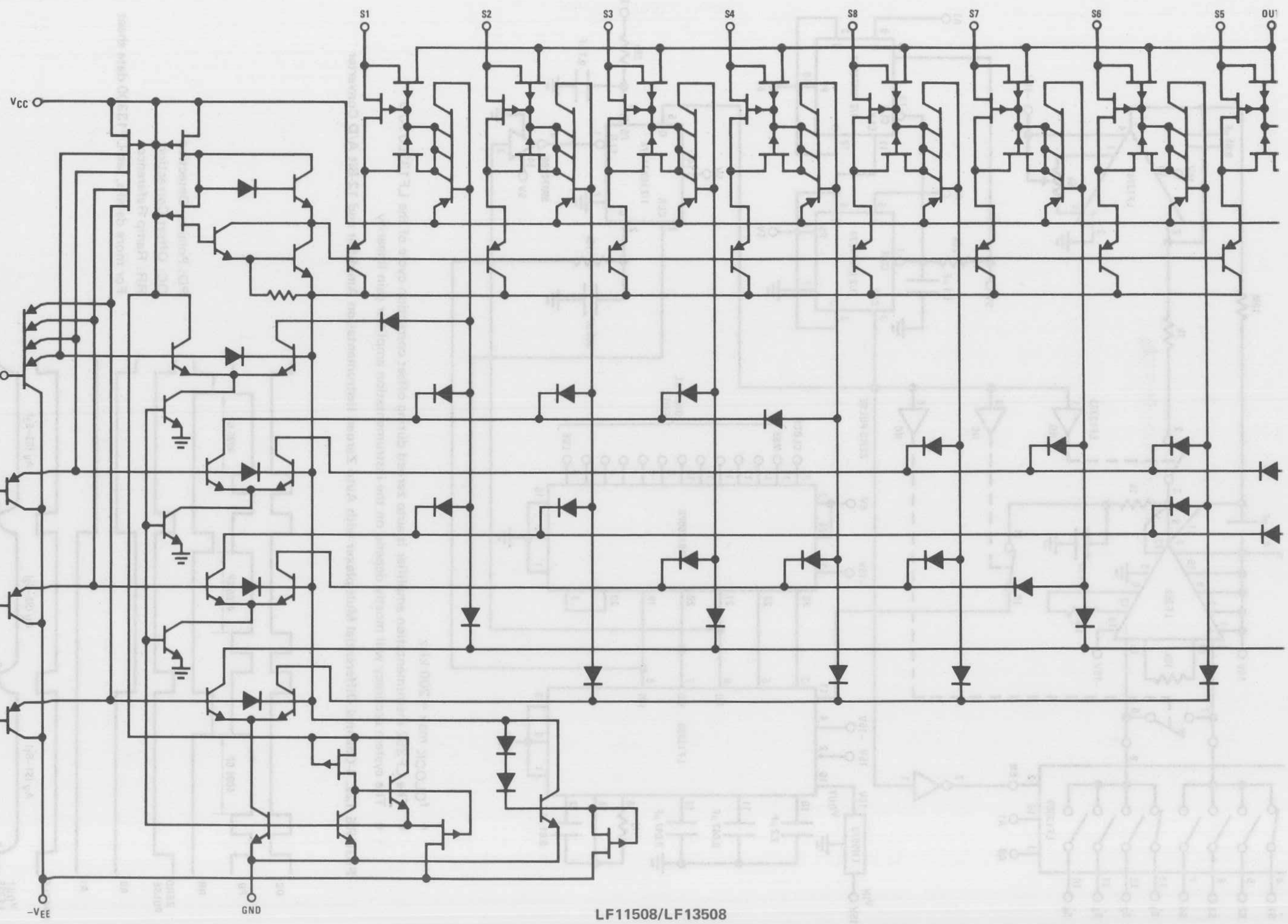
- f_{CLOCK} max = 200 kHz
- The LF352 instrumentation amplifier is auto zeroed during offset correction cycle of the LF13300 A/D
- The system accuracy will mostly depend on the instrumentation amplifier gain linearity

FIGURE 12a. 4-Channel Differential Multiplexer with Auto Zeroed Instrumentation Amplifier and 12-Bit A/D Converter



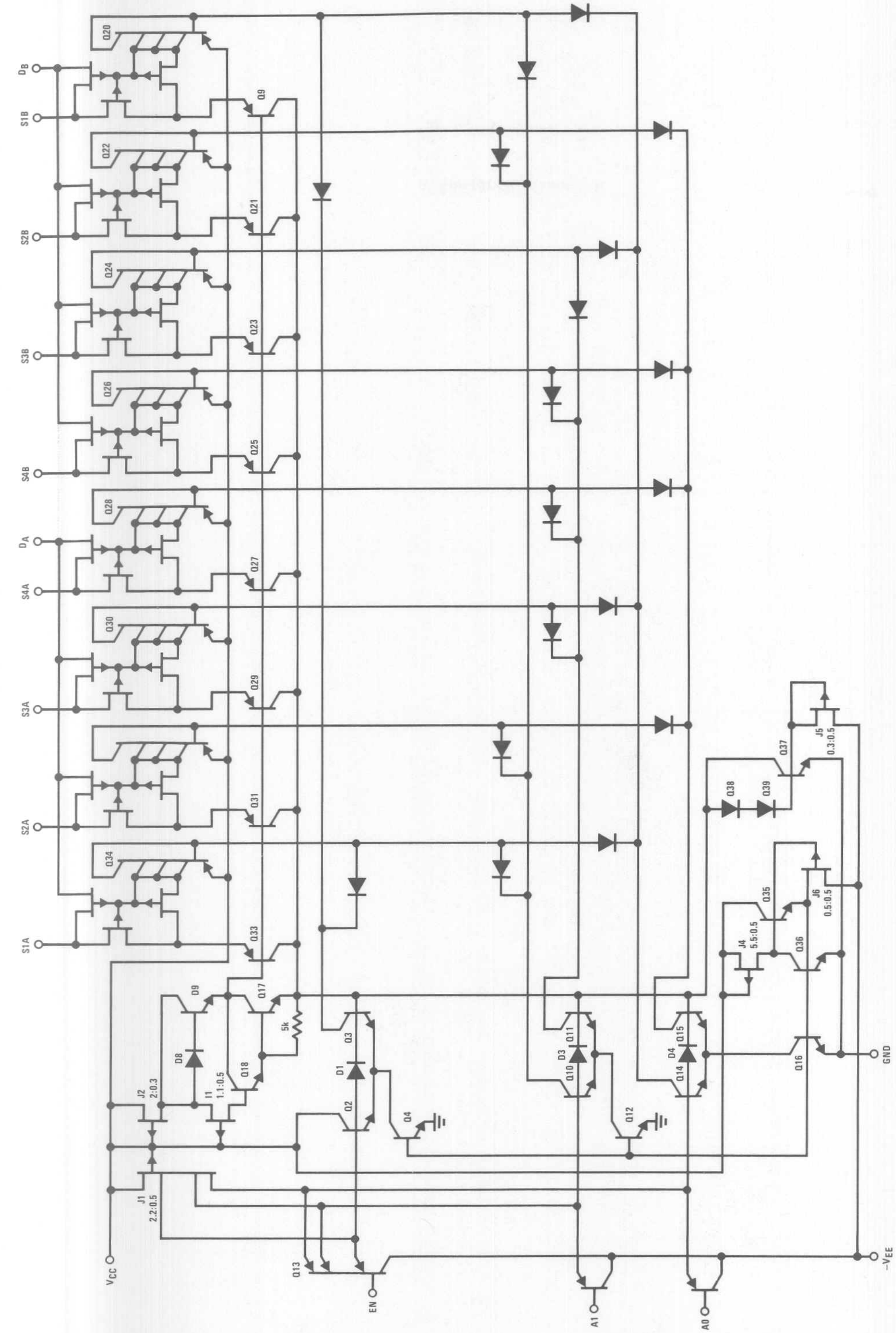
PD: Polarity Detection
OC: Offset Correction
RR: Ramp Reference
For more details, see LF13300 data sheet

FIGURE 12b. System Timing Diagram for Differential MUX



LF11508/LF13508

Schematic Diagrams (Continued)



LF11509/LF13509

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Section 7

Sample and Hold

Section Contents

Note. For additional information on sample and hold, see National Semiconductor's Hybrid Products Databook.

	LF198A	LF398A	LF198	LF398	LH0023	LH0023C	LH0043	LH0043C
Accuracy (% Max) Gain/Offset Error	0.01	0.01	0.02	0.02	0.01	0.02	0.1	0.3
Offset Voltage (mV Max)	2	3	5	10	20	20	40	40
Droop Rate (mV/sec, 25°C)								
$C_S = 1000$ pF	30	30	30	30	100	100	10	10
$C_S = 10000$ pF	3	3	3	3	10	10	1	1
Acquisition Time (μs, 25°C)								
$C_S = 1000$ pF	4	4	4	4	10	10	10	10
$C_S = 10000$ pF	20	20	20	20	50	50	50	50
Aperture Time (ns, 25°C)	25	25	25	25	150	150	20	20
Temperature Range (°C)	−55 to +125	0 to +70	−55 to +125	0 to +70	−55 to +125	−25 to +85	−55 to +125	−25 to +85
Comment	Low Drift	Low Drift	General Purpose	General Purpose	Low Drift	Low Drift	Medium Speed	Medium Speed

National Semiconductor

Sample and Hold

Definition of Terms

Acquisition Time: The time required to acquire a new analog input voltage with an output step of 10V. Note that acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.

Aperture Time: The delay required between "Hold" command and an input analog transition, so that the transition does not affect the held output.

Dynamic Sampling Error: The error introduced into the held output due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

Gain Error: The ratio of output voltage swing to input voltage swing in the sample mode expressed as a percent difference.

Hold Settling Time: The time required for the output to settle within 1 mV of final value after the "hold" logic command.

Hold Step: The voltage step at the output of the sample and hold when switching from sample mode to hold mode with a steady (dc) analog input voltage. Logic swing is 5V.

LF198/LF298/LF398, LF198A/LF398A Monolithic Sample and Hold Circuits

General Description

The LF198/LF298/LF398 are monolithic sample and hold circuits which utilize BI-FET technology to obtain ultra-high dc accuracy with fast acquisition of signal and low droop rate. Operating as a unity gain follower, dc gain accuracy is 0.002% typical and acquisition time is as low as 6μs to 0.01%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin and does not degrade input offset drift. The wide bandwidth allows the LF198 to be included inside the feedback loop of 1 MHz op amps without having stability problems. Input impedance of $10^{10}\Omega$ allows high source impedances to be used without degrading accuracy.

P-channel junction FET's are combined with bipolar devices in the output amplifier to give droop rates as low as 5 mV/min with a 1μF hold capacitor. The JFET's have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities. The overall design guarantees no feed-through from input to output in the hold mode even for input signals equal to the supply voltages.

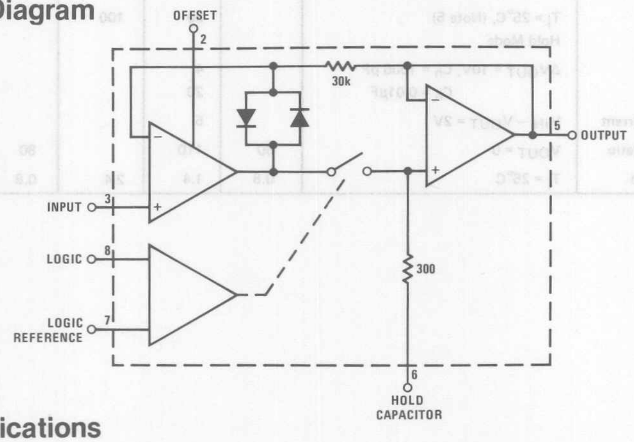
Features

- Operates from ±5V to ±18V supplies
- Less than 10μs acquisition time
- TTL, PMOS, CMOS compatible logic input
- 0.5 mV typical hold step at $C_h = 0.01\mu F$
- Low input offset
- 0.002% gain accuracy
- Low output noise in hold mode
- Input characteristics do not change during hold mode
- High supply rejection ratio in sample or hold
- Wide bandwidth

Logic inputs on the LF198 are fully differential with low input current, allowing direct connection to TTL, PMOS, and CMOS. Differential threshold is 1.4V. The LF198 will operate from ±5V to ±18V supplies. It is available in an 8-lead TO-5 package.

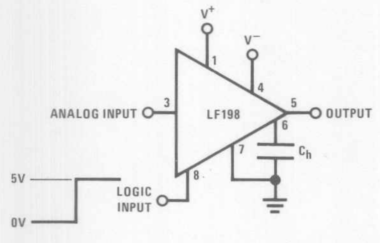
An "A" version is available with tightened electrical specifications.

Functional Diagram

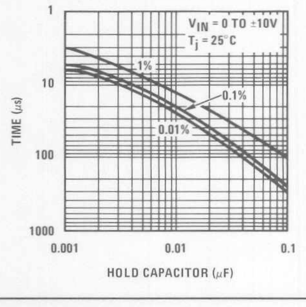


Typical Applications

Typical Connection



Acquisition Time



Operating Ambient Temperature Range	
LF198/LF198A	−55°C to +125°C
LF298	−25°C to +85°C
LF398/LF398A	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
(Note 2)	
Output Short Circuit Duration	Indefinite
Hold Capacitor Short Circuit Duration	10 sec
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 3)

PARAMETER	CONDITIONS	LF198/LF298			LF398			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage, (Note 6)	$T_j = 25°C$		1	3		2	7	mV
	Full Temperature Range			5			10	mV
Input Bias Current, (Note 6)	$T_j = 25°C$		5	25		10	50	nA
	Full Temperature Range			75			100	nA
Input Impedance	$T_j = 25°C$		10^{10}			10^{10}		Ω
Gain Error	$T_j = 25°C$, $R_L = 10k$		0.002	0.005		0.004	0.01	%
	Full Temperature Range			0.02			0.02	%
Feedthrough Attenuation Ratio at 1 kHz	$T_j = 25°C$, $C_h = 0.01\mu F$	86	96		80	90		dB
Output Impedance	$T_j = 25°C$, "HOLD" mode		0.5	2		0.5	4	Ω
	Full Temperature Range			4			6	Ω
"HOLD" Step, (Note 4)	$T_j = 25°C$, $C_h = 0.01\mu F$, $V_{OUT} = 0$		0.5	2.0		1.0	2.5	mV
Supply Current, (Note 6)	$T_j \geq 25°C$		4.5	5.5		4.5	6.5	mA
Logic and Logic Reference Input Current	$T_j = 25°C$		2	10		2	10	μA
Leakage Current into Hold Capacitor (Note 6)	$T_j = 25°C$, (Note 5) Hold Mode		30	100		30	200	pA
Acquisition Time to 0.1%	$\Delta V_{OUT} = 10V$, $C_h = 1000$ pF		4			4		μs
	$C_h = 0.01\mu F$		20			20		μs
Hold Capacitor Charging Current	$V_{IN} - V_{OUT} = 2V$		5			5		mA
Supply Voltage Rejection Ratio	$V_{OUT} = 0$	80	110		80	110		dB
Differential Logic Threshold	$T_j = 25°C$	0.8	1.4	2.4	0.8	1.4	2.4	V

Electrical Characteristics (Continued) (Note 3)

PARAMETER	CONDITIONS	LF198A MIN	LF198A TYP	LF198A MAX	LF398A MIN	LF398A TYP	LF398A MAX	UNITS
Input Offset Voltage, (Note 6)	$T_j = 25°C$		1	1		2	2	mV
	Full Temperature Range			2			3	mV
Input Bias Current, (Note 6)	$T_j = 25°C$		5	25		10	25	nA
	Full Temperature Range			75			50	nA
Input Impedance	$T_j = 25°C$		10^{10}			10^{10}		Ω
Gain Error	$T_j = 25°C$, $R_L = 10k$		0.002	0.005		0.004	0.005	%
	Full Temperature Range			0.01			0.01	%
Feedthrough Attenuation Ratio at 1 kHz	$T_j = 25°C$, $C_h = 0.01\mu F$	86	96		86	90		dB
Output Impedance	$T_j = 25°C$, "HOLD" mode		0.5	1		0.5	1	Ω
	Full Temperature Range			4			6	Ω
"HOLD" Step, (Note 4)	$T_j = 25°C$, $C_h = 0.01\mu F$, $V_{OUT} = 0$		0.5	1		1.0	1	mV
Supply Current, (Note 6)	$T_j \geq 25°C$		4.5	5.5		4.5	6.5	mA
Logic and Logic Reference Input Current	$T_j = 25°C$		2	10		2	10	μA
Leakage Current into Hold Capacitor (Note 6)	$T_j = 25°C$, (Note 5) Hold Mode		30	100		30	100	pA
Acquisition Time to 0.1%	$\Delta V_{OUT} = 10V$, $C_h = 1000$ pF		4	6		4	6	μs
	$C_h = 0.01\mu F$		20	25		20	25	μs
Hold Capacitor Charging Current	$V_{IN} - V_{OUT} = 2V$		5			5		mA
Supply Voltage Rejection Ratio	$V_{OUT} = 0$	90	110		90	110		dB
Differential Logic Threshold	$T_j = 25°C$	0.8	1.4	2.4	0.8	1.4	2.4	V

Note 1: The maximum junction temperature of the LF198/LF198A is 150°C, for the LF298, 115°C, and for the LF398/LF398A, 100°C. When operating at elevated ambient temperature, the power dissipation must be derated based on a thermal resistance (Θ_{jA}) of 150°C/W.

Note 2: Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.

Note 3: Unless otherwise specified, the following conditions apply. Unit is in "sample" mode, $V_S = \pm 15V$, $T_j = 25°C$, $-11.5V \leq V_{IN} \leq +11.5V$, $C_h = 0.01\mu F$, and $R_L = 10\ k\Omega$. Logic reference voltage = 0V and logic voltage = 2.5V.

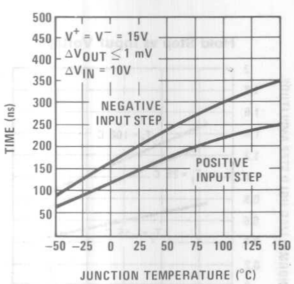
Note 4: Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1 pF, for instance, will create an additional 0.5 mV step with a 5V logic swing and a 0.01μF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.

Note 5: Leakage current is measured at a *junction* temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.

Note 6: These parameters guaranteed over a supply voltage range of ±5 to ±18V.

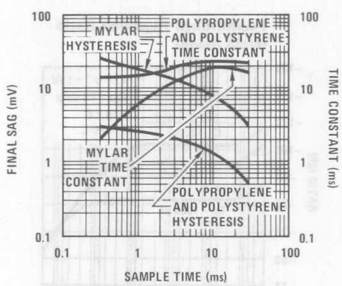
Typical Performance Characteristics

Aperture Time*

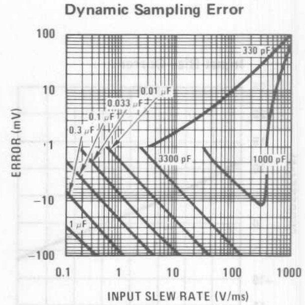


*See Definition of Terms

Capacitor Hysteresis

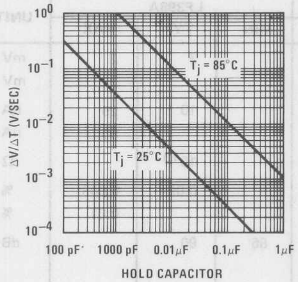


Dynamic Sampling Error

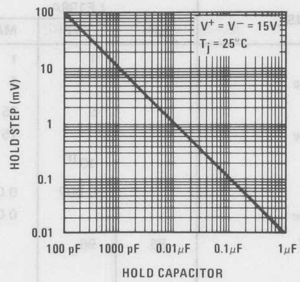


Typical Performance Characteristics (Continued)

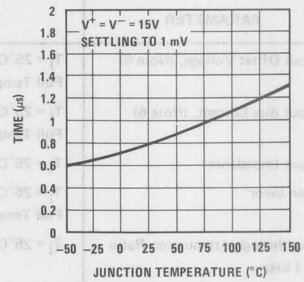
Output Droop Rate



Hold Step

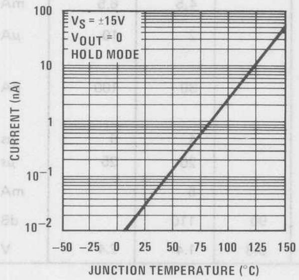


"Hold" Settling Time*

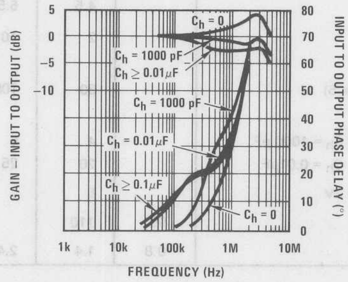


*See definition

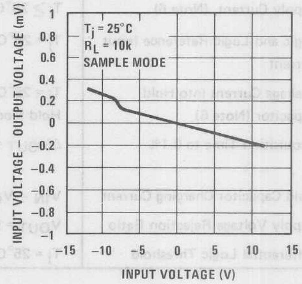
Leakage Current into Hold Capacitor



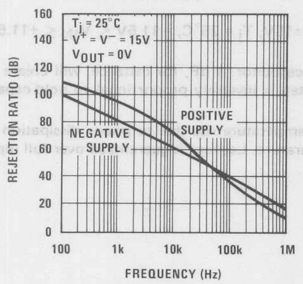
Phase and Gain (Input to Output, Small Signal)



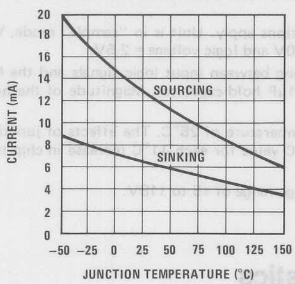
Gain Error



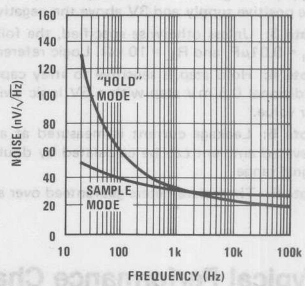
Power Supply Rejection



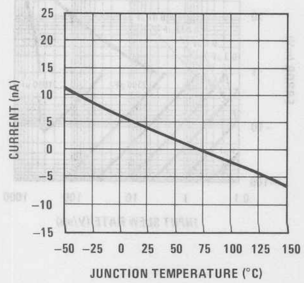
Output Short Circuit Current



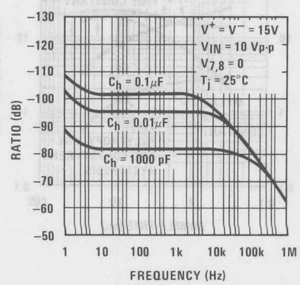
Output Noise



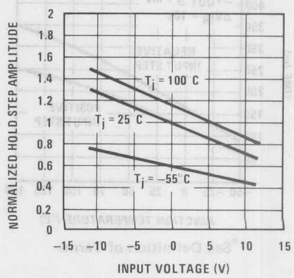
Input Bias Current



Feedthrough Rejection Ratio (Hold Mode)



Hold Step vs Input Voltage



Application Hints

Hold Capacitor

Hold step, acquisition time, and droop rate are the major trade-offs in the selection of a hold capacitor value. Size and cost may also become important for larger values. Use of the curves included with this data sheet should be helpful in selecting a reasonable value of capacitance. Keep in mind that for fast repetition rates or tracking fast signals, the capacitor drive currents may cause a significant temperature rise in the LF198.

A significant source of error in an accurate sample and hold circuit is dielectric absorption in the hold capacitor. A mylar cap, for instance, may "sag back" up to 0.2% after a quick change in voltage. A long "soak" time is required before the circuit can be put back into the hold mode with this type of capacitor. Dielectrics with very low hysteresis are polystyrene, polypropylene, and Teflon. Other types such as mica and polycarbonate are not nearly as good. Ceramic is unusable with > 1% hysteresis. The advantage of polypropylene over polystyrene is that it extends the maximum ambient temperature from 85°C to 100°C. "NPO" or "COG" capacitors are now available for 125°C operation and also have low dielectric absorption. For more exact data, see the curve labeled dielectric absorption error vs sample time. The hysteresis numbers on the curve are final values, taken after full relaxation. The hysteresis error can be significantly reduced if the output of the LF198 is digitized quickly after the hold mode is initiated. The hysteresis relaxation time constant in polypropylene, for instance, is 10–50 ms. If A-to-D conversion can be made within 1 ms, hysteresis error will be reduced by a factor of ten.

DC and AC Zeroing

DC zeroing is accomplished by connecting the offset adjust pin to the wiper of a 1 kΩ potentiometer which has one end tied to V^+ and the other end tied through a resistor to ground. The resistor should be selected to give ≈0.6 mA through the 1k potentiometer.

AC zeroing (hold step zeroing) can be obtained by adding an inverter with the adjustment pot tied input to output. A 10 pF capacitor from the wiper to the hold capacitor will give ±4 mV hold step adjustment with a 0.01μF hold capacitor and 5V logic supply. For larger logic swings, a smaller capacitor (< 10 pF) may be used.

Logic Rise Time

For proper operation, logic signals into the LF198 must have a minimum dV/dt of 1.0 V/μs. Slower signals will cause excessive hold step. If a R/C network is used in front of the logic input for signal delay, calculate the slope of the waveform at the threshold point to ensure that it is at least 1.0 V/μs.

Sampling Dynamic Signals

Sample error due to moving input signals probably causes more confusion among sample-and-hold users than any other parameter. The primary reason for this is that many users make the assumption that the sample and hold amplifier is truly locked on to the input signal while in the sample mode. In actuality, there are finite phase delays through the circuit creating an input-output differential for fast moving signals. In addition, although the output may have settled, the hold capacitor has an additional lag due to the 300Ω series resistor on the chip. This means that at the moment the "hold" command arrives, the hold capacitor voltage may be somewhat different than the actual analog input. The effect of these delays is opposite to the effect created by delays in the logic which switches the circuit from sample to hold. For example, consider an analog input of 20 Vp-p at 10 kHz. Maximum dV/dt is 0.6 V/μs. With no analog phase delay and 100 ns logic delay, one could expect up to (0.1μs)(0.6V/μs) = 60 mV error if the "hold" signal arrived near maximum dV/dt of the input. A positive-going input would give a +60 mV error. Now assume a 1 MHz (3 dB) bandwidth for the overall analog loop. This generates a phase delay of 160 ns. If the hold capacitor sees this exact delay, then error due to analog delay will be (0.16μs)(0.6 V/μs) = −96 mV. Total output error is +60 mV (digital) −96 mV (analog) for a total of −36 mV. To add to the confusion, analog delay is proportional to hold capacitor value while digital delay remains constant. A family of curves (dynamic sampling error) is included to help estimate errors.

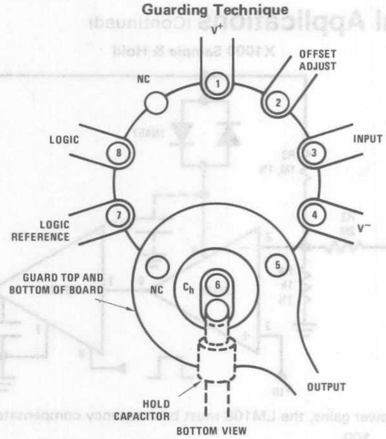
A curve labeled Aperture Time has been included for sampling conditions where the input is steady during the sampling period, but may experience a sudden change nearly coincident with the "hold" command. This curve is based on a 1 mV error fed into the output.

A second curve, Hold Settling Time indicates the time required for the output to settle to 1 mV after the "hold" command.

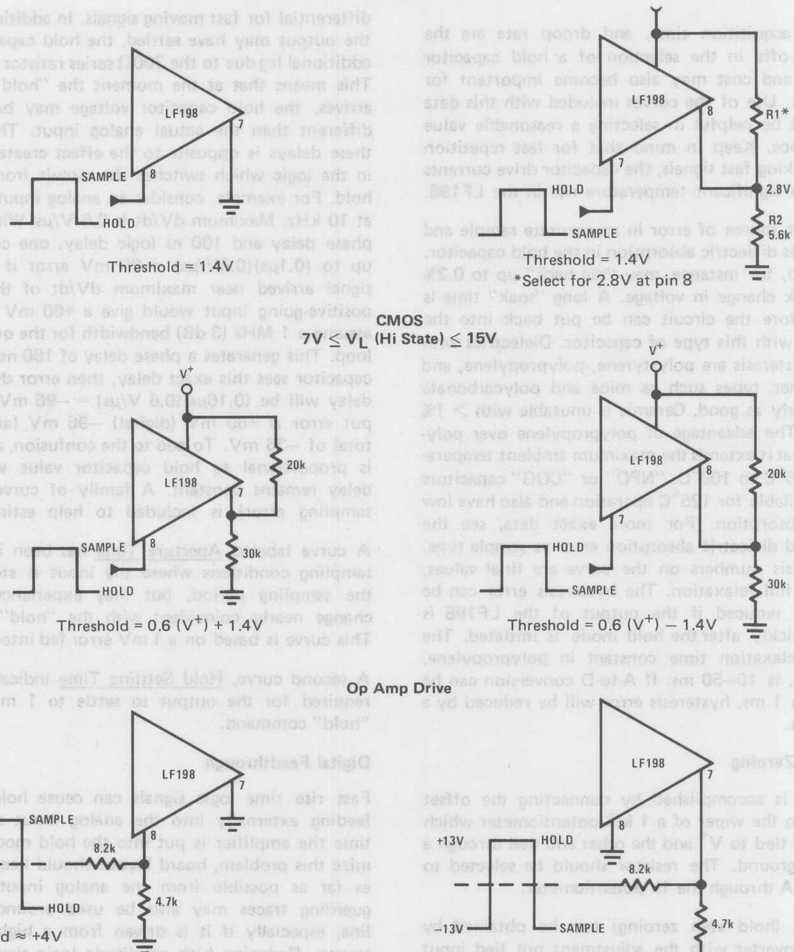
Digital Feedthrough

Fast rise time logic signals can cause hold errors by feeding externally into the analog input at the same time the amplifier is put into the hold mode. To minimize this problem, board layout should keep logic lines as far as possible from the analog input. Grounded guarding traces may also be used around the input line, especially if it is driven from a high impedance source. Reducing high amplitude logic signals to 2.5V will also help.

Guarding Technique

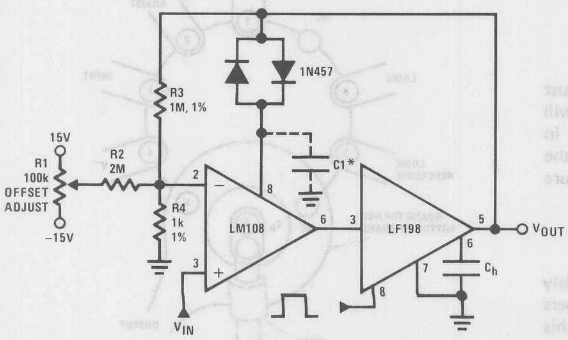


Use 10-pin layout. Guard around C_h is tied to output.



Typical Applications (Continued)

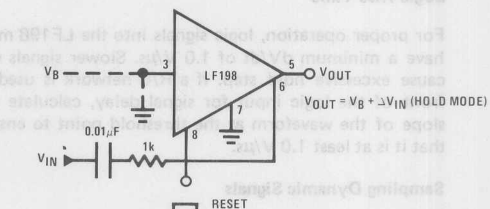
X1000 Sample & Hold



*For lower gains, the LM108 must be frequency compensated

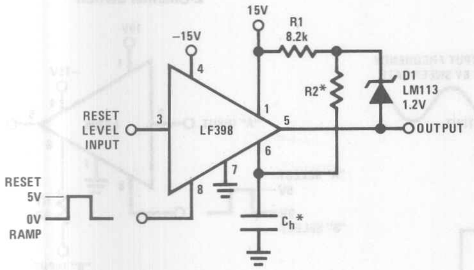
Use $\approx \frac{100}{A_V}$ pF from comp 2 to ground

Sample and Difference Circuit (Output Follows Input in Hold Mode)



Typical Applications (Continued)

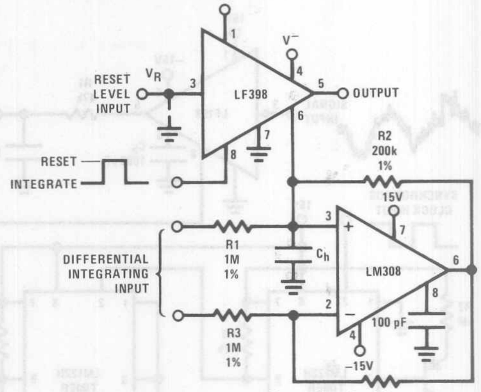
Ramp Generator with Variable Reset Level



*Select for ramp rate R ≥ 10k

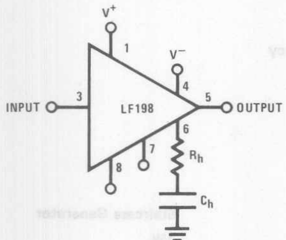
$$\frac{\Delta V}{\Delta T} = \frac{1.2V}{(R2)(C_h)}$$

Integrator with Programmable Reset Level



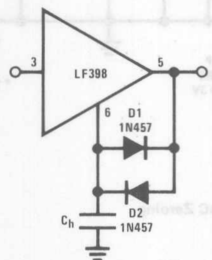
$$V_{OUT}\ (\text{Hold Mode}) = \left[\frac{1}{(R1)(C_h)}\int_0^t V_{IN}\,dt\right] + \left[V_R\right]$$

Output Holds at Average of Sampled Input

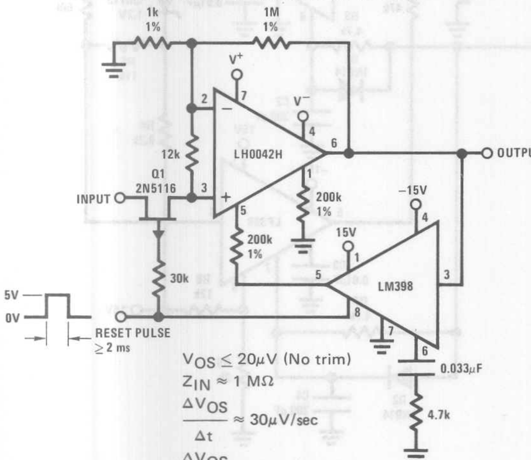


$$\text{Select } (R_h)(C_h) >> \frac{1}{2\pi f_{IN}\ (\text{Min})}$$

Increased Slew Current



Reset Stabilized Amplifier (Gain of 1000)



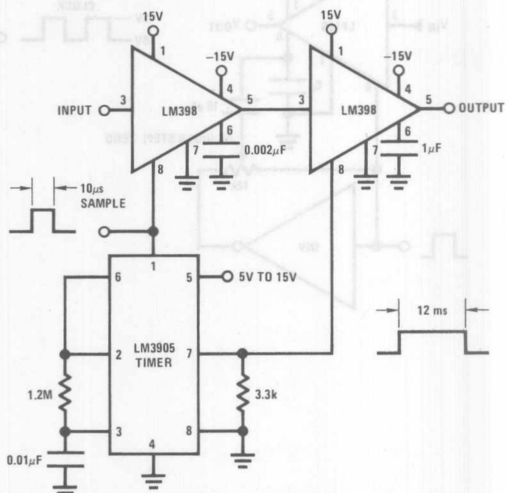
$V_{OS} \leq 20\mu V$ (No trim)

$Z_{IN} \approx 1\ M\Omega$

$\frac{\Delta V_{OS}}{\Delta t} \approx 30\mu V/sec$

$\frac{\Delta V_{OS}}{\Delta T} \approx 0.1\mu V/°C$

Fast Acquisition, Low Droop Sample & Hold



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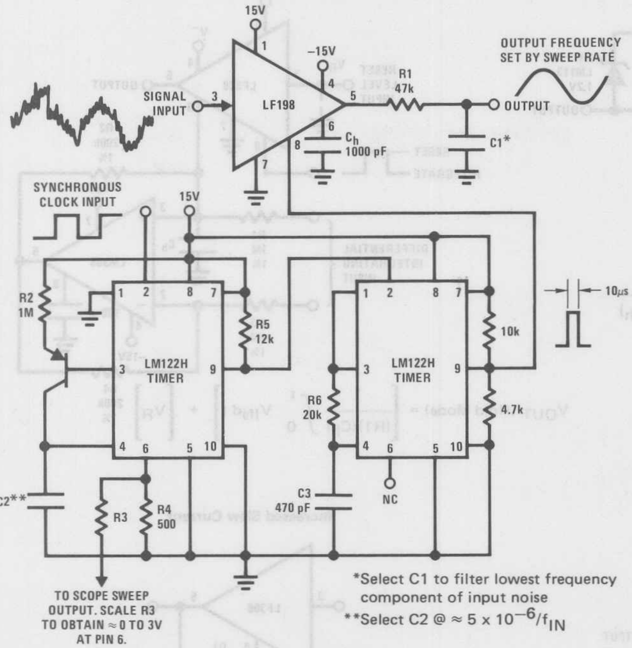
Typical Applications (Continued)

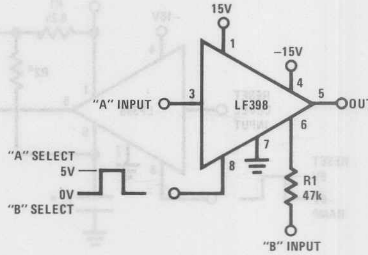
Synchronous Correlator for Recovering Signals Below Noise Level



*Select C1 to filter lowest frequency component of input noise

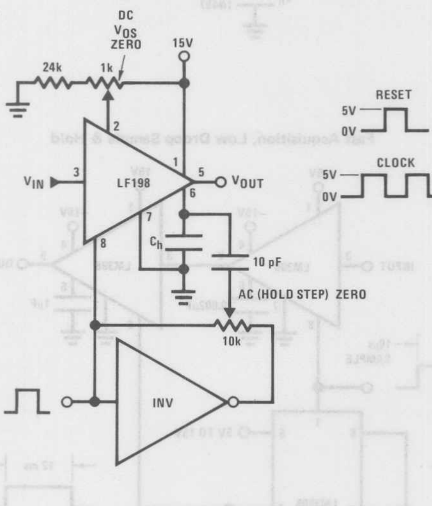
**Select C2 @ ≈ 5 x $10^{-6}/f_{IN}$

2-Channel Switch

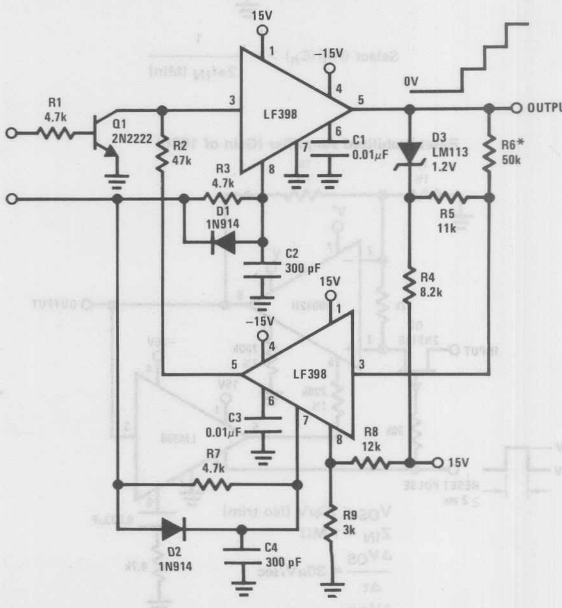


	A	B
Gain	1 ±0.02%	1 ±0.2%
Z_{IN}	$10^{10}\Omega$	47 kΩ
BW	≃1 MHz	≈400 kHz
Crosstalk @ 1 kHz	−90 dB	−90 dB
Offset	≤ 6 mV	≤ 75 mV

DC & AC Zeroing



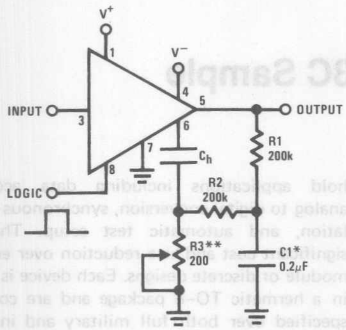
Staircase Generator



*Select for step height
50k → ≃ 1V Step

Typical Applications (Continued)

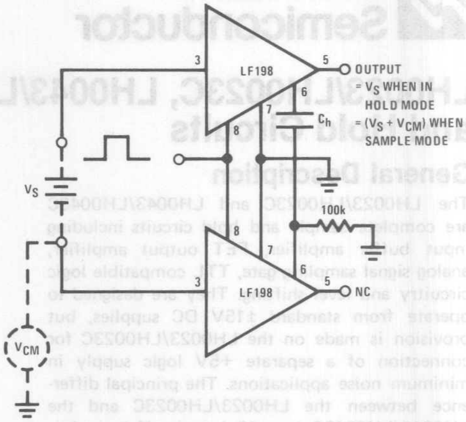
Capacitor Hysteresis Compensation



*Select for time constant C1 = $\frac{\tau}{100k}$

**Adjust for amplitude

Differential Hold



Definition of Terms

Hold Step: The voltage step at the output of the sample and hold when switching from sample mode to hold mode with a steady (dc) analog input voltage. Logic swing is 5V.

Acquisition Time: The time required to acquire a new analog input voltage with an output step of 10V. Note that acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.

Gain Error: The ratio of output voltage swing to input voltage swing in the sample mode expressed as a per cent difference.

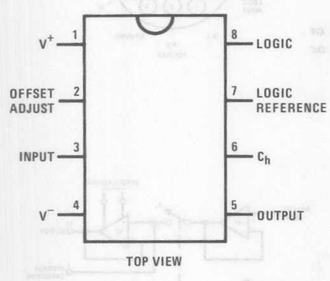
Hold Settling Time: The time required for the output to settle within 1 mV of final value after the "hold" logic command.

Dynamic Sampling Error: The error introduced into the held output due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

Aperture Time: The delay required between "Hold" command and an input analog transition, so that the transition does not affect the held output.

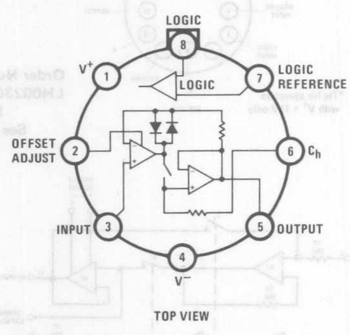
Connection Diagrams

Dual-In-Line Package



Order Number LF398N or LF398AN
See NS Package N08A

Metal Can Package



Order Number LF198H, LF298H, LF398H, LF198AH or LF398AH
See NS Package H08C

LH0023/LH0023C, LH0043/LH0043C Sample and Hold Circuits

General Description

The LH0023/LH0023C and LH0043/LH0043C are complete sample and hold circuits including input buffer amplifier, FET output amplifier, analog signal sampling gate, TTL compatible logic circuitry and level shifting. They are designed to operate from standard ±15V DC supplies, but provision is made on the LH0023/LH0023C for connection of a separate +5V logic supply in minimum noise applications. The principal difference between the LH0023/LH0023C and the LH0043/LH0043C is a 10:1 trade-off in performance on sample accuracy vs sample acquisition time. Devices are pin compatible except that TTL logic is inverted between the two types.

The LH0023/LH0023C and LH0043/LH0043C are ideally suited for a wide variety of sample and hold applications including data acquisition, analog to digital conversion, synchronous demodulation, and automatic test setup. They offer significant cost and size reduction over equivalent module or discrete designs. Each device is available in a hermetic TO-8 package and are completely specified over both full military and instrument temperature ranges.

The LH0023 and LH0043 are specified for operation over the −55°C to +125°C military temperature range. The LH0023C and LH0043C are specified for operation over the −25°C to +85°C temperature range.

Features

LH0023/LH0023C

- Sample accuracy−0.01% max
- Hold drift rate−0.5 mV/sec typ
- Sample acquisition time−100 μs max for 20V
- Aperture time−150 ns typ
- Wide analog range−±10V min
- Logic input−TTL/DTL
- Offset adjustable to zero with single 10k pot
- Output short circuit proof

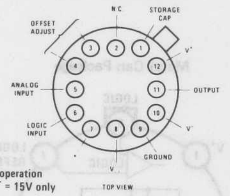
Features

LH0043/LH0043C

- Sample acquisition time−15 μs max for 20V
  4 μs typ for 5V
- Aperture time−20 nS typ
- Hold drift rate−1 mV/sec typ
- Sample accuracy−0.1% max
- Wide analog range−±10V min
- Logic input−TTL/DTL
- Offset adjustable to zero with single 10k pot
- Output short circuit proof

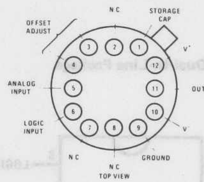
Block and Connection Diagrams

LH0023/LH0023C

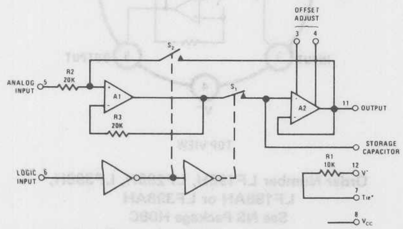


*Tie for operation with V+ = 15V only

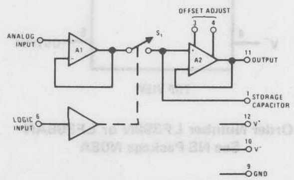
LH0043/LH0043C



Order Number LH0023G or LH0023CG or LH0043G or LH0043CG
See Package H12B



*Tie to pin 8 for operation without V_{CC} supply.



Absolute Maximum Ratings

Supply Voltage (V^+ and V^-)		±20V
Logic Supply Voltage (V_{CC}) LH0023, LH0023C		+7.0V
Logic Input Voltage (V_6)		+5.5V
Analog Input Voltage (V_5)		±15V
Power Dissipation		See graph
Output Short Circuit Duration		Continuous
Operating Temperature Range	LH0023, LH0043	−55°C to +125°C
	LH0023C, LH0043C	−25°C to +85°C
Storage Temperature Range		−65°C to +150°C
Lead Soldering (10 sec)		300°C

Electrical Characteristics LH0023/LH0023C (Note 1)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0023			LH0023C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Sample (Logic "1") Input Voltage	V_{CC} = 4.5V	2.0			2.0			V
Sample (Logic "1") Input Current	V_6 = 2.4V, V_{CC} = 5.5V			5.0			5.0	μA
Hold (Logic "0") Input Voltage	V_{CC} = 4.5V			0.8			0.8	V
Hold (Logic "0") Input Current	V_6 = 0.4V, V_{CC} = 5.5V			0.5			0.5	mA
Analog Input Voltage Range		±10	±11		±10	±11		V
Supply Current – I_{10}	V_5 = 0V, V_6 = 2V, V_{11} = 0V		4.5	6		4.5	6	mA
Supply Current – I_{12}	V_5 = 0V, V_6 = 0.4V, V_{11} = 0V		4.5	6		4.5	6	mA
Supply Current – I_8	V_8 = 5.0V, V_5 = 0		1.0	1.6		1.0	1.6	mA
Sample Accuracy	V_{OUT} = ±10V (Full Scale)		0.002	0.01		0.002	0.02	%
DC Input Resistance	Sample Mode	500	1000		300	1000		kΩ
	Hold Mode	20	25		20	25		kΩ
Input Current – I_5	Sample Mode		0.2	1.0		0.3	1.5	μA
Input Capacitance			3.0			3.0		pF
Leakage Current – pin 1	V_5 = ±10V; V_{11} = ±10V, T_A = 25°C		10.0	200		20.0	500	pA
	V_5 = ±10V; V_{11} = ±10V			2.5			2	nA
Drift Rate	V_{OUT} = ±5V, C_S = 0.01 μF, T_A = 25°C		0.5			0.5		mV/s
Drift Rate	V_{OUT} = ±10V, C_S = 0.01 μF, T_A = 25°C		1.0	20		2.0	50	mV/s
Drift Rate	V_{OUT} = ±10V, C_S = 0.01 μF			0.50			0.2	mV/ms
Aperture Time			150			150		ns
Sample Acquisition Time	ΔV_{OUT} = 20V, C_S = 0.01 μF		50	100		50	100	μs
Output Amplifier Slew Rate		1.5	3.0		1.5	3.0		V/μs
Output Offset Voltage (without null)	$R_S \leq$ 10k, V_5 = 0V, V_6 = 2.0V			±20			±20	mV
Analog Voltage Output Range	$R_L \geq$ 1k, T_A = 25°C	±10	±11		±10	±11		V
	$R_L \geq$ 2k	±10	±12		±10	±12		V

Note 1: Unless otherwise noted, these specifications apply for V^+ = +15V, V_{CC} = +5V, V^- = −15V, pin 9 grounded, a 0.01μF capacitor connected between pin 1 and ground over the temperature range −55°C to +125°C for the LH0023, and −25°C to +85°C for the LH0023C. All typical values are for T_A = 25°C.

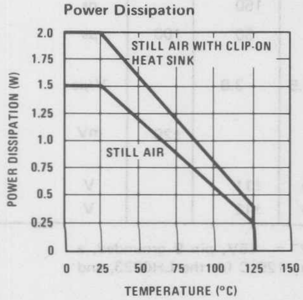
Electrical Characteristics LH0043/LH0043C: (Note 2)

PARAMETER	CONDITIONS	LIMITS LH0043 MIN	LH0043 TYP	LH0043 MAX	LH0043C MIN	LH0043C TYP	LH0043C MAX	UNITS
Hold (Logic "1") Input Voltage		2.0			2.0			V
Hold (Logic "1") Input Current	$V_6 = 2.4V$			5.0			5.0	μA
Sample (Logic "0") Input Voltage				0.8			0.8	V
Sample (Logic "0") Input Current	$V_6 = 0.4V$			1.5			1.5	mA
Analog Input Voltage Range		±10	±11		±10	±11		V
Supply Current	$V_5 = 0V$, $V_6 = 2V$, $V_{11} = 0V$		20	22		20	22	mA
	$V_5 = 0V$, $V_6 = 0.4V$, $V_{11} = 0V$		14	18		14	18	mA
Sample Accuracy	$V_{OUT} = \pm 10V$ (Full Scale)		0.02	0.1		0.02	0.3	%
DC Input Resistance	$T_C = 25°C$	10^{10}	10^{12}		10^{10}	10^{12}		Ω
Input Current − I_5			1.0	5.0		2.0	10.0	nA
Input Capacitance			1.5			1.5		pF
Leakage Current—pin 1	$V_5 = \pm 10V$; $V_{11} = \pm 10$, $T_C = 25°C$		10	25		20	50	pA
	$V_5 = \pm 10V$; $V_{11} = \pm 10V$		10	25		2	5	nA
Drift Rate	$V_{OUT} = \pm 10V$, $C_S = 0.001\ \mu F$, $T_C = 25°C$		10	25		20	50	mV/s
Drift Rate	$V_{OUT} = \pm 10V$, $C_S = 0.001\ \mu F$		10	25		2	5	mV/ms
Drift Rate	$V_{OUT} = \pm 10V$, $C_S = 0.01\ \mu F$, $T_C = 25°C$		1	2.5		2	5	mV/s
Drift Rate	$V_{OUT} = \pm 10V$, $C_S = 0.01\ \mu F$		1	2.5		0.2	0.5	mV/ms
Aperture Time			20	60		20	60	ns
Sample Acquisition Time	$\Delta V_{OUT} = 20V$, $C_S = 0.001\ \mu F$		10	15		10	15	μs
	$\Delta V_{OUT} = 20V$, $C_S = 0.01\ \mu F$		30	50		30	50	μs
	$\Delta V_{OUT} = 5V$, $C_S = 0.001\ \mu F$		4			4		μs
Output Amplifier Slew Rate	$V_{OUT} = 5V$, $C_S = 0.001\ \mu F$	1.5	3.0		1.5	3.0		$V/\mu s$
Output Offset Voltage (without null)	$R_S \leq 10k$, $V_5 = 0V$, $V_6 = 0V$			±40			±40	mV
Analog Voltage Output Range	$R_L \geq 1k$, $T_A = 25°C$	±10	±11		±10	±11		V
	$R_L \geq 2k$	±10	±12		±10	±12		V

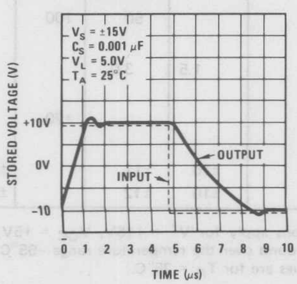
Note 2: Unless otherwise noted, these specifications apply for $V^+ = +15V$, $V^- = -15V$, pin 9 grounded, a 5000 pF capacitor connected between pin 1 and ground over the temperature range −55°C to +125°C for the LH0043, and −25°C to +85°C for the LH0043C. All typical values are for $T_C = 25°C$.

Typical Performance Characteristics

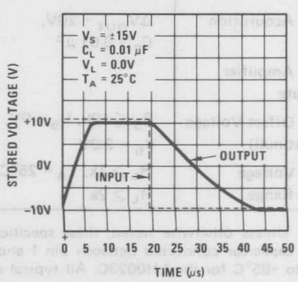
Power Dissipation



Sample Acquisition Time—LH0043

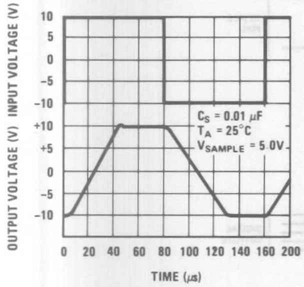


Sample Acquisition Time—LH0043

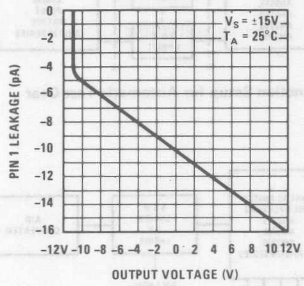


Typical Performance Characteristics (Continued)

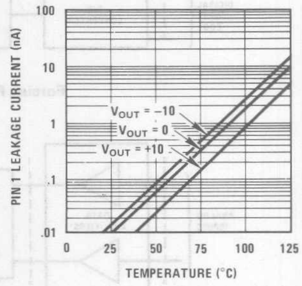
Sample Acquisition Time—LH0023



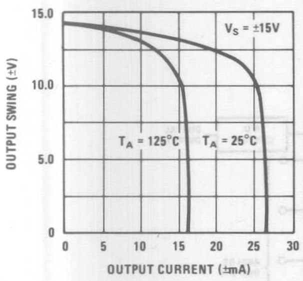
Pin 1 Leakage Current vs Output Voltage



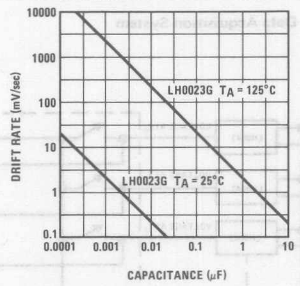
Pin 1 Leakage Current vs Temperature



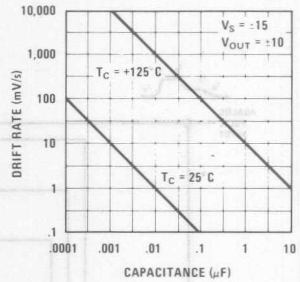
Output Current Limiting



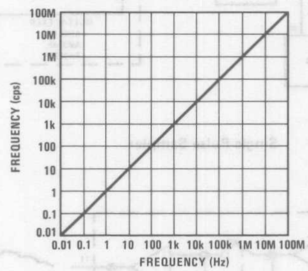
Drift vs Capacitance (LH0023)



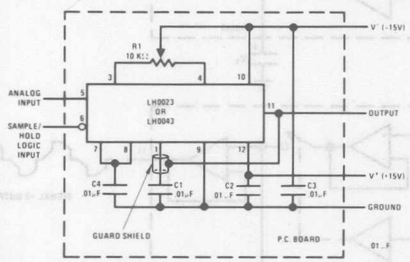
Drift vs Capacitance (LH0043)



(LH0023)

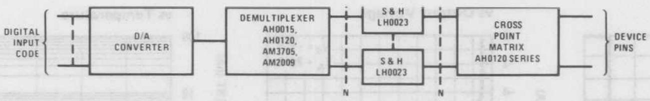


Typical Applications

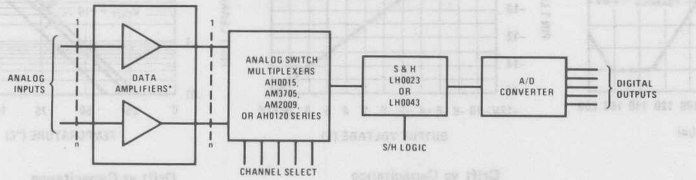


Note 1: C1 is polystyrene.
Note 2: C2, C3, C4 are cermic disc.
Note 3: Jumper 7–8 and C4 not required for LH0043.
Note 4: R1 optional if zero trim is required.

How to Build a Sample and Hold Module

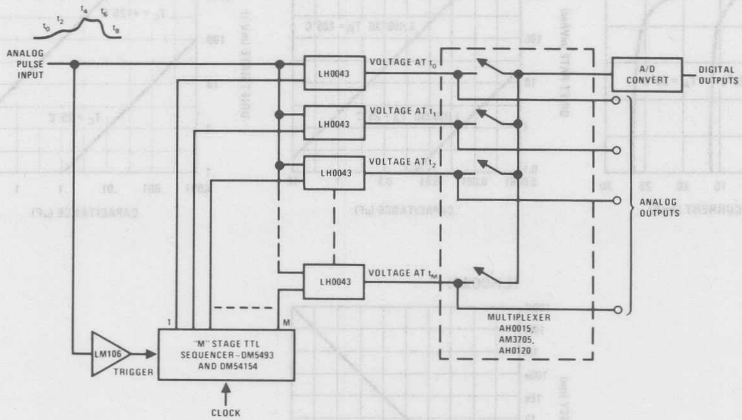


Forcing Function Setup for Automatic Test Gear

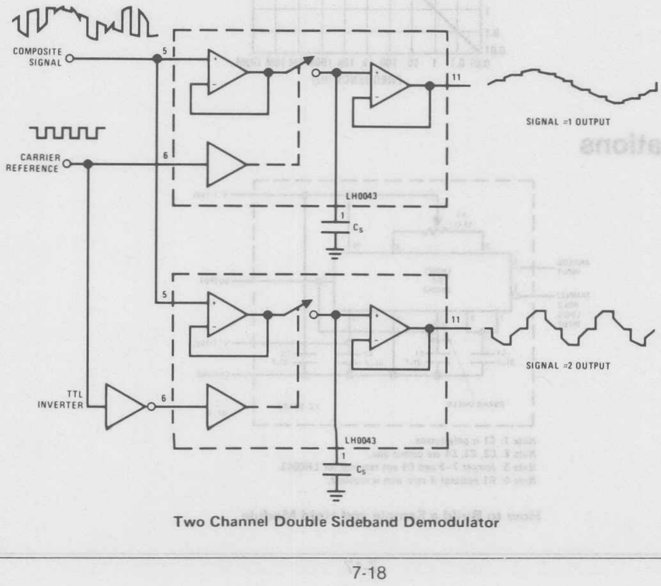


*See op amp selection guide for details. Most popular types include LH0052, LM108, LM112, LH0044, LH0036, and LH0038.

Data Acquisition System



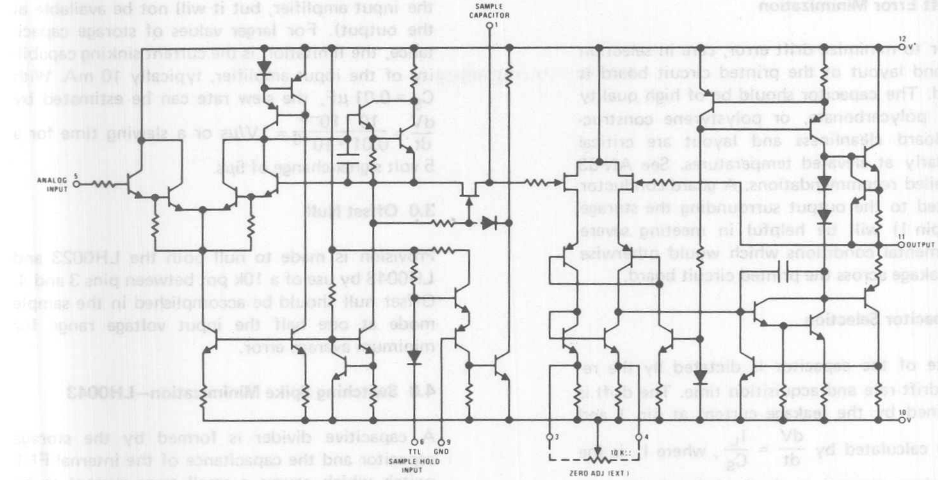
Single Pulse Sampler



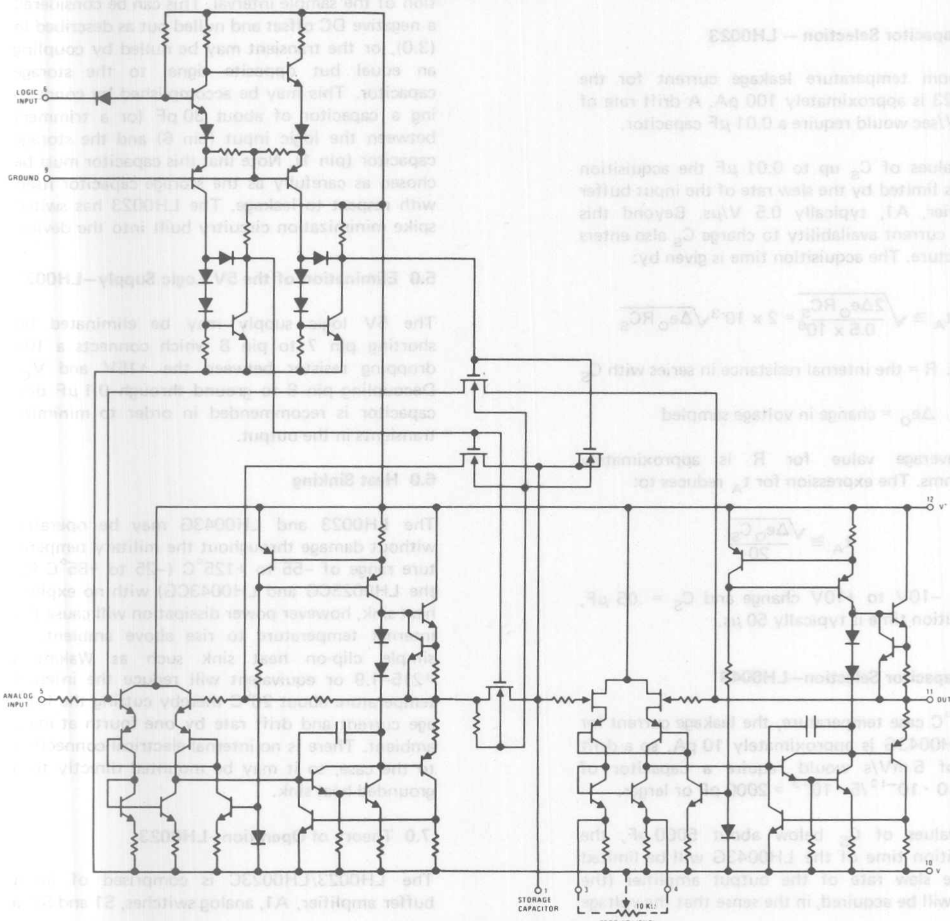
Two Channel Double Sideband Demodulator

Schematic Diagrams

LH0043/LH0043C



LH0023/LH0023C



Applications Information

1.0 Drift Error Minimization

In order to minimize drift error, care in selection of C_S and layout of the printed circuit board is required. The capacitor should be of high quality Teflon, polycarbonate, or polystyrene construction. Board cleanliness and layout are critical particularly at elevated temperatures. See AN-63 for detailed recommendations. A guard conductor connected to the output surrounding the storage node (pin 1) will be helpful in meeting severe environmental conditions which would otherwise cause leakage across the printed circuit board.

2.0 Capacitor Selection

The size of the capacitor is dictated by the required drift rate and acquisition time. The drift is determined by the leakage current at pin 1 and may be calculated by $\frac{dV}{dt} = \frac{I_L}{C_S}$, where I_L is the total leakage current at pin 1 of the device, and C_S is the value of the storage capacitor.

2.1 Capacitor Selection — LH0023

At room temperature leakage current for the LH0023 is approximately 100 pA. A drift rate of 10 mV/sec would require a 0.01 μF capacitor.

For values of C_S up to 0.01 μF the acquisition time is limited by the slew rate of the input buffer amplifier, A1, typically 0.5 V/μs. Beyond this point, current availability to charge C_S also enters the picture. The acquisition time is given by:

$$t_A \cong \sqrt{\frac{2\Delta e_O RC_S}{0.5 \times 10^6}} = 2 \times 10^{-3}\sqrt{\Delta e_O RC_S}$$

where: R = the internal resistance in series with C_S

Δe_O = change in voltage sampled

An average value for R is approximately 600 ohms. The expression for t_A reduces to:

$$t_A \cong \frac{\sqrt{\Delta e_O C_S}}{20}$$

For a −10V to +10V change and C_S = .05 μF, acquisition time is typically 50 μs.

2.2 Capacitor Selection—LH0043

At 25°C case temperature, the leakage current for the LH0043G is approximately 10 pA, so a drift rate of 5 mV/s would require a capacitor of $C_S = 10 \cdot 10^{-12}/5 \cdot 10^{-3}$ = 2000 pF or larger.

For values of C_S below about 5000 pF, the acquisition time of the LH0043G will be limited by the slew rate of the output amplifier (the signal will be acquired, in the sense that the voltage will be stored on the capacitor, in much less time as dictated by the slew rate and current capacity of the input amplifier, but it will not be available at the output). For larger values of storage capacitance, the limitation is the current sinking capability of the input amplifier, typically 10 mA. With C_S = 0.01 μF, the slew rate can be estimated by $\frac{dV}{dt} = \frac{10 \cdot 10^{-3}}{0.01 \cdot 10^{-6}}$ = 1V/μs or a slewing time for a 5 volt signal change of 5μs.

3.0 Offset Null

Provision is made to null both the LH0023 and LH0043 by use of a 10k pot between pins 3 and 4. Offset null should be accomplished in the sample mode at one half the input voltage range for minimum average error.

4.0 Switching Spike Minimization—LH0043

A capacitive divider is formed by the storage capacitor and the capacitance of the internal FET switch which causes a small error current to be injected into the storage capacitor at the termination of the sample interval. This can be considered a negative DC offset and nulled out as described in (3.0), or the transient may be nulled by coupling an equal but opposite signal to the storage capacitor. This may be accomplished by connecting a capacitor of about 30 pF (or a trimmer) between the logic input (pin 6) and the storage capacitor (pin 1). Note that this capacitor must be chosen as carefully as the storage capacitor itself with respect to leakage. The LH0023 has switch spike minimization circuitry built into the device.

5.0 Elimination of the 5V Logic Supply—LH0023

The 5V logic supply may be eliminated by shorting pin 7 to pin 8 which connects a 10k dropping resistor between the +15V and V_C. Decoupling pin 8 to ground through 0.1 μF disc capacitor is recommended in order to minimize transients in the output.

6.0 Heat Sinking

The LH0023 and LH0043G may be operated without damage throughout the military temperature range of −55 to +125°C (−25 to +85°C for the LH0023CG and LH0043CG) with no explicit heat sink, however power dissipation will cause the internal temperature to rise above ambient. A simple clip-on heat sink such as Wakefield #215–1.9 or equivalent will reduce the internal temperature about 20°C thereby cutting the leakage current and drift rate by one fourth at max. ambient. There is no internal electrical connection to the case, so it may be mounted directly to a grounded heat sink.

7.0 Theory of Operation—LH0023

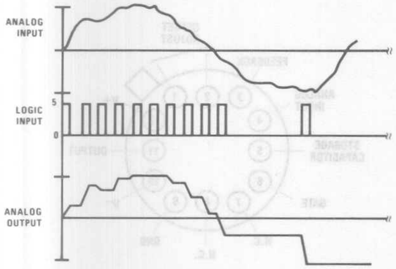
The LH0023/LH0023C is comprised of input buffer amplifier, A1, analog switches, S1 and S2, a

Applications Information (Continued)

TTL to MOS level translator, and output buffer amplifier, A2. In the "sample" mode, the logic input is raised to logic "1" ($V_6 \leq 2.0V$) which closes S1 and opens S2. Storage capacitor, C_S, is charged to the input voltage through S1 and the output slews to the input voltage. In the "hold" mode, the logic input is lowered to logic "0" ($V_6 \leq 0.8V$) opening S1 and closing S2. C_S retains the sample voltage which is applied to the output via A2. Since S1 is open, the input signal is overridden, and leakage across the MOS switch is therefore minimized. With S1 open, drift is primarily determined by input bias current of A2, typically 100 pA at 25°C.

7.1 Theory of Operation—LH0043

The LH0043/LH0043C is comprised of input buffer amplifier A1, FET switch S1 operated by a TTL compatible level translator, and output buffer amplifier A2. To enter the "sample" mode, the logic input is taken to the TTL logic "0" state ($V_6 = 0.8V$) which commands the switch S1



closed and allows A1 to make the storage capacitor voltage equal to the analog input voltage. In the "hold" mode ($V_6 = 2.0V$), S1 is opened isolating the storage capacitor from the input and leaving it charged to a voltage equal to the last analog input voltage before entering the hold mode. The storage capacitor voltage is brought to the output by low leakage amplifier A2.

8.0 Definitions

V_5: The voltage at pin 5, e.g., the analog input voltage.

V_6: The voltage at pin 6, e.g., the logic control input signal.

V_{11}: The voltage at pin 11, e.g., the output signal.

T_A: The temperature of the ambient air.

T_C: The temperature of the device case at the center of the bottom of the header.

Acquisition Time:
The time required for the output (pin 11) to settle within the rated accuracy after a specified input change is applied to the input (pin 5) with the logic input (pin 6) in the low state.

Aperture Time:
The time indeterminacy when switching from sample mode to hold including the delay from the time the mode control signal (pin 6) passes through its threshold (1.4 volts) to the time the circuit actually enters the hold mode.

Output Offset Voltage:
The voltage at the output terminal (pin 11) with the analog input (pin 5) at ground and logic input (pin 6) in the "sample" mode. This will always be adjustable to zero using a 10k pot between pins 3 and 4 with the wiper arm returned to V^-.

LH0053/LH0053C High Speed Sample and Hold Amplifier

General Description

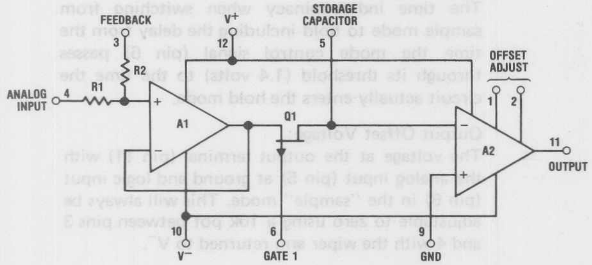
The LH0053/LH0053C is a high speed sample and hold circuit capable of acquiring a 20V step signal in under 5.0μs.

The device is ideally suited for a variety of high speed data acquisition applications including analog buffer memories for A to D conversion and synchronous demodulation.

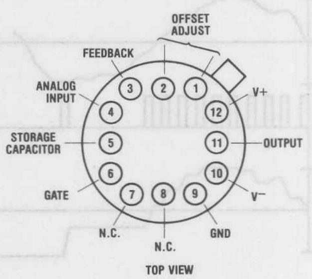
Features

- Sample acquisition time 10μs max. for 20V signal
- FET switch for preset or reset function
- Sample accuracy null
- Offset adjust to 0V
- DTL/TTL compatible FET gate
- Single storage capacitor

Schematic and Connection Diagrams

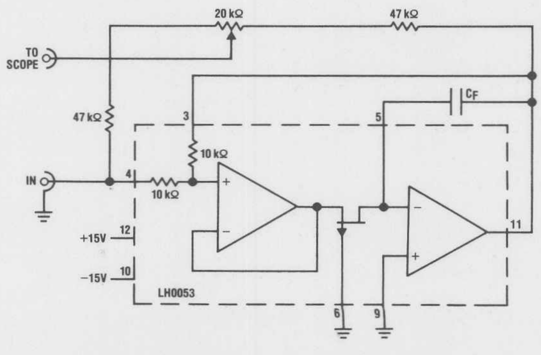


Metal Can Package



Order Number LH0053G or LH0053CG
See Package H12B

AC Test Circuit



Acquisition Time Test Circuit

Absolute Maximum Ratings

Supply Voltage (V^+ and V^-)	±18V
Gate Input Voltage (V_6)	±20V
Analog Input Voltage (V_4)	±15V
Input Current (I_8 and I_5)	±10 mA
Power Dissipation	1.5W
Output Short Circuit Duration	Continuous
Operating Temperature Range	
LH0053	−55°C to +125°C
LH0053C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 1)

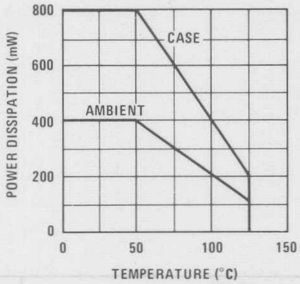
Parameter	Conditions	Limits						Units
		LH0053			LH0053C			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Sample (Gate "0") Input Voltage				0.5			0.5	V
Sample (Gate "0") Input Current	$V_6 = 0.5V$, $T_A = 25°C$			−5.0			−5.0	μA
	$V_6 = 0.5V$			−100			−100	μA
Hold (Gate "1") Input Voltage		4.5			4.5			V
Hold (Gate "1") Input Current	$V_6 = 4.5V$, $T_A = 25°C$			1.0				nA
	$V_6 = 4.5V$			1.0				μA
Analog Input Voltage Range		±10	±11		±10	±11		V
Supply Current	$V_4 = 0V$, $V_6 = 0.5V$		13	18		13	18	mA
Input Bias Current (I_4)	$V_4 = 0V$, $T_A = 25°C$		120	250		150	500	nA
Input Resistance		5.0	10	15	5.0	10	15	kΩ
Analog Output Voltage Range	$R_L = 2.0 k\Omega$	±10	±12		±10	±12		V
Output Offset Voltage	$V_4 = 0V$, $V_6 = 0.5V$, $T_A = 25°C$		5.0	7.0		5.0	10	mV
	$V_4 = 0V$, $V_6 = 0.5V$			10			15	mV
Sample Accuracy (Note 2)	$V_4 = \pm 10V$, $V_6 = 0.5V$, $T_A = 25°C$		0.1	0.2		0.1	0.3	%
Aperture Time	$\Delta V_6 = 4.5V$, $T_A = 25°C$		10	25		10	25	ns
Sample Acquisition Time	$V_4 = \pm 10V$, $T_A = 25°C$, $C_F = 1000 pF$, $V_6 = 0V$		5.0	10		8.0	15	μs
Sample Acquisition Time	$V_4 = \pm 10V$, $T_A = 25°C$, $C_F = 100 pF$, $V_6 = 0V$		4.0			4.0		μs
Output Slew Rate	$\Delta V_{IN} = \pm 10V$, $T_A = 25°C$, $C_F = 100 pF$, $V_6 = 0V$		20			20		V/μs
Large Signal Bandwidth	$V_4 = \pm 10V$, $T_A = 25°C$, $C_F = 1000 pF$		200			200		kHz
Leakage Current (Pin 5)	$V_4 = \pm 10V$, $T_A = 25°C$,		6.0	50		10	100	pA
	$V_4 = \pm 10V$			30			30	nA
Drift Rate	$V_4 = \pm 10V$, $T_A = 25°C$, $C_F = 1000 pF$		6.0	50		10	100	mV/s
Drift Rate	$V_4 = \pm 10V$, $C_F = 1000 pF$			30			30	V/s

Note 1: Unless otherwise noted, these specifications apply for $V_S = \pm 15V$, pin 9 grounded, a 1000 pF capacitor between pin 5 and pin 11, pin 3 shorted to pin 11, over the temperture range −55°C to +125°C for the LH0053 and −25°C to +85°C for the LH0053C. All typical values are for $T_A = 25°C$.

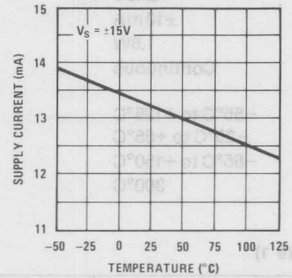
Note 2: Sample accuracy may be nulled by inserting a potentiometer in the feedback loop. This compensates for source impedance and feedback resistor tolerances.

Typical Performance Characteristics

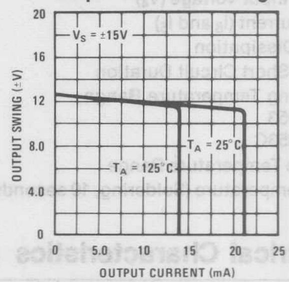
Power Dissipation



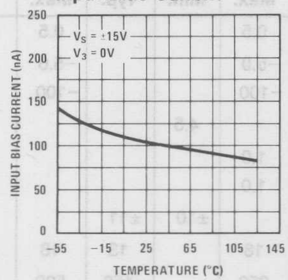
Supply Current vs. Temperature



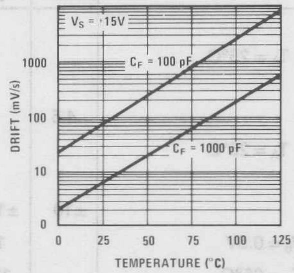
Output Current Limiting



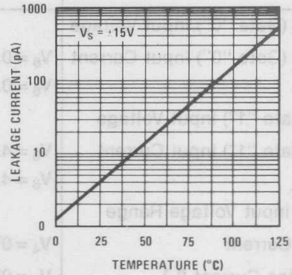
Input Bias Current



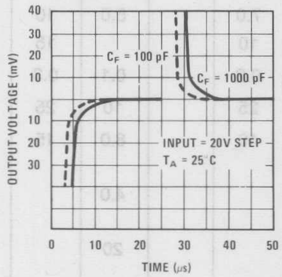
Drift



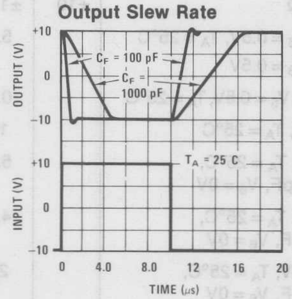
Leakage Current at Pin 5



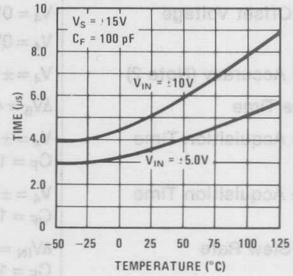
Sample Acquisition Time



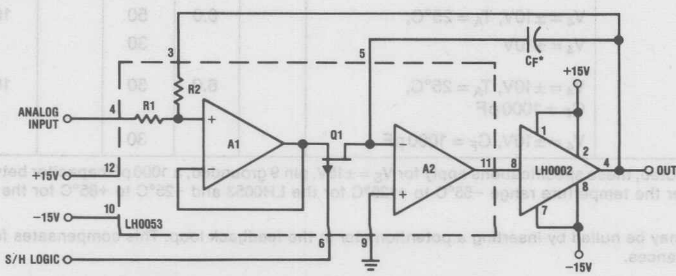
Output Slew Rate



Acquisition Time vs. Temperature



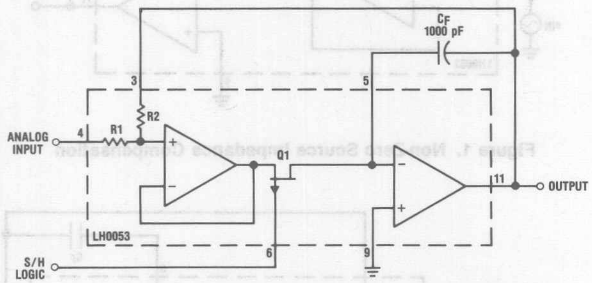
Typical Applications



*POLYSTYRENE CONSTRUCTION.

Increasing Output Drive Capability

Typical Applications (Continued)



Sample and Hold

Applications Information

Source Impedance Compensation

The gain accuracy (linearity) of the LH0053/LH0053C is set by two internal precision resistors. Circuit applications in which the source impedance is non-zero will result in a closed loop gain error, e.g. if $R_S = 10\Omega$, a gain error of 0.1% results. Figures 1 and 2 show methods for accomodating non-zero source impedance.

Drift Error Minimization

In order to minimize drift error, care in selecting C_F and layout of the printed circuit board are required. The capacitor should be of high quality teflon, polycarbonate, or polystyrene construction. Board layout and clean lines are critical particularly at elevated temperature.

A ground guard (shield) surrounding pin 5 will minimize leakage currents to and from the summing junction, arising from extraneous signals. See AN-63 for detailed recommendations.

Capacitor Selection

The size of the capacitor is determined by the required drift rate usually at the expense of acquisition time.

The drift is dictated by leakage current at pin 5 and is given by:

$$\frac{dv}{dt} = \frac{I_L}{C_F}$$

Where I_L is the leakage current at pin 5 and C_F is the value of the capacitance. The room temperature leakage of the LH0053 is typically 6.0 pA, and a 1000 pF capacitor will yield a drift rate of 6.0 mV per second.

For values of C_F below 1000 pF acquisition for the LH0053 is primarily governed by the slew rate of the input amplifier (20 V/μs) and the setting time of the output amplifier ($\cong$1.0 μs). For values above $C_F = 1000$ pF, acquisition time is given by:

$$t_a = \frac{C_F\,\Delta V}{I_{DSS}} + t_{S2}$$

Where:

C_F = The value of the capacitor

ΔV = The magnitude of the input step, e.g. 20V

I_{DSS} = The ON current of switch Q1 $\cong$ 5.0 mA

t_{S2} = The setting time of output amplifier $\cong$ 1.0 μs

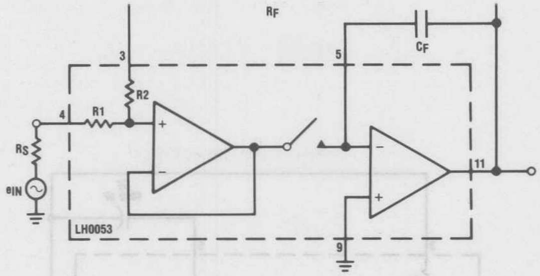


Figure 1. Non-Zero Source Impedance Compensation

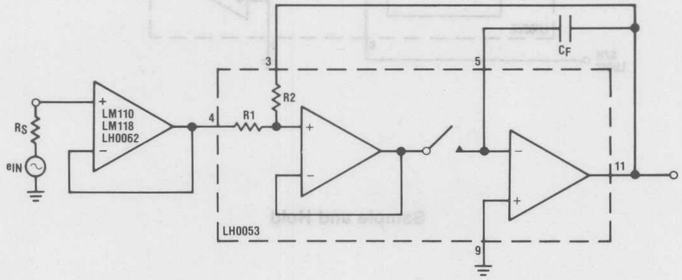


Figure 2. Non-Zero Source Impedance Buffering

Gate Input Considerations

5.0V TTL Applications

The LH0053 Gate input (pin 6) will interface directly with 5.0V TTL. However, TTL gates typically pull up to 2.5V in the logic "1" state. It is therefore advisable to use a 10kΩ pull-up resistor between the 5.0V, V_{CC}, and the output of the gate as shown in Figure 3.

To obtain the highest speed and fastest acquisition time, the gate drive shown in Figure 6 is recommended.

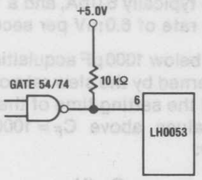


Figure 3. TTL Logic Compatibility

CMOS Applications

The LH0053 gate input may be interfaced directly with 74C, CMOS operating off of V_{CC}'s from 5.0V to 15V. However, transient currents of several milliamps can flow on the rising and falling edges of the input signal. It is, therefore, advisable to parallel the outputs of two 54C/74C gates as shown in Figure 4.

It should be noted that leakage at pin 5 in the hold mode will be increased by a factor of 2 to 3 when operating into 15V logic levels.

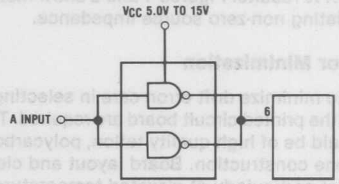


Figure 4. CMOS Logic Compatibility

Heat Sinking.

The LH0053 may be operated over the military temperature range, −55°C to +125°C, without incurring damage to the device. However, a clip on heat sink such as the Wakefield 215 Series or Thermalloy 2240 will reduce the internal temperature rise by about 20°C. The result is a two-fold improvement in drift rate at temperature.

Applications Information (Continued)

Since the case of the device is electrically isolated from the circuit, the LH0053 may be mounted directly to a grounded heat sink.

Power Supply Decoupling

Amplifiers A1 and A2 within the LH0053 are very wide band devices and are sensitive to power supply inductance. It is advisable to bypass V^+ (pin 12) and V^- (pin 10) to ground with $0.1\mu F$ disc capacitors in order to prevent oscillation. Should this procedure prove inadequate, the disc capacitors should be paralleled with $4.7\mu F$ solid tantalum electrolytic capacitors.

DC Offset Adjust

Output offset error may be adjusted to zero using the circuit shown in Figure 5. Offset null should be accomplished in the sample mode ($V_6 \leqslant 0.5V$) and analog input (pin 4) equal to zero volts.

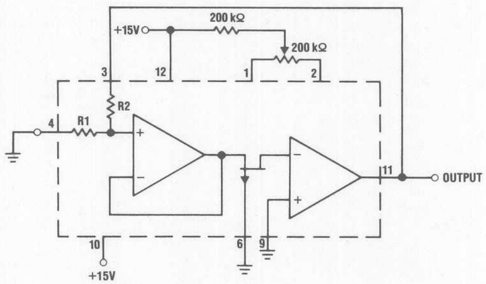


Figure 5. Offset Null Circuit

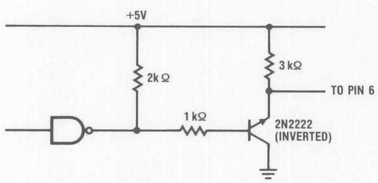


Figure 6. High Speed Gate Drive Circuit

Definition of Terms

Voltage, V_4: The voltage at pin 4, i.e., the analog input voltage.

Voltage, V_6: The voltage at pin 6, i.e., the logic control signal. A logic "1" input, $V_6 \leqslant 4.5V$, places the LH0053 in the HOLD mode; a logic "0" input ($V_6 \leqslant 0.5V$) places the device in sample mode.

Acquisition Time: The time required for the output (pin 11) to settle within the rated accuracy after a specified input change is applied to Analog Input 1 (pin 4) with logic input, (pin 6) in the logic "0" state.

Aperture Time: The time indeterminacy when switching from the "sample" mode to the HOLD mode measured from the time the logic input passes through its threshold (2.0V) to the time the device actually enters the HOLD mode.

Sample Accuracy: Difference between input voltage and output voltage while in the sample mode, expressed as a percent of the input voltage.

Section 8

A to D, D to A

8

Section Contents

† For additional information, see National Semiconductor's Data Conversion/Acquisition Handbook.

Part No.	Resolution (Bits)	Absolute Accuracy (Max)	Conversion Time	Input Voltage Range	Output Logic Levels	Supplies (V)	Temperature Range* M	I	C	Package	Comments
A/D CONVERTER											
ADC0800	8	±2 LSB	50 μs	±5V	TTL, TRI-STATE®	+5, −12	•		•	18-Pin DIP	
ADC0801	8	±1/4 LSB	110 μs	5V	TTL, TRI-STATE	+5	•	•	•	20-Pin DIP	Differential Input
ADC0802	8	±1/2 LSB	110 μs	5V	TTL, TRI-STATE	+5	•	•	•	20-Pin DIP	Differential Input
ADC0803	8	±1/2 LSB	110 μs	5V	TTL, TRI-STATE	+5		•	•	20-Pin DIP	Differential Input
ADC0804	8	±1 LSB	110 μs	5V	TTL, TRI-STATE	+5			•	20-Pin DIP	Differential Input
ADC0805	8	±1 LSB	110 μs	5V	TTL, TRI-STATE	+5		•	•	20-Pin DIP	Works with 5V Reference
ADC0808	8	±1/2 LSB	100 μs	5V	TTL, TRI-STATE	+5	•	•	•	28-Pin DIP	8-Channel MUX
ADC0809	8	±1 LSB	100 μs	5V	TTL, TRI-STATE	+5		•	•	28-Pin DIP	8-Channel MUX
ADC0816	8	±1/2 LSB	100 μs	5V	TTL, TRI-STATE	+5	•	•	•	40-Pin DIP	16-Channel MUX
ADC0817	8	±1 LSB	100 μs	5V	TTL, TRI-STATE	+5		•	•	40-Pin DIP	16-Channel MUX
†ADC0831B	8	±1/2 LSB	80 μs	5V	TTL	+5 to +9		•	•	8-Pin DIP	Serial I/O
†ADC0831C	8	±1 LSB	80 μs	5V	TTL	+5 to +9		•	•	8-Pin DIP	Serial I/O
†ADC0832B	8	±1/2 LSB	80 μs	5V	TTL	+5 to +9		•	•	8-Pin DIP	2-Channel MUX Serial I/O
†ADC0832C	8	±1 LSB	80 μs	5V	TTL	+5 to +9		•	•	8-Pin DIP	2-Channel MUX Serial I/O
ADC0833B	8	±1/2 LSB	80 μs	5V	TTL	+5 to +9		•	•	14-Pin DIP	4-Channel MUX Serial I/O
ADC0833C	8	±1 LSB	80 μs	5V	TTL	+5 to +9		•	•	14-Pin DIP	4-Channel MUX Serial I/O
†ADC0834B	8	±1/2 LSB	80 μs	5V	TTL	+5 to +9		•	•	14-Pin DIP	4-Channel MUX Serial I/O
†ADC0834C	8	±1 LSB	80 μs	5V	TTL	+5 to +9		•	•	14-Pin DIP	4-Channel MUX Serial I/O
†ADC0838B	8	±1/2 LSB	80 μs	5V	TTL	+5 to +9		•	•	20-Pin DIP	8-Channel MUX Serial I/O
†ADC0838C	8	±1 LSB	80 μs	5V	TTL	+5 to +9		•	•	20-Pin DIP	8-Channel MUX Serial I/O
†ADC1001B	10	±1/2 LSB	200 μs	5V	TTL, TRI-STATE	+5		•	•	20-Pin DIP	Differential Input
ADC1001C	10	±1 LSB	200 μs	5V	TTL, TRI-STATE	+5		•	•	20-Pin DIP	Differential Input
†ADC1021B	10	±1/2 LSB	200 μs	5V	TTL, TRI-STATE	+5		•	•	24-Pin DIP	Differential Input
ADC1021C	10	±1 LSB	200 μs	5V	TTL, TRI-STATE	+5		•		24-Pin DIP	Differential Input
†ADC1080	10	±1/2 LSB	18 μs	±10V	TTL	+5, ±12 to ±15		•		32-Pin DIP	With Reference and Clock

Part No.	Resolution (Bits)	Absolute Accuracy (Max)	Conversion Time	Input Voltage Range	Output Logic Levels	Supplies (V)	Temperature Range* M	I	C	Package	Comments
A/D CONVERTER (Continued)											
ADB1200 LF13300	12	± 1/2 LSB	36 ms	± 11V	TTL, TRI-STATE	+ 5, − 15 ± 15			•	28-Pin DIP 18-Pin DIP	Dual Slope
ADC1210	12	± 1/2 LSB	26 μs	10.2V	CMOS	+ 5 to ± 15	•	•		24-Pin DIP	
ADC1211	12(10)	± 1 LSB	30 μs	10.2V	CMOS	+ 5 to ± 15	•	•		24-Pin DIP	
†ADC1280	12	± 1/2 LSB	22 μs	± 10V	TTL	+ 5, ± 12 to ± 15		•		32-Pin DIP	With Reference and Clock
ADC3511	3 1/2-Digit	0.05%	200 ms	2V	TTL, TRI-STATE	+ 5			•	24-Pin DIP	Integrating μP Compatible
ADC3711	3 3/4-Digit	0.05%	400 ms	2V	TTL, TRI-STATE	+ 5			•	24-Pin DIP	Integrating μP Compatible
LM131	V-F	0.01%	N/A	V_{CC} − 2V	N/A	+ 5 to + 40	•	•	•	8-Pin DIP or TO-99 Can	Voltage-to-Frequency Converter 100 kHz Max
DIGITAL VOLTMETER											
ADD3501	3 1/2-Digit	0.05%	200 ms	2V	7-Segment LED Drive	+ 5			•	28-Pin DIP	3 1/2-Digit LED DVM
ADD3701	3 3/4-Digit	0.05%	400 ms	2V	7-Segment LED Drive	+ 5			•	28-Pin DIP	3 3/4-Digit LED DVM

*Temperature ranges are: "M" is − 55°C to + 125°C ambient; "I" is − 40°C to + 85°C or − 25°C to + 85°C; "C" is 0°C to 70°C.

†Product to be announced.

Part No.	Resolution (Bits)	Linearity @ 25°C (Max)	Internal Reference	Output Op Amp	Settling Time (+1/2 LSB)	Supplies (V)	Temperature Range* M	I	C	Package	Comments
DAC0800	8	0.19			100 ns	± 5 to ± 15	•		•	16-Pin DIP	High Speed Multiplying
DAC0801	8	0.39			100 ns	± 5 to ± 15	•		•	16-Pin DIP	High Speed Multiplying
DAC0802	8	0.10			100 ns	± 5 to ± 15	•		•	16-Pin DIP	High Speed Multiplying
DAC0806	8	0.78			150 ns	± 5 to ± 15			•	16-Pin DIP	Multiplying
DAC0807	8	0.39			150 ns	± 5 to ± 15			•	16-Pin DIP	Multiplying
DAC0808	8	0.19			150 ns	± 5 to ± 15	•		•	16-Pin DIP	Multiplying
DAC0830	8	0.05			1 μs	5 to 15	•	•	•	20-Pin DIP	μP Compatible 4-Quadrant Multiplying
DAC0831	8	0.10			1 μs	5 to 15		•	•	20-Pin DIP	μP Compatible 4-Quadrant Multiplying
DAC0832	8	0.20			1 μs	5 to 15		•	•	20-Pin DIP	μP Compatible 4-Quadrant Multiplying
DAC1000	10	0.05			500 ns	5 to 15	•	•	•	24-Pin DIP	μP Compatible Double Buffered
DAC1001	10	0.1			500 ns	5 to 15		•	•	24-Pin DIP	μP Compatible Double Buffered
DAC1002	10	0.2			500 ns	5 to 15		•	•	24-Pin DIP	μP Compatible Double Buffered
DAC1006	10	0.05			500 ns	5 to 15	•	•	•	20-Pin DIP	μP Compatible Double Buffered
DAC1007	10	0.1			500 ns	5 to 15		•	•	20-Pin DIP	μP Compatible Double Buffered
DAC1008	10	0.2			500 ns	5 to 15		•	•	20-Pin DIP	μP Compatible Double Buffered
DAC1020	10	0.05			500 ns	5 to 15	•	•	•	16-Pin DIP	4-Quadrant Multiplying
DAC1021	10	0.1			500 ns	5 to 15	•	•	•	16-Pin DIP	4-Quadrant Multiplying
DAC1022	10	0.2			500 ns	5 to 15	•	•	•	16-Pin DIP	4-Quadrant Multiplying
DAC1200	12	0.012	•	•	300 ns – I_{OUT} 2.5 μs – V_{OUT}	± 15	•	•		24-Pin DIP	Current or Voltage Mode
DAC1201	12	0.049	•	•	300 ns – I_{OUT} 2.5 μs – V_{OUT}	± 15	•	•		24-Pin DIP	Current or Voltage Mode
DAC1208	12	0.012			1 μs	5 to 15		•	•	24-Pin DIP	μP Compatible 4-Quadrant Multiplying
DAC1209	12	0.024			1 μs	5 to 15		•	•	24-Pin DIP	μP Compatible 4-Quadrant Multiplying

											4-Quadrant Multiplying
DAC1218	12	0.012			1 μs	5 to 15	•		•	18-Pin DIP	4-Quadrant Multiplying
DAC1219	12	0.024			1 μs	5 to 15	•		•	18-Pin DIP	4-Quadrant Multiplying
DAC1220	12	0.05			500 ns	5 to 15	•	•	•	18-Pin DIP	4-Quadrant Multiplying
DAC1221	12	0.1			500 ns	5 to 15	•	•	•	18-Pin DIP	4-Quadrant Multiplying
DAC1222	12	0.2			500 ns	5 to 15	•	•	•	18-Pin DIP	4-Quadrant Multiplying
DAC1230	12	0.012			1 μs	5 to 15	•	•	•	20-Pin DIP	μP Compatible 4-Quadrant Multiplying
DAC1231	12	0.024			1 μs	5 to 15		•	•	20-Pin DIP	μP Compatible 4-Quadrant Multiplying
DAC1232	12	0.05			1 μs	5 to 15		•	•	20-Pin DIP	μP Compatible 4-Quadrant Multiplying
†DAC1265A	12	0.006	•		200 ns	± 15	•		•	24-Pin DIP	Hi-Speed
†DAC1265	12	0.012	•		200 ns	± 15	•		•	24-Pin DIP	Hi-Speed
DAC1280	12	0.024	•	•	300 ns – I_{OUT} 2.5 μs – V_{OUT}	± 15			•	24-Pin DIP	Current or Voltage Mode
DAC1280A	12	0.012	•	•	300 ns – I_{OUT} 2.5 μs – V_{OUT}	± 11.4 to ± 15.75			•	24-Pin DIP	Current or Voltage Mode
DAC1285	12	0.012	•	•	300 ns – I_{OUT} 2.5 μs – V_{OUT}	± 15	•	•		24-Pin DIP	Current or Voltage Mode
DAC1285A	12	0.012	•	•	300 ns – I_{OUT} 2.5 μs – V_{OUT}	± 11.4 to ± 15.75	•	•		24-Pin DIP	Current or Voltage Mode

*Ambient temperature range for "M" is −55°C to +125°C, "I" is −25°C to +85°C or −40°C to +85°C, "C" is 0°C to 70°C.
†Product to be announced.

National Semiconductor

Definition of Terms

Accuracy: Sum of all errors: non-linearity, zero-scale, full-scale, temperature drift, etc. Careful–this term is sometimes confused with resolution and/or non-linearity.

Conversion Time: The time required for a complete measurement by an A/D converter.

Full-Scale Error: Deviation from true full-scale output when specified reference voltage is applied.

Full-Scale Tempco: Change in scale error due to temperature, usually expressed in parts per million per degree (ppm/°C).

Monotonicity: A DAC whose output always increases for increasing digital input codes is said to be monotonic, i.e., does not decrease at any point.

Non-Linearity: Worst-case deviation from the line between the endpoints (zero and full-scale). Can be expressed as a percentage of full-scale or in fractions of an LSB. ± 1/2 LSB is a desirable specification.

Power-Supply Sensitivity: The sensitivity of a converter to DC changes in power-supply voltages is normally expressed in terms of percentage change in analog input value. Power-supply sensitivity may also be expressed in relation to a specified DC shift of the supply voltage.

Quantizing Error: ± 1/2 LSB error inherent in all A/D conversions. Cannot be eliminated.

Ratiometric Converter: The output of an A/D converter is a digital number proportional to the ratio of (some measure of) the input to a reference. Most requirements for conversions call for an absolute measurement, i.e., against a fixed reference. In some cases, where the measurement is affected by a changing reference voltage, it is advantageous to use that same reference as the reference for the conversion, to eliminate the effect of variation.

Resolution: The most important converter specification. This is the number of steps the full-scale signal can be divided into, and therefore the size of the steps. May be expressed as the number of bits in the digital word, the size of a least significant bit (smallest step) as a percent of full-scale, or an LSB in millivolts (for a given full-scale).

Bits	Steps (2N)	LSB Size (% of Full-Scale)	LSB Size (10V Full-Scale)
6	64	1.588%	158.8 mV
8	256	0.392%	39.2 mV
10	1,024	0.0978%	9.78 mV
12	4,096	0.0244%	2.44 mV
14	16,384	0.0061%	0.61 mV
16	65,536	0.0015%	0.15 mV

Settling Time: Time from change in input until output remains within ± 1/2 LSB (or some specified percentage) of final output.

3 1/2 Digit BCD: Maximum output count or display is ± 1.999 (± 2000 counts)—approximately 11 binary bits plus sign.

3 3/4 Digit BCD: Maximum output count or display is ± 3.999 (± 4000 counts)—approximately 12 binary bits plus sign.

National Semiconductor

AD7520/AD7530 10-Bit, AD7521/AD7531 12-Bit Binary Multiplying D/A Converters

General Description

The AD7520 and the AD7521 are, respectively, 10 and 12-bit binary multiplying digital-to-analog converters. A deposited thin film R-2R resistor ladder divides the reference current and provides the circuit with excellent temperature tracking characteristics (typically 0.0002%/°C linearity error temperature coefficient). The circuit uses CMOS current switches and drive circuitry to achieve low power consumption (30 mW max) and low leakages (200 nA max). The digital inputs are compatible with DTL/TTL logic levels as well as full CMOS logic level swings. This part, combined with an external amplifier and voltage reference, can be used as a standard D/A converter; however, it is also very attractive for multiplying applications (such as digitally controlled gain blocks) since its linearity error is essentially independent of the voltage reference.

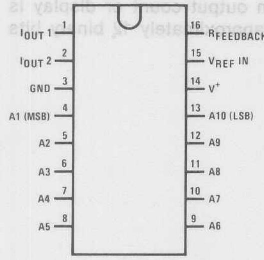
This part is available with 10-bit (0.05%), 9-bit (0.10%), and 8-bit (0.20%) non-linearity. The AD7520L, AD7520K, and AD7520J are direct replacements for the 10-bit resolution AD7520 and AD7530 family, and equivalent to AD7533 family. The AD7521K, AD7521J and AD7521L are direct replacements for the 12-bit resolution AD7521 and AD7531 family. For more information, see DAC1020 data sheet.

Features

- Linearity specified with zero and full-scale adjust only
- Integrated thin film on CMOS structure
- 10-bit or 12-bit resolution
- Low power dissipation 10 mW @ 15V typ
- Accepts variable or fixed reference $-25V \leq V_{REF} \leq +25V$
- 4-quadrant multiplying capability
- Interfaces directly with DTL, TTL and CMOS
- Fast settling time—600 ns typ
- Low feedthrough error—1/2 LSB @ 100 kHz typ

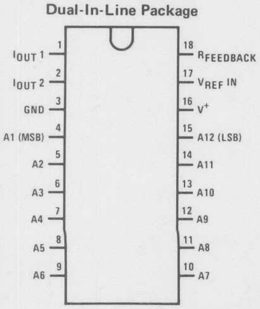
Connection Diagrams

AD7520/AD7530
Dual-In-Line Package



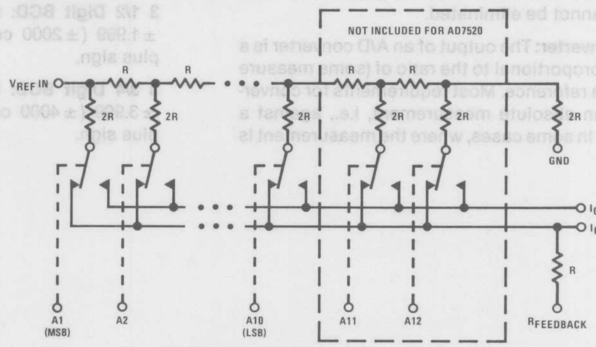
TOP VIEW

AD7521/AD7531
Dual-In-Line Package



TOP VIEW

Equivalent Circuit



Switches shown in digital high state

Ordering Information*

10-BIT D/A CONVERTERS

TEMPERATURE RANGE		0°C to 70°C		−40°C to +85°C		−55°C to +125°C
ACCURACY	0.05%	AD7520LN	AD7530LN	AD7520LD	AD7530LD	AD7520UD
	0.10%	AD7520KN	AD7530KN	AD7520KD	AD7530KD	AD7520TD
	0.20%	AD7520JN	AD7530JN	AD7520JD	AD7530JD	AD7520SD
PACKAGE OUTLINE		N16A		D16C		D16C

12-BIT D/A CONVERTERS

TEMPERATURE RANGE		0°C to 70°C		−40°C to +85°C		−55°C to +125°C
ACCURACY	0.05%	AD7521LN	AD7531LN	AD7521LD	AD7531LD	AD7521UD
	0.10%	AD7521KN	AD7531KN	AD7521KD	AD7531KD	AD7521TD
	0.20%	AD7521JN	AD7531JN	AD7521JD	AD7531JD	AD7521SD
PACKAGE OUTLINE		N18A		D18A		D18A

*Note: Devices ordered using these P/N's will be marked with AD7520 series and DAC102X series numbers.

Absolute Maximum Ratings

V^+ to Gnd	17V
V_{REF} to Gnd	±25V
Digital Input Voltage Range	V^+ to Gnd
DC Voltage at Pin 1 or Pin 2 (Note 3)	−100 mV to V^+
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Temperature Range

	MIN	MAX	UNITS
AD7520LN, AD7520KN, AD7520JN	0	+70	°C
AD7521LN, AD7521KN, AD7521JN	0	+70	°C
AD7530LN, AD7530KN, AD7530JN	0	+70	°C
AD7531LN, AD7531KN, AD7531JN	0	+70	°C
AD7520LD, AD7520KD, AD7520JD	−40	+85	°C
AD7521LD, AD7521KD, AD7521JD	−40	+85	°C
AD7530LD, AD7530KD, AD7530JD	−40	+85	°C
AD7531LD, AD7531KD, AD7531JD	−40	+85	°C
AD7520UD, AD7520TD, AD7520SD	−55	+125	°C
AD7521UD, AD7521TD, AD7521SD	−55	+125	°C

Electrical Characteristics (V^+ = 15V, V_{REF} = 10.000V, T_A = 25°C unless otherwise specified)

PARAMETER	CONDITIONS	AD7520L, AD7520K, AD7520J			AD7521L, AD7521K, AD7521J			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Resolution		10			12			Bits
Linearity Error	$T_{MIN} \le T_A \le T_{MAX}$, $-10V \le V_{REF} \le +10V$, (Note 1) End Point Adjustment Only (See Linearity Error in Definition of Terms)							
10-bit Parts	AD7520L, AD7520U, AD7521L, AD7521U, AD7530L, AD7531L			0.05			0.05	% FSR
9-bit Parts	AD7520T, AD7520K, AD7521T, AD7521K, AD7530K, AD7531K			0.10			0.10	% FSR
8-bit Parts	AD7520S, AD7520J, AD7521S, AD7521J, AD7530J, AD7531J			0.20			0.20	% FSR
Linearity Error Tempco	$-10V \le V_{REF} \le +10V$, (Notes 1 and 2)		0.0002			0.0002		% FS/°C
Full-Scale Error	$-10V \le V_{REF} \le +10V$, (Notes 1 and 2)		0.3			0.3		% FS
Full-Scale Error Tempco	$T_{MIN} < T_A < T_{MAX}$, (Note 2)			0.001			0.001	% FS/°C
Output Leakage Current								
I_{OUT1}	All Digital Inputs Low, $T_{MIN} \le T_A \le T_{MAX}$			200			200	nA
I_{OUT2}	All Digital Inputs High, $T_{MIN} \le T_A \le T_{MAX}$			200			200	nA
Power Supply Sensitivity	All Digital Inputs High, $14V \le V^+ \le 16V$ (*Figure 2* of DAC1020 data sheet)		0.005			0.005		% FS/V
V_{REF} Input Resistance		10	15	20	10	15	20	kΩ
Full-Scale Current Settling Time	R_L = 100Ω from 0 to 99.95% FS All Digital Inputs Switched Simultaneously		500			500		ns
V_{REF} Feedthrough	All Digital Inputs Low, V_{REF} = 20 Vp-p @ 100 kHz			10			10	mVp-p
	D Package (Note 4)		6	9		6	9	mVp-p
	N Package		2	5		2	5	mVp-p
Output Capacitance								
I_{OUT1}	All Digital Inputs Low		40			40		pF
	All Digital Inputs High		200			200		pF
I_{OUT2}	All Digital Inputs Low		200			200		pF
	All Digital Inputs High		40			40		pF
Digital Input	(Note 1)							
Low Threshold	$T_{MIN} < T_A < T_{MAX}$,			0.8			0.8	V
High Threshold	$T_{MIN} < T_A < T_{MAX}$	2.4			2.4			V
Digital Input Current	$T_{MIN} \le T_A \le T_{MAX}$							
	Digital Input High		1	100		1	100	μA
	Digital Input Low		−50	−200		−50	−200	μA
Supply Current	All Digital Inputs High		0.2	1.6		0.2	1.6	mA
	All Digital Inputs Low		0.6	2		0.6	2	mA
Operating Power Supply Range		5		15	5		15	V

Note 1: V_{REF} = ±10V and V_{REF} = ±1V.

Note 2: Using internal feedback resistor.

Note 3: Both I_{OUT1} and I_{OUT2} must go to ground or the virtual ground of an operational amplifier. For every millivolt offset between I_{OUT1} or I_{OUT2}, 0.005% linearity error will be introduced.

Note 4: To achieve this low feedthrough in D package, the user must ground the metal lid.

ADB1200 12-Bit Binary A/D Building Block

General Description

The ADB1200 is the digital controller for the LF13300D* analog building block. Together they form an integrating 12-bit A/D converter. The ADB1200 provides all the necessary control functions, plus features like auto zeroing, polarity and overrange indication, as well as continuous conversion. The 12-bit plus sign parallel and serial outputs are TRI-STATE® TTL level compatible. The device also includes output latches to simplify data bus interfacing.

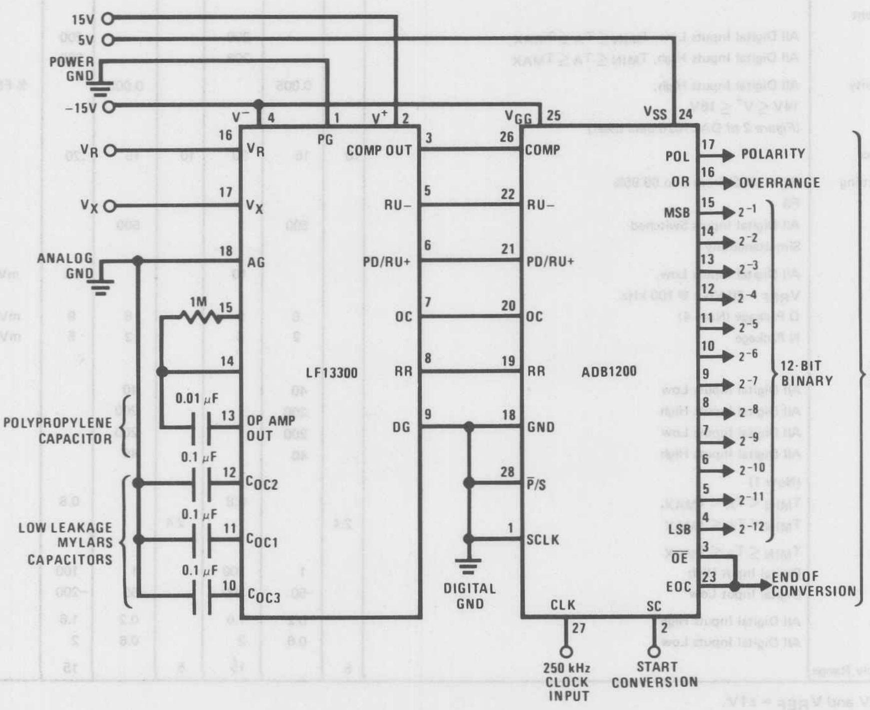
*See LF13300D data sheet for more information

Features

- 12-bit binary output
- Parallel or serial output
- TRI-STATE output
- Polarity indication
- Overrange indication
- Continuous conversion capability
- 100% overrange capability
- 5V, −15V power requirements
- TTL compatible
- Clock frequency to 1 MHz

Circuit Diagram/Typical Applications

12-Bit A/D Converter



Absolute Maximum Ratings

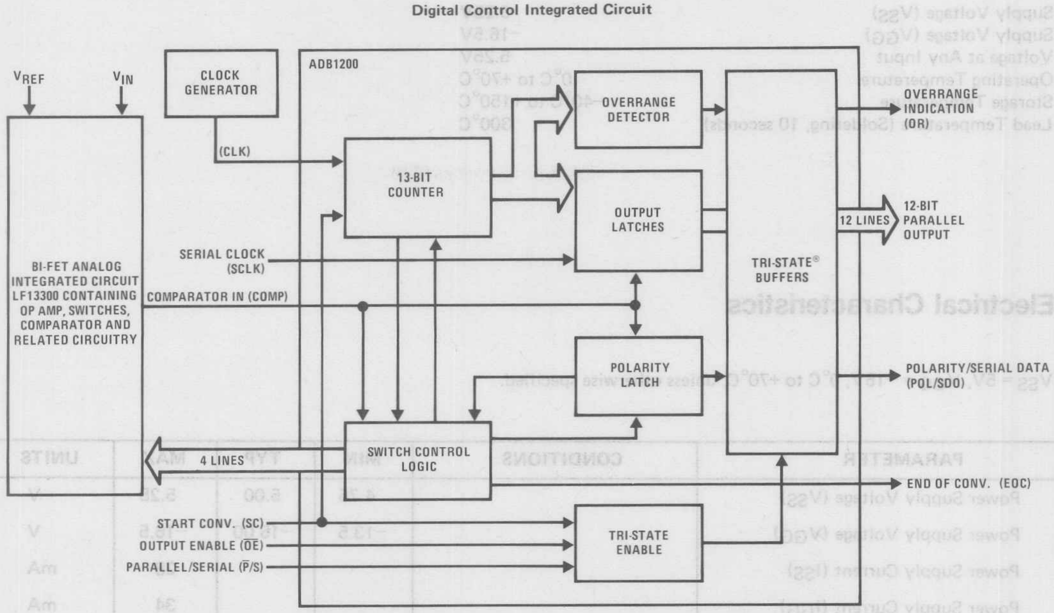
Supply Voltage (V_{SS})	5.25V
Supply Voltage (V_{GG})	−16.5V
Voltage at Any Input	5.25V
Operating Temperature	0°C to +70°C
Storage Temperature	−40°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

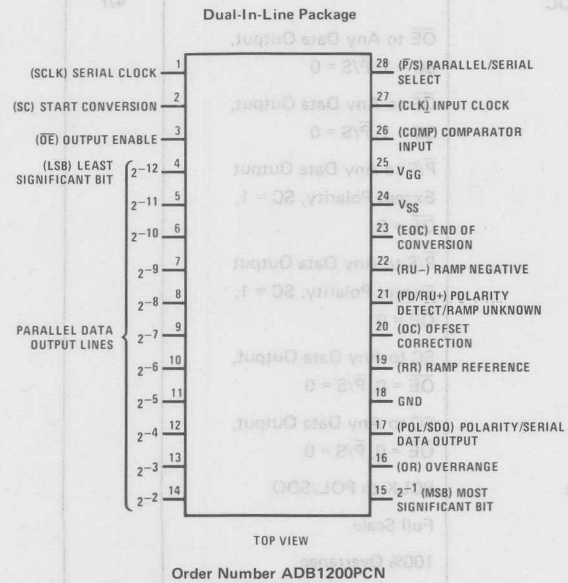
V_{SS} = 5V, V_{GG} = −15V, 0°C to +70°C, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage (V_{SS})		4.75	5.00	5.25	V
Power Supply Voltage (V_{GG})		−13.5	−15.00	−16.5	V
Power Supply Current (I_{SS})				28	mA
Power Supply Current (I_{GG})				34	mA
Logic "1" Input Voltage		3.4			V
Logic "0" Input Voltage				0.8	V
Logic "1" Output Voltage	V_{SS} = 4.75V, I_{OH} = 100 µA	3.8			V
Logic "0" Output Voltage	V_{SS} = 5.25V, I_{OL} = −1.6 mA			0.4	V
Width of EOC	Auto Cycle	5/f			sec
Prop. Delay COMP to EOC		4/f		5/f+1 µs	sec
Output Enable Time	$\overline{OE}$ to Any Data Output, SC = 1, $\overline{P}$/S = 0			1.0	µs
Output Disable Time	$\overline{OE}$ to Any Data Output, SC = 1, $\overline{P}$/S = 0			2.4	µs
Output Enable Time	$\overline{P}$/S to Any Data Output Except Polarity, SC = 1, $\overline{OE}$ = 0			0.9	µs
Output Disable Time	$\overline{P}$/S to Any Data Output Except Polarity, SC = 1, $\overline{OE}$ = 0			2.2	µs
Output Enable Time	SC to Any Data Output, $\overline{OE}$ = 0, $\overline{P}$/S = 0			1.0	µs
Output Disable Time	SC to Any Data Output, $\overline{OE}$ = 0, $\overline{P}$/S = 0			2.4	µs
Prop. Delay Serial Clock	SCLK to POL/SDO			0.6	µs
Conversion Time	Full Scale			8966/f	sec
Conversion Time	100% Overrange			13062/f	sec
Maximum Clock Frequency	CLK, Pin 27	500	1000		kHz
Maximum Serial Clock Frequency	SCLK, Pin 1	500	1000		kHz

Block Diagram



Connection Diagram



Order Number ADB1200PCN
See NS Package N28A

Functional Description

OPERATION

The ADB1200 is designed for use with the LF13300 analog front end. Four control signals are supplied to the LF13300 and 1 control signal is required from the LF13300. The conversion cycle is composed of 5 distinct phases. They are: Phase I — Offset Correct; Phase II — Polarity Detect; Phase III — Initialization; Phase IV — Ramp Unknown; Phase V — Ramp Reference.

Phase I — Offset Correct (256 Clock Periods)

This phase is initiated by taking the Start Conversion (SC) and the Output Enable ($\overline{OE}$) lines to a logic "1". At this time, Offset Correct (OC) will be a logic "1". The LF13300 requires this phase to correct any intrinsic offset voltage errors prior to the polarity detect phase.

Phase II — Polarity Detect (256 Clock Periods)

This phase is used to determine polarity of the analog input. At the midpoint of this phase, COMP from the LF13300 is examined for polarity. If COMP = logic "1", then the input voltage is positive. If COMP = logic "0", then the input is negative. The Polarity Detect signal (PD/RU+) will be at a logic "1" during this entire phase. The above operation is also necessary to determine which integrator input (positive or negative) of the LF13300 should be used for proper A/D conversion (see LF13300 data sheet).

Phase III — Initialization (256 Clock Periods)

This phase is identical to Phase I and is used by the LF13300 to eliminate any offsets induced as a result of the Polarity Detect Phase. Offset Correct (OC) will be at a logic "1".

Phase IV — Ramp Unknown (4096 Clock Periods)

The unknown input voltage is integrated for a fixed time, 4096 clock periods, during this phase. The result of the Phase II Polarity Detect Cycle determines whether PD/RU+ or RU− will be at logic "1". If Phase II indicates a positive input, the PD/RU+ signal will be a logic "1". If phase II indicates a negative input, Ramp Negative (RU−) will be a logic "1". These 2 signals will never be at logic "1" simultaneously.

Phase V — Ramp Reference

This phase is a variable length phase depending on the magnitude of the analog input voltage. During this time, Ramp Reference (RR) will be in the logic "1" state. When COMP goes to a logic "0" state, or when the internal counter reaches 100% of full scale (8192 clock periods), the Ramp Reference (RR) signal goes to the logic "0" state, the counter output is loaded into the output register, and the End of Conversion (EOC) signal goes to a logic "1". The Polarity Bit will reflect whatever value was determined during Phase II. The output register will hold the data until a new conversion is completed and new data is loaded into the register. The $\overline{OE}$ line must be low in the logic "0" state and SC must be high in the logic "1" state to enable the outputs.

DATA OUTPUTS

Both serial and parallel outputs are available. In either case, $\overline{OE}$ must be low and SC must be high to enable the outputs. For parallel output, the $\overline{P}$/S line must be low in the logic "0" state. For serial outputs, the $\overline{P}$/S line must be high. In the serial mode, the data is shifted out of the Polarity/Serial Output (POL/SDO) line and all other data outputs are in the high impedance state. Each Serial Clock (SCLK) will right shift the output register one bit. Thus, 13 clock pulses are required to fully shift out the data. The data will be shifted out in the following order: Polarity, Overrange, MSB, 2SB, 3SB, . . . , LSB. If $\overline{OE}$ and $\overline{P}$/S are in the logic "0" state and SC in the logic "1" state, all outputs will momentarily go to the logic "1" state for 1 clock period immediately preceding EOC.

CONTINUOUS CONVERT MODE

In this mode, the End of Conversion (EOC) output is connected to the $\overline{OE}$ input. As long as SC is in the logic "1" state, then each EOC will initiate a new conversion. The data outputs will be disabled for the first 5 clock cycles after EOC goes high.

Truth Table

INPUT	SC	OE	P/S	LSB											MSB	OVER-RANGE	POLARITY
100% Full Scale	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Full Scale	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1
Zero	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Zero	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
−Full Scale	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0
−100% Full Scale	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0
Any	1	1	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
Any	1	0	1	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Serial Output
Any	0	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

1 = High
0 = Low
Z = High Impedance
X = Don't Care

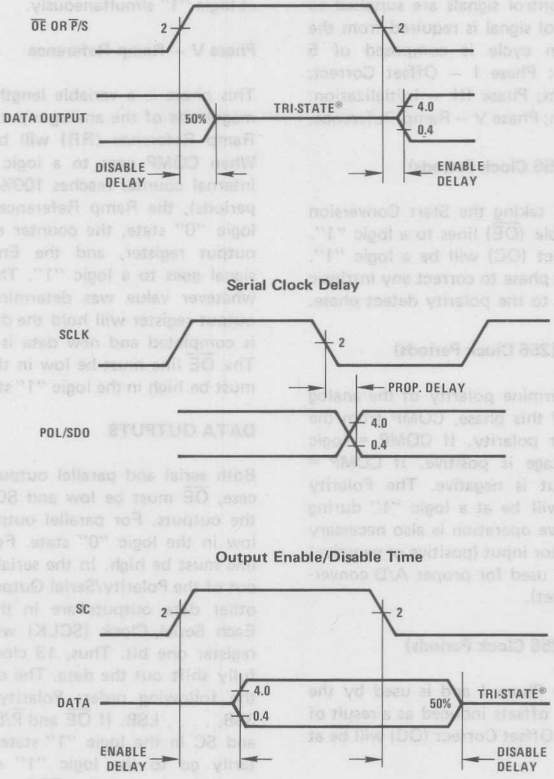


FIGURE 1. Parallel Data

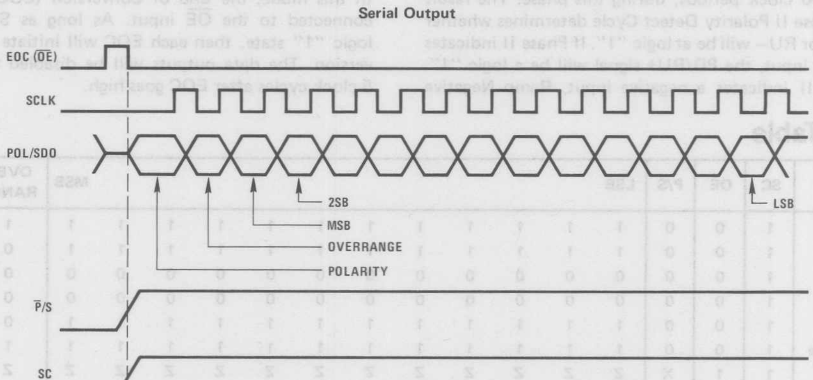


FIGURE 2. Serial Data

Timing Diagrams (Continued)

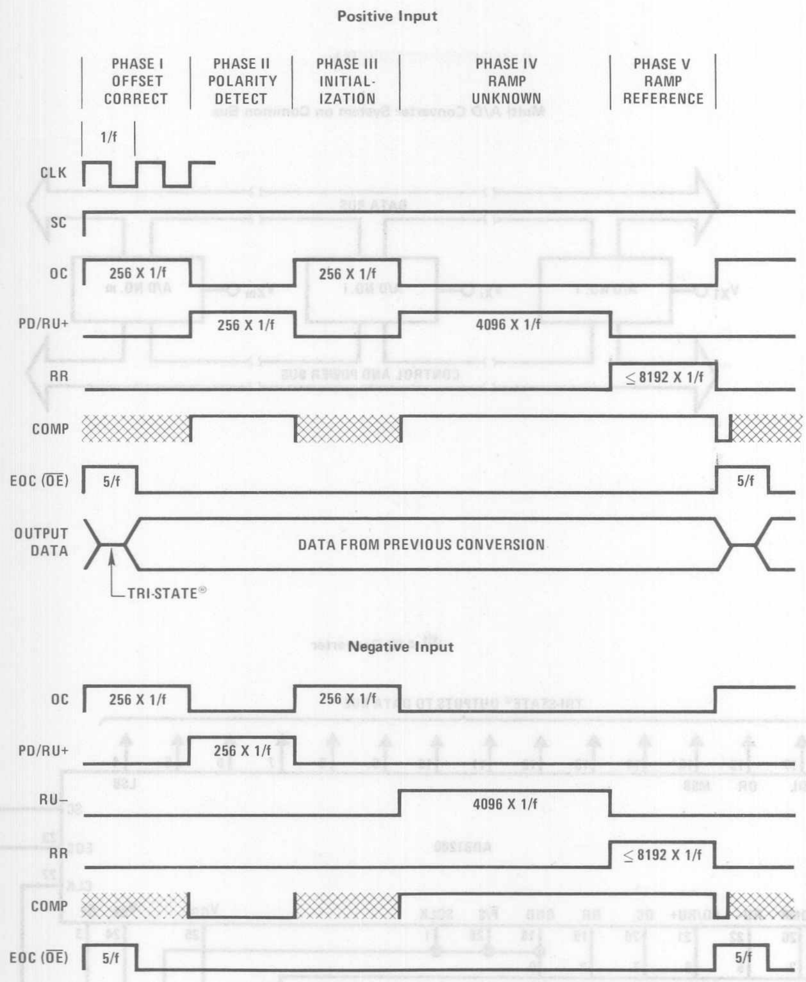


FIGURE 3. Continuous Conversion Mode

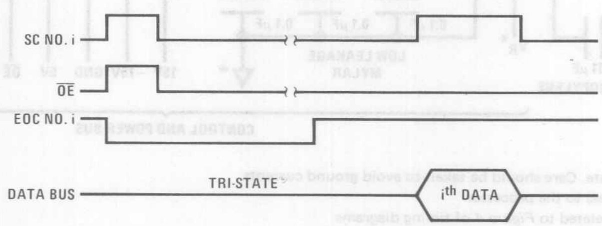


FIGURE 4. i^{th} A/D Converter Data Retrieval Sequence

ADB1200

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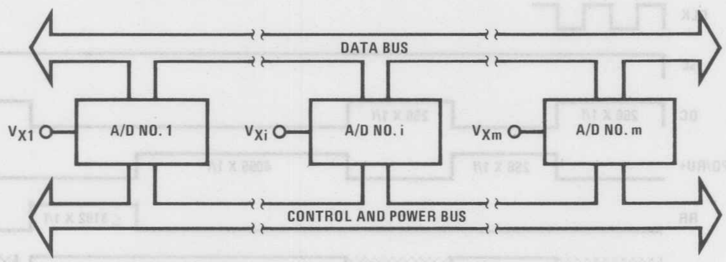
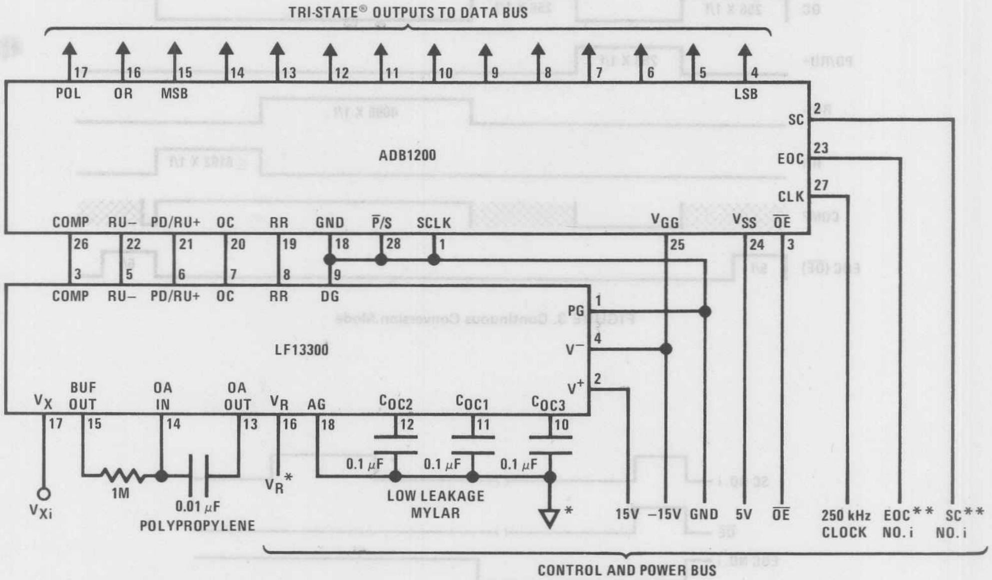
Typical Applications (Continued)

Multi A/D Converter System on Common Bus



i[th] A/D Converter



*May be common or separate. Care should be taken to avoid ground currents

**Direct or multiplexed access to the processor

Note. This application is related to *Figure 4* of timing diagrams

National Semiconductor

ADC0800 8-Bit A/D Converter

General Description

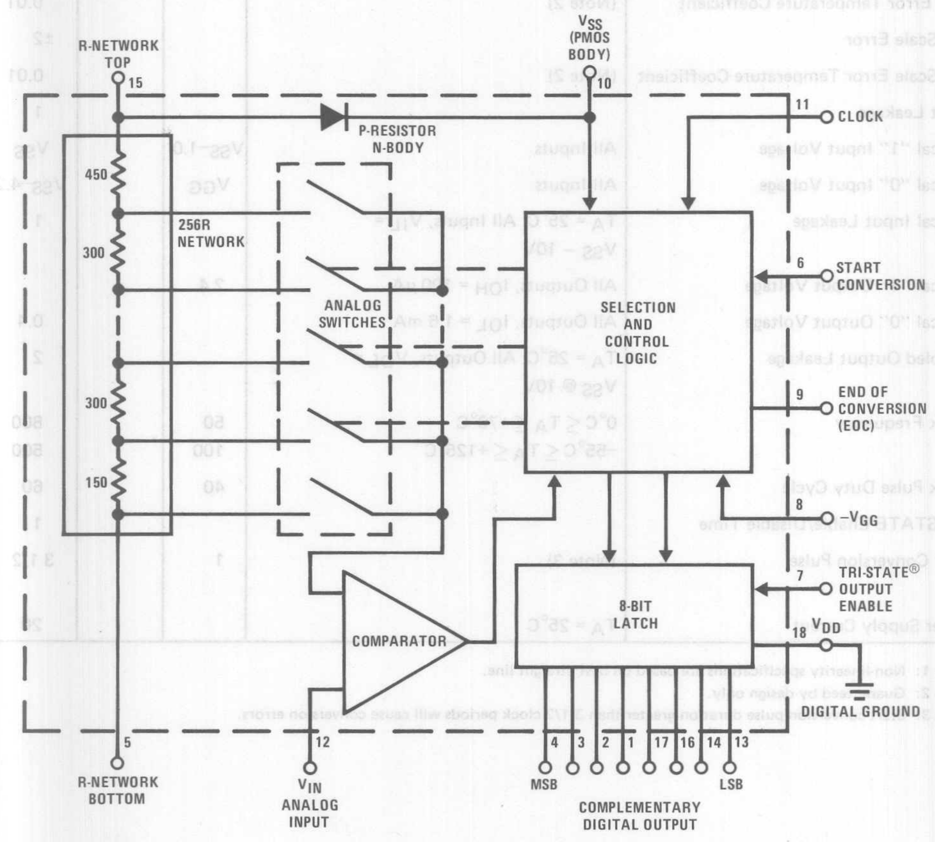
The ADC0800 is an 8-bit monolithic A/D converter using P-channel ion-implanted MOS technology. It contains a high input impedance comparator, 256 series resistors and analog switches, control logic and output latches. Conversion is performed using a successive approximation technique where the unknown analog voltage is compared to the resistor tie points using analog switches. When the appropriate tie point voltage matches the unknown voltage, conversion is complete and the digital outputs contain an 8-bit complementary binary word corresponding to the unknown. The binary output is TRI-STATE® to permit bussing on common data lines.

The ADC0800PD is specified over −55°C to +125°C and the ADC0800PCD is specified over 0°C to 70°C.

Features

- Low cost
- ±5V, 10V input ranges
- No missing codes
- Ratiometric conversion
- TRI-STATE outputs
- Fast — $T_C = 50\ \mu s$
- Contains output latches
- TTL compatible
- Supply voltages — 5 V_{DC} and −12 V_{DC}
- Resolution — 8 bits
- Linearity — ±1 LSB
- Conversion speed — 40 clock periods
- Clock range — 50 to 800 kHz

Block Diagram



(00000000 = +full-scale)

8

Supply Voltage (V_{GG})	V_{SS}−22V
Voltage at Any Input	V_{SS} + 0.3V to V_{SS}−22V
Storage Temperature	150°C
Operating Temperature	
ADC0800PD	−55°C to +125°C
ADC0800PCD	0°C to +70°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

These specifications apply for V_{SS} = 5.0 V_{DC}, V_{GG} = −12.0 V_{DC}, V_{DD} = 0 V_{DC}, a reference voltage of 10.000 V_{DC} across the on-chip R-network ($V_{R\text{-NETWORK TOP}}$ = 5.000 V_{DC} and $V_{R\text{-NETWORK BOTTOM}}$ = −5.000 V_{DC}), and a clock frequency of 800 kHz. For all tests, a 475Ω resistor is used from pin 5 to ground. Unless otherwise noted, these specifications apply over an ambient temperature range of −55°C to +125°C for the ADC0800PD and 0°C to +70°C for the ADC0800PCD.

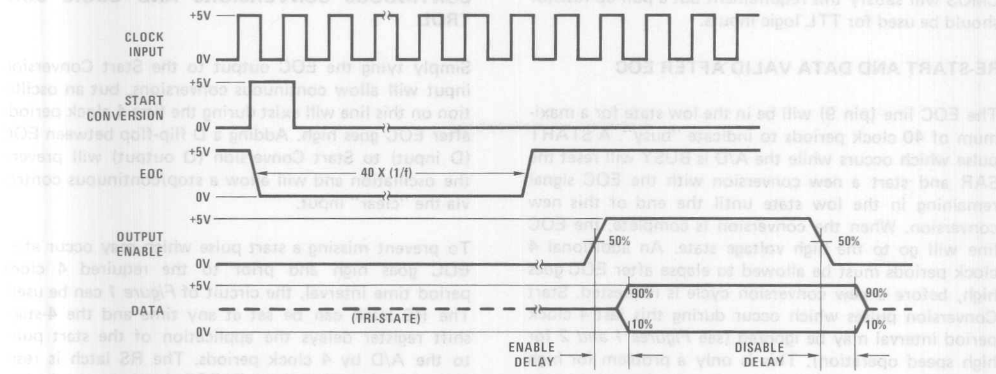
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Non-Linearity	T_A = 25°C, (Note 1)			±1	LSB
	Over Temperature, (Note 1)			±2	LSB
Differential Non-Linearity				±1/2	LSB
Zero Error				±2	LSB
Zero Error Temperature Coefficient	(Note 2)			0.01	%/°C
Full-Scale Error				±2	LSB
Full-Scale Error Temperature Coefficient	(Note 2)			0.01	%/°C
Input Leakage				1	μA
Logical "1" Input Voltage	All Inputs	V_{SS}−1.0		V_{SS}	V
Logical "0" Input Voltage	All Inputs	V_{GG}		V_{SS}−4.2	V
Logical Input Leakage	T_A = 25°C, All Inputs, V_{IL} = V_{SS} − 10V			1	μA
Logical "1" Output Voltage	All Outputs, I_{OH} = 100 μA	2.4			V
Logical "0" Output Voltage	All Outputs, I_{OL} = 1.6 mA			0.4	V
Disabled Output Leakage	T_A = 25°C, All Outputs, V_{OL} = V_{SS} @ 10V			2	μA
Clock Frequency	0°C ≤ T_A ≤ +70°C	50		800	kHz
	−55°C ≤ T_A ≤ +125°C	100		500	kHz
Clock Pulse Duty Cycle		40		60	%
TRI-STATE Enable/Disable Time				1	μs
Start Conversion Pulse	(Note 3)	1		3 1/2	Clock Periods
Power Supply Current	T_A = 25°C			20	mA

Note 1: Non-linearity specifications are based on best straight line.

Note 2: Guaranteed by design only.

Note 3: Start conversion pulse duration greater than 3 1/2 clock periods will cause conversion errors.

Timing Diagram



Data is complementary binary (full scale is all "0's" output).

Application Hints

OPERATION

The ADC0800 contains a network with 256-300Ω resistors in series. Analog switch taps are made at the junction of each resistor and at each end of the network. In operation, a reference (10.00V) is applied across this network of 256 resistors. An analog input (V_{IN}) is first compared to the center point of the ladder via the appropriate switch. If V_{IN} is larger than $V_{REF}/2$, the internal logic changes the switch points and now compares V_{IN} and 3/4 V_{REF}. This process, known as successive approximation, continues until the best match of V_{IN} and V_{REF}/N is made. N now defines a specific tap on the resistor network. When the conversion is complete, the logic loads a binary word corresponding to this tap into the output latch and an end of conversion (EOC) logic level appears. The output latches hold this data valid until a new conversion is completed and new data is loaded into the latches. The data transfer occurs in about 200 ns so that valid data is present virtually all the time. Conversion requires 40 clock periods. The device may be operated in the free running mode by connecting the Start Conversion line to the End of Conversion line. However, to ensure start-up under all possible conditions, an external Start Conversion pulse is required during power up conditions.

REFERENCE

The reference applied across the 256 resistor network determines the analog input range. V_{REF} = 10.00V with the top of the R-network connected to 5V and the bottom connected to −5V gives a ±5V range. The reference can be level shifted between V_{SS} and V_{GG}. However, the voltage, which is applied to the top of the R-network (pin 15), must not exceed V_{SS} to prevent forward biasing the on-chip parasitic silicon diode which exists between the P-diffused resistors (pin 15) and the N-type body (pin 10, V_{SS}). Use of a standard logic power supply for V_{SS} can cause problems, both due to initial voltage tolerance and changes over temperature. A solution is to power the V_{SS} line (15 mA max drain) from the output of the op amp which is used to bias the top of the R-network (pin 15). The analog input voltage and the voltage which is applied to the bottom of the R-network (pin 5) must be at least 7V above the $-V_{DD}$ supply voltage to insure adequate voltage drive to the analog switches .

Other reference voltages may be used (such as 10.24V). If a 5V reference is used, the analog range will be 5V and accuracy will be reduced by a factor of 2. Thus, for maximum accuracy, it is desirable to operate with at least a 10V reference. For TTL logic levels, this requires 5V and −5V for the R-network. CMOS can operate at the 10 V_{DC} V_{SS} level and a single 10 V_{DC} reference can be used. All digital voltage levels for both inputs and outputs will be from ground to V_{SS}.

ANALOG INPUT AND SOURCE RESISTANCE CONSIDERATIONS

The lead to the analog input (pin 12) should be kept as short as possible. Both noise and digital clock coupling to this input can cause conversion errors. To minimize any input errors, the following source resistance considerations should be noted:

For $R_s \leq 5k$	No analog input bypass capacitor required, although a 0.1 μF input bypass capacitor will prevent pick-up due to unavoidable series lead inductance.
For $5k < R_s \leq 20k$	A 0.1 μF capacitor from the input (pin 12) to ground should be used.
For $R_s > 20k$	Input buffering is necessary.

If the overall converter system requires lowpass filtering of the analog input signal, use a 20 kΩ or less series resistor for a passive RC section or add an op amp RC active lowpass filter (with its inherent low output resistance) to insure accurate conversions.

CLOCK COUPLING

The clock lead should be kept away from the analog input line to reduce coupling.

LOGIC INPUTS

The logical "1" input voltage swing for the Clock, Start Conversion and Output Enable should be (V_{SS} − 1.0V).

Application Hints (Continued)

CMOS will satisfy this requirement but a pull-up resistor should be used for TTL logic inputs.

RE-START AND DATA VALID AFTER EOC

The EOC line (pin 9) will be in the low state for a maximum of 40 clock periods to indicate "busy". A START pulse which occurs while the A/D is BUSY will reset the SAR and start a new conversion with the EOC signal remaining in the low state until the end of this new conversion. When the conversion is complete, the EOC line will go to the high voltage state. An additional 4 clock periods must be allowed to elapse after EOC goes high, before a new conversion cycle is requested. Start Conversion pulses which occur during this last 4 clock period interval may be ignored (see *Figures 1 and 2* for high speed operation). This is only a problem for high conversion rates and keeping the number of conversions per second less than (1/44) x f_{CLOCK} automatically guarantees proper operation. For example, for an 800 kHz clock, 18,000 conversions per second are allowed. The transfer of the new digital data to the output is initiated when EOC goes to the high voltage state.

POWER SUPPLIES

Standard supplies are V_{SS} = 5V, V_{GG} = −12V and V_{DD} = 0V. Device accuracy is dependent on stability of the reference voltage and has slight sensitivity to $V_{SS} - V_{GG}$. V_{DD} has no effect on accuracy. Noise spikes on the V_{SS} and V_{GG} supplies can cause improper conversion; therefore, filtering each supply with a 4.7 μF tantalum capacitor is recommended.

CONTINUOUS CONVERSIONS AND LOGIC CONTROL

Simply tying the EOC output to the Start Conversion input will allow continuous conversions, but an oscillation on this line will exist during the first 4 clock periods after EOC goes high. Adding a D flip-flop between EOC (D input) to Start Conversion (Q output) will prevent the oscillation and will allow a stop/continuous control via the "clear" input.

To prevent missing a start pulse which may occur after EOC goes high and prior to the required 4 clock period time interval, the circuit of *Figure 1* can be used. The RS latch can be set at any time and the 4-stage shift register delays the application of the start pulse to the A/D by 4 clock periods. The RS latch is reset 1 clock period after the A/D EOC signal goes to the low voltage state. This circuit also provides a Start Conversion pulse to the A/D which is 1 clock period wide.

A second control logic application circuit is shown in *Figure 2*. This allows an asynchronous start pulse of arbitrary length less than T_C, continuously converts for a fixed high level and provides a single clock period start pulse to the A/D. The binary counter is loaded with a count of 11 when the start pulse to the A/D appears. Counting is inhibited until the EOC signal from the A/D goes high. A carry pulse is then generated 4 clock periods after EOC goes high and is used to reset the input RS latch. This carry pulse can be used to indicate that the conversion is complete, the data has transferred to the output buffers and the system is ready for a new conversion cycle.

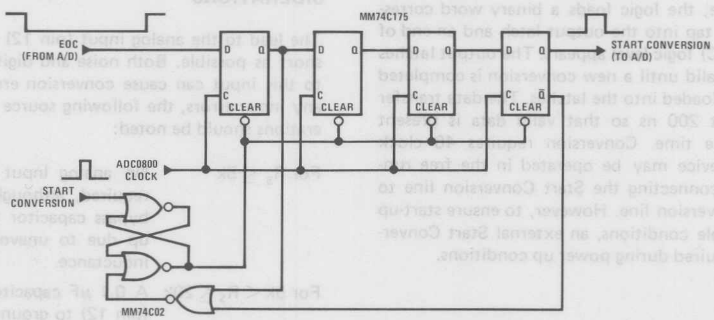


FIGURE 1. Delaying an Asynchronous Start Pulse

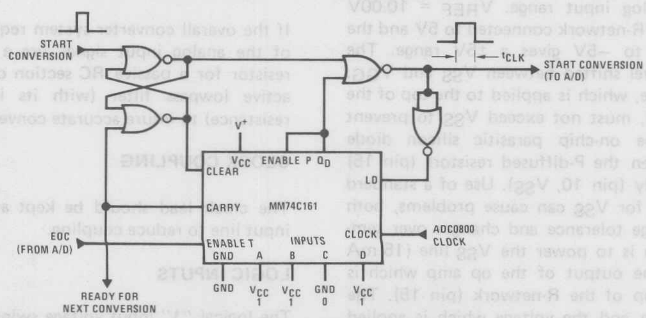


FIGURE 2. A/D Control Logic

Application Hints (Continued)

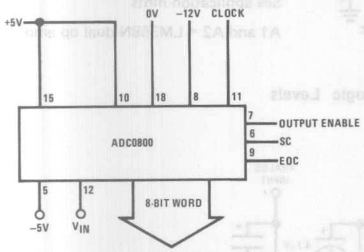
ZERO AND FULL-SCALE ADJUSTMENT

Zero Adjustment: This is the offset voltage required at the bottom of the R-network (pin 5) to make the 11111111 to 11111110 transition when the input voltage is 1/2 LSB (20 mV for a 10.24V scale). In most cases, this can be accomplished by having a 1 kΩ pot on pin 5. A resistor of 475Ω can be used as a non-adjustable best approximation from pin 5 to ground.

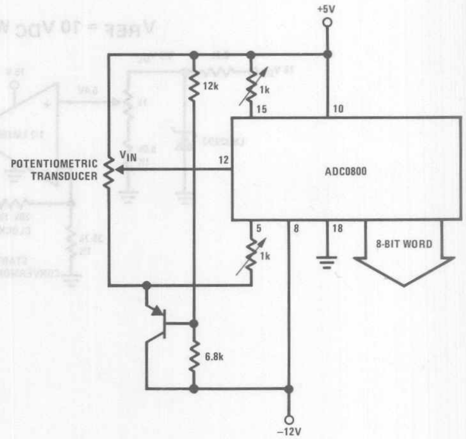
Full-Scale Adjustment: This is the offset voltage required at the top of the R-network (pin 15) to make the 00000001 to 00000000 transition when the input voltage is 1 1/2 LSB from full-scale (60 mV less than full-scale for a 10.24V scale). This voltage is guaranteed to be within 2 LSB for the ADC0800. In most cases, this can be accomplished by having a 1 kΩ pot on pin 15.

Typical Applications

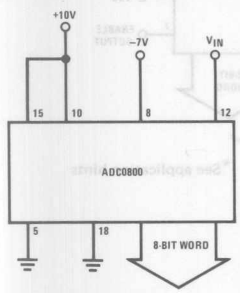
General Connection



Ratiometric Input Signal with Tracking Reference

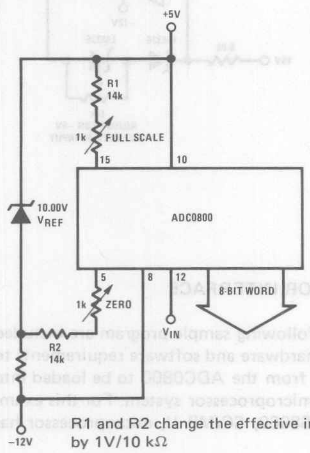


Hi-Voltage CMOS Output Levels



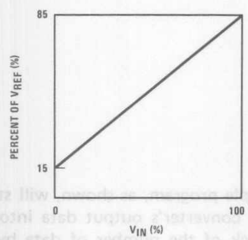
0V to 10V V_{IN} range
0V to 10V output levels

Level Shifted Zero and Full-Scale for Transducers



R1 and R2 change the effective input range by 1V/10 kΩ

Level Shifted Input Signal Range



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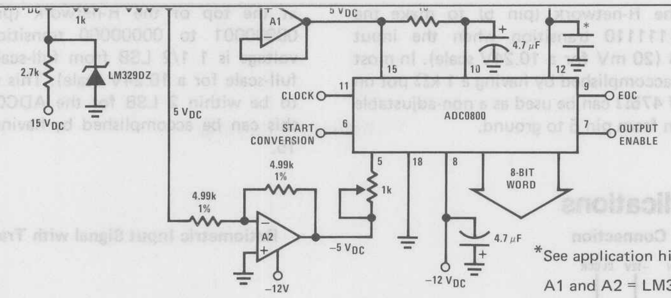
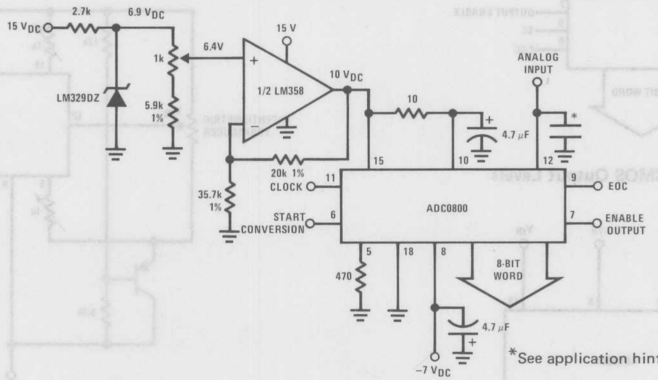


*See application hints

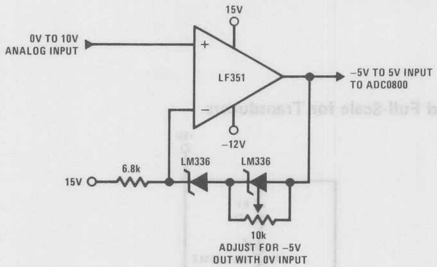
A1 and A2 = LM358N dual op amp

V_{REF} = 10 V_{DC} With 10V CMOS Logic Levels



*See application hints

Input Level Shifting



- Permits TTL compatible outputs with 0V to 10V input range (0V to −10V input range achieved by reversing polarity of zener diodes and returning the 6.8k resistor to V^{-}).

MICROPROCESSOR INTERFACE

Figure 3 and the following sample program are included to illustrate both hardware and software requirements to allow output data from the ADC0800 to be loaded into the memory of a microprocessor system. For this example, National's INS8060, SC/MP II, microprocessor has been used.

The sample program, as shown, will start the converter, load the converter's output data into the accumulator, keep track of the number of data bytes entered, complement the data and store this data into sequential memory locations. After 256 bytes have been entered, the control jumps to the user's program where proces-

Typical Applications (Continued)

sing of the data entered will be implemented. A more practical program whereby each data byte entered will be processed before another entry is made can easily be done by jumping back to the user's program at the end of the interrupt routine (where the data is loaded into the accumulator and stored in memory). The end of the user's program should provide a jump back to the INITIALIZE statement to start a new conversion and generate a new data entry.

The following arbitrarily chosen addresses and pointer assignments are used in this example:

Pointer 1 — WORD COUNT (ADDR:0100)
Also used to point to the A/D converter at address 0500 for this example when data is to be entered.

Pointer 2 — ENTERED DATA (ADDR's: 0200→ 02FF)
Data is stored in 2's complement binary form, i.e, 01111111 → +full-scale and 10000000 → – full-scale.

Pointer 3 — LOAD DATA SUBROUTINE (starts at ADDR:0300)
Executed when an EOC signal generates an interrupt request via sense A after an IEN (interrupt enable) instruction.

The address for the converter (0500) is unique for this particular sample program but may not be in a user's system so a different converter address must be used. Note that in *Figure 3* ADX and ADY for the address decode circuitry would be address bits ADB10 and ADB8 (pins 35 and 33 on the SC/MP II package) for converter address 0500.

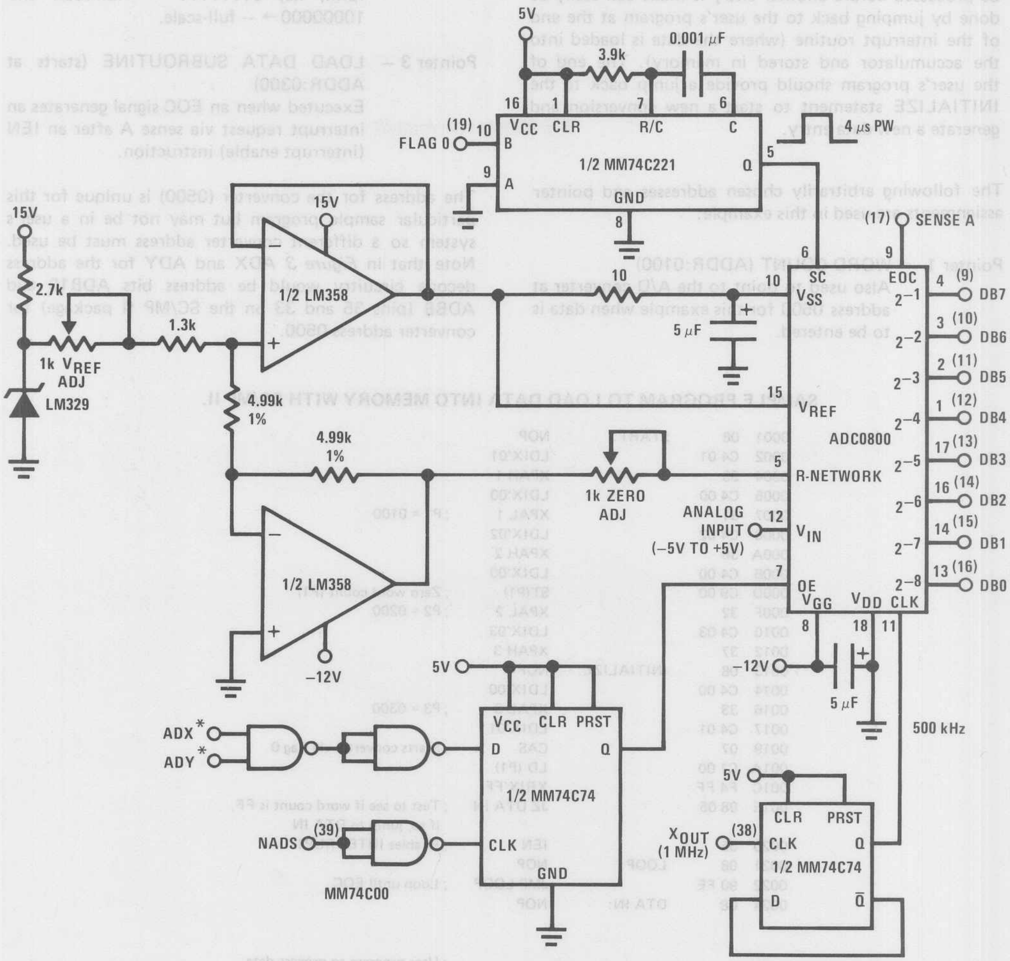
SAMPLE PROGRAM TO LOAD DATA INTO MEMORY WITH SC/MP II.

```
0001  08     START:        NOP
0002  C4 01                LDIX'01
0004  35                   XPAH 1
0005  C4 00                LDIX'00
0007  31                   XPAL 1      ; P1 = 0100
0008  C4 02                LDIX'02
000A  36                   XPAH 2
000B  C4 00                LDIX'00
000D  C9 00                ST(P1)      ; Zero word count (P1)
000F  32                   XPAL 2      ; P2 = 0200
0010  C4 03                LDIX'03
0012  37                   XPAH 3
0013  08     INITIALIZE:   NOP
0014  C4 00                LDIX'00
0016  33                   XPAL 3      ; P3 = 0300
0017  C4 01                LDIX'01
0019  07                   CAS         ; Starts converter via flag 0
001A  C1 00                LD (P1)
001C  F4 FF                XRIX'FF
001E  98 05                JZ DTA IN   ; Test to see if word count is FF,
                                         if so, jump to DTA IN
0020  05                   IEN         ; Enables INTERRUPT
0021  08     LOOP:         NOP
0022  90 FE                JMP LOOP    ; Loop until EOC
0024  08     DTA IN:       NOP
                           .
                           .
                           .           ; User program to process data
                           .
                           .

             :DATA ENTRY SUBROUTINE
0300  08     DATA IN SR:   NOP
0301  A9 00                ILD (P1)    ; Increment word count
0303  C4 05                LDIX'05
0305  35                   XPAH 1      ; P1 will point to converter
0306  C1 00                LD (P1)     ; Converter data loaded into
                                         accumulator
0308  F4 7F                XRIX'7F     ; Put data in 2's complement form
030A  CE 01                ST @ 1(P2)  ; Store data
030C  C4 00                LDIX'00
030E  07                   CAS         ; Resets flag 0
030F  C4 01                LDIX'01
0311  35                   XPAH 1      ; Resets P1 to point at word count
0312  C4 13                LDIX'13
0314  33                   XPAL 3
0315  3F                   XPPC 3      ; Return to INITIALIZE to start a
                                         new conversion
```

8

Typical Applications (Continued)



- Setting flag 0 (FLG0 = 1) with software, starts conversion (FLG0 must be cleared before another conversion can be initiated)
- With interrupt enabled an EOC will force an interrupt. Interrupt subroutine should load converter data into the accumulator.
- Output data is in complementary offset binary form
- Numbers in parentheses denote pin numbers of SC/MP chip

*ADX and ADY can be any of the address lines but they must be high *only* at the time the converter output data is to be put on the data bus (i.e., the converter must have its own unique address)

FIGURE 3. Interfacing to the SC/MP II Microprocessor

Typical Applications (Continued)

TESTING THE A/D CONVERTER

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LED's to display the resulting digital output code as shown in *Figure 4*. Note that the LED drivers invert the digital output of the A/D converter to provide a binary display. A lab DVM can be used if a precision voltage source is not available. After adjusting the zero and full-scale, any number of points can be checked, as desired.

For ease of testing, a 10.24 V_{DC} reference is recommended for the A/D converter. This provides an LSB of 40 mV (10.240/256). To adjust the zero of the A/D, an analog input voltage of 1/2 LSB or 20 mV should be applied and the zero adjust potentiometer should be set to provide a flicker on the LSB LED readout with all the other display LEDs OFF.

To adjust the full-scale adjust potentiometer, an analog input which is 1 1/2 LSB less than the reference (10.240–0.060 or 10.180 V_{DC}) should be applied to the analog input and the full-scale adjusted for a flicker on the LSB LED, but this time with all the other LEDs ON.

A complete circuit for a simple A/D tester is shown in *Figure 5*. Note that the clock input voltage swing and the digital output voltage swings are from 0V to 10.24V. The MM74C901 provides a voltage translation to 5V operation and also the logic inversion so the readout LEDs are in binary.

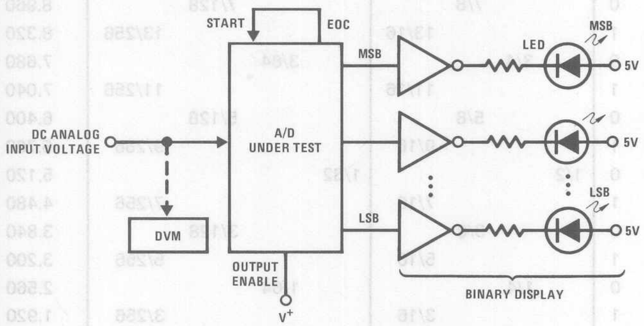


FIGURE 4. Basic A/D Tester

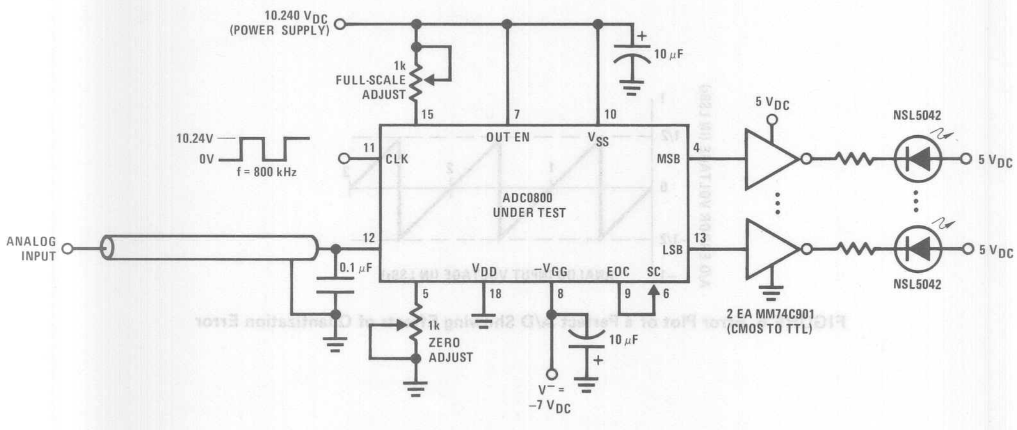


FIGURE 5. Complete Basic Tester Circuit

dividing the 8 bits into the 4 most significant bits and 4 least significant bits. Table I shows the fractional binary equivalent of these two 8-bit groups. By adding the decoded voltages which are obtained from the column: "Input Voltage Value with a 10.240 V_{REF}" of both the MS and LS groups, the value of the digital display can be determined. For example, for an output LED display of "1011 0110" or "B6" (in hex) the voltage values from the table are 7.04 + 0.24 or

values of a perfect A/D converter. The input voltage has to change by ±1/2 LSB (±20 mV), the "quantization uncertainty" of an A/D, to obtain an output digital code change. The effects of this quantization error have to be accounted for in the interpretation of the test results. A plot of this natural error source is shown in *Figure 6* where, for clarity, both the analog input voltage and the error voltage are normalized to LSBs.

TABLE I. DECODING THE DIGITAL OUTPUT LEDs

HEX	BINARY	FRACTIONAL BINARY VALUE FOR		INPUT VOLTAGE VALUE WITH 10.24 V_{REF}	
		MS GROUP	LS GROUP	MS GROUP	LS GROUP
F	1 1 1 1	15/16	15/256	9.600	0.600
E	1 1 1 0	7/8	7/128	8.960	0.560
D	1 1 0 1	13/16	13/256	8.320	0.520
C	1 1 0 0	3/4	3/64	7.680	0.480
B	1 0 1 1	11/16	11/256	7.040	0.440
A	1 0 1 0	5/8	5/128	6.400	0.400
9	1 0 0 1	9/16	9/256	5.760	0.360
8	1 0 0 0	1/2	1/32	5.120	0.320
7	0 1 1 1	7/16	7/256	4.480	0.280
6	0 1 1 0	3/8	3/128	3.840	0.240
5	0 1 0 1	5/16	5/256	3.200	0.200
4	0 1 0 0	1/4	1/64	2.560	0.160
3	0 0 1 1	3/16	3/256	1.920	0.120
2	0 0 1 0	1/8	1/128	1.280	0.080
1	0 0 0 1	1/16	1/256	0.640	0.040
0	0 0 0 0			0	0

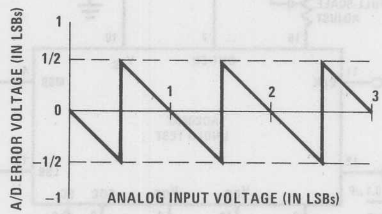


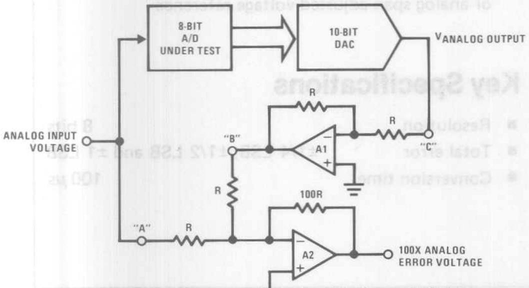
FIGURE 6. Error Plot of a Perfect A/D Showing Effects of Quantization Error

the analog input voltage and the LED outputs will provide a binary counting sequence from zero to full-scale.

The techniques described so far are suitable for an engineering evaluation or a quick check on performance. For a higher speed test system, or to obtain plotted data, a digital-to-analog converter is needed for the test set-up. An accurate 10-bit DAC can serve as the precision voltage source for the A/D. Errors of the A/D under test can be provided as either analog voltages or differences in two digital words.

A basic A/D tester which uses a DAC and provides the error as an analog output voltage is shown in *Figure 7*. The 2 op amps can be eliminated if a lab DVM with a numerical subtraction feature is available to directly readout the difference voltage, "A–C". The analog generator and an X-Y plotter can be used to provide analog error (Y axis) versus analog input (X axis). The construction details of a tester of this type are provided in the NSC application note AN-179, "Analog-to-Digital Converter Testing".

For operation with a microprocessor or a computer-based test system, it is more convenient to present the errors digitally. This can be done with the circuit of *Figure 8* where the output code transitions can be detected as the 10-bit DAC is incremented. This provides 1/4 LSB steps for the 8-bit A/D under test. If the results of this test are automatically plotted with the analog input on the X axis and the error (in LSB's) as the Y axis, a useful transfer function of the A/D under test results. For acceptance testing, the plot is not necessary and the testing speed can be increased by establishing internal limits on the allowed error for each code.



All R's = 0.05% tolerance

FIGURE 7. A/D Tester with Analog Error Output

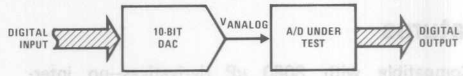
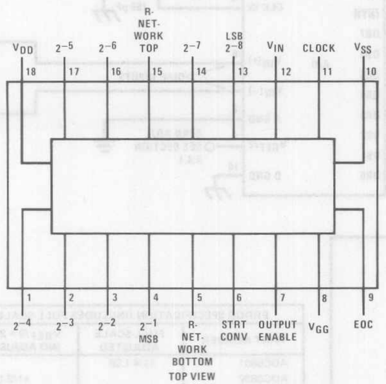


FIGURE 8. Basic "Digital" A/D Tester

Connection Diagram

Dual-In-Line Package



Order Number ADC0800PD (–55°C to +125°C)
or ADC0800PCD (0°C to +70°C)
See NS Package D18A

National Semiconductor

ADC0801, ADC0802, ADC0803, ADC0804, ADC0805 8-Bit µP Compatible A/D Converters

General Description

The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters which use a differential potentiometric ladder—similar to the 256R products. These converters are designed to allow operation with the NSC800 and INS8080A derivative control bus, and TRI-STATE® output latches directly drive the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

A new differential analog voltage input allows increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

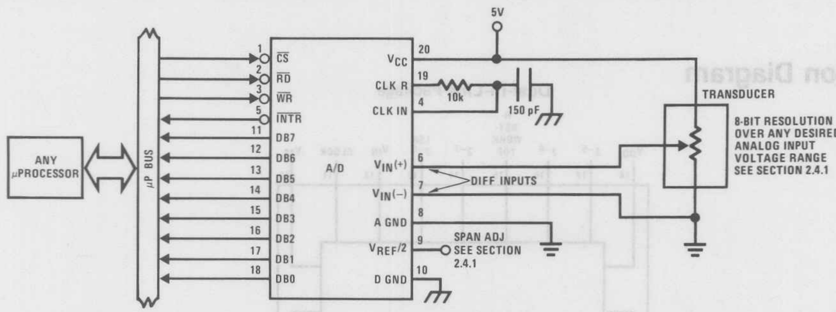
Features

- Compatible with 8080 µP derivatives—no interfacing logic needed — access time — 135 ns
- Easy interface to all microprocessors, or operates "stand alone"
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and T^2L voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3" standard width 20-pin DIP package
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference

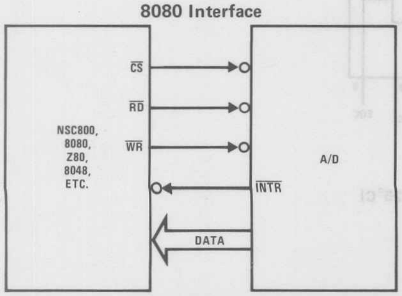
Key Specifications

- Resolution 8 bits
- Total error ±1/4 LSB, ±1/2 LSB and ±1 LSB
- Conversion time 100 µs

Typical Applications



8080 Interface



ERROR SPECIFICATION (INCLUDES FULL-SCALE, ZERO ERROR, AND NON-LINEARITY)			
PART NUMBER	FULL-SCALE ADJUSTED	$V_{REF}/2$ = 2.500 V_{DC} (NO ADJUSTMENTS)	$V_{REF}/2$ = NO CONNECTION (NO ADJUSTMENTS)
ADC0801	±1/4 LSB		
ADC0802		±1/2 LSB	
ADC0803	±1/2 LSB		
ADC0804		±1 LSB	
ADC0805			±1 LSB

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage	
Logic Control Inputs	−0.3V to +18V
At Other Input and Outputs	−0.3V to (V_{CC} + 0.3V)
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A = 25°C	875 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Ratings (Notes 1 and 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0801/02LD	$-55°C \le T_A \le +125°C$
ADC0801/02/03/04LCD	$-40°C \le T_A \le +85°C$
ADC0801/02/03/05LCN	$-40°C \le T_A \le +85°C$
ADC0804LCN	$0°C \le T_A \le +70°C$
Range of V_{CC}	4.5 V_{DC} to 6.3 V_{DC}

Electrical Characteristics

The following specifications apply for V_{CC} = 5 V_{DC}, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK} = 640 kHz unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ADC0801: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±1/4	LSB
ADC0802: Total Unadjusted Error (Note 8)	$V_{REF}/2$ = 2.500 V_{DC}			±1/2	LSB
ADC0803: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±1/2	LSB
ADC0804: Total Unadjusted Error (Note 8)	$V_{REF}/2$ = 2.500 V_{DC}			±1	LSB
ADC0805: Total Unadjusted Error (Note 8)	$V_{REF}/2$—No Connection			±1	LSB
$V_{REF}/2$ Input Resistance (Pin 9)	ADC0801/02/03/05	2.5	8.0		kΩ
	ADC0804 (Note 9)	1.0	1.3		kΩ
Analog Input Voltage Range	(Note 4) V(+) or V(−)	Gnd−0.05		V_{CC}+0.05	V_{DC}
DC Common-Mode Error	Over Analog Input Voltage Range		±1/16	±1/8	LSB
Power Supply Sensitivity	V_{CC} = 5 V_{DC} ±10% Over Allowed $V_{IN}(+)$ and $V_{IN}(-)$ Voltage Range (Note 4)		±1/16	±1/8	LSB

AC Electrical Characteristics

The following specifications apply for V_{CC} = 5 V_{DC} and T_A = 25°C unless otherwise specified.

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
T_c	Conversion Time	f_{CLK} = 640 kHz (Note 6)	103		114	µs
T_c	Conversion Time	(Note 5, 6)	66		73	$1/f_{CLK}$
f_{CLK}	Clock Frequency	V_{CC} = 5V, (Note 5)	100	640	1460	kHz
	Clock Duty Cycle	(Note 5)	40		60	%
CR	Conversion Rate In Free-Running Mode	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$ = 0 V_{DC}, f_{CLK} = 640 kHz			8770	conv/s
$t_{W(\overline{WR})L}$	Width of $\overline{WR}$ Input (Start Pulse Width)	$\overline{CS}$ = 0 V_{DC} (Note 7)	100			ns
t_{ACC}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	C_L = 100 pF		135	200	ns
t_{1H}, t_{0H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	C_L = 10 pF, R_L = 10k (See TRI-STATE Test Circuits)		125	200	ns
t_{WI}, t_{RI}	Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$			300	450	ns
C_{IN}	Input Capacitance of Logic Control Inputs			5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance (Data Buffers)			5	7.5	pF

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CONTROL INPUTS [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]						
V_{IN} (1)	Logical "1" Input Voltage (Except Pin 4 CLK IN)	$V_{CC} = 5.25\ V_{DC}$	2.0		15	V_{DC}
V_{IN} (0)	Logical "0" Input Voltage (Except Pin 4 CLK IN)	$V_{CC} = 4.75\ V_{DC}$			0.8	V_{DC}
I_{IN} (1)	Logical "1" Input Current (All Inputs)	$V_{IN} = 5\ V_{DC}$		0.005	1	μA_{DC}
I_{IN} (0)	Logical "0" Input Current (All Inputs)	$V_{IN} = 0\ V_{DC}$	−1	−0.005		μA_{DC}
CLOCK IN AND CLOCK R						
V_{T+}	CLK IN (Pin 4) Positive Going Threshold Voltage		2.7	3.1	3.5	V_{DC}
V_{T-}	CLK IN (Pin 4) Negative Going Threshold Voltage		1.5	1.8	2.1	V_{DC}
V_H	CLK IN (Pin 4) Hysteresis $(V_{T+}) - (V_{T-})$		0.6	1.3	2.0	V_{DC}
V_{OUT} (0)	Logical "0" CLK R Output Voltage	$I_O = 360\ \mu A$ $V_{CC} = 4.75\ V_{DC}$			0.4	V_{DC}
V_{OUT} (1)	Logical "1" CLK R Output Voltage	$I_O = -360\ \mu A$ $V_{CC} = 4.75\ V_{DC}$	2.4			V_{DC}
DATA OUTPUTS AND $\overline{INTR}$						
$V_{OUT}(0)$	Logical "0" Output Voltage					
	Data Outputs	$I_{OUT} = 1.6$ mA, $V_{CC} = 4.75\ V_{DC}$			0.4	V_{DC}
	$\overline{INTR}$ Output	$I_{OUT} = 1.0$ mA, $V_{CC} = 4.75\ V_{DC}$			0.4	V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	$I_O = -360\mu A$, $V_{CC} = 4.75\ V_{DC}$	2.4			V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	$I_O = -10\ \mu A$, $V_{CC} = 4.75\ V_{DC}$	4.5			V_{DC}
I_{OUT}	TRI-STATE Disabled Output Leakage (All Data Buffers)	$V_{OUT} = 0\ V_{DC}$	−3			μA_{DC}
		$V_{OUT} = 5\ V_{DC}$			3	μA_{DC}
I_{SOURCE}		V_{OUT} Short to Gnd, $T_A = 25°C$	4.5	6		mA_{DC}
I_{SINK}		V_{OUT} Short to V_{CC}, $T_A = 25°C$	9.0	16		mA_{DC}
POWER SUPPLY						
I_{CC}	Supply Current (Includes Ladder Current)	$f_{CLK} = 640$ kHz, $V_{REF}/2$ = NC, $T_A = 25°C$ and $\overline{CS}$ = "1"				
		ADC0801/02/03/05		1.1	1.8	mA
		ADC0804 (Note 9)		1.9	2.5	mA

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltages are measured with respect to Gnd, unless otherwise specified. The separate A Gnd point should always be wired to the D Gnd.

Note 3: A zener diode exists, internally, from V_{CC} to Gnd and has a typical breakdown voltage of 7 V_{DC}.

Note 4: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see block diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Accuracy is guaranteed at f_{CLK} = 640 kHz. At higher clock frequencies accuracy can degrade. For lower clock frequencies, the duty cycle limits can be extended so long as the minimum clock high time interval or minimum clock low time interval is no less than 275 ns.

Note 6: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The start request is internally latched, see *Figure 2* and section 2.0.

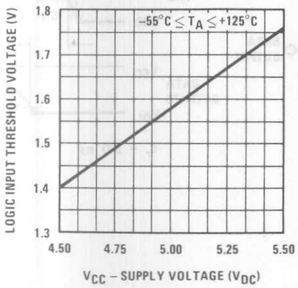
Note 7: The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input and therefore timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see timing diagrams).

Note 8: None of these A/Ds requires a zero adjust (see section 2.5.1). To obtain zero code at other analog input voltages see section 2.5 and *Figure 5*.

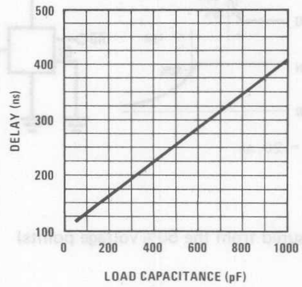
Note 9: For ADC0804LCD typical value of $V_{REF}/2$ input resistance is 8 kΩ and of I_{CC} is 1.1 mA.

Typical Performance Characteristics

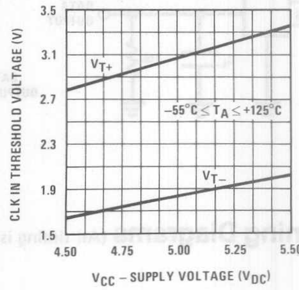
Logic Input Threshold Voltage vs. Supply Voltage



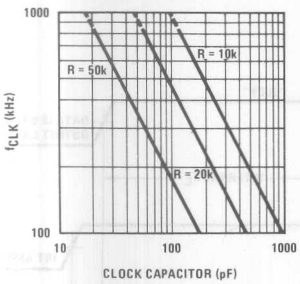
Delay From Falling Edge of RD to Output Data Valid vs. Load Capacitance



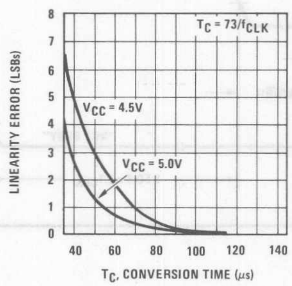
CLK IN Schmitt Trip Levels vs. Supply Voltage



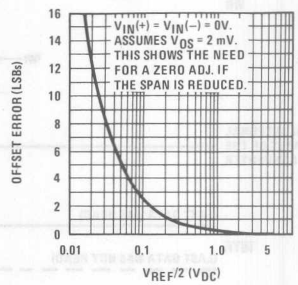
f_{CLK} vs. Clock Capacitor



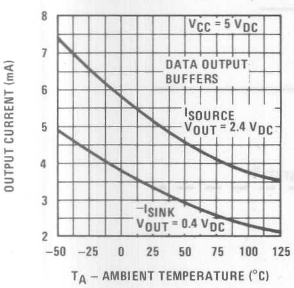
Full-Scale Error vs Conversion Time



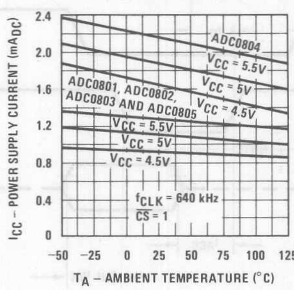
Effect of Unadjusted Offset Error vs. $V_{REF}/2$ Voltage



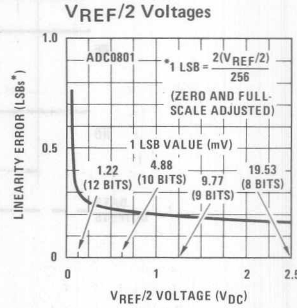
Output Current vs Temperature



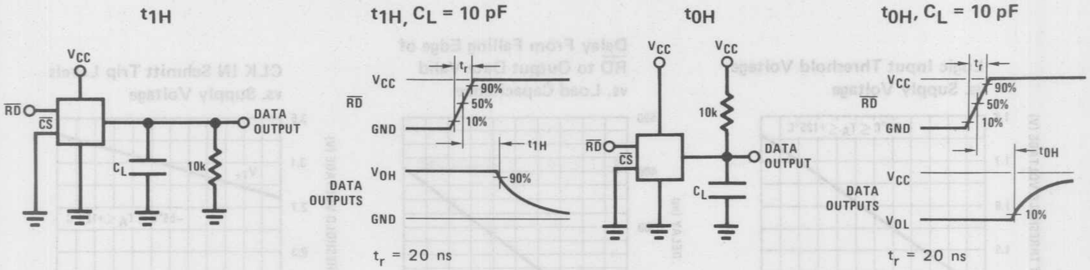
Power Supply Current vs Temperature (Note 9)



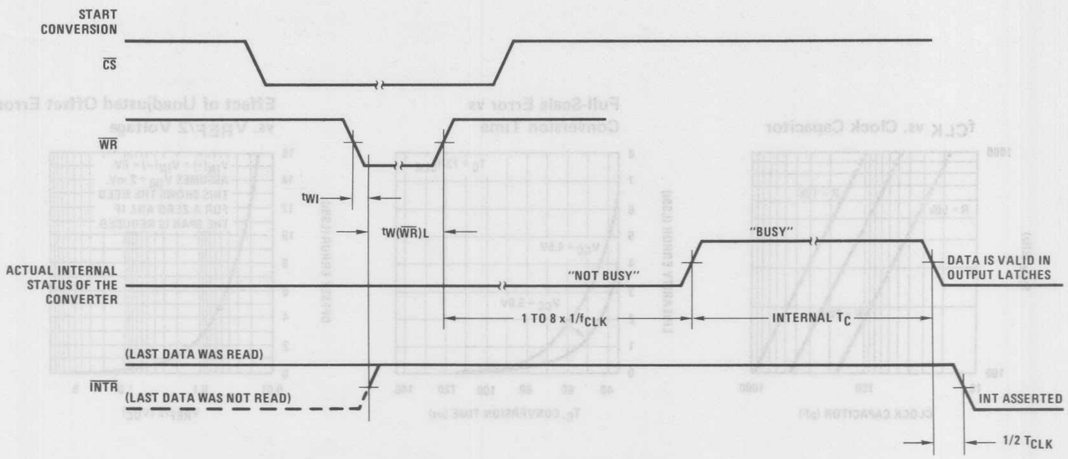
Linearity Error at Low $V_{REF}/2$ Voltages



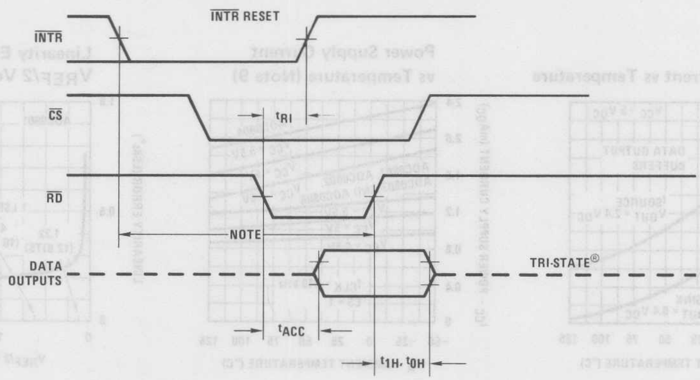
TRI-STATE® Test Circuits and Waveforms



Timing Diagrams (All timing is measured from the 50% voltage points)



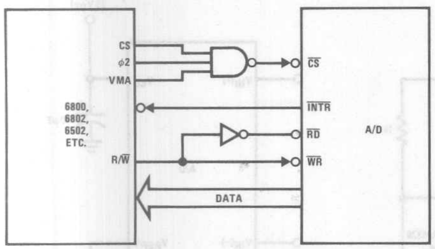
Output Enable and Reset $\overline{INTR}$



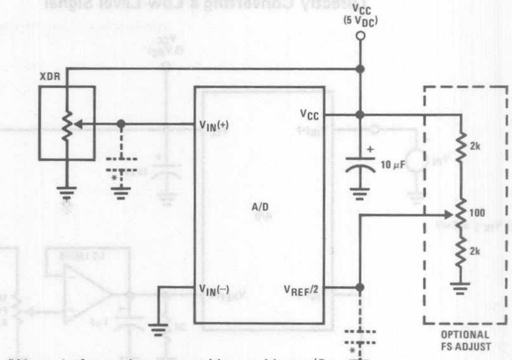
Note: Read strobe must occur 8 clock periods ($8/f_{CLK}$) after assertion of interrupt to guarantee reset of $\overline{INTR}$.

Typical Applications (Continued)

6800 Interface

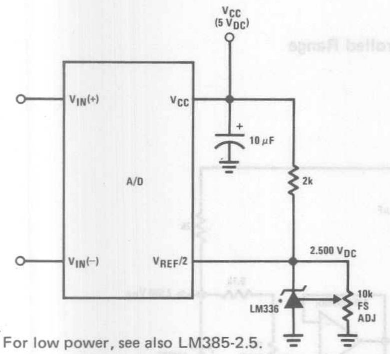


Ratiometric with Full-Scale Adjust



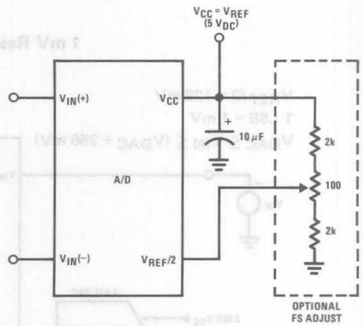
*Note: before using caps at V_{IN} or $V_{REF}/2$, see section 2.3.2 Input Bypass Capacitors.

Absolute with a 2.500V Reference

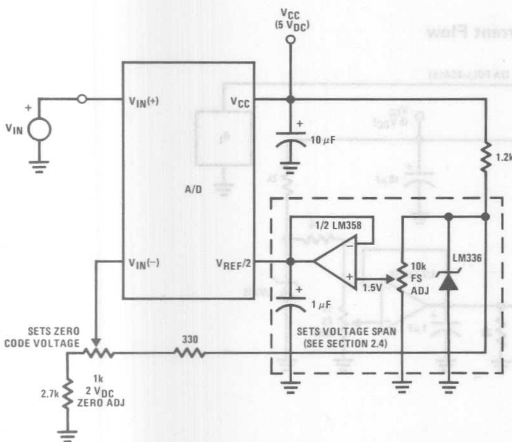


*For low power, see also LM385-2.5.

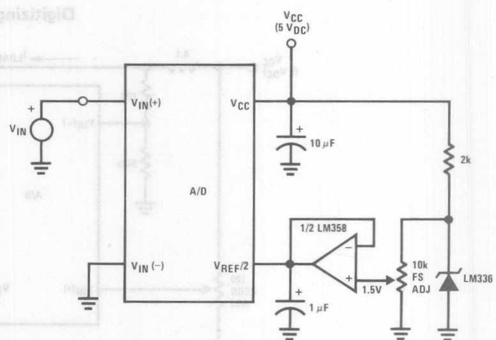
Absolute with a 5V Reference

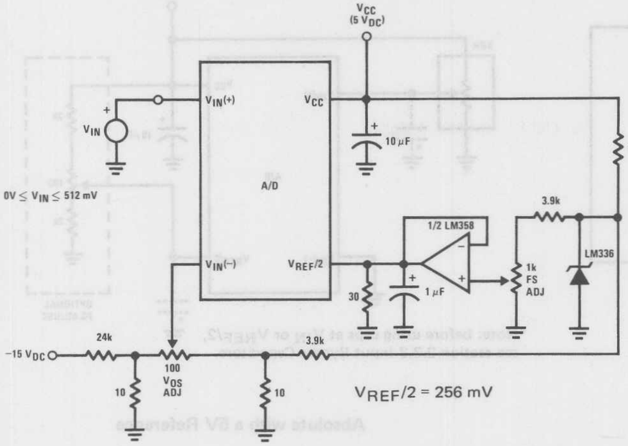


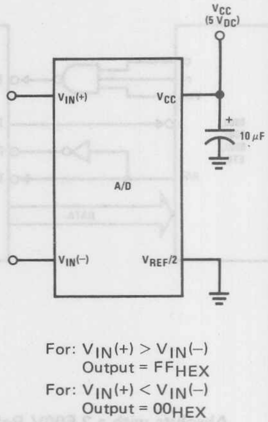
Zero-Shift and Span Adjust: 2V ≤ V_{IN} ≤ 5V



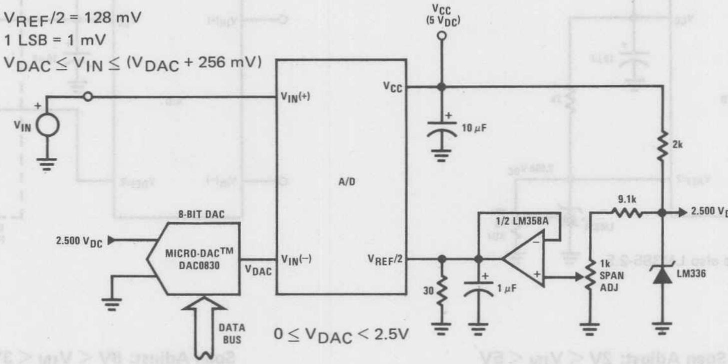
Span Adjust: 0V ≤ V_{IN} ≤ 3V



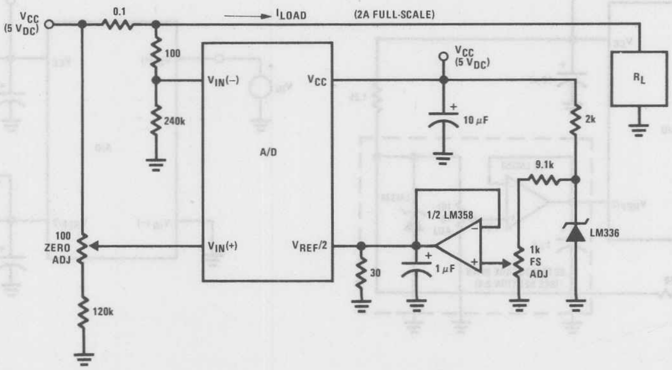




1 mV Resolution with µP Controlled Range

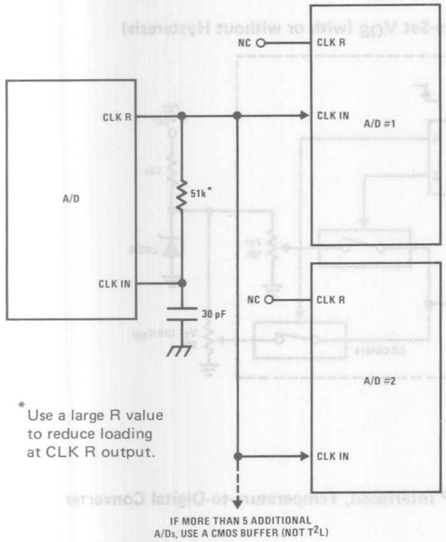


Digitizing a Current Flow



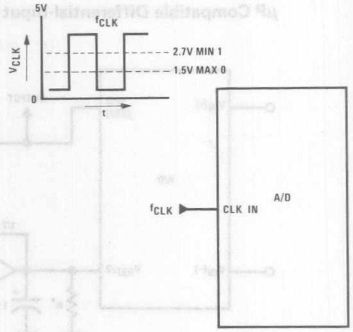
Typical Applications (Continued)

Self-Clocking Multiple A/Ds



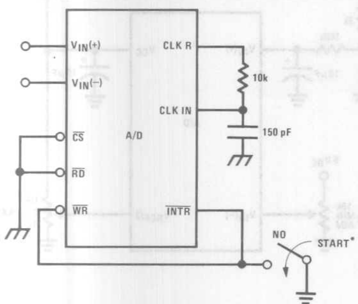
*Use a large R value to reduce loading at CLK R output.

External Clocking



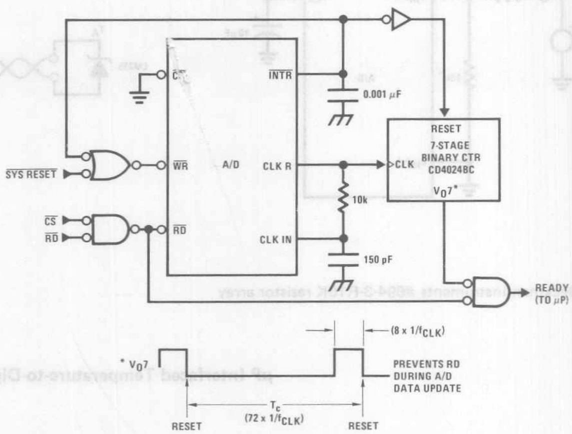
100 kHz $\leq f_{CLK} \leq$ 1460 kHz

Self-Clocking in Free-Running Mode

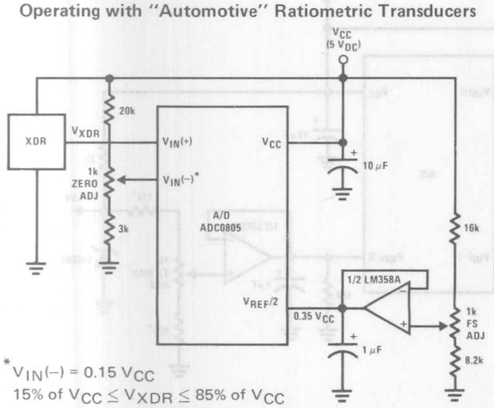


*After power-up, a momentary grounding of the WR input is needed to guarantee operation.

μP Interface for Free-Running A/D

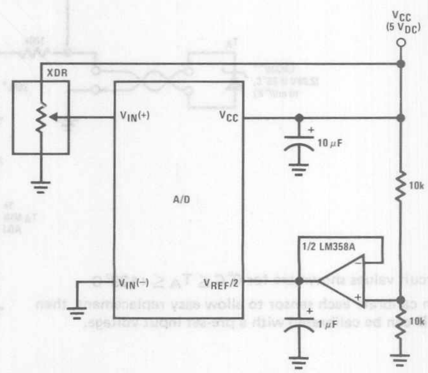


Operating with "Automotive" Ratiometric Transducers



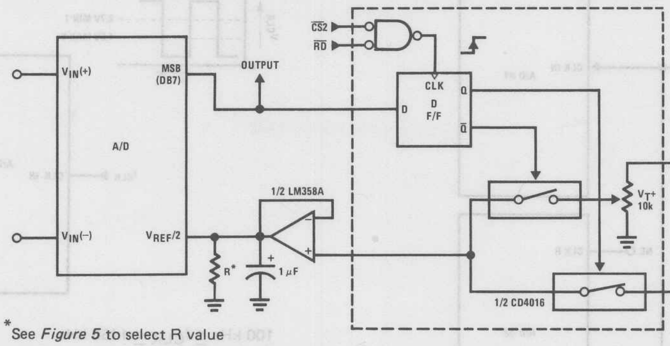
*$V_{IN}(-) = 0.15\ V_{CC}$
15% of $V_{CC} \leq V_{XDR} \leq$ 85% of V_{CC}

Ratiometric with $V_{REF}/2$ Forced



Typical Applications (Continued)

µP Compatible Differential-Input Comparator with Pre-Set V_{OS} (with or without Hysteresis)

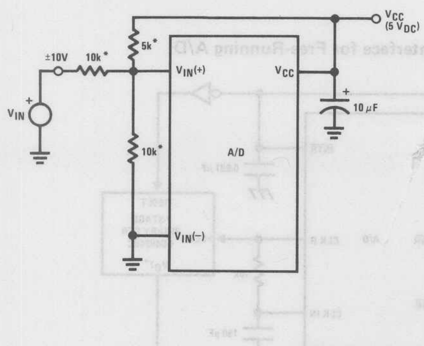


*See *Figure 5* to select R value

DB7 = "1" for $V_{IN}(+) > V_{IN}(-) + (V_{REF}/2)$

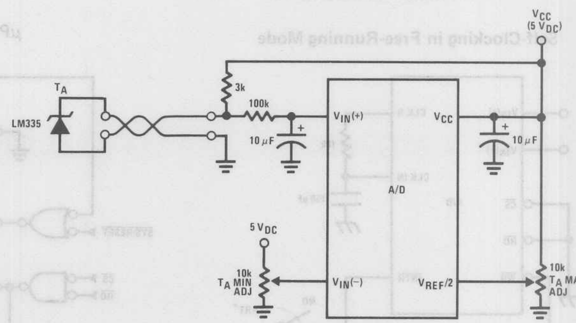
Omit circuitry within the dotted area if hysteresis is not needed

Handling ±10V Analog Inputs

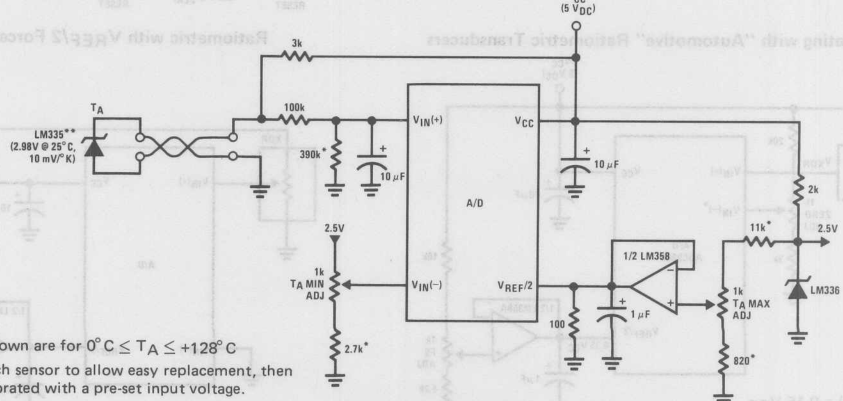


*Beckman Instruments #694-3-R10K resistor array

Low-Cost, µP Interfaced, Temperature-to-Digital Converter



µP Interfaced Temperature-to-Digital Converter

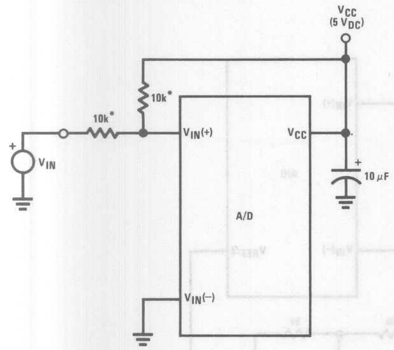


*Circuit values shown are for $0^{\circ}C \leq T_A \leq +128^{\circ}C$

**Can calibrate each sensor to allow easy replacement, then A/D can be calibrated with a pre-set input voltage.

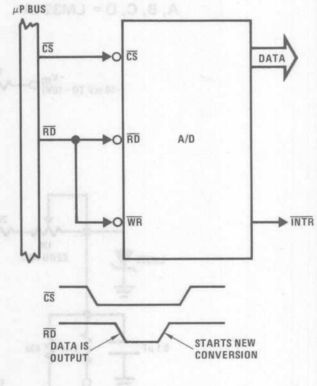
Typical Applications (Continued)

Handling ±5V Analog Inputs

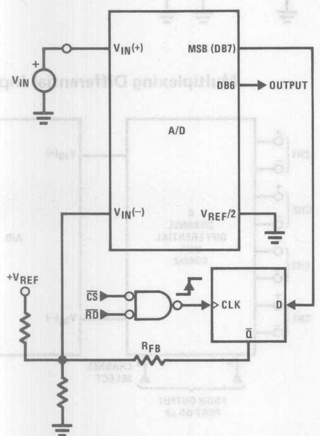


*Beckman Instruments #694-3-R10K resistor array

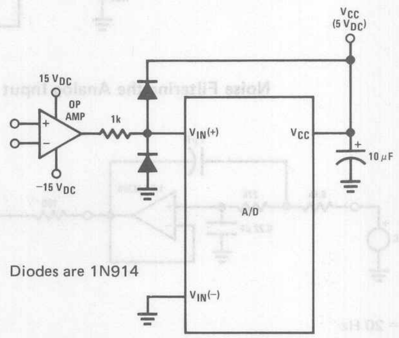
Read-Only Interface



µP Interfaced Comparator with Hysteresis

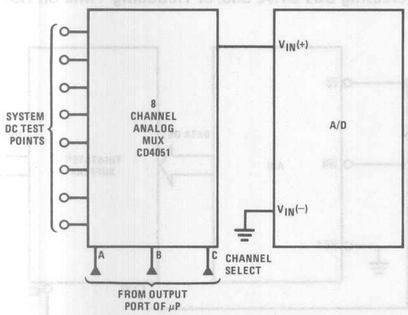


Protecting the Input

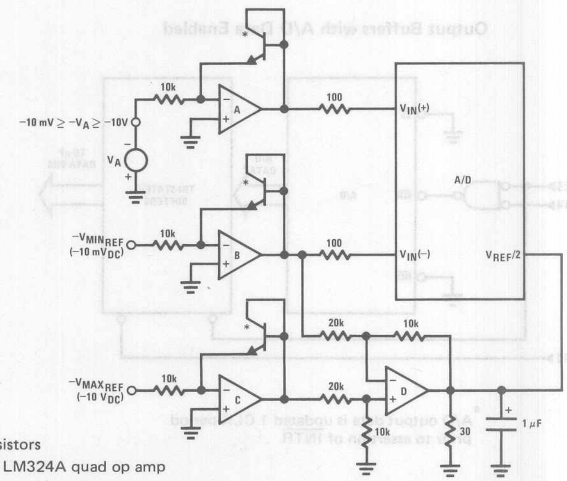


Diodes are 1N914

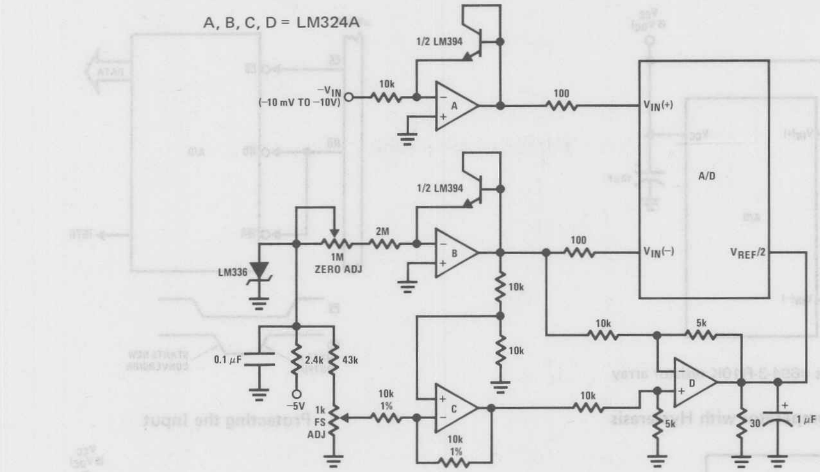
Analog Self-Test for a System



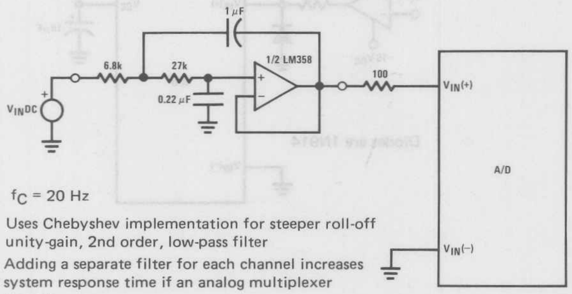
A Low-Cost, 3-Decade Logarithmic Converter



*LM389 transistors
A, B, C, D = LM324A quad op amp



Noise Filtering the Analog Input

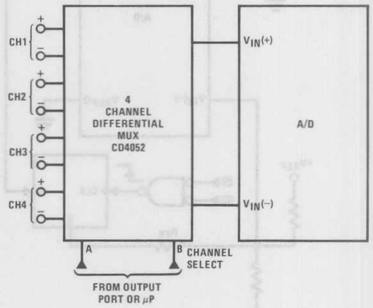


$f_C = 20$ Hz

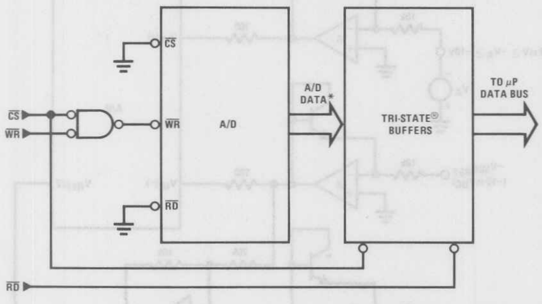
Uses Chebyshev implementation for steeper roll-off unity-gain, 2nd order, low-pass filter

Adding a separate filter for each channel increases system response time if an analog multiplexer is used

Multiplexing Differential Inputs

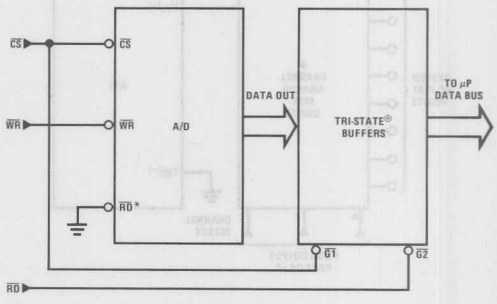


Output Buffers with A/D Data Enabled



*A/D output data is updated 1 CLK period prior to assertion of $\overline{\text{INTR}}$

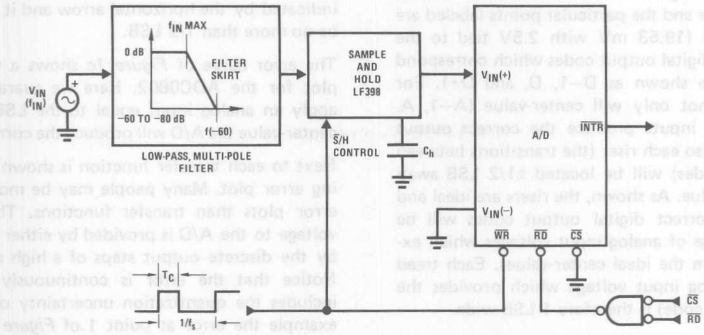
Increasing Bus Drive and/or Reducing Time on Bus



*Allows output data to set-up at falling edge of $\overline{\text{CS}}$

Typical Applications (Continued)

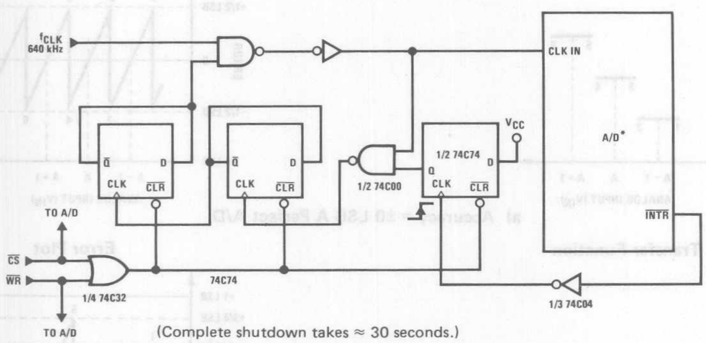
Sampling an AC Input Signal



Note 1: Oversample whenever possible [keep fs > 2f(−60)] to eliminate input frequency folding (aliasing) and to allow for the skirt response of the filter.

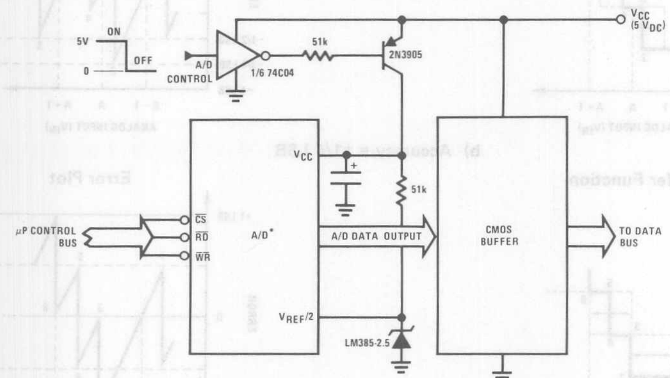
Note 2: Consider the amplitude errors which are introduced within the passband of the filter.

70% Power Savings by Clock Gating



(Complete shutdown takes ≈ 30 seconds.)

Power Savings by A/D and V_{REF} Shutdown



*Use ADC0801, 02, 03 or 05 for lowest power consumption.

Note: Logic inputs can be driven to V_{CC} with A/D supply at zero volts.

Buffer prevents data bus from overdriving outputs of A/D when in shutdown mode.

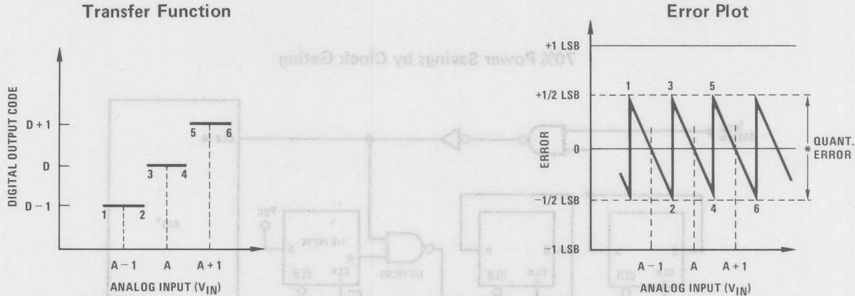
1.0 UNDERSTANDING A/D ERROR SPECS

A perfect A/D transfer characteristic (staircase waveform) is shown in *Figure 1a.* The horizontal scale is analog input voltage and the particular points labeled are in steps of 1 LSB (19.53 mV with 2.5V tied to the $V_{REF}/2$ pin). The digital output codes which correspond to these inputs are shown as D−1, D, and D+1. For the perfect A/D, not only will center-value (A−1, A, A+1, . . .) analog inputs produce the correct output digital codes, but also each riser (the transitions between adjacent output codes) will be located ±1/2 LSB away from each center-value. As shown, the risers are ideal and have no width. Correct digital output codes will be provided for a range of analog input voltages which extend ±1/2 LSB from the ideal center-values. Each tread (the range of analog input voltage which provides the same digital output code) is therefore 1 LSB wide.

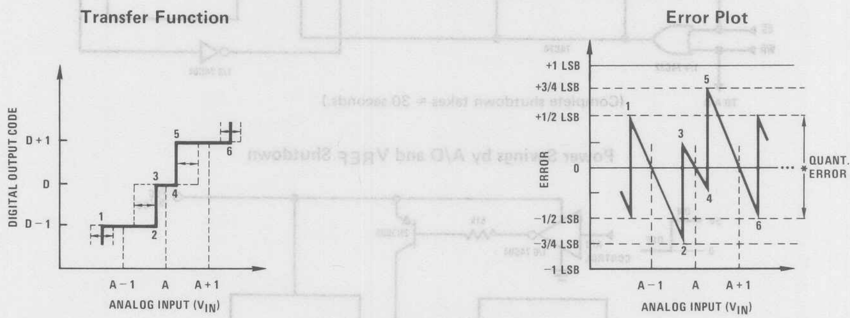
Figure 1b shows a worst case error plot for the ADC0801. All center-valued inputs are guaranteed to produce the correct output codes and the adjacent risers are guaranteed to be no closer to the center-value points than ±1/4 LSB. In other words, if we apply an analog input equal to the center-value ±1/4 LSB, *we guarantee* that the A/D will produce the correct digital code. The maximum range of the position of the code transition is indicated by the horizontal arrow and it is guaranteed to be no more than 1/2 LSB.

The error curve of *Figure 1c* shows a worst case error plot for the ADC0802. Here we guarantee that if we apply an analog input equal to the LSB analog voltage center-value the A/D will produce the correct digital code.

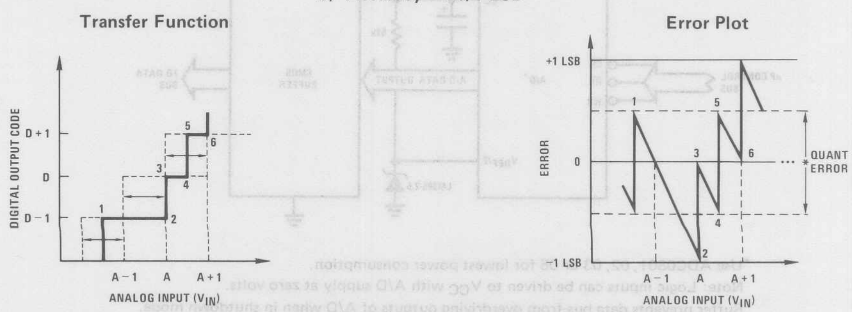
Next to each transfer function is shown the corresponding error plot. Many people may be more familiar with error plots than transfer functions. The analog input voltage to the A/D is provided by either a linear ramp or by the discrete output steps of a high resolution DAC. Notice that the error is continuously displayed and includes the quantization uncertainty of the A/D. For example the error at point 1 of *Figure 1a* is +1/2 LSB because the digital code appeared 1/2 LSB in advance of the center-value of the tread. The error plots always have a constant negative slope and the abrupt upside steps are always 1 LSB in magnitude.



a) Accuracy = ±0 LSB A Perfect A/D



b) Accuracy = ±1/4 LSB



c) Accuracy = ±1/2 LSB

FIGURE 1. Clarifying the Error Specs of an A/D Converter

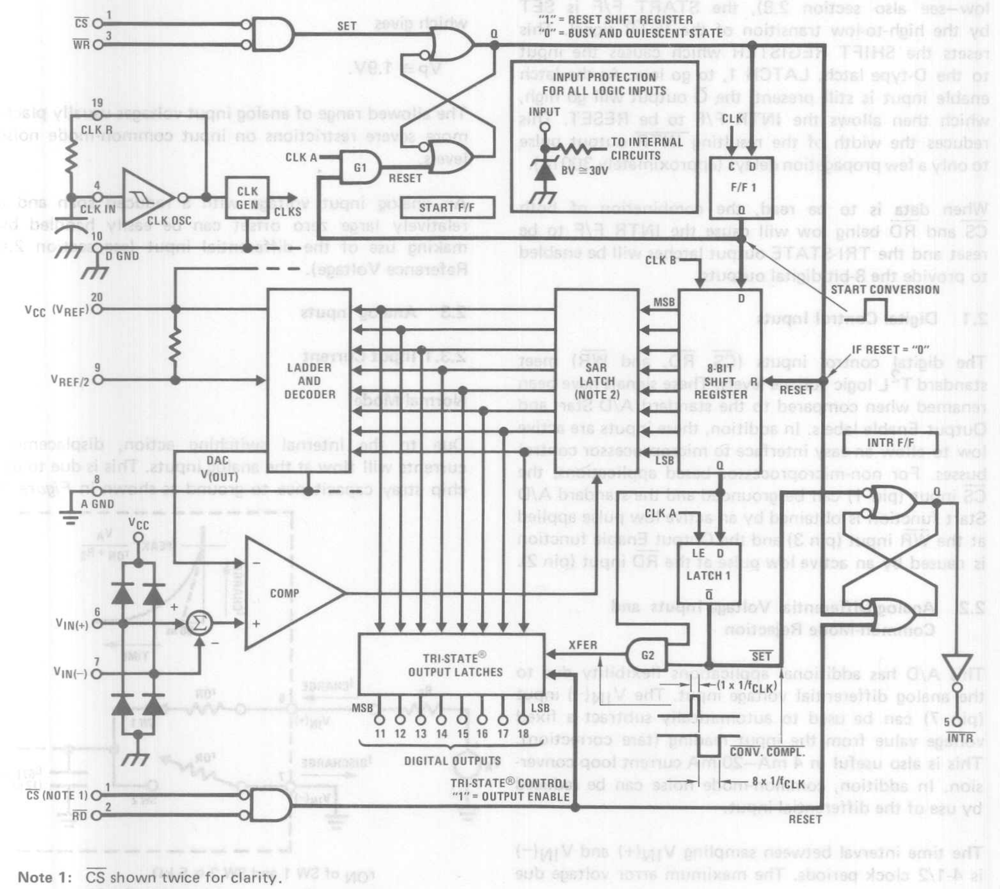
2.0 FUNCTIONAL DESCRIPTION

The ADC0801 series contains a circuit equivalent of the 256R network. Analog switches are sequenced by successive approximation logic to match the analog difference input voltage [$V_{IN}(+) - V_{IN}(-)$] to a corresponding tap on the R network. The most significant bit is tested first and after 8 comparisons (64 clock cycles) a digital 8-bit binary code (1111 1111 = full-scale) is transferred to an output latch and then an interrupt is asserted ($\overline{INTR}$ makes a high-to-low transition). A conversion in process can be interrupted by issuing a second start command. The device may be operated in the free-running mode by connecting $\overline{INTR}$ to the $\overline{WR}$ input with $\overline{CS}$ = 0. To insure start-up under all possible conditions, an external $\overline{WR}$ pulse is required during the first power-up cycle.

On the high-to-low transition of the $\overline{WR}$ input the internal SAR latches and the shift register stages are reset. As long as the $\overline{CS}$ input and $\overline{WR}$ input remain low, the A/D will remain in a reset state. *Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition.*

A functional diagram of the A/D converter is shown in *Figure 2*. All of the package pinouts are shown and the major logic control paths are drawn in heavier weight lines.

The converter is started by having $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register, resets the Interrupt (INTR) F/F and inputs a "1" to the D flop, F/F1, which is at the input end of the 8-bit shift register. Internal clock signals then transfer this "1" to the Q output of F/F1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a "1") the start F/F is reset and the 8-bit shift register then can have the "1" clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect (both outputs of the start F/F would momentarily be at a "1" level) and the 8-bit shift register would continue to be held in the reset mode. This logic therefore allows for wide $\overline{CS}$ and $\overline{WR}$ signals and the converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start F/F.



Note 1: $\overline{CS}$ shown twice for clarity.

Note 2: SAR = Successive Approximation Register.

FIGURE 2. Block Diagram

TRI-STATE output latches. When LATCH 1 is subsequently enabled, the Q output makes a high-to-low transition which causes the INTR F/F to set. An inverting buffer then supplies the $\overline{\text{INTR}}$ output signal.

Note that this $\overline{\text{SET}}$ control of the INTR F/F remains low for 8 of the external clock periods (as the internal clocks run at 1/8 of the frequency of the external clock). If the data output is continuously enabled ($\overline{\text{CS}}$ and $\overline{\text{RD}}$ both held low), the $\overline{\text{INTR}}$ output will still signal the end of conversion (by a high-to-low transition), because the $\overline{\text{SET}}$ input can control the Q output of the INTR F/F even though the RESET input is constantly at a "1" level in this operating mode. This $\overline{\text{INTR}}$ output will therefore stay low for the duration of the $\overline{\text{SET}}$ signal, which is 8 periods of the external clock frequency (assuming the A/D is not started during this interval).

When operating in the free-running or continuous conversion mode ($\overline{\text{INTR}}$ pin tied to $\overline{\text{WR}}$ and $\overline{\text{CS}}$ wired low—see also section 2.8), the START F/F is SET by the high-to-low transition of the $\overline{\text{INTR}}$ signal. This resets the SHIFT REGISTER which causes the input to the D-type latch, LATCH 1, to go low. As the latch enable input is still present, the $\overline{\text{Q}}$ output will go high, which then allows the INTR F/F to be RESET. This reduces the width of the resulting $\overline{\text{INTR}}$ output pulse to only a few propagation delays (approximately 300 ns).

When data is to be read, the combination of both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ being low will cause the INTR F/F to be reset and the TRI-STATE output latches will be enabled to provide the 8-bit digital outputs.

2.1 Digital Control Inputs

The digital control inputs ($\overline{\text{CS}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$) meet standard T^2L logic voltage levels. These signals have been renamed when compared to the standard A/D Start and Output Enable labels. In addition, these inputs are active low to allow an easy interface to microprocessor control busses. For non-microprocessor based applications, the $\overline{\text{CS}}$ input (pin 1) can be grounded and the standard A/D Start function is obtained by an active low pulse applied at the $\overline{\text{WR}}$ input (pin 3) and the Output Enable function is caused by an active low pulse at the $\overline{\text{RD}}$ input (pin 2).

2.2 Analog Differential Voltage Inputs and Common-Mode Rejection

This A/D has additional applications flexibility due to the analog differential voltage input. The $V_{IN}(-)$ input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading (tare correction). This is also useful in 4 mA–20 mA current loop conversion. In addition, common-mode noise can be reduced by use of the differential input.

The time interval between sampling $V_{IN}(+)$ and $V_{IN}(-)$ is 4-1/2 clock periods. The maximum error voltage due where:

ΔV_e is the error voltage due to sampling delay

V_P is the peak value of the common-mode voltage

f_{cm} is the common-mode frequency

As an example, to keep this error to 1/4 LSB (~5 mV) when operating with a 60 Hz common-mode frequency, f_{cm}, and using a 640 kHz A/D clock, f_{CLK}, would allow a peak value of the common-mode voltage, V_P, which is given by:

$$V_P = \frac{[\Delta V_{e(MAX)}\,(f_{CLK})]}{(2\pi f_{cm})\,(4.5)}$$

or

$$V_P = \frac{(5 \times 10^{-3})\,(640 \times 10^{3})}{(6.28)\,(60)\,(4.5)}$$

which gives

$$V_P \cong 1.9V.$$

The allowed range of analog input voltages usually places more severe restrictions on input common-mode noise levels.

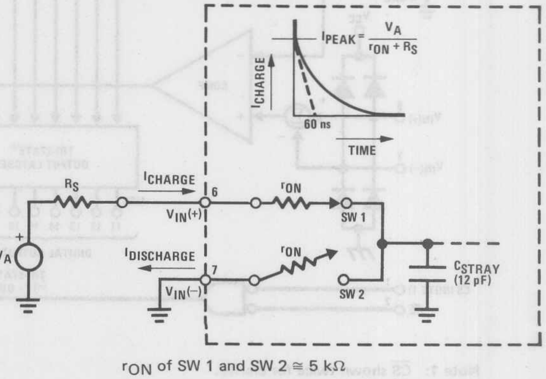
An analog input voltage with a reduced span and a relatively large zero offset can be easily handled by making use of the differential input (see section 2.4 Reference Voltage).

2.3 Analog Inputs

2.3.1 Input Current

Normal Mode

Due to the internal switching action, displacement currents will flow at the analog inputs. This is due to on-chip stray capacitance to ground as shown in *Figure 3*.



r_{ON} of SW 1 and SW 2 $\cong$ 5 kΩ

$\tau = r_{ON}\,C_{STRAY} \cong 5\text{ k}\Omega \times 12\text{ pF} = 60\text{ ns}$

FIGURE 3. Analog Input Impedance

The voltage on this capacitance is switched and will result in currents entering the $V_{IN}(+)$ input pin and leaving the $V_{IN}(-)$ input which will depend on the analog differential input voltage levels. These current transients occur at the leading edge of the internal clocks. They rapidly decay and *do not cause errors* as the on-chip comparator is strobed at the end of the clock period.

Fault Mode

If the voltage source which is applied to the $V_{IN}(+)$ pin exceeds the allowed operating range of V_{CC} + 50 mV, large input currents can flow through a parasitic diode to the V_{CC} pin. If these currents could exceed the 1 mA max allowed spec, an external diode (1N914) should be added to bypass this current to the V_{CC} pin (with the current bypassed with this diode, the voltage at the $V_{IN}(+)$ pin can exceed the V_{CC} voltage by the forward voltage of this diode).

2.3.2 Input Bypass Capacitors

Bypass capacitors at the inputs will average these charges and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN}(+)$ input voltage at full-scale. For continuous conversions with a 640 kHz clock frequency with the $V_{IN}(+)$ input at 5V, this DC current is at a maximum of approximately 5 μA. Therefore, *bypass capacitors should not be used at the analog inputs or the $V_{REF}/2$ pin* for high resistance sources (> 1 kΩ). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the detrimental effects of the voltage drop across this input resistance, which is due to the average value of the input current, can be eliminated with a full-scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a precise linear function of the differential input voltage.

2.3.3 Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used, *will not cause errors* as the input currents settle out prior to the comparison time. If a low pass filter is required in the system, use a low valued series resistor ($\lesssim$ 1 kΩ) for a passive RC section or add an op amp RC active low pass filter. For low source resistance applications, ($\lesssim$ 1 kΩ), a 0.1 μF bypass capacitor at the inputs will prevent pickup due to series lead inductance of a long wire. A 100Ω series resistor can be used to isolate this capacitor—both the R and C are placed outside the feedback loop—from the output of an op amp, if used.

2.3.4 Noise

The leads to the analog inputs (pins 6 and 7) should be kept as short as possible to minimize input noise coupling. Both noise and undesired digital clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below 5 kΩ. Larger values of source resistance can cause undesired system noise pickup. Input bypass capacitors, placed from the analog inputs to ground, will eliminate system noise pickup but can create analog scale errors as these capacitors will average the transient input switching currents of the A/D (see section 2.3.1). This scale error depends on both a large source resistance and the use of an input bypass capacitor. This error can be eliminated by doing a full-scale adjustment of the A/D (adjust $V_{REF}/2$ for a proper full-scale reading—see section 2.5.2 on Full-Scale Adjustment) with the source resistance and input bypass capacitor in place.

2.4 Reference Voltage

2.4.1 Span Adjust

For maximum applications flexibility, these A/Ds have been designed to accommodate a 5 V_{DC}, 2.5 V_{DC} or an adjusted voltage reference. This has been achieved in the design of the IC as shown in *Figure 4*.

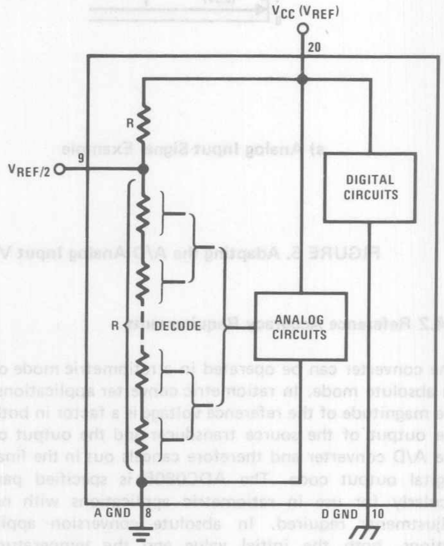
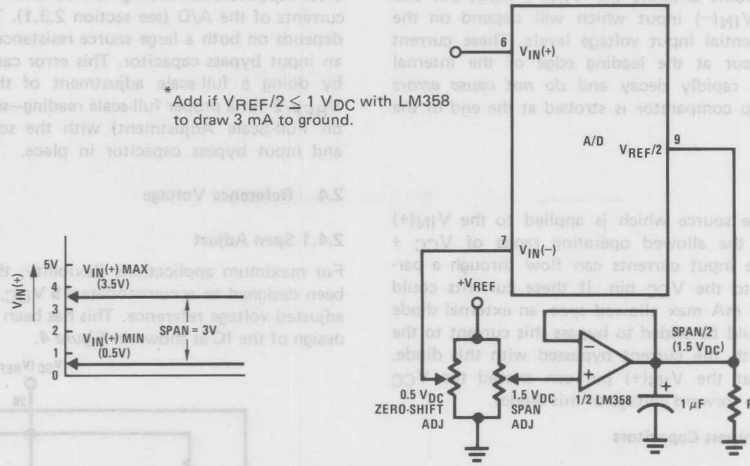


FIGURE 4. The $V_{REFERENCE}$ Design on the IC

Notice that the reference voltage for the IC is either 1/2 of the voltage which is applied to the V_{CC} supply pin, or is equal to the voltage which is externally forced at the $V_{REF}/2$ pin. This allows for a ratiometric voltage reference using the V_{CC} supply, a 5 V_{DC} reference voltage can be used for the V_{CC} supply or a voltage less than 2.5 V_{DC} can be applied to the $V_{REF}/2$ input for increased application flexibility. The internal gain to the $V_{REF}/2$ input is 2 making the full-scale differential input voltage twice the voltage at pin 9.

An example of the use of an adjusted reference voltage is to accommodate a reduced span—or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from 0.5 V_{DC} to 3.5 V_{DC}, instead of 0V to 5 V_{DC}, the span would be 3V as shown in *Figure 5*. With 0.5 V_{DC} applied to the $V_{IN}(-)$ pin to absorb the offset, the reference voltage can be made equal to 1/2 of the 3V span or 1.5 V_{DC}. The A/D now will encode the $V_{IN}(+)$ signal from 0.5V to 3.5V with the 0.5V input corresponding to zero and the 3.5 V_{DC} input corresponding to full-scale. The full 8 bits of resolution are therefore applied over this reduced analog input voltage range.



a) Analog Input Signal Example

b) Accommodating an Analog Input from 0.5V (Digital Out = 00_{HEX}) to 3.5V (Digital Out = FF_{HEX})

FIGURE 5. Adapting the A/D Analog Input Voltages to Match an Arbitrary Input Signal Range

2.4.2 Reference Accuracy Requirements

The converter can be operated in a ratiometric mode or an absolute mode. In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter and therefore cancels out in the final digital output code. The ADC0805 is specified particularly for use in ratiometric applications with no adjustments required. In absolute conversion applications, both the initial value and the temperature stability of the reference voltage are important accuracy factors in the operation of the A/D converter. For $V_{REF}/2$ voltages of 2.5 V_{DC} nominal value, initial errors of ±10 mV_{DC} will cause conversion errors of ±1 LSB due to the gain of 2 of the $V_{REF}/2$ input. In reduced span applications, the initial value and the stability of the $V_{REF}/2$ input voltage become even more important. For example, if the span is reduced to 2.5V, the analog input LSB voltage value is correspondingly reduced from 20 mV (5V span) to 10 mV and 1 LSB at the $V_{REF}/2$ input becomes 5 mV. As can be seen, this reduces the allowed initial tolerance of the reference voltage and requires correspondingly less absolute change with temperature variations. Note that spans smaller than 2.5V place even tighter requirements on the initial accuracy and stability of the reference source.

In general, the magnitude of the reference voltage will require an initial adjustment. Errors due to an improper value of reference voltage appear as full-scale errors in the A/D transfer function. IC voltage regulators may be used for references if the ambient temperature changes are not excessive. The LM336B 2.5V IC reference diode (from National Semiconductor) is available which has a temperature stability of 1.8 mV typ (6 mV max) over $0°C \leq T_A \leq +70°C$. Other temperature range parts are also available.

2.5 Errors and Reference Voltage Adjustments

2.5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the A/D V_{IN} (−) input at this $V_{IN(MIN)}$ value (see Applications section). This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the V (−) input and applying a small magnitude positive voltage to the V (+) input. Zero error is the difference between the actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal 1/2 LSB value (1/2 LSB = 9.8 mV for $V_{REF}/2 = 2.500\ V_{DC}$).

2.5.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage which is 1-1/2 LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the $V_{REF}/2$ input (pin 9 or the V_{CC} supply if pin 9 is not used) for a digital output code which is just changing from 1111 1110 to 1111 1111.

2.5.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal which does not go to ground) this new zero reference should be properly adjusted first. A $V_{IN}(+)$ voltage which equals this desired zero reference plus 1/2 LSB (where the LSB is calculated for the desired analog span, 1 LSB = analog span/256) is applied to pin 6 and the zero reference voltage at pin 7 should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.

The full-scale adjustment should then be made (with the proper $V_{IN}(-)$ voltage applied) by forcing a voltage to the $V_{IN}(+)$ input which is given by:

$$V_{IN}(+)\ \text{fs adj} = V_{MAX} - 1.5 \left[\frac{(V_{MAX} - V_{MIN})}{256}\right],$$

where:

V_{MAX} = The high end of the analog input range

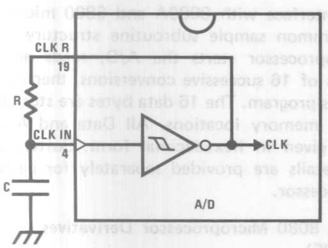
and

V_{MIN} = the low end (the offset zero) of the analog range. (Both are ground referenced.)

The $V_{REF}/2$ (or V_{CC}) voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

2.6 Clocking Option

The clock for the A/D can be derived from the CPU clock or an external RC can be added to provide self-clocking. The CLK IN (pin 4) makes use of a Schmitt trigger as shown in *Figure 6*.



$$f_{CLK} \cong \frac{1}{1.1\ RC}$$

$R \cong 10\ k\Omega$

FIGURE 6. Self-Clocking the A/D

Heavy capacitive or DC loading of the clock R pin should be avoided as this will disturb normal converter operation. Loads less than 50 pF, such as driving up to 7 A/D converter clock inputs from a single clock R pin of 1 converter, are allowed. For larger clock line loading, a CMOS or low power T^2L buffer or PNP input logic should be used to minimize the loading on the clock R pin (do not use a standard T^2L buffer).

2.7 Restart During a Conversion

If the A/D is restarted ($\overline{CS}$ and $\overline{WR}$ go low and return high) during a conversion, the converter is reset and a new conversion is started. The output data latch is not updated if the conversion in process is not allowed to be completed, therefore the data of the previous conversion remains in this latch. The $\overline{INTR}$ output also simply remains at the "1" level.

2.8 Continuous Conversions

For operation in the free-running mode an initializing pulse should be used, following power-up, to insure circuit operation. In this application, the $\overline{CS}$ input is grounded and the $\overline{WR}$ input is tied to the $\overline{INTR}$ output. This $\overline{WR}$ and $\overline{INTR}$ node should be momentarily forced to logic low following a power-up cycle to guarantee operation.

2.9 Driving the Data Bus

This MOS A/D, like MOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry, which is tied to the data bus, will add to the total capacitive loading, even in TRI-STATE (high impedance mode). Backplane bussing also greatly adds to the stray capacitance of the data bus.

There are some alternatives available to the designer to handle this problem. Basically, the capacitive loading of the data bus slows down the response time, even though DC specifications are still met. For systems operating with a relatively slow CPU clock frequency, more time is available in which to establish proper logic levels on the bus and therefore higher capacitive loads can be driven (see typical characteristics curves).

At higher CPU clock frequencies time can be extended for I/O reads (and/or writes) by inserting wait states (8080) or using clock extending circuits (6800).

Finally, if time is short and capacitive loading is high, external bus drivers must be used. These can be TRI-STATE buffers (low power Schottky is recommended such as the DM74LS240 series) or special higher drive current products which are designed as bus drivers. High current bipolar bus drivers with PNP inputs are recommended.

2.10 Power Supplies

Noise spikes on the V_{CC} supply line can cause conversion errors as the comparator will respond to this noise. A low inductance tantalum filter capacitor should be used close to the converter V_{CC} pin and values of 1 μF or greater are recommended. If an unregulated voltage is available in the system, a separate LM340LAZ-5.0, TO-92, 5V voltage regulator for the converter (and other analog circuitry) will greatly reduce digital noise on the V_{CC} supply.

2.11 Wiring and Hook-Up Precautions

Standard digital wire wrap sockets are not satisfactory for breadboarding this A/D converter. Sockets on PC boards can be used and all logic signal wires and leads should be grouped and kept as far away as possible from the analog signal leads. Exposed leads to the analog inputs can cause undesired digital noise and hum pickup, therefore shielded leads may be necessary in many applications.

bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point. A test for proper grounding is to measure the zero error of the A/D converter. Zero errors in excess of 1/4 LSB can usually be traced to improper board layout and wiring (see section 2.5.1 for measuring the zero error).

3.0 TESTING THE A/D CONVERTER

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in *Figure 7*.

For ease of testing, the $V_{REF}/2$ (pin 9) should be supplied with 2.560 V_{DC} and a V_{CC} supply voltage of 5.12 V_{DC} should be used. This provides an LSB value of 20 mV.

If a full-scale adjustment is to be made, an analog input voltage of 5.090 V_{DC} (5.120 − 1 1/2 LSB) should be applied to the $V_{IN}(+)$ pin with the $V_{IN}(-)$ pin grounded. The value of the $V_{REF}/2$ input voltage should then be adjusted until the digital output code is just changing from 1111 1110 to 1111 1111. This value of $V_{REF}/2$ should then be used for all the tests.

The digital output LED display can be decoded by dividing the 8 bits into 2 hex characters, the 4 most significant (MS) and the 4 least significant (LS). Table I shows the fractional binary equivalent of these two 4-bit groups. By adding the decoded voltages which are obtained from the column: Input voltage value for a 2.560 $V_{REF}/2$ of both the MS and the LS groups, the value of

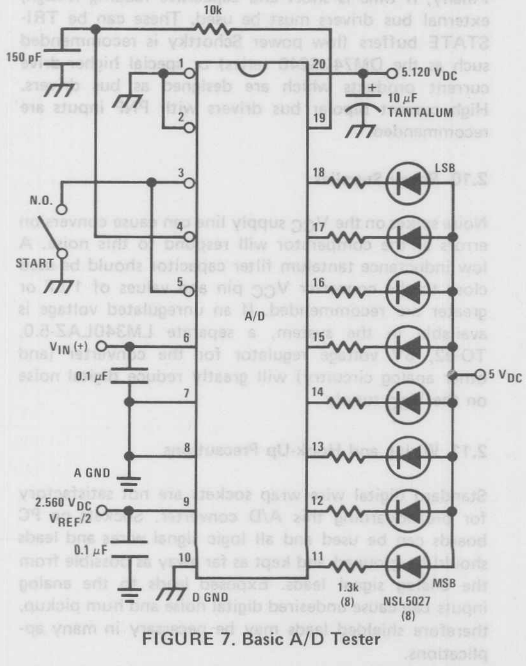


FIGURE 7. Basic A/D Tester

values of a perfect A/D converter. The effects of quantization error have to be accounted for in the interpretation of the test results.

For a higher speed test system, or to obtain plotted data, a digital-to-analog converter is needed for the test set-up. An accurate 10-bit DAC can serve as the precision voltage source for the A/D. Errors of the A/D under test can be provided as either analog voltages or differences in 2 digital words.

A basic A/D tester which uses a DAC and provides the error as an analog output voltage is shown in *Figure 8*. The 2 op amps can be eliminated if a lab DVM with a numerical subtraction feature is available to directly readout the difference voltage, "A–C". The analog input voltage can be supplied by a low frequency ramp generator and an X-Y plotter can be used to provide analog error (Y axis) versus analog input (X axis). The construction details of a tester of this type are provided in the NSC application note AN-179, "Analog-to-Digital Converter Testing".

For operation with a microprocessor or a computer-based test system, it is more convenient to present the errors digitally. This can be done with the circuit of *Figure 9*, where the output code transitions can be detected as the 10-bit DAC is incremented. This provides 1/4 LSB steps for the 8-bit A/D under test. If the results of this test are automatically plotted with the analog input on the X axis and the error (in LSB's) as the Y axis, a useful transfer function of the A/D under test results. For acceptance testing, the plot is not necessary and the testing speed can be increased by establishing internal limits on the allowed error for each code.

4.0 MICROPROCESSOR INTERFACING

To discuss the interface with 8080A and 6800 microprocessors, a common sample subroutine structure is used. The microprocessor starts the A/D, reads and stores the results of 16 successive conversions, then returns to the user's program. The 16 data bytes are stored in 16 successive memory locations. All Data and Addresses will be given in hexadecimal form. Software and hardware details are provided separately for each type of microprocessor.

4.1 Interfacing 8080 Microprocessor Derivatives (8048, 8085)

This converter has been designed to directly interface with derivatives of the 8080 microprocessor. The A/D can be mapped into memory space (using standard memory address decoding for $\overline{CS}$ and the $\overline{MEMR}$ and $\overline{MEMW}$ strobes) or it can be controlled as an I/O device by using the $\overline{I/O\ R}$ and $\overline{I/O\ W}$ strobes and decoding the address bits A0 → A7 (or address bits A8 → A15 as they will contain the same 8-bit address information) to obtain the $\overline{CS}$ input. Using the I/O space provides 256 additional addresses and may allow a simpler 8-bit address decoder but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D should be mapped into memory space. An example of an A/D in I/O space is shown in *Figure 10*.

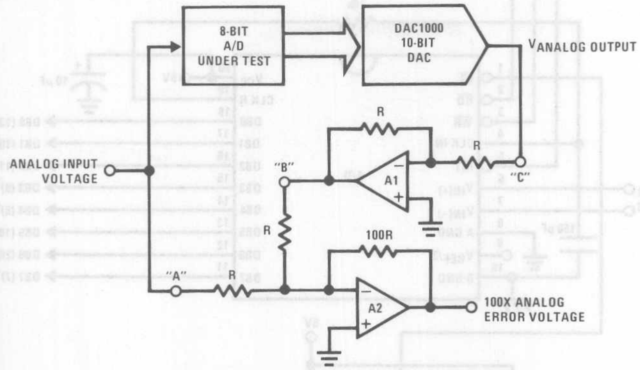


FIGURE 8. A/D Tester with Analog Error Output

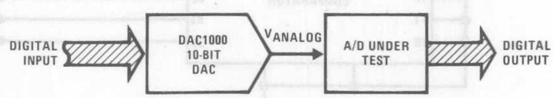
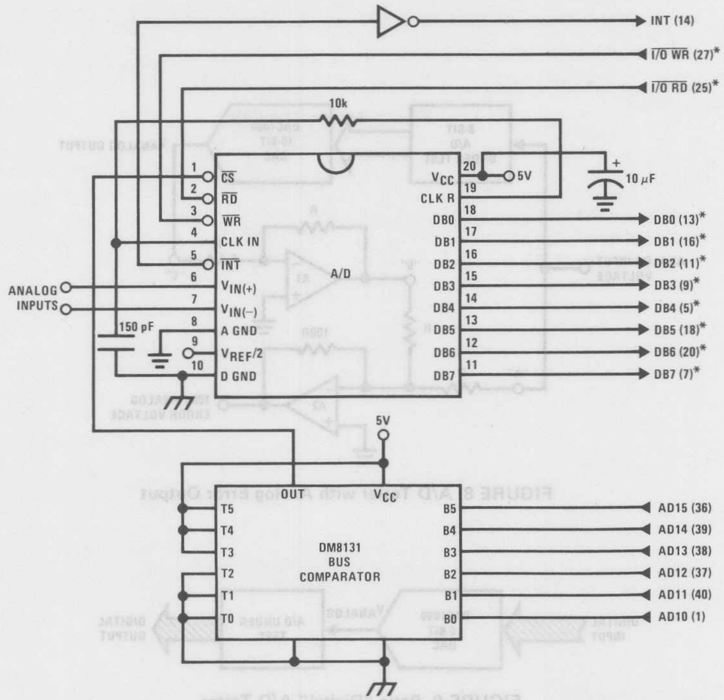


FIGURE 9. Basic "Digital" A/D Tester

TABLE I. DECODING THE DIGITAL OUTPUT LEDs

HEX	BINARY	FRACTIONAL BINARY VALUE FOR		OUTPUT VOLTAGE CENTER VALUES WITH $V_{REF}/2 = 2.560\ V_{DC}$	
		MS GROUP	LS GROUP	VMS GROUP*	VLS GROUP*
F	1 1 1 1	15/16	15/256	4.800	0.300
E	1 1 1 0	7/8	7/128	4.480	0.280
D	1 1 0 1	13/16	13/256	4.160	0.260
C	1 1 0 0	3/4	3/64	3.840	0.240
B	1 0 1 1	11/16	11/256	3.520	0.220
A	1 0 1 0	5/8	5/128	3.200	0.200
9	1 0 0 1	9/16	9/256	2.880	0.180
8	1 0 0 0	1/2	1/32	2.560	0.160
7	0 1 1 1	7/16	7/256	2.240	0.140
6	0 1 1 0	3/8	3/128	1.920	0.120
5	0 1 0 1	5/16	5/256	1.600	0.100
4	0 1 0 0	1/4	1/64	1.280	0.080
3	0 0 1 1	3/16	3/256	0.960	0.060
2	0 0 1 0	1/8	1/128	0.640	0.040
1	0 0 0 1	1/16	1/256	0.320	0.020
0	0 0 0 0			0	0

*V Display Output = VMS Group + VLS Group



Note 1: *Pin numbers for the INS8228 system controller, others are INS8080A.

Note 2: Pin 23 of the INS8228 must be tied to +12V through a 1 kΩ resistor to generate the RST 7 instruction when an interrupt is acknowledged as required by the accompanying sample program.

FIGURE 10. ADC0801–INS8080A CPU Interface

SAMPLE PROGRAM FOR *FIGURE 10* ADC0801–INS8080A CPU INTERFACE

```
0038   C3 00 03   RST 7:        JMP  LD DATA
 .        .
 .        .          .
0100   21 00 02   START:        LXI H 0200H    ; HL pair will point to
                                               ; data storage locations
0103   31 00 04   RETURN:       LXI SP 0400H   ; Initialize stack pointer (Note 1)
0106   7D                       MOV A, L       ; Test # of bytes entered
0107   FE OF                    CPI OF H       ; If # = 16. JMP to
0109   CA 13 01                 JZ CONT        ; user program
010C   D3 E0                    OUT E0 H       ; Start A/D
010E   FB                       EI             ; Enable interrupt
010F   00         LOOP:         NOP            ; Loop until end of
0110   C3 0F 01                 JMP LOOP       ; conversion
0113   .          CONT:           .
 .     .            .             .
 .     .          (User program to .
                  process data)
 .     .                          .
 .     .                          .
 .     .            .             .
0300   DB E0      LD DATA:      IN E0 H        ; Load data into accumulator
0302   77                       MOV M, A       ; Store data
0303   23                       INX H          ; Increment storage pointer
0304   C3 03 01                 JMP  RETURN
```

Note 1: The stack pointer must be dimensioned because a RST 7 instruction pushes the PC onto the stack.

Note 2: All addresses used were arbitrarily chosen.

The standard control bus signals of the 8080 (CS, RD and WR) can be directly wired to the digital control inputs of the A/D and the bus timing requirements are met to allow both starting the converter and outputting the data onto the data bus. A bus driver should be used for larger microprocessor systems where the data bus leaves the PC board and/or must drive capacitive loads larger than 100 pF.

4.1.1 Sample 8080A CPU Interfacing Circuitry and Program

The following sample program and associated hardware shown in *Figure 10* may be used to input data from the converter to the INS8080A CPU chip set (comprised of the INS8080A microprocessor, the INS8228 system controller and the INS8224 clock generator). For simplicity, the A/D is controlled as an I/O device, specifically an 8-bit bi-directional port located at an arbitrarily chosen port address, E0. The TRI-STATE output capability of the A/D eliminates the need for a peripheral interface device, however address decoding is still required to generate the appropriate CS for the converter.

It is important to note that in systems where the A/D converter is 1-of-8 or less I/O mapped devices, no address decoding circuitry is necessary. Each of the 8 address bits (A0 to A7) can be directly used as CS inputs—one for each I/O device.

4.1.2 INS8048 Interface

The INS8048 interface technique with the ADC0801 series (see *Figure 11*) is simpler than the 8080A CPU interface. There are 24 I/O lines and three test input lines in the 8048. With these extra I/O lines available, one of the I/O lines (bit 0 of port 1) is used as the chip select signal to the A/D, thus eliminating the use of an external address decoder. Bus control signals RD, WR and INT of the 8048 are tied directly to the A/D. The 16 converted data words are stored at on-chip RAM locations from 20 to 2F (Hex). The RD and WR signals are generated by reading from and writing into a dummy address, respectively. A sample interface program is shown below.

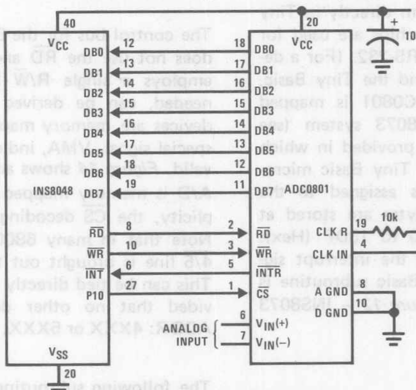


FIGURE 11. INS8048 Interface

SAMPLE PROGRAM FOR *FIGURE 11* INS8048 INTERFACE

```
04 10              JMP     10H          ; Program starts at addr 10
                   ORG     3H
04 50              JMP     50H          ; Interrupt jump vector
                   ORG     10H          ; Main program
99 FE              ANL     P1, #0FEH    ; Chip select
81                 MOVX    A, @R1       ; Read in the 1st data
                                        ; to reset the intr
89 01   START:     ORL     P1, #1       ; Set port pin high
B8 20              MOV     R0, #20H     ; Data address
B9 FF              MOV     R1, #0FFH    ; Dummy address
BA 10              MOV     R2, #10H     ; Counter for 16 bytes
23 FF   AGAIN:     MOV     A, #0FFH     ; Set ACC for intr loop
99 FE              ANL     P1, #0FEH    ; Send CS (bit 0 of P1)
91                 MOVX    @R1, A       ; Send WR out
05                 EN      I            ; Enable interrupt
96 21   LOOP:      JNZ     LOOP         ; Wait for interrupt
EA 1B              DJNZ    R2, AGAIN    ; If 16 bytes are read
00                 NOP                  ; go to user's program
00                 NOP
                   ORG     50H
81      INDATA:    MOVX    A, @R1       ; Input data, CS still low
A0                 MOV     @R0, A       ; Store in memory
18                 INC     R0           ; Increment storage counter
89 01              ORL     P1, #1       ; Reset CS signal
27                 CLR     A            ; Clear ACC to get out of
93                 RETR                 ; the interrupt loop
```

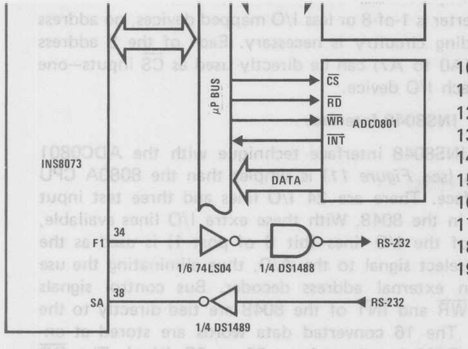


FIGURE 12. INS8073 Interface

4.1.3 INS8073 Interface

The INS8073 allows users to program directly in Tiny Basic. DS1488/1489 driver/receiver chips are used for level buffering to communicate via RS-232. (For a detailed description of the INS8073 and the Tiny Basic, see INS8073 data sheet.) The ADC0801 is mapped into the memory space of the 8073 system (see *Figure 12*). A RAM of 1k bytes is provided in which the first 256 bytes are used by the Tiny Basic micro-interpreter. Address 3000 (Hex) is assigned to the A/D and the 16 converted data bytes are stored at external RAM locations from 13D0 to 13DF (Hex). STAT function is used to examine the interrupt signal from the A/D. A sample Tiny Basic subroutine is given in the sample program for *Figure 12* – INS8073 Interface.

4.2 Interfacing the Z-80

The Z-80 control bus is slightly different from that of the 8080. General $\overline{RD}$ and $\overline{WR}$ strobes are provided and separate memory request, $\overline{MREQ}$, and I/O request, $\overline{IORQ}$, signals are used which have to be combined with the generalized strobes to provide the equivalent 8080 signals. An advantage of operating the A/D in I/O space with the Z-80 is that the CPU will automatically insert one wait state (the $\overline{RD}$ and $\overline{WR}$ strobes are extended one clock period) to allow more time for the I/O devices to respond. Logic to map the A/D in I/O space is shown in *Figure 13*.

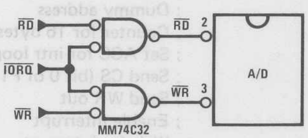


FIGURE 13. Mapping the A/D as an I/O Device for Use with the Z-80 CPU

Additional I/O advantages exist as software DMA routines are available and use can be made of the output data transfer which exists on the upper 8 address lines (A8 to A15) during I/O input instructions. For example, MUX channel selection for the A/D can be accomplished with this operating mode.

SAMPLE PROGRAM FOR *FIGURE 12* – INS8073 INTERFACE

```
100   C = 16                         ; REM C is the 16 bytes counter
110   D = #13D0                      ; REM D points to data address
120   @ #3000 = A                    ; REM start A/D
130   A = STAT AND #20               ; REM wait until interrupt
140   IF A <> 0 THEN GO TO 130       ; REM from A/D
150   @ D = @ #3000                  ; REM input converted data
160   D = D + 1                      ; REM increment data address
170   C = C − 1                      ; REM check counter
180   IF C > 0 THEN GO TO 120        ; REM if 16 data have been read
190   RETURN                         ; REM return to main program
```

4.3 Interfacing 6800 Microprocessor Derivatives (6502, etc.)

The control bus for the 6800 microprocessor derivatives does not use the $\overline{RD}$ and $\overline{WR}$ strobe signals. Instead it employs a single R/$\overline{W}$ line and additional timing, if needed, can be derived from the $\phi 2$ clock. All I/O devices are memory mapped in the 6800 system, and a special signal, VMA, indicates that the current address is valid. *Figure 14* shows an interface schematic where the A/D is memory mapped in the 6800 system. For simplicity, the $\overline{CS}$ decoding is shown using 1/2 DM8092. Note that in many 6800 systems, an already decoded $\overline{4/5}$ line is brought out to the common bus at pin 21. This can be tied directly to the $\overline{CS}$ pin of the A/D, provided that no other devices are addressed at HEX ADDR: 4XXX or 5XXX.

The following subroutine essentially performs the same function as in the case of the 8080A interface and it can be called from anywhere in the user's program.

In *Figure 15* the ADC0801 series is interfaced to the M6800 microprocessor through (the arbitrarily chosen) Port B of the MC6820 or MC6821 Peripheral Interface Adapter, (PIA). Here the $\overline{CS}$ pin of the A/D is grounded since the PIA is already memory mapped in the M6800 system and no $\overline{CS}$ decoding is necessary. Also notice that the A/D output data lines are connected to the microprocessor bus under program control through the PIA and therefore the A/D $\overline{RD}$ pin can be grounded.

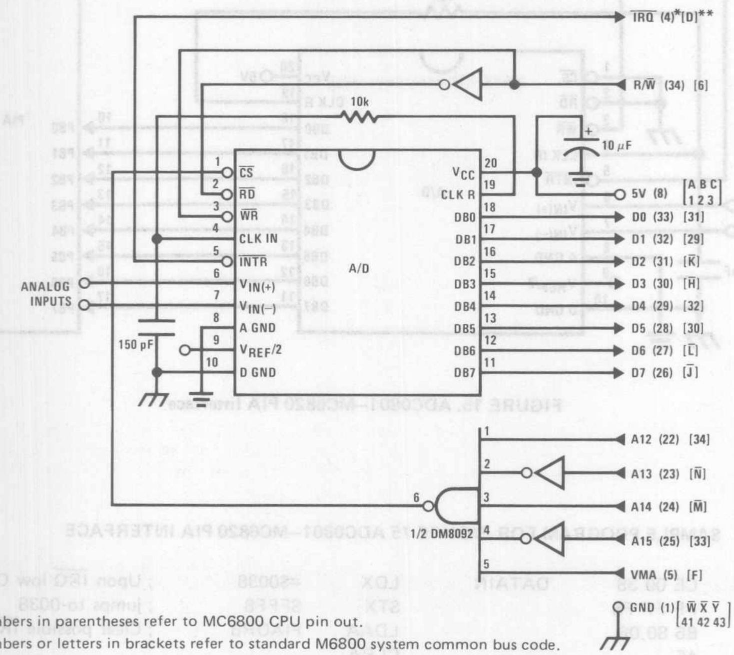
A sample interface program equivalent to the previous one, is shown below *Figure 15*. The PIA Data and Control Registers of Port B are located at HEX addresses 8006 and 8007, respectively.

5.0 GENERAL APPLICATIONS

The following applications show some interesting uses for the A/D. The fact that one particular microprocessor is used is not meant to be restrictive. Each of these application circuits would have its counterpart using any microprocessor which is desired.

5.1 Multiple ADC0801 Series to MC6800 CPU Interface

To transfer analog data from several channels to a single microprocessor system, a multiple converter scheme presents several advantages over the conventional multiplexer single-converter approach. With the ADC0801 series, the differential inputs allow individual span adjustment for each channel. Furthermore, all analog input channels are sensed simultaneously, which essentially divides the microprocessor's total system servicing time by the number of channels, since all conversions occur simultaneously. This scheme is shown in *Figure 16*.



Note 1: Numbers in parentheses refer to MC6800 CPU pin out.

Note 2: Numbers or letters in brackets refer to standard M6800 system common bus code.

FIGURE 14. ADC0801–MC6800 CPU Interface

SAMPLE PROGRAM FOR *FIGURE 14* ADC0801–MC6800 CPU INTERFACE

```
0010   DF 36      DATAIN   STX    TEMP2      ; Save contents of X
0012   CE 00 2C            LDX    #$002C     ; Upon IRQ low CPU
0015   FF FF F8            STX    $FFF8      ; jumps to 002C
0018   B7 50 00            STAA   $5000      ; Starts ADC0801
001B   0E                  CLI
001C   3E         CONVRT   WAI               ; Wait for interrupt
001D   DE 34               LDX    TEMP1
001F   8C 02 0F            CPX    #$020F     ; Is final data stored?
0022   27 14               BEQ    ENDP
0024   B7 50 00            STAA   $5000      ; Restarts ADC0801
0027   08                  INX
0028   DF 34               STX    TEMP1
002A   20 F0               BRA    CONVRT
002C   DE 34      INTRPT   LDX    TEMP1
002E   B6 50 00            LDAA   $5000      ; Read data
0031   A7 00               STAA   X          ; Store it at X
0033   3B                  RTI
0034   02 00      TEMP1    FDB    $0200      ; Starting address for
                                             ; data storage
0036   00 00      TEMP2    FDB    $0000
0038   CE 02 00   ENDP     LDX    #$0200     ; Reinitialize TEMP1
003B   DF 34               STX    TEMP1
003D   DE 36               LDX    TEMP2
003F   39                  RTS
                                             ; Return from subroutine
                                             ; To user's program
```

Note 1: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.

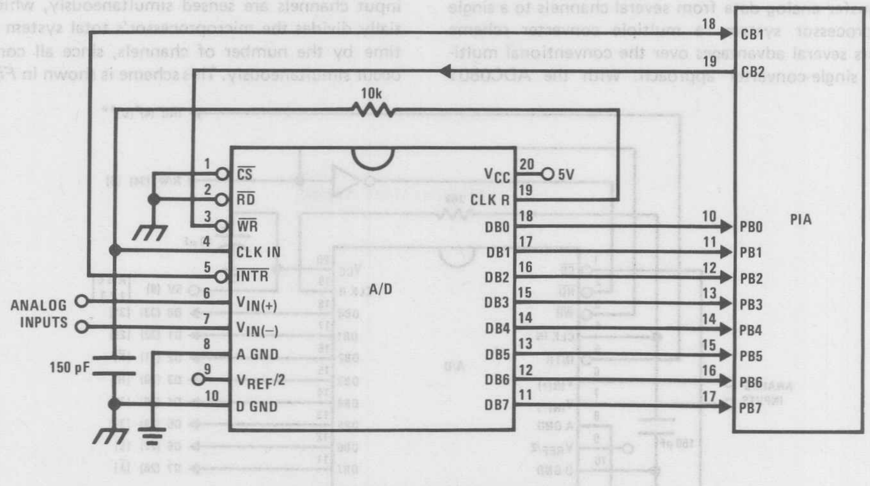


FIGURE 15. ADC0801–MC6820 PIA Interface

SAMPLE PROGRAM FOR *FIGURE 15* ADC0801–MC6820 PIA INTERFACE

```
0010  CE 00 38   DATAIN   LDX    #$0038    ; Upon IRQ low CPU
0013  FF FF F8            STX    $FFF8     ; jumps to 0038
0016  B6 80 06            LDAA   PIAORB    ; Clear possible IRQ flags
0019  4F                  CLRA
001A  B7 80 07            STAA   PIACRB
001D  B7 80 06            STAA   PIAORB    ; Set Port B as input
0020  0E                  CLI
0021  C6 34               LDAB   #$34
0023  86 3D               LDAA   #$3D
0025  F7 80 07   CONVRT   STAB   PIACRB    ; Starts ADC0801
0028  B7 80 07            STAA   PIACRB
002B  3E                  WAI              ; Wait for interrupt
002C  DE 40               LDX    TEMP1
002E  8C 02 0F            CPX    #$020F    ; Is final data stored?
0031  27 0F               BEQ    ENDP
0033  08                  INX
0034  DF 40               STX    TEMP1
0036  20 ED               BRA    CONVRT
0038  DE 40      INTRPT   LDX    TEMP1
003A  B6 80 06            LDAA   PIAORB    ; Read data in
003D  A7 00               STAA   X         ; Store it at X
003F  3B                  RTI
0040  02 00      TEMP1    FDB    $0200     ; Starting address for
                                           ; data storage
0042  CE 02 00   ENDP     LDX    #$0200    ; Reinitialize TEMP1
0045  DF 40               STX    TEMP1
0047  39                  RTS              ; Return from subroutine
                 PIAORB   EQU    $8006     ; To user's program
                 PIACRB   EQU    $8007
```

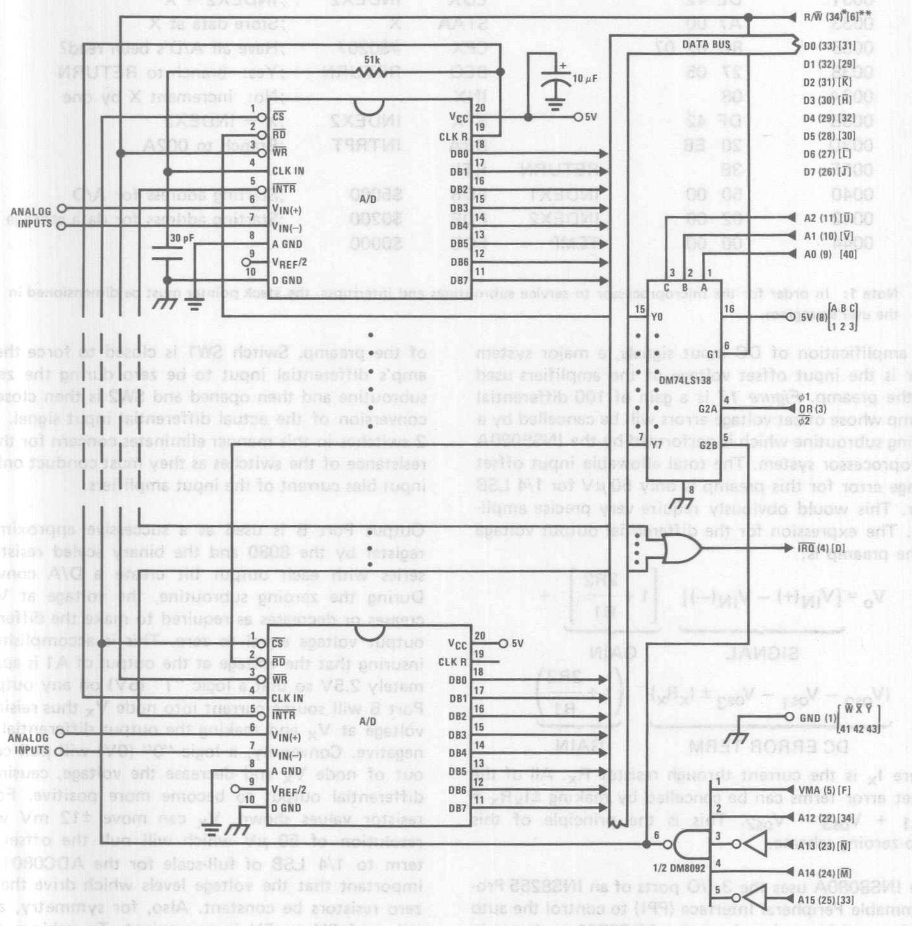
The following schematic and sample subroutine (DATA IN) may be used to interface (up to) 8 ADC0801's directly to the MC6800 CPU. This scheme can easily be extended to allow the interface of more converters. In this configuration the converters are (arbitrarily) located at HEX address 5000 in the MC6800 memory space. To save components, the clock signal is derived from just one RC pair on the first converter. This output drives the other A/Ds.

All the converters are started simultaneously with a STORE instruction at HEX address 5000. Note that any other HEX address of the form 5XXX will be decoded by the circuit, pulling all the $\overline{CS}$ inputs low. This can easily be avoided by using a more definitive address decoding scheme. All the interrupts are ORed together to insure that all A/Ds have completed their conversion before the microprocessor is interrupted.

The subroutine, DATA IN, may be called from anywhere in the user's program. Once called, this routine initializes the CPU, starts all the converters simultaneously and waits for the interrupt signal. Upon receiving the interrupt, it reads the converters (from HEX addresses 5000 through 5007) and stores the data successively at (arbitrarily chosen) HEX addresses 0200 to 0207, before returning to the user's program. All CPU registers then recover the original data they had before servicing DATA IN.

5.2 Auto-Zeroed Differential Transducer Amplifier and A/D Converter

The differential inputs of the ADC0801 series eliminate the need to perform a differential to single ended conversion for a differential transducer. Thus, one op amp can be eliminated since the differential to single ended conversion is provided by the differential input of the ADC0801 series. In general, a transducer preamp is required to take advantage of the full A/D converter input dynamic range.



Note 1: Numbers in parentheses refer to MC6800 CPU pin out.

Note 2: Numbers or letters in brackets refer to standard M6800 system common bus code.

FIGURE 16. Interfacing Multiple A/Ds in an MC6800 System

```
0010   DF 44      DATAIN   STX    TEMP      ; Save Contents of X
0012   CE 00 2A            LDX    #$002A    ; Upon IRQ LOW CPU
0015   FF FF F8            STX    $FFF8     ; Jumps to 002A
0018   B7 50 00            STAA   $5000     ; Starts all A/D's
001B   0E                  CLI
001C   3E                  WAI              ; Wait for interrupt
001D   CE 50 00            LDX    #$5000
0020   DF 40               STX    INDEX1    ; Reset both INDEX
0022   CE 02 00            LDX    #$0200    ; 1 and 2 to starting
0025   DF 42               STX    INDEX2    ; addresses
0027   DE 44               LDX    TEMP
0029   39                  RTS              ; Return from subroutine
002A   DE 40      INTRPT   LDX    INDEX1    ; INDEX1 → X
002C   A6 00               LDAA   X         ; Read data in from A/D at X
002E   08                  INX              ; Increment X by one
002F   DF 40               STX    INDEX1    ; X → INDEX1
0031   DE 42               LDX    INDEX2    ; INDEX2 → X
0033   A7 00               STAA   X         ; Store data at X
0035   8C 02 07            CPX    #$0207    ; Have all A/D's been read?
0038   27 05               BEQ    RETURN    ; Yes:  branch to RETURN
003A   08                  INX              ; No:  increment X by one
003B   DF 42               STX    INDEX2    ; X → INDEX2
003D   20 EB               BRA    INTRPT    ; Branch to 002A
003F   3B         RETURN   RTI
0040   50 00      INDEX1   FDB    $5000     ; Starting address for A/D
0042   02 00      INDEX2   FDB    $0200     ; Starting address for data storage
0044   00 00      TEMP     FDB    $0000
```

Note 1: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.

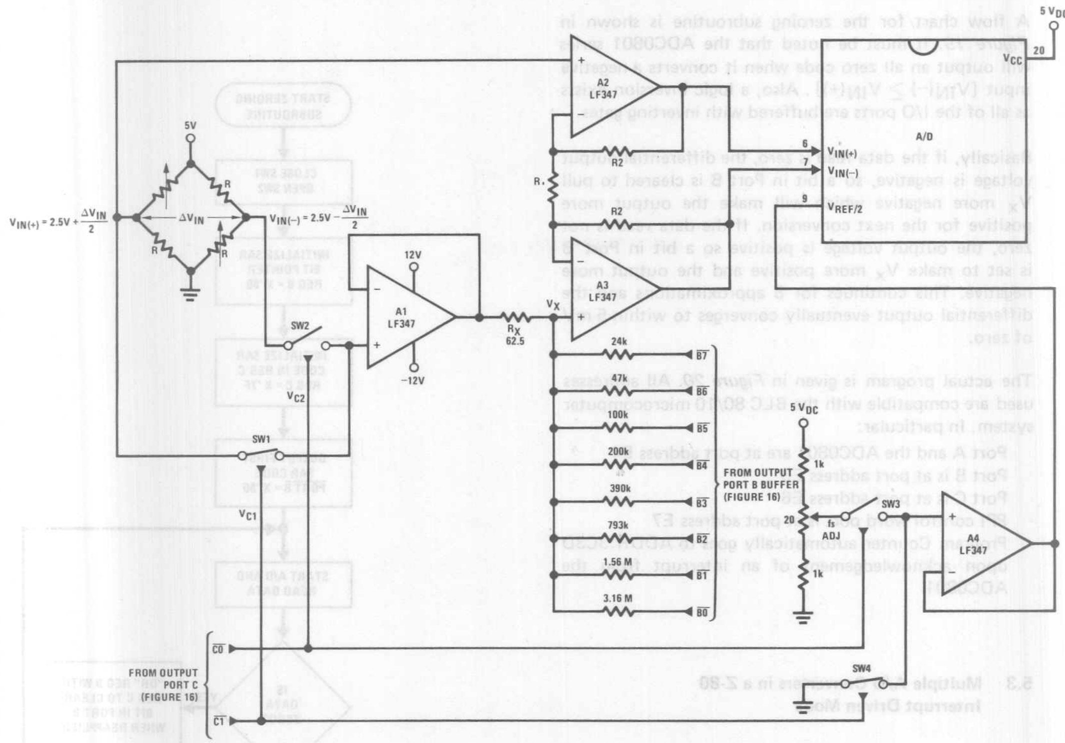
For amplification of DC input signals, a major system error is the input offset voltage of the amplifiers used for the preamp. *Figure 17* is a gain of 100 differential preamp whose offset voltage errors will be cancelled by a zeroing subroutine which is performed by the INS8080A microprocessor system. The total allowable input offset voltage error for this preamp is only 50 μV for 1/4 LSB error. This would obviously require very precise amplifiers. The expression for the differential output voltage of the preamp is:

$$V_o = \underbrace{[V_{IN}(+) - V_{IN}(-)]}_{\text{SIGNAL}} \underbrace{\left[1 + \frac{2R2}{R1}\right]}_{\text{GAIN}} + \underbrace{(V_{os2} - V_{os1} - V_{os3} \pm I_x R_x)}_{\text{DC ERROR TERM}} \underbrace{\left(1 + \frac{2R2}{R1}\right)}_{\text{GAIN}}$$

where I_x is the current through resistor R_x. All of the offset error terms can be cancelled by making $\pm I_x R_x = V_{os1} + V_{os3} - V_{os2}$. This is the principle of this auto-zeroing scheme.

The INS8080A uses the 3 I/O ports of an INS8255 Programmable Peripheral Interface (PPI) to control the auto zeroing and input data from the ADC0801 as shown in *Figure 18*. The PPI is programmed for basic I/O operation (mode 0) with Port A being an input port and Ports B and C being output ports. Two bits of Port C are used to alternately open or close the 2 switches at the input of the preamp. Switch SW1 is closed to force the preamp's differential input to be zero during the zeroing subroutine and then opened and SW2 is then closed for conversion of the actual differential input signal. Using 2 switches in this manner eliminates concern for the ON resistance of the switches as they must conduct only the input bias current of the input amplifiers.

Output Port B is used as a successive approximation register by the 8080 and the binary scaled resistors in series with each output bit create a D/A converter. During the zeroing subroutine, the voltage at V_x increases or decreases as required to make the differential output voltage equal to zero. This is accomplished by insuring that the voltage at the output of A1 is approximately 2.5V so that a logic "1" (5V) on any output of Port B will source current into node V_x thus raising the voltage at V_x and making the output differential more negative. Conversely, a logic "0" (0V) will pull current out of node V_x and decrease the voltage, causing the differential output to become more positive. For the resistor values shown, V_x can move ±12 mV with a resolution of 50 μV which will null the offset error term to 1/4 LSB of full-scale for the ADC0801. It is important that the voltage levels which drive the autozero resistors be constant. Also, for symmetry, a logic swing of 0V to 5V is convenient. To achieve this, a CMOS buffer is used for the logic output signals of Port B and this CMOS package is powered with a stable 5V source. Buffer amplifier A1 is necessary so that it can source or sink the D/A output current.



Note 1: R2 = 49.5 R1

Note 2: Switches are CD4066BC CMOS analog switches.

Note 3: The 9 resistors used in the auto-zero section can be ±5% tolerance.

FIGURE 17. Gain of 100 Differential Transducer Preamp

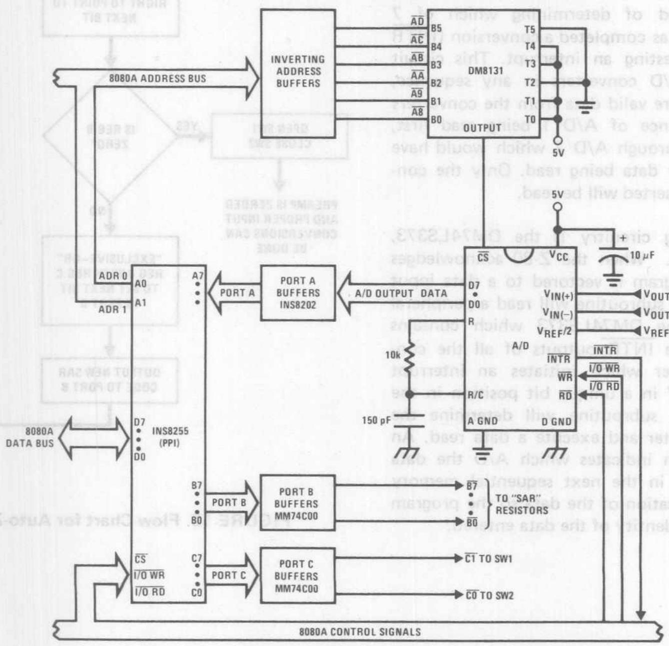


FIGURE 18. Microprocessor Interface Circuitry for Differential Preamp

A flow chart for the zeroing subroutine is shown in *Figure 19*. It must be noted that the ADC0801 series will output an all zero code when it converts a negative input $[V_{IN}(-) \geq V_{IN}(+)]$. Also, a logic inversion exists as all of the I/O ports are buffered with inverting gates.

Basically, if the data read is zero, the differential output voltage is negative, so a bit in Port B is cleared to pull V_X more negative which will make the output more positive for the next conversion. If the data read is not zero, the output voltage is positive so a bit in Port B is set to make V_X more positive and the output more negative. This continues for 8 approximations and the differential output eventually converges to within 5 mV of zero.

The actual program is given in *Figure 20*. All addresses used are compatible with the BLC 80/10 microcomputer system. In particular:

Port A and the ADC0801 are at port address E4
Port B is at port address E5
Port C is at port address E6
PPI control word port is at port address E7
Program Counter automatically goes to ADDR:3C3D upon acknowledgement of an interrupt from the ADC0801

5.3 Multiple A/D Converters in a Z-80 Interrupt Driven Mode

In data acquisition systems where more than one A/D converter (or other peripheral device) will be interrupting program execution of a microprocessor, there is obviously a need for the CPU to determine which device requires servicing. *Figure 21* and the accompanying software is a method of determining which of 7 ADC0801 converters has completed a conversion ($\overline{INTR}$ asserted) and is requesting an interrupt. This circuit allows starting the A/D converters in any sequence, but will input and store valid data from the converters with a priority sequence of A/D 1 being read first, A/D 2 second, etc., through A/D 7 which would have the lowest priority for data being read. Only the converters whose INT is asserted will be read.

The key to decoding circuitry is the DM74LS373, 8-bit D type flip-flop. When the Z-80 acknowledges the interrupt, the program is vectored to a data input Z-80 subroutine. This subroutine will read a peripheral status word from the DM74LS373 which contains the logic state of the $\overline{INTR}$ outputs of all the converters. Each converter which initiates an interrupt will place a logic "0" in a unique bit position in the status word and the subroutine will determine the identity of the converter and execute a data read. An identifier word (which indicates which A/D the data came from) is stored in the next sequential memory location above the location of the data so the program can keep track of the identity of the data entered.

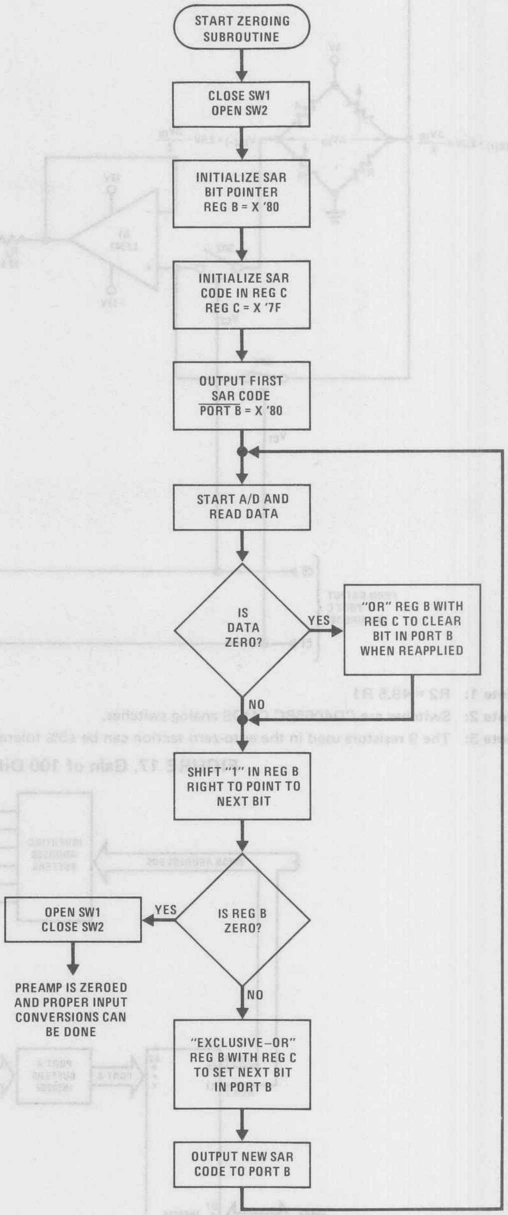


FIGURE 19. Flow Chart for Auto-Zero Routine

				; Initialize SAR bit pointer
3D0B	3E7F	MVI A 7F		; Initialize SAR code
3D0D	4F	MOV C,A	Return	
3D0E	D3E5	OUT B		; Port B = SAR code
3D10	31AA3D	LXI SP 3DAA	Start	; Dimension stack pointer
3D13	D3E4	OUT A		; Start A/D
3D15	FB	IE		
3D16	00	NOP	Loop	; Loop until $\overline{INT}$ asserted
3D17	C3163D	JMP Loop		
3D1A	7A	MOV A,D	Auto-Zero	
3D1B	C600	ADI 00		
3D1D	CA2D3D	JZ Set C		; Test A/D output data for zero
3D20	78	MOV A,B	Shift B	
3D21	F600	ORI 00		; Clear carry
3D23	1F	RAR		; Shift "1" in B right one place
3D24	FE00	CPI 00		; Is B zero? If yes last
3D26	CA373D	JZ Done		; approximation has been made
3D29	47	MOV B,A		
3D2A	C3333D	JMP New C		
3D2D	79	MOV A,C	Set C	
3D2E	B0	ORA B		; Set bit in C that is in same
3D2F	4F	MOV C,A		; position as "1" in B
3D30	C3203D	JMP Shift B		
3D33	A9	XRA C	New C	; Clear bit in C that is in
3D34	C30D3D	JMP Return		; same position as "1" in B
3D37	47	MOV B,A	Done	; then output new SAR code.
3D38	7C	MOV A,H		; Open SW1, close SW2 then
3D39	EE03	XRI 03		; proceed with program. Preamp
3D3B	D3E6	OUT C		; is now zeroed.
3D3D		.	Normal	
		.		
		.		
		Program for processing proper data values		
3C3D	DBE4	IN A	Read A/D Subroutine	; Read A/D data
3C3F	EEFF	XRI FF		; Invert data
3C41	57	MOV D,A		
3C42	78	MOV A,B		; Is B Reg = 0? If not stay
3C43	E6FF	ANI FF		; in auto zero subroutine
3C45	C21A3D	JNZ Auto-Zero		
3C48	C33D3D	JMP Normal		

Note: All numerical values are hexadecimal representations.

FIGURE 20. Software for Auto-Zeroed Differential A/D

5.3 Multiple A/D Converters in a Z-80 Interrupt Driven Mode (Continued)

The following notes apply:

1) It is assumed that the CPU automatically performs a RST 7 instruction when a valid interrupt is acknowledged (CPU is in interrupt mode 1). Hence, the subroutine starting address of X0038.

2) The address bus from the Z-80 and the data bus to the Z-80 are assumed to be inverted by bus drivers.

3) A/D data and identifying words will be stored in sequential memory locations starting at the arbitrarily chosen address X 3E00.

4) The stack pointer must be dimensioned in the main program as the RST 7 instruction automatically pushes the PC onto the stack and the subroutine uses an additional 6 stack addresses.

5) The peripherals of concern are mapped into I/O space with the following port assignments:

HEX PORT ADDRESS	PERIPHERAL
00	MM74C374 8-bit flip-flop
01	A/D 1
02	A/D 2
03	A/D 3
04	A/D 4
05	A/D 5
06	A/D 6
07	A/D 7

This port address also serves as the A/D identifying word in the program.

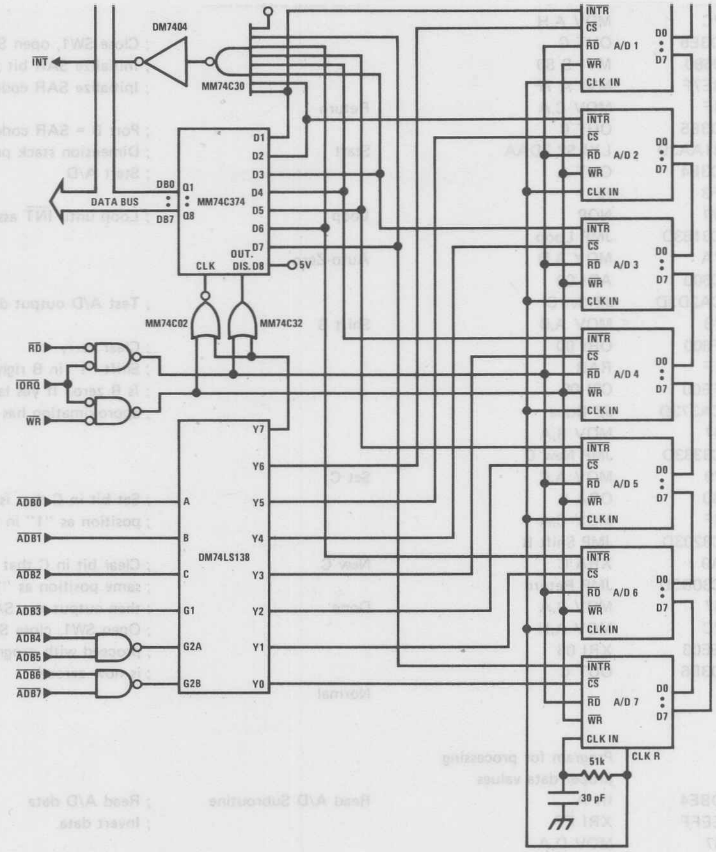


FIGURE 21. Multiple A/Ds with Z-80 Type Microprocessor

INTERRUPT SERVICING SUBROUTINE

LOC	OBJ CODE		SOURCE STATEMENT	COMMENT
0038	E5		PUSH HL	; Save contents of all registers affected by
0039	C5		PUSH BC	; this subroutine.
003A	F5		PUSH AF	; Assumed INT mode 1 earlier set.
003B	21 00 3E		LD (HL),X3E00	; Initialize memory pointer where data will be stored.
003E	0E 01		LD C,X01	; C register will be port ADDR of A/D converters.
0040	D300		OUT X00,A	; Load peripheral status word into 8-bit latch.
0042	DB00		IN A, X00	; Load status word into accumulator.
0044	47		LD B,A	; Save the status word.
0045	79	TEST	LD A,C	; Test to see if the status of all A/D's have
0046	FE 08		CP, X08	; been checked. If so, exit subroutine.
0048	CA 60 00		JPZ, DONE	
004B	78		LD A,B	; Test a single bit in status word by looking for
004C	1F		RRA	; a "1" to be rotated into the CARRY (an INT
004D	47		LD B,A	; is loaded as a "1"). If CARRY is set then load
004E	DA 5500		JPC, LOAD	; contents of A/D at port ADDR in C register.
0051	0C	NEXT	INC C	; If CARRY is not set, increment C register to point
0052	C3 4500		JP,TEST	; to next A/D, then test next bit in status word.
0055	ED 78	LOAD	IN A, (C)	; Read data from interrupting A/D and invert
0057	EE FF		XOR FF	; the data.
0059	77		LD (HL),A	; Store the data.
005A	2C		INC L	
005B	71		LD (HL),C	; Store A/D identifier (A/D port ADDR).
005C	2C		INC L	
005D	C3 51 00		JP,NEXT	; Test next bit in status word.
0060	F1	DONE	POP AF	; Re-establish all registers as they were
0061	C1		POP BC	; before the interrupt.
0062	E1		POP HL	
0063	C9		RET	; Return to original program.

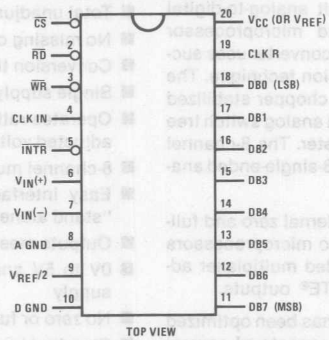
Ordering Information

TEMPERATURE RANGE		0°C TO 70°C	−40°C TO +85°C	−40°C TO +85°C	−55°C TO +125°C
ERROR	±1/4 Bit Adjusted		ADC0801LCN	ADC0801LCD	ADC0801LD
	±1/2 Bit Unadjusted		ADC0802LCN	ADC0802LCD	ADC0802LD
	±1/2 Bit Adjusted		ADC0803LCN	ADC0803LCD	
	±1 Bit Unadjusted	ADC0804LCN	ADC0805LCN	ADC0804LCD	
PACKAGE OUTLINE		N20A–MOLDED DIP		D20A–CAVITY DIP	D20A–CAVITY DIP

Connection Diagram

ADC080X

Dual-In-Line Package



National Semiconductor

ADC0808, ADC0809 8-Bit μP Compatible A/D Converters With 8-Channel Multiplexer

General Description

The ADC0808, ADC0809 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 8-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 8-channel multiplexer can directly access any of 8-single-ended analog signals.

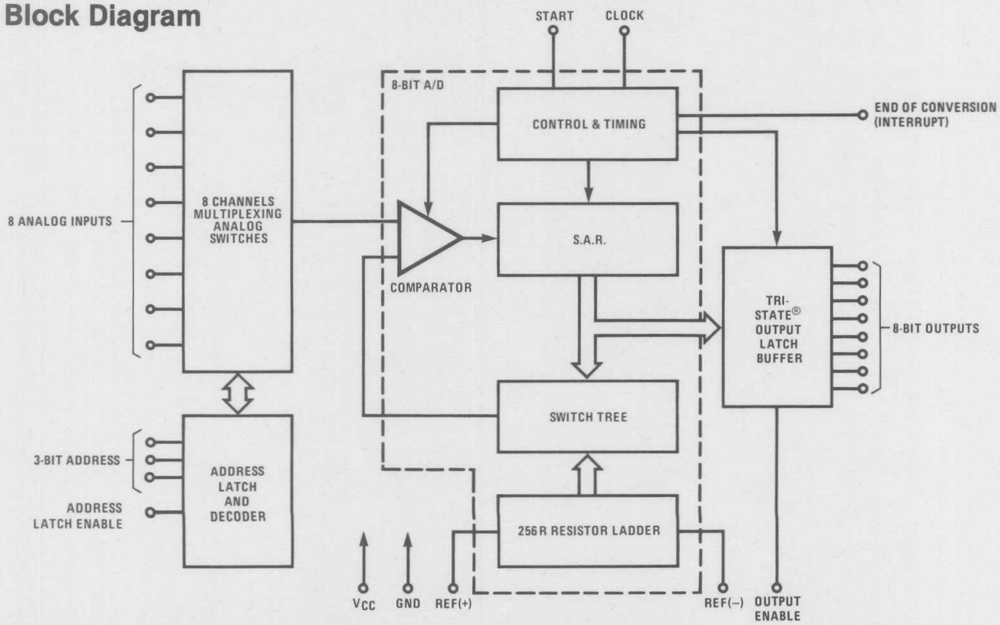
The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE® outputs.

The design of the ADC0808, ADC0809 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0808, ADC0809 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications. For 16-channel multiplexer with common output (sample/hold port) see ADC0816 data sheet. (See AN-247 for more information.

Features

- Resolution — 8-bits
- Total unadjusted error — ± 1/2 LSB and ± 1 LSB
- No missing codes
- Conversion time — 100 μs
- Single supply — 5 V_{DC}
- Operates ratiometrically or with 5 V_{DC} or analog span adjusted voltage reference
- 8-channel multiplexer with latched control logic
- Easy interface to all microprocessors, or operates "stand alone"
- Outputs meet T^2L voltage level specifications
- 0V to 5V analog input voltage range with single 5V supply
- No zero or full-scale adjust required
- Standard hermetic or molded 28-pin DIP package
- Temperature range −40°C to +85°C or −55°C to +125°C
- Low power consumption — 15 mW
- Latched TRI-STATE® output

Block Diagram



Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage at Any Pin Except Control Inputs	−0.3V to (V_{CC} + 0.3V)
Voltage at Control Inputs (START, OE, CLOCK, ALE, ADD A, ADD B, ADD C)	−0.3V to +15V
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A = 25°C	875 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Ratings (Notes 1 and 2)

Temperature Range (Note 1)	$T_{MIN} \le T_A \le T_{MAX}$
ADC0808CJ	$-55°C \le T_A \le +125°C$
ADC0808CCJ, ADC0808CCN, ADC0809CCN	$-40°C \le T_A \le +85°C$
Range of V_{CC} (Note 1)	4.5 V_{DC} to 6.0 V_{DC}

Electrical Characteristics

Converter Specifications: $V_{CC} = 5\ V_{DC} = V_{REF(+)}$, $V_{REF(-)}$ = GND, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK} = 640 kHz unless otherwise stated.

	Parameter	Conditions	Min	Typ	Max	Units
	ADC0808					
	Total Unadjusted Error	25°C			±1/2	LSB
	(Note 5)	T_{MIN} to T_{MAX}			±3/4	LSB
	ADC0809					
	Total Unadjusted Error	0°C to 70°C			±1	LSB
	(Note 5)	T_{MIN} to T_{MAX}			±1 1/4	LSB
	Input Resistance	From Ref(+) to Ref(−)	1.0	2.5		kΩ
	Analog Input Voltage Range	(Note 4) V(+) or V(−)	GND−0.10		V_{CC}+0.10	V_{DC}
$V_{REF(+)}$	Voltage, Top of Ladder	Measured at Ref(+)		V_{CC}	V_{CC}+0.1	V
$\frac{V_{REF(+)}+V_{REF(-)}}{2}$	Voltage, Center of Ladder		V_{CC}/2−0.1	V_{CC}/2	V_{CC}/2+0.1	V
$V_{REF(-)}$	Voltage, Bottom of Ladder	Measured at Ref(−)	−0.1	0		V
	Comparator Input Current	f_c = 640 kHz, (Note 6)	−2	±0.5	2	μA

Electrical Characteristics

Digital Levels and DC Specifications: ADC0808CJ $4.5V \le V_{CC} \le 5.5V$, $-55°C \le T_A \le +125°C$ unless otherwise noted ADC0808CCJ, ADC0808CCN, and ADC0809CCN $4.75 \le V_{CC} \le 5.25V$, $-40°C \le T_A \le +85°C$ unless otherwise noted

	Parameter	Conditions	Min	Typ	Max	Units
ANALOG MULTIPLEXER						
$I_{OFF(+)}$	OFF Channel Leakage Current	V_{CC} = 5V, V_{IN} = 5V, T_A = 25°C		10	200	nA
		T_{MIN} to T_{MAX}			1.0	μA
$I_{OFF(-)}$	OFF Channel Leakage Current	V_{CC} = 5V, V_{IN} = 0, T_A = 25°C	−200	−10		nA
		T_{MIN} to T_{MAX}	−1.0			μA
CONTROL INPUTS						
$V_{IN(1)}$	Logical "1" Input Voltage		V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$I_{IN(1)}$	Logical "1" Input Current (The Control Inputs)	V_{IN} = 15V			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (The Control Inputs)	V_{IN} = 0	−1.0			μA
I_{CC}	Supply Current	f_{CLK} = 640 kHz		0.3	3.0	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DATA OUTPUTS AND EOC (INTERRUPT)						
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_O = -360\ \mu A$	V_{CC}-0.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_O = 1.6$ mA			0.45	V
$V_{OUT(0)}$	Logical "0" Output Voltage EOC	$I_O = 1.2$ mA			0.45	V
I_{OUT}	TRI-STATE® Output Current	$V_O = 5V$			3	μA
		$V_O = 0$	−3			μA

Electrical Characteristics

Timing Specifications: $V_{CC} = V_{REF(+)} = 5V$, $V_{REF(-)} = GND$, $t_r = t_f = 20$ ns and $T_A = 25°C$ unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{WS}	Minimum Start Pulse Width	*(Figure 5)*		100	200	ns
t_{WALE}	Minimum ALE Pulse Width	*(Figure 5)*		100	200	ns
t_s	Minimum Address Set-Up Time	*(Figure 5)*		25	50	ns
t_H	Minimum Address Hold Time	*(Figure 5)*		25	50	ns
t_D	Analog MUX Delay Time From ALE	$R_S = 0\Omega$ *(Figure 5)*		1	2.5	μs
t_{H1}, t_{H0}	OE Control to Q Logic State	$C_L = 50$ pF, $R_L = 10k$ *(Figure 8)*		125	250	ns
t_{1H}, t_{0H}	OE Control to Hi-Z	$C_L = 10$ pF, $R_L = 10k$ *(Figure 8)*		125	250	ns
t_c	Conversion Time	$f_c = 640$ kHz, *(Figure 5)* (Note 7)	90	100	116	μs
f_c	Clock Frequency		10	640	1280	kHz
t_{EOC}	EOC Delay Time	*(Figure 5)*	0		$8 + 2\ \mu s$	Clock Periods
C_{IN}	Input Capacitance	At Control Inputs		10	15	pF
C_{OUT}	TRI-STATE® Output Capacitance	At TRI-STATE® Outputs, (Note 12)		10	15	pF

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: A zener diode exists, internally, from V_{CC} to GND and has a typical breakdown voltage of 7 V_{DC}.

Note 4: Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. The spec allows 100 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 100 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.900 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors. See *Figure 3*. None of these A/Ds requires a zero or full-scale adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.5V full-scale) the reference voltages can be adjusted to achieve this. See *Figure 13*.

Note 6: Comparator input current is a bias current into or out of the chopper stabilized comparator. The bias current varies directly with clock frequency and has little temperature dependence *(Figure 6)*. See paragraph 4.0.

Note 7: The outputs of the data register are updated one clock cycle before the rising edge of EOC.

Functional Description

Multiplexer: The device contains an 8-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. Table I shows the input states for the address lines to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

TABLE I

SELECTED ANALOG CHANNEL	ADDRESS LINE C	ADDRESS LINE B	ADDRESS LINE A
IN0	L	L	L
IN1	L	L	H
IN2	L	H	L
IN3	L	H	H
IN4	H	L	L
IN5	H	L	H
IN6	H	H	L
IN7	H	H	H

CONVERTER CHARACTERISTICS

The Converter

The heart of this single chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections: the 256R ladder network, the successive approximation register, and the comparator. The converter's digital outputs are positive true.

The 256R ladder network approach *(Figure 1)* was chosen over the conventional R/2R ladder because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage.

The bottom resistor and the top resistor of the ladder network in *Figure 1* are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached +1/2 LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. *Figure 2* shows a typical example of a 3-bit converter. In the ADC0808, ADC0809, the approximation technique is extended to 8 bits using the 256R network.

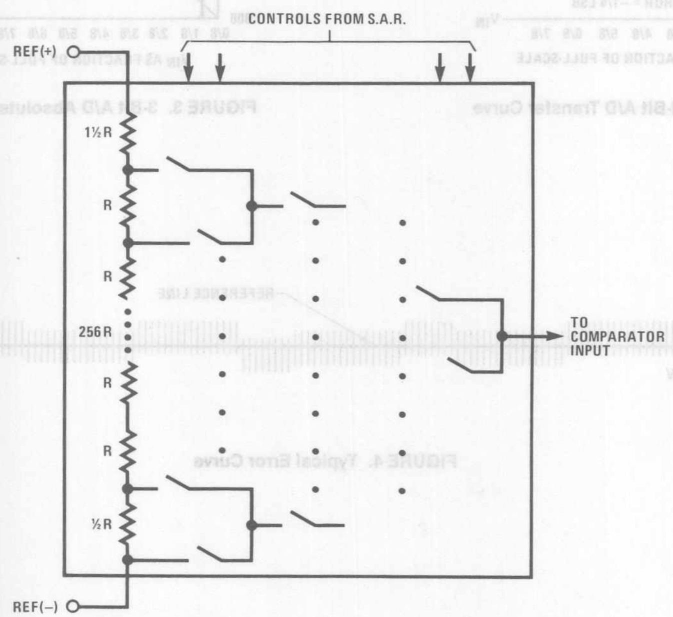


FIGURE 1. Resistor Ladder and Switch Tree

Functional Description (Continued)

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion (SC) pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 0 and 8 clock pulses after the rising edge of start conversion.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on the repeatability of the device. A chopper-stabilized comparator provides the most effective method of satisfying all the converter requirements.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed through a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

Figure 4 shows a typical error curve for the ADC0808 as measured using the procedures outlined in AN-179.

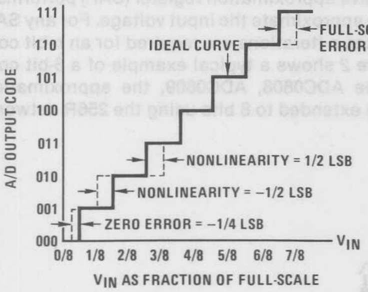


FIGURE 2. 3-Bit A/D Transfer Curve

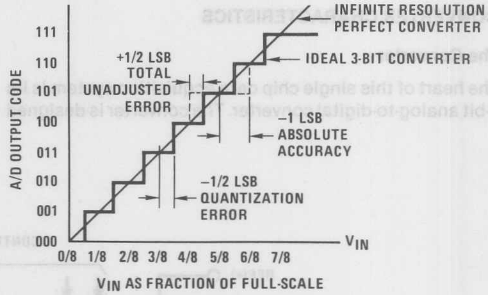


FIGURE 3. 3-Bit A/D Absolute Accuracy Curve

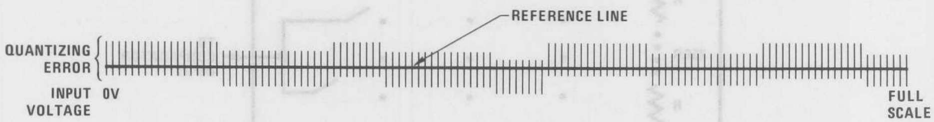
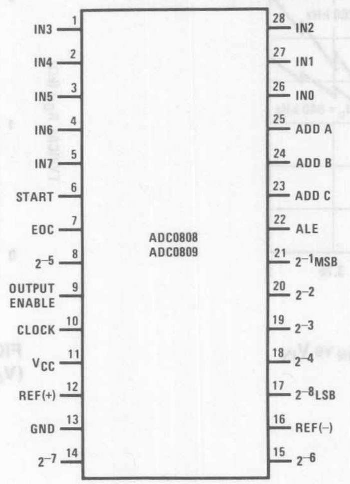


FIGURE 4. Typical Error Curve

Connection Diagram

Dual-In-Line Package



TOP VIEW

Timing Diagram

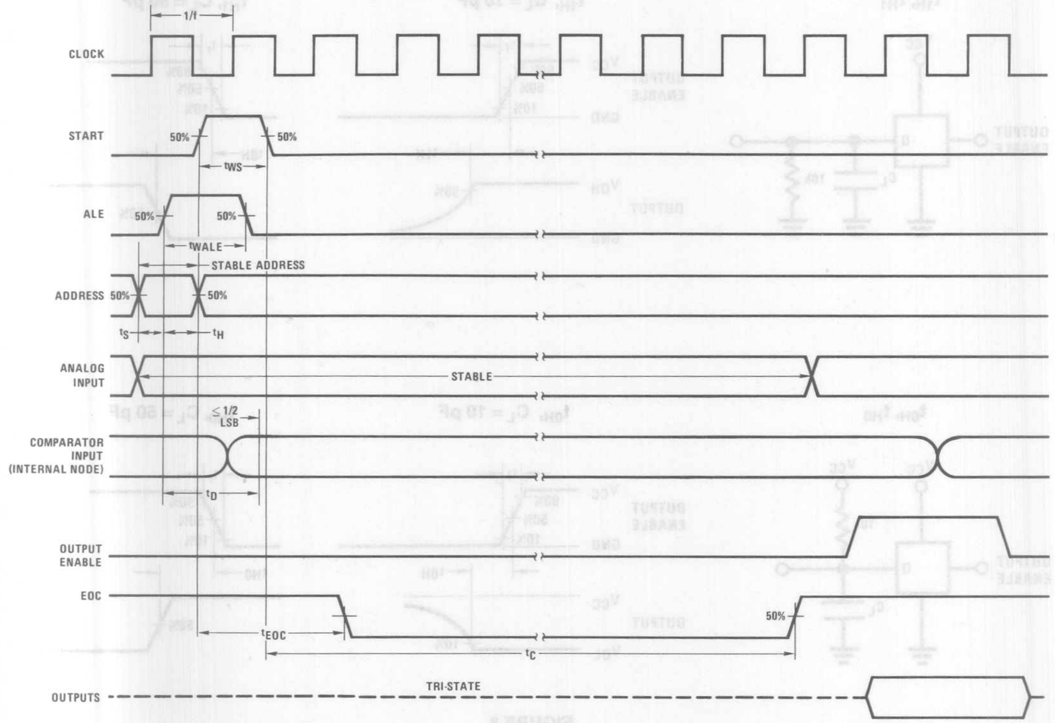


FIGURE 5

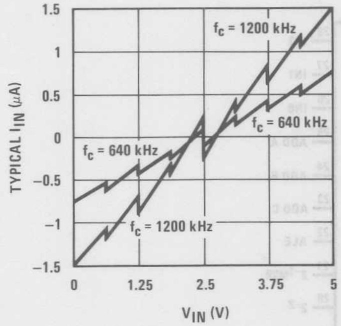


FIGURE 6. Comparator I_{IN} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

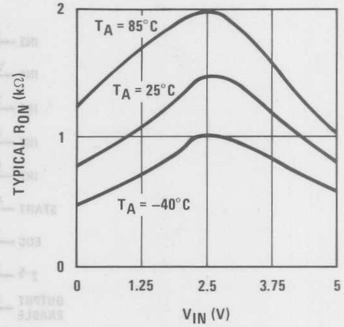


FIGURE 7. Multiplexer R_{ON} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

TRI-STATE® Test Circuits and Timing Diagrams

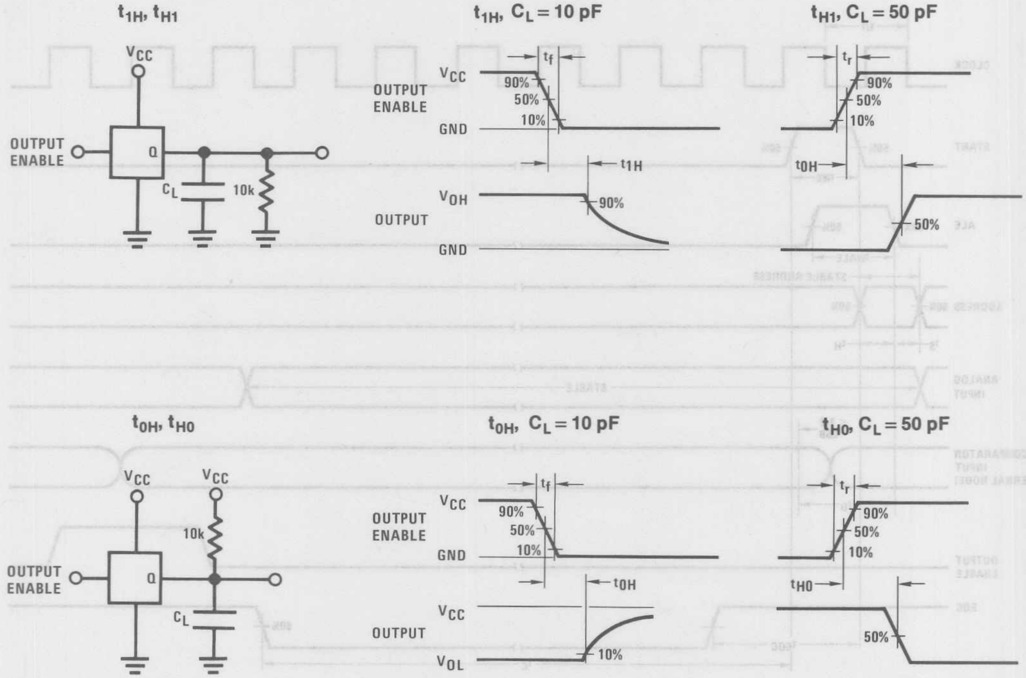


FIGURE 8

Applications Information

OPERATION

1.0 Ratiometric Conversion

The ADC0808, ADC0809 is designed as a complete Data Acquisition System (DAS) for ratiometric conversion systems. In ratiometric systems, the physical variable being measured is expressed as a percentage of full-scale which is not necessarily related to an absolute standard. The voltage input to the ADC0808 is expressed by the equation

$$\frac{V_{IN}}{V_{fs} - V_Z} = \frac{D_X}{D_{MAX} - D_{MIN}} \tag{1}$$

V_{IN} = Input voltage into the ADC0808

V_{fs} = Full-scale voltage

V_Z = Zero voltage

D_X = Data point being measured

D_{MAX} = Maximum data limit

D_{MIN} = Minimum data limit

A good example of a ratiometric transducer is a potentiometer used as a position sensor. The position of the wiper is directly proportional to the output voltage which is a ratio of the full-scale voltage across it. Since the data is represented as a proportion of full-scale, reference requirements are greatly reduced, eliminating a large source of error and cost for many applications. A major advantage of the ADC0808, ADC0809 is that the input voltage range is equal to the supply range so the transducers can be connected directly across the supply and their outputs connected directly into the multiplexer inputs, *(Figure 9)*.

Ratiometric transducers such as potentiometers, strain gauges, thermistor bridges, pressure transducers, etc., are suitable for measuring proportional relationships; however, many types of measurements must be referred to an absolute standard such as voltage or current. This means a system reference must be used which relates the full-scale voltage to the standard volt. For example, if $V_{CC} = V_{REF} = 5.12V$, then the full-scale range is divided into 256 standard steps. The smallest standard step is 1 LSB which is then 20 mV.

2.0 Resistor Ladder Limitations

The voltages from the resistor ladder are compared to the selected input 8 times in a conversion. These voltages are coupled to the comparator via an analog switch tree which is referenced to the supply. The voltages at the top, center and bottom of the ladder must be controlled to maintain proper operation.

The top of the ladder, Ref(+), should not be more positive than the supply, and the bottom of the ladder, Ref(−), should not be more negative than ground. The center of the ladder voltage must also be near the center of the supply because the analog switch tree changes from N-channel switches to P-channel switches. These limitations are automatically satisfied in ratiometric systems and can be easily met in ground referenced systems.

Figure 10 shows a ground referenced system with a separate supply and reference. In this system, the supply must be trimmed to match the reference voltage. For instance, if a 5.12V is used, the supply should be adjusted to the same voltage within 0.1V.

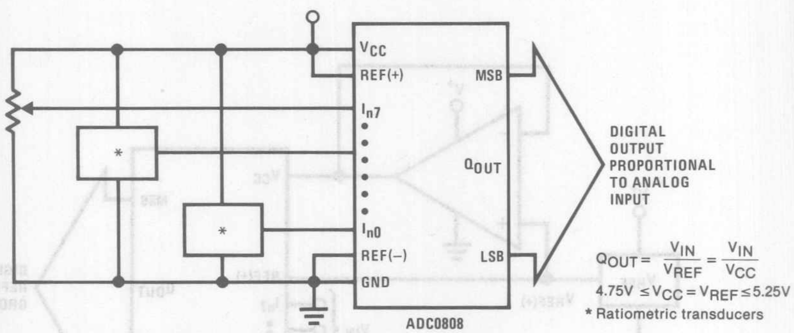


FIGURE 9. Ratiometric Conversion System

Applications Information (Continued)

The ADC0808 needs less than a milliamp of supply current so developing the supply from the reference is readily accomplished. In *Figure 11* a ground referenced system is shown which generates the supply from the reference. The buffer shown can be an op amp of sufficient drive to supply the milliamp of supply current and the desired bus drive, or if a capacitive bus is driven by the outputs a large capacitor will supply the transient supply current as seen in *Figure 12*. The LM301 is overcompensated to insure stability when loaded by the 10 μF output capacitor.

The top and bottom ladder voltages cannot exceed V_{CC} and ground, respectively, but they can be symmetrically less than V_{CC} and greater than ground. The center of the ladder voltage should always be near the center of the supply. The sensitivity of the converter can be increased, (i.e., size of the LSB steps decreased) by using a symmetrical reference system. In *Figure 13*, a 2.5V reference is symmetrically centered about $V_{CC}/2$ since the same current flows in identical resistors. This system with a 2.5V reference allows the LSB bit to be half the size of a 5V reference system.

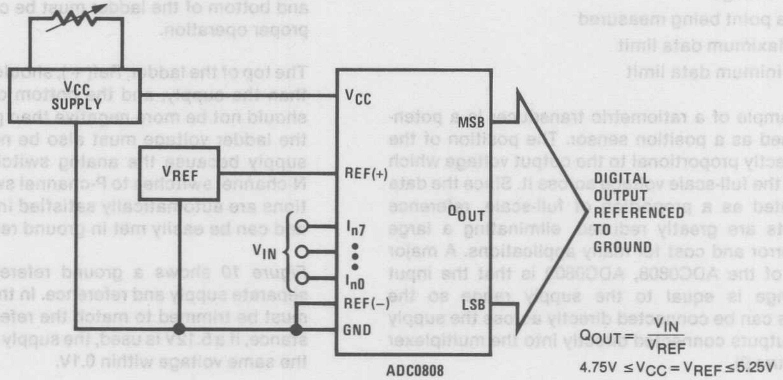


FIGURE 10. Ground Referenced Conversion System Using Trimmed Supply

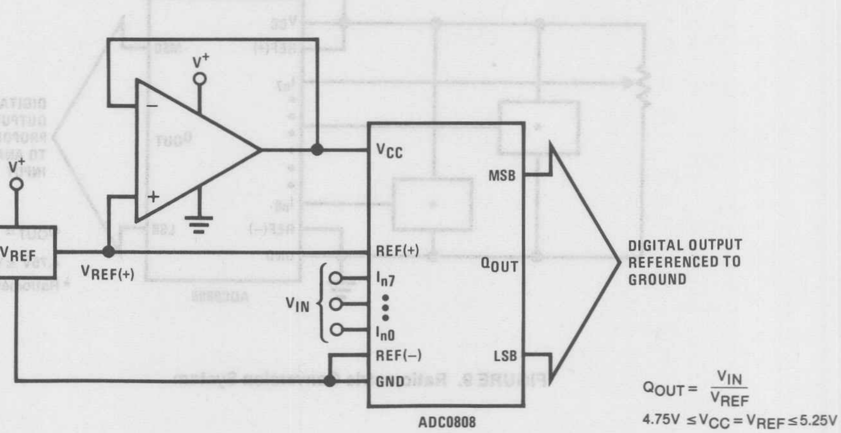


FIGURE 11. Ground Referenced Conversion System with Reference Generating V_{CC} Supply

Applications Information (Continued)

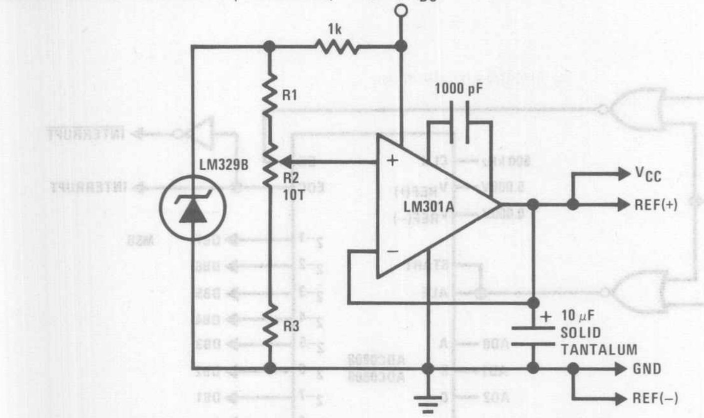


FIGURE 12. Typical Reference and Supply Circuit

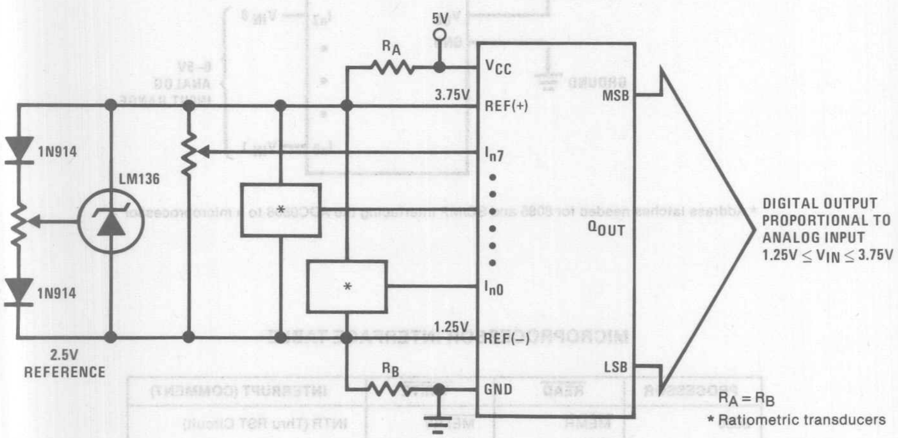


FIGURE 13. Symmetrically Centered Reference

3.0 Converter Equations

The transition between adjacent codes N and N+1 is given by:

$$V_{IN} = \left\{ (V_{REF(+)} - V_{REF(-)}) \left[\frac{N}{256} + \frac{1}{512} \right] \pm V_{TUE} \right\} + V_{REF(-)} \qquad (2)$$

The center of an output code N is given by:

$$V_{IN} = \left\{ (V_{REF(+)} - V_{REF(-)}) \left[\frac{N}{256} \right] \pm V_{TUE} \right\} + V_{REF(-)} \qquad (3)$$

The output code N for an arbitrary input are the integers within the range:

$$N = \frac{V_{IN} - V_{REF(-)}}{V_{REF(+)} - V_{REF(-)}} \times 256 \pm \text{Absolute Accuracy} \qquad (4)$$

where: V_{IN} = Voltage at comparator input
$V_{REF(+)}$ = Voltage at Ref(+)
$V_{REF(-)}$ = Voltage at Ref(−)
V_{TUE} = Total unadjusted error voltage (typically $V_{REF(+)} \div 512$)

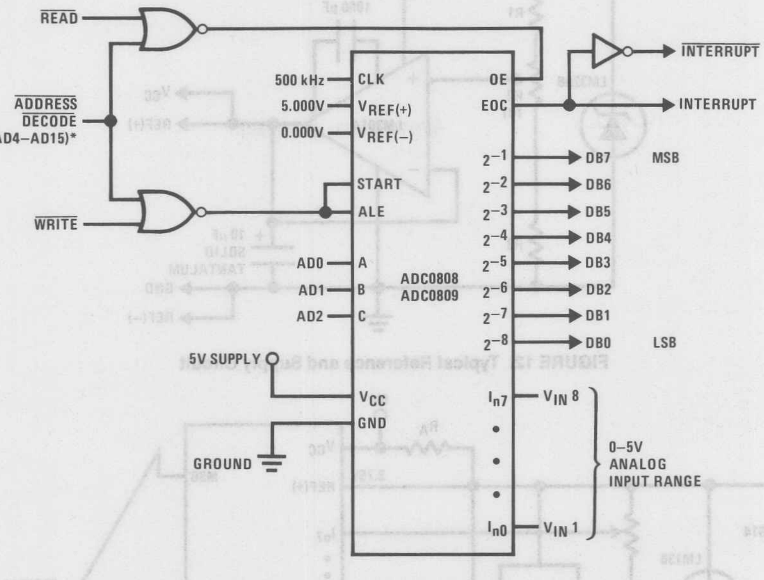
4.0 Analog Comparator Inputs

The dynamic comparator input current is caused by the periodic switching of on-chip stray capacitances. These are connected alternately to the output of the resistor ladder/switch tree network and to the comparator input as part of the operation of the chopper stabilized comparator.

The average value of the comparator input current varies directly with clock frequency and with V_{IN} as shown in *Figure 6.*

If no filter capacitors are used at the analog inputs and the signal source impedances are low, the comparator input current should not introduce converter errors, as the transient created by the capacitance discharge will die out before the comparator output is strobed.

If input filter capacitors are desired for noise reduction and signal conditioning they will tend to average out the dynamic comparator input current. It will then take on the characteristics of a DC bias current whose effect can be predicted conventionally.



* Address latches needed for 8085 and SC/MP interfacing the ADC0808 to a microprocessor

MICROPROCESSOR INTERFACE TABLE

PROCESSOR	$\overline{\text{READ}}$	$\overline{\text{WRITE}}$	INTERRUPT (COMMENT)
8080	$\overline{\text{MEMR}}$	$\overline{\text{MEMW}}$	INTR (Thru RST Circuit)
8085	$\overline{\text{RD}}$	$\overline{\text{WR}}$	INTR (Thru RST Circuit)
Z-80	$\overline{\text{RD}}$	$\overline{\text{WR}}$	$\overline{\text{INT}}$ (Thru RST Circuit, Mode 0)
SC/MP	NRDS	NWDS	SA (Thru Sense A)
6800	VMA·ϕ2·R/W	VMA·ϕ2·$\overline{\text{R/W}}$	$\overline{\text{IRQA}}$ or $\overline{\text{IRQB}}$ (Thru PIA)

Ordering Information

TEMPERATURE RANGE		−40°C to +85°C		−55°C to +125°C
Error	± 1/2 Bit Unadjusted	ADC0808CCN	ADC0808CCJ	ADC0808CJ
	± 1 Bit Unadjusted	ADC0809CCN		
Package Outline		N28A Molded DIP	J28A Hermetic DIP	J28A Hermetic DIP

National Semiconductor

A to D, D to A

ADC0816, ADC0817 8-Bit μP Compatible A/D Converters with 16-Channel Multiplexer

General Description

The ADC0816, ADC0817 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 16-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 16-channel multiplexer can directly access any one of 16-single-ended analog signals, and provides the logic for additional channel expansion. Signal conditioning of any analog input signal is eased by direct access to the multiplexer output, and to the input of the 8-bit A/D converter.

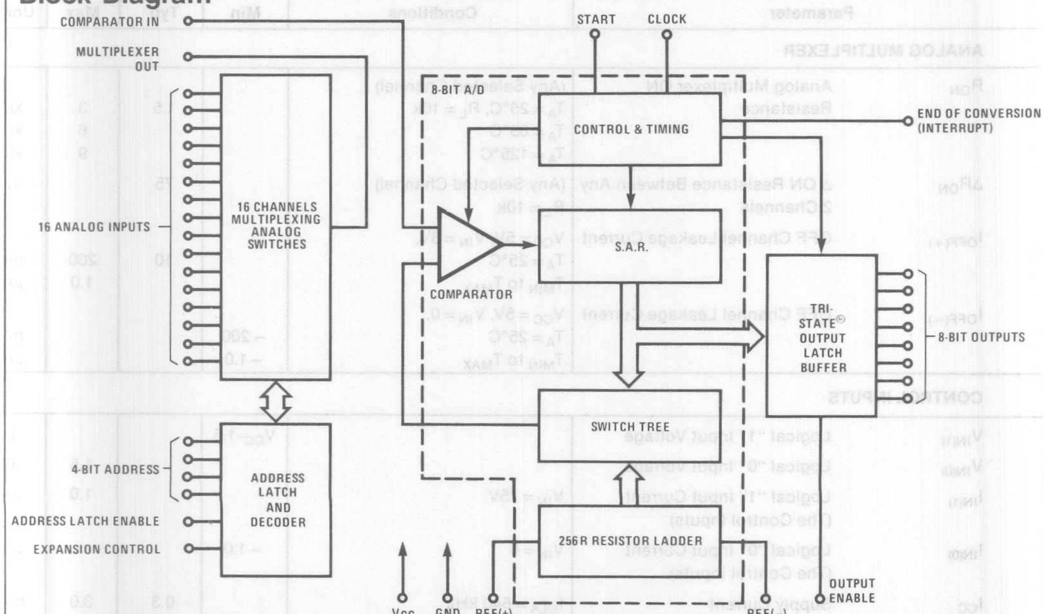
The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE® outputs.

The design of the ADC0816, ADC0817 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0816, ADC0817 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications. For similar performance in an 8-channel, 28-pin, 8-bit A/D converter, see the ADC0808, ADC0809 data sheet. (See AN-258 for more information.)

Features

- Resolution — 8-bits
- Total unadjusted error — ± 1/2 LSB and ± 1 LSB
- No missing codes
- Conversion time — 100 μs
- Single supply — 5 V_{DC}
- Operates ratiometrically or with 5 V_{DC} or analog span adjusted voltage reference
- 16-channel multiplexer with latched control logic
- Easy interface to all microprocessors, or operates "stand alone"
- Outputs meet T^2L voltage level specifications
- 0V to 5V analog input voltage range with single 5V supply
- No zero or full-scale adjust required
- Standard hermetic or molded 40-pin DIP package
- Temperature range −40°C to +85°C or −55°C to +125°C
- Low power consumption — 15 mW
- Latched TRI-STATE® output
- Direct access to "comparator in" and "multiplexer out" for signal conditioning

Block Diagram



Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage at Any Pin Except Control Inputs	−0.3V to (V_{CC} + 0.3V)
Voltage at Control Inputs (START, OE, CLOCK, ALE, EXPANSION CONTROL, ADD A, ADD B, ADD C, ADD D)	−0.3V to 15V
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A = 25°C	875 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Ratings (Notes 1 and 2)

Temperature Range (Note 1)	$T_{MIN} \le T_A \le T_{MAX}$
ADC0816CJ	$-55°C \le T_A \le +125°C$
ADC0816CCJ, ADC0816CCN, ADC0817CCN	$-40°C \le T_A \le +85°C$
Range of V_{CC} (Note 1)	4.5 V_{DC} to 6.0 V_{DC}
Voltage at Any Pin Except Control Inputs	0V to V_{CC}
Voltage at Control Inputs (START, OE, CLOCK, ALE, EXPANSION CONTROL, ADD A, ADD B, ADD C, ADD D)	0V to 15V

Electrical Characteristics

Converter Specifications: $V_{CC} = 5\ V_{DC} = V_{REF(+)}$, $V_{REF(-)}$ = GND, $V_{IN} = V_{COMPARATOR\ IN}$, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK} = 640 kHz unless otherwise stated.

	Parameter	Conditions	Min	Typ	Max	Units
	ADC0816 Total Unadjusted Error (Note 5)	25°C			±1/2	LSB
		T_{MIN} to T_{MAX}			±3/4	LSB
	ADC0817 Total Unadjusted Error (Note 5)	0°C to 70°C			±1	LSB
		T_{MIN} to T_{MAX}			±1 1/4	LSB
	Input Resistance	From Ref(+) to Ref(−)	1.0	4.5		kΩ
	Analog Input Voltage Range	(Note 4) V(+) or V(−)	GND−0.10		V_{CC}+0.10	V_{DC}
$V_{REF(+)}$	Voltage, Top of Ladder	Measured at Ref(+)		V_{CC}	V_{CC}+0.1	V
$\frac{V_{REF(+)}+V_{REF(-)}}{2}$	Voltage, Center of Ladder		V_{CC}/2−0.1	V_{CC}/2	V_{CC}/2+0.1	V
$V_{REF(-)}$	Voltage, Bottom of Ladder	Measured at Ref(−)	−0.1	0		V
	Comparator Input Current	f_c = 640 kHz, (Note 6)	−2	±0.5	2	μA

Electrical Characteristics

Digital Levels and DC Specifications: ADC0816CJ $4.5V \le V_{CC} \le 5.5V$, $-55°C \le T_A \le +125°C$ unless otherwise noted. ADC0816CCJ, ADC0816CCN, ADC0817CCN $4.75V \le V_{CC} \le 5.25V$, $-40°C \le T_A \le +85°C$ unless otherwise noted.

	Parameter	Conditions	Min	Typ	Max	Units
ANALOG MULTIPLEXER						
R_{ON}	Analog Multiplexer ON Resistance	(Any Selected Channel) T_A = 25°C, R_L = 10k		1.5	3	kΩ
		T_A = 85°C			6	kΩ
		T_A = 125°C			9	kΩ
ΔR_{ON}	Δ ON Resistance Between Any 2 Channels	(Any Selected Channel) R_L = 10k		75		Ω
$I_{OFF(+)}$	OFF Channel Leakage Current	V_{CC} = 5V, V_{IN} = 5V, T_A = 25°C		10	200	nA
		T_{MIN} to T_{MAX}			1.0	μA
$I_{OFF(-)}$	OFF Channel Leakage Current	V_{CC} = 5V, V_{IN} = 0, T_A = 25°C	−200			nA
		T_{MIN} to T_{MAX}	−1.0			μA
CONTROL INPUTS						
$V_{IN(1)}$	Logical "1" Input Voltage		V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$I_{IN(1)}$	Logical "1" Input Current (The Control Inputs)	V_{IN} = 15V			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (The Control Inputs)	V_{IN} = 0	−1.0			μA
I_{CC}	Supply Current	f_{CLK} = 640 kHz		0.3	3.0	mA

Electrical Characteristics (Continued)

Digital Levels and DC Specifications: ADC0816CJ — 4.5V ⩽ V_{CC} ⩽ 5.5V, −55°C ⩽ T_A ⩽ +125°C unless otherwise noted. ADC0816CCJ, ADC0816CCN, ADC0817CCN — 4.75V ⩽ V_{CC} ⩽ 5.25V, −40°C ⩽ T_A ⩽ +85°C unless otherwise noted.

	Parameter	Conditions	Min.	Typ.	Max.	Units
DATA OUTPUTS AND EOC (INTERRUPT)						
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_O = -360\mu A$, $T_A = 85°C$ $I_O = -300\mu A$, $T_A = 125°C$	$V_{CC} - 0.4$			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_O = 1.6 mA$			0.45	V
$V_{OUT(0)}$	Logical "0" Output Voltage EOC	$I_O = 1.2 mA$			0.45	V
I_{OUT}	TRI-STATE® Output Current	$V_O = V_{CC}$ $V_O = 0$	 −3.0		3.0	µA µA

Electrical Characteristics

Timing Specifications: $V_{CC} = V_{REF(+)} = 5V$, $V_{REF(-)} = GND$, $t_r = t_f = 20$ ns and $T_A = 25°C$ unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{WS}	Minimum Start Pulse Width	*(Figure 5)*		100	200	ns
t_{WALE}	Minimum ALE Pulse Width	*(Figure 5)*		100	200	ns
t_s	Minimum Address Set-Up Time	*(Figure 5)*		25	50	ns
t_H	Minimum Address Hold Time	*(Figure 5)*		25	50	ns
t_D	Analog MUX Delay Time From ALE	$R_S = 0\Omega$ *(Figure 5)*		1	2.5	µs
t_{H1}, t_{H0}	OE Control to Q Logic State	$C_L = 50$ pF, $R_L = 10k$ *(Figure 8)*		125	250	ns
t_{1H}, t_{0H}	OE Control to Hi-Z	$C_L = 10$ pF, $R_L = 10k$ *(Figure 8)*		125	250	ns
t_c	Conversion Time	$f_c = 640$ kHz, *(Figure 5)* (Note 7)	90	100	116	µs
f_c	Clock Frequency		10	640	1280	kHz
t_{EOC}	EOC Delay Time	*(Figure 5)*	0		8 + 2 µs	Clock Periods
C_{IN}	Input Capacitance	At Control Inputs		10	15	pF
C_{OUT}	TRI-STATE® Output Capacitance	At TRI-STATE Outputs. (Note 7)		10	15	pF

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: A zener diode exists, internally, from V_{CC} to GND and has a typical breakdown voltage of 7 V_{DC}.

Note 4: Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. The spec allows 100 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 100 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.900 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Total unadjusted error includes offset, full-scale, and linearity errors. See *Figure 3*. None of these A/Ds requires a zero or full-scale adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.5V full-scale) the reference voltages can be adjusted to achieve this. See *Figure 13*.

Note 6: Comparator input current is a bias current into or out of the chopper stabilized comparator. The bias current varies directly with clock frequency and has little temperature dependence *(Figure 6)*. See paragraph 4.0.

Note 7: The outputs of the data register are updated one clock cycle before the rising edge of EOC.

Functional Description

Multiplexer: The device contains a 16-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. Table I shows the input states for the address line and the expansion control line to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

TABLE I

SELECTED ANALOG CHANNEL	ADDRESS LINE D	C	B	A	EXPANSION CONTROL
IN0	L	L	L	L	H
IN1	L	L	L	H	H
IN2	L	L	H	L	H
IN3	L	L	H	H	H
IN4	L	H	L	L	H
IN5	L	H	L	H	H
IN6	L	H	H	L	H
IN7	L	H	H	H	H
IN8	H	L	L	L	H
IN9	H	L	L	H	H
IN10	H	L	H	L	H
IN11	H	L	H	H	H
IN12	H	H	L	L	H
IN13	H	H	L	H	H
IN14	H	H	H	L	H
IN15	H	H	H	H	H
All Channels OFF	X	X	X	X	L

X = don't care

Additional single-ended analog signals can be multiplexed to the A/D converter by disabling all the multiplexer inputs using the expansion control. The additional external signals are connected to the comparator input and the device ground. Additional signal conditioning (i.e., prescaling, sample and hold, instrumentation amplification, etc.) may also be added between the analog input signal and the comparator input.

CONVERTER CHARACTERISTICS

The Converter

The heart of this single chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections: the 256R ladder network, the successive approximation register, and the comparator. The converter's digital outputs are positive true.

The 256R ladder network approach *(Figure 1)* was chosen over the conventional R/2R ladder because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage.

The bottom resistor and the top resistor of the ladder network in *Figure 1* are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached +1/2 LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

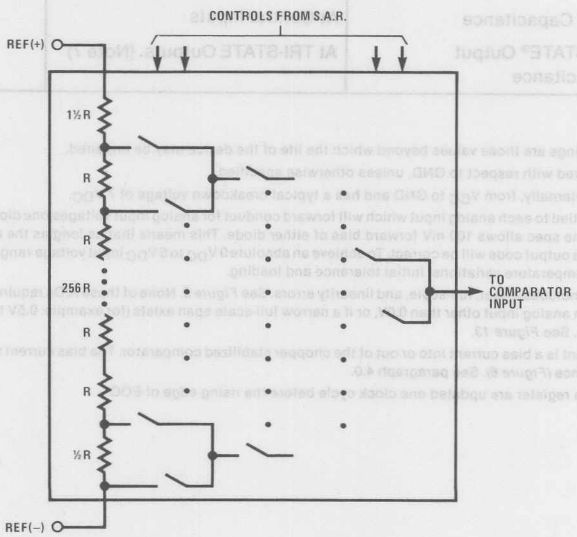


FIGURE 1. Resistor Ladder and Switch Tree

Functional Description (Continued)

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. *Figure 2* shows a typical example of a 3-bit converter. In the ADC0816, ADC0817, the approximation technique is extended to 8 bits using the 256R network.

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion (SC) pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 0 and 8 clock pulses after the rising edge of start conversion.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on the repeatability of the device. A chopper-stabilized comparator provides the most effective method of satisfying all the converter requirements.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed through a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

Figure 4 shows a typical error curve for the ADC0816 as measured using the procedures outlined in AN-179.

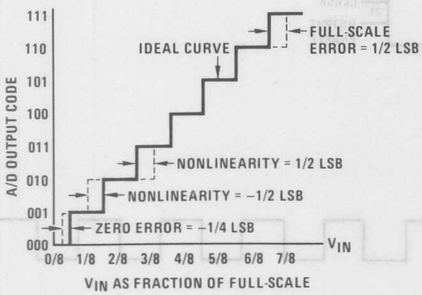


FIGURE 2. 3-Bit A/D Transfer Curve

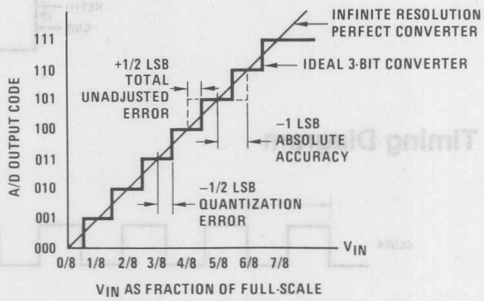


FIGURE 3. 3-Bit A/D Absolute Accuracy Curve

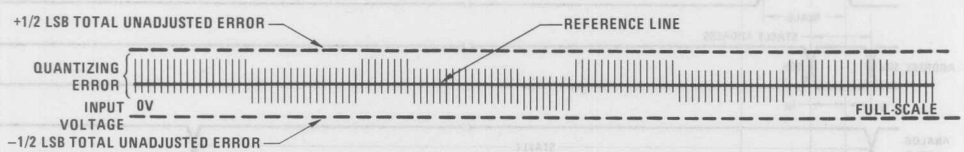
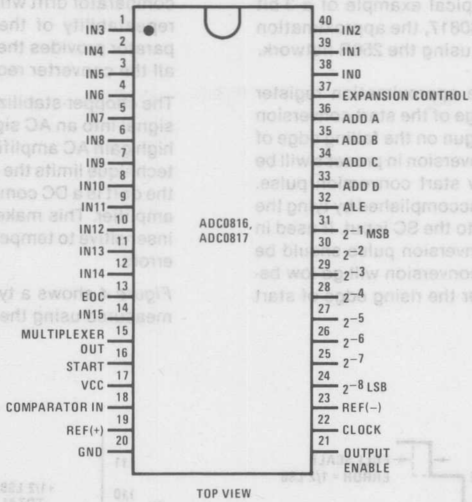


FIGURE 4. Typical Error Curve

Connection Diagram

Dual-In-Line Package



Timing Diagram

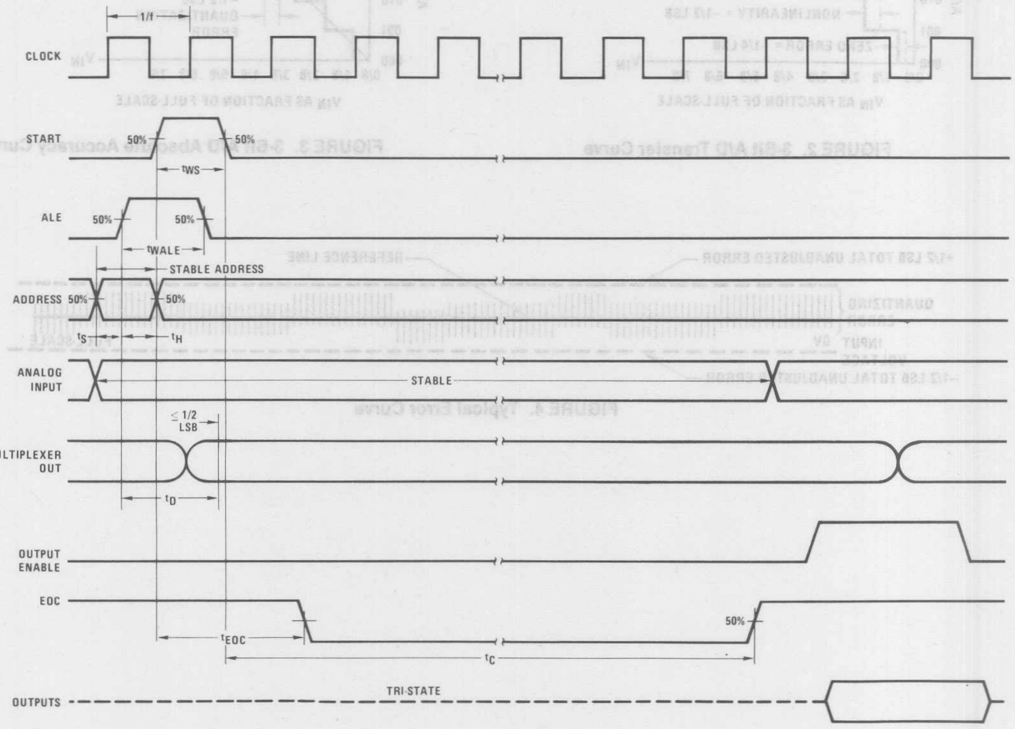


FIGURE 5

Typical Performance Characteristics

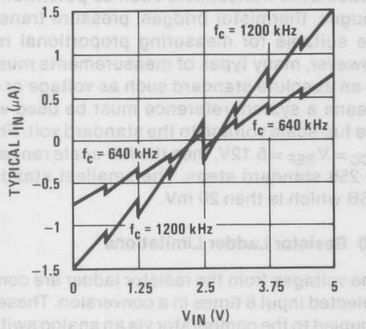


FIGURE 6. Comparator I_{IN} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

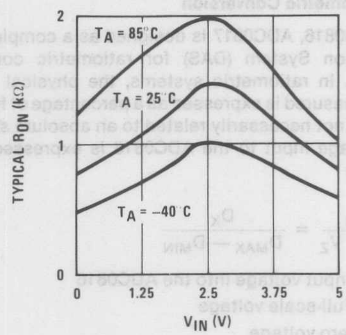


FIGURE 7. Multiplexer R_{ON} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

TRI-STATE® Test Circuits and Timing Diagrams

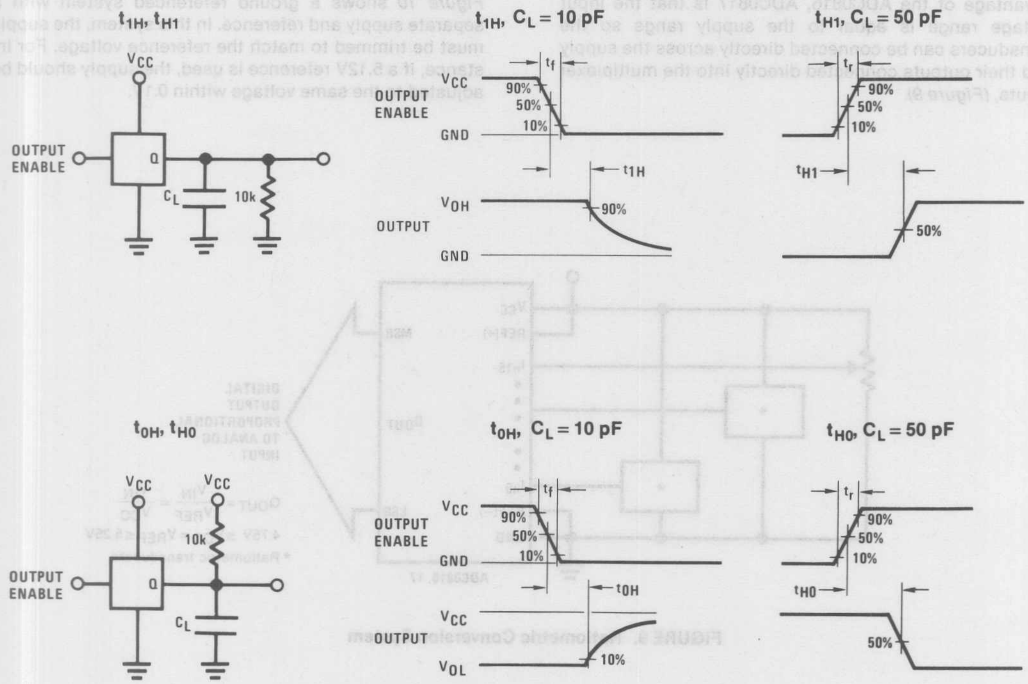


FIGURE 8

Applications Information

OPERATION

1.0 Ratiometric Conversion

The ADC0816, ADC0817 is designed as a complete Data Acquisition System (DAS) for ratiometric conversion systems. In ratiometric systems, the physical variable being measured is expressed as a percentage of full-scale which is not necessarily related to an absolute standard. The voltage input to the ADC0816 is expressed by the equation

$$\frac{V_{IN}}{V_{fs} - V_Z} = \frac{D_X}{D_{MAX} - D_{MIN}} \qquad (1)$$

V_{IN} = Input voltage into the ADC0816
V_{fs} = Full-scale voltage
V_Z = Zero voltage
D_X = Data point being measured
D_{MAX} = Maximum data limit
D_{MIN} = Minimum data limit

A good example of a ratiometric transducer is a potentiometer used as a position sensor. The position of the wiper is directly proportional to the output voltage which is a ratio of the full-scale voltage across it. Since the data is represented as a proportion of full-scale, reference requirements are greatly reduced, eliminating a large source of error and cost for many applications. A major advantage of the ADC0816, ADC0817 is that the input voltage range is equal to the supply range so the transducers can be connected directly across the supply and their outputs connected directly into the multiplexer inputs, *(Figure 9).*

Ratiometric transducers such as potentiometers, strain gauges, thermistor bridges, pressure transducers, etc., are suitable for measuring proportional relationships; however, many types of measurements must be referred to an absolute standard such as voltage or current. This means a system reference must be used which relates the full-scale voltage to the standard volt. For example, if $V_{CC} = V_{REF} = 5.12V$, then the full-scale range is divided into 256 standard steps. The smallest standard step is 1 LSB which is then 20 mV.

2.0 Resistor Ladder Limitations

The voltages from the resistor ladder are compared to the selected input 8 times in a conversion. These voltages are coupled to the comparator via an analog switch tree which is referenced to the supply. The voltages at the top, center and bottom of the ladder must be controlled to maintain proper operation.

The top of the ladder, Ref(+), should not be more positive than the supply, and the bottom of the ladder, Ref(−), should not be more negative than ground. The center of the ladder voltage must also be near the center of the supply because the analog switch tree changes from N-channel switches to P-channel switches. These limitations are automatically satisfied in ratiometric systems and can be easily met in ground referenced systems.

Figure 10 shows a ground referenced system with a separate supply and reference. In this system, the supply must be trimmed to match the reference voltage. For instance, if a 5.12V reference is used, the supply should be adjusted to the same voltage within 0.1V.

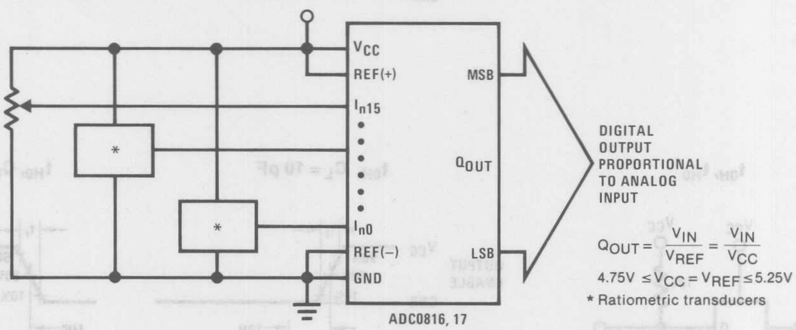


FIGURE 9. Ratiometric Conversion System

Applications Information (Continued)

The ADC0816 needs less than a milliamp of supply current so developing the supply from the reference is readily accomplished. In *Figure 11* a ground referenced system is shown which generates the supply from the reference. The buffer shown can be an op amp of sufficient drive to supply the milliamp of supply current and the desired bus drive, or if a capacitive bus is driven by the outputs a large capacitor will supply the transient supply current as seen in *Figure 12*. The LM301 is overcompensated to insure stability when loaded by the 10 μF output capacitor.

The top and bottom ladder voltages cannot exceed V_{CC} and ground, respectively, but they can be symmetrically less than V_{CC} and greater than ground. The center of the ladder voltage should always be near the center of the supply. The sensitivity of the converter can be increased, (i.e., size of the LSB steps decreased) by using a symmetrical reference system. In *Figure 13*, a 2.5V reference is symmetrically centered about $V_{CC}/2$ since the same current flows in identical resistors. This system with a 2.5V reference allows the LSB to be half the size of the LSB in a 5V reference system.

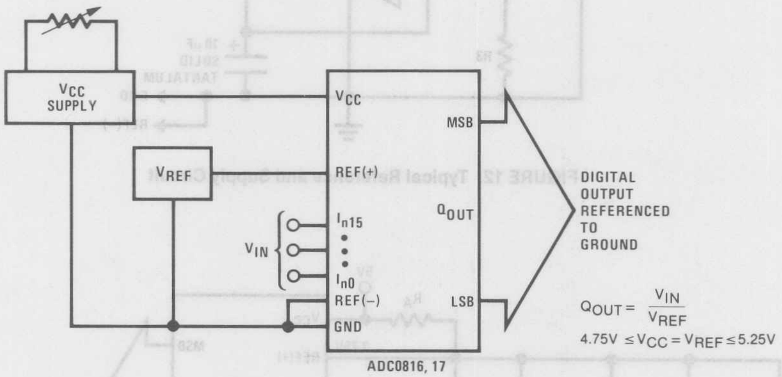


FIGURE 10. Ground Referenced Conversion System Using Trimmed Supply

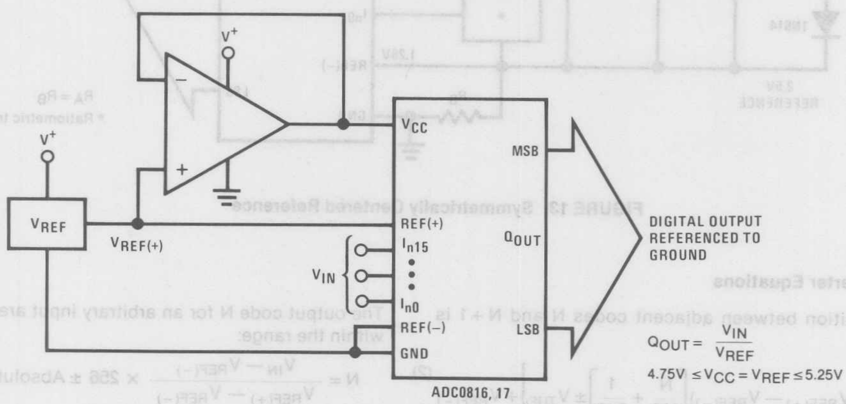


FIGURE 11. Ground Referenced Conversion System with Reference Generating V_{CC} Supply

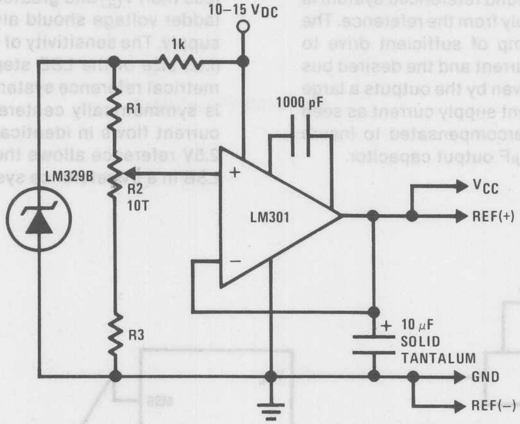


FIGURE 12. Typical Reference and Supply Circuit

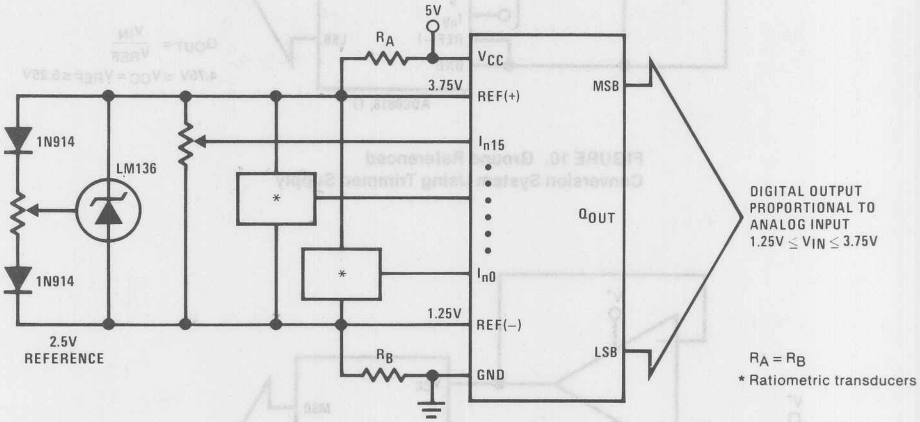


FIGURE 13. Symmetrically Centered Reference

3.0 Converter Equations

The transition between adjacent codes N and N+1 is given by:

$$V_{IN} = \left\{ (V_{REF(+)} - V_{REF(-)}) \left[\frac{N}{256} + \frac{1}{512} \right] \pm V_{TUE} \right\} + V_{REF(-)} \quad (2)$$

The center of an output code N is given by:

$$V_{IN} = \left\{ (V_{REF(+)} - V_{REF(-)}) \left[\frac{N}{256} \right] \pm V_{TUE} \right\} + V_{REF(-)} \quad (3)$$

The output code N for an arbitrary input are the integers within the range:

$$N = \frac{V_{IN} - V_{REF(-)}}{V_{REF(+)} - V_{REF(-)}} \times 256 \pm \text{Absolute Accuracy} \quad (4)$$

where: V_{IN} = Voltage at comparator input
$V_{REF(+)}$ = Voltage at Ref(+)
$V_{REF(-)}$ = Voltage at Ref(−)
V_{TUE} = Total unadjusted error voltage (typically $V_{REF(+)} \div 512$)

Applications Information (Continued)

4.0 Analog Comparator Inputs

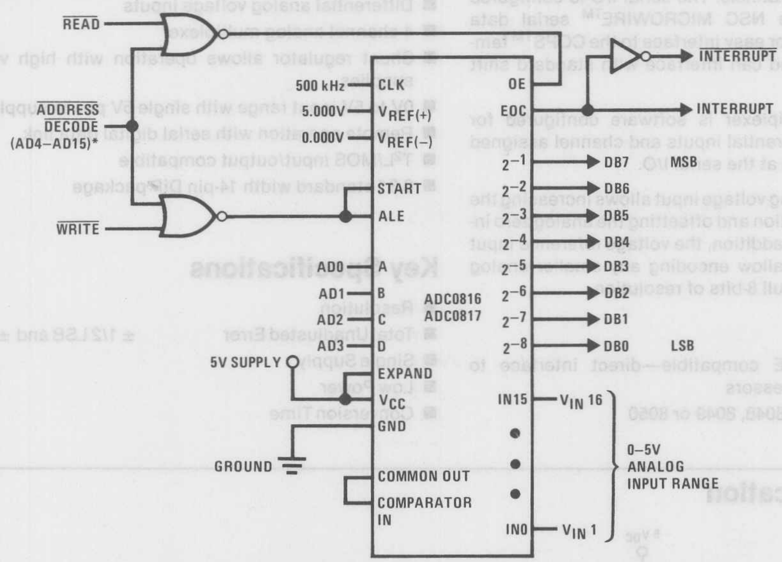
The dynamic comparator input current is caused by the periodic switching of on-chip stray capacitances. These are connected alternately to the output of the resistor ladder/switch tree network and to the comparator input as part of the operation of the chopper stabilized comparator.

The average value of the comparator input current varies directly with clock frequency and with V_{IN} as shown in *Figure 6*.

If no filter capacitors are used at the analog or comparator inputs and the signal source impedances are low, the comparator input current should not introduce converter errors, as the transient created by the capacitance discharge will die out before the comparator output is strobed.

If input filter capacitors are desired for noise reduction and signal conditioning they will tend to average out the dynamic comparator input current. It will then take on the characteristics of a DC bias current whose effect can be predicted conventionally. See AN-258 for further discussion.

Typical Application



* Address latches needed for 8085 and SC/MP interfacing the ADC0816, 17 to a microprocessor

Microprocessor Interface Table

PROCESSOR	$\overline{\text{READ}}$	$\overline{\text{WRITE}}$	INTERRUPT (COMMENT)
8080	$\overline{\text{MEMR}}$	$\overline{\text{MEMW}}$	INTR (Thru RST Circuit)
8085	$\overline{\text{RD}}$	$\overline{\text{WR}}$	INTR (Thru RST Circuit)
Z-80	$\overline{\text{RD}}$	$\overline{\text{WR}}$	$\overline{\text{INT}}$ (Thru RST Circuit, Mode 0)
SC/MP	NRDS	NWDS	SA (Thru Sense A)
6800	VMA·ϕ2·R/W	VMA·ϕ2·$\overline{\text{R/W}}$	$\overline{\text{IRQA}}$ or $\overline{\text{IRQB}}$ (Thru PIA)

Ordering Information

TEMPERATURE RANGE		−40°C to +85°C		−55°C to +125°C
Error	±1/2 Bit Unadjusted	ADC0816CCN	ADC0816CCJ	ADC0816CJ
	±1 Bit Unadjusted	ADC0817CCN		
Package Outline		N40A Molded DIP	J40A Hermetic DIP	J40A Hermetic DIP

National Semiconductor

ADC0833 8-Bit Serial I/O A/D Converter with 4-Channel Multiplexer

General Description

The ADC0833 series is an 8-bit successive approximation A/D converter with a serial I/O and configurable input multiplexer with 4 channels. The serial I/O is configured to comply with the NSC MICROWIRE™ serial data exchange standard for easy interface to the COPS™ family of processors, and can interface with standard shift registers or μPs.

The 4-channel multiplexer is software configured for single ended or differential inputs and channel assigned by a 4-bit serial word at the serial I/O.

The differential analog voltage input allows increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8-bits of resolution.

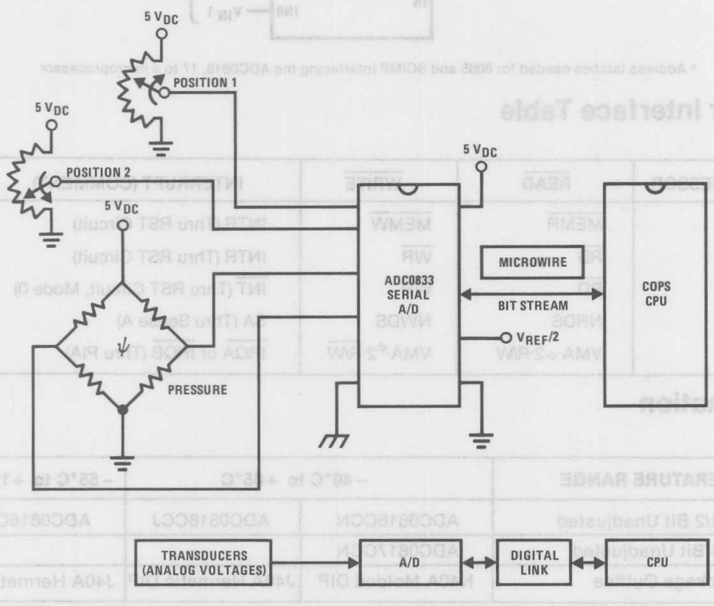
Features

- NSC MICROWIRE compatible—direct interface to COPS family processors
- Easy interface to 8048, 8049 or 8050
- Works with 2.5V (LM336) voltage reference
- No full-scale or zero adjust required
- Differential analog voltage inputs
- 4-channel analog multiplexer
- Shunt regulator allows operation with high voltage supplies
- 0V to 5V input range with single 5V power supply
- Remote operation with serial digital data link
- T^2L/MOS input/output compatible
- 0.3″ standard width 14-pin DIP package

Key Specifications

Resolution	8-Bits
Total Unadjusted Error	± 1/2 LSB and ± 1 LSB
Single Supply	5 V_{DC}
Low Power	15 mW
Conversion Time	80 μs

Typical Application



Absolute Maximum Ratings (Notes 1 and 2)

Current into V^+ (Note 5)	10 mA
Supply Voltage, V_{CC} (Note 5)	6.5V
Voltage	
Logic Inputs	−0.3V to +18V
Analog Inputs	−0.3V to V_{CC}+0.3V
Storage Temperature	−65°C to +150°C
Package Dissipation at T_A = 25°C (Board Mount)	0.8W
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Ratings (Notes 1 and 2)

Supply Voltage, V_{CC}	4.5 V_{DC} to 6.3 V_{DC}
Temperature Range	$T_{MIN} \leq T_A \leq T_{MAX}$
ADC0833BD, ADC0833CD	$-55°C \leq T_A \leq 125°C$
ADC0833BCD, ADC0833CCD	$-40°C \leq T_A \leq 85°C$
ADC0833BCN, ADC0833CCN	$0°C \leq T_A \leq 70°C$

Converter and Multiplexer Electrical Characteristics

The following specifications apply for $V_{CC} = V^+ = 5V$, $T_{MIN} \leq T_A \leq T_{MAX}$ and f_{CLK} = 100 kHz unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Total Unadjusted Error:					
ADC0833B	$V_{REF}/2$ Forced to 2.500 V_{DC}			±1/2	LSB
ADC0833C	$V_{REF}/2$ Forced to 2.500 V_{DC}			±1	LSB
Reference Input Resistance (Thevinin Equivalent)			9		kΩ
Common-Mode Input Range (Note 4)	All MUX Inputs and COM Input	GND−0.05		V_{CC}+0.05	V
DC Common-Mode Error	Differential Mode		±1/16		LSB
Power Supply Sensitivity	V_{CC} = 5V ± 5%		±1/16		LSB
I_{OFF}, Off Channel Leakage Current (Note 3)	On Channel = 5V Off Channels = 0V	−1			μA
	T_A = 25°C	−50			nA
	On Channel = 0V Off Channels = 5V			1	μA
	T_A = 25°C			50	nA
I_{ON}, On Channel Leakage Current (Note 3)	On Channel = 0V Off Channels = 5V	−1			μA
	T_A = 25°C	−200			nA
	On Channel = 5V Off Channel = 0V			1	μA
	T_A = 25°C			200	nA

AC Electrical Characteristics

The following specifications apply for V_{CC} = 5V, $t_r = t_f$ = 20 ns and T_A = 25°C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
f_{CLK}, Clock Frequency		10		200	kHz
Clock Duty Cycle		40		60	%
T_C, Conversion time	Not Including MUX Addressing Time			8	$1/f_{CLK}$
t_{SETUP}, $\overline{SE}$ or $\overline{CS}$ Falling Edge or Data Input Valid to CLK Rising Edge			200		ns
t_{HOLD}, Data Input Valid after CLK Rising Edge			200		ns

Parameter	Conditions	Min	Typ	Max	Units
t_{pd1}, t_{pd0}—CLK Falling Edge to Output Data Valid (Note 6)	$C_L = 100$ pF Data MSB First Data LSB First		 650 250		 ns ns
t_{1H}, t_{0H}—Rising Edge of $\overline{CS}$ to Data Output and SARS Hi-Z	$C_L = 10$ pF, $R_L = 10k$ (See TRI-STATE® Test Circuits)		125		ns
C_{IN}, Capacitance of Logic Inputs			5		pF
C_{OUT}, Capacitance of Logic Outputs			5		pF

DC Electrical Characteristics

The following specifications apply for $V_{CC} = 5V$ and $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
$V_{IN(1)}$, Logical "1" Input Voltage	$V_{CC} = 5.25V$	2.0		15	V
$V_{IN(0)}$, Logical "0" Input Voltage	$V_{CC} = 4.75V$			0.8	V
$I_{IN(1)}$, Logical "1" Input Current	$V_{IN} = V_{CC}$		0.005	1	μA
$I_{IN(0)}$, Logical "0" Input Current	$V_{IN} = 0V$	−1	−0.005		μA
$V_{OUT(1)}$, Logical "1" Output Voltage	$I_{OUT} = -360\ \mu A$, $V_{CC} = 4.75V$ $I_{OUT} = -10\ \mu A$, $V_{CC} = 4.75V$	2.4 4.5			V V
$V_{OUT(0)}$, Logical "0" Output Voltage	$I_{OUT} = 1.6$ mA, $V_{CC} = 4.75V$			0.4	V
I_{OUT}, TRI-STATE Output Current (DO, SARS)	$V_{OUT} = 0.4V$ $V_{OUT} = 5V$		0.1 0.1	100 3	μA_{DC} μA_{DC}
I_{SOURCE}	V_{OUT} Short to GND, $T_A = 25°C$		14		mA
I_{SINK}	V_{OUT} Short to V_{CC}, $T_A = 25°C$		16		mA
I_{CC}, Supply Current (Note 5)	$V_{REF}/2$ Open Circuit		3.0		mA
I^+, Current into V^+ (Note 5)				10	mA

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltages are measured with respect to ground.

Note 3: Leakage current is measured with the clock not switching.

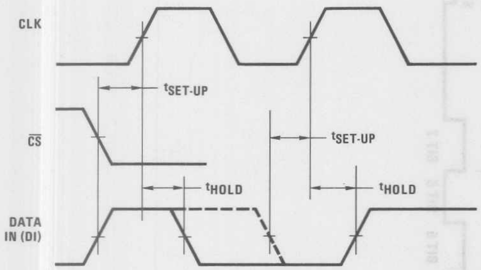
Note 4: For $V_{IN}(-) \ge V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see Block Diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: An internal zener diode exists from V_{CC} to GND on the V^+ and V_{CC} inputs. The breakdown of these zeners is approximately 7V. The V^+ zener is intended to operate as a shunt regulator and connects to the V_{CC} via a diode. When using this regulator to power the A/D, this diode guarantees the V_{CC} input to be operating below the zener voltage (7V − 0.6V). It is recommended that a series resistor be used to limit the maximum current into the V^+ input.

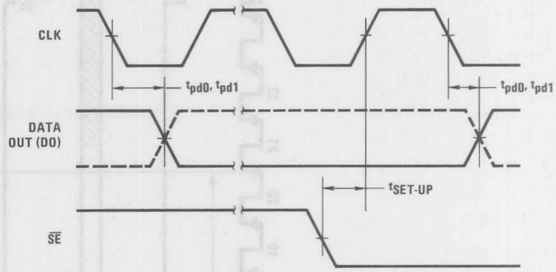
Note 6: Since data, MSB first, is the output of the comparator used in the successive approximation loop, an additional delay is built in (see Block Diagram) to allow for comparator response time.

Timing Diagrams

Data Input Timing

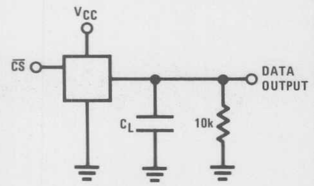


Data Output Timing

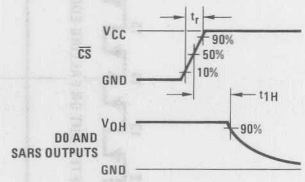


TRI-STATE Test Circuits and Waveforms

t_{1H}

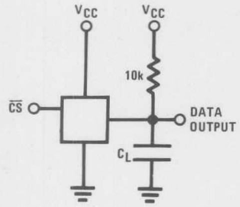


t_{1H}, $C_L = 10$ pF

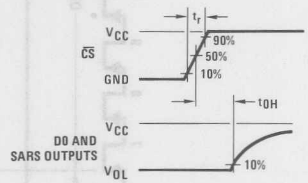


$t_r = 20$ ns

t_{0H}

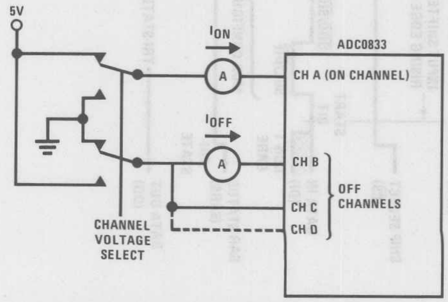


t_{0H}, $C_L = 10$ pF

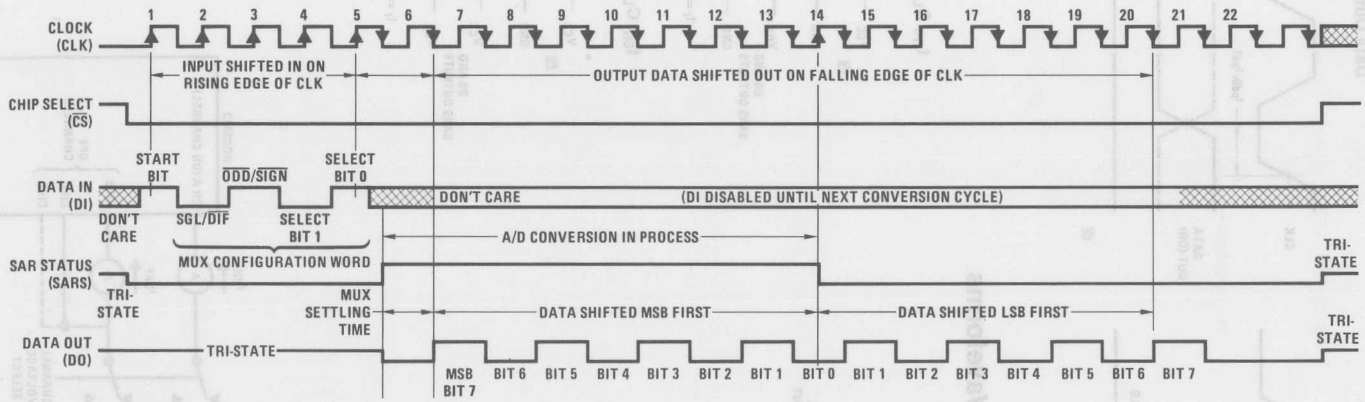


$t_r = 20$ ns

Leakage Current Test Circuit



Functional Timing Diagram



MUX Addressing

The 4-channel multiplexer is software configurable as single ended or differential inputs. The configuration and channel assignment of the multiplexer is accomplished with a 4-bit serial input word which must be preceded by a leading "1" or start bit (leading zeros are ignored).

Differential inputs are restricted to adjacent channel pairs. For example channel 0 and channel 1 may be selected as a differential pair. Channel 0 or 1 cannot act differentially with any other channel. In addition to selecting differential mode the sign may also be selected. Channel 0 may be selected as the positive input and channel 1 as the negative input or vice versa.

Data is always shifted in on the rising clock edge and shifted out on the falling clock edge.

If $\overline{CS}$ goes high, the conversion is stopped and all internal circuitry is reset. If another conversion is desired, $\overline{CS}$ must make a high-to-low transition followed by address information.

TABLE I. MUX ADDRESSING

Single-Ended MUX Mode

Address				Channel #			
SGL/ $\overline{DIF}$	$\overline{ODD}$/ SIGN	SELECT 1	SELECT 0	0	1	2	3
1	0	0	1	+			
1	0	1	1			+	
1	1	0	1		+		
1	1	1	1				+

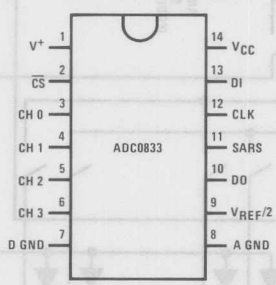
COM is internally tied to A GND

Differential MUX Mode

Address				Channel #			
SGL/ $\overline{DIF}$	$\overline{ODD}$/ SIGN	SELECT 1	SELECT 0	0	1	2	3
0	0	0	1	+	−		
0	0	1	1			+	−
0	1	0	1	−	+		
0	1	1	1			−	+

Connection Diagram

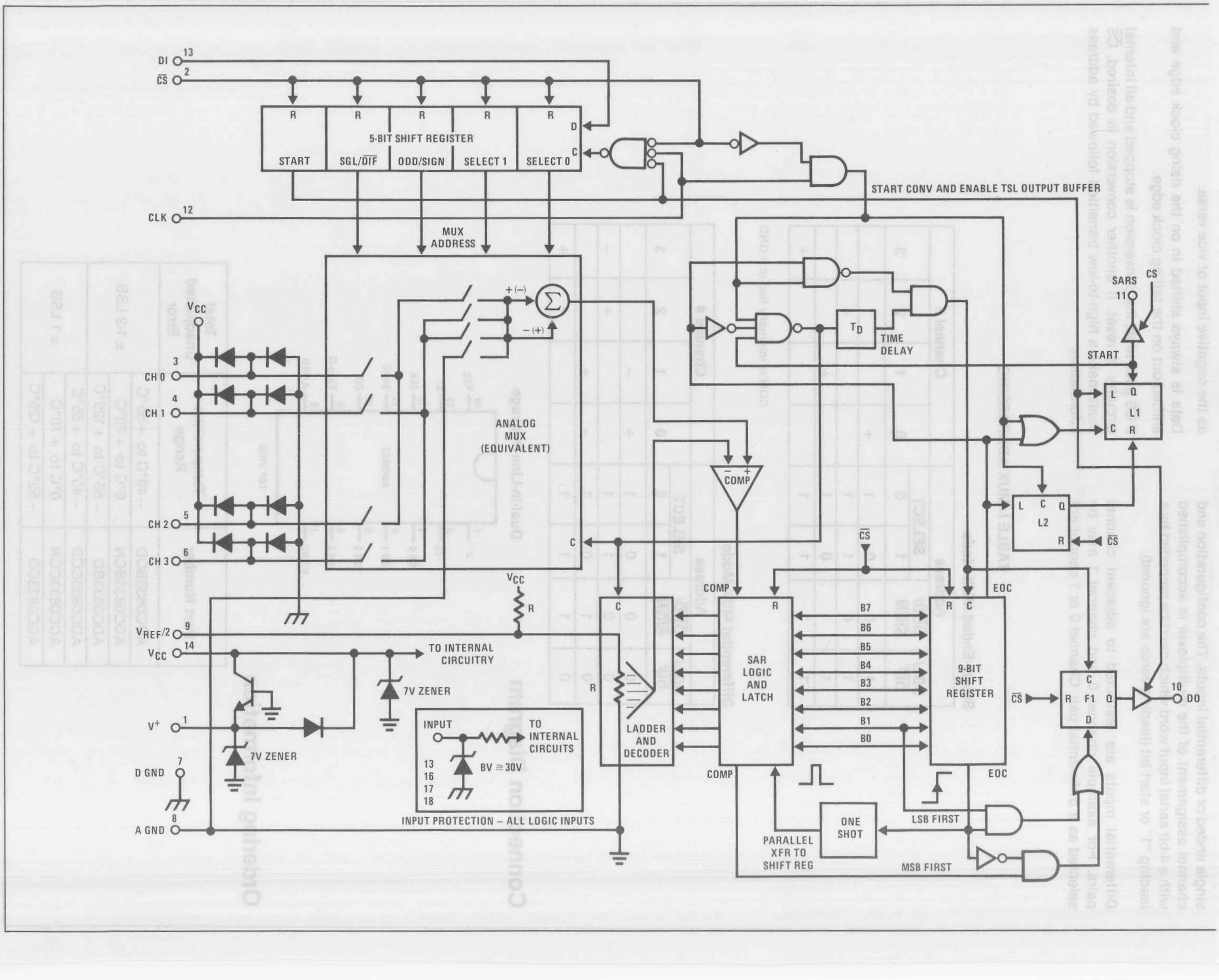
Dual-In-Line Package



TOP VIEW

Ordering Information

Part Number	Temperature Range	Total Unadjusted Error
ADC0833BCD	−40°C to +85°C	±1/2 LSB
ADC0833BCN	0°C to +70°C	
ADC0833BD	−55°C to +125°C	
ADC0833CCD	−40°C to +85°C	±1 LSB
ADC0833CCN	0°C to +70°C	
ADC0833CD	−55°C to +125°C	


DI 13
CS 2
5-BIT SHIFT REGISTER
START
SGL/DIF
ODD/SIGN
SELECT 1
SELECT 0
CLK 12
START CONV AND ENABLE TSL OUTPUT BUFFER
MUX ADDRESS
ANALOG MUX (EQUIVALENT)
COMP
TIME DELAY
SARS 11
START
L1
L2
CH 0 3
CH 1 4
CH 2 5
CH 3 6
VREF/2 9
VCC 14
TO INTERNAL CIRCUITRY
7V ZENER
V+ 1
D GND 7
A GND 8
INPUT
TO INTERNAL CIRCUITS
BV ≅ 30V
INPUT PROTECTION – ALL LOGIC INPUTS
LADDER AND DECODER
SAR LOGIC AND LATCH
9-BIT SHIFT REGISTER
EOC
B7
B6
B5
B4
B3
B2
B1
B0
F1
10 DO
ONE SHOT
PARALLEL XFR TO SHIFT REG
LSB FIRST
MSB FIRST

ADC1001, ADC1021 10-Bit μP Compatible A/D Converters

General Description

The ADC1001 and ADC1021 are CMOS, 10-bit successive approximation A/D converters. The 20-pin ADC1001 is pin compatible with the ADC0801 8-bit A/D family. The 10-bit data word is read in two 8-bit bytes, formatted left justified and high byte first. The six least significant bits of the second byte are set to zero, as is proper for a 16-bit word.

The 24-pin ADC1021 outputs 10 bits in parallel and is intended for interface to a 16-bit data bus.

A differential analog voltage input allows increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 10 bits of resolution.

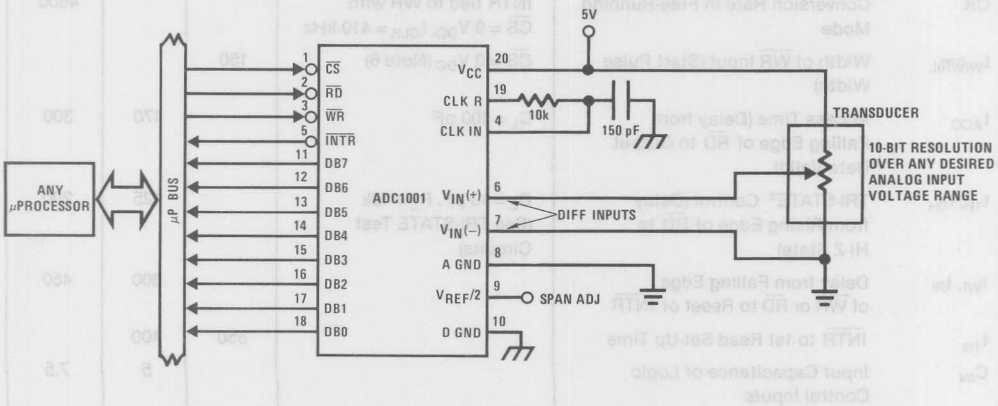
Features

- ADC1001 is pin compatible with ADC0801 series 8-bit A/D
- Compatible with NSC800 and 8080 μP derivatives — no interfacing logic needed — access time 170 ns
- Easily interfaced to 6800 μP derivatives with minimal external logic
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and T^2L voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference
- 0.3″ standard width 20-pin DIP package or 24 pins with 10-bit parallel output

Key Specifications

- Resolution: 10 bits
- Linearity error: ± 1/2 LSB and ± 1 LSB
- Conversion time: 200 μs

Typical Application



Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC}) (Note 3)	6.5V
Logic Control Inputs	−0.3V to +18V
Voltage at Other Inputs and Outputs	−0.3V to (V_{CC} + 0.3V)
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A = 25°C	875 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Ratings (Notes 1 and 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC1001BD, ADC1001CD ADC1021BD, ADC1021CD	$-55°C \le T_A \le +125°C$
ADC1001BCD, ADC1001CCD ADC1021BCD, ADC1021CCD	$-40°C \le T_A \le +85°C$
ADC1001BCN, ADC1001CCN ADC1021BCN, ADC1021CCN	$0°C \le T_A \le +70°C$
Range of V_{CC}	4.5 V_{DC} to 6.3 V_{DC}

Converter Characteristics

Converter Specifications: V_{CC} = 5 V_{DC}, $V_{REF}/2$ = 2.500 V_{DC}, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK} = 410 kHz unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
ADC1001B, ADC1021B:					
Linearity Error				±1/2	LSB
Zero Error				±1	LSB
Full-Scale Error				±1	LSB
ADC1001C, ADC1021C:					
Linearity Error				±1	LSB
Zero Error				±2	LSB
Full-Scale Error				±2	LSB
$V_{REF}/2$ Input Resistance	Input Resistance at Pin 9	3.2	5.2		kΩ
Analog Input Voltage Range	(Note 4) V(+) or V(−)	GND − 0.05		V_{CC} + 0.05	V_{DC}
DC Common-Mode Error	Over Analog Input Voltage Range		±1/8		LSB
Power Supply Sensitivity	V_{CC} = 5 V_{DC} ±5% Over Allowed $V_{IN}(+)$ and $V_{IN}(-)$ Voltage Range (Note 4)		±1/8		LSB

AC Electrical Characteristics

Timing Specifications: V_{CC} = 5 V_{DC} and T_A = 25°C unless otherwise specified.

Parameter		Conditions	Min	Typ	Max	Units
T_c	Conversion Time	(Note 5) f_{CLK} = 410 kHz	82 200		89 217	$1/f_{CLK}$ μs
f_{CLK}	Clock Frequency	(Note 8)	100		1260	kHz
	Clock Duty Cycle		40		60	%
CR	Conversion Rate In Free-Running Mode	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$ = 0 V_{DC}, f_{CLK} = 410 kHz			4600	conv/s
$t_{W(\overline{WR})L}$	Width of $\overline{WR}$ Input (Start Pulse Width)	$\overline{CS}$ = 0 V_{DC} (Note 6)	150			ns
t_{ACC}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	C_L = 100 pF		170	300	ns
t_{1H}, t_{0H}	TRI-STATE® Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	C_L = 10 pF, R_L = 10k (See TRI-STATE Test Circuits)		125	200	ns
t_{WI}, t_{RI}	Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$			300	450	ns
t_{1rs}	$\overline{INTR}$ to 1st Read Set-Up Time		550	400		ns
C_{IN}	Input Capacitance of Logic Control Inputs			5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance (Data Buffers)			5	7.5	pF

TRI-STATE® is a registered trademark of National Semiconductor Corp.

DC Electrical Characteristics

The following specifications apply for $V_{CC} = 5\ V_{DC}$ and $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise specified.

Parameter		Conditions	Min	Typ	Max	Units
CONTROL INPUTS [Note: CLK IN is the input of a Schmitt trigger circuit and is therefore specified separately]						
V_{IN} (1)	Logical "1" Input Voltage (Except CLK IN)	$V_{CC} = 5.25\ V_{DC}$	2.0		15	V_{DC}
V_{IN} (0)	Logical "0" Input Voltage (Except CLK IN)	$V_{CC} = 4.75\ V_{DC}$			0.8	V_{DC}
I_{IN} (1)	Logical "1" Input Current (All Inputs)	$V_{IN} = 5\ V_{DC}$		0.005	1	μA_{DC}
I_{IN} (0)	Logical "0" Input Current (All Inputs)	$V_{IN} = 0\ V_{DC}$	−1	−0.005		μA_{DC}
CLOCK IN						
V_T+	CLK IN Positive Going Threshold Voltage		2.7	3.1	3.5	V_{DC}
V_T-	CLK IN Negative Going Threshold Voltage		1.5	1.8	2.1	V_{DC}
V_H	CLK IN Hysteresis $(V_T+) - (V_T-)$		0.6	1.3	2.0	V_{DC}
OUTPUTS AND $\overline{\text{INTR}}$						
$V_{OUT}(0)$	Logical "0" Output Voltage	$I_{OUT} = 1.6$ mA, $V_{CC} = 4.75\ V_{DC}$			0.4	V_{DC}
$V_{OUT}(1)$	Logical "1" Output Voltage	$I_O = -360\ \mu A$, $V_{CC} = 4.75\ V_{DC}$ $I_O = -10\ \mu A$, $V_{CC} = 4.75\ V_{DC}$	2.4 4.5			V_{DC} V_{DC}
I_{OUT}	TRI-STATE Disabled Output Leakage (All Data Buffers)	$V_{OUT} = 0.4\ V_{DC}$ $V_{OUT} = 5\ V_{DC}$		0.1 0.1	−100 3	μA_{DC} μA_{DC}
I_{SOURCE}		V_{OUT} Short to GND, $T_A = 25°C$	4.5	6		mA_{DC}
I_{SINK}		V_{OUT} Short to V_{CC}, $T_A = 25°C$	9.0	16		mA_{DC}
POWER SUPPLY						
I_{CC}	Supply Current (Includes Ladder Current)	$f_{CLK} = 410$ kHz, $V_{REF}/2 = NC$, $T_A = 25°C$ and $\overline{CS} = 1$		1.5	2.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltages are measured with respect to GND, unless otherwise specified. The separate A GND point should always be wired to the D GND.

Note 3: A zener diode exists, internally, from V_{CC} to GND and has a typical breakdown voltage of 7 V_{DC}.

Note 4: For $V_{IN}(-) \ge V_{IN}(+)$ the digital output code will be all zeros. Two on-chip diodes are tied to each analog input (see Block Diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct–especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

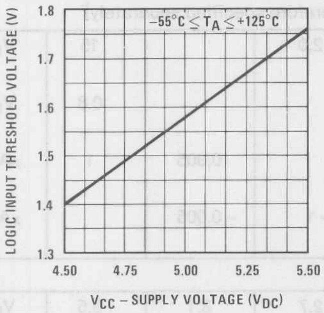
Note 5: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The start request is internally latched, see *Figure 1.*

Note 6: The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input and therefore timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see Timing Diagrams).

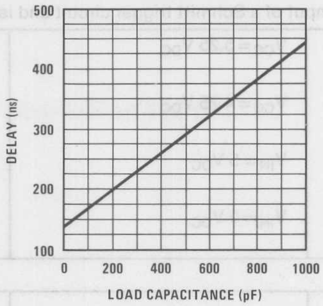
Note 7: All typical values are for $T_A = 25°C$.

Note 8: Accuracy is guaranteed at $f_{CLK} = 410$ kHz. At higher clock frequencies accuracy can degrade.

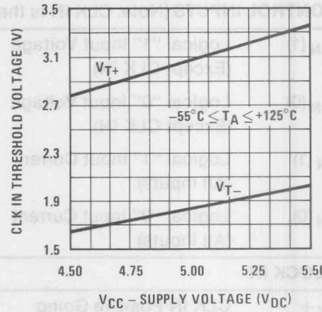
Voltage vs Supply Voltage



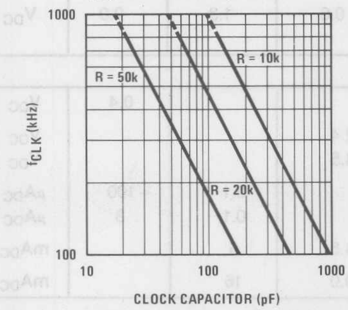
vs Load Capacitance



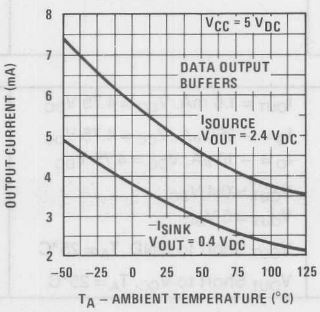
vs Supply Voltage



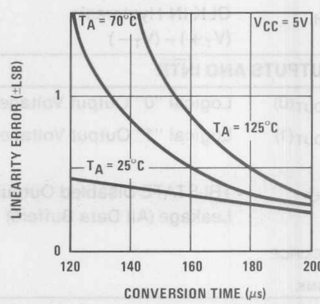
f_{CLK} vs Clock Capacitor



Output Current vs Temperature

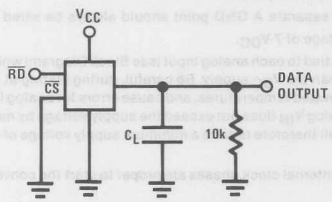


Typical Linearity Error vs Conversion Time

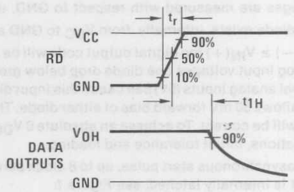


TRI-STATE Test Circuits and Waveforms

t_{1H}

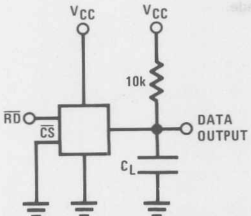


t_{1H}, C_L = 10 pF

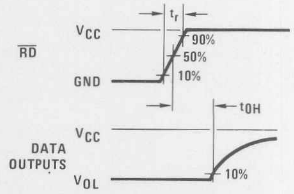


t_r = 20 ns

t_{0H}

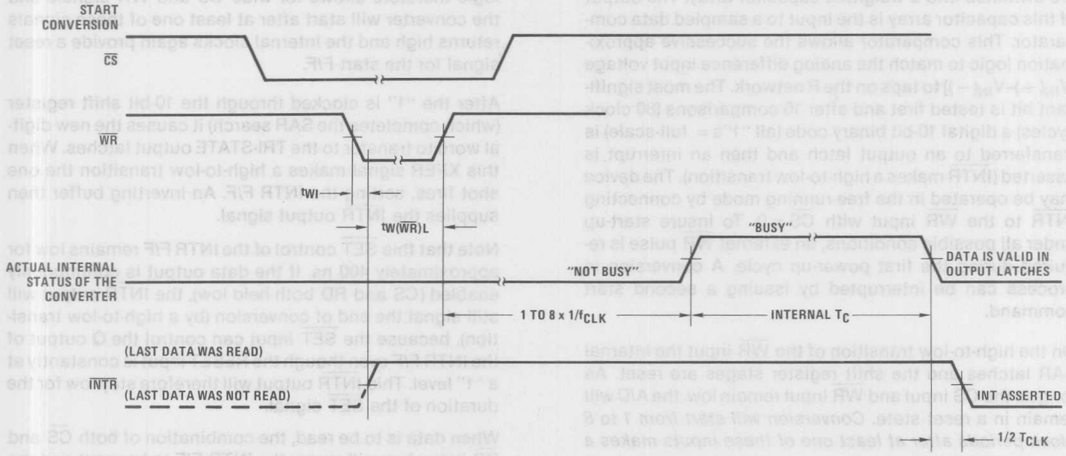


t_{0H}, C_L = 10 pF

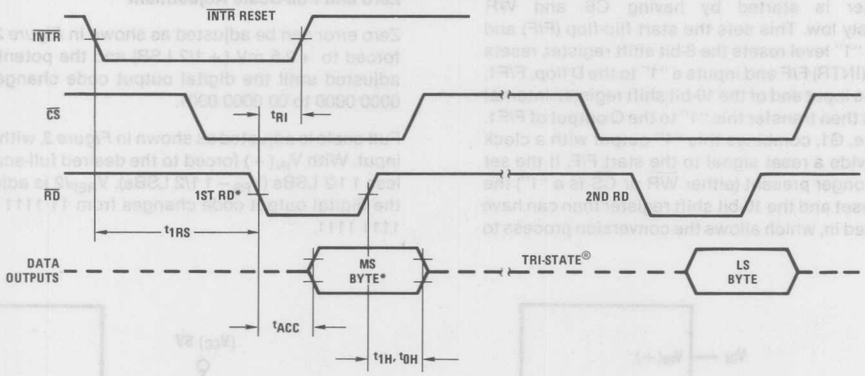


t_r = 20 ns

Timing Diagrams



Output Enable and Reset INTR



*The 24-pin ADC1021 outputs all 10 bits on each RD.

Note: All timing is measured from the 50% voltage points.

BYTE SEQUENCING FOR THE 20-PIN ADC1001

Byte Order	8-Bit Data Bus Connection							
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1st	MSB Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2
2nd	Bit 1	LSB Bit 0	0	0	0	0	0	0

Functional Description

The ADC1001, ADC1021 are mechanized using an advanced potentiometric resistive ladder network. The analog inputs, as well as the taps of this ladder network, are switched into a weighted capacitor array. The output of this capacitor array is the input to a sampled data comparator. This comparator allows the successive approximation logic to match the analog difference input voltage [$V_{IN}(+)-V_{IN}(-)$] to taps on the R network. The most significant bit is tested first and after 10 comparisons (80 clock cycles) a digital 10-bit binary code (all "1"s = full-scale) is transferred to an output latch and then an interrupt is asserted ($\overline{INTR}$ makes a high-to-low transition). The device may be operated in the free-running mode by connecting $\overline{INTR}$ to the $\overline{WR}$ input with $\overline{CS}=0$. To insure start-up under all possible conditions, an external $\overline{WR}$ pulse is required during the first power-up cycle. A conversion in process can be interrupted by issuing a second start command.

On the high-to-low transition of the $\overline{WR}$ input the internal SAR latches and the shift register stages are reset. As long as the $\overline{CS}$ input and $\overline{WR}$ input remain low, the A/D will remain in a reset state. *Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition.*

A functional diagram of the A/D converter is shown in *Figure 1*. All of the inputs and outputs are shown and the major logic control paths are drawn in heavier weight lines.

The converter is started by having $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register, resets the Interrupt (INTR) F/F and inputs a "1" to the D flop, F/F1, which is at the input end of the 10-bit shift register. Internal clock signals then transfer this "1" to the Q output of F/F1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a "1") the start F/F is reset and the 10-bit shift register then can have the "1" clocked in, which allows the conversion process to continue. If the set signal were to still be present, this reset pulse would have no effect and the 10-bit shift register would continue to be held in the reset mode. This logic therefore allows for wide $\overline{CS}$ and $\overline{WR}$ signals and the converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start F/F.

After the "1" is clocked through the 10-bit shift register (which completes the SAR search) it causes the new digital word to transfer to the TRI-STATE output latches. When this XFER signal makes a high-to-low transition the one shot fires, setting the INTR F/F. An inverting buffer then supplies the $\overline{INTR}$ output signal.

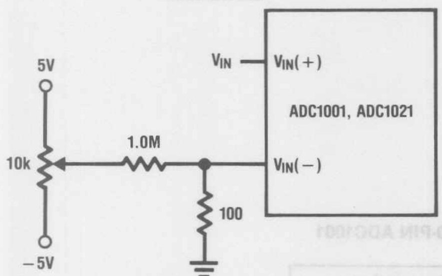
Note that this $\overline{SET}$ control of the INTR F/F remains low for approximately 400 ns. If the data output is continuously enabled ($\overline{CS}$ and $\overline{RD}$ both held low), the $\overline{INTR}$ output will still signal the end of conversion (by a high-to-low transition), because the $\overline{SET}$ input can control the Q output of the INTR F/F even though the RESET input is constantly at a "1" level. This $\overline{INTR}$ output will therefore stay low for the duration of the $\overline{SET}$ signal.

When data is to be read, the combination of both $\overline{CS}$ and $\overline{RD}$ being low will cause the INTR F/F to be reset and the TRI-STATE output latches will be enabled.

Zero and Full-Scale Adjustment

Zero error can be adjusted as shown in *Figure 2*. $V_{IN}(+)$ is forced to +2.5 mV (+1/2 LSB) and the potentiometer is adjusted until the digital output code changes from 00 0000 0000 to 00 0000 0001.

Full-scale is adjusted as shown in *Figure 3*, with the $V_{REF}/2$ input. With $V_{IN}(+)$ forced to the desired full-scale voltage less 1 1/2 LSBs ($V_{FS}-1\ 1/2$ LSBs), $V_{REF}/2$ is adjusted until the digital output code changes from 11 1111 1110 to 11 1111 1111.



NOTE: $V_{IN}(-)$ should be biased so that $V_{IN}(-) \geq -0.05V$ when potentiometer wiper is set at most negative voltage position.

FIGURE 2. Zero Adjust Circuit

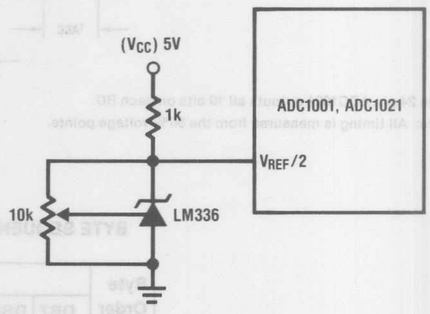
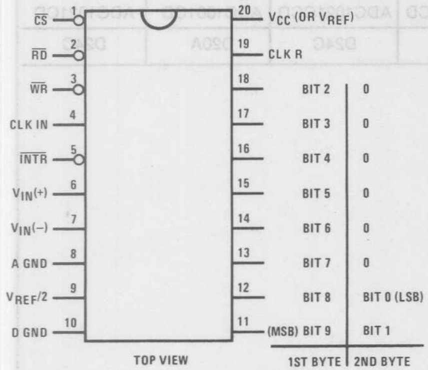
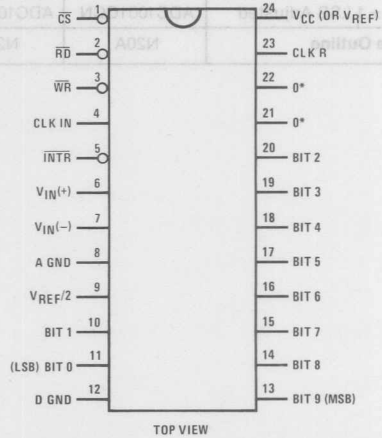


FIGURE 3. Full-Scale Adjust

Dual-In-Line Package

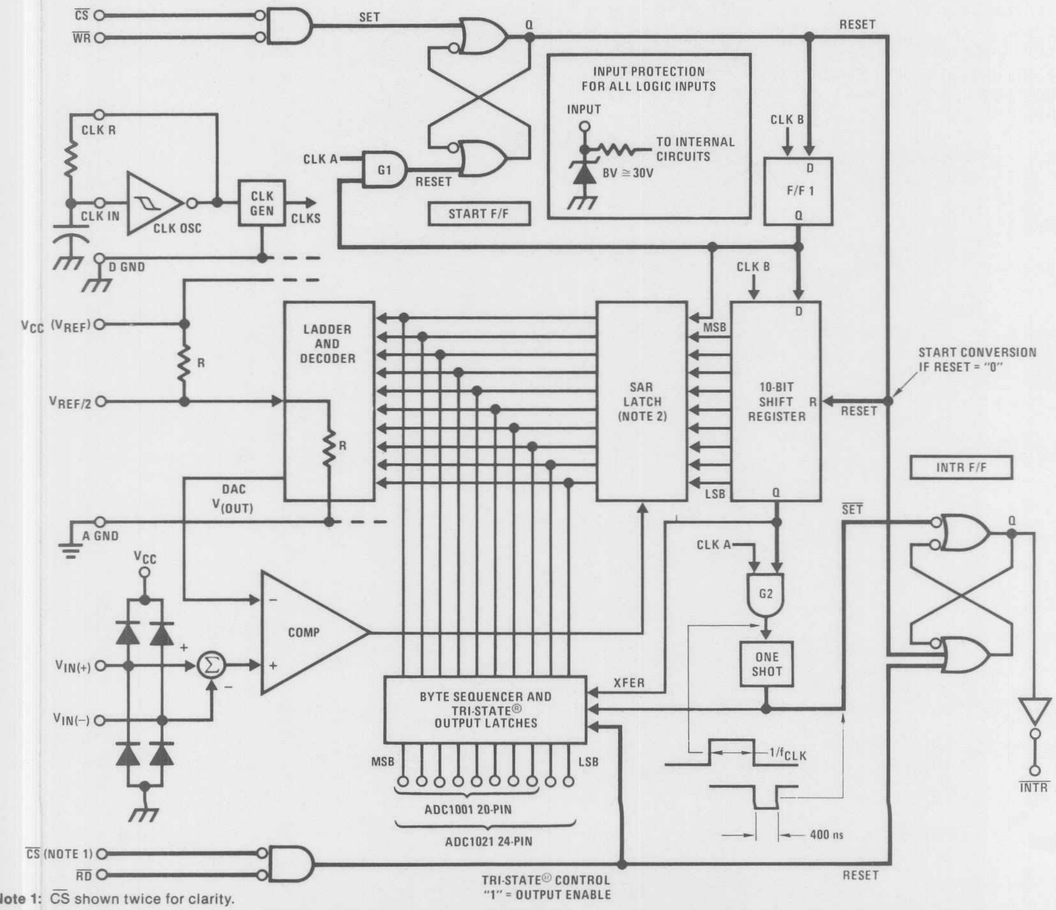


Dual-In-Line Package



*TRI-STATE® output buffers which output 0 during $\overline{RD}$.

Block Diagram



Note 1: $\overline{CS}$ shown twice for clarity.

Note 2: SAR = Successive Approximation Register.

FIGURE 1

Temperature Range		0°C to +70°C		−40°C to +85°C		−55°C to +125°C	
Error	± 1/2 LSB Adjusted	ADC1001BCN	ADC1021BCN	ADC1001BCD	ADC1021BCD	ADC1001BD	ADC1021BD
	± 1 LSB Adjusted	ADC1001CCN	ADC1021CCN	ADC1001CCD	ADC1021CCD	ADC1001CD	ADC1021CD
Package Outline		N20A	N24A	D20A	D24C	D20A	D24C

National Semiconductor

A to D, D to A
PRELIMINARY

ADC1080, ADC1280 12-Bit Successive Approximation A/D Converters

General Description

The ADC1080 and ADC1280 are complete successive approximation analog-to-digital converters that include an internal clock, reference and comparator.

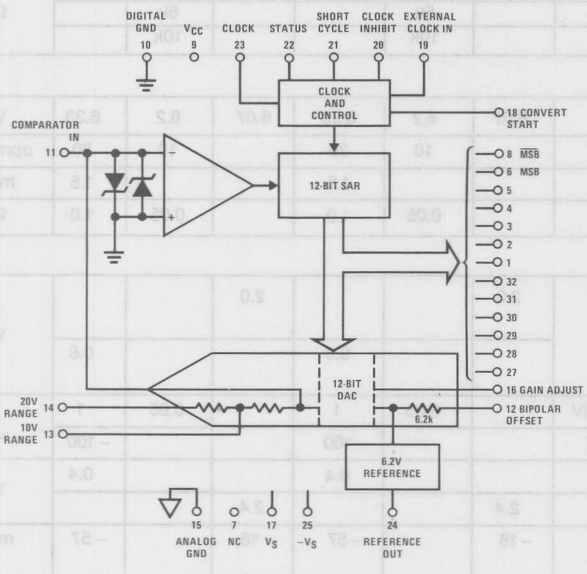
The design of the ADC1080 and ADC1280 includes scaling resistors that provide analog signal ranges of ±2.5V, ±5.0V, ±10V, 0V to 5V, or 0V to 10V. The 6.2V precision reference may be used for external applications. All digital signals are fully TTL compatible; output data may be read in both serial and parallel form.

The ADC1280 has a maximum linearity of 0.012% of FSR and the ADC1080 has a maximum linearity of 0.048% of FSR. Both grades are specified for use over the −25°C to +85°C temperature range and both are available in a 32-pin DIP.

Features

- Completely self-contained with internal reference, clock, and comparator
- High reliability exact replacement for ADC80
- ±1/2 LSB linearity for ADC1280
- Input voltage ranges of ±2.5V, ±5V, ±10V, 0V to 5V, and 0V to 10V
- 6.2V reference available for external use at 1.5 mA
- Conversion speed—22 μs
- Short cycle and external clock options for faster conversion time

Block Diagram



Connection Diagram

Dual-In-Line Package

Absolute Maximum Ratings

Supply Voltage (V^+ and V^-)	±18V	Operating Temperature Range	−55°C to +100°C
Logic Supply Voltage	7V	Storage Temperature Range	−65°C to +150°C
Reference Input Voltage (V_{REF})	0V, 18V	Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

$T_A = -25°C$ to $+85°C$, $V_S = \pm 11.4V$ to $\pm 16.00V$, $V_{CC} = 4.75V$ to $5.25V$ unless otherwise noted.

Parameter	Conditions	ADC1280 Min	ADC1280 Typ (Note 1)	ADC1280 Max	ADC1080 Min	ADC1080 Typ (Note 1)	ADC1080 Max	Units
CONVERTER CHARACTERISTICS								
Resolution		12			10			Bits
Linearity Error	$T_A = 25°C$			±0.012			±0.048	% FSR (Note 3)
Linearity Error Tempco				±3			±3	ppm of FSR/°C
Differential Linearity Error			±1/2			±1/2		LSB
No Missing Codes	(Note 2)	12			10			Bits
Full-Scale (Gain) Error	$T_A = 25°C$ (Note 4)		±0.1			±0.1		% FSR
Zero-Scale (Offset) Error	$T_A = 25°C$ (Note 4) Unipolar		±0.05			±0.05		%FSR
	$T_A = 25°C$ (Note 4) Bipolar		±0.1			±0.1		%FSR
Full-Scale (Gain) Tempco				±30			±30	ppm/°C
Zero-Scale (Offset) Tempco	Unipolar			±3			±3	ppm of FSR/°C
	Bipolar			±15			±15	ppm of FSR/°C
Analog Input Voltage Range	Unipolar	0V to 5V, 0V to 10V						V
	Bipolar	±2.5V, ±5V, ±10V						V
Input Impedance (Direct Input)	0V to 5V, ±2.5V		2.5k			2.5k		Ω
	0V to 10V, ±5V		5k			5k		Ω
	±10V		10k			10k		Ω
REFERENCE CHARACTERISTICS								
Reference Voltage		6.07	6.2	6.33	6.07	6.2	6.33	V
Tempco of Drift			10	20		10	20	ppm/°C
External Use Current				1.5			1.5	mA
Output Impedance			0.05	1.0		0.05	1.0	Ω
DIGITAL AND DC CHARACTERISTICS								
Logic 1 Input Voltage (Bit Off)	Incl Ext Clock Input	2.0			2.0			V
Logic 0 Input Voltage (Bit On)	Incl Ext Clock Input			0.8			0.8	V
Logic 1 Input Current	Incl Ext Clock Input, $V_{IN} = 2.5V$		0.05	1		0.05	1	μA
Logic 0 Input Current	Incl Ext Clock Input, $V_{IN} = 0V$			−100			−100	μA
Logic 0 Output Voltage	$I_{OUT} = 3.2$ mA			0.4			0.4	V
Logic 1 Output Voltage	$I_O = 360$ μA	2.4			2.4			V
Short Circuit Output Current	$V_{CC} = $ Max	−18		−57	−18		−57	mA
Power Supply Current	$T_A = 25°C$, I^+		16			16		mA
	$T_A = 25°C$, I^-		12			12		mA
	$T_A = 25°C$, I_{CC}		92			92		mA
Power Supply Sensitivity	V_S		0.003			0.003		FSR/% V_S
	V_{CC}		0.0015			0.0015		FSR/% V_{CC}

Electrical Characteristics (Continued)

$T_A = -25°C$ to $+85°C$, $V_S = \pm 11.4V$ to $\pm 16.00V$, $V_{CC} = 4.75V$ to $5.25V$ unless otherwise noted.

Parameter	Conditions		ADC1280 Min	ADC1280 Typ (Note 1)	ADC1280 Max	ADC1080 Min	ADC1080 Typ (Note 1)	ADC1080 Max	Units
AC CHARACTERISTICS									
Conversion Time	$T_A = 25°C$	Internal Clock		22	25			21	μs
		External Clock		16	18			12	μs
Clock Frequency	Internal			575			575		kHz
Convert Command			100			100			ns

Note 1: All typical values are for $T_A = 25°C$.

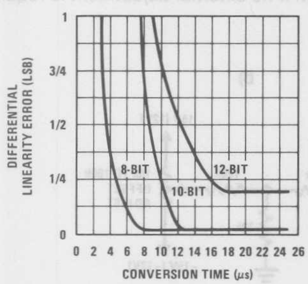
Note 2: Guarantees that for increasing analog voltage, the digital code increases. This specification guarantees monotonicity.

Note 3: FSR means "full-scale range" and is 20V for ±10V range, 10V for ±5V range.

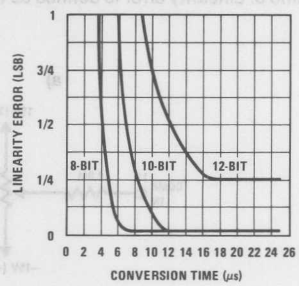
Note 4: Externally adjustable to zero.

Typical Performance Curves

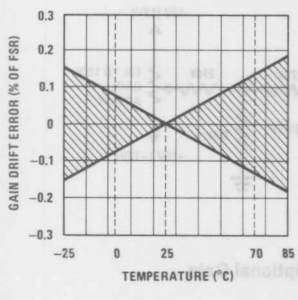
Linearity Error vs Conversion Time (Normalized)



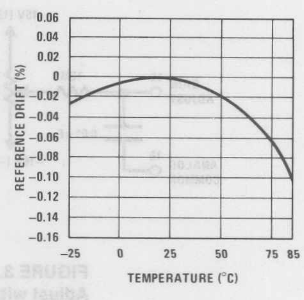
Differential Linearity Error vs Conversion Time (Normalized)



Maximum Gain Drift Error—% of FSR vs Temperature



Reference Drift—% Error vs Temperature



transfer function shown in *Figure 1.* There is an inherent quantization uncertainty of ± 1/2 LSB associated with the resolution.

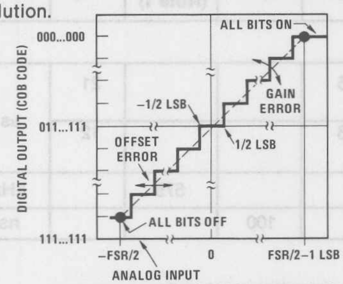


FIGURE 1. Transfer Characteristics for an Ideal Bipolar A/D

The remaining errors in the A/D converters are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, reference error, and power supply rejection. The matching and tracking errors in the ADC1080 and ADC1280 have been minimized by the use of a monolithic DAC that includes the scaling network. The initial gain and offset errors are specified at ± 0.1% FSR for gain and ± 0.05% FSR for offset. These errors may be trimmed to zero by the use of the external trim circuits as shown in *Figures 2 and 3*. Linearity error is defined as the deviation verter accuracy. Differential nonlinearity is a measure of the deviation in staircase step width between codes from the ideal least significant bit step size *(Figure 1).*

Monotonic behavior requires that the differential linearity error be less than 1 LSB; however, a monotonic converter can have missing codes.

There are three types of drift error over temperature: offset, gain, and linearity. Offset drift causes a shift of the transfer characteristics left or right over the operating temperature range. Gain drift causes a rotation of the transfer characteristic about the zero or minus full-scale point.

1.1 Gain and Offset Error

Initial gain and offset errors are factory trimmed to ± 0.1% of FSR (± 0.05% for unipolar offset) at 25°C.

Gain and offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC1080 and ADC1280 as shown in *Figures 2 and 3*. Multiturn potentiometers with 100 ppm/°C or better TCRs are recommended for minimum drift over temperature and time. These pots may be any value from 10 kΩ to 100 kΩ. All resistors should be 20% or better. Pin 16 (gain adjust) may be left open if no external adjustment is required.

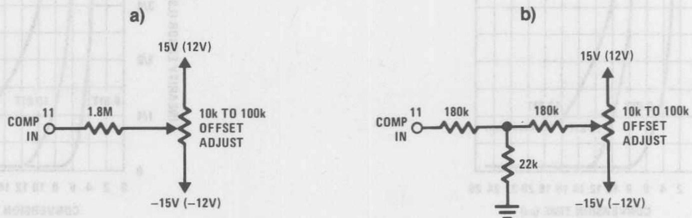


FIGURE 2. Two Methods of Connecting Optional Offset Adjust with a 0.4% of FSR Range of Adjustment

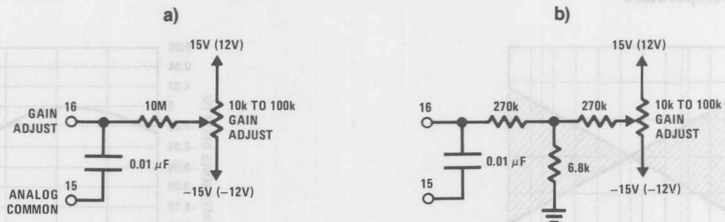


FIGURE 3. Two Methods of Connecting Optional Gain Adjust with a 0.6% Range of Adjustment

Adjustment Procedure

Offset—Connect the offset potentiometer as shown in *Figure 2*. Sweep the input through the end point transition voltage that should cause an output transition to all ones.

Adjust the offset potentiometer until the actual end point transition voltage occurs at E_{IN}^{OFF}. The ideal transition voltage values of the input are given in Table I.

Gain—Connect the gain adjust potentiometer as shown in *Figure 3*. Sweep the input through the end point transition voltage that should cause an output transition to all zeros.

Adjust the gain potentiometer until the actual end point transition voltage occurs E_{IN}^{ON}. Table I details the transition voltage levels required.

1.2 Accuracy Drift vs Temperature

Three major drift parameters degrade A/D converter accuracy over temperature: they are gain, offset and linearity drift. The worst case accuracy drift is the summation of all three drift errors over temperature. Statistically, these errors do not add algebraically, but are random variables which behave as root-sum-squared (RSS) or 1σ errors as follows:

$$RSS = \sqrt{\in g^2 + \in o^2 + \in e^2}$$

where $\in g$ = gain drift error (ppm/°C)

$\in o$ = offset drift error (ppm of FSR/°C)

$\in e$ = linearity error (ppm of FSR/°C)

For *unipolar* operation, the total RSS drift is ±30.3 ppm/°C and for *bipolar* operation, the total RSS drift is ±33.7 ppm/°C.

1.3 Accuracy vs Speed

In successive approximation A/D converters, the conversion speed affects linearity and differential linearity errors. Conversion speed and its effect on linearity and differential linearity errors for the ADC1080 and ADC1280 are shown in *Figures 3 and 4*.

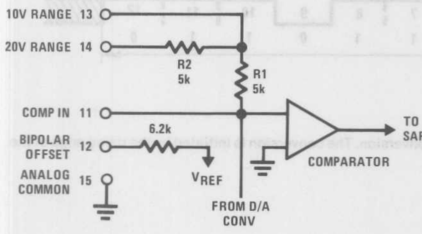


FIGURE 4. Input Scaling Circuit

The ADC1080 and ADC1280 conversion speeds are specified for a maximum linearity error of ±1/2 LSB and a differential linearity error of ±1/2 LSB with the internal clock. Faster conversion speeds up to 23 µs for 12 bits, 12 µs for 10 bits, and 6 µs for 8 bits are possible with an external clock.

1.4 Power Supply Sensitivity

Changes in the DC power supplies will affect the accuracy of the ADC1080 and ADC1280. Normally, regulated power supplies with 1% or less ripple are recommended.

1.5 Layout Precautions

Analog and digital commons are not connected internally in the ADC1080 and ADC1280, but should be connected together as close to the unit as possible, preferably to a large ground plane under the A/D. If these grounds must be run separately, use a wide conductor pattern between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout.

1.6 Input Scaling

The ADC1080 and ADC1280 input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table I. See *Figure 4* for circuit details.

TABLE I. INPUT SCALING CONNECTIONS

Input Signal Range	Output Code	Connect Pin 12 To Pin	Connect Pin 14 To	Connect Input Signal To
±10V	COB or CTC	11	Input Signal	14
±5V	COB or CTC	11	Open	13
±2.5V	COB or CTC	11	Pin 11	13
0V to 5V	CSB	15	Pin 11	13
0V to 10V	CSB	15	Open	13

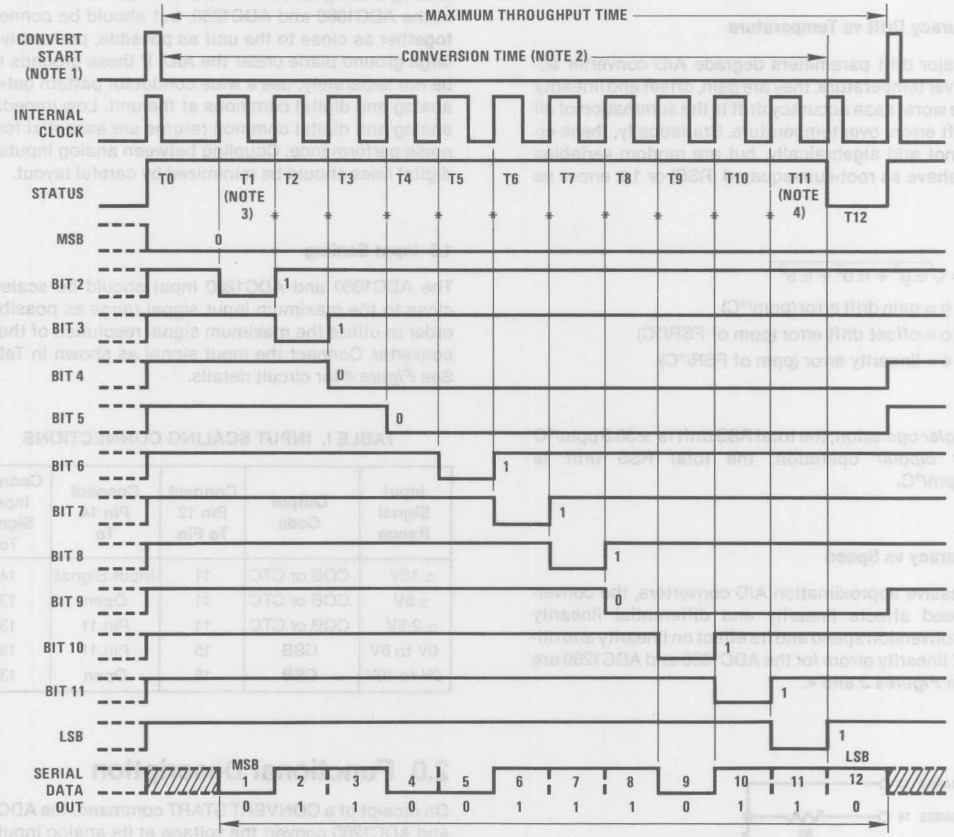
2.0 Functional Description

On receipt of a CONVERT START command, the ADC1080 and ADC1280 convert the voltage at its analog input into an equivalent 12-bit binary number. This conversion is accomplished as follows: the 12-bit successive approximation register (SAR) has its 12-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

2.1 Timing

The Timing Diagram is shown in *Figure 5*. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through 13 cycles. All SAR parallel bit and STATUS flip-flops are initialized on the leading edge, and the gated clock inhibit signal is removed on the trailing edge of the CONVERT START signal. At time t0, B1 is reset and B2–B12 are set unconditionally. At t1 the bit 1 decision is made (keep) and bit 2 is unconditionally reset. At t2, the bit 2 decision is made (keep) and bit 3 is reset unconditionally. This sequence continues until the bit 12 (LSB) decision (keep) is made at t12. After a 40 ns delay period, the STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the Logic 0 state.

Corresponding serial and parallel data bits become valid on the same positive-going clock edge. Serial data does not change and is guaranteed valid on negative-going clock edges, however; serial data can be transferred quite simply by clocking it into a receiving shift register on these edges (see *Figure 5*).



Note 1: The convert start pulse width is 100 ns min and must remain low during a conversion. The conversion is initiated by the rising edge of the convert command.

Note 2: 25 μs for 12 bits and 21 μs for 10 bits (max).

Note 3: MSB decision.

Note 4: LSB decision 40 ns prior to the status going low.

* Bit decisions

FIGURE 5. Timing Diagram (Binary Code 011001110110)

Incorporation of this 40 ns delay guarantees that the parallel (and serial) data are valid at the Logic 1 to Logic 0 transition of the STATUS flag, permitting parallel data transfer to be initiated by the trailing edge of the STATUS signal.

2.2 Digital Output Data

Both parallel and serial data from TTL storage registers are in negative true form. Parallel data output coding is complementary binary for unipolar ranges and either complementary offset binary or complementary two's complement binary, depending on whether bit 1 (pin 6) or its logical inverse bit 1 (pin 8) is used as the MSB. Parallel data becomes valid approximately 40 ns before the STATUS flag returns to Logic 0, permitting parallel data transfer to be clocked on the "1" to "0" transition of the STATUS flag.

Serial data coding is complementary binary for unipolar input ranges and complementary offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid 200 ns after the rising clock edges, permitting serial data to be clocked directly into a receiving register on these edges as shown in *Figure 5.* There are 13 negative-going clock edges in the complete 12-bit conversion cycle, as shown in *Figure 5.* The first edge shifts an invalid bit into the register, which is shifted out on the 13th negative-going clock edge. All serial data bits will have been correctly transferred and be in the receiving shift register locations shown at the completion of the conversion period.

2.3 Short Cycle Input

A short cycle input, pin 21, permits the timing cycle shown in *Figure 5* to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 12-bit resolution. When 12-bit resolution is required, pin 21 is connected to 5V (pin 9). When 10-bit resolution is desired, pin 21 is connected to bit 11 output pin 28. The conversion cycle then terminates, and the STATUS flag resets after the bit 10 decision (t10 + 40 ns in the Timing Diagram of *Figure 5*). Short cycle pin connections and associated maximum 12-bit, 10-bit and 8-bit conversion times are summarized in Table II.

TABLE II. SHORT CYCLE CONNECTIONS

Connect Short Cycle Pin 21 To Pin	Bits	Resolution (% FSR)	Maximum Conversion Time (μs)	Status Flag Reset
9	12	0.024	25	t12 + 40 ns
28	10	0.100	21	t10 + 40 ns
30	8	0.390	17	t8 + 40 ns

2.4 Control Modes

The timing sequence of the ADC1080 and ADC1280 allows the device to be easily operated in a variety of systems with different control modes. The most common control modes are illustrated in *Figures 6–9.*

2.5 Calibration

External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in *Figures 10 and 11*, are used for device calibration. To prevent interaction of these two adjustments, zero is always adjusted first and then gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and − FS for bipolar input ranges). Gain is adjusted with the analog input near the most postive end of the analog range.

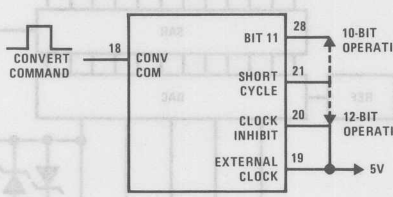


FIGURE 6. Internal Clock—Normal Operating Mode. Conversion Initiated by the Rising Edge of the Convert Command. The Internal Clock Runs Only During Conversion.

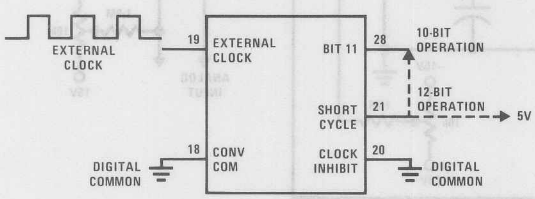


FIGURE 7. Continuous Conversion with External Clock. Conversion is Initiated by 14th Clock Pulse. Clock Runs Continuously.

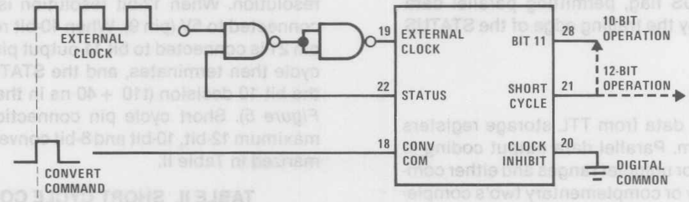


FIGURE 8. Continuous External Clock. Conversion Initiated by Rising Edge of Convert Command. The Convert Command Must be Synchronized with Clock.

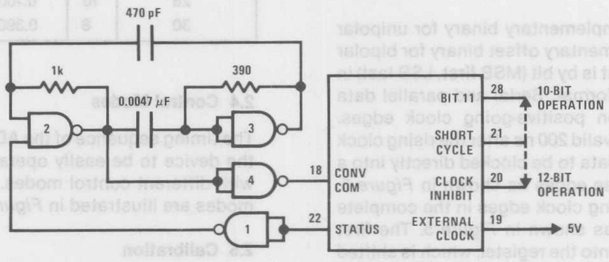


FIGURE 9. Continuous Conversion with Internal Clock. Conversion is Initiated by the 14th Clock Pulse. Clock Runs Continuously. The Oscillator Formed by Gates 2 and 3 Insures that the Conversion Process will Start When Logic Power is First Turned On.

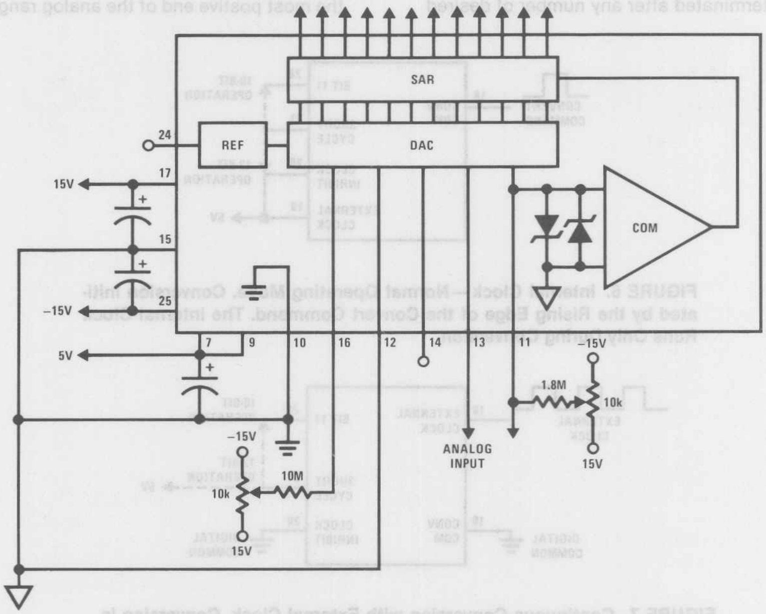


FIGURE 10. Analog and Power Connections for Unipolar 0V–10V Input Range

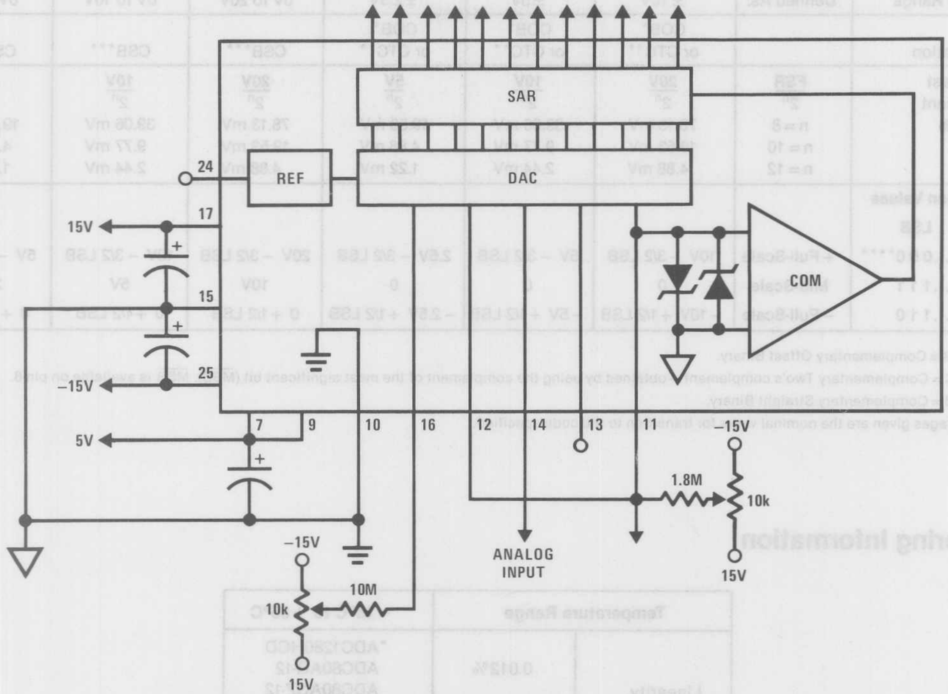


FIGURE 11. Analog and Power Connections for Bipolar ±10V Input Range

0V to 10V Range: Set analog input to +1 LSB = +0.0024V. Adjust zero for digital output = 1 1 1 1 1 1 1 1 1 1 1 0. Zero is now calibrated. Set analog input to +FSR −2 LSB = +9.9952V. Adjust gain for 0 0 0 0 0 0 0 0 0 0 0 1 digital output code; full-scale (gain) is now calibrated. Half-scale calibration check: set analog input to +5.0000V; digital output code should be 0 1 1 1 1 1 1 1 1 1 1 1.

−10V to +10V Range: Set analog input to −9.9951V; adjust zero for 1 1 1 1 1 1 1 1 1 1 1 0 digital output (complementary offset binary) code. Set analog input to +9.9902V; adjust gain for 0 0 0 0 0 0 0 0 0 0 0 1 digital output (complementary offset binary) code. Half-scale calibration check: set analog input to 0.0000V; digital output (complementary offset binary) code should be 0 1 1 1 1 1 1 1 1 1 1 1.

Other Ranges: Representative digital coding for 0V to 10V and −10V to +10V ranges is given above. Coding relationships and calibration points for 0V to 5V, −2.5V to +2.5V and −5V to +5V ranges can be found by halving the corresponding code equivalents listed for the 0V to 10V and −10V to +10V ranges, respectively.

Zero and full-scale calibration can be accomplished to a precision of approximately ±1/4 LSB using the static adjustment procedure described in paragraph 1.1. By summing a small sine or triangular wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level.

TABLE III. INPUT VOLTAGES AND CODE DEFINITIONS

Binary (BIN) Output	INPUT VOLTAGE RANGE AND LSB VALUES						
Analog Input Voltage Range	Defined As:	± 10V	± 5V	± 2.5V	0V to 20V	0V to 10V	0V to 5V
Code Designation		COB* or CTC**	COB* or CTC**	COB* or CTC**	CSB***	CSB***	CSB***
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$
	n = 8	78.13 mV	39.06 mV	19.53 mV	78.13 mV	39.06 mV	19.53 mV
	n = 10	19.53 mV	9.77 mV	4.88 mV	19.53 mV	9.77 mV	4.88 mV
	n = 12	4.88 mV	2.44 mV	1.22 mV	4.88 mV	2.44 mV	1.22 mV
Transition Values **MSB LSB**							
0 0 0...0 0 0****	+ Full-Scale	10V − 3/2 LSB	5V − 3/2 LSB	2.5V − 3/2 LSB	20V − 3/2 LSB	10V − 3/2 LSB	5V − 3/2 LSB
0 1 1...1 1 1	Mid-Scale	0	0	0	10V	5V	2.5V
1 1 1...1 1 0	− Full-Scale	− 10V + 1/2 LSB	− 5V + 1/2 LSB	− 2.5V + 1/2 LSB	0 + 1/2 LSB	0 + 1/2 LSB	0 + 1/2 LSB

*COB = Complementary Offset Binary.

**CTC = Complementary Two's complement—obtained by using the complement of the most significant bit ($\overline{MSB}$). $\overline{MSB}$ is available on pin 8.

***CSB = Complementary Straight Binary.

****Voltages given are the nominal value for transition to the code specified.

Ordering Information

Temperature Range		− 25°C to + 85°C
Linearity (Accuracy)	0.012%	*ADC1280HCD ADC80AG-12 ADC80AGZ-12
	0.048%	*ADC1080HCD ADC80AG-10 ADC80AGZ-10
Package		D32B

*Devices may be ordered by either part number

National Semiconductor

ADC1210, ADC1211 12-Bit CMOS A/D Converters

General Description

The ADC1210, ADC1211 are low power, medium speed, 12-bit successive approximation, analog-to-digital converters. The devices are complete converters requiring only the application of a reference voltage and a clock for operation. Included within the device are the successive approximation logic, CMOS analog switches, precision laser trimmed thin film R-2R ladder network and FET input comparator.

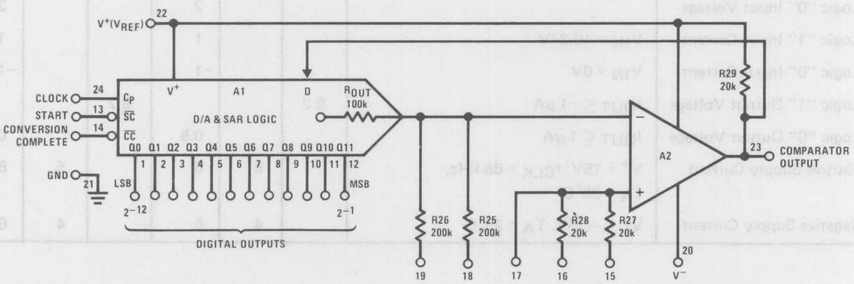
The ADC1210 offers 12-bit resolution and 12-bit accuracy, and the ADC1211 offers 12-bit resolution with 10-bit accuracy. The inverted binary outputs are directly compatible with CMOS logic. The ADC1210, ADC1211 will operate over a wide supply range, convert both bipolar and unipolar analog inputs, and operate in either a continuous conversion mode or logic-controlled START-STOP conversion mode. The devices are capable of making a 12-bit conversion in 100 μs typ, and can be connected to convert 10 bits in 30 μs.

Both devices are available in military and industrial temperature ranges.

Features

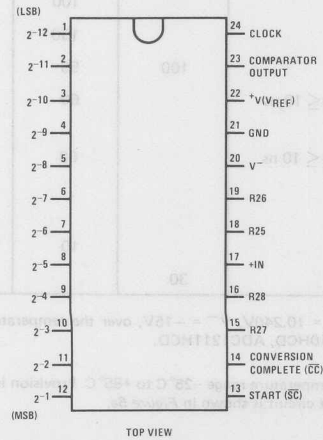
- 12-bit resolution
- ±1/2 LSB linearity
- Single +5V to ±15V supply range
- 100 μs 12-bit, 30 μs 10-bit conversion rate
- CMOS compatible outputs
- Bipolar or unipolar analog inputs
- 200 kΩ analog input impedance
- Low cost

Block Diagram



Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number ADC1210HCD, ADC1211HCD, ADC1210HD or ADC1211HD
See NS Package D24D

Voltage At Any Logic Pin	$V^+ + 0.3V$	ADC1210HD, ADC1211HD	$-55^\circ C$ to $+125^\circ C$
Analog Input Voltage	±15V	ADC1210HCD, ADC1211HCD	$-25^\circ C$ to $+85^\circ C$
Maximum Digital Output Current	±10 mA	Storage Temperature Range	$-65^\circ C$ to $+150^\circ C$
Maximum Comparator Output Current	50 mA	Lead Temperature (Soldering, 10 seconds)	$300^\circ C$
Comparator Output Short-Circuit Duration	5 Seconds		

DC Electrical Characteristics (Notes 1 and 2)

PARAMETER	CONDITIONS	ADC1210 MIN	ADC1210 TYP	ADC1210 MAX	ADC1211 MIN	ADC1211 TYP	ADC1211 MAX	UNITS
Resolution		12			12			Bits
Linearity Error	(Note 3)							
	$f_{CLK} = 65$ kHz, $T_A = 25^\circ C$			±0.0122			±0.0488	% FS
	$f_{CLK} = 65$ kHz			±0.0244				% FS
Full Scale Error	$T_A = 25^\circ C$, Unadjusted			0.1			0.25	% FS
Zero Scale Error	$T_A = 25^\circ C$, Unadjusted			0.1			0.25	% FS
Quantization Error				±1/2			±1/2	LSB
Input Resistor Values	R27, R28		20			20		kΩ
Input Resistor Values	R25, R26		200			200		kΩ
Input Resistor Ratios	R25/R26, R27/R28			0.1			0.1	%
Logic "1" Input Voltage		8			8			V
Logic "0" Input Voltage				2			2	V
Logic "1" Input Current	$V_{IN} = 10.24V$			1			1	µA
Logic "0" Input Current	$V_{IN} = 0V$			−1			−1	µA
Logic "1" Output Voltage	$I_{OUT} \leq -1\ \mu A$	9.2			9.2			V
Logic "0" Output Voltage	$I_{OUT} \leq 1\ \mu A$			0.5			0.5	V
Positive Supply Current	$V^+ = 15V$, $f_{CLK} = 65$ kHz, $T_A = 25^\circ C$		5	8		5	8	mA
Negative Supply Current	$V^- = -15V$, $T_A = 25^\circ C$		4	6		4	6	mA

AC Electrical Characteristics $T_A = 25^\circ C$, (Notes 1 and 2)

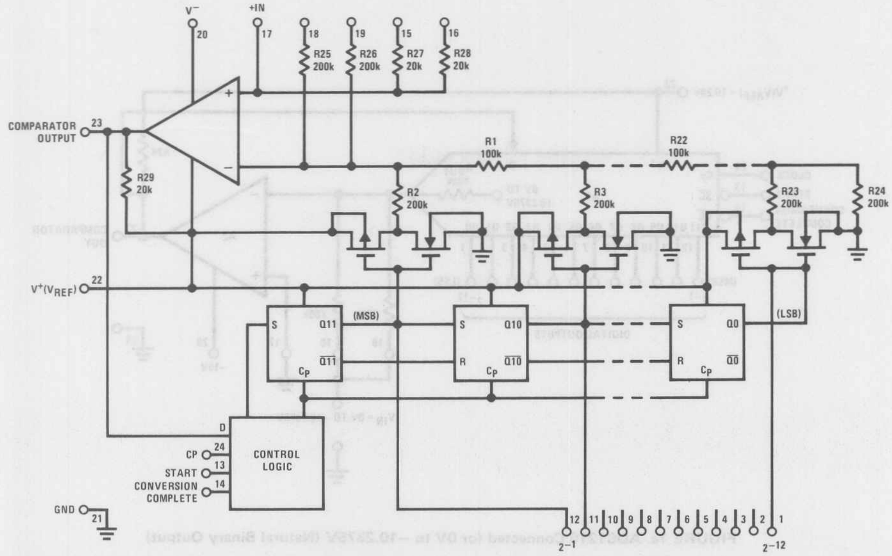
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Conversion Time			100	200	µs
Maximum Clock Frequency			130	65	kHz
Clock Pulse Width		100	50		ns
Propagation Delay From Clock to Data Output (Q0 to Q11)	$t_r \leq t_f \leq 10$ ns		60	150	ns
Propagation Delay From Clock to Conversion Complete	$t_r \leq t_f \leq 10$ ns		60	150	ns
Clock Rise and Fall Time				5	µs
Input Capacitance			10		pF
Start Conversion Set-Up Time		30			ns

Note 1: Unless otherwise noted, these specifications apply for $V^+ = 10.240V$, $V^- = -15V$, over the temperature range $-55^\circ C$ to $+125^\circ C$ for the ADC1210HD, ADC1211HD, and $-25^\circ C$ to $+85^\circ C$ for the ADC1210HCD, ADC1211HCD.

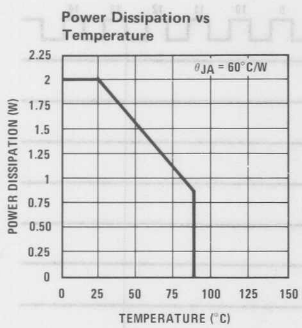
Note 2: All typical values are for $T_A = 25^\circ C$.

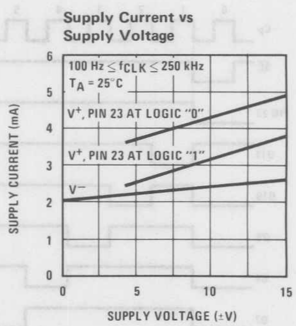
Note 3: Unless otherwise noted, this specification applies over the temperature range $-25^\circ C$ to $+85^\circ C$. Provision is made to adjust zero scale error to 0V and full-scale to 10.2375V during testing. Standard linearity test circuit is shown in *Figure 5a*.

Schematic Diagram



Note: 3 bits shown for clarity





1.0 THEORY OF OPERATION

The ADC1210, ADC1211 are successive approximation analog-to-digital converters, i.e., the conversion takes place 1 bit at a time by comparing the output of the internal D/A to the (unknown) input voltage. The START input (pin 13), when taken low, causes the register to reset synchronously on the next CLOCK low-to-high transition. The MSB, Q11 is set to the low state, and the remaining bits, Q0 through Q10, will be set to the high state. The register will remain in this state until the $\overline{SC}$ input is taken high. When START goes high, the conversion will begin on the low-to-high transition of the CLOCK pulse. Q11 will then assume the state of pin 23. If pin 23 is high, Q11 will be high; if pin 23 is low, Q11 will remain low. At the same time, the next bit, Q10 is set low. All remaining bits, Q0–Q9 will remain unchanged (high). This process will continue until the LSB (Q0) is found. When the conversion process is completed, it is indicated by CONVERSION COMPLETE ($\overline{CC}$) (pin 14) going low. The logic levels at the data output pins (pins 1–12) are the complemented-binary representation of the converted analog signal with Q11 being the MSB and Q0 being the LSB. The register will remain in the above state until the $\overline{SC}$ is again taken low.

An application example is shown in *Figure 1*. In this case, a 0 to −10.2375V input is being converted using the ADC1210 with V^+ = 10.240V, V^- = −15V. *Figure 1b* is the timing diagram for full scale input. *Figure 1c* is the timing diagram for zero scale input, *Figure 1d* is the timing diagram for −3.4125V input (010101010101 = output).

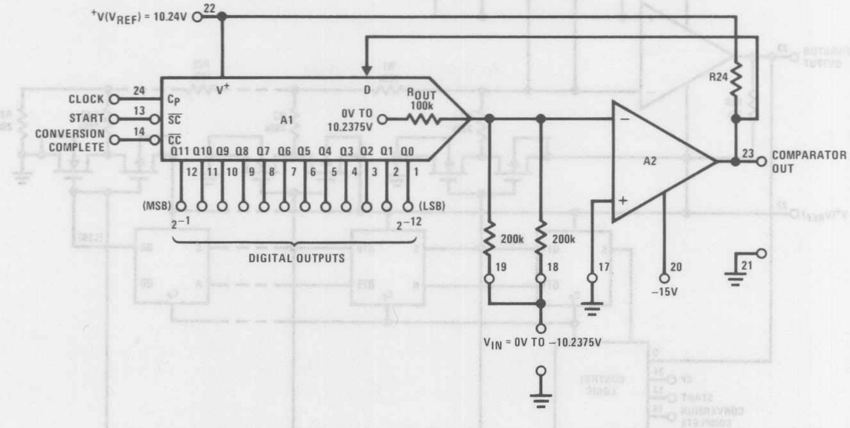


FIGURE 1a. ADC1210 Connected for 0V to −10.2375V (Natural Binary Output)

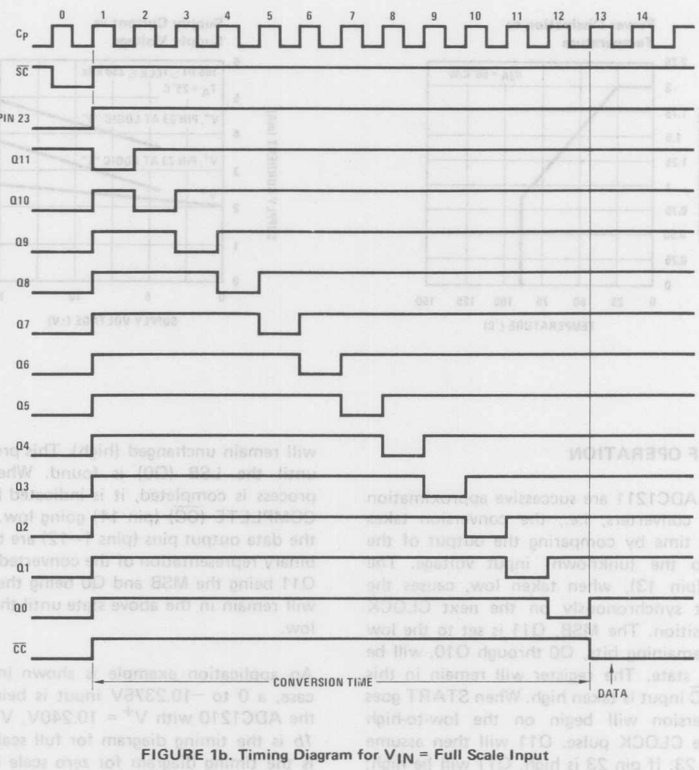


FIGURE 1b. Timing Diagram for V_{IN} = Full Scale Input

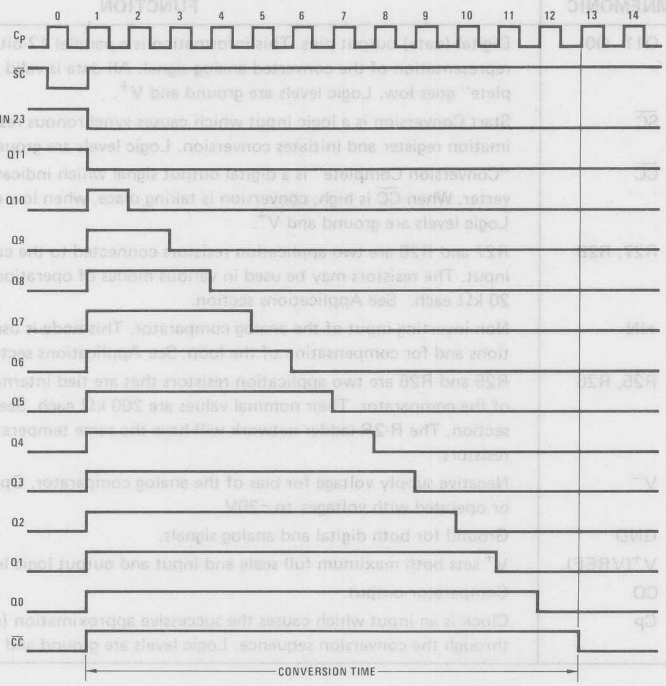


FIGURE 1c. Timing Diagram for V_{IN} = Zero Scale

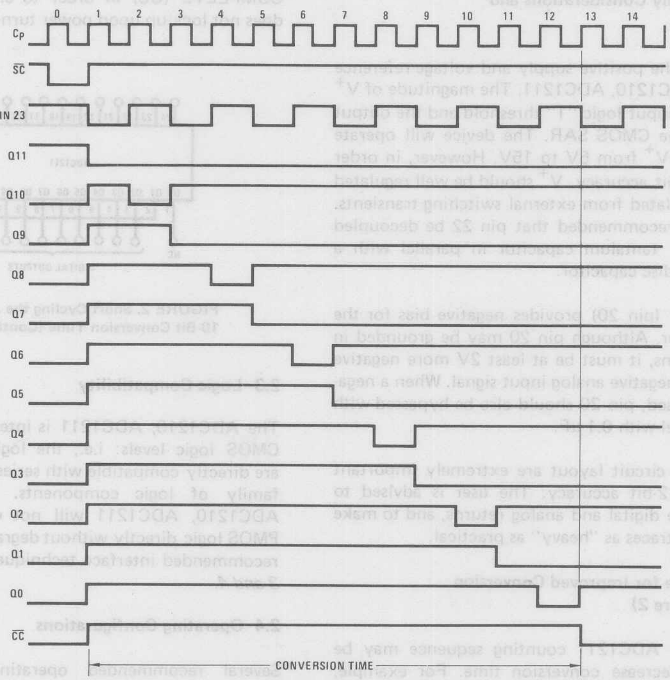


FIGURE 1d. Timing Diagram for V_{IN} = −3.4125V (010101010101)

1–12	Q11–Q0	Digital (data) output pins. This information is a parallel 12-bit complemented binary representation of the converted analog signal. All data is valid when "Conversion Complete" goes low. Logic levels are ground and V^+.
13	$\overline{SC}$	Start Conversion is a logic input which causes synchronous reset of the successive approximation register and initiates conversion. Logic levels are ground and V^+.
14	$\overline{CC}$	"Conversion Complete" is a digital output signal which indicates the status of the converter. When $\overline{CC}$ is high, conversion is taking place, when low conversion is completed. Logic levels are ground and V^+.
15, 16	R27, R28	R27 and R28 are two application resistors connected to the comparator non-inverting input. The resistors may be used in various modes of operation. Their nominal values are 20 kΩ each. See Applications section.
17	+IN	Non-inverting input of the analog comparator. This node is used in various configurations and for compensation of the loop. See Applications section.
18, 19	R25, R26	R25 and R26 are two application resistors that are tied internally to the inverting input of the comparator. Their nominal values are 200 kΩ each. See Applications section. The R-2R ladder network will have the same temperature coefficient as these resistors.
20	V^-	Negative supply voltage for bias of the analog comparator. Optionally may be grounded or operated with voltages to −20V.
21	GND	Ground for both digital and analog signals.
22	V^+(VREF)	V^+ sets both maximum full scale and input and output logic levels.
23	CO	Comparator output.
24	Cp	Clock is an input which causes the successive approximation (shift) register to advance through the conversion sequence. Logic levels are ground and V^+.

2.0 APPLICATIONS

2.1 Power Supply Considerations and Decoupling

Pin 22 is both the positive supply and voltage reference input to the ADC1210, ADC1211. The magnitude of V^+ determines the input logic "1" threshold and the output voltage from the CMOS SAR. The device will operate over a range of V^+ from 5V to 15V. However, in order to preserve 12-bit accuracy, V^+ should be well regulated (0.01%) and isolated from external switching transients. It is therefore recommended that pin 22 be decoupled with a 4.7 μF tantalum capacitor in parallel with a 0.1 μF ceramic disc capacitor.

The V^- supply (pin 20) provides negative bias for the FET comparator. Although pin 20 may be grounded in some applications, it must be at least 2V more negative than the most negative analog input signal. When a negative supply is used, pin 20 should also be bypassed with 4.7 μF in parallel with 0.1 μF.

Grounding and circuit layout are extremely important in preserving 12-bit accuracy. The user is advised to employ separate digital and analog returns, and to make these PC board traces as "heavy" as practical.

2.2 Short Cycle for Improved Conversion Time (Figure 2)

The ADC1210, ADC1211 counting sequence may be truncated to decrease conversion time. For example, when using the ADC1211, 2 clock intervals may be "saved" if 10-bit conversion accuracy is taking place. The Q2 output should be "OR'd" with CONVERSION COMPLETE ($\overline{CC}$) in order to ensure that the register does not lock-up upon power turn-on.

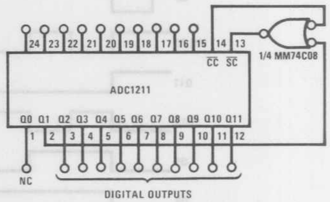


FIGURE 2. Short Cycling the ADC1211 to Improve 10-Bit Conversion Time (Continuous Conversion)

2.3 Logic Compatibility

The ADC1210, ADC1211 is intended to interface with CMOS logic levels: i.e., the logic inputs and outputs are directly compatible with series 54C/74C and CD4000 family of logic components. The outputs of the ADC1210, ADC1211 will not drive LPTTL, TTL or PMOS logic directly without degrading accuracy. Various recommended interface techniques are shown in *Figures 3 and 4*.

2.4 Operating Configurations

Several recommended operating configurations are shown in *Figure 5*.

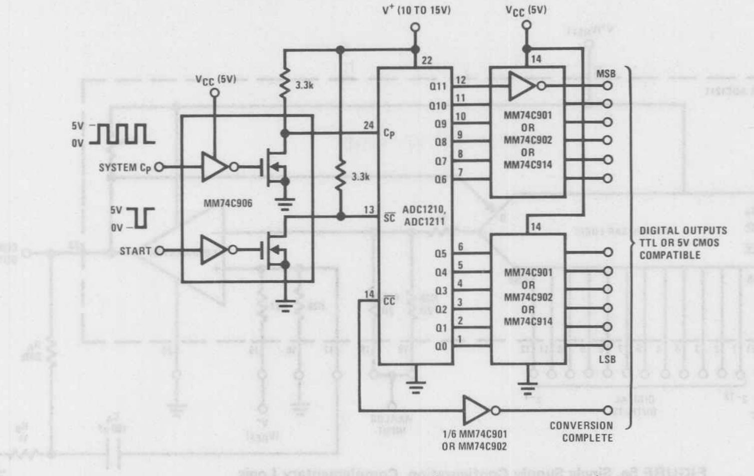


FIGURE 3. Interfacing an ADC1210, ADC1211 Running on $V^+ > V_{CC}$. Example: $V^+ = 10.24V$, System $V_{CC} = 5V$

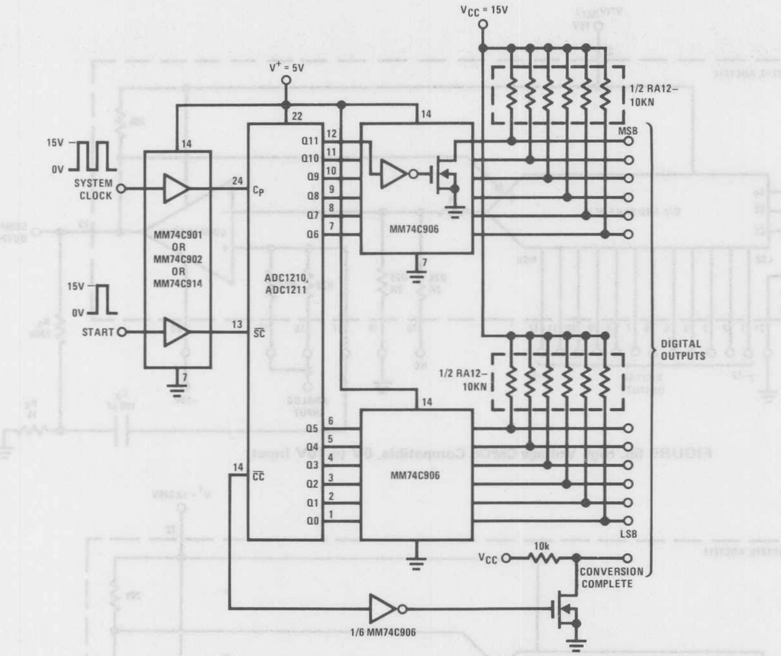
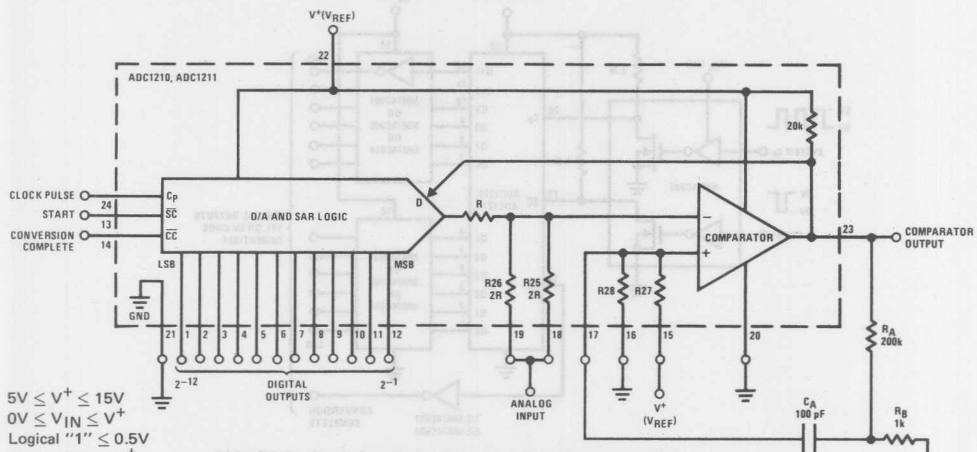


FIGURE 4. Interfacing an ADC1210, ADC1211 Running on $V^+ < V_{CC}$. Example: $V^+ = 5V$, $V_{CC} = 15V$

2.5 Offset and Full Scale Adjust

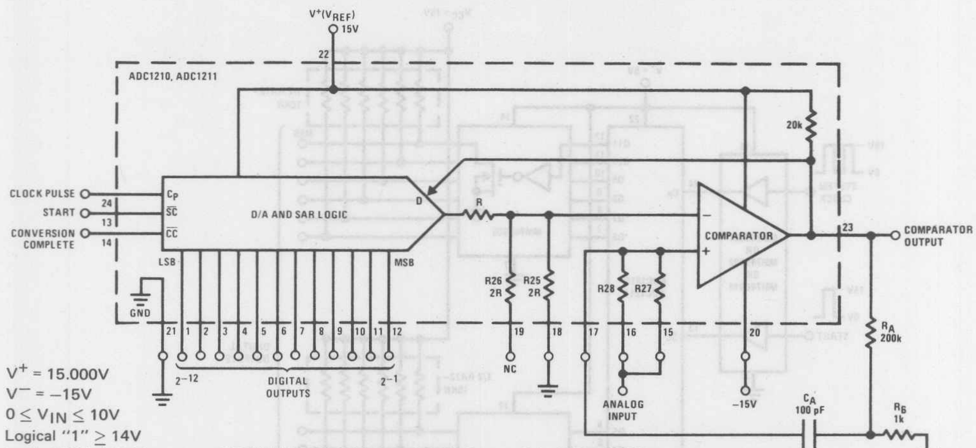
A variety of techniques may be employed to adjust Offset and Full Scale on the ADC1210, ADC1211. A straight-forward Full Scale Adjust is to incrementally vary V^+ (V_{REF}) to match the analog input voltage. A recommended technique is shown in *Figure 6*. An LM199 and low drift op amp (e.g., the LH0044) are used to provide the precision reference. The ADC1210, ADC1211 is put in the continuous convert mode by shorting pins 13 and 14. An analog voltage equal to V_{REF} minus 1 1/2 LSB (10.23625V) is applied to pins 18 and 19, and R1 is adjusted until the LSB flickers equally between logic "1" and logic "0" (all other outputs must be stable logic "0"). Offset Null is accomplished by then applying an analog input voltage equal to 1/2 LSB at pins 18 and 19. R2 is adjusted until the LSB output flickers equally between logic "1" and logic "0" (all other bits are stable). In the circuit of *Figure 6*, the ADC1210, ADC1211 is configured for Complementary Binary logic and the values shown are for $V^+ = 10.240V$, $V_{FS} = 10.2375V$, LSB = 2.5 mV.

An alternate technique is shown in *Figure 7*. In this instance, an LH0071 is used to provide the reference voltage. An analog input voltage equal to V_{REF} minus 1 1/2 LSB (10.23625V) is applied to pins 18 and 19.



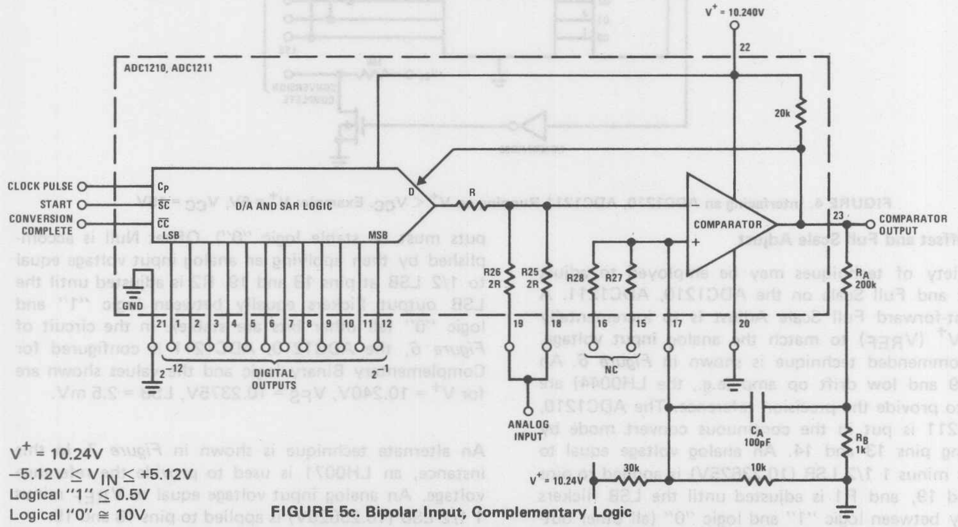
$5V \leq V^{+} \leq 15V$
$0V \leq V_{IN} \leq V^{+}$
Logical "1" $\leq 0.5V$
Logical "0" $\cong V^{+}$

FIGURE 5a. Single Supply Configuration, Complementary Logic



$V^{+} = 15.000V$
$V^{-} = -15V$
$0 \leq V_{IN} \leq 10V$
Logical "1" $\geq 14V$
Logical "0" $\leq 0.5V$

FIGURE 5b. High Voltage CMOS Compatible, 0V to 10V Input



$V^{+} = 10.24V$
$-5.12V \leq V_{IN} \leq +5.12V$
Logical "1" $\leq 0.5V$
Logical "0" $\cong 10V$

FIGURE 5c. Bipolar Input, Complementary Logic

Applications Information (Continued)

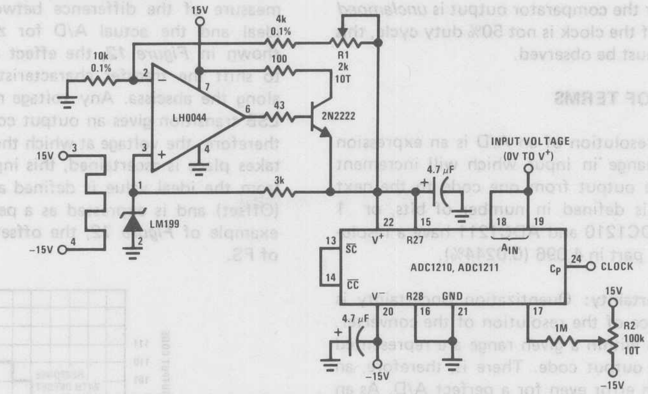


FIGURE 6. Offset and Full Scale Adjustment for Complementary Binary

R1 is adjusted until the LSB output flickers equally between logic "1" and logic "0" (all other outputs must be a stable logic "0"). For Offset Null, an analog voltage equal to 1/2 LSB (1.25 mV) is then applied to pins 18 and 19, and R2, is adjusted until the LSB output flickers equally between logic "1" and "0".

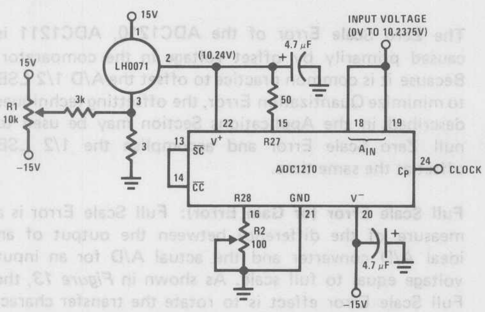


FIGURE 7. Offset and Full-Scale Adjustment Technique Using LH0071

In both techniques shown, adjusting the Full-Scale first and then Offset minimizes adjustment interaction. At least one iteration is recommended as a self-check.

2.6 Start Pulse Considerations

To assure reliable conversion accuracy, the START (SC) pulse applied to pin 13 of the ADC1210 should be synchronized to the conversion clock. One simple way to do that is the circuit shown in *Figure 8.* Note that once a conversion cycle is initiated, the $\overline{\text{START}}$ signal cannot effect the conversion operation until it is completed.

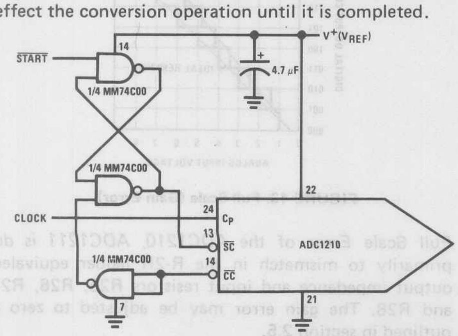


FIGURE 8. Synchronizing the $\overline{\text{START}}$ Pulse

The circuit insures that in no case can the ADC1210 make an error in the Most Significant Bit (MSB) decision. Without the circuit, it is possible for energy from the trailing edge of an asynchronous $\overline{\text{START}}$ pulse to be coupled into the ADC1210's comparator. If the analog input is near half-scale, the charge injected can force an error in the MSB decision. The circuit allows one clock period for this energy to dissipate before the decision is recorded.

2.7 ADC1210 Conversion at 26 μs

The ADC1210 can run at 500 kHz clock frequency, or 12-bit conversion time of 26 μs *(Figure 9)*. The comparator output is clamped low until the successive approximation register (SAR) is ready to strobe in the data at the rising edge of the conversion clock. Comparator oscillation is suppressed and kept from influencing the conversion decisions, eliminating the need for the AC hysteresis circuit above clock frequency of 65 kHz that is recommended.

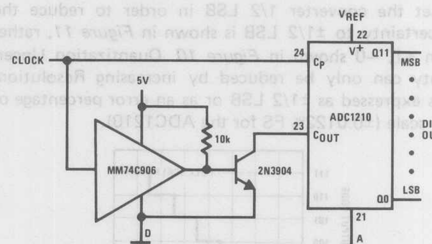


FIGURE 9. Conversion at 26 μs

A complementary phased clock is required. The positive phase is used to clock the converter SAR as is normally the case. The same signal is buffered and inverted by the transistor. The open collector is wire-ORed to the output of the comparator. During the first half of the clock cycle (50% duty cycle), the comparator output is clamped and disabled, though its internal operation is still in normal working order. The last half cycle of the clock unclamps the comparator output. Thus, the output is permitted to slew to the final logic state just before the decision is logged into the SAR. The MM74C906 buffer (or with two inverting buffers) provides adequate propogation delay such that the comparator output data is held long enough to resolve any internal logic setup time requirements.

3.0 DEFINITION OF TERMS

Resolution: The Resolution of an A/D is an expression of the smallest change in input which will increment (or decrement) the output from one code to the next adjacent code. It is defined in number of bits, or 1 part in 2^n. The ADC1210 and ADC1211 have a resolution of 12 bits or 1 part in 4,096 (0.0244%).

Quantization Uncertainty: Quantization Uncertainty is a direct consequence of the resolution of the converter. All analog voltages within a given range are represented by a single digital output code. There is, therefore, an inherent conversion error even for a perfect A/D. As an example, the transfer characteristic of a perfect 3-bit A/D is shown in *Figure 10*.

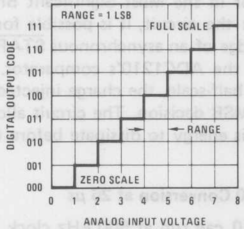


FIGURE 10. Quantization Uncertainty of a Perfect 3-Bit A/D

As can be seen, all input voltages between 0V and 1V are represented by an output code of 000. All input voltages between 1V and 2V are represented by an output code of 001, etc. If the midpoint of the range is assumed to be the nominal value (e.g., 0.5V), there is an Uncertainty of ±1/2 LSB. It is common practice to offset the converter 1/2 LSB in order to reduce the Uncertainty to ±1/2 LSB is shown in *Figure 11*, rather than +1, −0 shown in *Figure 10*. Quantization Uncertainty can only be reduced by increasing Resolution. It is expressed as ±1/2 LSB or as an error percentage of full scale (±0.0122% FS for the ADC1210).

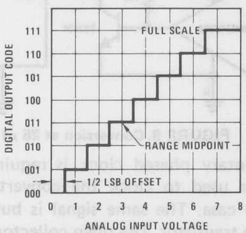


FIGURE 11. Transfer Characteristic Offset 1/2 LSB to Minimize Quantizing Uncertainty

Linearity Error: Linearity Error is the maximum deviation from a straight line passing through the end points of the A/D transfer characteristic. It is measured after calibrating Zero and Full Scale Error. The Linearity Error of the ADC1210 is guaranteed to be less than ±1/2 LSB or ±0.0122% of FS and ±0.0488% of FS for the AD1211. Linearity is a performance characteristic intrinsic to the device and cannot be externally adjusted.

Zero Scale Error (Offset): ... to shift the transfer characteristic to the right or left along the abscissa. Any voltage more negative than the LSB transition gives an output code of 000. In practice, therefore, the voltage at which the 000 to 001 transition takes place is ascertained, this input voltage's departure from the ideal value is defined as the Zero Scale Error (Offset) and is expressed as a percentage of FS. In the example of *Figure 12*, the offset is 2 LSB's or 0.286% of FS.

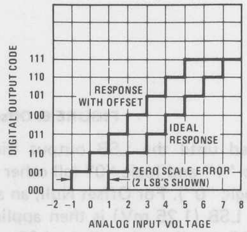


FIGURE 12. A/D Transfer Characteristic with Offset

The Zero Scale Error of the ADC1210, ADC1211 is caused primarily by offset voltage in the comparator. Because it is common practice to offset the A/D 1/2 LSB to minimize Quantization Error, the offsetting techniques described in the Applications Section may be used to null Zero Scale Error and accomplish the 1/2 LSB offset at the same time.

Full Scale Error (or Gain Error): Full Scale Error is a measure of the difference between the output of an ideal A/D converter and the actual A/D for an input voltage equal to full scale. As shown in *Figure 13*, the Full Scale Error effect is to rotate the transfer characteristic angularly about the origin. Any voltage more positive than the Full Scale transition gives an output code of 111. In practice, therefore, the voltage at which the transition from 111 to 110 occurs is ascertained. The input voltage's departure from the ideal value is defined as Full Scale Error and is expressed as a percentage of FS. In the example of *Figure 13*, Full Scale Error is 1 1/2 LSB's, or 0.214% of FS.

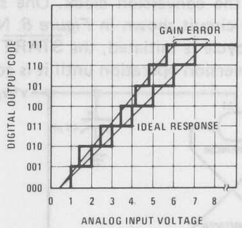


FIGURE 13. Full Scale (Gain Error)

Full Scale Error of the ADC1210, ADC1211 is due primarily to mismatch in the R-2R ladder equivalent output impedance and input resistors R25, R26, R27, and R28. The gain error may be adjusted to zero as outlined in section 2.5.

Monotonicity and Missing Codes: Monotonicity is a property of a D/A which requires an increasing or constant output voltage for an increasing digital input code. Monotonicity of a D/A converter does not, in itself, guarantee that an A/D built with that D/A will not have missing codes. However, the ADC1210 and ADC1211 are guaranteed to have no missing codes.

Conversion Time: The ADC1210, ADC1211 are successive approximation A/D converters requiring 13 clock intervals for a conversion to specified accuracy for the ADC1210 and 11 clocks for the ADC1211. There is a trade-off between accuracy and clock frequency due to settling time of the ladder and propagation delay through the comparator. By modifying the hysteresis network around the comparator, conversions with 10-bit accuracy can be made in 30 μs. Replace R_A, R_B and C_A in *Figure 5* with a 10 MΩ resistor between pin 23 (Comparator Output) and pin 17 (+ IN), and increase the clock rate to 366 kHz.

In order to prevent errors during conversion, the analog input voltage should not be allowed to change by more than ±1/2 LSB. This places a maximum slew rate of 12.5 μV/μs on the analog input voltage. The usual solution to this restriction is to place a Sample and Hold in front of the A/D. For additional application information, refer to application note AN245.

National Semiconductor

A to D, D to A

DAC0800, DAC0801, DAC0802 8-Bit Digital-to-Analog Converters

General Description

The DAC0800 series are monolithic 8-bit high-speed current-output digital-to-analog converters (DAC) featuring typical settling times of 100 ns. When used as a multiplying DAC, monotonic performance over a 40 to 1 reference current range is possible. The DAC0800 series also features high compliance complementary current outputs to allow differential output voltages of 20 Vp-p with simple resistor loads as shown in *Figure 1*. The reference-to-full-scale current matching of better than ±1 LSB eliminates the need for full-scale trims in most applications while the nonlinearities of better than ±0.1% over temperature minimizes system error accumulations.

The noise immune inputs of the DAC0800 series will accept TTL levels with the logic threshold pin, V_{LC}, pin 1 grounded. Simple adjustments of the V_{LC} potential allow direct interface to all logic families. The performance and characteristics of the device are essentially unchanged over the full ± 4.5V to ±18V power supply range; power dissipation is only 33 mW with ±5V supplies and is independent of the logic input states.

The DAC0800, DAC0802, DAC0800C, DAC0801C and DAC0802C are a direct replacement for the DAC-08, DAC-08A, DAC-08C, DAC-08E and DAC-08H, respectively.

Features

- Fast settling output current — 100 ns
- Full scale error — ±1 LSB
- Nonlinearity over temperature — ±0.1%
- Full scale current drift — ±10 ppm/°C
- High output compliance — −10V to +18V
- Complementary current outputs
- Interface directly with TTL, CMOS, PMOS and others
- 2 quadrant wide range multiplying capability
- Wide power supply range — ±4.5V to ±18V
- Low power consumption — 33 mW at ±5V
- Low cost

Typical Applications

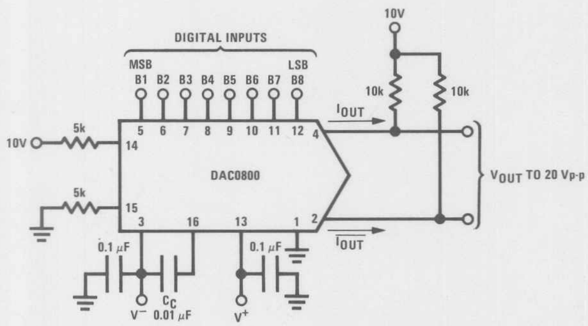
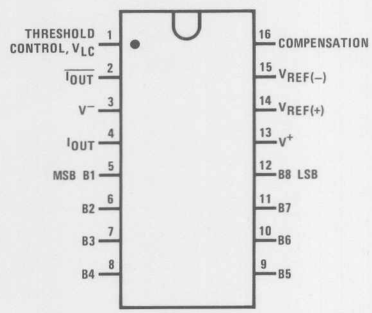


FIGURE 1. ±20 Vp-p Output Digital-to-Analog Converter

Connection Diagram

Dual-In-Line Package



TOP VIEW

Ordering Information

NON LINEARITY	TEMPERATURE RANGE	ORDER NUMBERS* D PACKAGE (D16C)		J PACKAGE (J16A)		N PACKAGE (N16A)	
±0.1% FS	$-55°C \leq T_A \leq +125°C$	DAC0802LD	DAC-08AQ				
±0.1% FS	$0°C \leq T_A \leq +70°C$			DAC0802LCJ	DAC-08HQ	DAC0802LCN	DAC-08HP
±0.19% FS	$-55°C \leq T_A \leq +125°C$	DAC0800LD	DAC-08Q				
±0.19% FS	$0°C \leq T_A \leq +70°C$			DAC0800LCJ	DAC-08EQ	DAC0800LCN	DAC-08EP
±0.39% FS	$0°C \leq T_A \leq +70°C$			DAC0801LCJ	DAC-08CQ	DAC0801LCN	DAC-08CP

*Note. Devices may be ordered by using either order number.

Absolute Maximum Ratings

Supply Voltage	±18V or 36V
Power Dissipation (Note 1)	500 mW
Reference Input Differential Voltage (V14 to V15)	V^- to V^+
Reference Input Common-Mode Range (V14, V15)	V^- to V^+
Reference Input Current	5 mA
Logic Inputs	V^- to V^- plus 36V
Analog Current Outputs	*Figure 24*
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

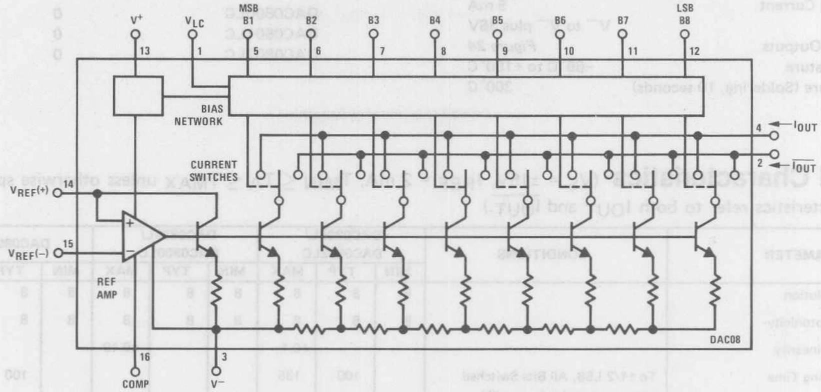
	MIN	MAX	UNITS
Temperature (T_A)			
DAC0802L	−55	+125	°C
DAC0800L	−55	+125	°C
DAC0800LC	0	+70	°C
DAC0801LC	0	+70	°C
DAC0802LC	0	+70	°C

Electrical Characteristics (V_S = ±15V, I_{REF} = 2 mA, $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.)

	PARAMETER	CONDITIONS	DAC0802L/ DAC0802LC			DAC0800L/ DAC0800LC			DAC0801LC			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
	Resolution		8	8	8	8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	8	8	8	Bits
	Nonlinearity				±0.1			±0.19			±0.39	%FS
t_s	Settling Time	To ±1/2 LSB, All Bits Switched "ON" or "OFF", T_A = 25°C		100	135					100	150	ns
		DAC0800L					100	135				ns
		DAC0800LC					100	150				ns
t_{PLH}, t_{PHL}	Propagation Delay	T_A = 25°C										
	Each Bit			35	60		35	60		35	60	ns
	All Bits Switched			35	60		35	60		35	60	ns
TCI_{FS}	Full Scale Tempco			±10	±50		±10	±50		±10	±80	ppm/°C
V_{OC}	Output Voltage Compliance	Full Scale Current Change < 1/2 LSB, R_{OUT} > 20 MΩ Typ	−10		18	−10		18	−10		18	V
I_{FS4}	Full Scale Current	V_{REF} = 10.000V, R14 = 5.000 kΩ R15 = 5.000 kΩ, T_A = 25°C	1.984	1.992	2.000	1.94	1.99	2.04	1.94	1.99	2.04	mA
I_{FSS}	Full Scale Symmetry	$I_{FS4} - I_{FS2}$		±0.5	±4.0		±1	±8.0		±2	±16	μA
I_{ZS}	Zero Scale Current			0.1	1.0		0.2	2.0		0.2	4.0	μA
I_{FSR}	Output Current Range	V^- = −5V	0	2.0	2.1	0	2.0	2.1	0	2.0	2.1	mA
		V^- = −8V to −18V	0	2.0	4.2	0	2.0	4.2	0	2.0	4.2	mA
	Logic Input Levels											
V_{IL}	Logic "0"	V_{LC} = 0V			0.8			0.8			0.8	V
V_{IH}	Logic "1"		2.0			2.0			2.0			V
	Logic Input Current	V_{LC} = 0V										
I_{IL}	Logic "0"	$-10V \le V_{IN} \le +0.8V$		−2.0	−10		−2.0	−10		−2.0	−10	μA
I_{IH}	Logic "1"	$2V \le V_{IN} \le +18V$		0.002	10		0.002	10		0.002	10	μA
V_{IS}	Logic Input Swing	V^- = −15V	−10		18	−10		18	−10		18	V
V_{THR}	Logic Threshold Range	V_S = ±15V	−10		13.5	−10		13.5	−10		13.5	V
I_{15}	Reference Bias Current			−1.0	−3.0		−1.0	−3.0		−1.0	−3.0	μA
dI/dt	Reference Input Slew Rate	*(Figure 24)*	4.0	8.0		4.0	8.0		4.0	8.0		mA/μs
$PSSI_{FS+}$	Power Supply Sensitivity	$4.5V \le V^+ \le 18V$		0.0001	0.01		0.0001	0.01		0.0001	0.01	%/%
$PSSI_{FS-}$		$-4.5V \le V^- \le 18V$		0.0001	0.01		0.0001	0.01		0.0001	0.01	%/%
		I_{REF} = 1 mA										
	Power Supply Current	V_S = ±5V, I_{REF} = 1 mA										
I+				2.3	3.8		2.3	3.8		2.3	3.8	mA
I−				−4.3	−5.8		−4.3	−5.8		−4.3	−5.8	mA
		V_S = 5V, −15V, I_{REF} = 2 mA										
I+				2.4	3.8		2.4	3.8		2.4	3.8	mA
I−				−6.4	−7.8		−6.4	−7.8		−6.4	−7.8	mA
		V_S = ±15V, I_{REF} = 2 mA										
I+				2.5	3.8		2.5	3.8		2.5	3.8	mA
I−				−6.5	−7.8		−6.5	−7.8		−6.5	−7.8	mA
P_D	Power Dissipation	±5V, I_{REF} = 1 mA		33	48		33	48		33	48	mW
		5V, −15V, I_{REF} = 2 mA		108	136		108	136		108	136	mW
		±15V, I_{REF} = 2 mA		135	174		135	174		135	174	mW

Note 1: The maximum junction temperature of the DAC0800, DAC0801 and DAC0802 is 125°C. For operating at elevated temperatures, devices in the dual-in-line J or D package must be derated based on a thermal resistance of 100°C/W, junction to ambient, 175°C/W for the molded dual-in-line N package.

Block Diagram



Equivalent Circuit

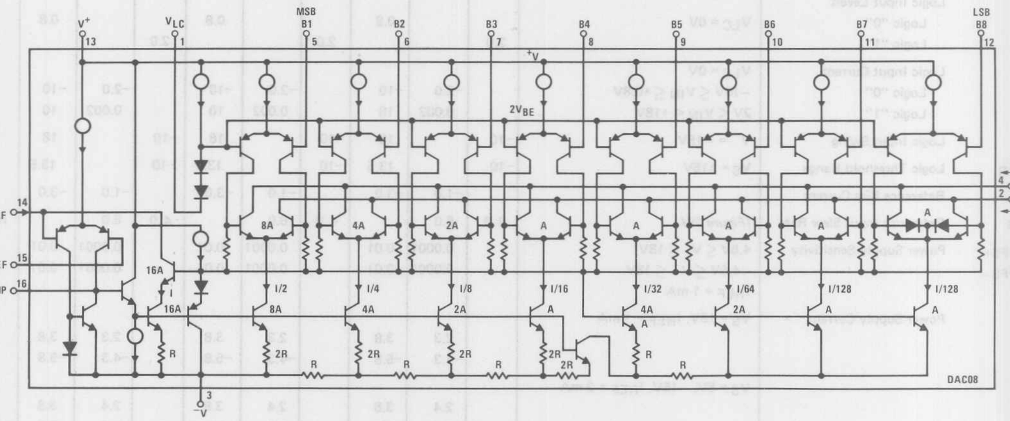


FIGURE 2

Typical Performance Characteristics

Full Scale Current vs Reference Current

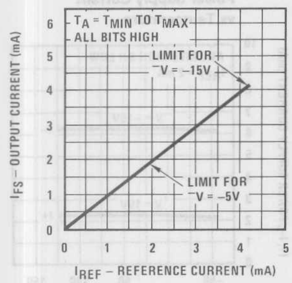


FIGURE 3

LSB Propagation Delay vs I_{FS}

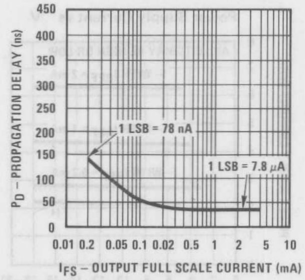
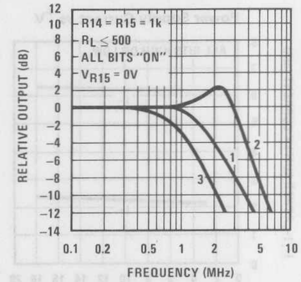


FIGURE 4

Reference Input Frequency Response



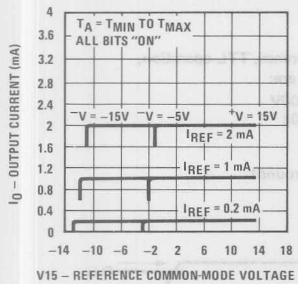
Curve 1: C_C = 15 pF, V_{IN} = 2 Vp-p centered at 1V.

Curve 2: C_C = 15 pF, V_{IN} = 50 mVp-p centered at 200 mV.

Curve 3: C_C = 0 pF, V_{IN} = 100 mVp-p at 0V and applied through 50 Ω connected to pin 14. 2V applied to R14.

FIGURE 5

Reference Amp Common-Mode Range



Note. Positive common-mode range is always (V+) − 1.5V.

FIGURE 6

Logic Input Current vs Input Voltage

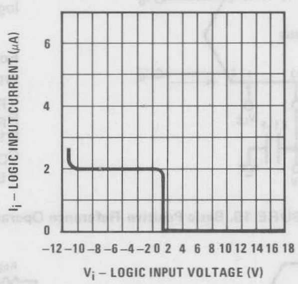


FIGURE 7

$V_{TH} - V_{LC}$ vs Temperature

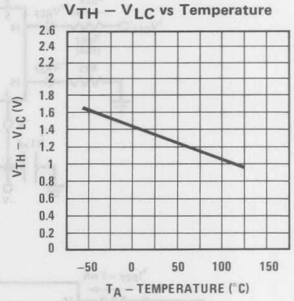


FIGURE 8

Output Current vs Output Voltage (Output Voltage Compliance)

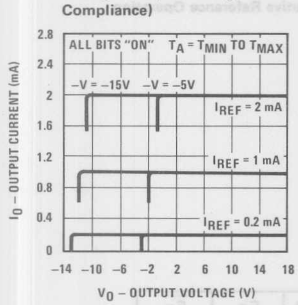


FIGURE 9

Output Voltage Compliance vs Temperature

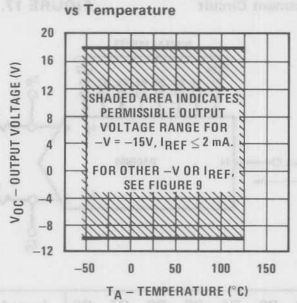
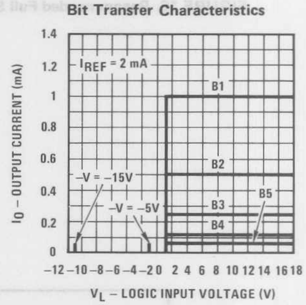


FIGURE 10

Bit Transfer Characteristics



Note. B1–B8 have identical transfer characteristics. Bits are fully switched with less than 1/2 LSB error, at less than ±100 mV from actual threshold. These switching points are guaranteed to lie between 0.8 and 2V over the operating temperature range (V_{LC} = 0V).

FIGURE 11

Typical Performance Characteristics (Continued)

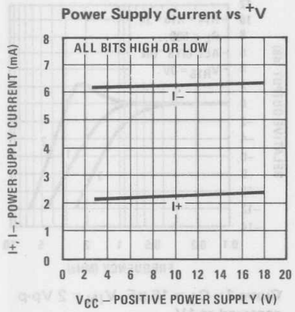


FIGURE 12

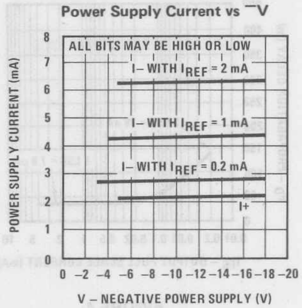


FIGURE 13

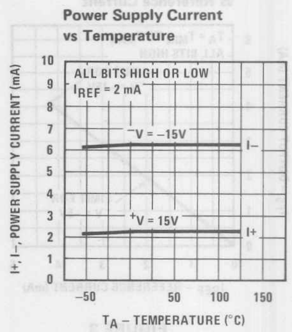
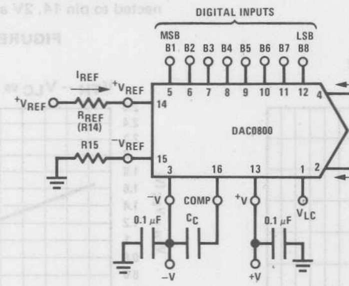


FIGURE 14

Typical Applications (Continued)



$$I_{FS} \approx \frac{+V_{REF}}{R_{REF}} \times \frac{255}{256}$$

$I_O + \overline{I_O} = I_{FS}$ for all logic states

For fixed reference, TTL operation, typical values are:

$V_{REF} = 10.000V$
$R_{REF} = 5.000k$
$R15 \approx R_{REF}$
$C_C = 0.01\ \mu F$
$V_{LC} = 0V$ (Ground)

FIGURE 15. Basic Positive Reference Operation

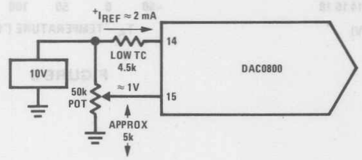
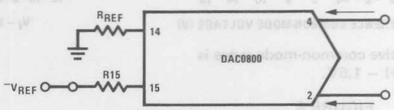


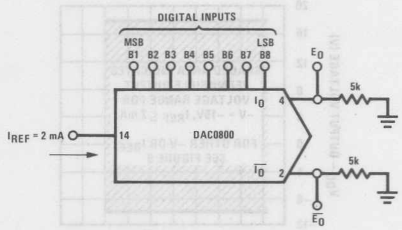
FIGURE 16. Recommended Full Scale Adjustment Circuit



$$I_{FS} \approx \frac{-V_{REF}}{R_{REF}} \times \frac{255}{256}$$

Note. R_{REF} sets I_{FS}; R15 is for bias current cancellation

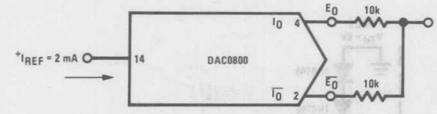
FIGURE 17. Basic Negative Reference Operation



	B1	B2	B3	B4	B5	B6	B7	B8	I_O mA	$\overline{I_O}$ mA	E_O	$\overline{E_O}$
Full Scale	1	1	1	1	1	1	1	1	1.992	0.000	−9.960	0.000
Full Scale−LSB	1	1	1	1	1	1	1	0	1.984	0.008	−9.920	−0.040
Half Scale+LSB	1	0	0	0	0	0	0	1	1.008	0.984	−5.040	−4.920
Half Scale	1	0	0	0	0	0	0	0	1.000	0.992	−5.000	−4.960
Half Scale−LSB	0	1	1	1	1	1	1	1	0.992	1.000	−4.960	−5.000
Zero Scale+LSB	0	0	0	0	0	0	0	1	0.008	1.984	−0.040	−9.920
Zero Scale	0	0	0	0	0	0	0	0	0.000	1.992	0.000	−9.960

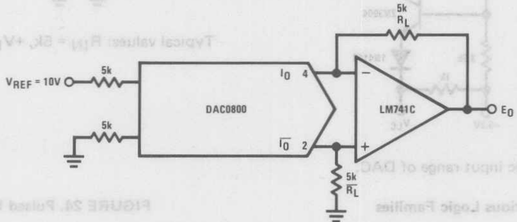
FIGURE 18. Basic Unipolar Negative Operation

Typical Applications (Continued)



	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$\overline{E_O}$
Pos. Full Scale	1	1	1	1	1	1	1	1	−9.920	+10.000
Pos. Full Scale−LSB	1	1	1	1	1	1	1	0	−9.840	+9.920
Zero Scale+LSB	1	0	0	0	0	0	0	1	−0.080	+0.160
Zero Scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero Scale−LSB	0	1	1	1	1	1	1	1	+0.080	0.000
Neg. Full Scale+LSB	0	0	0	0	0	0	0	1	+9.920	−9.840
Neg. Full Scale	0	0	0	0	0	0	0	0	+10.000	−9.920

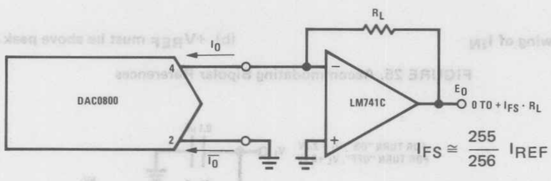
FIGURE 19. Basic Bipolar Output Operation



If $R_L = \overline{R_L}$ within ±0.05%, output is symmetrical about ground

	B1	B2	B3	B4	B5	B6	B7	B8	E_O
Pos. Full Scale	1	1	1	1	1	1	1	1	+9.920
Pos. Full Scale−LSB	1	1	1	1	1	1	1	0	+9.840
(+) Zero Scale	1	0	0	0	0	0	0	0	+0.040
(−) Zero Scale	0	1	1	1	1	1	1	1	−0.040
Neg. Full Scale+LSB	0	0	0	0	0	0	0	1	−9.840
Neg. Full Scale	0	0	0	0	0	0	0	0	−9.920

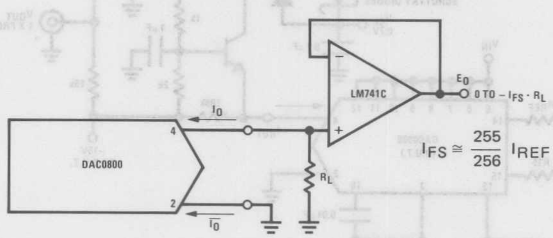
FIGURE 20. Symmetrical Offset Binary Operation



$$I_{FS} \cong \frac{255}{256} I_{REF}$$

For complementary output (operation as negative logic DAC), connect inverting input of op amp to $\overline{I_O}$ (pin 2), connect I_O (pin 4) to ground.

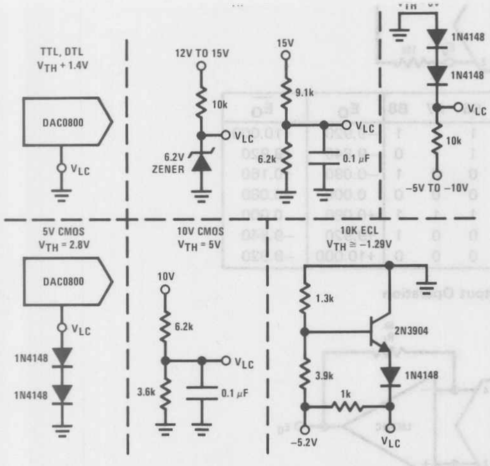
FIGURE 21. Positive Low Impedance Output Operation



$$I_{FS} \cong \frac{255}{256} I_{REF}$$

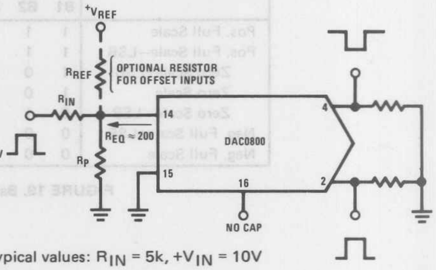
For complementary output (operation as a negative logic DAC) connect non-inverting input of op amp to $\overline{I_O}$ (pin 2); connect I_O (pin 4) to ground.

FIGURE 22. Negative Low Impedance Output Operation



Note. Do not exceed negative logic input range of DAC.

FIGURE 23. Interfacing with Various Logic Families



Typical values: R_{IN} = 5k, $+V_{IN}$ = 10V

FIGURE 24. Pulsed Reference Operation

(a) $I_{REF} \geq$ peak negative swing of I_{IN}

(b) $+V_{REF}$ must be above peak positive swing of V_{IN}

FIGURE 25. Accommodating Bipolar References

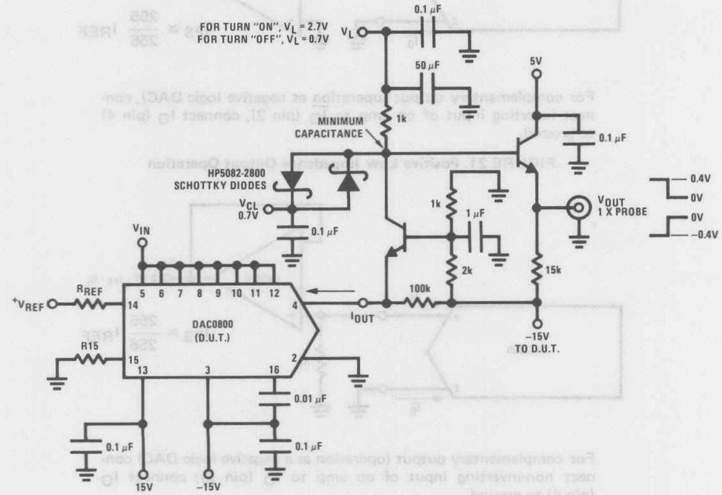
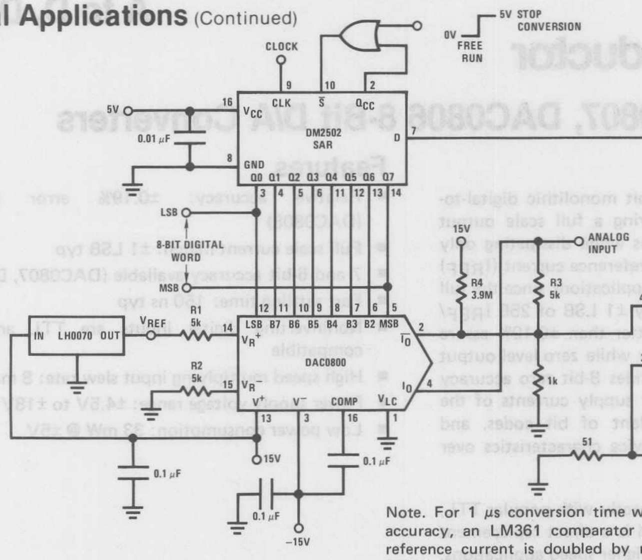


FIGURE 26. Settling Time Measurement

Typical Applications (Continued)



Note. For 1 μs conversion time with 8-bit resolution and 7-bit accuracy, an LM361 comparator replaces the LM319 and the reference current is doubled by reducing R1, R2 and R3 to 2.5 kΩ and R4 to 2 MΩ.

FIGURE 27. A Complete 2 μs Conversion Time, 8-Bit A/D Converter

National Semiconductor

DAC0808, DAC0807, DAC0806 8-Bit D/A Converters

General Description

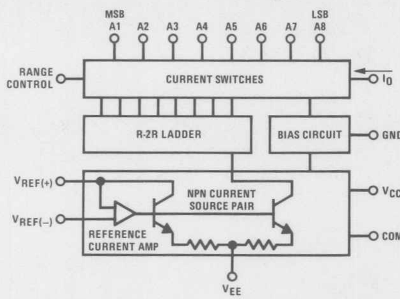
The DAC0808 series is an 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current settling time of 150 ns while dissipating only 33 mW with ±5V supplies. No reference current (I_{REF}) trimming is required for most applications since the full scale output current is typically ±1 LSB of 255 I_{REF}/256. Relative accuracies of better than ±0.19% assure 8-bit monotonicity and linearity while zero level output current of less than 4 μA provides 8-bit zero accuracy for $I_{REF} \geq 2$ mA. The power supply currents of the DAC0808 series are independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range.

The DAC0808 will interface directly with popular TTL, DTL or CMOS logic levels, and is a direct replacement for the MC1508/MC1408. For higher speed applications, see DAC0800 data sheet.

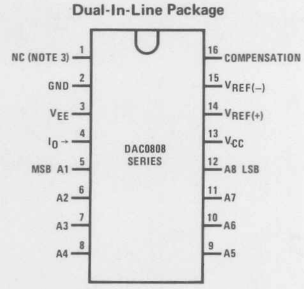
Features

- Relative accuracy: ±0.19% error maximum (DAC0808)
- Full scale current match: ±1 LSB typ
- 7 and 6-bit accuracy available (DAC0807, DAC0806)
- Fast settling time: 150 ns typ
- Noninverting digital inputs are TTL and CMOS compatible
- High speed multiplying input slew rate: 8 mA/μs
- Power supply voltage range: ±4.5V to ±18V
- Low power consumption: 33 mW @ ±5V

Block and Connection Diagrams

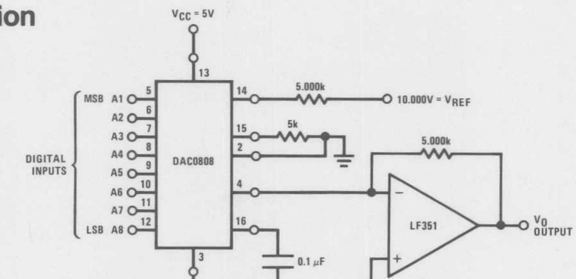


Dual-In-Line Package



TOP VIEW

Typical Application



$$V_O = 10V \left(\frac{A1}{2} + \frac{A2}{4} + \ldots \frac{A8}{256}\right)$$

FIGURE 1. +10V Output Digital to Analog Converter

Ordering Information

ACCURACY	OPERATING TEMPERATURE RANGE	ORDER NUMBERS*					
		D PACKAGE (D16C)		J PACKAGE (J16A)		N PACKAGE (N16A)	
8-bit	$-55°C \leq T_A \leq +125°C$	DAC0808LD	MC1508L8				
8-bit	$0°C \leq T_A \leq +75°C$			DAC0808LCJ	MC1408L8	DAC0808LCN	MC1408P8
7-bit	$0°C \leq T_A \leq +75°C$			DAC0807LCJ	MC1408L7	DAC0807LCN	MC1408P7
6-bit	$0°C \leq T_A \leq +75°C$			DAC0806LCJ	MC1408L6	DAC0806LCN	MC1408P6

*Note. Devices may be ordered by using either order number.

Applied Output Voltage, V_O			
Reference Current, I_{14}	5 mA	Storage Temperature Range	−65°C to +150°C
Reference Amplifier Inputs, V14, V15	V_{CC}, V_{EE}		

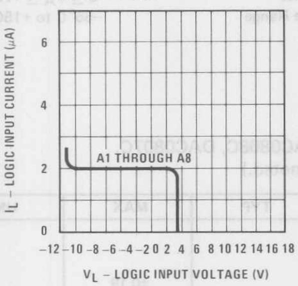
Electrical Characteristics

(V_{CC} = 5V, V_{EE} = −15 V_{DC}, V_{REF}/R14 = 2 mA, DAC0808: T_A = −55°C to +125°C, DAC0808C, DAC0807C, DAC0806C, T_A = 0°C to +75°C, and all digital inputs at high logic level unless otherwise noted.)

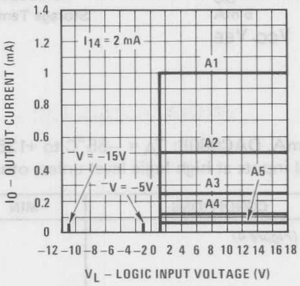
	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
E_r	Relative Accuracy (Error Relative to Full Scale I_O)	*(Figure 4)*				%
	DAC0808L (LM1508-8), DAC0808LC (LM1408-8)				±0.19	%
	DAC0807LC (LM1408-7), (Note 1)				±0.39	%
	DAC0806LC (LM1408-6), (Note 1)				±0.78	%
	Settling Time to Within 1/2 LSB (Includes t_{PLH})	T_A = 25°C (Note 2), *(Figure 5)*		150		ns
t_{PLH}, t_{PHL}	Propagation Delay Time	T_A = 25°C, *(Figure 5)*		30	100	ns
TCI_O	Output Full Scale Current Drift			±20		ppm/°C
MSB	Digital Input Logic Levels	*(Figure 3)*				
V_{IH}	High Level, Logic "1"		2			V_{DC}
V_{IL}	Low Level, Logic "0"				0.8	V_{DC}
MSB	Digital Input Current	*(Figure 3)*				
	High Level	V_{IH} = 5V		0	0.040	mA
	Low Level	V_{IL} = 0.8V		−0.003	−0.8	mA
I_{15}	Reference Input Bias Current	*(Figure 3)*		−1	−3	μA
	Output Current Range	*(Figure 3)*				
		V_{EE} = −5V	0	2.0	2.1	mA
		V_{EE} = −15V, T_A = 25°C	0	2.0	4.2	mA
I_O	Output Current	V_{REF} = 2.000V, R14 = 1000Ω, *(Figure 3)*	1.9	1.99	2.1	mA
	Output Current, All Bits Low	*(Figure 3)*		0	4	μA
	Output Voltage Compliance	$E_r \leq$ 0.19%, T_A = 25°C				
	Pin 1 Grounded,				−0.55, +0.4	V_{DC}
	V_{EE} Below −10V				−5.0, +0.4	V_{DC}
SRI_{REF}	Reference Current Slew Rate	*(Figure 6)*	4	8		mA/μs
	Output Current Power Supply Sensitivity	$-5V \leq V_{EE} \leq -16.5V$		0.05	2.7	μA/V
	Power Supply Current (All Bits Low)	*(Figure 3)*				
I_{CC}				2.3	22	mA
I_{EE}				−4.3	−13	mA
	Power Supply Voltage Range	T_A = 25°C, *(Figure 3)*				
V_{CC}			4.5	5.0	5.5	V_{DC}
V_{EE}			−4.5	−15	−16.5	V_{DC}
	Power Dissipation					
	All Bits Low	V_{CC} = 5V, V_{EE} = −5V		33	170	mW
		V_{CC} = 5V, V_{EE} = −15V		106	305	mW
	All Bits High	V_{CC} = 15V, V_{EE} = −5V		90		mW
		V_{CC} = 15V, V_{EE} = −15V		160		mW

Note 1: All current switches are tested to guarantee at least 50% of rated current.
Note 2: All bits switched.
Note 3: Range control is not required.

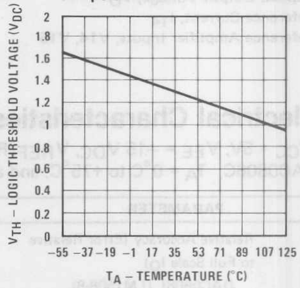
Input Voltage



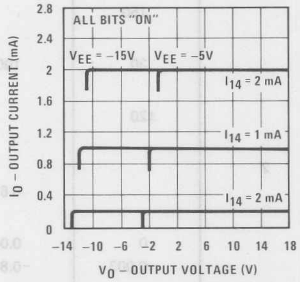
Bit Transfer Characteristics



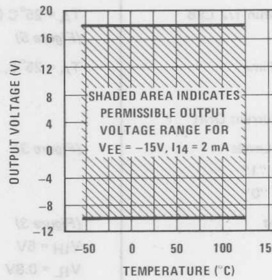
Temperature



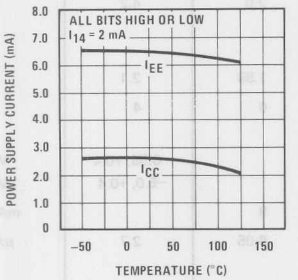
Output Current vs Output Voltage (Output Voltage Compliance)



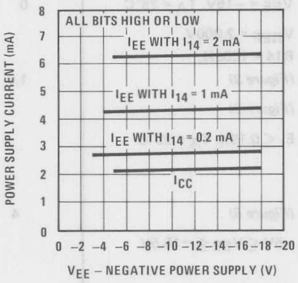
Output Voltage Compliance vs Temperature



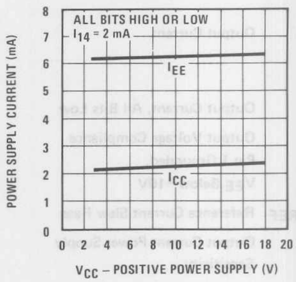
Typical Power Supply Current vs Temperature



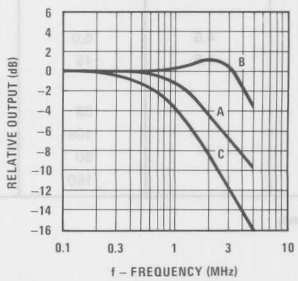
Typical Power Supply Current vs V_{EE}



Typical Power Supply Current vs V_{CC}



Reference Input Frequency Response



Unless otherwise specified: R14 = R15 = 1 kΩ, C = 15 pF, pin 16 to V_{EE}; R_L = 50Ω, pin 4 to ground.

Curve A: Large Signal Bandwidth Method of *Figure 7*, V_{REF} = 2 Vp-p offset 1 V above ground

Curve B: Small Signal Bandwidth Method of *Figure 7*, R_L = 250Ω, V_{REF} = 50 mVp-p offset 200 mV above ground.

Curve C: Large and Small Signal Bandwidth Method of *Figure 9* (no op amp, R_L = 50Ω), R_S = 50Ω, V_{REF} = 2V, V_S = 100 mVp-p centered at 0V.

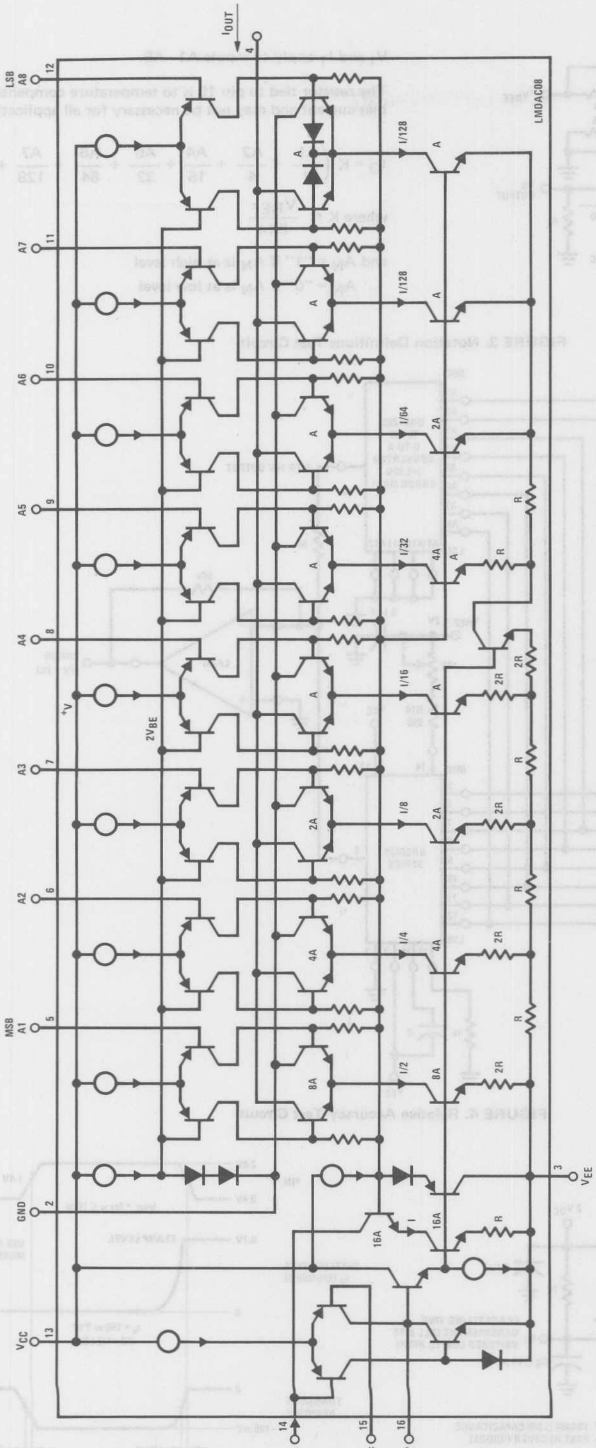
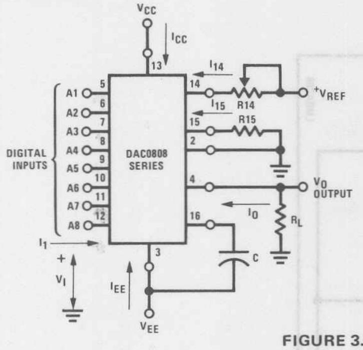


FIGURE 2. Equivalent Circuit of the DAC0808 Series

Test Circuits



V_I and I_1 apply to inputs A1–A8.

The resistor tied to pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_O = K\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right)$$

where $K \cong \dfrac{V_{REF}}{R14}$

and A_N = "1" if A_N is at high level

A_N = "0" if A_N is at low level

FIGURE 3. Notation Definitions Test Circuit

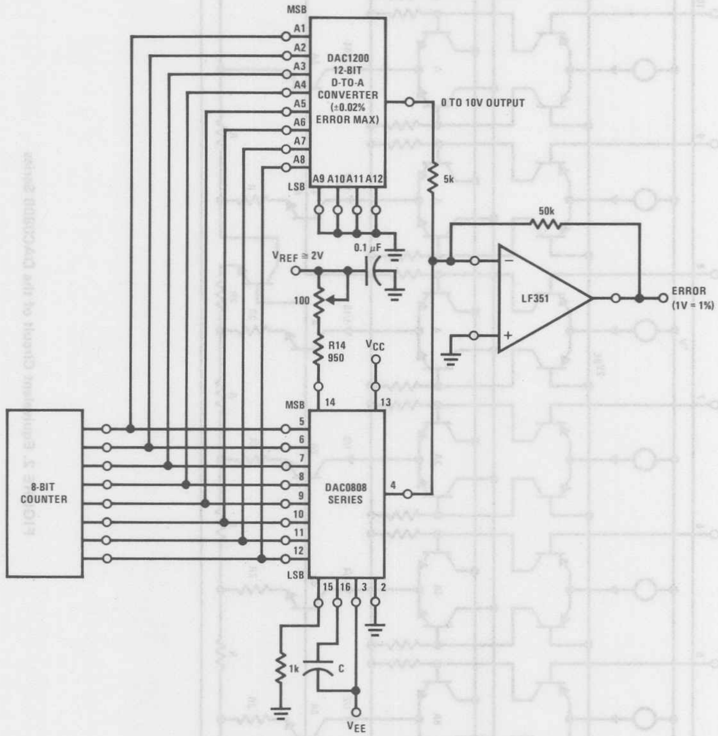


FIGURE 4. Relative Accuracy Test Circuit

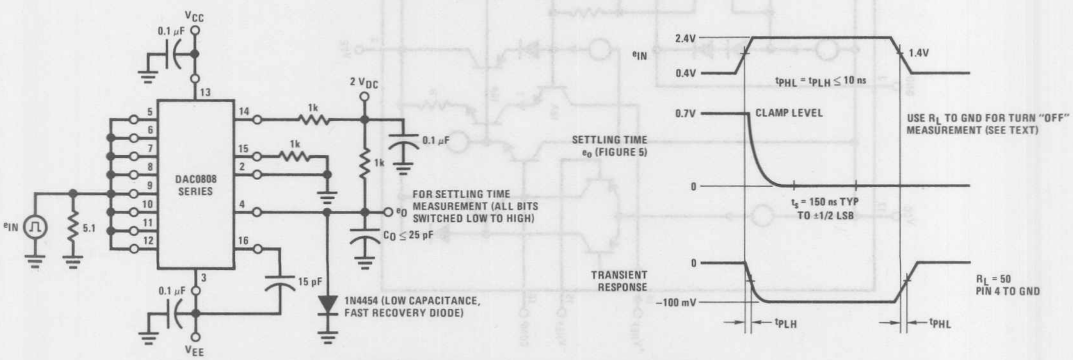


FIGURE 5. Transient Response and Settling Time

Test Circuits (Continued)

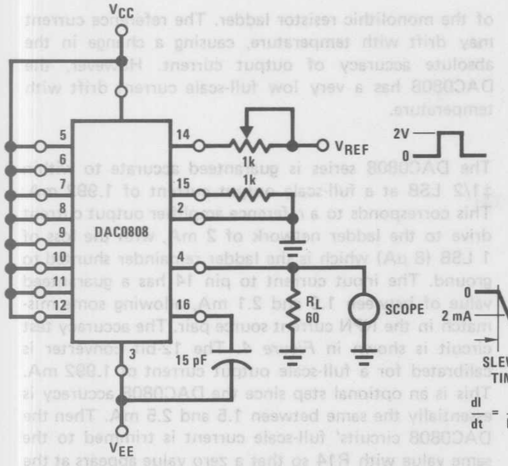


FIGURE 6. Reference Current Slew Rate Measurement

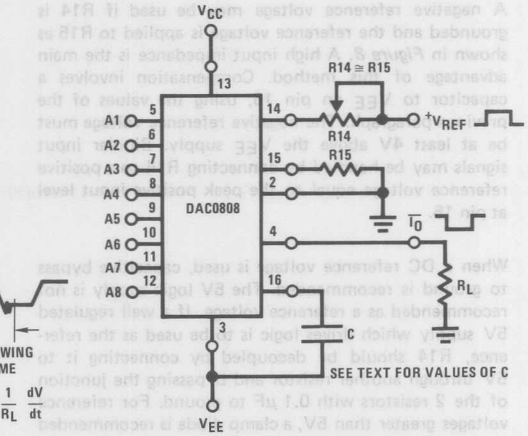


FIGURE 7. Positive V_{REF}

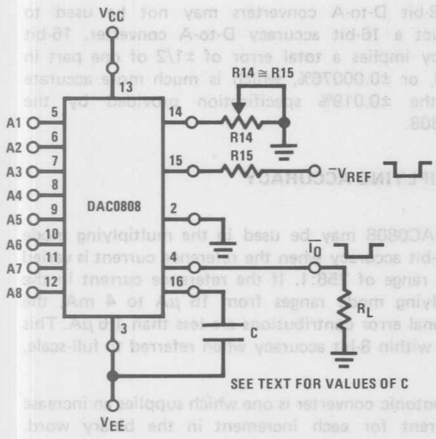


FIGURE 8. Negative V_{REF}

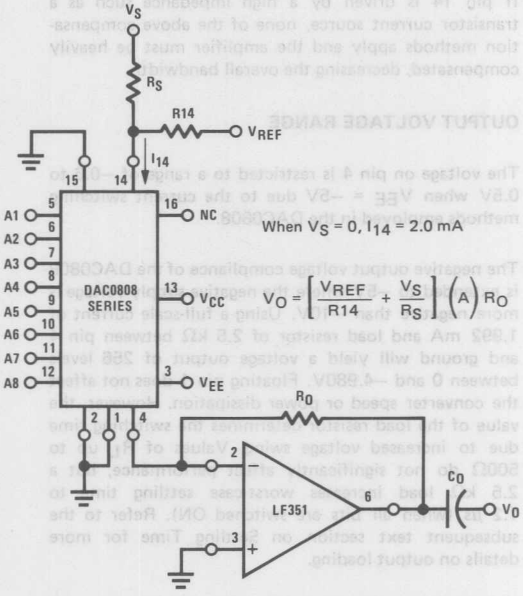


FIGURE 9. Programmable Gain Amplifier or Digital Attenuator Circuit

Application Hints

REFERENCE AMPLIFIER DRIVE AND COMPENSATION

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current, I_{14}, must always flow into pin 14, regardless of the set-up method or reference voltage polarity.

Connections for a positive voltage are shown in *Figure 7*. The reference voltage source supplies the full current I_{14}. For bipolar reference signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R15 with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increases in R14 to maintain proper phase margin; for R14 values of 1, 2.5 and 5 kΩ, minimum capacitor values are 15, 37 and 75 pF. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection.

shown in *Figure 8*. A high input impedance is the main advantage of this method. Compensation involves a capacitor to V_{EE} on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 4V above the V_{EE} supply. Bipolar input signals may be handled by connecting R14 to a positive reference voltage equal to the peak positive input level at pin 15.

When a DC reference voltage is used, capacitive bypass to ground is recommended. The 5V logic supply is not recommended as a reference voltage. If a well regulated 5V supply which drives logic is to be used as the reference, R14 should be decoupled by connecting it to 5V through another resistor and bypassing the junction of the 2 resistors with 0.1 μF to ground. For reference voltages greater than 5V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

OUTPUT VOLTAGE RANGE

The voltage on pin 4 is restricted to a range of −0.6 to 0.5V when V_{EE} = −5V due to the current switching methods employed in the DAC0808.

The negative output voltage compliance of the DAC0808 is extended to −5V where the negative supply voltage is more negative than −10V. Using a full-scale current of 1.992 mA and load resistor of 2.5 kΩ between pin 4 and ground will yield a voltage output of 256 levels between 0 and −4.980V. Floating pin 1 does not affect the converter speed or power dissipation. However, the value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500Ω do not significantly affect performance, but a 2.5 kΩ load increases worst-case settling time to 1.2 μs (when all bits are switched ON). Refer to the subsequent text section on Settling Time for more details on output loading.

OUTPUT CURRENT RANGE

The output current maximum rating of 4.2 mA may be used only for negative supply voltages more negative than −7V, due to the increased voltage drop across the resistors in the reference current amplifier.

ACCURACY

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full-scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full-scale current. The relative accuracy of the DAC0808 is essentially constant with temperature due to the excellent temperature tracking may drift with temperature, causing a change in the absolute accuracy of output current. However, the DAC0808 has a very low full-scale current drift with temperature.

The DAC0808 series is guaranteed accurate to within ±1/2 LSB at a full-scale output current of 1.992 mA. This corresponds to a reference amplifier output current drive to the ladder network of 2 mA, with the loss of 1 LSB (8 μA) which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2.1 mA, allowing some mismatch in the NPN current source pair. The accuracy test circuit is shown in *Figure 4*. The 12-bit converter is calibrated for a full-scale output current of 1.992 mA. This is an optional step since the DAC0808 accuracy is essentially the same between 1.5 and 2.5 mA. Then the DAC0808 circuits' full-scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accuracy D-to-A converter. 16-bit accuracy implies a total error of ±1/2 of one part in 65,536, or ±0.00076%, which is much more accurate than the ±0.019% specification provided by the DAC0808.

MULTIPLYING ACCURACY

The DAC0808 may be used in the multiplying mode with 8-bit accuracy when the reference current is varied over a range of 256:1. If the reference current in the multiplying mode ranges from 16 μA to 4 mA, the additional error contributions are less than 1.6 μA. This is well within 8-bit accuracy when referred to full-scale.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the DAC0808 is monotonic for all values of reference current above 0.5 mA. The recommended range for operation with a DC reference current is 0.5 to 4 mA.

SETTLING TIME

The worst-case switching condition occurs when all bits are switched ON, which corresponds to a low-to-high transition for all bits. This time is typically 150 ns for settling to within ±1/2 LSB, for 8-bit accuracy, and 100 ns to 1/2 LSB for 7 and 6-bit accuracy. The turn OFF is typically under 100 ns. These times apply when $R_L \leq 500\Omega$ and $C_O \leq 25$ pF.

Extra care must be taken in board layout since this is usually the dominant factor in satisfactoy test results when measuring settling time. Short leads, 100 μF supply bypassing for low frequencies, and minimum scope lead length are all mandatory.

National Semiconductor

MICRO-DAC™ DAC0830/0831/0832 8-Bit μP Compatible, Double-Buffered D to A Converters

General Description

The DAC0830 is an advanced CMOS/Si-Cr 8-bit multiplying DAC designed to interface directly with the 8080, 8048, 8085, Z-80, and other popular microprocessors. A deposited silicon-chromium R-2R resistor ladder network divides the reference current and provides the circuit with excellent temperature tracking characteristics (0.05% of Full Scale Range maximum linearity error over temperature). The circuit uses CMOS current switches and control logic to achieve low power consumption and low output leakage current errors. Special circuitry provides TTL logic input voltage level compatibility.

Double buffering allows these DACs to output a voltage corresponding to one digital word while holding the next digital word. This permits the simultaneous updating of any number of DACs.

The DAC0830 series are the 8-bit members of a family of microprocessor-compatible DAC's (MICRO-DAC's™). For applications demanding higher resolution, the DAC1000 series (10-bits) and the DAC1208 and DAC1230 (12-bits) are available alternatives.

Micro-Dac is a trademark of National Semiconductor Corp.

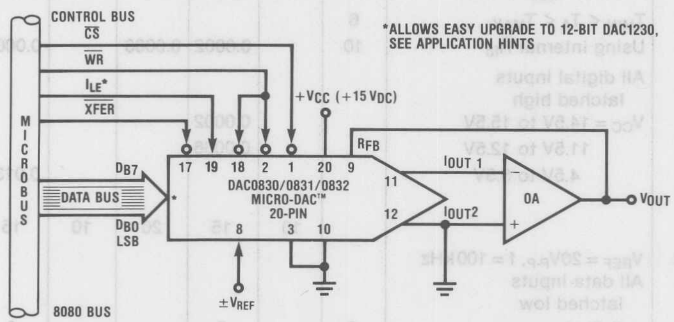
Features

- Double-buffered, single-buffered or flow-through digital data inputs
- Easy interchange and pin-compatible with 12-bit DAC1230 series
- Direct interface to all popular microprocessors
- Linearity specified with zero and full scale adjust only—NOT BEST STRAIGHT LINE FIT.
- Works with ±10V reference-full 4-quadrant multiplication
- Can be used in the voltage switching mode
- Logic inputs which meet TTL voltage level specs (1.4V logic threshold)
- Operates "STAND ALONE" (without μP) if desired

Key Specifications

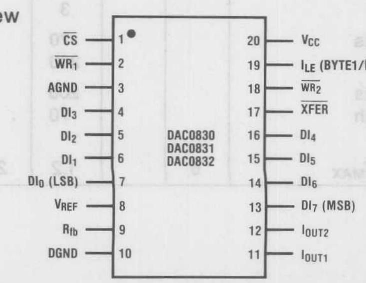
■ Current settling time	1 μs
■ Resolution	8-bits
■ Linearity (guaranteed over temp.)	8, 9, or 10 bits
■ Gain Tempco	0.0002% FS/°C
■ Low power dissipation	20 mW
■ Single power supply	5 to 15 V_{DC}

Typical Application



*ALLOWS EASY UPGRADE TO 12-BIT DAC1230, SEE APPLICATION HINTS

Pin Configuration Top View



†THIS IS NECESSARY FOR THE 12-BIT DAC1230 SERIES TO PERMIT INTERCHANGING FROM AN 8-BIT TO A 12-BIT DAC WITH NO PC BOARD CHANGES AND NO SOFTWARE CHANGES, SEE APPLICATIONS SECTION.

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	17 V_{DC}
Voltage at any digital input	V_{CC} to GND
Voltage at V_{REF} input	±25V
Storage temperature range	−65°C to +150°C
Package dissipation at $T_A = 25°C$ (Note 3)	500 mW
DC voltage applied to I_{OUT1} or I_{OUT2} (Note 4)	−100 mV to V_{CC}
Lead temperature (soldering, 10 seconds)	300°C

Operating Ratings

Temperature Range	
Part numbers with 'LCN' suffix	0°C to 70°C
Part numbers with 'LCD' suffix	−40°C to +85°C
Part numbers with 'LD' Suffix	−55°C to +125°C
Voltage at any digital input	V_{CC} TO GND

General Electrical Characteristics $T_A = 25°C$, $V_{REF} = 10.000\,V_{DC}$ unless otherwise noted

Parameter	Conditions	See Note	$V_{CC} = 12V_{DC} \pm 5\%$ to $15V_{DC} \pm 5\%$ Min.	Typ.	Max.	$V_{CC} = 5V_{DC} \pm 5\%$ Min.	Typ.	Max.	Units
Resolution			8	8	8	8	8	8	bits
Linearity Error	Zero and full scale adjusted	4,7							
	$T_{MIN} < T_A < T_{MAX}$	6							
	$-10V \le V_{REF} \le +10V$	5							
	DAC0830				0.05			0.05	% of FSR
	DAC0831				0.1			0.1	% of FSR
	DAC0832				0.2			0.2	% of FSR
Differential Nonlinearity	Zero and full scale adjusted	4,7							
	$T_{MIN} < T_A < T_{MAX}$	6							
	$-10V \le V_{REF} \le +10V$	5							
	DAC0830				0.1			0.1	% of FSR
	DAC0831				0.2			0.2	% of FSR
	DAC0832				0.4			0.4	% of FSR
Monotonicity	$T_{MIN} < T_A < T_{MAX}$	4,6							
	$-10V \le V_{REF} \le +10V$	5	8	8	8	8	8	8	bits
Gain Error	Using internal R_{fb}								
	$-10V \le V_{REF} \le +10V$	5	−1.0	±0.2	1.0	−1.0	±0.2	1.0	% of FS
Gain Error Tempco	$T_{MIN} < T_A < T_{MAX}$	6							
	Using internal R_{fb}	10		0.0002	0.0006		0.0002	0.0006	% of FS/°C
Power Supply Rejection	All digital inputs latched high								
	$V_{CC} = 14.5V$ to $15.5V$			0.0002					% FSR/V
	11.5V to 12.5V			0.0006					% FSR/V
	4.5V to 5.5V						0.0130		%FSR/V
Reference Input Resistance			10	15	20	10	15	20	kΩ
Output Feedthrough Error	$V_{REF} = 20V_{P\text{-}P}$, f = 100 kHz								
	All data inputs latched low								
	D Package	9		3			3		$mV_{P\text{-}P}$
	N Package			3			3		$mV_{P\text{-}P}$
Output Capacitance I_{OUT1}	All data inputs latched low			70			70		pF
I_{OUT2}				200			200		pF
I_{OUT1}	All data inputs latched high			200			200		pF
I_{OUT2}				70			70		pF
Supply Current Drain	$T_{MIN} \le T_A \le T_{MAX}$	6		1.2	2.0		1.2	2.0	mA

General Electrical Characteristics $T_A = 25°C$, $V_{REF} = 10.000\ V_{DC}$ unless otherwise noted

Parameter	Conditions	See Note	$V_{CC} = 12V_{DC} \pm 5\%$ to $15V_{DC} \pm 5\%$ Min.	Typ.	Max.	$V_{CC} = 5V_{DC} \pm 5\%$ Min.	Typ.	Max.	Units
Output Leakage Current	$T_{MIN} \leq T_A \leq T_{MAX}$	6							
I_{OUT1}	All data inputs latched low	11			100			100	nA
I_{OUT2}	All data inputs latched high				100			100	nA
Digital Input Voltages	$T_{MIN} \leq T_A \leq T_{MAX}$	6							
	Low Level								
	LD suffix				0.8			0.6	V_{DC}
	Parts with LCD or LCN suffix				0.8			0.8	V_{DC}
	High Level-All Parts		2.0			2.0			V_{DC}
Digital Input Currents	$T_{MIN} \leq T_A \leq T_{MAX}$	6							
	Digital inputs < 0.8V			−50	−200		−50	−200	μA_{DC}
	Digital inputs > 2.0V			0.1	+10		0.1	+10	μA_{DC}
Current Settling Time t_S	$V_{IL} = 0V$, $V_{IH} = 5V$			1.0			1.0		μs
Write and XFER Pulse Width t_W	$V_{IL} = 0V$, $V_{IH} = 5V$, $T_A = 25°C$	8	320	60		320	250		ns
	$T_{MIN} \leq T_A \leq T_{MAX}$	10	320	100		500	350		ns
Data Set Up Time t_{DS}	$V_{IL} = 0V$, $V_{IH} = 5V$, $T_A = 25°C$	10	320	60		320	250		ns
	$T_{MIN} \leq T_A \leq T_{MAX}$		320	100		500	350		ns
Data Hold Time t_{DH}	$V_{IL} = 0V$, $V_{IH} = 5V$ $T_A = 25°C$	10	90	50		300	200		ns
	$T_{MIN} \leq T_A \leq T_{MAX}$		90	60		350	260		ns
Control Set Up Time t_{CS}	$V_{IL} = 0V$, $V_{IL} = 5V$, $T_A = 25°C$	10	320	60		320	250		ns
	$T_{MIN} \leq T_A \leq T_{MAX}$		320	100		500	350		ns
Control Hold Time t_{CH}	$V_{IL} = 0V$, $V_{IH} = 5V$, $T_A = 25°C$	10	10			10			ns
	$T_{MIN} \leq T_A \leq T_{MAX}$		10			10			ns

Note 1: *"Absolute Maximum Ratings"* are those values beyond which the safety of the device cannot be guaranteed. These specifications are not meant to imply that the devices should be operated at these *"Absolute Maximum"* limits.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: This 500 mW specification applies for all packages. The low intrinsic power dissipation of this part (and the fact that there is no way to significantly modify the power dissipation) removes concern for heat sinking.

Note 4: For current switching applications, both I_{OUT1} and I_{OUT2} must go to ground or the "Virtual Ground" of an operational amplifier. The linearity error is degraded by approximately $V_{OS} \div V_{REF}$. For example, if $V_{REF} = 10V$ then a 1 mV offset, V_{OS}, on I_{OUT1} or I_{OUT2} will introduce an additional 0.01% linearity error.

Note 5: Guaranteed at $V_{REF} = \pm 10\ V_{DC}$ and $V_{REF} = \pm 1\ V_{DC}$.

Note 6: $T_{MIN} = 0°C$ and $T_{MAX} = 70°C$ for "LCN" suffix parts.
$T_{MIN} = -40°C$ and $T_{MAX} = 85°C$ for "LCD" suffix parts.
$T_{MIN} = -55°C$ and $T_{MAX} = 125°C$ for "LD" suffix parts.

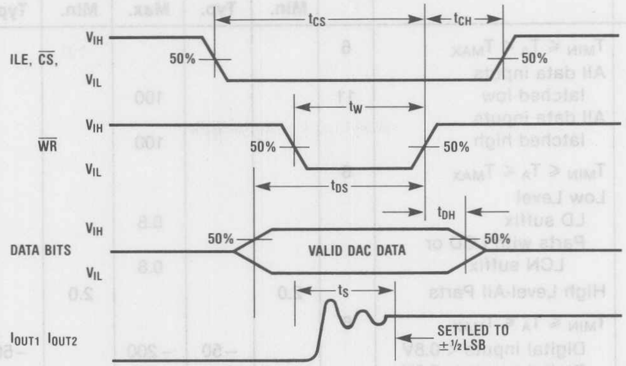
Note 7: The unit "FSR" stands for "Full Scale Range." "Linearity Error" and "Power Supply Rejection" specs are based on this unit to eliminate dependence on a particular V_{REF} value and to indicate the true performance of the part. The "Linearity Error" specification of the DAC0830 is "0.05% of FSR (MAX)." This guarantees that after performing a zero and full scale adjustment (See Sections 2.5 and 2.6), the plot of the 256 analog voltage outputs will each be within $0.05\% \times V_{REF}$ of a straight line which passes through zero and full scale.

Note 8: This specification implies that all parts are guaranteed to operate with a write pulse or transfer pulse width (t_W) of 320 ns. A typical part will operate with t_W of only 100 ns. The entire write pulse must occur within the valid data interval for the specified t_W, t_{DS}, t_{DH}, and t_S to apply.

Note 9: To achieve this low feedthrough in the D package, the user must ground the metal lid. If the lid is left floating, the feedthrough is typically 6 mV.

Note 10: Guaranteed by design but not tested.

Note 11: A 100 nA leakage current with $R_{fb} = 20k$ and $V_{REF} = 10V$ corresponds to a zero error of $(100 \times 10^{-9} \times 20 \times 10^3) \times 100/10$ which is 0.02% of FS.



Definition of Package Pinouts

Control Signals (All control signals level actuated)

$\overline{CS}$: **Chip Select** (active low). The $\overline{CS}$ in combination with ILE will enable $\overline{WR_1}$.

ILE: **Input Latch Enable** (active high). The ILE in combination with $\overline{CS}$ enables $\overline{WR_1}$.

$\overline{WR_1}$: **Write 1**. The active low $\overline{WR_1}$ is used to load the digital input data bits (DI) into the input latch. The data in the input latch is latched when $\overline{WR_1}$ is high. To update the input latch — $\overline{CS}$ and $\overline{WR_1}$ must be low while ILE is high.

$\overline{WR_2}$: **Write 2** (active low). This signal, in combination with $\overline{XFER}$, causes the 8-bit data which is available in the input latch to transfer to the DAC register.

$\overline{XFER}$: **Transfer control signal** (active low). The $\overline{XFER}$ will enable $\overline{WR_2}$.

Other Pin Functions

DI_0–DI_7: **Digital Inputs**. DI_0 is the least significant bit (LSB) and DI_7 is the most significant bit (MSB).

I_{OUT1}: **DAC Current Output 1**. I_{OUT1} is a maximum for a digital code of all 1's in the DAC register, and is zero for all 0's in DAC register.

I_{OUT2}: **DAC Current Output 2**. I_{OUT2} is a constant minus I_{OUT1}, or $I_{OUT1} + I_{OUT2} =$ constant (I full scale for a fixed reference voltage).

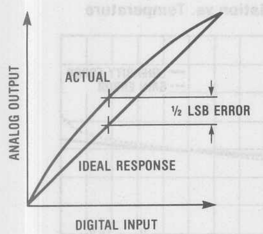
R_{fb}: **Feedback Resistor**. The feedback resistor is provided on the IC chip for use as the shunt feedback resistor for the external op amp which is used to provide an output voltage for the DAC. This on-chip resistor should always be used (not an external resistor) since it matches the resistors which are used in the on-chip R-2R ladder and tracks these resistors over temperature.

V_{REF}: **Reference Voltage Input**. This input connects an external precision voltage source to the internal R-2R ladder. V_{REF} can be selected over the range of +10 to −10V. This is also the analog voltage input for a 4-quadrant multiplying DAC application.

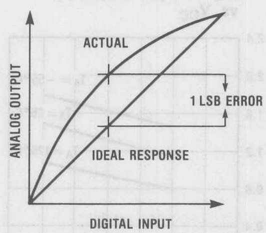
V_{CC}: **Digital Supply Voltage**. This is the power supply pin for the part. V_{CC} can be from +5 to $+15V_{DC}$. Operation is optimum for $+15V_{DC}$.

AGND: **Analog Ground**. This is the ground for the analog circuitry. This pin must always be connected to the digital ground potential.

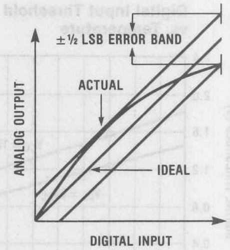
DGND: **Digital Ground**. This is the ground for the digital logic.



a) End point test after zero and fs adj.



b) Best straight line



c) Shifting fs adj. to pass best straight line test

Definition of Terms

Resolution: Resolution is directly related to the number of switches or bits within the DAC. For example, the DAC0830 has 2^8 or 256 steps and therefore has 8-bit resolution.

Linearity Error: Linearity Error is the maximum deviation from a *straight line passing through the endpoints of the DAC transfer characteristic*. It is measured after adjusting for zero and full-scale. Linearity error is a parameter intrinsic to the device and cannot be externally adjusted.

National's linearity "end point test" (a) and the "best straight line" test (b,c) used by other suppliers are illustrated above. The "end point test" greatly simplifies the adjustment procedure by eliminating the need for multiple iterations of checking the linearity and then adjusting full scale until the linearity is met. The "end point test" guarantees that linearity is met after a single full scale adjust. (One adjustment vs. multiple iterations of the adjustment.) The "end point test" uses a standard zero and F.S. adjustment procedure and is a much more stringent test for DAC linearity.

Power Supply Sensitivity: Power supply sensitivity is a measure of the effect of power supply changes on the DAC full-scale output.

Settling Time: Settling time is the time required from a code transition until the DAC output reaches within ±½LSB of the final output value. Full-scale settling time requires a zero to full-scale or full-scale to zero output change.

Full-Scale Error: Full scale error is a measure of the output error between an ideal DAC and the actual device output. Ideally, for the DAC0830 series, full-scale is V_{REF} − 1 LSB. For V_{REF} = 10V and unipolar operation, $V_{FULL\text{-}SCALE}$ = 10.0000V − 39 mV = 9.961V. Full-scale error is adjustable to zero.

Differential Nonlinearity: The difference between any two consecutive codes in the transfer curve from the theoretical 1 LSB is differential nonlinearity.

Monotonic: If the output of a DAC increases for increasing digital input code, then the DAC is monotonic. An 8-bit DAC which is monotonic to 8 bits simply means that increasing digital input codes will produce an increasing analog output.

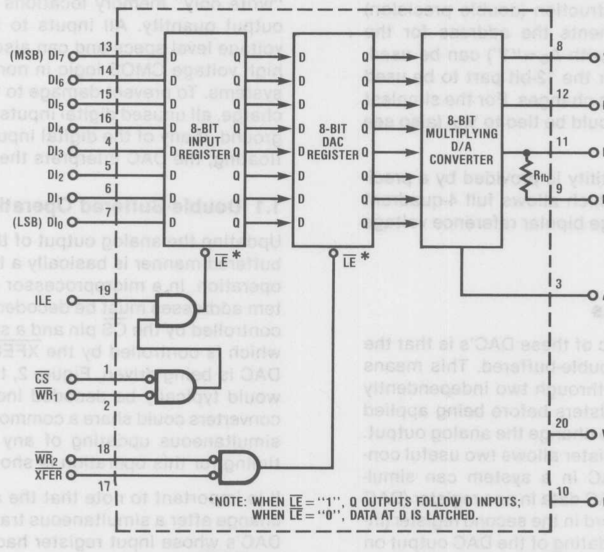
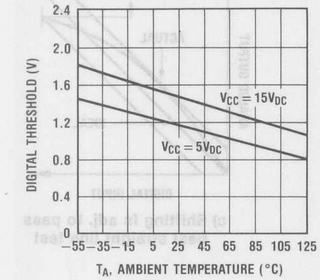
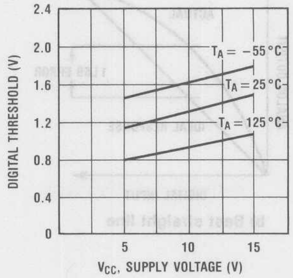


Figure 1. DAC0830 Functional Diagram

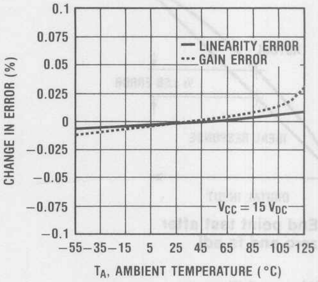
Digital Input Threshold vs. Temperature



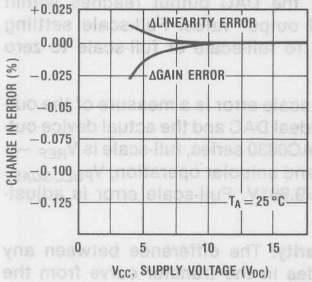
Digital Input Threshold vs. V_{CC}



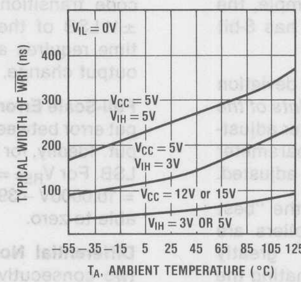
Gain and Linearity Error Variation vs. Temperature



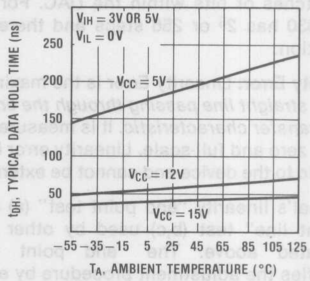
Gain and Linearity Error Variation vs. Supply Voltage



Typical Write Pulse Width



Typical Data Hold Time



DAC0830 Series Application Hints

These DAC's are the industry's first microprocessor compatible, double-buffered 8-bit multiplying D to A converters. Double-buffering allows the utmost application flexibility from a digital control point of view. This 20-pin device is also pin for pin compatible (with one exception) with the DAC1230, a 12-bit MICRO-DAC™. In the event that a system's analog output resolution and accuracy must be upgraded, substituting the DAC1230 can be easily accomplished. By tying address bit A_0 to the ILE pin, a two-byte μP write instruction (double precision) which automatically increments the address for the second byte write (starting with A_0 = "1") can be used. This allows either an 8-bit or the 12-bit part to be used with no hardware or software changes. For the simplest 8-bit application, this pin should be tied to V_{CC} (also see other uses in section 1.1).

Analog signal control versatility is provided by a precision R-2R ladder network which allows full 4-quadrant multiplication of a wide range bipolar reference voltage by an applied digital word.

1.0 Digital Considerations

A most unique characteristic of these DAC's is that the 8-bit digital input byte is double-buffered. This means that the data must transfer through two independently controlled 8-bit latching registers before being applied to the R-2R ladder network to change the analog output. The addition of a second register allows two useful control features. First, any DAC in a system can simultaneously hold the current DAC data in one register (DAC register) and the next data word in the second register (input register) to allow fast updating of the DAC output on demand. Second, and probably more important, double-buffering allows any number of DAC's in a system to be updated to their new analog output levels simultaneously via a common strobe signal.

The timing requirements and logic level convention of the register control signals have been designed to minimize or eliminate external interfacing logic when applied to most popular microprocessors and development systems. It is easy to think of these converters as 8-bit "write only" memory locations that provide an analog output quantity. All inputs to these DAC's meet TTL voltage level specs and can also be driven directly with high voltage CMOS logic in non-microprocessor based systems. To prevent damage to the chip from static discharge, all unused digital inputs should be tied to V_{CC} or ground. If any of the digital inputs are inadvertantly left floating, the DAC interprets the pin as a logic "1".

1.1 Double-Buffered Operation

Updating the analog output of these DAC's in a double-buffered manner is basically a two step or double write operation. In a microprocessor system two unique system addresses must be decoded, one for the input latch controlled by the $\overline{CS}$ pin and a second for the DAC latch which is controlled by the $\overline{XFER}$ line. If more than one DAC is being driven, Figure 2, the $\overline{CS}$ line of each DAC would typically be decoded individually, but all of the converters could share a common $\overline{XFER}$ address to allow simultaneous updating of any number of DAC's. The timing for this operation is shown, Figure 3.

It is important to note that the analog outputs that will change after a simultaneous transfer are those from the DAC's whose input register had been modified prior to the $\overline{XFER}$ command.

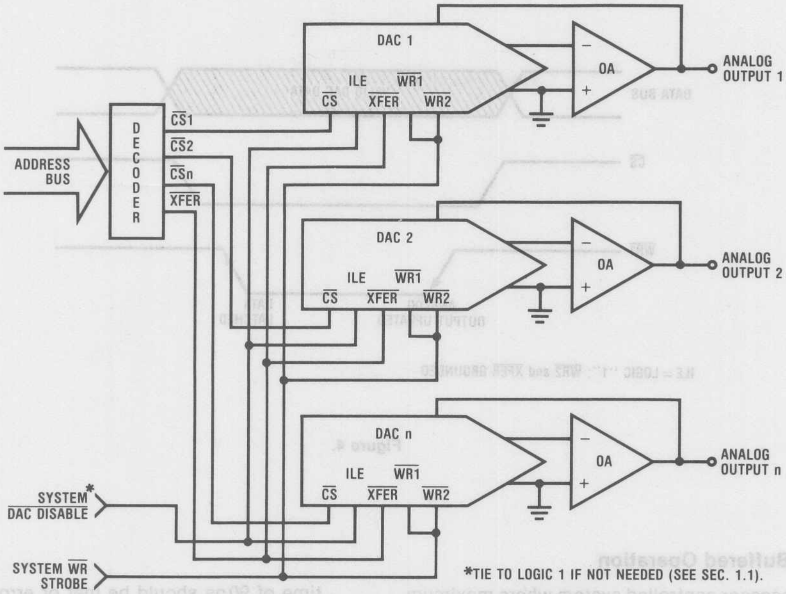


Figure 2. Controlling Multiple DAC's

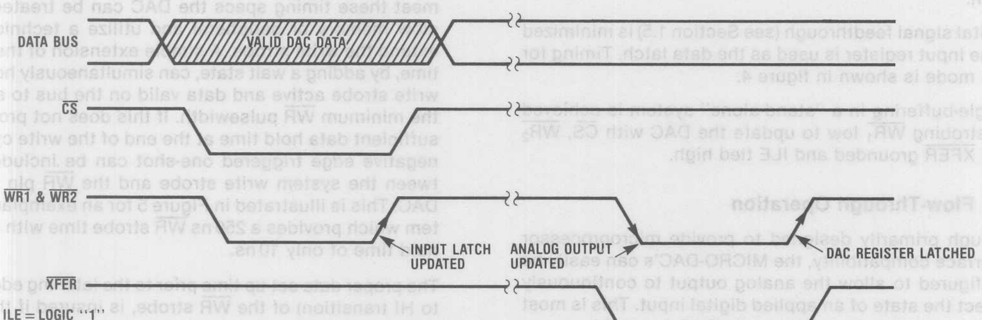


Figure 3.

The ILE pin is an active high chip select which can be decoded from the address bus as a qualifier for the normal $\overline{CS}$ signal generated during a write operation. This can be used to provide a higher degree of decoding unique control signals for a particular DAC, and thereby create a more efficient addressing scheme.

Another useful application of the ILE pin of each DAC in a multiple DAC system is to tie these inputs together and use this as a control line that can effectively "freeze" the outputs of all the DAC's at their present value. Pulling this line low latches the input register and prevents new data from being written to the DAC. This can be particularly useful in multiprocessing systems to allow a processor other than the one controlling the DAC's to take over control of the data bus and control lines. If this second system were to use the same addresses as those decoded for DAC control (but for a different purpose) the ILE function would prevent the DAC's from being erroneously altered.

In a "Stand-Alone" system the control signals are generated by discrete logic. In this case double-buffering can be controlled by simply taking $\overline{CS}$ and $\overline{XFER}$ to a logic "0", ILE to a logic "1" and pulling $\overline{WR}_1$ low to load data to the input latch. Pulling $\overline{WR}_2$ low will then update the analog output. A logic "1" on either of these lines will prevent the changing of the analog output.

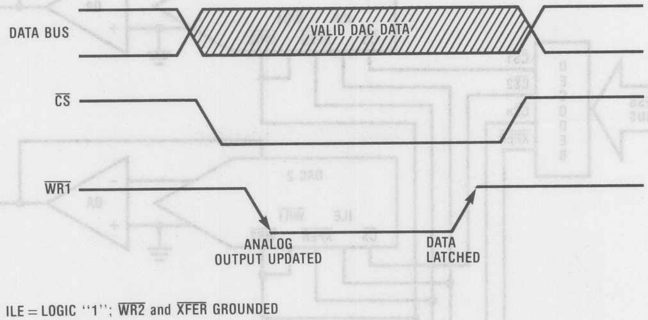


Figure 4.

1.2 Single-Buffered Operation

In a microprocessor controlled system where maximum data throughput to the DAC is of primary concern, or when only one DAC of several needs to be updated at a time, a single-buffered configuration can be used. One of the two internal registers allows the data to flow through and the other register will serve as the data latch.

Digital signal feedthrough (see Section 1.5) is minimized if the input register is used as the data latch. Timing for this mode is shown in figure 4.

Single-buffering in a "stand-alone" system is achieved by strobing $\overline{WR_1}$ low to update the DAC with $\overline{CS}$, $\overline{WR_2}$ and $\overline{XFER}$ grounded and ILE tied high.

1.3 Flow-Through Operation

Though primarily designed to provide microprocessor interface compatibility, the MICRO-DAC's can easily be configured to allow the analog output to continuously reflect the state of an applied digital input. This is most useful in applications where the DAC is used in a continuous feedback control loop and is driven by a binary up-down counter, or in function generation circuits where a ROM is continuosly providing DAC data.

Simply grounding $\overline{CS}$, $\overline{WR_1}$, $\overline{WR_2}$, and $\overline{XFER}$ and tying ILE high allows both internal registers to follow the applied digital inputs (flow-through) and directly affect the DAC analog output.

1.4 Control Signal Timing

When interfacing these MICRO-DAC's to any microprocessor, there are two important time relationships that must be considered to insure proper operation. The first is the minimum $\overline{WR}$ strobe pulse width which is specified as 500 ns for all valid operating conditions of supply voltage and ambient temperature, but typically a pulse width of only 100 ns is adequate if $V_{CC} = 15V_{DC}$. A second consideration is that the guaranteed minimum data hold time of 90 ns should be met or erroneous data can be latched. This hold time is defined as the length of time data must be held valid on the digital inputs *after* a qualified (via $\overline{CS}$) $\overline{WR}$ strobe makes a low to high transition to latch the applied data.

If the controlling device or system does not inherently meet these timing specs the DAC can be treated as a slow memory or peripheral and utilize a technique to extend the write strobe. A simple extension of the write time, by adding a wait state, can simultaneously hold the write strobe active and data valid on the bus to satisfy the minimum $\overline{WR}$ pulsewidth. If this does not provide a sufficient data hold time at the end of the write cycle, a negative edge triggered one-shot can be included between the system write strobe and the $\overline{WR}$ pin of the DAC. This is illustrated in Figure 5 for an exemplary system which provides a 250 ns $\overline{WR}$ strobe time with a data hold time of only 10 ns.

The proper data set-up time prior to the latching edge (LO to HI transition) of the $\overline{WR}$ strobe, is insured if the $\overline{WR}$ pulsewidth is within spec and the data is valid on the bus for the duration of the DAC $\overline{WR}$ strobe.

1.5 Digital Signal Feedthrough

When data is latched in the internal registers, but the digital inputs are changing state, a narrow spike of current may flow out of the current output terminals. This spike is caused by the rapid switching of internal logic gates that are responding to the input changes.

There are several recommendations to minimize this effect. When latching data in the DAC, always use the input register as the latch. Second, reducing the V_{CC} supply for the DAC from +15 volts to the +5V offers a factor of 5 improvement in the magnitude of the feedthrough, but at the expense of internal logic switching speed. Finally, increasing C_C (Figure 8) to a value consistent with the actual circuit bandwidth requirements can provide a substantial damping effect on any output spikes.

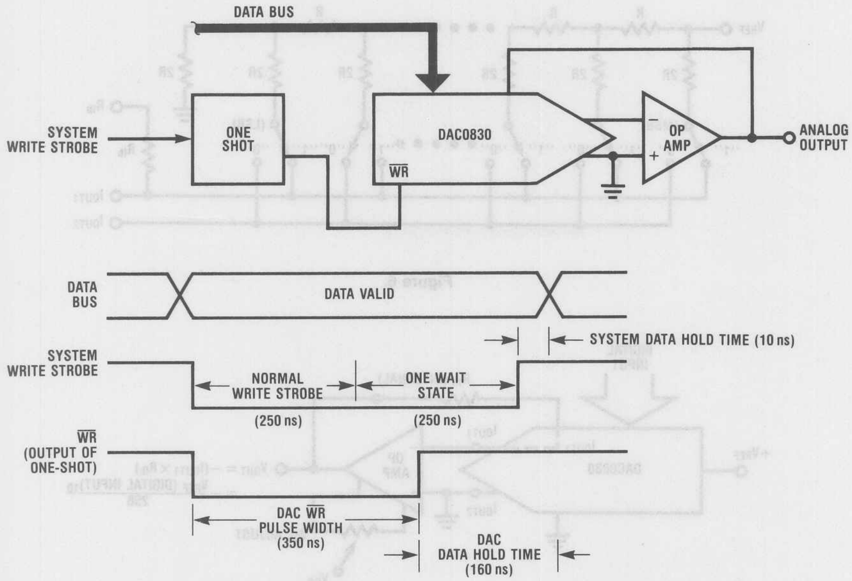


Figure 5. Accommodating a High Speed System

2.0 Analog Considerations

The fundamental purpose of any D to A converter is to provide an accurate analog output quantity which is representative of the applied digital word. In the case of the DAC0830, the output, I_{OUT1}, is a current directly proportional to the product of the applied reference voltage and the digital input word. For application versatility, a second output, I_{OUT2}, is provided as a current directly proportional to the complement of the digital input. Basically:

$$I_{OUT1} = \frac{V_{REF}}{15\,k\Omega} \times \frac{\text{Digital Input}}{256};$$

$$I_{OUT2} = \frac{V_{REF}}{15\,k\Omega} \times \frac{255 - \text{Digital Input}}{256}$$

where the digital input is the decimal (base 10) equivalent of the applied 8-bit binary word (0 to 255), V_{REF} is the voltage at pin 8 and 15 kΩ is the nominal value of the internal resistance, R, of the R-2R ladder network (discussed in Section 2.1).

Several factors external to the DAC itself must be considered to maintain analog accuracy and are covered in subsequent sections.

2.1 The Current Switching R-2R Ladder

The analog circuitry, Figure 6, consists of a silicon-chromium (SiCr or Si-chrome) thin film R-2R ladder which is deposited on the surface oxide of the monolithic chip. As a result, there are no parasitic diode problems with the ladder (as there may be with diffused resistors) so the reference voltage, V_{REF}, can range −10V to +10V even if V_{CC} for the device is $5V_{DC}$.

The digital input code to the DAC simply controls the position of the SPDT current switches and steers the available ladder current to either I_{OUT1} or I_{OUT2} as determined by the logic input level ("1" or "0") respectively, as shown in Figure 6. The MOS switches operate in the current mode with a small voltage drop across them and can therefore switch currents of either polarity. This is the basis for the 4-quadrant muliplying feature of this DAC.

2.2 Basic Unipolar Output Voltage

To maintain linearity of output current with changes in the applied digital code, it is important that the voltages at both of the current output pins be as near ground potential ($0V_{DC}$) as possible. With $V_{REF} = +10V$ every millivolt appearing at either I_{OUT1} or I_{OUT2} will cause a 0.01% linearity error. In most applications this output current is converted to a voltage by using an op amp as shown in Figure 7.

The inverting input of the op amp is a "virtual ground" created by the feedback from its output through the internal 15 kΩ resistor, R_{fb}. All of the output current (determined by the digital input and the reference voltage) will flow through R_{fb} to the output of the amplifier. Two-quadrant operation can be obtained by reversing the polarity of V_{REF} thus causing I_{OUT1} to flow into the DAC and be sourced from the output of the amplifier. The output voltage, in either case, is always equal to $I_{OUT1} \times R_{fb}$ and is the opposite polarity of the reference voltage.

The reference can be either a stable DC voltage souce or an AC signal anywhere in the range from −10V to +10V. The DAC can be thought of as a digitally controlled attenuator: the output voltage is always less than or equal to the applied reference voltage. The V_{REF} terminal of the device presents a nominal impedance of 15 kΩ to ground to external circuitry.

Always use the internal R_{fb} resistor to create an output voltage since this resistor matches (and tracks with temperature) the value of the resistors used to generate the output current (I_{OUT1}).

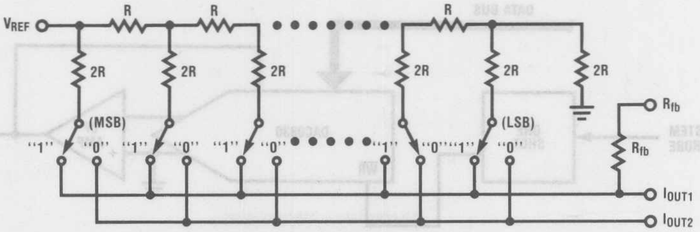


Figure 6.

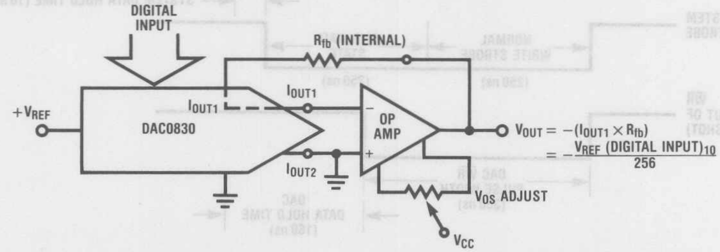


Figure 7.

2.3 Op Amp Considerations

The op amp used in Figure 7 should have offset voltage nulling capability (See Section 2.5).

The selected op amp should have as low a value of input bias current as possible. The product of the bias current times the feedback resistance creates an output voltage error which can be significant in low reference voltage applications. BI-FET™* op amps are highly recommended for use with these DACs because of their very low input current.

Transient response and settling time of the op amp are important in fast data throughput applications. The largest stability problem is the feedback pole created by the feedback resistance, R_{fb}, and the output capacitance of the DAC. This appears from the op amp output to the (−) input and includes the stray capacitance at this node. Addition of a lead capacitance, C_C in Figure 8, greatly reduces overshoot and ringing at the output for a step change in DAC output current.

Finally, the output voltage swing of the amplifier must be greater than V_{REF} to allow reaching the full scale output voltage. Depending on the loading on the output of the amplifier and the available op amp supply voltages (only ±12 volts in many development systems), a reference voltage less than 10 volts may be necessary to obtain the full analog output voltage range.

*BI-FET is a trademark of National Semiconductor Corporation.

2.4 Bipolar Output Voltage with a Fixed Reference

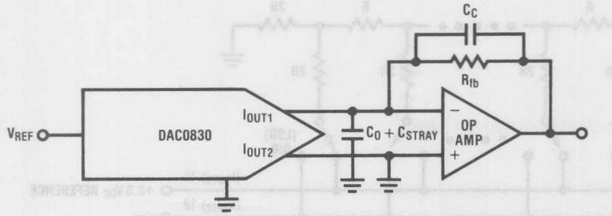
The addition of a second op amp to the previous circuitry can be used to generate a bipolar output voltage from a fixed reference voltage. This, in effect, gives sign significance to the MSB of the digital input word and allows two-quadrant multiplication of the reference voltage. The polarity of the reference can also be reversed to realize full 4-quadrant multiplication: $\pm V_{REF} \times \pm$Digital Code $= \mp V_{OUT}$. This circuit is shown in Figure 9.

This configuration features several improvements over existing circuits for bipolar outputs with other multiplying DAC's. Only the offset voltage of amplifier 1 has to be nulled to preserve linearity of the DAC. The offset voltage error of the second op amp (although a constant output voltage error) has no effect on linearity. It should be nulled only if absolute output accuracy is required. Finally, the values of the resistors around the second amplifier do not have to match the internal DAC resistors, they need only to match and temperature track each other. A thin film 4-resistor network available from Beckman Instruments, Inc. (part no. 694-3-R10K-D) is ideally suited for this application. These resistors are matched to 0.1% and exhibit only 5 ppm/°C resistance tracking tempco. Two of the four available 10 kΩ resistors can be paralleled to form R in Figure 9 and the other two can be used independently as the resistances labeled 2R.

2.5 Zero Adjustment

For accurate conversions, the input offset voltage of the output amplifier must always be nulled. Amplifier offset errors create an overall degradation of DAC linearity.

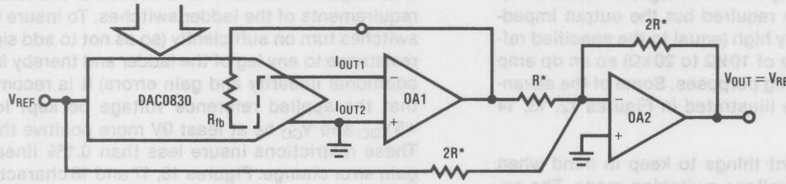
The fundamental purpose of zeroing is to make the voltage appearing at the DAC outputs as near $0V_{DC}$ as possible. This is accomplished for the typical DAC — op amp connection (Figure 7) by shorting out R_{fb}, the amplifier feedback resistor, and adjusting the V_{OS} nulling potentiometer of the op amp until the output reads zero volts. This is done, of course, with an applied digital code of all zeros if I_{OUT1} is driving the op amp (all one's for I_{OUT2}). The short around R_{fb} is then removed and the converter is zero adjusted.



OP AMP	C_C	t_s (0 TO FULL SCALE)
LF356	22 pF	4 μs
LF351	22 pF	5 μs
LF357*	10 pF	2 μs

*2.4kΩ RESISTOR ADDED FROM (−) INPUT TO GROUND TO INSURE STABILITY

Figure 8.



$$V_{OUT} = V_{REF} \frac{(\text{DIGITAL CODE} - 128)}{128}$$

$$1\ \text{LSB} = \frac{|V_{REF}|}{128}$$

*THESE RESISTORS ARE AVAILABLE FROM BECKMAN INSTRUMENTS, INC. AS THEIR PART NO. 694-3-R10K-D

INPUT CODE	IDEAL V_{OUT}	
MSB . . . LSB	$+V_{REF}$	$-V_{REF}$
1 1 1 1 1 1 1 1	$V_{REF} - 1\ \text{LSB}$	$\lvert V_{REF}\rvert + 1\ \text{LSB}$
1 1 0 0 0 0 0 0	$V_{REF}/2$	$-\lvert V_{REF}\rvert/2$
1 0 0 0 0 0 0 0	0	0
0 1 1 1 1 1 1 1	$-1\ \text{LSB}$	$+1\ \text{LSB}$
0 0 1 1 1 1 1 1	$-\frac{\lvert V_{REF}\rvert}{2} - 1\ \text{LSB}$	$\frac{\lvert V_{REF}\rvert}{2} + 1\ \text{LSB}$
0 0 0 0 0 0 0 0	$-\lvert V_{REF}\rvert$	$+\lvert V_{REF}\rvert$

Figure 9.

2.6 Full-Scale Adjustment

In the case where the matching of R_{fb} to the R value of the R-2R ladder (typically ±0.2%) is insufficient for full-scale accuracy in a particular application, the V_{REF} voltage can be adjusted or an external resistor and potentiometer can be added as shown in Figure 10 to provide a full-scale adjustment.

The temperature coefficients of the resistors used for this adjustment are an important concern. To prevent degradation of the gain error tempco by the external resistors, their temperature coefficients ideally would have to match that of the internal DAC resistors, which is a highly impractical constraint. For the values shown in Figure 10, if the resistor and the potentiometer each had a temperature coefficient of ±100 ppm/°C maximum, the overall gain error tempco would be degraded a maximum of 0.0025%/°C for an adjustment pot setting of less than 3% of R_{fb}.

2.7 Using the DAC0830 in a Voltage Switching Configuration

The R-2R ladder can also be operated as a voltage switching network. In this mode the ladder is used in an inverted manner from the standard current switching configuration. The reference voltage is connected to one of the current output terminals (I_{OUT1} for true binary digital control, I_{OUT2} is for complementary binary) and the output voltage is taken from the normal V_{REF} pin. The converter output is now a voltage in the range from 0V to 255/256 V_{REF} as a function of the applied digital code as shown in Figure 11.

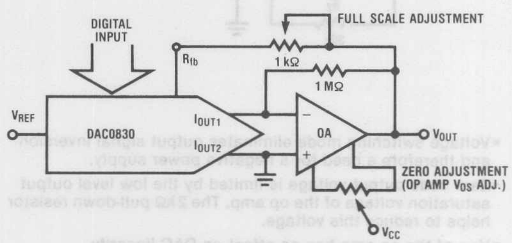


Figure 10. Adding Full-Scale Adjustment

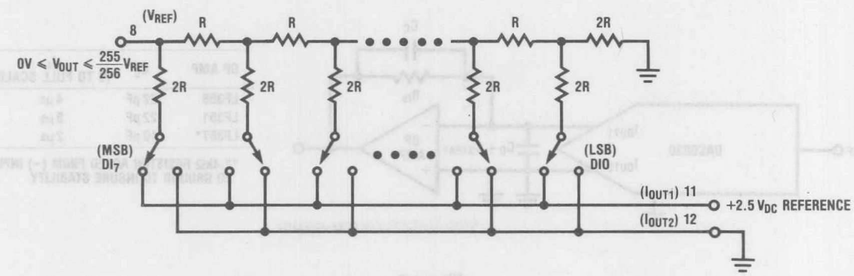
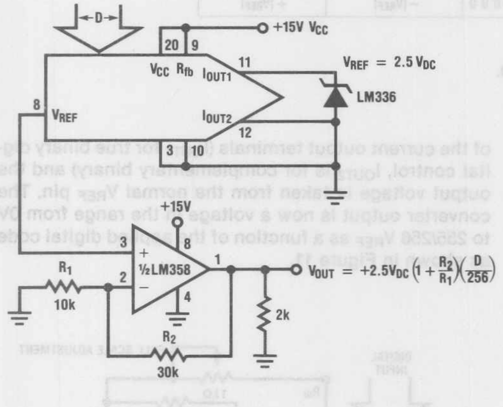


Figure 11. Voltage Mode Switching

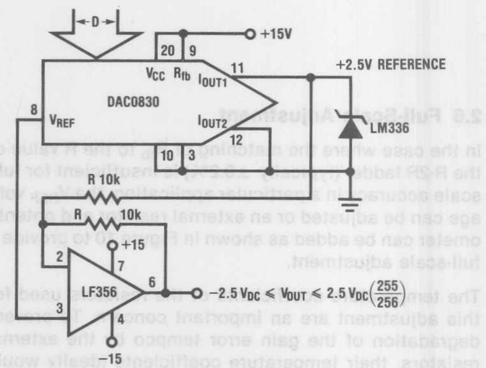
This configuration offers several useful application advantages. Since the output is a voltage, an external op amp is not necessarily required but the output impedance of the DAC is fairly high (equal to the specified reference input resistance of 10 kΩ to 20 kΩ) so an op amp may be used for buffering purposes. Some of the advantages of this mode are illustrated in Figures 12, 13, 14 and 15.

There are two important things to keep in mind when using this DAC in the voltage switching mode. The applied reference voltage must be positive since there are internal parasitic diodes from ground to the I_{OUT1} and I_{OUT2} terminals which would turn on if the applied reference went negative. There is also a dependence of conversion linearity and gain error on the voltage difference between V_{CC} and the voltage applied to the normal current output terminals. This is a result of the voltage drive requirements of the ladder switches. To insure that all 8 switches turn on sufficiently (so as not to add significant resistance to any leg of the ladder and thereby introduce additional linearity and gain errors) it is recommended that the applied reference voltage be kept less than $+5\,V_{DC}$ and V_{CC} be at least 9V more positive than V_{REF}. These restrictions insure less than 0.1% linearity and gain error change. Figures 16, 17 and 18 characterize the effects of bringing V_{REF} and V_{CC} closer together as well as typical temperature performance of this voltage switching configuration.



- Voltage switching mode eliminates output signal inversion and therefore a need for a negative power supply.
- Zero code output voltage is limited by the low level output saturation voltage of the op amp. The 2 kΩ pull-down resistor helps to reduce this voltage.
- V_{OS} of the op amp has no effect on DAC linearity.

Figure 12. Single Supply DAC



- $V_{OUT} = 2.5\,V\left(\frac{D}{128} - 1\right)$
- Slewing and settling time for a full scale output change is ≈ 1.8 μs

Figure 13. Obtaining a Bipolar Output from a Fixed Reference with a Single Op Amp

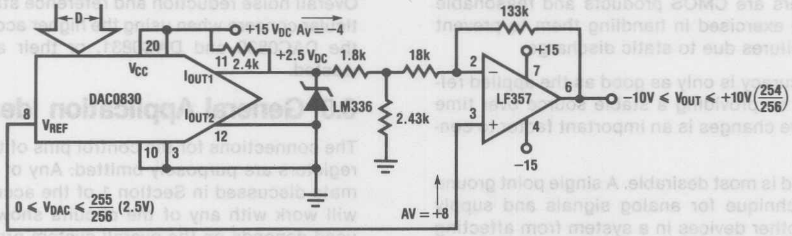
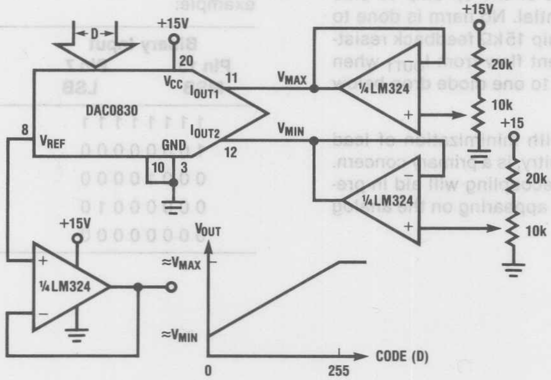


Figure 14. Bipolar Output with Increased Output Voltage Swing



- Only a single +15V supply required
- Non-interactive full-scale and zero code output adjustments
- V_{MAX} and V_{MIN} must be ≤ +5VDC and ≥ 0V.
- Incremental Output Step $= \frac{1}{256}\,(V_{MAX} - V_{MIN})$.
- $V_{OUT} = \frac{D}{256}(V_{MAX} - V_{MIN}) + \frac{255}{256}\,V_{MIN}$

Figure 15. Single Supply DAC with Level Shift and Span-Adjustable Output

Gain and Linearity Error Variation vs. Supply Voltage

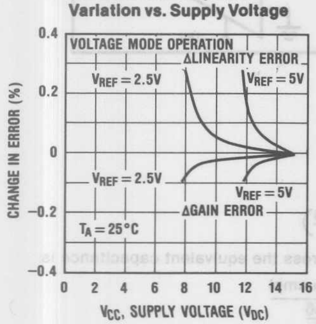


Figure 16.

Gain and Linearity Error Variation vs. Reference Voltage

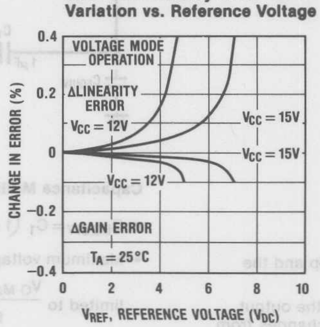


Figure 17.

Gain and Linearity Error Variation vs. Temperature

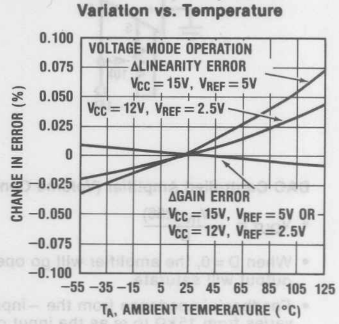


Figure 18.

NOTE: For these curves, V_{REF} is the voltage applied to pin 11 (I_{OUT1}) with pin 12 (I_{OUT2}) grounded.

Conversion accuracy is only as good as the applied reference voltage so providing a stable source over time and temperature changes is an important factor to consider.

A "good" ground is most desirable. A single point ground distribution technique for analog signals and supply returns keeps other devices in a system from affecting the output of the DAC's.

During power-up supply voltage sequencing, the −15V (or −12V) supply of the op amp may appear first. This will typically cause the output of the op amp to bias near the negative supply potential. No harm is done to the DAC, however, as the on-chip 15 kΩ feedback resistor sufficiently limits the current flow from I_{OUT1} when this lead is internally clamped to one diode drop below ground.

Careful circuit construction with minimization of lead lengths around the analog circuitry, is a primary concern. Good high frequency supply decoupling will aid in preventing inadvertant noise from appearing on the analog output.

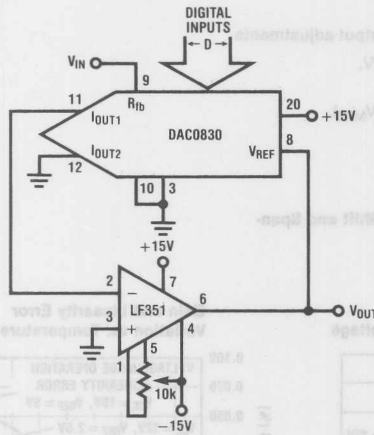
wasted.

3.0 General Application Ideas

The connections for the control pins of the digital input registers are purposely omitted. Any of the control formats discussed in Section 1 of the accompanying text will work with any of the circuits shown. The method used depends on the overall system provisions and requirements.

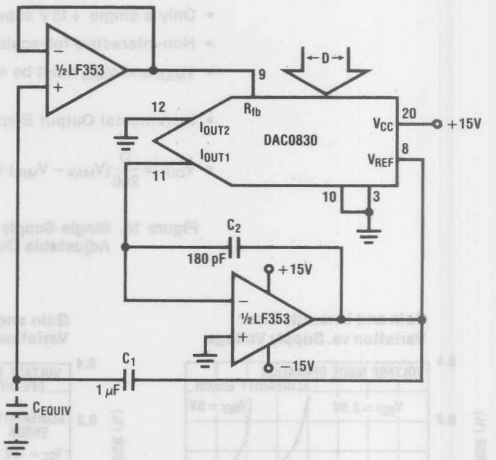
The digital input code is referred to as D and represents the decimal equivalent value of the 8-bit binary input, for example:

Binary Input Pin 13 MSB	Pin 7 LSB	D Decimal Equivalent
1 1 1 1 1 1 1 1		255
1 0 0 0 0 0 0 0		128
0 0 0 1 0 0 0 0		16
0 0 0 0 0 0 1 0		2
0 0 0 0 0 0 0 0		0



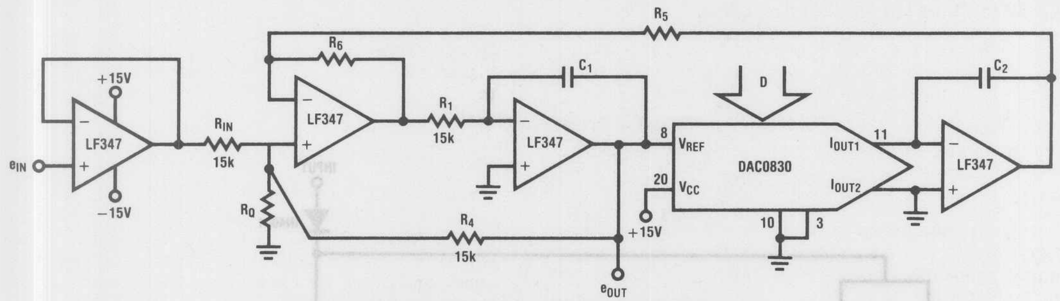
DAC Controlled Amplifier (Volume Control)

- $V_{OUT} = \frac{-V_{IN}\,(256)}{D}$
- When D = 0, the amplifier will go open loop and the output will saturate.
- Feedback impedance from the − input to the output varies from 15 kΩ to ∞ as the input code changes from full-scale to zero.



Capacitance Multiplier

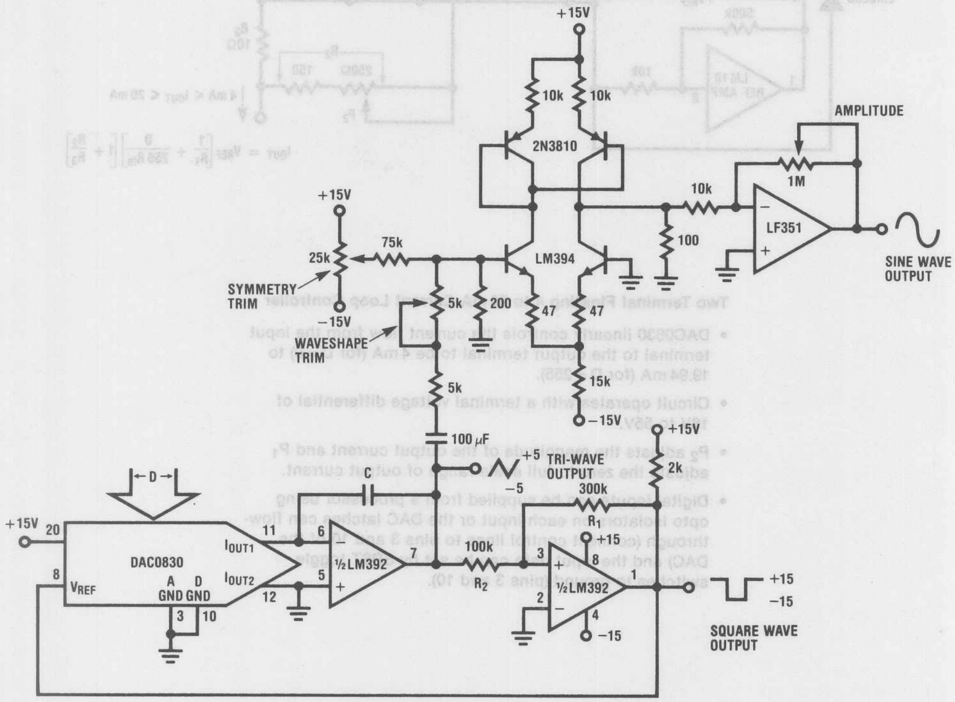
- $C_{EQUIV} = C_1 \left(1 + \frac{256}{D}\right)$
- Maximum voltage across the equivalent capacitance is limited to $\frac{V_{O\,MAX}\text{ (op amp)}}{1 + \frac{256}{D}}$
- C_2 is used to improve settling time of op amp.



Variable f_O, Variable Q_O, Constant BW Bandpass Filter

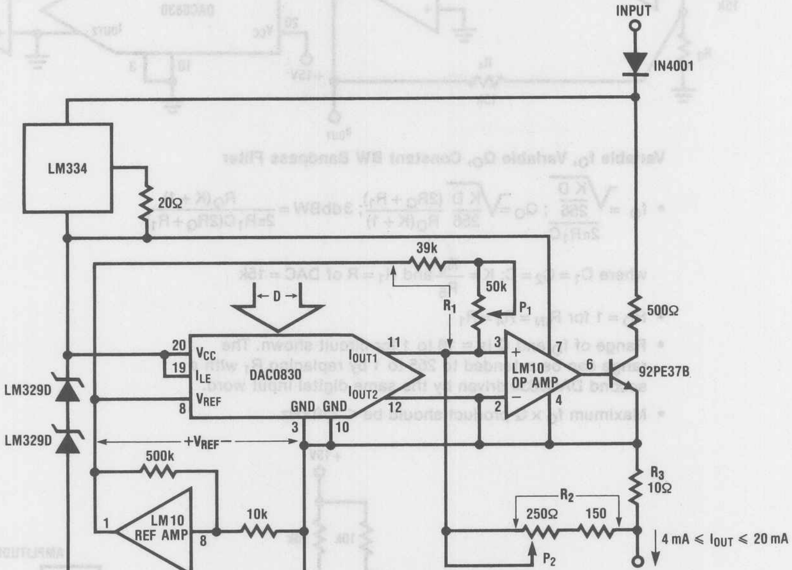
- $f_O = \dfrac{\sqrt{\dfrac{K\,D}{256}}}{2\pi R_1 C}$; $Q_O = \sqrt{\dfrac{K\,D}{256}}\,\dfrac{(2R_Q+R_1)}{R_Q(K+1)}$; $3\,\text{dbBW} = \dfrac{R_Q(K+1)}{2\pi R_1 C(2R_Q+R_1)}$

  where $C_1 = C_2 = C$; $K = \dfrac{R_6}{R_5}$ and $R_1 = R$ of DAC $= 15k$
- $H_O = 1$ for $R_{IN} = R_4 = R_1$
- Range of f_O and Q is ≈ 16 to 1 for circuit shown. The range can be extended to 255 to 1 by replacing R_1 with a second DAC0830 driven by the same digital input word.
- Maximum $f_O \times Q$ product should be ≤ 200 kHz.



DAC Controlled Function Generator

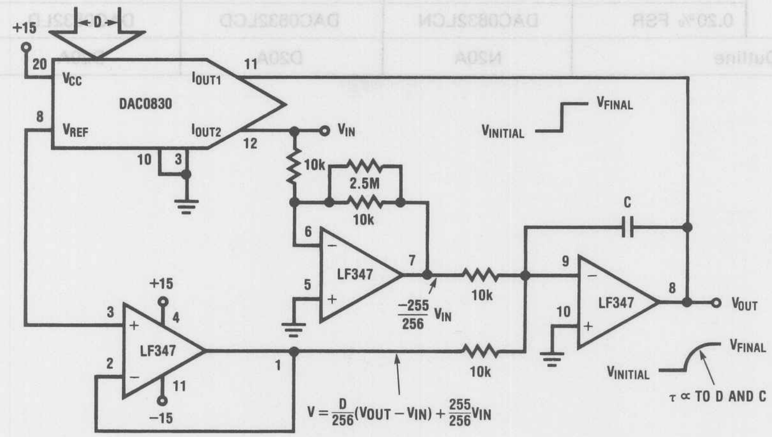
- DAC controls the frequency of sine, square, and triangle outputs.
- $f = \dfrac{D}{256(20k)C}$ for $V_{0MAX} = V_{0MIN}$ of square wave output and $R_1 = 3R_2$.
- 255 to 1 linear frequency range; oscillator stops with D = 0
- Trim symmetry and wave-shape for minimum sine wave distortion.



$$I_{OUT} = V_{REF}\left[\frac{1}{R_1} + \frac{D}{256\,R_{fb}}\right]\left[1 + \frac{R_2}{R_3}\right]$$

Two Terminal Floating 4 to 20 mA Current Loop Controller

- DAC0830 linearly controls the current flow from the input terminal to the output terminal to be 4 mA (for D = 0) to 19.94 mA (for D = 255).
- Circuit operates with a terminal voltage differential of 16V to 55V.
- P_2 adjusts the magnitude of the output current and P_1 adjusts the zero to full scale range of output current.
- Digital inputs can be supplied from a processor using opto isolators on each input or the DAC latches can flow-through (connect control lines to pins 3 and 10 of the DAC) and the input data can be set by SPST toggle switches to ground (pins 3 and 10).



DAC Controlled Exponential Time Response

- Output responds exponentially to input changes and automatically stops when $V_{OUT} = V_{IN}$
- Output time constant is directly proportional to the DAC input code and capacitor C
- Input voltage must be positive (See section 2.7)

Temperature Range		0°C to +70°C	−40°C to +85°C	−55°C to +125°C
Linearity Error	0.05% FSR	DAC0830LCN	DAC0830LCD	DAC0830LD
	0.10% FSR	DAC0831LCN	DAC0831LCD	DAC0831LD
	0.20% FSR	DAC0832LCN	DAC0832LCD	DAC0832LD
Package Outline		N20A	D20A	D20A

National Semiconductor

MICRO-DAC:™ DAC1000/1/2 and DAC1006/7/8, μP Compatible, Double-Buffered D to A Converters

General Description

The DAC1000/1/2 and DAC1006/7/8 are advanced CMOS/Si-Cr 10-, 9- and 8-bit accurate multiplying DACs which are designed to interface directly with the 8080, 8048, 8085, Z-80 and other popular microprocessors. These DACs appear as a memory location or an I/O port to the μP and no interfacing logic is needed.

These devices, combined with an external amplifier and voltage reference, can be used as standard D/A converters; and they are very attractive for multiplying applications (such as digitally controlled gain blocks) since their linearity error is essentially independant of the voltage reference. They become equally attractive in audio signal processing equipment as audio gain controls or as programmable attenuators which marry high quality audio signal processing to digitally based systems under microprocessor control.

All of these DACs are double buffered. They can load all 10 bits or two 8-bit bytes and the data format can be either right justified or left justified. The analog section of these DACs is essentially the same as that of the DAC1020.

The DAC1000 series are the 10-bit members of a family of microprocessor-compatible DAC's (MICRO-DAC's™). For applications requiring other resolutions, the DAC0830 series (8 bits) and the DAC1208 and DAC1230 (12 bits) are available alternatives.

Part #	Accuracy (bits)	Pin	Description
DAC1000	10	24	Has all logic features
DAC1001	9		
DAC1002	8		
DAC1006	10	20	For left-justified data
DAC1007	9		
DAC1008	8		

MICRO-DAC™ is a trademark of National Semiconductor Corp.

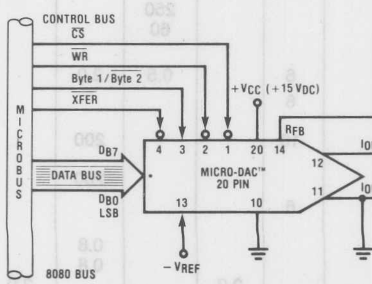
Features

- Uses easy to adjust END POINT specs, NOT BEST STRAIGHT LINE FIT
- Low power consumption
- Direct interface to all popular microprocessors.
- Integrated thin film on CMOS structure
- Double-buffered, single-buffered or flow through digital data inputs.
- Loads two 8-bit bytes or a single 10-bit word.
- Logic inputs which meet T^2L voltage level specs (1.4V logic threshold).
- Works with ±10V reference — full 4-quadrant multiplication.
- Operates STAND ALONE (without μP) if desired.
- Available in 0.3″ standard 20-pin and 0.6″ 24-pin package.
- Differential non-linearity selection available as special order.

Key Specifications

- Output Current Settling Time — 500 ns
- Resolution — 10 bits
- Linearity — 10, 9, and 8 bits (guaranteed over temp.)
- Gain Tempco — −0.0003% of FS/°C
- Low Power Dissipation (including ladder) — 20 mW
- Single Power Supply — 5 to 15 V_{DC}

Typical Application



DAC1006/1007/1008

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	17 V_{DC}
Voltage at any digital input	V_{CC} to GND
Voltage at V_{REF} input	±25V
Storage temperature range	−65°C to +150°C
Package dissipation at $T_A = 25°C$ (Note 3)	500 mW
DC voltage applied to I_{OUT1} or I_{OUT2} (Note 4)	−100 mV to V_{CC}
Lead temperature (soldering, 10 seconds)	300°C

Operating Ratings

Temperature Range	
Part numbers with 'LCN' suffix	0°C to 70°C
Part numbers with 'LCD' suffix	−40°C to +85°C
Part numbers with 'LD' Suffix	−55°C to +125°C
Voltage at any digital input	V_{CC} to GND

General Electrical Characteristics $T_A = 25°C$, $V_{REF} = 10.000\,V_{DC}$ unless otherwise noted

Parameter	Conditions	See Note	$V_{CC} = 12V_{DC} \pm 5\%$ to $15V_{DC} \pm 5\%$ Min.	Typ.	Max.	$V_{CC} = 5V_{DC} \pm 5\%$ Min.	Typ.	Max.	Units
Resolution					10			10	bits
Linearity Error	Endpoint adjust only	4,7							
	$T_{MIN} < T_A < T_{MAX}$	6							
	$-10V \leq V_{REF} \leq +10V$	5							
	DAC1000 and 1006				0.05			0.05	% of FSR
	DAC1001 and 1007				0.1			0.1	% of FSR
	DAC1002 and 1008				0.2			0.2	% of FSR
Differential Nonlinearity	Endpoint adjust only	4,7							
	$T_{MIN} < T_A < T_{MAX}$	6							
	$-10V \leq V_{REF} \leq +10V$	5							
	DAC1000 and 1006				0.1			0.1	% of FSR
	DAC1001 and 1007				0.2			0.2	% of FSR
	DAC1002 and 1008				0.4			0.4	% of FSR
Monotonicity	$T_{MIN} < T_A < T_{MAX}$	4,6							
	$-10V \leq V_{REF} \leq +10V$	5							
	DAC1000 and 1006		10			10			bits
	DAC1001 and 1007		9			9			bits
	DAC1002 and 1008		8			8			bits
Gain Error	Using internal R_{fb}								
	$-10V \leq V_{REF} \leq +10V$	5	−1.0	±0.3	1.0	−1.0	±0.3	1.0	% of FS
Gain Error Tempco	$T_{MIN} < T_A < T_{MAX}$	6							
	Using internal R_{fb}	9		−0.0003	−0.001		−0.0006	−0.002	% of FS/°C
Power Supply Rejection	All digital inputs latched high								
	V_{CC} = 14.5V to 15.5V			0.003	0.008				% FSR/V
	11.5V to 12.5V			0.004	0.010				% FSR/V
	4.75V to 5.25V						0.033	0.10	% FSR/V
Reference Input Resistance			10	15	20	10	15	20	kΩ
Output Feedthrough Error	$V_{REF} = 20V_{P-P}$, f = 100 kHz								
	All data inputs latched low								
	D Package			130			130		mV_{P-P}
	N Package			90			90		mV_{P-P}
Output Capacitance I_{OUT1}	All data inputs			60			60		pF
I_{OUT2}	latched low			250			250		pF
I_{OUT1}	All data inputs			250			250		pF
I_{OUT2}	latched high			60			60		pF
Supply Current Drain	$T_{MIN} \leq T_A \leq T_{MAX}$	6		0.5	2.0		0.5	2.0	mA
Output Leakage Current	$T_{MIN} \leq T_A \leq T_{MAX}$	6							
I_{OUT1}	All data inputs latched low	10			200			200	nA
I_{OUT2}	All data inputs latched high				200			200	nA
Digital Input Voltages	$T_{MIN} \leq T_A \leq T_{MAX}$	6							
	Low level								
	LD suffix				0.8			0.6	V_{DC}
	LCD or LCN suffix				0.8			0.8	V_{DC}
	High level (all parts)		2.0			2.0			V_{DC}

General Electrical Characteristics $T_A = 25°C$, $V_{REF} = 10.000\ V_{DC}$ unless otherwise noted

Parameter		Conditions	See Note	$V_{CC} = 12V_{DC} \pm 5\%$ to $15V_{DC} \pm 5\%$ Min.	Typ.	Max.	$V_{CC} = 5V_{DC} \pm 5\%$ Min.	Typ.	Max.	Units
Digital Input Currents		$T_{MIN} \leq T_A \leq T_{MAX}$	6							
		Digital inputs < 0.8V			−40	−150		−40	−150	μA_{DC}
		Digital inputs > 2.0V			1.0	+10		1.0	+10	μA_{DC}
Current Settling Time	t_S	$V_{IL} = 0V$, $V_{IH} = 5V$			500			500		ns
Write and XFER Pulse Width	t_W	$V_{IL} = 0V$, $V_{IH} = 5V$, $T_A = 25°C$	8	150	60		320	200		ns
		$T_{MIN} \leq T_A \leq T_{MAX}$	9	320	100		500	250		ns
Data Set Up Time	t_{DS}	$V_{IL} = 0V$, $V_{IH} = 5V$, $T_A = 25°C$	9	150	80		320	170		ns
		$T_{MIN} \leq T_A \leq T_{MAX}$		320	120		500	250		ns
Data Hold Time	t_{DH}	$V_{IL} = 0V$, $V_{IH} = 5V$ $T_A = 25°C$	9	200	100		320	220		ns
		$T_{MIN} \leq T_A \leq T_{MAX}$		250	120		500	320		ns
Control Set Up Time	t_{CS}	$V_{IL} = 0V$, $V_{IL} = 5V$, $T_A = 25°C$	9	150	60		320	180		ns
		$T_{MIN} \leq T_A \leq T_{MAX}$		320	100		500	260		ns
Control Hold Time	t_{CH}	$V_{IL} = 0V$, $V_{IH} = 5V$, $T_A = 25°C$	9	10	0		10	0		ns
		$T_{MIN} \leq T_A \leq T_{MAX}$		10	0		10	0		ns

Note 1: *"Absolute Maximum Ratings"* are those values beyond which the safety of the device cannot be guaranteed. These specifications are not meant to imply that the devices should be operated at these *"Absolute Maximum"* limits.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: This 500 mW specification applies for all packages. The low intrinsic power dissipation of this part (and the fact that there is no way to significantly modify the power dissipation) removes concern for heat sinking.

Note 4: For current switching applications, both I_{OUT1} and I_{OUT2} must go to ground or the "Virtual Ground" of an operational amplifier. The linearity error is degraded by approximately $V_{OS} \div V_{REF}$. For example, if $V_{REF} = 10V$ then a 1 mV offset, V_{OS}, on I_{OUT1} or I_{OUT2} will introduce an additional 0.01% linearity error.

Note 5: Guaranteed at $V_{REF} = \pm 10\ V_{DC}$ and $V_{REF} = \pm 1\ V_{DC}$.

Note 6: $T_{MIN} = 0°C$ and $T_{MAX} = 70°C$ for "LCN" suffix parts.
$T_{MIN} = -40°C$ and $T_{MAX} = 85°C$ for "LCD" suffix parts.
$T_{MIN} = -55°C$ and $T_{MAX} = 125°C$ for "LD" suffix parts.

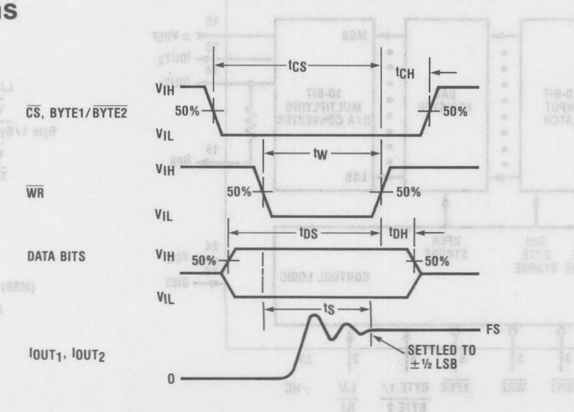
Note 7: The unit "FSR" stands for "Full Scale Range." "Linearity Error" and "Power Supply Rejection" specs are based on this unit to eliminate dependence on a particular V_{REF} value and to indicate the true performance of the part. The "Linearity Error" specification of the DAC1000 is "0.05% of FSR (MAX)." This guarantees that after performing a zero and full scale adjustment (See Sections 2.5 and 2.6), the plot of the 1024 analog voltage outputs will each be within $0.05\% \times V_{REF}$ of a straight line which passes through zero and full scale.

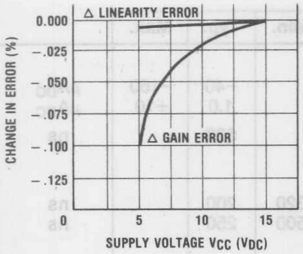
Note 8: This specification implies that all parts are guaranteed to operate with a write pulse or transfer pulse width (t_W) of 320 ns. A typical part will operate with t_W of only 100 ns. The entire write pulse must occur within the valid data interval for the specified t_W, t_{DS}, t_{DH}, and t_S to apply.

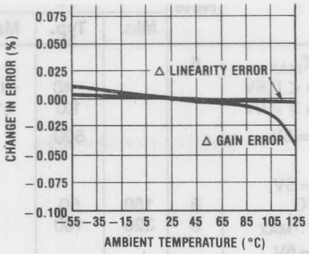
Note 9: Guaranteed by design but not tested.

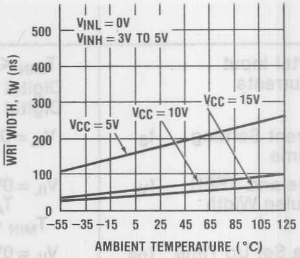
Note 10: A 200 nA leakage current with $R_{fb} = 20k$ and $V_{REF} = 10V$ corresponds to a zero error of $(200 \times 10^{-9} \times 20 \times 10^3) \times 100 \div 10$ which is 0.04% of FS.

Switching Waveforms

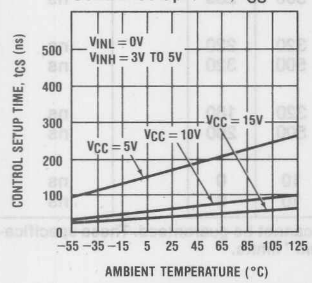




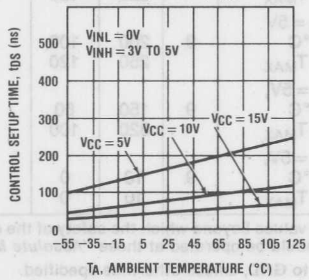




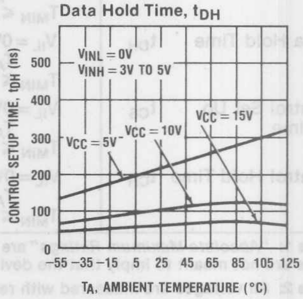
Control Setup Time, t_{CS}



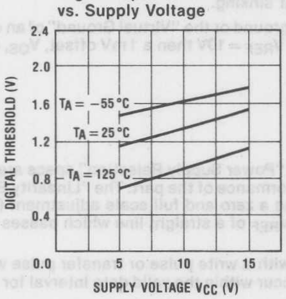
Data Setup Time, t_{DS}



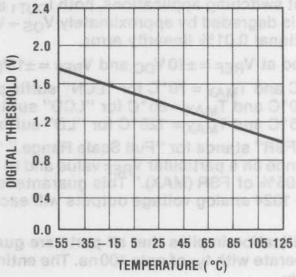
Data Hold Time, t_{DH}



Digital Input Threshold vs. Supply Voltage

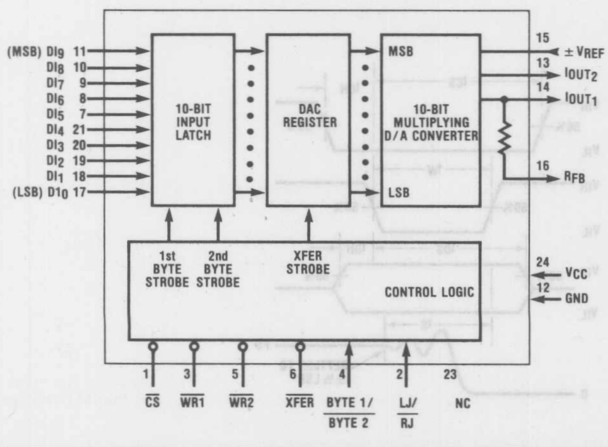


Digital Input Threshold vs. Temperature

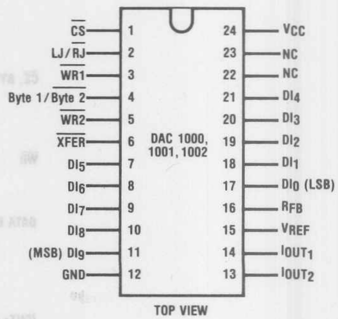


Block and Connection Diagrams

DAC1000/1001/1002 (24-Pin Parts)



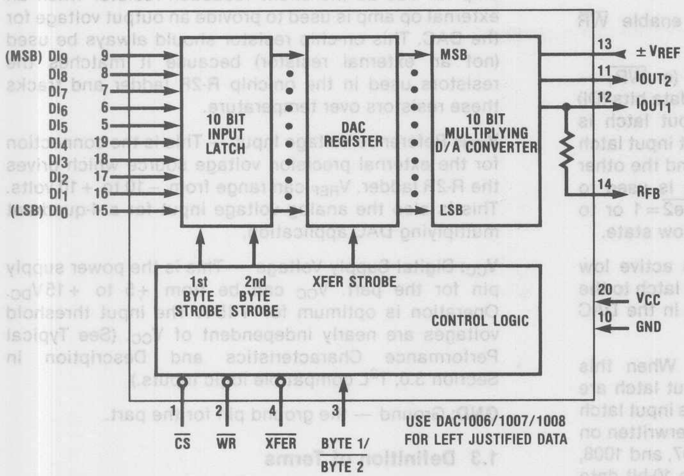
DAC1000/1001/1002 (24-Pin Parts)



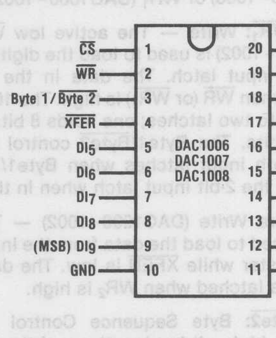
TOP VIEW

Block and Connection Diagrams (cont'd)

DAC1006/1007/1008 (20-Pin Parts)

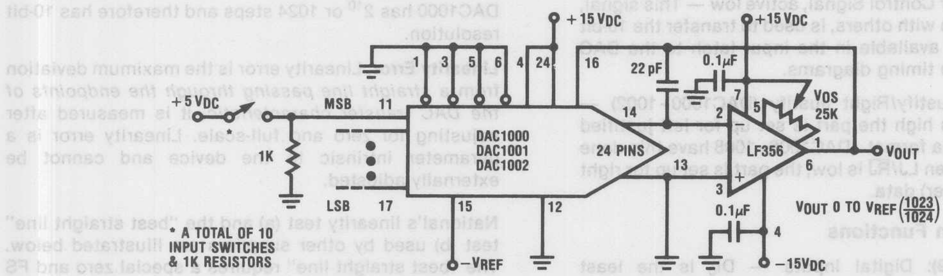


DAC1006/1007/1008 (20-Pin Parts)



TOP VIEW

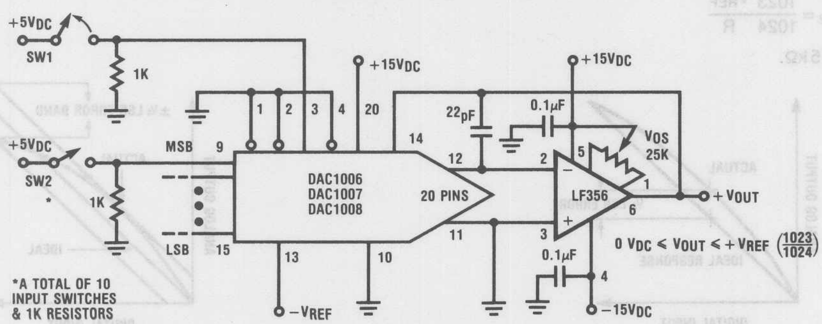
DAC1000/1001/1002 — Simple Hookup for a "Quick Look"



Notes:

1. For $V_{REF} = -10.240 V_{DC}$ the output voltage steps are approximately 10 mV each.
2. Operation is set up for flow through — no latching of digital input data.
3. Single point ground is strongly recommended.

DAC1006/1007/1008 — Simple Hookup for a "Quick Look"



Notes:

1. For $V_{REF} = -10.240 V_{DC}$ the output voltage steps are approximately 10 mV each.
2. SW1 is a normally closed switch. While SW1 is closed, the DAC register is latched and new data can be loaded into the input latch via the 10 SW2 switches. When SW1 is momentarily opened the new data is transferred from the input latch to the DAC register and is latched when SW1 again closes.

1.0 Definition of Package Pinouts

1.1 Control Signals (All control signals are level actuated.)

$\overline{CS}$: Chip Select — active low, it will enable $\overline{WR}$ (DAC1003-1008) or WR_1 (DAC1000-1002).

$\overline{WR}$ or $\overline{WR_1}$: Write — The active low $\overline{WR}$ (or $\overline{WR_1}$ — DAC1000-1002) is used to load the digital data bits (DI) into the input latch. The data in the input latch is latched when $\overline{WR}$ (or $\overline{WR_1}$) is high. The 10-bit input latch is split into two latches; one holds 8 bits and the other holds 2 bits. The Byte1/$\overline{\text{Byte2}}$ control pin is used to select both input latches when Byte1/$\overline{\text{Byte2}}$ = 1 or to overwrite the 2-bit input latch when in the low state.

$\overline{WR_2}$: Extra Write (DAC1000-1002) — The active low $\overline{WR_2}$ is used to load the data from the input latch to the DAC register while $\overline{XFER}$ is low. The data in the DAC register is latched when WR_2 is high.

Byte1/$\overline{\text{Byte2}}$: Byte Sequence Control — When this control is high, all ten locations of the input latch are enabled. When low, only two locations of the input latch are enabled and these two locations are overwritten on the second byte write. On the DAC1006, 1007, and 1008, the Byte1/$\overline{\text{Byte2}}$ must be low to transfer the 10-bit data in the input latch to the DAC register.

$\overline{XFER}$: Transfer Control Signal, active low — This signal, in combination with others, is used to transfer the 10-bit data which is available in the input latch to the DAC register — see timing diagrams.

LJ/$\overline{RJ}$: Left Justify/Right Justify (DAC1000-1002) — When LJ/$\overline{RJ}$ is high the part is set up for left justified (fractional) data format. (DAC1006-1008 have this done internally.) When LJ/$\overline{RJ}$ is low, the part is set up for right justified (integer) data.

1.2 Other Pin Functions

DI_i (i = 0 to 9): Digital Inputs — DI_0 is the least significant bit (LSB) and DI_9 is the most significant bit (MSB).

I_{OUT1}: DAC Current Output 1 — I_{OUT1} is a maximum for a digital input code of all 1s and is zero for a digital input code of all 0s.

I_{OUT2}: DAC Current Output 2 — I_{OUT2} is a constant minus I_{OUT1}, or

$$I_{OUT1} + I_{OUT2} = \frac{1023}{1024}\frac{V_{REF}}{R}$$

where $R \cong 15\,k\Omega$.

R_{FB}: Feedback Resistor — This is provided on the IC chip for use as the shunt feedback resistor when an external op amp is used to provide an output voltage for the DAC. This on-chip resistor should always be used (not an external resistor) because it matches the resistors used in the on-chip R-2R ladder and tracks these resistors over temperature.

V_{REF}: Reference Voltage Input — This is the connection for the external precision voltage source which drives the R-2R ladder. V_{REF} can range from −10 to +10 volts. This is also the analog voltage input for a 4-quadrant multiplying DAC application.

V_{CC}: Digital Supply Voltage — This is the power supply pin for the part. V_{CC} can be from +5 to $+15V_{DC}$. Operation is optimum for +15V. The input threshold voltages are nearly independent of V_{CC}. (See Typical Performance Characteristics and Description in Section 3.0, T^2L compatible logic inputs.)

GND: Ground — the ground pin for the part.

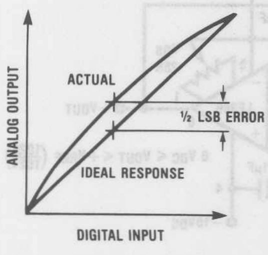
1.3 Definition of Terms

Resolution: Resolution is directly related to the number of switches or bits within the DAC. For example, the DAC1000 has 2^{10} or 1024 steps and therefore has 10-bit resolution.

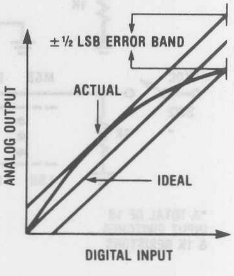
Linearity Error: Linearity error is the maximum deviation from a *straight line passing through the endpoints of the DAC transfer characteristic.* It is measured after adjusting for zero and full-scale. Linearity error is a parameter intrinsic to the device and cannot be externally adjusted.

National's linearity test (a) and the "best straight line" test (b) used by other suppliers are illustrated below. The "best straight line" requires a special zero and FS adjustment for each part, which is almost impossible for the user to determine. The "end point test" uses a standard zero and FS adjustment procedure and is a much more stringent test for DAC linearity.

Power Supply Sensitivity: Power supply sensitivity is a measure of the effect of power supply changes on the DAC full-scale output (which is the worst case).



a. End Point Test After Zero and FS Adj.



b. Best Straight Line

Power Supply Sensitivity: Power supply sensitivity is a measure of the effect of power supply changes on the DAC full-scale output (which is the worst case).

Settling Time: Settling time is the time required from a code transition until the DAC output reaches within ±½ LSB of the final output value. Full-scale settling time requires a zero to full-scale or full-scale to zero output change.

Full-Scale Error: Full scale error is a measure of the output error between an ideal DAC and the actual device output. Ideally, for the DAC1000 series, full-scale is $V_{REF} - 1$ LSB. For $V_{REF} = -10V$ and unipolar operation, $V_{FULL\text{-}SCALE} = 10.0000V - 9.8mV = 9.9902V$. Full-scale error is adjustable to zero.

Monotonicity: If the output of a DAC increases for increasing digital input code, then the DAC is monotonic. A 10-bit DAC with 10-bit monotonicity will produce an increasing analog output when all 10 digital inputs are exercised. A 10-bit DAC with 9-bit monotonicity will be monotonic when only the most significant 9 bits are exercised. Similarly, 8-bit monotonicity is guaranteed when only the most significant 8 bits are exercised.

2.0 Double Buffering

These DACs are double-buffered, microprocessor compatible versions of the DAC1020 10-bit multiplying DAC. The addition of the buffers for the digital input data not only allows for storage of this data, but also provides a way to assemble the 10-bit input data word from two write cycles when using an 8-bit data bus. Thus, the next data update for the DAC output can be made with the complete new set of 10-bit data. Further, the double buffering allows many DACs in a system to store current data and also the next data. The updating of the new data for each DAC is also not time critical. When all DACs are updated, a common strobe signal can then be used to cause all DACs to switch to their new analog output levels.

3.0 T^2L Compatible Logic Inputs

To guarantee T^2L voltage compatibility of the logic inputs, a novel bipolar (NPN) regulator circuit is used. This makes the input logic thresholds equal to the forward drop of two diodes (and also matches the temperature variation) as occurs naturally in T^2L. The basic circuit is shown in Figure 1. A curve of digital input threshold as a function of power supply voltage is shown in the Typical Performance Characteristics section.

4.0 Application Hints

The DC stability of the V_{REF} source is the most important factor to maintain accuracy of the DAC over time and temperature changes. A good single point ground for the analog signals is next in importance.

These MICRO-DAC™ converters are CMOS products and reasonable care should be exercised in handling them prior to final mounting on a PC board. The digital inputs are protected, but permanent damage may occur if the part is subjected to high electrostatic fields. Store unused parts in conductive foam or anti-static rails.

4.1 Power Supply Sequencing & Decoupling

Some IC amplifiers draw excessive current from the Analog inputs to V− when the supplies are first turned on. To prevent damage to the DAC — an external Schottky diode connected from I_{OUT1} or I_{OUT2} to ground may be required to prevent destructive currents in I_{OUT1} or I_{OUT2}. If an LM741 or LF356 is used — these diodes are not required.

The standard power supply decoupling capacitors which are used for the op amp are adequate for the DAC.

4.2 Op Amp Bias Current & Input Leads

The op amp bias current (I_B) CAN CAUSE DC ERRORS. BI-FET™ op amps have very low bias current, and there-

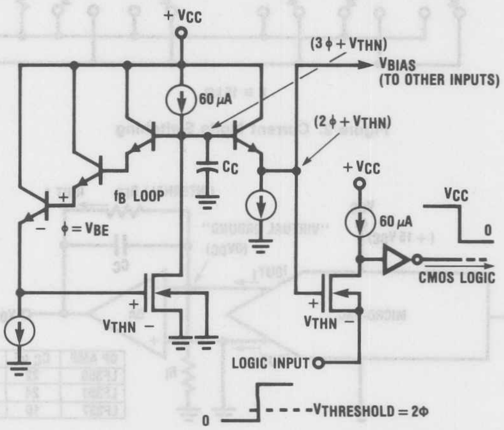


Figure 1. Basic Logic Threshold Loop

The distance from the I_{OUT1} pin of the DAC to the inverting input of the op amp should be kept as short as possible to prevent inadvertent noise pickup.

5.0 Analog Applications

The analog section of these DACs uses an R-2R ladder which can be operated both in the current switching mode and in the voltage switching mode.

The major product changes (compared with the DAC1020) have been made in the digital functioning of the DAC. The analog functioning is reviewed here for completeness. For additional analog applications, such as multipliers, attenuators, digitally controlled amplifiers and low frequency sine wave oscillators, refer to the DAC1020 data sheet. Some basic circuit ideas are presented in this section in addition to complete applications circuits.

5.1 Operation in Current Switching Mode

The analog circuitry, Figure 2, consists of a silicon-chromium (Si-Cr) thin film R-2R ladder which is deposited on the surface oxide of the monolithic chip. As a result, there is no parasitic diode connected to the V_{REF} pin as would exist if diffused resistors were used. The reference voltage input (V_{REF}) can therefore range from −10V to +10V.

The digital input code to the DAC simply controls the position of the SPDT current switches, SW0 to SW9. A logical 1 digital input causes the current switch to steer small voltage drop across them and can therefore switch currents of either polarity. This is the basis for the 4-quadrant multiplying feature of this DAC.

5.1.1 Providing a Unipolar Output Voltage with the DAC in the Current Switching Mode

A voltage output is provided by making use of an external op amp as a current-to-voltage converter. The idea is to use the internal feedback resistor, R_{FB}, from the output of the op amp to the inverting (−) input. Now, when current is entered at this inverting input, the feedback action of the op amp keeps that input at ground potential. This causes the applied input current to be diverted to the feedback resistor. The output voltage of the op amp is forced to a voltage given by:

$$V_{OUT} = -(I_{OUT1} \times R_{FB})$$

Notice that the sign of the output voltage depends on the direction of current flow through the feedback resistor.

In current switching mode applications, both current output pins (I_{OUT1} and I_{OUT2}) should be operated at $0\,V_{DC}$. This is accomplished as shown in Figure 3. The capacitor, C_C, is used to compensate for the output capacitance of the DAC and the input capacitance of the op amp. The required feedback resistor, R_{FB}, is available on the chip (one end is internally tied to I_{OUT1}) and must be used since an external resistor will not provide the needed matching and temperature tracking. This circuit can therefore be simplified as shown in

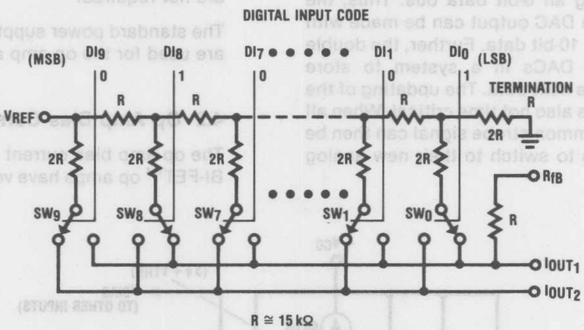
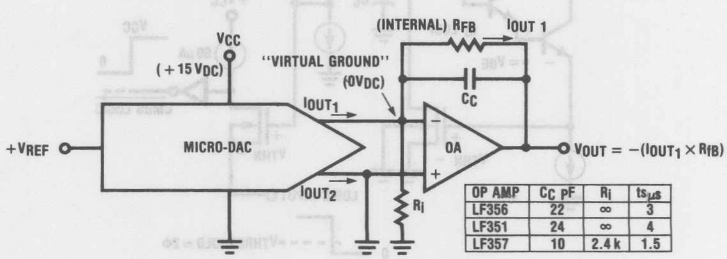


Figure 2. Current Mode Switching



OP AMP	C_C pF	R_i	$t_{s\mu s}$
LF356	22	∞	3
LF351	24	∞	4
LF357	10	2.4 k	1.5

Figure 3. Converting I_{OUT} to V_{OUT}

Figure 4, where the sign of the reference voltage has been changed to provide a positive output voltage. Note that the output current, I_{OUT1}, now flows through the R_{FB} pin.

5.1.2 Providing a Bipolar Output Voltage with the DAC in the Current Switching Mode

The addition of a second op amp to the circuit of Figure 4 can be used to generate a bipolar output voltage from a fixed reference voltage (Figure 5). This, in effect, gives sign significance to the MSB of the digital input word to allow two quadrant multiplication of the reference voltage. The polarity of the reference can also be reversed to realize the full four-quadrant multiplication.

The applied digital word is offset binary which includes a code to output zero volts without the need of a large valued resistor common to existing bipolar multiplying DAC circuits. Offset binary code can be derived from 2's complement data (most common for signed processor arithmetic) by inverting the state of the MSB in either software or hardware. After doing this the output then responds in accordance to the following expression:

$$V_O = V_{REF} \times \frac{D}{512}$$

where V_{REF} can be positive or negative and D is the signed decimal equivalent of the 2's complement processor data. ($-512 \leqslant D \leqslant +511$ or $1000000000 \leqslant D \leqslant 0111111111$). If the applied digital input is interpreted as the decimal equivalent of a true binary word, V_{OUT} can be found by:

$$V_O = V_{REF}\left(\frac{D-512}{512}\right) \qquad 0 \leqslant D \leqslant 1023$$

With this configuration, only the offset voltage of amplifier 1 need be nulled to preserve linearity of the DAC. The offset voltage error of the second op amp has no effect on linearity. It presents a constant output voltage error and should be nulled only if absolute accuracy is needed. Another advantage of this configuration is that the values of the external resistors required do not have to match the value of the internal DAC resistors; they need only to match and temperature track each other.

A thin film 4 resistor network available from Beckman Instruments, Inc. (part no. 694-3-R10K-D) is ideally suited for this application. Two of the four available 10kΩ resistor can be paralleled to form R in Figure 5 and the other two can be used separately as the resistors labeled 2R.

Operation is summarized in the table below:

2's Comp. (Decimal)	2's Comp. (Binary)	Applied Digital Input	Applied True Binary (Decimal)	V_{OUT} $+V_{REF}$	V_{OUT} $-V_{REF}$
+511	0111111111	1111111111	1023	V_{REF} − 1 LSB	$-\lvert V_{REF}\rvert$ + 1 LSB
+256	0100000000	1100000000	768	$V_{REF}/2$	$-\lvert V_{REF}\rvert/2$
0	0000000000	1000000000	512	0	0
−1	1111111111	0111111111	511	−1 LSB	+1 LSB
−256	1100000000	0100000000	256	$-V_{REF}/2$	$+\lvert V_{REF}\rvert/2$
−512	1000000000	0000000000	0	$-V_{REF}$	$+\lvert V_{REF}\rvert$

with: $1\ LSB = \frac{\lvert V_{REF}\rvert}{512}$

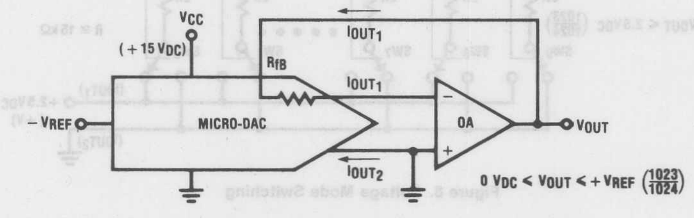


Figure 4. Providing a Unipolar Output Voltage

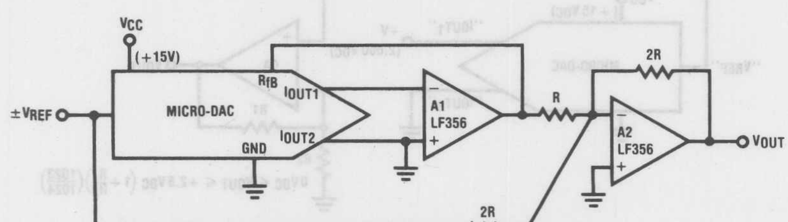


Figure 5. Providing a Bipolar Output Voltage with the DAC in the Current Switching Mode

5.2 Analog Operation in the Voltage Switching Mode

Some useful application circuits result if the R-2R ladder is operated in the voltage switching mode. There are two very important things to remember when using the DAC in the voltage mode. The reference voltage (+V) must always be positive since there are parasitic diodes to ground on the I_{OUT1} pin which would turn on if the reference voltage went negative. To maintain a degradation of linearity less than ±0.005%, keep $+V \leq 3V_{DC}$ and V_{CC} at least 10V more positive than +V. Figures 6 and 7 show these errors for the voltage switching mode. This operation appears unusual, since a reference voltage (+V) is applied to the I_{OUT1} pin and the voltage output is the V_{REF} pin. This basic idea is shown in Figure 8.

This V_{OUT} range can be scaled by use of a non-inverting gain stage as shown in Figure 9.

Notice that this is unipolar operation since all voltages are positive. A bipolar output voltage can be obtained by using a single op amp as shown in Figure 10. For a digital input code of all zeros, the output voltage from the V_{REF} pin is zero volts. The external op amp now has a single input of +V and is operating with a gain of −1 to this input. The output of the op amp therefore will be at −V for a digital input of all zeros. As the digital code increases, the output voltage at the V_{REF} pin increases. Notice that the gain of the op amp to voltages which are applied to the (+) input is +2 and the gain to voltages which are applied to the input resistor, R, is −1. The output voltage of the op amp depends on both of these inputs and is given by:

$$V_{OUT} = (+V)(-1) + V_{REF}(+2)$$

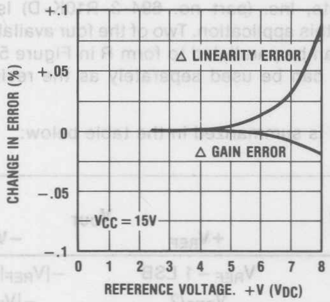


Figure 6.

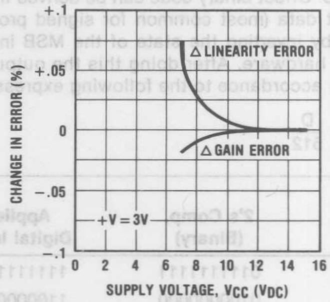


Figure 7.

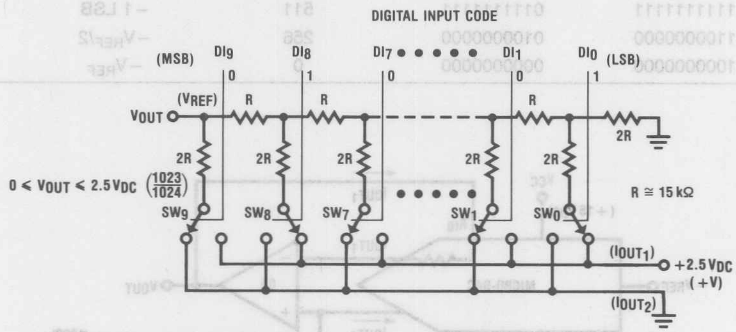


Figure 8. Voltage Mode Switching

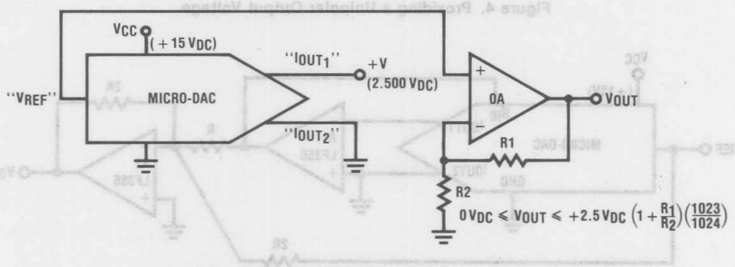


Figure 9. Amplifying the Voltage Mode Output (Single Supply Operation)

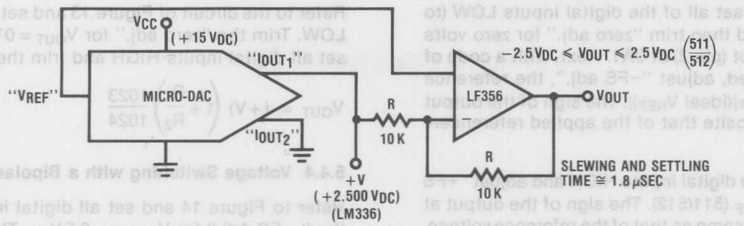


Figure 10. Providing a Bipolar Output Voltage with a Single Op Amp

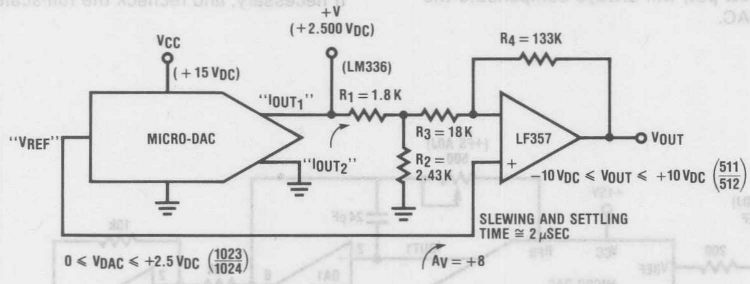


Figure 11. Increasing the Output Voltage Swing

The output voltage swing can be expanded by adding 2 resistors to Figure 10 as shown in Figure 11. These added resistors are used to attenuate the +V voltage. The overall gain, $A_V(-)$, from the +V terminal to the output of the op amp determines the most negative output voltage, $-4(+V)$ (when the V_{REF} voltage at the + input of the op amp is zero) with the component values shown. The complete dynamic range of V_{OUT} is provided by the gain from the (+) input of the op amp. As the voltage at the V_{REF} pin ranges from 0V to +V (1023/1024) the output of the op amp will range from $-10\,V_{DC}$ to +10V (1023/1024) when using a +V voltage of $+2.500\,V_{DC}$. The $2.5\,V_{DC}$ reference voltage can be easily developed by using the LM336 zener which can be biased through the R_{FB} internal resistor, connected to V_{CC}.

5.3 Op Amp V_{OS} Adjust (Zero Adjust) for Current Switching Mode

Proper operation of the ladder requires that all of the 2R legs always go to exactly $0\,V_{DC}$ (ground). Therefore offset voltage, V_{OS}, of the external op amp cannot be tolerated as every millivolt of V_{OS} will introduce 0.01% of added linearity error. At first this seems unusually sensitive, until it becomes clear the 1mV is 0.01% of the 10V reference! High resolution converters of high accuracy require attention to every detail in an application to achieve the available performance which is inherent in the part. To prevent this source of error, the V_{OS} of the op amp has to be initially zeroed. This is the "zero adjust" of the DAC calibration sequence and should be done first.

If the V_{OS} is to be adjusted there are a few points to consider. Note that no "dc balancing" resistance should be used in the grounded positive input lead of the op amp. This resistance and the input current of the op amp can also create errors. The low input biasing current of the BI-FET™ op amps makes them ideal for use in DAC current to voltage applications. The V_{OS} of the op amp should be adjusted with a digital input of all zeros to force $I_{OUT} = 0\,mA$. A 1KΩ resistor can be temporarily connected from the inverting input to ground to provide a dc gain of approximately 15 to the V_{OS} of the op amp and make the zeroing easier to sense.

5.4 Full-Scale Adjust

The full-scale adjust procedure depends on the application circuit and whether the DAC is operated in the current switching mode or in the voltage switching mode. Techniques are given below for all of the possible application circuits.

5.4.1 Current Switching with Unipolar Output Voltage

After doing a "zero adjust," set all of the digital input levels HIGH and adjust the magnitude of V_{REF} for

$$V_{OUT} = -(\text{ideal } V_{REF})\ \frac{1023}{1024}$$

This completes the DAC calibration.

at the inverting input (pin 2) of 0A1. Next, with a code of all zeros still applied, adjust "−FS adj.", the reference voltage, for $V_{OUT} = \pm|(\text{ideal } V_{REF})|$. The sign of the output voltage will be opposite that of the applied reference.

Finally, set all of the digital inputs HIGH and adjust "+FS adj." for $V_{OUT} = V_{REF}$ (511/512). The sign of the output at this time will be the same as that of the reference voltage. The addition of the 200Ω resistor in series with the V_{REF} pin of the DAC is to force the circuit gain error from the DAC to be negative. This insures that adding resistance to R_{fb}, with the 500Ω pot, will always compensate the gain error of the DAC.

set all digital inputs HIGH and trim the "FS Adj." for:

$$V_{OUT} = (+V)\left(1 + \frac{R_1}{R_2}\right)\frac{1023}{1024}$$

5.4.4 Voltage Switching with a Bipolar Output Voltage

Refer to Figure 14 and set all digital inputs LOW. Trim the "− FS Adj." for $V_{OUT} = -2.5\,V_{DC}$. Then set all digital inputs HIGH and trim the "+ FS Adj." for $V_{OUT} = +2.5$ $(511/512)V_{DC}$. Test the zero by setting the MS digital input HIGH and all the rest LOW. Adjust V_{OS} of amp #3, if necessary, and recheck the full-scale values.

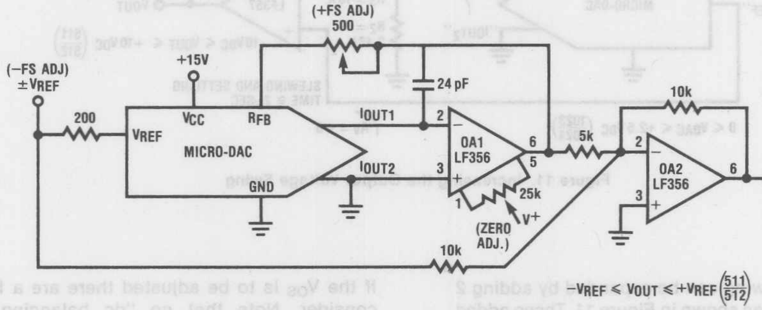


Figure 12. Full Scale Adjust — Current Switching with Bipolar Output Voltage

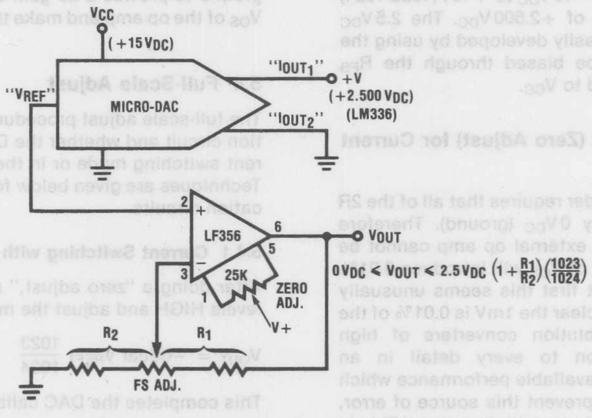


Figure 13. Full Scale Adjust — Unipolar Output Voltage

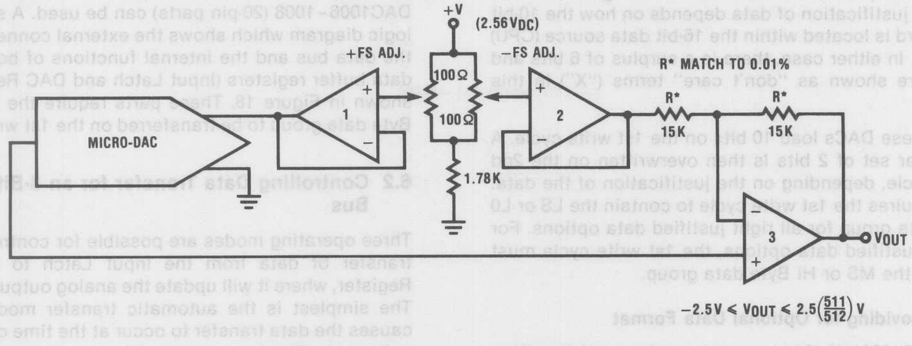


Figure 14. Voltage Switching with a Bipolar Output Voltage

6.0 Digital Control Description

The DAC1000 series of products can be used in a wide variety of operating modes. Most of the options are shown in Table I. Also shown in this table are the section numbers of this data sheet where each of the operating modes is discussed. For example, if your main interest is interfacing to a μP with an 8-bit data bus you will be directed to Section 6.1.0.

The first consideration is "will the DAC be interfaced to a μP with an 8-bit or a 16-bit data bus or used in the stand-alone mode?" For the 8-bit data bus, a second selection is made on how the 2nd digital data buffer (the DAC Latch) is updated by a transfer from the 1st digital data buffer (the Input Latch). Three options are provided: 1) an automatic transfer when the 2nd data byte is written to the DAC, 2) a transfer which is under the control of the μP and can include more than one DAC in a simultaneous transfer, or 3) a transfer which is under the control of external logic. Further, the data format can be either left justified or right justified.

When interfacing to a μP with a 16-bit data bus only two selections are available: 1) operating the DAC with a single digital data buffer (the transfer of one DAC does not have to be synchronized with any other DACs in the system), or 2) operating with a double digital data buffer for simultaneous transfer, or updating, of more than one DAC.

For operating without a μP in the stand alone mode, three options are provided: 1) using only a single digital data buffer, 2) using both digital data buffers — "double buffered," or 3) allowing the input digital data to "flow through" to provide the analog output without the use of any data latches.

To reduce the required reading, only the applicable sections of 6.1 through 6.4 need be considered.

6.1 Interfacing to an 8-Bit Data Bus

Transferring 10 bits of data over an 8-bit bus requires two write cycles and provides four possible combinations which depend upon two basic data format and protocol decisions:

1. Is the data to be left justified (considered as fractional binary data with the binary point to the left) or right justified (considered as binary weighted data with the binary point to the right)?
2. Which byte will be transferred first, the most significant byte (MS byte) or the least significant byte (LS byte)?

Table 1.

Operating Mode / Data Bus	Automatic Transfer			μP Control Transfer			External Transfer		
	Section	Figure No. (24-Pin)	(20-Pin)	Section	Figure No. (24-Pin)	(20-Pin)	Section	Figure No. (24-Pin)	(20-Pin)
8-Bit Data Bus (6.1.0)									
Right Justified (6.1.1)	6.2.1	16		6.2.2	16		6.2.3	16	
Left Justified (6.1.2)	6.2.1	17	18	6.2.2	17	18	6.2.3	17	18
16-Bit Data Bus (6.3.0)	Single Buffered			Double Buffered			Flow Through		
	6.3.1	19	20	6.3.2	19	20	Not Applicable		
Stand Alone (6.4.0)	Single Buffered			Double Buffered			Flow Through		
	6.4.1	19	20	6.4.2	19	20	6.4.3	19	NA

These data possibilities are shown in Figure 15. Note that the justification of data depends on how the 10-bit data word is located within the 16-bit data source (CPU) register. In either case, there is a surplus of 6 bits and these are shown as "don't care" terms ("X") in this figure.

All of these DACs load 10 bits on the 1st write cycle. A particular set of 2 bits is then overwritten on the 2nd write cycle, depending on the justification of the data. This requires the 1st write cycle to contain the LS or L0 Byte data group for all right justified data options. For all left justified data options, the 1st write cycle must contain the MS or Hi Byte data group.

6.1.1 Providing for Optional Data Format

The DAC1000/1/2 (24-pin parts) can be used for either data formatting by tying the LJ/$\overline{RJ}$ pin either high or low, respectively. A simplified logic diagram which shows the external connections to the data bus and the internal functions of both of the data buffer registers (Input Latch and DAC Register) is shown in Figure 16 for the right justified data operation. Figure 17 is for left justified data.

6.1.2 For Left Justified Data

For applications which require left justified data, DAC1006-1008 (20-pin parts) can be used. A simplified logic diagram which shows the external connections to the data bus and the internal functions of both of the data buffer registers (Input Latch and DAC Register) is shown in Figure 18. These parts require the MS or Hi Byte data group to be transferred on the 1st write cycle.

6.2 Controlling Data Transfer for an 8-Bit Data Bus

Three operating modes are possible for controlling the transfer of data from the Input Latch to the DAC Register, where it will update the analog output voltage. The simplest is the automatic transfer mode, which causes the data transfer to occur at the time of the 2nd write cycle. This is recommended when the exact timing of the changes of the DAC analog output are not critical. This typically happens where each DAC is operating individually in a system and the analog updating of one DAC is not required to be synchronized to any other DAC. For synchronized DAC updating, two options are provided: μP control via a common $\overline{XFER}$ strobe or external update timing control via an external strobe. The details of these options are now shown.

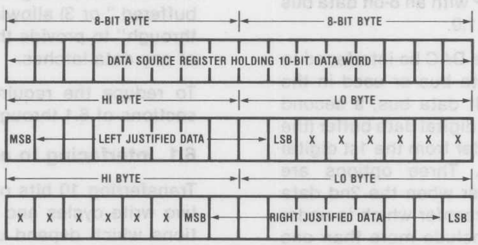


Figure 15. Fitting a 10-Bit Data Word into 16 Available Bit Locations

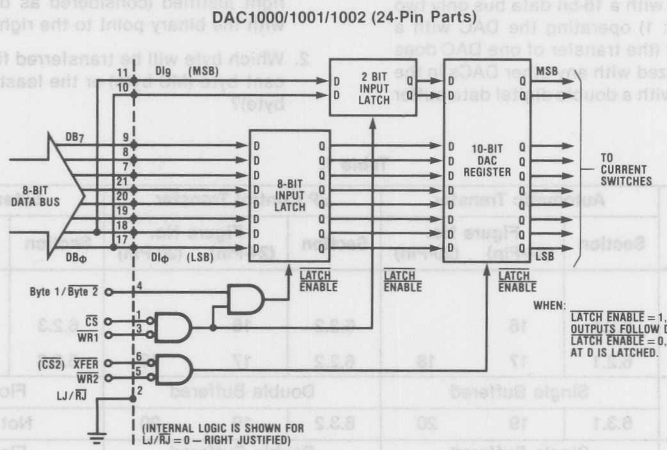


Figure 16. Input Connections and Controls for DAC1000-1002 Right Justified Data Option

DAC1000/1001/1002 (24-Pin Parts)

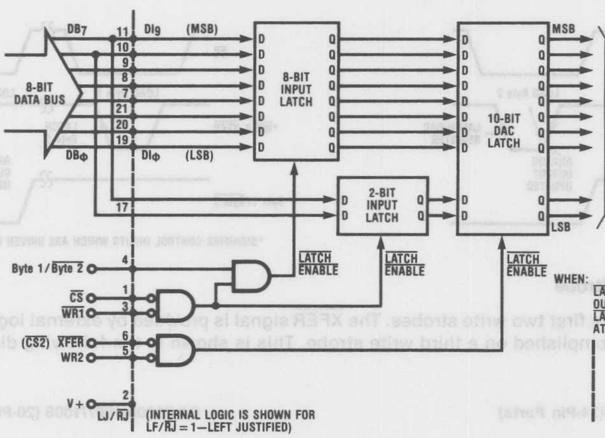


Figure 17. Input Connections and Controls for DAC1000-1002 Left Justified Data Option

DAC1006/1007/1008 (20-Pin Parts for Left Justified Data)

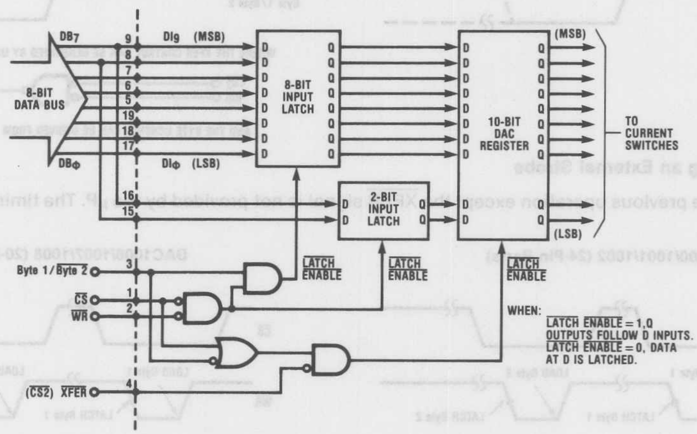
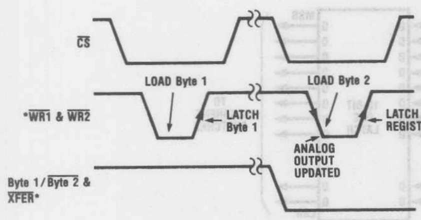


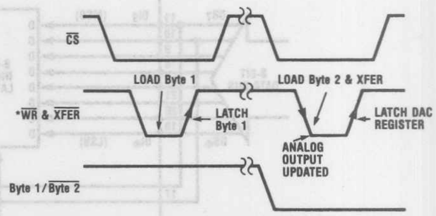
Figure 18. Input Connections and Controls for DAC1006/1007/1008 Left Justified Data

complete 10-bit word from the input latch to the DAC register. This is shown in the following timing diagrams; the point in time where the analog output is updated is also indicated on these diagrams.

DAC1000/1001/1002 (24-Pin Parts)



DAC1006/1007/1008 (20-Pin Parts)

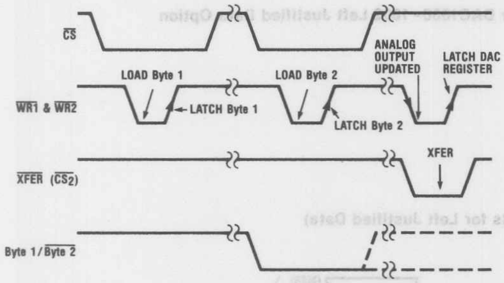


*SIGNIFIES CONTROL INPUTS WHICH ARE DRIVEN IN PARALLEL

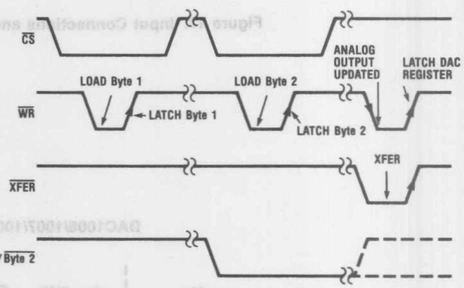
6.2.2 Transfer Using μP Write Strobe

The input latch is loaded with the first two write strobes. The XFER signal is provided by external logic, as shown below, to cause the transfer to be accomplished on a third write strobe. This is shown in the following diagrams:

DAC1000/1001/1002 (24-Pin Parts)



DAC1006/1007/1008 (20-Pin Parts)



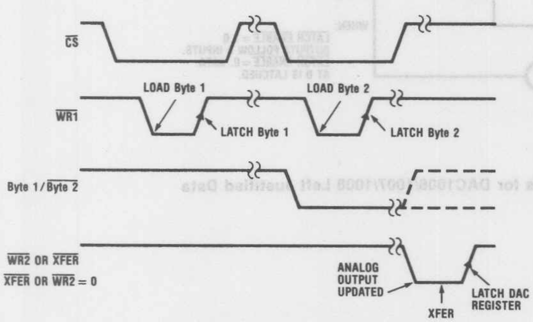
WHERE THE XFER CONTROL CAN BE GENERATED BY USING A SECOND CHIP SELECT AS:

AND THE BYTE CONTROL CAN BE DERIVED FROM THE ADDRESS BUS SIGNALS.

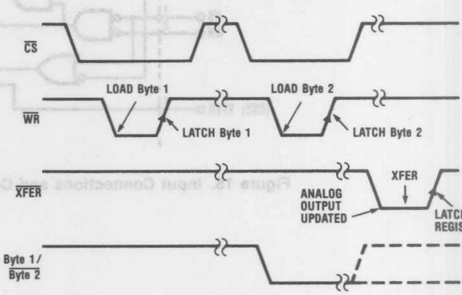
6.2.3 Transfer Using an External Strobe

This is similar to the previous operation except the XFER signal is not provided by the μP. The timing diagram for this is:

DAC1000/1001/1002 (24-Pin Parts)



DAC1006/1007/1008 (20-Pin Parts)



6.3 Interfacing to a 16-Bit Data Bus

The interface to a 16-bit data bus is easily handled by connecting to 10 of the available bus lines. This allows a wiring selected right justified or left justified data format. This is shown in the connection diagrams of Figures 19 and 20, where the use of DB6 to DB15 gives left justified data operation. Note that any part number can be used and the Byte1/Byte2 control should be wired Hi.

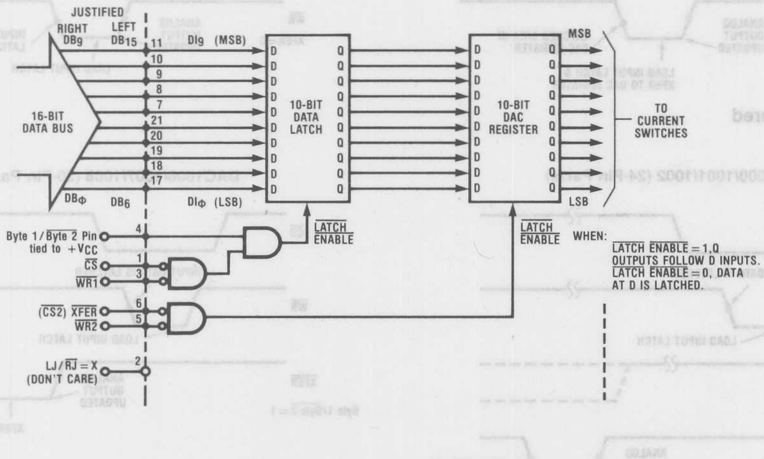


Figure 19. Input Connections and Logic for DAC1000-1002 with 16-Bit Data Bus

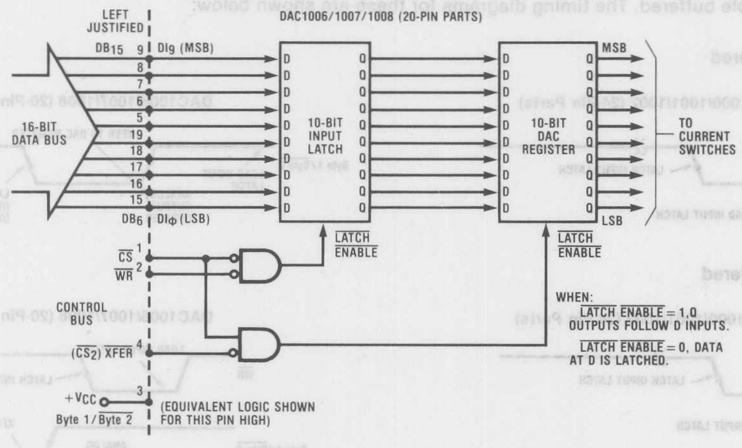
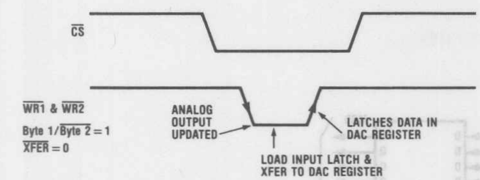


Figure 20. Input Connections and Logic for DAC1006/1007/1008 with 16-Bit Data Bus

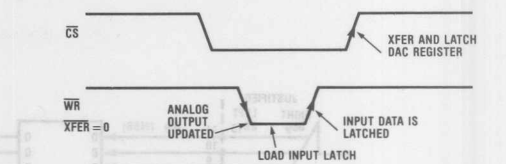
Three operating modes are possible: flow through, single buffered, or double buffered. The timing diagrams for these are shown below:

6.3.1 Single Buffered

DAC1000/1001/1002 (24-Pin Parts)

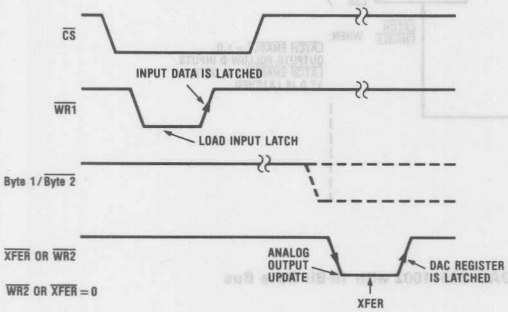


DAC1006/1007/1008 (20-Pin Parts)

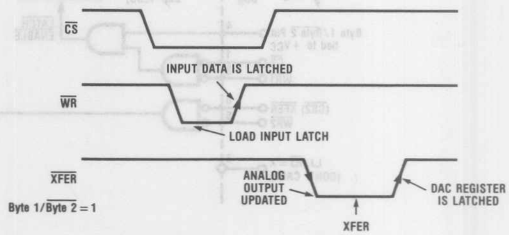


6.3.2 Double Buffered

DAC1000/1001/1002 (24-Pin Parts)



DAC1006/1007/1008 (20-Pin Parts)

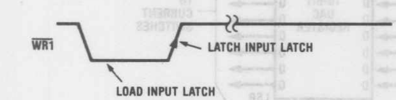


6.4 Stand Alone Operation

For applications for a DAC which are not under μP control (stand alone) there are two basic operating modes, single buffered and double buffered. The timing diagrams for these are shown below:

6.4.1 Single Buffered

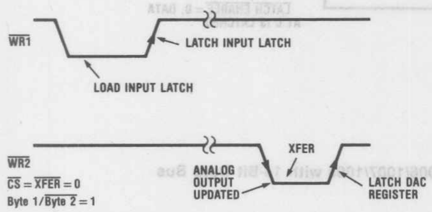
DAC1000/1001/1002 (24-Pin Parts)



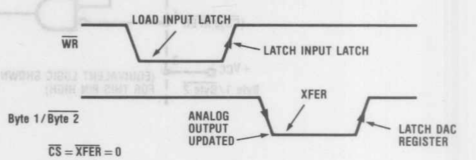
DAC1006/1007/1008 (20-Pin Parts)*

6.4.2 Double Buffered

DAC1000/1001/1002 (24-Pin Parts)



DAC1006/1007/1008 (20-Pin Parts)*



*For a connection diagram of this operating mode use Figure 18 for the Logic and Figure 20 for the Data Input connections.

DAC1000/1001/1002 (24-Pin Parts)

$\overline{WR1} = \overline{WR2} = \overline{CS} = \overline{XFER} = 0$
Byte 1/$\overline{\text{Byte 2}} = 1$

7.0 Microprocessor Interface

The logic functions of the DAC1000 family have been oriented towards an ease of interface with all popular μPs. The following sections discuss in detail a few useful interface schemes.

7.1 DAC1000/1/2 to INS8080A Interface

Figure 21 illustrates the simplicity of interfacing the DAC1000 to an INS8080A based microprocessor system. The circuit will perform an automatic transfer of the 10 bits of output data from the CPU to the DAC register as outlined in Section 6.2.1, "Controlling Data Transfer for an 8-Bit Data Bus."

Since a double byte write is necessary to control the DAC with the INS8080A, a possible instruction to achieve this is a PUSH of a register pair onto a "stack" in memory. The 16-bit register pair word will contain the 10 bits of the eventual DAC input data in the proper

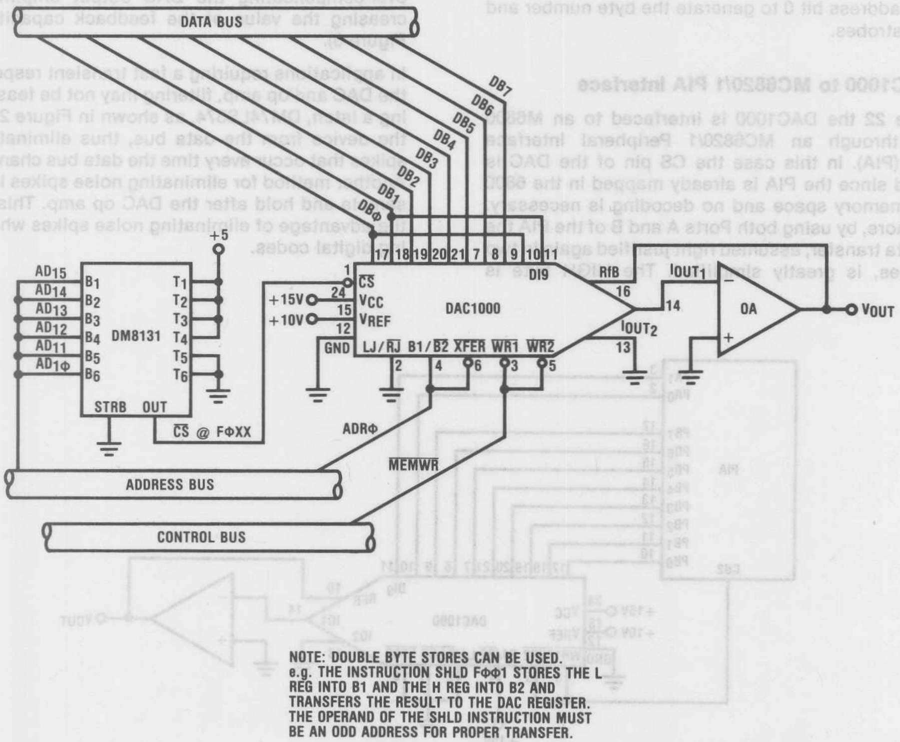


Figure 21. Interfacing the DAC1000 to the INS8080A CPU Group

output the higher order byte of the register pair (i.e., register B of the BC pair) first. The DAC will actually appear as a two-byte "stack" in memory to the CPU. The auto-decrementing of the stack pointer during a PUSH allows using address bit 0 of the stack pointer as the $\overline{\text{Byte1}}$/Byte2 and $\overline{\text{XFER}}$ strobes if bit 0 of the stack pointer address − 1, (SP − 1), is a "1" as presented to the DAC. Additional address decoding by the DM8131 will generate a unique DAC chip select (CS) and synchronize this CS to the two memory write strobes of the PUSH instruction.

To reset the stack pointer so new data may be output to the same DAC, a POP instruction followed by instructions to insure that proper data is in the DAC data register pair before it is "PUSHED" to the DAC should be executed, as the POP instruction will arbitrarily alter the contents of a register pair.

Another double byte write instruction is Store H and L Direct (SHLD), where the HL register pair would temporarily contain the DAC data and the two sequential addresses for the DAC are specified by the instruction op code. The auto incrementing of the DAC address by the SHLD instruction permits the same simple scheme of using address bit 0 to generate the byte number and transfer strobes.

7.2 DAC1000 to MC6820/1 PIA Interface

In Figure 22 the DAC1000 is interfaced to an M6800 system through an MC6820/1 Peripheral Interface Adapter (PIA). In this case the CS pin of the DAC is grounded since the PIA is already mapped in the 6800 system memory space and no decoding is necessary. Furthermore, by using both Ports A and B of the PIA the 10-bit data transfer, assumed right justified again in two 8-bit bytes, is greatly simplified. The HIGH byte is occur simultaneously upon CB2 going LOW under program control. The 10-bit data word in the DAC register will be latched (and hence V_{OUT} will be fixed) when CB2 is brought back HIGH.

If both output ports of the PIA are not available, it is possible to interface the DAC1000 through a single port without much effort. However, additional logic at the CB2 (or CA2) lines or access to some of the 6800 system control lines will be required.

7.3 Noise Considerations

A typical digital/microprocessor bus environment is a tremendous potential source of high frequency noise which can be coupled to sensitive analog circuitry. The fast edges of the data and address bus signals generate frequency components of 10's of megahertz and can cause noise spikes to appear at the DAC output. These noise spikes occur when the data bus changes state or when data is transferred between the latches of the device.

In low frequency or DC applications, low pass filtering can reduce these noise spikes. This is accomplished by over-compensating the DAC output amplifier by increasing the value of the feedback capacitor (C_C in Figure 3).

In applications requiring a fast transient response from the DAC and op amp, filtering may not be feasible. Adding a latch, DM74LS374, as shown in Figure 23 isolates the device from the data bus, thus eliminating noise spikes that occur every time the data bus changes state. Another method for eliminating noise spikes is to add a sample and hold after the DAC op amp. This also has the advantage of eliminating noise spikes when changing digital codes.

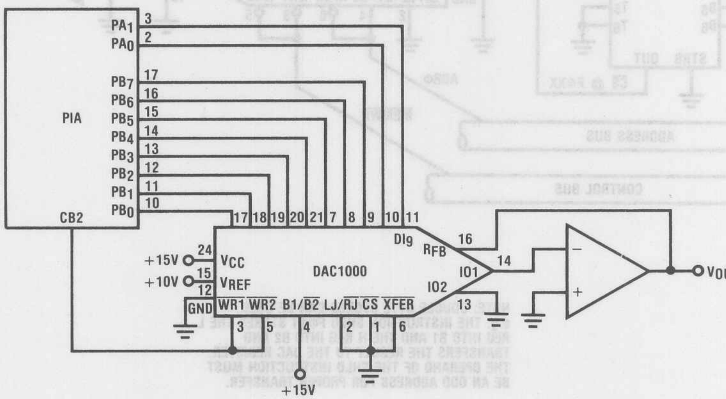


Figure 22. DAC1000 to MC6820/1 PIA Interface

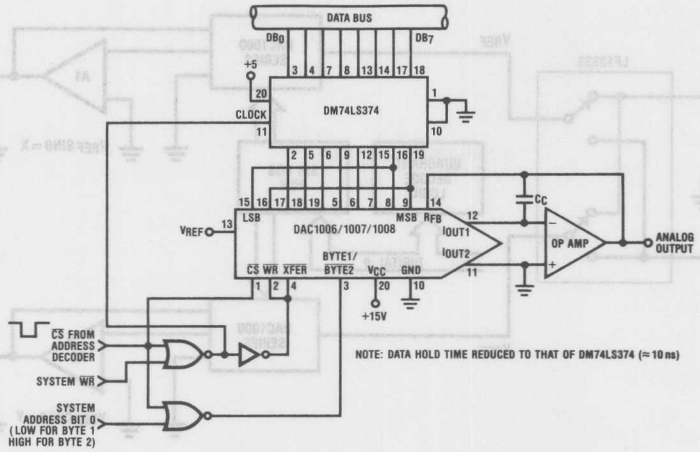


Figure 23. Isolating Data Bus from DAC Circuitry to Eliminate Digital Noise Coupling

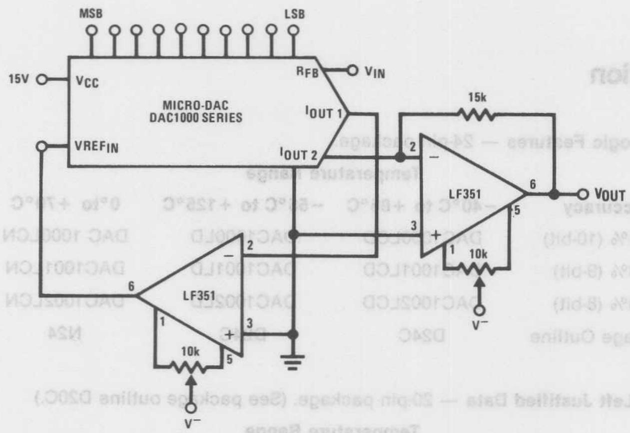


Figure 24. Digitally Controlled Amplifier/Attenuator

7.4 Digitally Controlled Amplifier/Attenuator

An unusual application of the DAC, Figure 24, applies the input voltage via the on-chip feedback resistor. The lower op amp automatically adjusts the $V_{REF\ IN}$ voltage such that I_{OUT1} is equal to the input current (V_{IN}/Rf_B). The magnitude of this $V_{REF\ IN}$ voltage depends on the digital word which is in the DAC register. I_{OUT2} then depends upon both the magnitude of V_{IN} and the digital word. The second op amp converts I_{OUT2} to a voltage, V_{OUT}, which is given by:

$$V_{OUT} = V_{IN}\left(\frac{1023 - N}{N}\right), \text{ where } 0 < N \leqslant 1023.$$

Note that $N = 0$ (or a digital code of all zeros) is not allowed or this will cause the output amplifier to saturate at either $\pm V_{MAX}$, depending on the sign of V_{IN}.

To provide a digitally controlled divider, the output op amp can be eliminated. Ground the I_{OUT2} pin of the DAC and V_{OUT} is now taken from the lower op amp (which also drives the V_{REF} input of the DAC). The expression for V_{OUT} is now given by

$$V_{OUT} = -\frac{V_{IN}}{M}$$ where M = Digital input (expressed as a fractional binary number).
$0 < M < 1$.

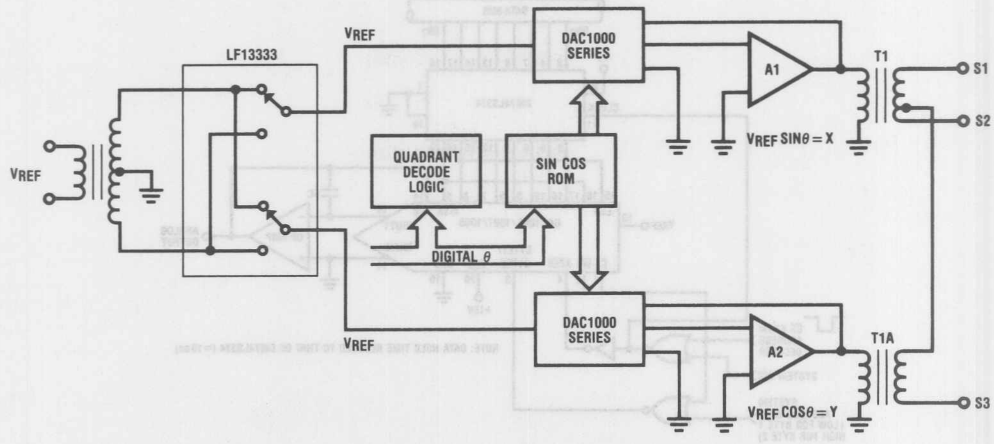


Figure 25. Digital to Synchro Converter

Ordering Information

1. **All Logic Features** — 24-pin package.

	Temperature Range		
Accuracy	**−40°C to +85°C**	**−55°C to +125°C**	**0°to +70°C**
0.05% (10-bit)	DAC1000LCD	DAC1000LD	DAC 1000LCN
0.10% (9-bit)	DAC1001LCD	DAC1001LD	DAC1001LCN
0.20% (8-bit)	DAC1002LCD	DAC1002LD	DAC1002LCN
Package Outline	D24C	D24C	N24

2. **For Left Justified Data** — 20-pin package. (See package outline D20C.)

	Temperature Range		
Accuracy	**−40°C to +85°C**	**−55°C to +125°C**	**0°to +70°C**
0.05% (10-bit)	DAC1006LCD	DAC1006LD	DAC1006LCN
0.10% (9-bit)	DAC1007LCD	DAC1007LD	DAC1007LCN
0.20% (8-bit)	DAC1008LCD	DAC1008LD	DAC1008LCN
Package Outline	D20C	D20C	N20

National Semiconductor

DAC1020, DAC1021, DAC1022 10-Bit Binary Multiplying D/A Converter DAC1220, DAC1221, DAC1222 12-Bit Binary Multiplying D/A Converter

General Description

The DAC1020 and the DAC1220 are, respectively, 10 and 12-bit binary multiplying digital-to-analog converters. A deposited thin film R-2R resistor ladder divides the reference current and provides the circuit with excellent temperature tracking characteristics (0.0002%/°C linearity error temperature coefficient maximum). The circuit uses CMOS current switches and drive circuitry to achieve low power consumption (30 mW max) and low output leakages (200 nA max). The digital inputs are compatible with DTL/TTL logic levels as well as full CMOS logic level swings. This part, combined with an external amplifier and voltage reference, can be used as a standard D/A converter; however, it is also very attractive for multiplying applications (such as digitally controlled gain blocks) since its linearity error is essentially independent of the voltage reference. All inputs are protected from damage due to static discharge by diode clamps to V^+ and ground.

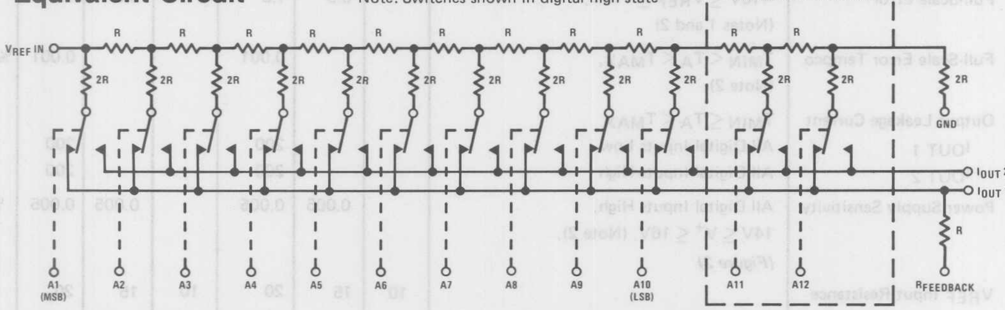
This part is available with 10-bit (0.05%), 9-bit (0.10%), and 8-bit (0.20%) non-linearity guaranteed over temperature (note 1 of electrical characteristics). The DAC1020, DAC1021 and DAC1022 are direct replacements for the 10-bit resolution AD7520 and AD7530 and equivalent to the AD7533 family. The DAC1220, DAC1221 and DAC1222 are direct replacements for the 12-bit resolution AD7521 and AD7531 family.

Features

- Linearity specified with zero and full-scale adjust only
- Non-linearity guaranteed over temperature
- Integrated thin film on CMOS structure
- 10-bit or 12-bit resolution
- Low power dissipation 10 mW @15V typ
- Accepts variable or fixed reference $-25V \le V_{REF} \le 25V$
- 4-quadrant multiplying capability
- Interfaces directly with DTL, TTL and CMOS
- Fast settling time—500 ns typ
- Low feedthrough error—1/2 LSB @ 100 kHz typ

Equivalent Circuit

Note. Switches shown in digital high state



Ordering Information

10-BIT D/A CONVERTERS

TEMPERATURE RANGE		0°C to 70°C		-40°C to +85°C		-55°C to +125°C	
ACCURACY	0.05%	DAC1020LCN	AD7520LN AD7530LN	DAC1020LCD	AD7520LD AD7530LD	DAC1020LD	AD7520UD
	0.10%	DAC1021LCN	AD7520KN AD7530KN	DAC1021LCD	AD7520KD AD7530KD	DAC1021LD	AD7520TD
	0.20%	DAC1022LCN	AD7520JN AD7530JN	DAC1022LCD	AD7520JD AD7530JD	DAC1022LD	AD7520SD
PACKAGE OUTLINE		N16A		D16C		D16C	

12-BIT D/A CONVERTERS

TEMPERATURE RANGE		0°C to 70°C		-40°C to +85°C		-55°C to +125°C	
ACCURACY	0.05%	DAC1220LCN	AD7521LN AD7531LN	DAC1220LCD	AD7521LD AD7531LD	DAC1220LD	AD7521UD
	0.10%	DAC1221LCN	AD7521KN AD7531KN	DAC1221LCD	AD7521KD AD7531KD	DAC1221LD	AD7521TD
	0.20%	DAC1222LCN	AD7521JN AD7531JN	DAC1222LCD	AD7521JD AD7531JD	DAC1222LD	AD7521SD
PACKAGE OUTLINE		N18A		D18A		D18A	

Note. Devices may be ordered by either part number.

V^+ to Gnd	17V
V_{REF} to Gnd	±25V
Digital Input Voltage Range	V^+ to Gnd
DC Voltage at Pin 1 or Pin 2 (Note 3)	−100 mV to V^+
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Temperature (T_A)			
DAC1020LD, DAC1021LD,	−55	+125	°C
DAC1022LD, DAC1220LD,	−55	+125	°C
DAC1221LD, DAC1222LD	−55	+125	°C
DAC1020LCD, DAC1021LCD,	−40	+85	°C
DAC1022LCD, DAC1220LCD,	−40	+85	°C
DAC1221LCD, DAC1222LCD	−40	+85	°C
DAC1020LCN, DAC1021LCN	0	+70	°C
DAC1022LCN, DAC1220LCN	0	+70	°C
DAC1221LCN, DAC1222LCN	0	+70	°C

Electrical Characteristics

(V^+ = 15V, V_{REF} = 10.000V, T_A = 25°C unless otherwise specified)

PARAMETER	CONDITIONS	DAC1020, DAC1021, DAC1022			DAC1220, DAC1221, DAC1222			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Resolution		10			12			Bits
Linearity Error	$T_{MIN} < T_A < T_{MAX}$, $-10V < V_{REF} < +10V$, (Note 1) End Point Adjustment Only (See Linearity Error in Definition of Terms)							
10-Bit Parts	DAC1020, DAC1220			0.05			0.05	% FSR
9-Bit Parts	DAC1021, DAC1221			0.10			0.10	% FSR
8-Bit Parts	DAC1022, DAC1222			0.20			0.20	% FSR
Linearity Error Tempco	$-10V \le V_{REF} \le +10V$, (Notes 1 and 2)			0.0002			0.0002	% FS/°C
Full-Scale Error	$-10V \le V_{REF} \le +10V$, (Notes 1 and 2)		0.3	1.0		0.3	1.0	% FS
Full-Scale Error Tempco	$T_{MIN} < T_A < T_{MAX}$, (Note 2)			0.001			0.001	% FS/°C
Output Leakage Current	$T_{MIN} \le T_A \le T_{MAX}$							
$I_{OUT\ 1}$	All Digital Inputs Low			200			200	nA
$I_{OUT\ 2}$	All Digital Inputs High			200			200	nA
Power Supply Sensitivity	All Digital Inputs High, $14V \le V^+ \le 16V$, (Note 2), *(Figure 2)*		0.005	0.005		0.005	0.005	% FS/V
V_{REF} Input Resistance		10	15	20	10	15	20	kΩ
Full-Scale Current Settling Time	R_L = 100Ω from 0 to 99.95% FS							
	All Digital Inputs Switched Simultaneously		500			500		ns
V_{REF} Feedthrough	All Digital Inputs Low, V_{REF} = 20 Vp-p @ 100 kHz			10			10	mVp-p
	D Package (Note 4)		6	9		6	9	mVp-p
	N Package		2	5		2	5	mVp-p
Output Capacitance								
$I_{OUT\ 1}$	All Digital Inputs Low		40			40		pF
	All Digital Inputs High		200			200		pF
$I_{OUT\ 2}$	All Digital Inputs Low		200			200		pF
	All Digital Inputs High		40			40		pF
Digital Input	*(Figure 1)*							
Low Threshold	$T_{MIN} < T_A < T_{MAX}$			0.8			0.8	V
High Threshold	$T_{MIN} < T_A < T_{MAX}$	2.4			2.4			V

PARAMETER	CONDITIONS	DAC1020, DAC1021 DAC1022			DAC1220, DAC1221 DAC1222			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Digital Input Current	$T_{MIN} \leq T_A \leq T_{MAX}$							
	Digital Input High		1	100		1	100	μA
	Digital Input Low		−50	−200		−50	−200	μA
Supply Current	All Digital Inputs High		0.2	1.6		0.2	1.6	mA
	All Digital Inputs Low		0.6	2		0.6	2	mA
Operating Power Supply Range	*(Figures 1 and 2)*	5		15	5		15	V

Note 1: V_{REF} = ±10V and V_{REF} = ±1V. A linearity error temperature coefficient of 0.0002% FS for a 45°C rise only guarantees 0.009% maximum change in linearity error. For instance, if the linearity error at 25°C is 0.045% FS it could increase to 0.054% at 70°C and the DAC will be no longer a 10-bit part. Note, however, that the linearity error is specified over the device full temperature range which is a more stringent specification since *it includes* the linearity error temperature coefficient.

Note 2: Using internal feedback resistor as shown in *Figure 3*.

Note 3: Both $I_{OUT\,1}$ and $I_{OUT\,2}$ must go to ground or the virtual ground of an operational amplifier. If V_{REF} = 10V, every millivolt offset between $I_{OUT\,1}$ or $I_{OUT\,2}$, 0.005% linearity error will be introduced.

Note 4: To achieve this low feedthrough in the D package, the user must ground the metal lid.

Typical Performance Characteristics

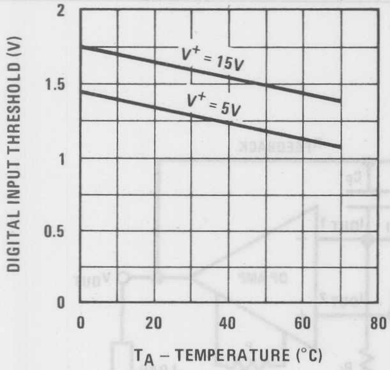


FIGURE 1. Digital Input Threshold vs Ambient Temperature

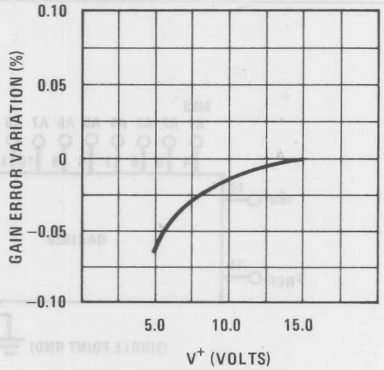


FIGURE 2. Gain Error Variation vs V^+

Typical Applications

The following applications are also valid for 12-bit systems using the DAC1220 and 2 additional digital inputs.

Operational Amplifier Bias Current *(Figure 3)*

The op amp bias current, I_b, flows through the 15k internal feedback resistor. BI-FET op amps have low I_b and, therefore, the 15k x I_b error they introduce is negligible; they are strongly recommended for the DAC1020 applications.

V_{OS} Considerations

The output impedance, R_{OUT}, of the DAC is modulated by the digital input code which causes a modulation of the operational amplifier output offset. It therefore recommended to adjust the op amp V_{OS}. R_{OUT} is ~15k if more than 4 digital inputs are high; R_{OUT} is ~45k if a single digital input is high, and R_{OUT} approaches infinity if all inputs are low.

Operational Amplifier V_{OS} Adjust *(Figure 3)*

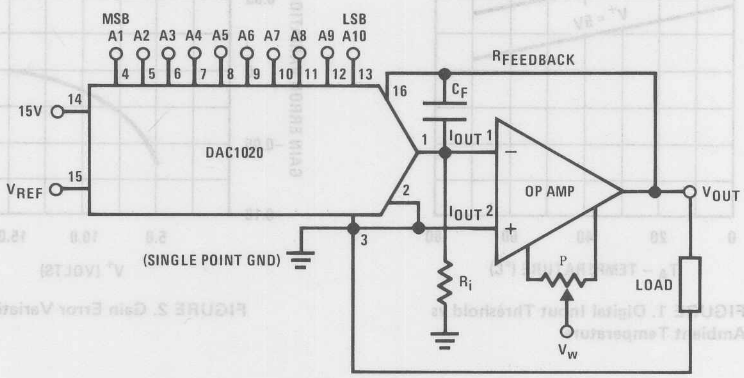
Connect all digital inputs, A1–A10, to ground and adjust the potentiometer to bring the op amp V_{OUT} pin to within ±1 mV from ground potential. If V_{REF} is less than 10V, a finer V_{OS} adjustment is required. It is helpful to increase the resolution of the V_{OS} adjust procedure by connecting a 1 kΩ resistor between the inverting input of the op amp to ground. After V_{OS} has been adjusted, remove the 1 kΩ.

Full-Scale Adjust *(Figure 4)*

Switch high all the digital inputs, A1–A10, and measure the op amp output voltage. Use a 500Ω potentiometer, as shown, to bring $||V_{OUT}||$ to a voltage equal to V_{REF} x 1023/1024.

SELECTING AND COMPENSATING THE OPERATIONAL AMPLIFIER

OP AMP FAMILY	C_F	R_i	P	V_w	CIRCUIT SETTLING TIME, t_s	CIRCUIT SMALL SIGNAL BW
LM357	10 pF	2.4k	25k	V^+	1.5 µs	1M
LM356	22 pF	∞	25k	V^+	3 µs	0.5M
LF351	24 pF	∞	10k	V^-	4 µs	0.5M
LM741	0	∞	10k	V^-	40 µs	200 kHz



$$V_{OUT} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \ldots \frac{A10}{1024}\right)$$

$$-10V \leq V_{REF} \leq 10V$$

$$0 \leq V_{OUT} \leq -\frac{1023}{1024} V_{REF}$$

where $A_N = 1$ if the A_N digital input is high
$A_N = 0$ if the A_N digital input is low

FIGURE 3. Basic Connection: Unipolar or 2-Quadrant Multiplying Configuration (Digital Attenuator)

Typical Applications (Continued)

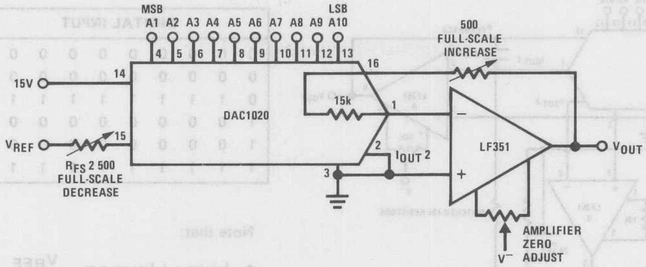


FIGURE 4: Full-Scale Adjust

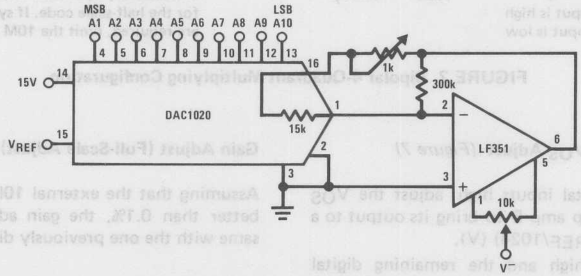
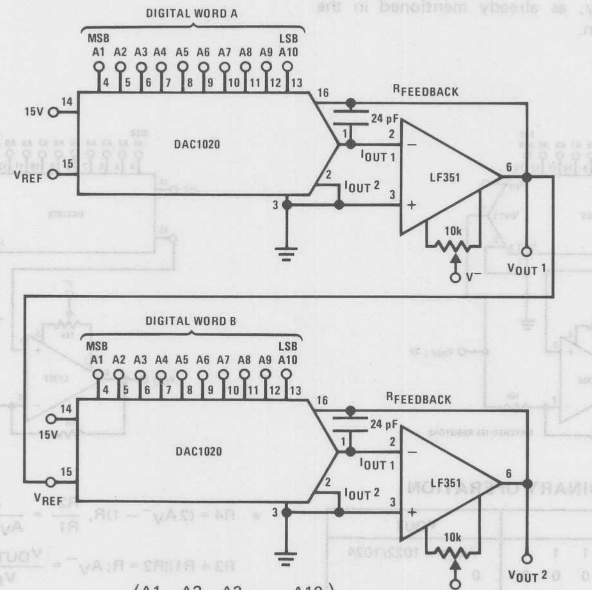


FIGURE 5. Alternate Full-Scale Adjust: (Allows Increasing or Decreasing the Gain)



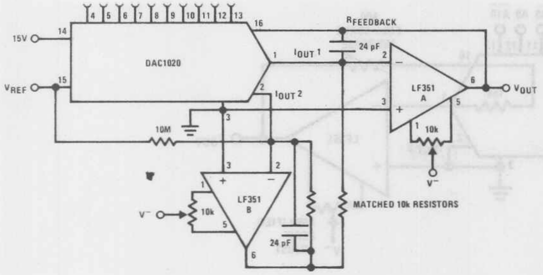
$$V_{OUT1} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \ldots \frac{A10}{1024}\right)$$

$$V_{OUT2} = V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \ldots \frac{A10}{1024}\right) \times \left(\frac{B1}{2} + \frac{B2}{4} + \frac{B3}{8} + \ldots \frac{B10}{1024}\right)$$

where V_{REF} can be an AC signal

FIGURE 6. Precision Analog-to-Digital Multiplier

8



DIGITAL INPUT										VOUT
0	0	0	0	0	0	0	0	0	0	$+V_{REF}$
0	0	0	0	0	0	0	0	0	1	$V_{REF} \times 1022/1024$
0	1	1	1	1	1	1	1	1	1	$V_{REF} \times 2/1024$
1	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	1	$-V_{REF} \times 2/1024$
1	1	1	1	1	1	1	1	1	1	$-V_{REF}$ (1022/1024)

Note that:

- $I_{OUT\,1} + I_{OUT\,2} = \dfrac{V_{REF}}{R_{LADDER}} \times \left(\dfrac{1023}{1024}\right)$
- By doubling the output range we get half the resolution
- The 10M resistor, adds a 1 LSB "thump", to allow full offset binary operation where the output reaches zero for the half-scale code. If symmetrical output excursions are required, omit the 10M resistor.

$$V_{OUT} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \ldots + \frac{A10}{1024} - \frac{1}{1024}\right)$$

where: AN = +1 if A_N input is high
AN = −1 if A_N input is low

FIGURE 7. Bipolar 4-Quadrant Multiplying Configuration

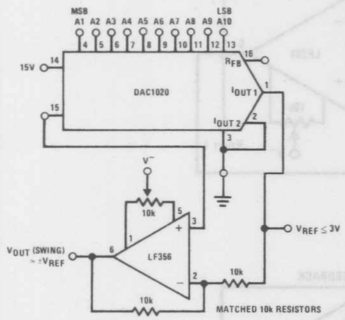
Operational Amplifiers V_{OS} Adjust *(Figure 7)*

a) Switch all the digital inputs high; adjust the V_{OS} potentiometer of op amp B to bring its output to a value equal to $-(V_{REF}/1024)$ (V).

b) Switch the MSB high and the remaining digital inputs low. Adjust the V_{OS} potentiometer of op amp A, to bring its output value to within a 1 mV from ground potential. For $V_{REF} < 10V$, a finer adjust is necessary, as already mentioned in the previous application.

Gain Adjust (Full-Scale Adjust)

Assuming that the external 10k resistors are matched to better than 0.1%, the gain adjust of the circuit is the same with the one previously discussed.

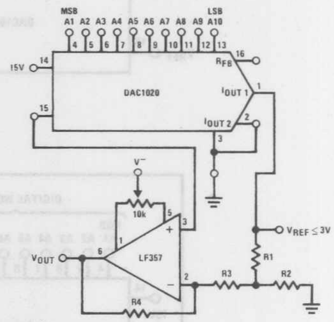


TRUE OFFSET BINARY OPERATION

DIGITAL INPUT										VOUT
1	1	1	1	1	1	1	1	1	1	$V_{REF} \times 1022/1024$
1	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	$-V_{REF}$

$t_s = 1.8\ \mu s$
use LM336 for a voltage reference

FIGURE 8. Bipolar Configuration with a Single Op Amp

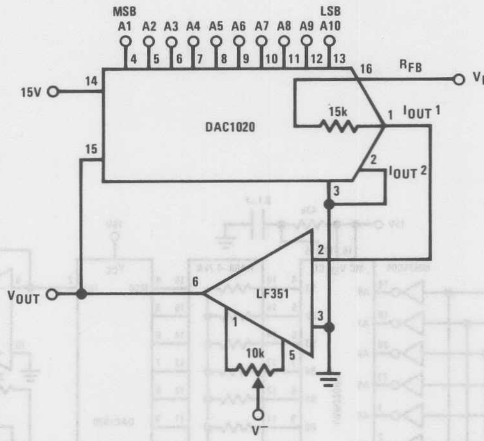


- $R4 = (2\,A_V^- - 1)R, \quad \dfrac{R2}{R1} = \dfrac{A_V^-}{A_V^- - 1}$

  $R3 + R1\|R2 = R;\ A_V^- = \dfrac{V_{OUT(PEAK)}}{V_{REF}}$, R = 20k
- Example: $V_{REF} = 2V$, V_{OUT} (swing) ≃ ±10V: $A_V^- = 5V$
  Then R4 = 9R, R1 = 0.8 R2. If R1 = 0.2R then R2 = 0.25R, R3 = 0.64R

FIGURE 9. Bipolar Configuration with Increased Output Swing

Typical Applications (Continued)

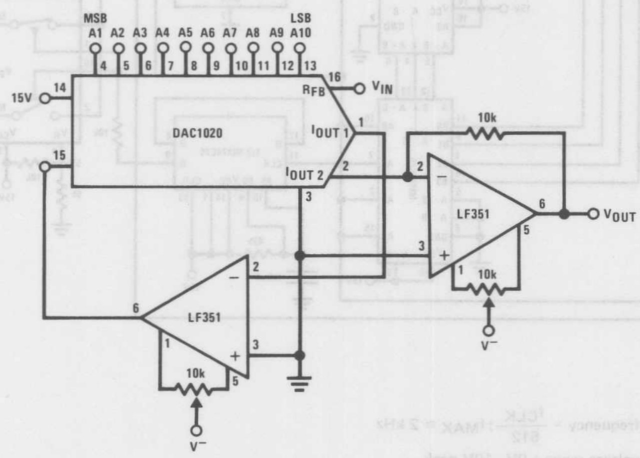


$$V_{OUT} = \frac{-V_{REF}}{\left(\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\dots\frac{A10}{1024}\right)}$$

where: V_{REF} can be an AC signal

- By connecting the DAC in the feedback loop of an operational amplifier a linear digitally control gain block can be realized
- Note that with all digital inputs low, the gain of the amplifier is infinity, that is, the op amp will saturate. In other words, we cannot divide the V_{REF} by zero!

FIGURE 10. Analog-to-Digital Divider (or Digitally Gain Controlled Amplifier)



$$V_{OUT} = V_{REF}\left[\frac{\frac{\overline{A1}}{2}+\frac{\overline{A2}}{4}+\dots+\frac{A10}{1024}}{\frac{A1}{2}+\frac{A2}{4}+\dots+\frac{\overline{A10}}{1024}}\right] \text{ or } V_{OUT} = V_{REF}\left(\frac{1023-N}{N}\right)$$

where: $0 \le N \le 1023$

$N = 0$ for A_N = all zeros

$N = 1$ for $A10 = 1$, $A1-A9 = 0$

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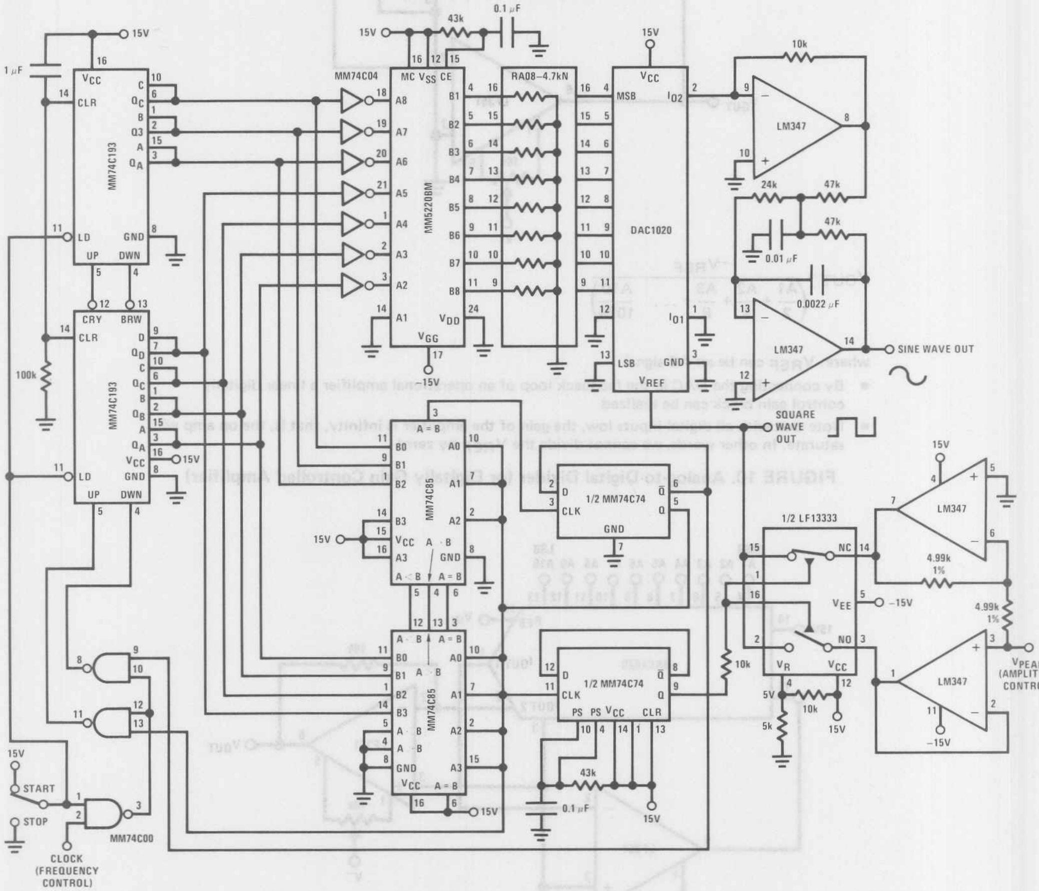
$N = 1023$ for A_N = all 1's

FIGURE 11. Digitally Controlled Amplifier-Attenuator

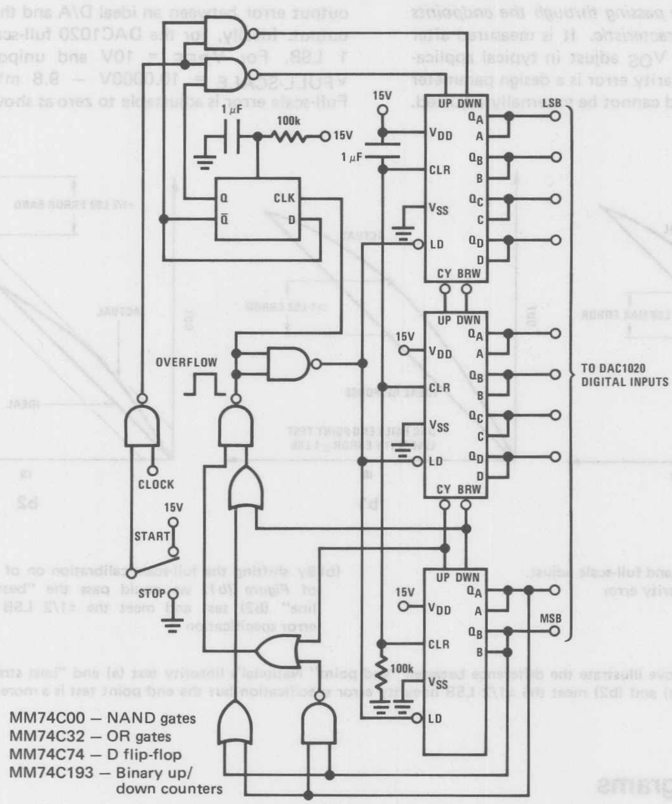
Typical Applications (Continued)



- Output frequency = $\frac{f_{CLK}}{512}$; $f_{MAX} \cong 2$ kHz
- Output voltage range = 0V–10V peak
- THD < 0.2%
- Excellent amplitude and frequency stability with temperature
- Low pass filter shown has a 1 kHz corner (for output frequencies below 10 Hz, filter corner should be reduced)
- Any periodic function can be implemented by modifying the contents of the look up table ROM
- No start up problems

FIGURE 12. Precision Low Frequency Sine Wave Oscillator Using Sine Look-Up ROM

Typical Applications (Continued)



MM74C00 — NAND gates
MM74C32 — OR gates
MM74C74 — D flip-flop
MM74C193 — Binary up/down counters

- Binary up/down counter digitally "ramps" the DAC output
- Can stop counting at any desired 10-bit input code
- Senses up or down count overflow and automatically reverses direction of count

FIGURE 13. A Useful Digital Input Code Generator for DAC Attenuator or Amplifier Circuits

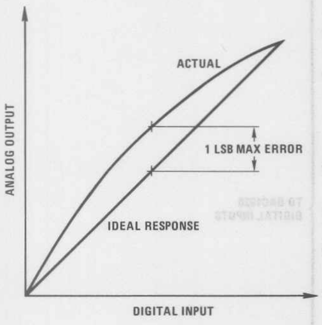
Resolution: Resolution is defined as the reciprocal of the number of discrete steps in the D/A output. It is directly related to the number of switches or bits within the D/A. For example, the DAC1020 has 2^{10} or 1024 steps while the DAC1220 has 2^{12} or 4096 steps. Therefore, the DAC1020 has 10-bit resolution, while the DAC1220 has 12-bit resolution.

Linearity Error: Linearity error is the maximum deviation from *a straight line passing through the endpoints of the D/A transfer characteristic.* It is measured after calibrating for zero (see V_{OS} adjust in typical applications) and full-scale. Linearity error is a design parameter intrinsic to the device and cannot be externally adjusted.

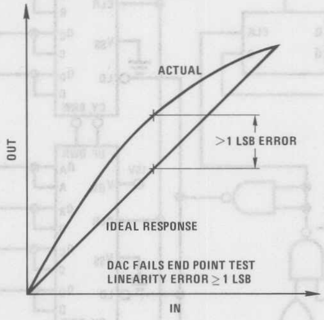
Power Supply Sensitivity: Power supply sensitivity is a measure of the effect of power supply changes on the D/A full-scale output.

Settling Time: Full-scale settling time requires a zero to full-scale or full-scale to zero output change. Settling time is the time required from a code transition until the D/A output reaches within ±1/2 LSB of final output value.

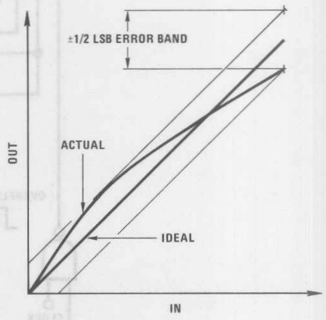
Full-Scale Error: Full-scale error is a measure of the output error between an ideal D/A and the actual device output. Ideally, for the DAC1020 full-scale is V_{REF} − 1 LSB. For V_{REF} = 10V and unipolar operation, $V_{FULL\text{-}SCALE}$ = 10.0000V − 9.8 mV = 9.9902V. Full-scale error is adjustable to zero as shown in *Figure 5*.



a



b1



b2

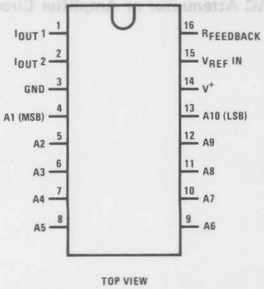
(a) End point test after zero and full-scale adjust. The DAC has 1 LSB linearity error

(b) By shifting the full-scale calibration on of the DAC of *Figure (b1)* we could pass the "best straight line" (b2) test and meet the ±1/2 LSB linearity error specification

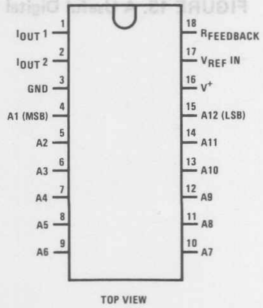
Note. (a), (b1) and (b2) above illustrate the difference between "end point" National's linearity test (a) and "best straight line" test. Note that both devices in (a) and (b2) meet the ±1/2 LSB linearity error specification but the end point test is a more "real life" way of characterizing the DAC.

Connection Diagrams

DAC102X
Dual-In-Line Package



DAC122X
Dual-In-Line Package



DAC1200, DAC1201 12-Bit Digital-to-Analog Converters

General Description

The DAC1200 series of D/A converters is a family of precision low-cost converter building blocks intended to fulfill a wide range of industrial and military D/A applications. These devices are complete functional blocks requiring only application of power for operation. The design combines a precision 12-bit weighted current source (12 current switches and 12-bit thin-film resistor network), a rapid-settling operational amplifier, and 10.24V buffered reference.

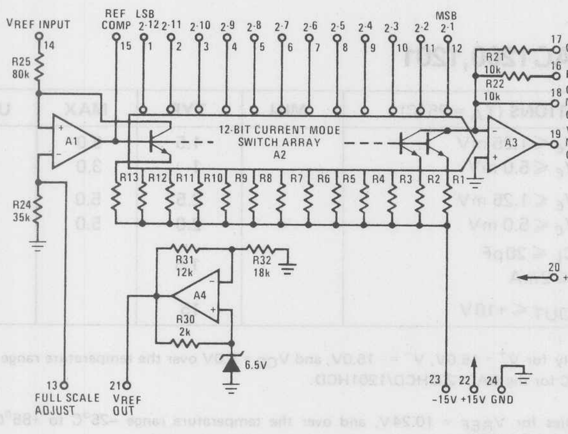
Input coding is complementary binary. In all instances, a logic "low" (⩽ 0.8V) turns a given bit ON, and a logic "high" (⩾ 2.0V) turns the bit OFF. Output format may be programmed for bipolar (±10V) or unipolar (0 to 10V) operation using internally supplied thin-film resistor pin strap options. Current mode operation is also available from 0 to 2 mA.

The entire series is available in hermetically sealed 24-lead DIP.

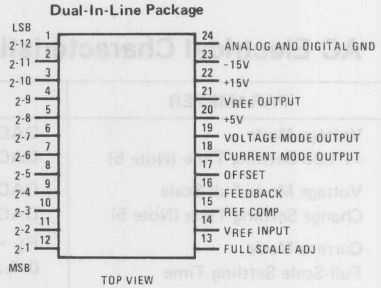
Features

- Circuit completely self-contained
- Both current and voltage-mode outputs
- Standard power supplies: ±15V and +5V
- Internal buffered reference: 10.24V
- 0 to 2 mA, ±10V or 0 to 10V output by strapping internal resistors; other scales by external resistors
- ±1/2 LSB linearity
- Fast settling time: 1.5 μs in current mode
  2.5 μs in voltage mode
- High slew rate: 15 V/μs
- TTL and CMOS compatible complementary binary input logic
- 12 bit linearity
- Standard 0.6" 24-pin DIP package

Block and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number DAC1200HD, DAC1200HCD, DAC1201HD or DAC1201HCD
See NS Package D24D

Absolute Maximum Ratings

Supply Voltage (V^+ & V^-)	±18V
Logic Supply Voltage (V_{CC})	+10V
Logic Input Voltage	−0.7V to +18V
Reference Input Voltage	−0V, +18V
Power Dissipation	(see graphs)
Short Circuit Duration (pins 18, 19 & 21)	Continuous
Operating Temperature Range	
DAC1200HD, DAC1201HD	−55°C to +125°C
DAC1200HCD, DAC1201HCD	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 sec.)	300°C

DC Electrical Characteristics DAC1200,1201 Binary D/A (Notes 1, 2)

PARAMETER	CONDITIONS	DAC1200/1200C			DAC1201/1201C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Resolution		12			12			Bits
Linearity Error (Note 3)	$T_A = 25°C$			±0.0122			±0.0488	% FS
				±0.0244			±0.0976	% FS
Offset Voltage	$T_A = 25°C$		1	5		1	10	mV
				10			15	mV
Voltage Mode Full-Scale Error (Note 3)	$V_{REF} = 10.240V$		0.01	0.1		0.02	0.2	% FS
Voltage Mode Full-Scale Error	Pin 21 connected to Pin 14, $T_A = 25°C$		0.1	0.6		0.1	0.7	% FS
Monotonicity (Notes 3, 4)		Guaranteed over the temperature range						
Voltage Mode Power Supply Sensitivity	$\Delta V^+ = \pm 2V$, $T_A = 25°C$, $V_{REF} = 10.240V$		0.002	0.02		0.002	0.02	% FS/V
	$\Delta V^- = \pm 2V$		0.002	0.02		0.002	0.02	% FS/V
	$\Delta V_{CC} = \pm 1V$		0.002	0.02		0.002	0.02	% FS/V
Output Voltage Range	$R_L = 5k$	±10.5	±12		±10.5	±12		V
Voltage Mode Output Short Circuit Current Limit	$T_A = 25°C$		20	50		20	50	mA
Current Mode Voltage Compliance	(Note 5)	±2.5			±2.5			V
Current Mode Output Impedance			15			15		kΩ
Reference Voltage	$0mA \leq I_{REF} \leq 2mA$, $T_A = 25°C$	10.190	10.240	10.290	10.190	10.240	10.290	V
Logic "1" Input Voltage (Bit OFF)		2.0			2.0			V
Logic "0" Input Voltage (Bit ON)				0.8			0.8	V
Logic "1" Input Current (Bit OFF)	$V_{IN} = 2.5V$		1	10		1	10	µA
Logic "0" Input Current (Bit ON)	$V_{IN} = 0V$		−10	−100		−10	−100	µA
Power Supply Current I^+	$V^+ = 15.0V$		10	15		10	15	mA
I^-	$V^- = -15.0V$, $T_A = 25$ C		25	30		25	30	mA
I_{CC}	$V_{CC} = 5.0V$		20	25		20	25	mA

AC Electrical Characteristics DAC1200,1201

PARAMETER	CONDITIONS ($T_A = 25°C$)	MIN	TYP	MAX	UNITS
Voltage Mode ±1 LSB Settling Time (Note 5)	DAC1200, $V_\epsilon \leq 1.25$ mV		1.5	3.0	µs
	DAC1201, $V_\epsilon \leq 5.0$ mV		1	3.0	µs
Voltage Mode Full-Scale Change Settling Time (Note 5)	DAC1200, $V_\epsilon \leq 1.25$ mV		2.5	5.0	µs
	DAC1201, $V_\epsilon \leq 5.0$ mV		2.0	5.0	µs
Current Mode Full-Scale Settling Time	$R_L = 1k\Omega$, $C_L \leq 20pF$, $0 \leq \Delta I_{OUT} \leq 2mA$		1.5		µs
Voltage Mode Slew Rate	$-10V \leq \Delta V_{OUT} \leq +10V$		15		V/µs

Note 1: Unless otherwise noted, these specifications apply for $V^+ = 15.0V$, $V^- = -15.0V$, and $V_{CC} = 5.0V$ over the temperature range −55°C to +125°C for the DAC1200HD/1201HD and −25°C to +85°C for the DAC1200HCD/1201HCD.

Note 2: All typical values are for $T_A = 25°C$.

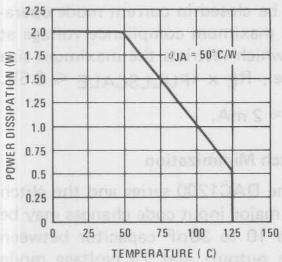
Note 3: Unless otherwise noted, this specification applies for $V_{REF} = 10.24V$, and over the temperature range −25°C to +85°C. Testing conditions include adjustment of offset to 0V and full-scale to 10.2375V.

Note 4: The DAC1200 is tested for monotonicity by stimulating all bits; the DAC1201 is tested for monotonicity by stimulating only the 10 MSBs and holding the 2 LSBs at 2.0V (i.e., 2 LSBs are OFF).

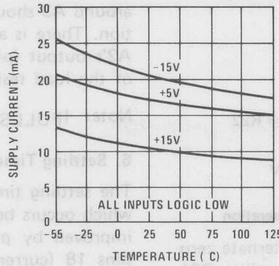
Note 5: Not tested — guaranteed by design.

Typical Performance Characteristics

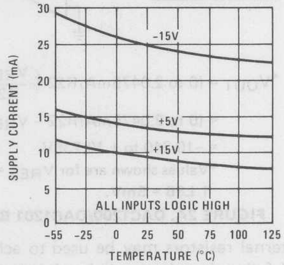
Maximum Power Dissipation

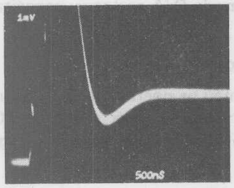


Supply Current vs Temperature

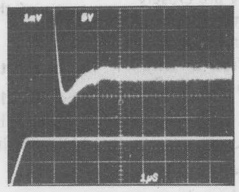


Supply Current vs Temperature

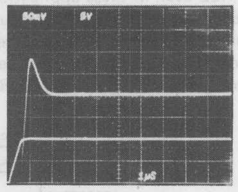




1 LSB Transition
1011 . . . 1 → 1100 . . . 0
V_O = 0, 10V
C_F = 30pF
T_A = 25°C



10V Full Scale Settling Time



10V Full Scale Pulse Response

Applications Information

1. Introduction

The DAC1200 series D/A converters are designed to minimize adjustments and user-supplied external components. For example, included in the package are a buffered reference, offset nulled output amplifier, and application resistors as well as the basic 12-bit current mode D/A.

However, the DAC1200 series is a sophisticated building block. **Its principles of operation and the following applications information should be read before applying power to the device.**

The user is referred to National Semiconductor Application Notes AN-156 and AN-157 for additional information.

2. Power Supply Selection & Decoupling

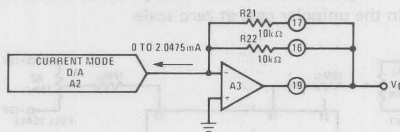
Selection of power supplies is important in applications requiring 0.01% accuracy. The ±15V supplies should be well regulated (±15V ± 0.1%) with less than 0.5mVrms of output noise and hum.

To realize the full speed capability of the device, all three power supply leads should be bypassed with 1μF tantalum electrolytic capacitors in shunt with 0.01μF ceramic disc capacitors no farther than ½ inch from the device package.

3. Unipolar and Bipolar Operation

The DAC1200 series D/A's may be configured for either unipolar or bipolar operation using resistors provided with the device. Figure 1A illustrates the proper connection for unipolar operation.

Bipolar operation is accomplished by offsetting the output amplifier A3 as shown in Figure 2A.



$$^{*}V_{OUT} = (I_{ZERO} \text{ to } I_{FULLSCALE})\left(\frac{R21 \cdot R22}{R21 + R22}\right)$$

$$= (0\text{mA to } 2.0475\text{mA})(5\text{k}\Omega)$$

$$= 0\text{V to } +10.2375\text{V}$$

*Values shown are for V_{REF} = 10.240V.

$$1 \text{ LSB Voltage Step} = \frac{10.240\text{V}}{4096} = 2.5\text{mV}.$$

$$1 \text{ LSB Current Step} = \frac{2.5\text{mV}}{5.0\text{k}\Omega} = 0.5\mu\text{A}$$

FIGURE 1A. DAC1200/DAC1201 Unipolar Operation

$$^{*}V_{OUT} = (0 \text{ to } 2.0475\text{mA})R22 - \frac{V_{REF}}{R22}R21$$

$$= (0 \text{ to } 2.0475\text{mA})R22 - V_{REF},\ R21 \equiv R22$$

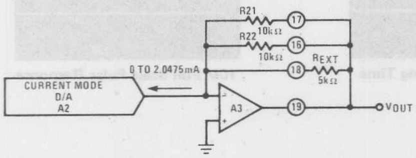
$$= -10.240 \text{ to } +10.235\text{V}$$

*Values shown are for $V_{REF} = 10.240\text{V}$

1 LSB = 5mV.

FIGURE 2A. DAC1200/DAC1201 Bipolar Operation

External resistors may be used to achieve alternate zero and full-scale voltages. It is advantageous to utilize R21 and R22 even in these applications since they are closely matched in TCR and temperature to the internal array. Figure 3 illustrates the recommended circuit for zero to 5V operation. R_{EXT} should be of metal film or wire-wound construction with a TCR of less than 10ppm/°C.



$$R_{TOTAL} = (R21) \parallel (R22) \parallel (R_{EXT}) = \frac{V_{FULLSCALE}}{2.0475\text{mA}} = 2.5\text{k}\Omega.$$

FIGURE 3. DAC1200 0 to 5.120V Operation

4. Offset and Full-Scale Adjust

If higher precision is required in the zero and full-scale, external adjustments may be made. The circuit of figure 4 illustrates the recommended circuit to adjust offset and full-scale of the DAC1200 series. The circuit will work equally well for unipolar or bipolar operation.

In bipolar operation, the offset is adjusted at minus full-scale; in the unipolar case at zero scale.

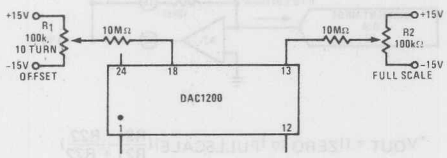


FIGURE 4. Offset & Full-Scale Adjust

For the values shown in figure 4, R1 will allow a ±7mV offset adjustment for the unipolar case and ±15mV for the bipolar case. R2 will allow a ±50mV adjustment of full scale.

around A3 should not be closed in current mode operation. There is a ±2.5V maximum compliance voltage at A2's output (pin 18) which restricts the maximum size of the load resistor; i.e., $R_L \times I_{FULLSCALE} \leqslant 2.5\text{V}$.

Note: $I_{FULLSCALE} \approx 2\text{ mA}$.

6. Settling Time & Glitch Minimization

The settling time of the DAC1200 series and the glitch which occurs between major input code changes may be improved by placing a 10 to 30pF capacitor between pins 18 (current-mode output) and 19 (voltage mode output). The capacitor is used to cancel output capacitance of the current mode D/A and stray capacitance at pin 18.

7. Current Output Boosting

The DAC1200 series may be operated as a "power D/A" by including a current buffer such as the LH0002 or LH0063 in the loop with A3 as shown in figure 5.

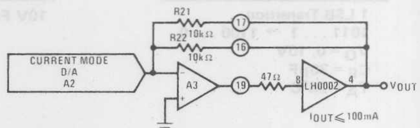


FIGURE 5. Current Boosted Output

8. Logic Input Coding

The sense of the logic inputs to the DAC1200 series is complementary; i.e., a given bit is turned ON by an active "low" input. Table I summarizes input status for the unipolar and bipolar complementary binary and BCD codes.

Other input codes may also be used. For example, the twos complement code, which is used extensively in computer and microprocessor applications, may be converted to the DAC1200 complementary bipolar format by inverting all bits except the MSB. The inversion may be accomplished in the microprocessor by software control, or by hardware using standard hex-inverters.

9. Reference Voltage

External reference voltages may be used with the DAC1200 series. Voltages other than 10.240 or 10.000V in the range of +5.0V to 11V will work satisfactorily for voltage mode operation. Full-scale voltage is always $V_{REF} - 1$ LSB where 1 LSB = $V_{REF}/4096$. Full-scale current may be predicted by:

$$I_{FULLSCALE} = (V_{REF})(0.19995117)\text{mA}$$

CODE TYPE	(Note 8) INPUT CODE MSB LSB	OUTPUT STATE	OUTPUT VOLTAGE V_{REF} = 10.240V	OUTPUT CURRENT
Unipolar Complementary Binary	0000 0000 0000	Full-Scale	+10.2375V	2.0475mA
	1111 1111 1110	1 LSB ON	+2.500mV	0.500μA
	1111 1111 1111	Zero Scale	Zero	Zero
Bipolar Complementary Binary	0000 0000 0000	Full-Scale	+10.235V	+1.0235mA
	0111 1111 1111	Half Full-Scale	-0.000V	0.000mA
	1111 1111 1110	1 LSB ON	-10.235V	-1.0235mA
	1111 1111 1111	Zero Scale	-10.240V	-1.0240mA

Note 8: Logic input sense is such that an active low ($V_{IN} \leq 0.8V$) turns a given bit ON and is represented as a logic "0" in the table.

Definition of Terms

Resolution

Resolution is defined as the reciprocal of the number of discrete steps in the D/A output (as designed). It is directly related to the number of switches or bits within the D/A. For example, the DAC1200 has 2^{12} or 4096 steps. Resolution may therefore be expressed variously as 12 bits, as 1 part in 2^{12}, as 1 part in 4096, or as a percentage (1/4096 x 100 = 0.0244%).

Linearity Error

Linearity error is the maximum deviation from a straight line passing through the endpoints of the D/A transfer characteristic. It is measured after calibrating for zero and full-scale. The linearity error of the DAC1200 series is guaranteed to be less than ±½ LSB or 0.0122% of F.S. for the DAC1200/1200C and ±0.0488% of F.S. for the DAC1201/DAC1201C. Linearity error is a design parameter intrinsic to the device and cannot be externally adjusted.

Offset Voltage

Offset voltage is an output voltage other than zero volts for unipolar operation (and other than minus full-scale for bipolar operation) with all bits turned OFF. In the DAC1200 series this error resides primarily in the output amplifier, A3. Offset voltage is adjustable to zero as discussed in the applications section.

Power Supply Sensitivity

Power supply sensitivity is a measure of the effect of power supply changes on the D/A full-scale output.

Settling Time

Two settling time parameters are specified for the DAC1200 series. Full-scale settling time requires a zero to full-scale or full-scale to zero output change. One LSB settling time requires one LSB output change. In both instances, settling time is the time required from a code transition until the D/A output reaches within ±½ LSB of final output value.

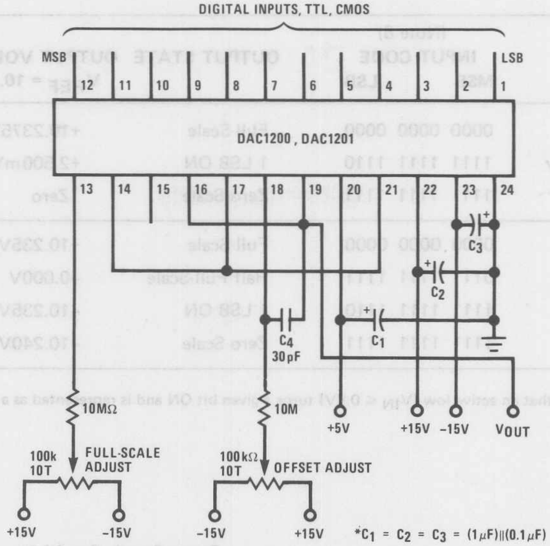
Monotonicity

Monotonicity is a characteristic of the D/A which requires a non-negative output step for an increasing input digital code. Monotonicity, therefore, demands no back steps or changes in sign of the slope of the D/A transfer characteristic.

Full-Scale Error

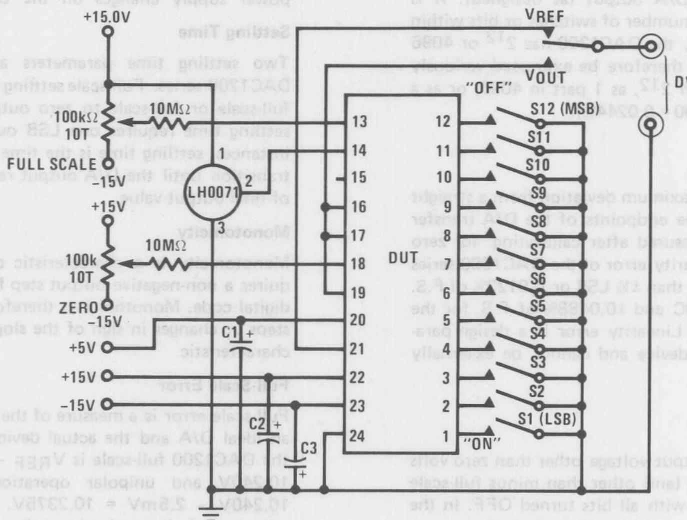
Full-scale error is a measure of the output error between an ideal D/A and the actual device output. Ideally, for the DAC1200 full-scale is V_{REF} − 1 LSB. For V_{REF} = 10.240V and unipolar operation, $V_{FULLSCALE}$ = 10.240V − 2.5mV = 10.2375V. Departures from this value include internal gain, scaling, and reference errors. Full-scale error is adjustable to zero as discussed in the **Applications** section.

Typical Application



20 Volt Full-Scale Complementary D/A

DC Test Circuit



C1 = C2 = C3 = 4.7μF (solid tantalum) in parallel with a 0.01μF ceramic disc

Ordering Information

PART NUMBER	PACKAGE	25°C LINEARITY ERROR	OPERATING TEMPERATURE RANGE
DAC1200HD	Ceramic DIP	0.01%	−55°C to +125°C
DAC1201HD	Ceramic DIP	0.05%	−55°C to +125°C
DAC1200HCD	Ceramic DIP	0.01%	−25°C to +85°C
DAC1201HCD	Ceramic DIP	0.05%	−25°C to +85°C

National Semiconductor

MICRO-DAC™ DAC1208, DAC1209, DAC1210, DAC1230, DAC1231, DAC1232 12-Bit, μP Compatible, Double-Buffered D to A Converters

General Description

The DAC1208 and the DAC1230 series are 12-bit multiplying D to A converters designed to interface directly with a wide variety of microprocessors (8080, 8048, 8085, Z-80, etc.). Double buffering input registers and associated control lines allow these DACs to appear as a two-byte "stack" in the system's memory or I/O space with no additional interfacing logic required.

The DAC1208 series provides all 12 input lines to allow single buffering for maximum throughput when used with 16-bit processors. These input lines can also be externally configured to permit an 8-bit data interface. The DAC1230 series can be used with an 8-bit data bus directly as it internally formulates the 12-bit DAC data from its 8 input lines. All of these DACs accept left-justified data from the processor.

The analog section is a precision silicon-chromium (Si-Cr) R-2R ladder network and twelve CMOS current switches. An inverted R-2R ladder structure is used with the binary weighted currents switched between the I_{OUT1} and I_{OUT2} maintaining a constant current in each ladder leg independent of the switch state. Special circuitry provides TTL logic input voltage level compatibility.

The DAC1208 series and DAC1230 series are the 12-bit members of a family of microprocessor compatible DACs (MICRO-DACs™). For applications requiring other resolutions, the DAC1000 series for 10-bit and DAC0830 series for 8-bit are available alternatives.

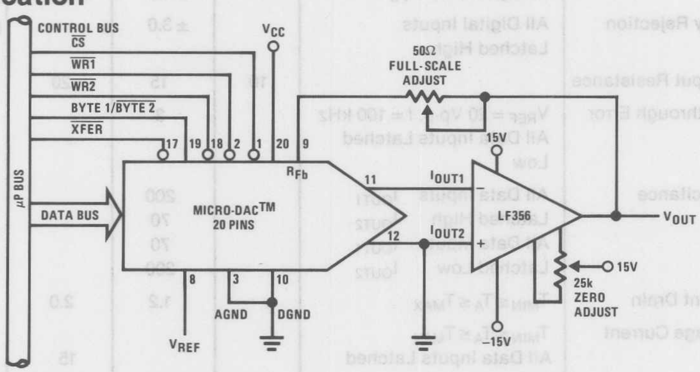
Features

- Linearity specified with zero and full-scale adjust only
- Direct interface to all popular microprocessors
- Double-buffered, single-buffered or flow through digital data inputs
- Logic inputs which meet TTL voltage level specs (1.4V logic threshold)
- Works with ±10V reference—full 4-quadrant multiplication
- Operates stand-alone (without μP) if desired
- All parts guaranteed 12-bit monotonic
- DAC1230 series is pin compatible with the DAC0830 series 8-bit MICRO-DACs

Key Specifications

■ Current Settling Time	1 μs
■ Resolution	12 Bits
■ Linearity (Guaranteed over temperature)	10, 11, or 12 Bits of FS
■ Gain Tempco	1.5 ppm/°C
■ Low Power Dissipation	20 mW
■ Single Power Supply	$5\ V_{DC}$ to $15\ V_{DC}$

Typical Application



Ordering Information

Accuracy	Package 20-Pin D20A	24-Pin D24C
0.012%	DAC1230LCD	DAC1208LCD
0.024%	DAC1231LCD	DAC1209LCD
0.05%	DAC1232LCD	DAC1210LCD

MICRO-DAC™ is a trademark of National Semiconductor Corp.

Voltage at Any Digital Input	V_{CC} to GND
Voltage at V_{REF} Input	±25V
Storage Temperature Range	−65°C to +150°C
Package Dissipation at $T_A = 25°C$ (Note 3)	500 mW
DC Voltage Applied to I_{OUT1} or I_{OUT2} (Note 4)	−100 mV to V_{CC}
Lead Temperature (Soldering, 10 seconds)	300°C

Range of V_{CC}	4.75 V_{DC} to 16 V_{DC}
Voltage at Any Digital Input	V_{CC} to GND

* Military temperature range device will be available in future.

Electrical Characteristics $T_A = 25°C$, $V_{REF} = 10.000\ V_{DC}$, $V_{CC} = 11.4\ V_{DC}$ to $15.75\ V_{DC}$ unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units	Notes
Resolution		12	12	12	Bits	
Linearity Error	Zero and Full-Scale					4, 7
(End Point Linearity)	Adjusted					
	$T_{MIN} < T_A < T_{MAX}$					6
	$-10V \le V_{REF} \le 10V$					5
	DAC1208, DAC1230			0.012	% of FSR	
	DAC1209, DAC1231			0.024	% of FSR	
	DAC1210, DAC1232			0.05	% of FSR	
Differential Non-Linearity	Zero and Full-Scale					4, 7
	Adjusted					
	$T_{MIN} < T_A < T_{MAX}$					6
	$-10V \le V_{REF} \le 10V$					5
	DAC1208, DAC1230			0.012	% of FSR	
	DAC1209, DAC1231			0.024	% of FSR	
	DAC1210, DAC1232			0.05	% of FSR	
Monotonicity	$T_{MIN} < T_A < T_{MAX}$					4, 6
	$-10V \le V_{REF} \le 10V$	12	12	12	Bits	5
Gain Error	Using Internal R_{Fb}					
	$-10V \le V_{REF} \le 10V$	−0.2	−0.01	0.0	% of FS	5
Gain Error Tempco	$T_{MIN} < T_A < T_{MAX}$					6, 7
	Using Internal R_{Fb}		±1.3	±6.0	ppm of FS/°C	10
Power Supply Rejection	All Digital Inputs		±3.0		ppm of FSR/V	7
	Latched High					
Reference Input Resistance		10	15	20	kΩ	
Output Feedthrough Error	$V_{REF} = 20$ Vp-p, f = 100 kHz		3		mVp-p	9
	All Data Inputs Latched					
	Low					
Output Capacitance	All Data Inputs I_{OUT1}		200		pF	
	Latched High I_{OUT2}		70		pF	
	All Data Inputs I_{OUT1}		70		pF	
	Latched Low I_{OUT2}		200		pF	
Supply Current Drain	$T_{MIN} \le T_A \le T_{MAX}$		1.2	2.0	mA	6
Output Leakage Current	$T_{MIN} \le T_A \le T_{MAX}$					6, 11
I_{OUT1}	All Data Inputs Latched			15	nA	6, 11
	Low					
I_{OUT2}	All Data Inputs Latched			15	nA	
	High					
Digital Input Threshold	$T_{MIN} \le T_A \le T_{MAX}$					6
	Low Threshold			0.8	V_{DC}	
	High Threshold	2.0			V_{DC}	
Digital Input Currents	$T_{MIN} \le T_A \le T_{MAX}$					6
	Digital Inputs < 0.8V		−50	−200	μA_{DC}	
	Digital Inputs > 2.0V		0.1	10	μA_{DC}	

Electrical Characteristics (Continued)

$T_A = 25°C$, $V_{REF} = 10.000\ V_{DC}$, $V_{CC} = 11.4\ V_{DC}$ to $15.75\ V_{DC}$ unless otherwise noted.

	Parameter	Conditions	Min	Typ	Max	Units	Notes
t_S	Full-Scale Current Settling Time	$R_L = 100\Omega$, Output Settled to 0.01% $\overline{CS} = \overline{WR1} = \overline{WR2} = \overline{XFER} = 0V$, Byte 1/$\overline{\text{Byte 2}}$ = 5V, DI_0 through DI_{11} Switched Simultaneously		1		μs	
t_W	Write and $\overline{XFER}$ Pulse Width	$V_{IL} = 0V$, $V_{IH} = 5V$	320	50		ns	8, 10
		$T_{MIN} \le T_A \le T_{MAX}$	320	80	—	ns	6, 8, 10
t_{DS}	Data Set-Up Time	$V_{IL} = 0V$, $V_{IH} = 5V$	320	70		ns	10
		$T_{MIN} \le T_A \le T_{MAX}$	320	80	—	ns	6, 10
t_{DH}	Data Hold Time	$V_{IL} = 0V$, $V_{IH} = 5V$	90	50		ns	10
		$T_{MIN} \le T_A \le T_{MAX}$	90	60		ns	6, 10
t_{CS}	Control Set-Up Time	$V_{IL} = 0V$, $V_{IH} = 5V$	320	60	—	ns	10
		$T_{MIN} \le T_A \le T_{MAX}$	320	100	—	ns	6, 10
t_{CH}	Control Hold Time	$V_{IL} = 0V$, $V_{IH} = 5V$	10	0		ns	10
		$T_{MIN} \le T_A \le T_{MAX}$	10	0	—	ns	6, 10

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. These specifications are not meant to imply that the devices should be operated at these "Absolute Maximum" limits.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: This 500 mW specification applies for all packages. The low intrinsic power dissipation of this part (and the fact that there is no way to significantly modify the power dissipation) removes concern for heat sinking.

Note 4: Both I_{OUT1} and I_{OUT2} must go to ground or the virtual ground of an operational amplifier. The linearity error is degraded by approximately $V_{OS} \div V_{REF}$. For example, if $V_{REF} = 10V$ then a 1 mV offset, V_{OS}, on I_{OUT1} or I_{OUT2} will introduce an additional 0.01% linearity error.

Note 5: Guaranteed at $V_{REF} = \pm 10\ V_{DC}$ and $V_{REF} = \pm 1\ V_{DC}$.

Note 6: $T_{MIN} = -40°C$ and $T_{MAX} = 85°C$.

Note 7: The unit FSR stands for full-scale range. Linearity Error and Power Supply Rejection specs are based on this unit to eliminate dependence on a particular V_{REF} value to indicate the true performance of the part. The Linearity Error specification of the DAC1208 is 0.012% of FSR(max). This guarantees that after performing a zero and full-scale adjustment, the plot of the 4096 analog voltage outputs will each be within 0.012% $\times$ V_{REF} of a straight line which passes through zero and full-scale. The unit ppm of FSR (parts per million of full-scale range) and ppm of FS (parts per million of full-scale) are used for convenience to define specs of very small percentage values, typical of higher accuracy converters. In this instance, 1 ppm of FSR = $V_{REF}/10^6$ is the conversion factor to provide an actual output voltage quantity. For example, the gain error tempco spec of ± 6 ppm of FS/°C represents a worst-case full-scale gain error change with temperature from $-40°C$ to $+85°C$ of $\pm(6)(V_{REF}/10^6)(125°C)$ or $\pm 0.75\ (10^{-3})\ V_{REF}$ which is $\pm 0.075\%$ of V_{REF}.

Note 8: This spec implies that all parts are guaranteed to operate with a write pulse or transfer pulse width (t_W) of 320 ns. A typical part will operate with t_W of only 100 ns. The entire write pulse must occur within the valid data interval for the specified t_W, t_{DS}, t_{DH} and t_S to apply.

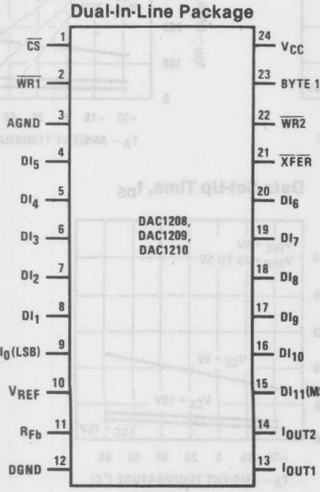
Note 9: To achieve this low feedthrough in the D package, the user must ground the metal lid. If the lid is left floating the feedthrough is typically 6 mV.

Note 10: Guaranteed by design but not tested.

Note 11: A 10 nA leakage current with $R_{Fb} = 20k$ and $V_{REF} = 10V$ corresponds to a zero error of $(10 \times 10^{-9} \times 20 \times 10^3) \times 100\%$ 10V or 0.002% of FS.

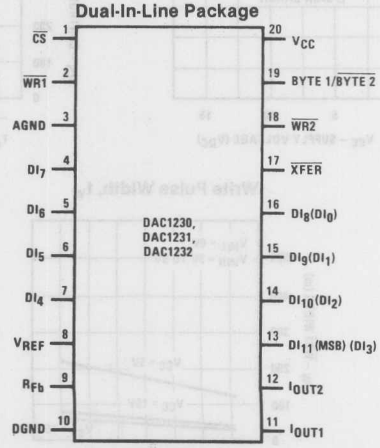
Connection Diagrams

Dual-In-Line Package



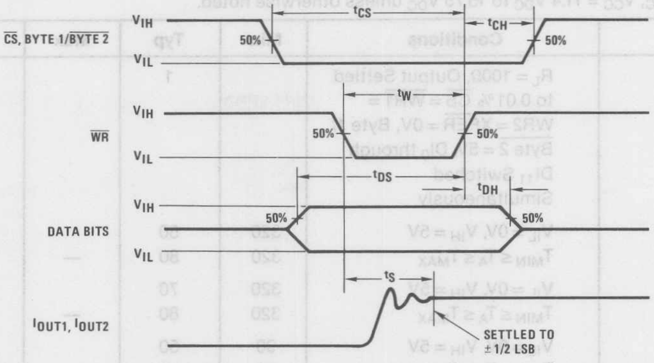
TOP VIEW

Dual-In-Line Package



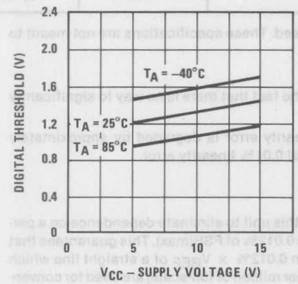
TOP VIEW

Switching Waveforms

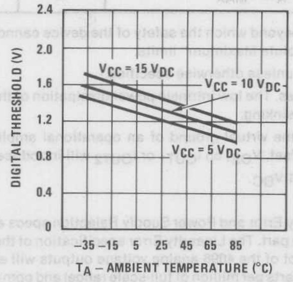


Typical Performance Characteristics

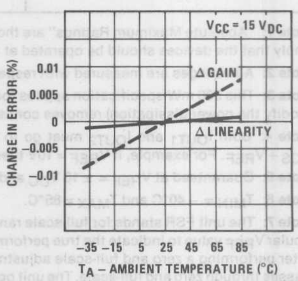
Digital Input Threshold vs VCC



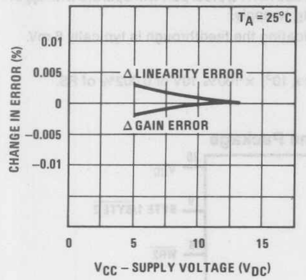
Digital Input Threshold vs Temperature



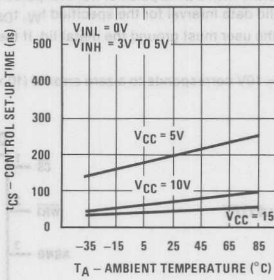
Gain and Linearity Error Variation vs Temperature



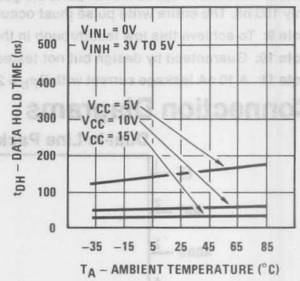
Gain and Linearity Error Variation vs Supply Voltage



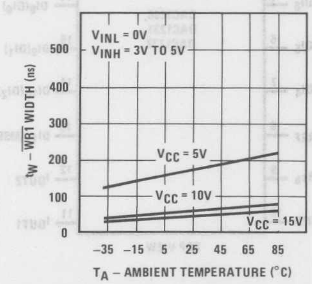
Control Set-Up Time, t_{CS}



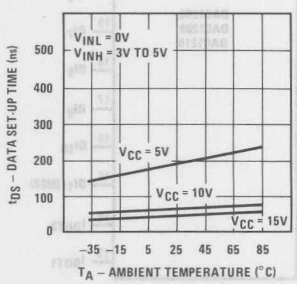
Data Hold Time, t_{DH}



Write Pulse Width, t_W



Data Set-Up Time, t_{DS}



Definition of Package Pinouts

CONTROL SIGNALS (all control signals are level actuated)

$\overline{CS}$: Chip Select (active low). The $\overline{CS}$ will enable $\overline{WR1}$.

$\overline{WR1}$: Write 1. The active low $\overline{WR1}$ is used to load the digital data bits (DI) into the input latch. The data in the input latch is latched when $\overline{WR1}$ is high. The 12-bit input latch is split into two latches, one holds the first 8 bits, while the other holds 4 bits. The Byte 1/$\overline{\text{Byte 2}}$ control pin is used to select both latches when Byte 1/$\overline{\text{Byte 2}}$ is high or to overwrite the 4-bit input latch when in the low state.

Byte 1/$\overline{\text{Byte 2}}$: Byte Sequence Control. When this control is high, all 12 locations of the input latch are enabled. When low, only the four least significant locations of the input latch are enabled.

$\overline{WR2}$: Write 2 (active low). The $\overline{WR2}$ will enable $\overline{XFER}$.

$\overline{XFER}$: Transfer Control Signal (active low). This signal, in combination with $\overline{WR2}$, causes the 12-bit data which is available in the input latches to transfer to the DAC register.

DI_0 to DI_{11}: Digital Inputs. DI_0 is the least significant digital input (LSB) and DI_{11} is the most significant digital input (MSB).

I_{OUT1}: DAC Current Output 1. I_{OUT1} is a maximum for a digital code of all 1s in the DAC register, and is zero for all 0s in the DAC register.

I_{OUT2}: DAC Current Output 2. I_{OUT2} is a constant minus I_{OUT1}, or $I_{OUT1} + I_{OUT2} = \text{constant}$ (for a fixed reference voltage). This constant current is

$$V_{REF} \times \left(1 - \frac{1}{4096}\right)$$

divided by the reference input resistance.

R_{Fb}: Feedback Resistor. The feedback resistor is provided on the IC chip for use as the shunt feedback resistor for the external op amp which is used to provide an output voltage for the DAC. This on-chip resistor should always be used (not an external resistor) since it matches the resistors which are used in the on-chip R-2R ladder and tracks these resistors over temperature.

V_{REF}: Reference Voltage Input. This input connects an external precision voltage source to the internal R-2R ladder. V_{REF} can be selected over the range of 10V to −10V. This is also the analog voltage input for a 4-quadrant multiplying DAC application.

V_{CC}: Digital Supply Voltage. This is the power supply pin for the part. V_{CC} can be from 5 V_{DC} to 15 V_{DC}. Operation is optimum for 15 V_{DC}.

AGND: Analog Ground. This is the ground for the analog circuitry.

DGND: Digital Ground. This is the ground for the digital logic.

Definition of Terms

Resolution: Resolution is defined as the reciprocal of the number of discrete steps in the DAC output. It is directly related to the number of switches or bits within the DAC. For example, the DAC1208 has 2^{12} or 4096 steps and therefore has 12-bit resolution.

Linearity Error: Linearity error is the maximum deviation from a *straight line passing through the endpoints of the DAC transfer characteristic.* It is measured after adjusting for zero and full-scale. Linearity error is a parameter intrinsic to the device and cannot be externally adjusted.

National's linearity test (a) and the best straight line test (b) used by other suppliers are illustrated below. The best straight line (b) requires a special zero and FS adjustment for each part, which is almost impossible for the user to determine. The end point test uses a standard zero FS adjustment procedure and is a much more stringent test for DAC linearity.

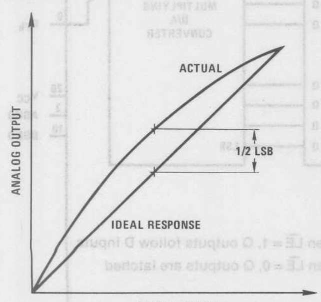
Power Supply Sensitivity: Power supply sensitivity is a measure of the effect of power supply changes on the DAC full-scale output.

Settling Time: Full-scale current settling time requires zero to full-scale or full-scale to zero output change. Settling time is the time required from a code transition until the DAC output reaches within ± 1/2 LSB of the final output value.

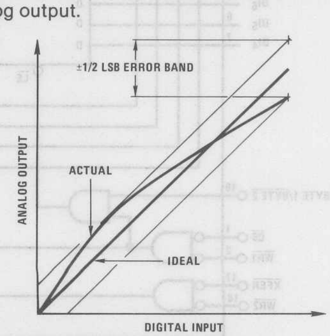
Full-Scale Error: Full-scale error is a measure of the output error between an ideal DAC and the actual device output. Ideally, for the DAC1208 or DAC1230 series, full-scale is V_{REF}–1 LSB. For $V_{REF} = 10V$ and unipolar operation, $V_{FULL\text{-}SCALE} = 10.0000V - 2.44\ mV = 9.9976V$. Full-scale error is adjustable to zero.

Differential Non-Linearity: The difference between any two consecutive codes in the transfer curve from the theoretical 1 LSB is differential non-linearity.

Monotonic: If the output of a DAC increases for increasing digital input code, then the DAC is monotonic. A 12-bit DAC which is monotonic to 12 bits simply means that input increasing digital input codes will produce an increasing analog output.



a) End point test after zero and FS adjust



b) Shifting FS adjust to pass best straight line test

These DACs are designed to provide all of the necessary digital input circuitry to permit a direct interface to a wide variety of microprocessor systems. The timing and logic level convention of the input control signals allow the DACs to be treated as a typical memory device or I/O peripheral with no external logic required in most systems. Essentially these DACs can be mapped as a two-byte stack in memory (or I/O space) to receive their 12 bits of input data in two successive 8-bit data writing sequences. The DAC1230 series is intended for use in systems with an 8-bit data bus. The DAC1208 series provides all 12 digital input lines which can be externally configured to be controlled from an 8-bit bus or can be driven directly from a 16-bit data bus.

logic levels in non-microprocessor based systems. To prevent damage to the chip from static discharge, all unused digital inputs should be tied to V_{CC} or ground. As a troubleshooting aid, if any of the digital inputs are inadvertently left floating, the DAC will interpret the pin as a logic "1".

Double buffered digital inputs allow the DAC to internally format the 12-bit word used to set the current switching R-2R ladder network (see section 2.0) from two 8-bit data write cycles. *Figures 1 and 2* show the internal data registers and their controlling logic circuitry. The timing diagrams for updating the DAC output are shown in sections 1.1, 1.2 and 1.3 for three possible control modes. The method used depends strictly upon the particular application.

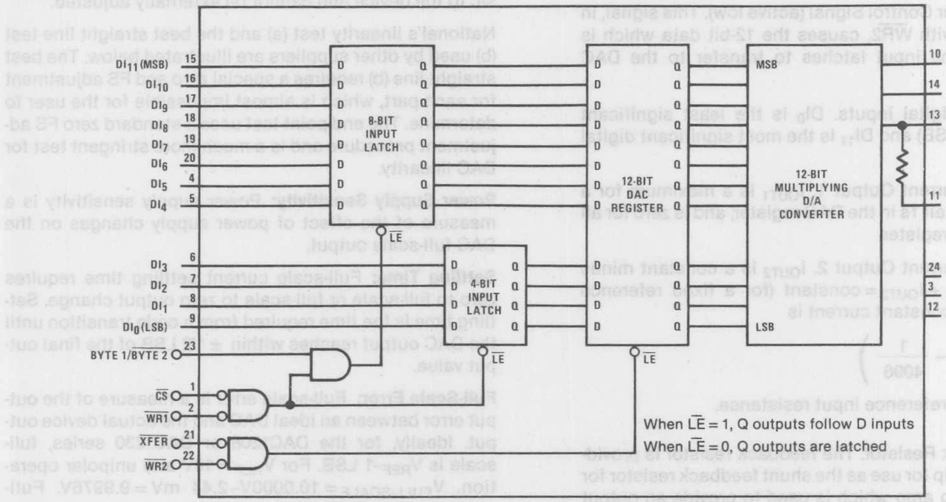


FIGURE 1. DAC1208, DAC1209, DAC1210 Functional Diagram

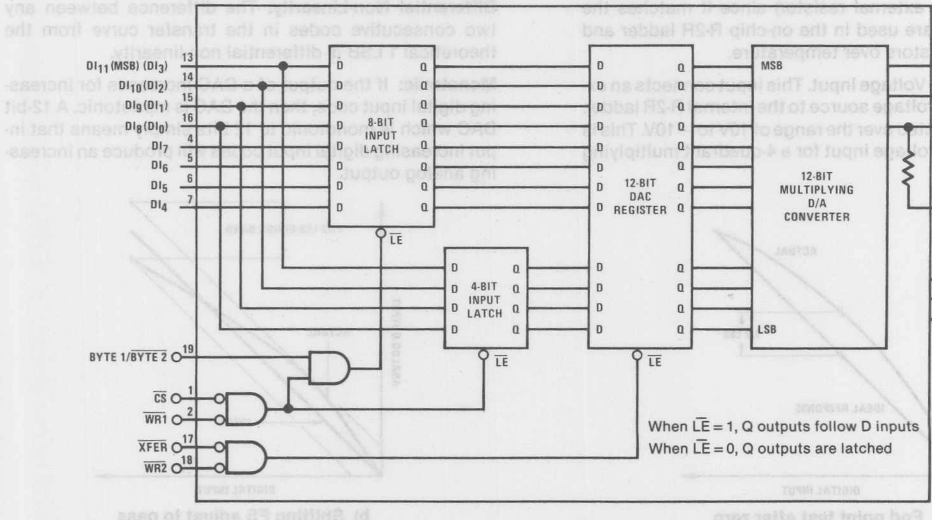
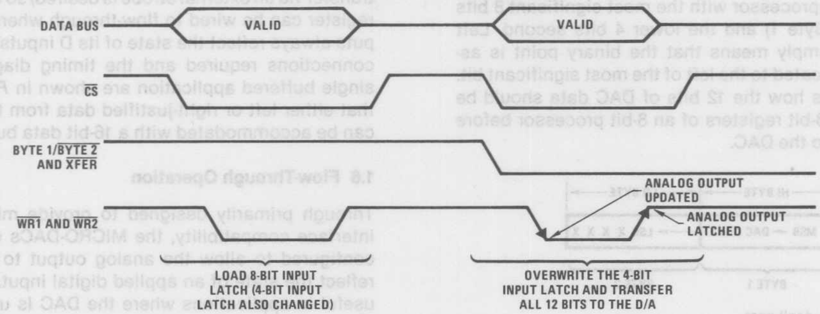


FIGURE 2. DAC1230, DAC1231, DAC1232 Functional Diagram

Application Hints (Continued)

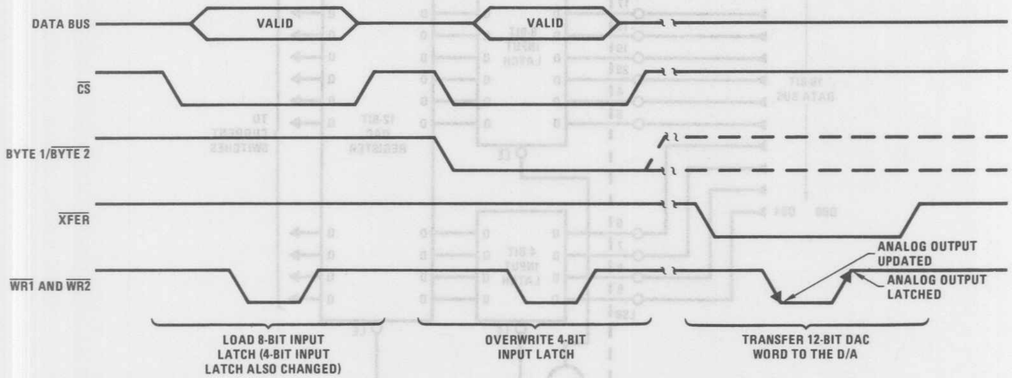
1.1 Automatic Transfer

The 12-bit DAC word is automatically transferred to the DAC register and the R-2R ladder when the second write (the 4 LSBs of the data) occurs.



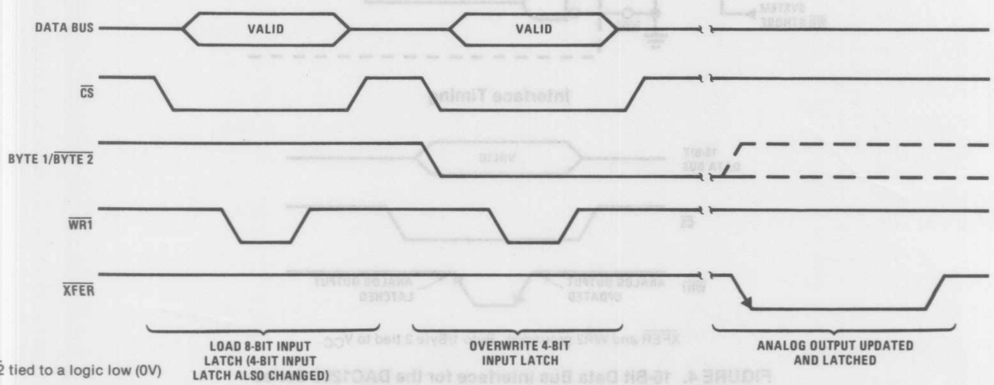
1.2 Independent Processor Transfer Control

In this case a separate address is decoded to provide the $\overline{XFER}$ signal. This allows the processor to load the next required DAC word but not change the analog output until some time later, most useful for the simultaneous updating of several DACs in a system where their $\overline{XFER}$ lines would be tied together.



1.3 Transfer via an External Strobe

This method is basically the same as the previous operation except the $\overline{XFER}$ signal is provided by a device other than the processor. This allows the DAC to hold the code for a conditional analog output signal which will be required on demand from an external monitoring device (an analog voltage comparator for instance).



$\overline{WR2}$ tied to a logic low (0V)

Application Hints (Continued)

1.4 Left-Justified Data Format

It is important to realize that the input registers of these DACs are arranged to accept a left-justified data word from the microprocessor with the most significant 8 bits coming first (Byte 1) and the lower 4 bits second. Left justification simply means that the binary point is assumed to be located to the left of the most significant bit. *Figure 3* shows how the 12 bits of DAC data should be arranged in 2 8-bit registers of an 8-bit processor before being written to the DAC.

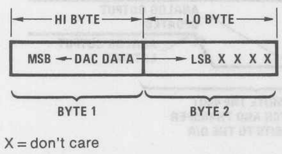


FIGURE 3. Left-Justified Data Format

1.5 16-Bit Data Bus Interface

The DAC1208 series provides all 12 digital input lines to permit a direct parallel interface to a 16-bit data bus. In this instance, double buffering is not always necessary (unless a simultaneous updating of several DACs or a data transfer via an external strobe is desired) so the 12-bit DAC register can be wired to flow-through whereby its Q outputs always reflect the state of its D inputs. The external connections required and the timing diagram for this single buffered application are shown in *Figure 4.* Note that either left or right-justified data from the processor can be accommodated with a 16-bit data bus.

1.6 Flow-Through Operation

Through primarily designed to provide microprocessor interface compatibility, the MICRO-DACs can easily be configured to allow the analog output to continuously reflect the state of an applied digital input. This is most useful in applications where the DAC is used in a continuous feedback control loop and is driven by a binary up-down counter, or in function generation circuits where a ROM is continuously providing DAC data.

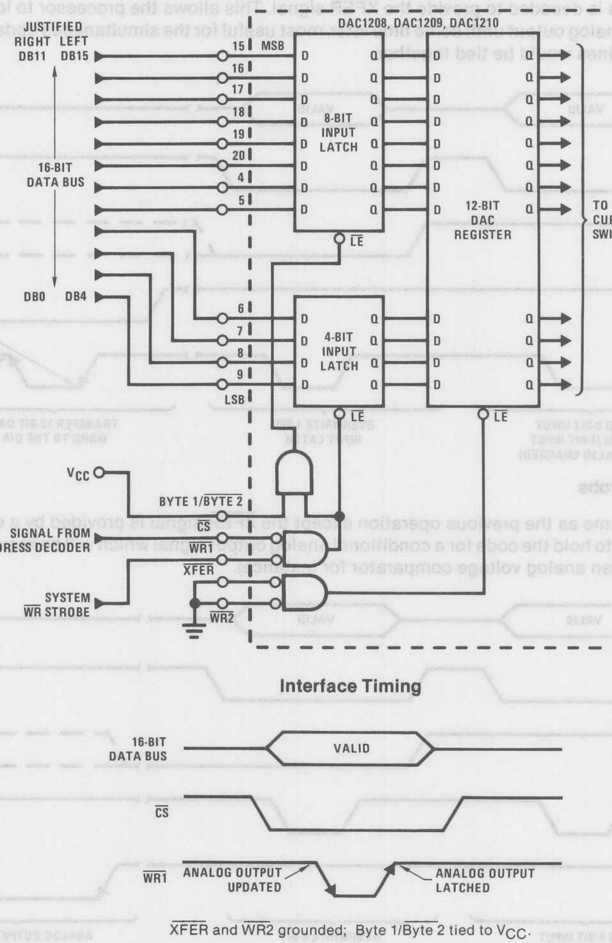


FIGURE 4. 16-Bit Data Bus Interface for the DAC1208 Series

Application Hints (Continued)

Only the DAC1208, DAC1209, DAC1210 devices can have all 12 inputs flow-through. Simply grounding $\overline{CS}$, $\overline{WR1}$, $\overline{WR2}$ and $\overline{XFER}$ and tying Byte 1/$\overline{Byte\ 2}$ high allows both internal registers to follow the applied digital inputs (flow-through) and directly affect the DAC analog output.

1.7 Address Decoding Tips

It is possible to map the MICRO-DACs into system ROM space to allow more efficient use of existing address decoding hardware. The DAC in effect could share the same addresses of any number of ROM locations. The ROM outputs will only be enabled by a READ of its address (gated by the system READ strobe) and the DAC will only accept data that is written to the same address (gated by the system WRITE strobe).

The Byte 1/$\overline{Byte\ 2}$ control function can easily be generated by the processor's least significant address bit (A0) by placing the DAC at two consecutive address locations and utilizing double-byte WRITE instructions which automatically increment or decrement the address. The $\overline{CS}$ and $\overline{XFER}$ signals would then be decoded from the remaining address bits. Care must be taken in selecting the actual address used for Byte 1 of the DAC to prevent a carry (as a result of incrementing the address for Byte 2) from propagating through the address word and changing any of the bits being decoded for $\overline{CS}$ or $\overline{XFER}$. *Figure 5* shows how to prevent this effect.

The same problem can occur from a borrow when an auto-decremented address is used; but only if the processor's address outputs are inverted before being decoded.

1.8 Control Signal Timing

When interfacing these MICRO-DACs to any microprocessor, there are two important time relationships that must be considered to insure proper operation. The first is the minimum $\overline{WR}$ strobe pulse width which is specified as 320 ns for V_{CC} = 11.4V to 15.75V and operation over temperature, but typically a pulse width of only 250 ns is adequate. A second consideration is that the guaranteed minimum data hold time of 90 ns should be met or erroneous data can be latched. This hold time is defined as the length of time data must be held valid on the digital inputs *after* a qualified (via $\overline{CS}$) $\overline{WR}$ strobe makes a low to high transition to latch the applied data.

If the controlling device or system does not inherently meet these timing specs the DAC can be treated as a slow memory or peripheral and utilize a technique to extend the write strobe. A simple extension of the write time, by adding a wait state, can simultaneously hold the write strobe active and data valid on the bus to satisfy the minimum $\overline{WR}$ pulse width. If this does not provide a sufficient data hold time at the end of the write cycle, a negative edge triggered one-shot can be included between the system write strobe and the $\overline{WR}$ pin of the DAC. This is illustrated in *Figure 6* for an exemplary system which provides a 250 ns $\overline{WR}$ strobe time with a data hold time of only 10 ns.

Write Cycle	Address Bits 15 … 2	1*	0**
First (Byte 1)	Decoded to Address DAC	0	1
Second (Byte 2)		1	0

* Starting with a 0 prevents a carry on address incrementing.
** Used as Byte1/$\overline{Byte2}$ Control

FIGURE 5

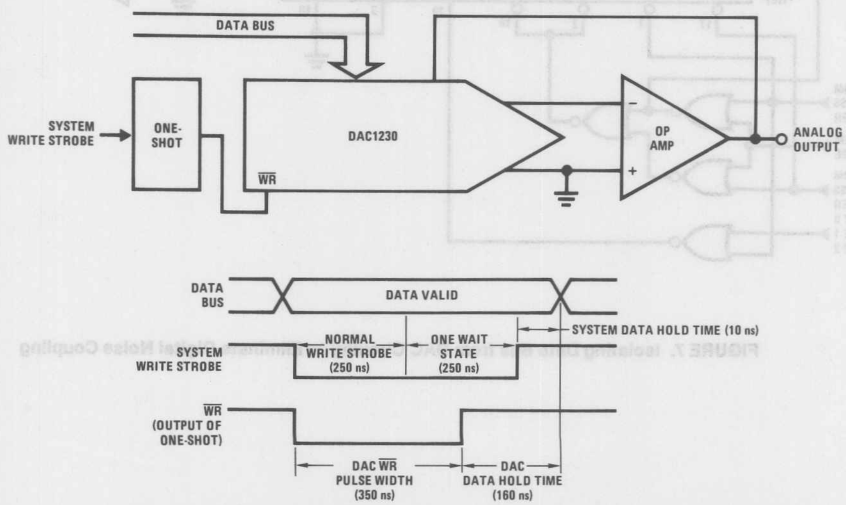


FIGURE 6. Accommodating a High Speed System

to high transition) of the $\overline{WR}$ strobe, is insured if the $\overline{WR}$ pulse width is within spec and the data is valid on the bus for the duration of the DAC $\overline{WR}$ strobe.

1.9 Digital Signal Feedthrough

A typical digital/microprocessor is a tremendous potential source of high frequency noise which can be coupled to sensitive analog circuitry. The fast edges of the data and address bus signals generate frequency components of 10's of megahertz and may cause fast transients to appear at the DAC output, even when data is latched internally.

In low frequency or DC applications, low pass filtering can reduce the magnitude of any fast transients. This is most easily accomplished by over-compensating the DAC output amplifier by increasing the value of its feedback capacitor.

DAC and op amp, filtering may not be feasible. In this event, digital signals can be completely isolated from the DAC circuitry, by the use of a DM74LS374 latch, until a valid $\overline{CS}$ signal is applied to update the DAC. This is shown in *Figure 7*.

A single TRI-STATE® data buffer such as the DM81LS95 can be used to isolate any number of DACs in a system. *Figure 8* shows this isolating circuitry and decoding hardware for a multiple DAC analog output card. Pull-up resistors are used on the buffer outputs to limit the impedance at the DAC digital inputs when the card is not selected. A unique feature of this card is that the DAC $\overline{XFER}$ strobes are controlled by the data bus. This allows a very flexible update of any combination of analog outputs via a transfer word which would contain a zero in the bit position assigned to any of the DACs required to change to a new output value.

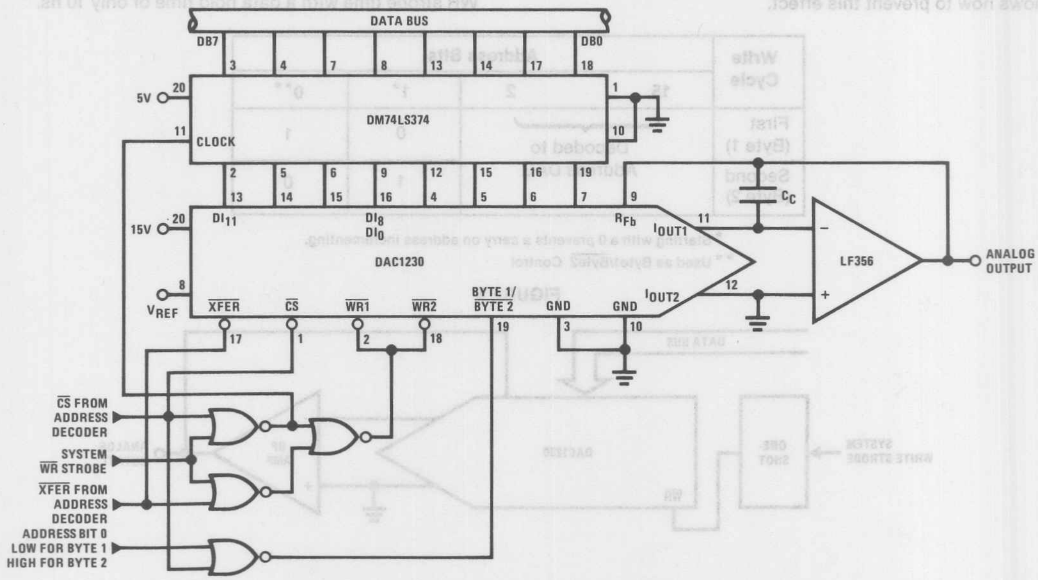


FIGURE 7. Isolating Data Bus from DAC Circuitry to Eliminate Digital Noise Coupling

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Application Hints (Continued)

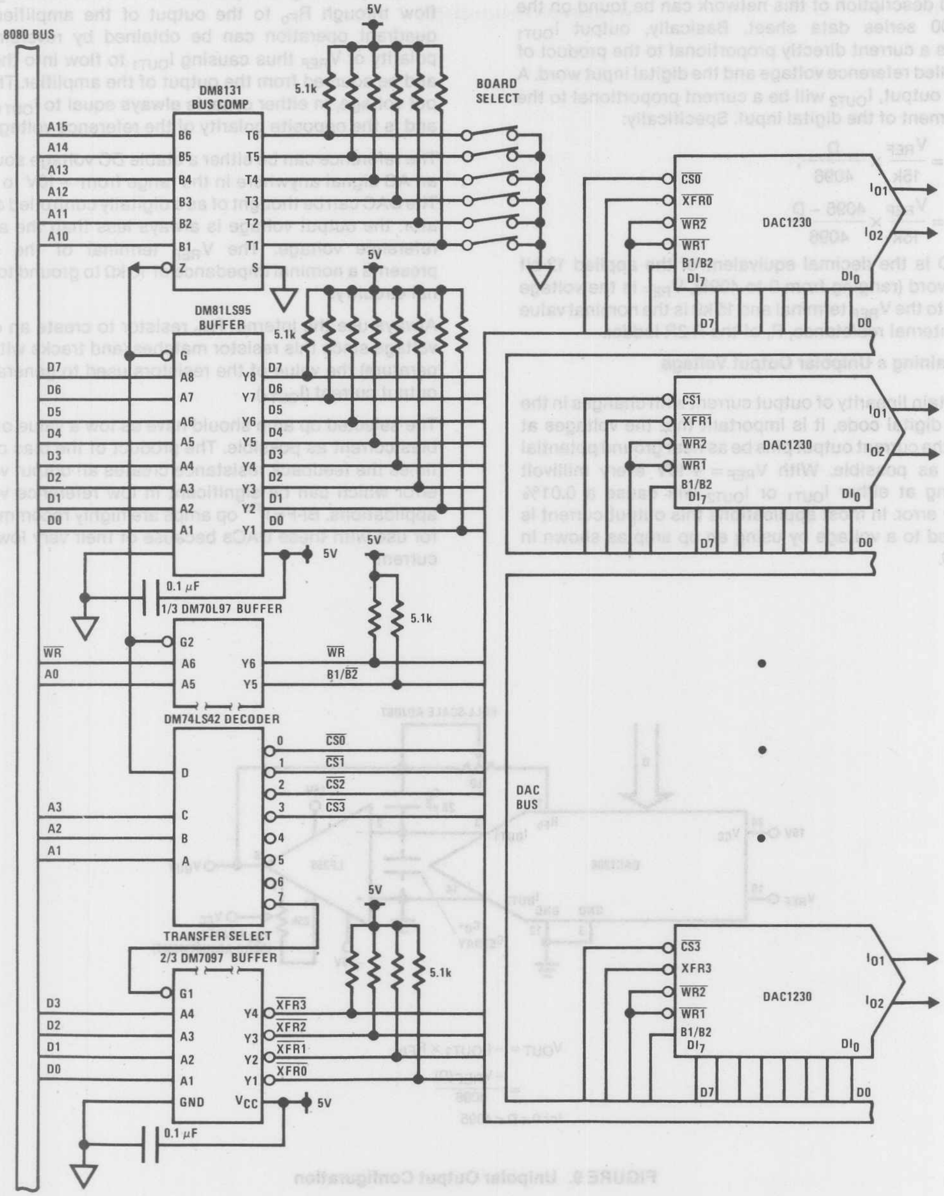


FIGURE 8. TRI-STATE® Buffers Isolate the Data and Control Lines from the DACs. A Transfer Word Provides a Flexible Update.

Application Hints (Continued)

2.0 ANALOG APPLICATIONS

The analog output signal for these DACs is derived from a conventional R-2R current switching ladder network. A detailed description of this network can be found on the DAC1000 series data sheet. Basically, output I_{OUT1} provides a current directly proportional to the product of the applied reference voltage and the digital input word. A second output, I_{OUT2} will be a current proportional to the complement of the digital input. Specifically:

$$I_{OUT1} = \frac{V_{REF}}{15k} \times \frac{D}{4096};$$

$$I_{OUT2} = \frac{V_{REF}}{15k} \times \frac{4095 - D}{4096}$$

where D is the decimal equivalent of the applied 12-bit binary word (ranging from 0 to 4095), V_{REF} is the voltage applied to the V_{REF} terminal and 15 kΩ is the nominal value of the internal resistance, R, of the R-2R ladder.

2.1 Obtaining a Unipolar Output Voltage

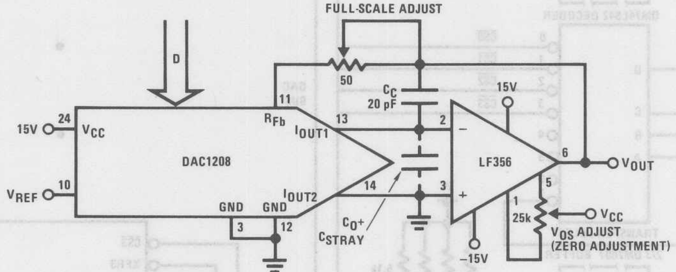
To maintain linearity of output current with changes in the applied digital code, it is important that the voltages at both of the current output pins be as near ground potential (0 V_{DC}) as possible. With $V_{REF} = +10V$ every millivolt appearing at either I_{OUT1} or I_{OUT2} will cause a 0.01% linearity error. In most applications this output current is converted to a voltage by using an op amp as shown in *Figure 9.*

The inverting input of the op amp is a virtual ground created by the feedback from its output through the internal 15 kΩ resistor, R_{Fb}. All of the output current (determined by the digital input and the reference voltage) will flow through R_{Fb} to the output of the amplifier. Two-quadrant operation can be obtained by reversing the polarity of V_{REF} thus causing I_{OUT1} to flow into the DAC and be sourced from the output of the amplifier. The output voltage, in either case, is always equal to $I_{OUT1} \times R_{Fb}$ and is the opposite polarity of the reference voltage.

The reference can be either a stable DC voltage source or an AC signal anywhere in the range from −10V to +10V. The DAC can be thought of as a digitally controlled attenuator: the output voltage is always less than the applied reference voltage. The V_{REF} terminal of the device presents a nominal impedance of 15 kΩ to ground to external circuitry.

Always use the internal R_{Fb} resistor to create an output voltage since this resistor matches (and tracks with temperature) the value of the resistors used to generate the output current (I_{OUT1}).

The selected op amp should have as low a value of input bias current as possible. The product of the bias current times the feedback resistance creates an output voltage error which can be significant in low reference voltage applications. BI-FET™ op amps are highly recommended for use with these DACs because of their very low input current.



$$V_{OUT} = -(I_{OUT1} \times R_{Fb})$$
$$= \frac{-V_{REF}(D)}{4096}$$
for $0 \le D \le 4095$

FIGURE 9. Unipolar Output Configuration

BI-FET™ is a trademark of National Semiconductor Corp.

Application Hints (Continued)

Transient response and settling time of the op amp are important in fast data throughput applications. The largest stability problem is the feedback pole created by the feedback resistance, R_{Fb}, and the output capacitance of the DAC. This appears from the op amp output to the (−) input and includes the stray capacitance at this node. Addition of a lead capacitance, C_C in *Figure 9*, greatly reduces overshoot and ringing at the output for a step change in DAC output current.

2.1.1 Zero and Full-Scale Adjustments

For accurate conversions, the input offset voltage of the output amplifier must always be nulled. Amplifier offset errors create an overall degradation of DAC linearity.

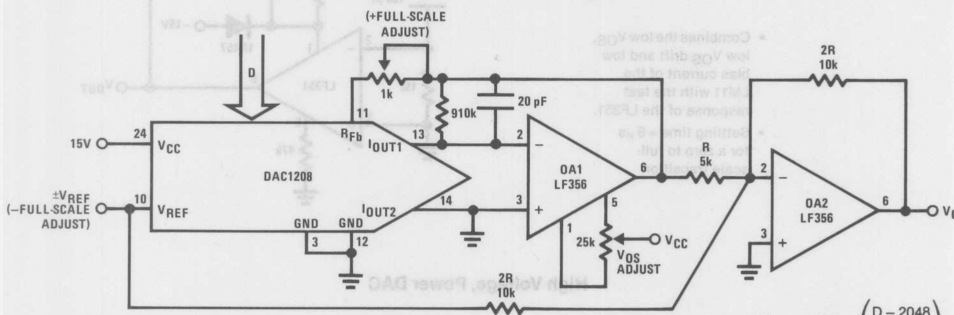
The fundamental purpose of zeroing is to make the voltage appearing at the DAC outputs as near 0 V_{DC} as possible. This is accomplished by shorting out R_{Fb}, the amplifier feedback resistor, and adjusting the V_{OS} nulling potentiometer of the op amp until the output reads zero volts. This is done, of course, with an applied digital code of all zeros if I_{OUT1} is driving the op amp (all ones for I_{OUT2}). The short around R_{Fb} is then removed and the converter is zero adjusted.

A unique feature of this series of DACs is that the full-scale or gain error is guaranteed to be negative. The gain error specification is a measure of how close the value of the internal feedback resistor, R_{Fb}, matches the R-2R ladder resistors. A negative gain error indicates that R_{Fb} is a smaller resistance value than it should be. To adjust this gain error, some resistance must always be added in series with R_{Fb}. The 50Ω potentiometer shown is sufficient to adjust the worst-case gain error for these devices.

2.2 Bipolar Output Voltage from a Fixed Reference

The addition of a second op amp to the unipolar output circuit can generate a bipolar output voltage from a fixed reference voltage. This, in effect, gives sign significance to the MSB of the digital input word to allow two quadrant multiplication of the reference voltage. The polarity of the reference can also be reversed to realize full 4-quadrant multiplication. This circuit is shown in *Figure 10.*

This configuration features several improvements over existing circuits for a bipolar output shown with other multiplying DACs. Only the offset voltage of amplifier 1 affects the linearity of the DAC. The offset voltage error of the second op amp (although a constant output error) has no effect on linearity. In addition, this configuration offers a non-interactive positive and negative full-scale calibration procedure.



$$V_{OUT} = V_{REF}\left(\frac{D-2048}{2048}\right)$$

for $0 \le D \le 4095$

$$1\ LSB = \frac{|V_{REF}|}{2048}$$

Input Code MSB...... LSB	Ideal V_{OUT} $+V_{REF}$	Ideal V_{OUT} $-V_{REF}$
111111111111	V_{REF} −1 LSB	$-\lvert V_{REF}\rvert$ +1 LSB
110000000000	$V_{REF}/2$	$-\lvert V_{REF}\rvert/2$
100000000000	0	0
011111111111	−1 LSB	+1 LSB
001111111111	$-\frac{V_{REF}}{2}$ −1 LSB	$\frac{\lvert V_{REF}\rvert}{2}$ +1 LSB
000000000000	$-V_{REF}$	$+\lvert V_{REF}\rvert$

FIGURE 10. Bipolar Output Voltage Configuration

To calibrate the bipolar output circuit, three adjustments are required. The first step is to set all of the digital input LOW (to force I_{OUT1} to 0) then null the V_{OS} of amplifier 1 by setting the voltage at its inverting input (pin 2) to zero volts. Next, with a code of all zeros still applied, adjust "− full-scale adjust", the reference voltage, for $V_{OUT} = \pm |V_{REF}$ ideal$|$. The polarity of the output voltage at this time will be opposite that of the applied reference. Finally, set all of the digital inputs HIGH and adjust "+ full-scale adjust" for

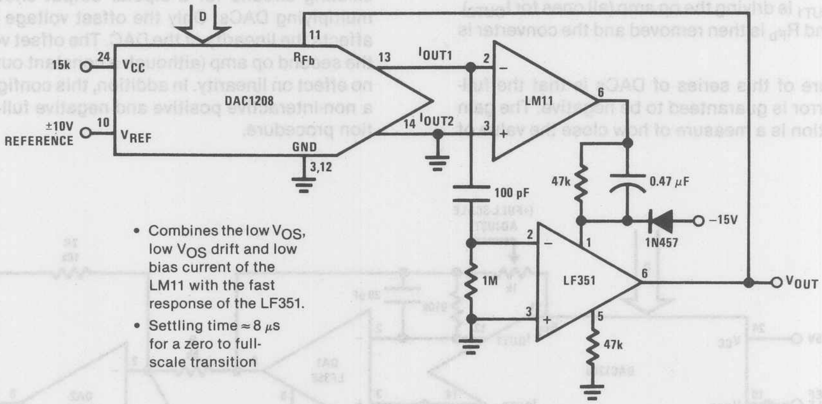
$$V_{OUT} = V_{REF}\,\frac{2047}{2048}.$$

The polarity of the output will be the same as that of the reference voltage.

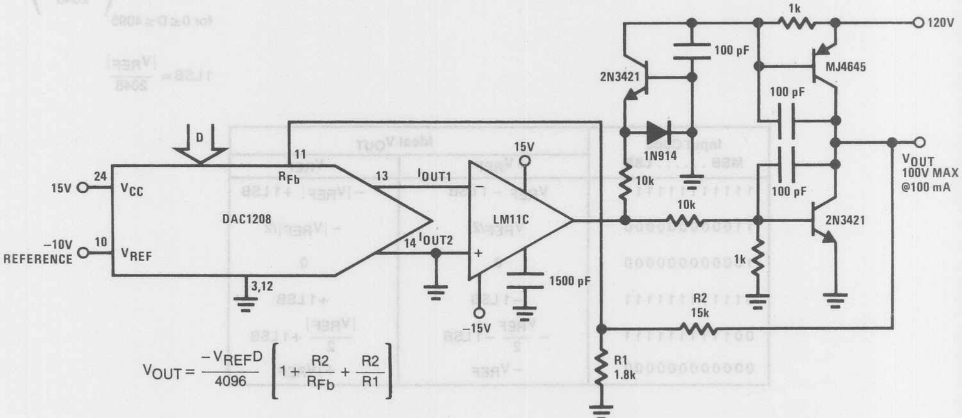
3.0 APPLICATION IDEAS

In this section the digital input word is represented by the letter D and is equal to the decimal equivalent of the 12-bit binary input. Hence D can be any integer value between 0 and 4095.

Composite Amplifier for Good DC Characteristics and Fast Output Response



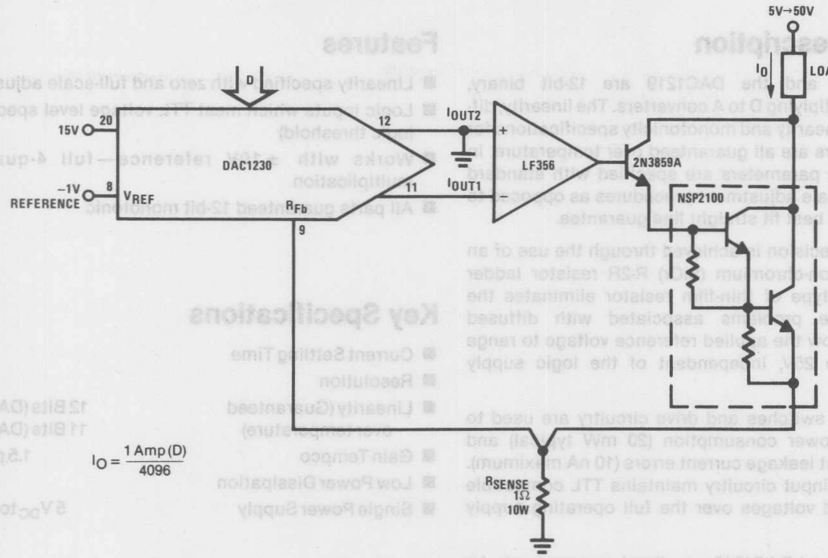
High Voltage, Power DAC



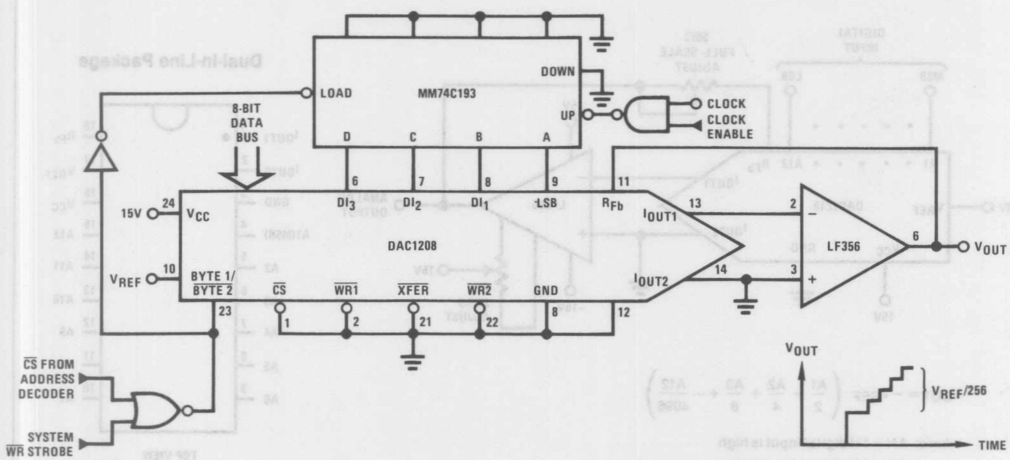
$$V_{OUT} = \frac{-V_{REF}D}{4096}\left[1 + \frac{R2}{R_{Fb}} + \frac{R2}{R1}\right]$$

Application Hints (Continued)

High Current Controller



8-Bit Course, 4-Bit Vernier DAC



National Semiconductor

DAC1218, DAC1219 12-Bit Binary Multiplying D/A Converter

General Description

The DAC1218 and the DAC1219 are 12-bit binary, 4-quadrant multiplying D to A converters. The linearity, differential non-linearity and monotonicity specifications for these converters are all guaranteed over temperature. In addition, these parameters are specified with standard zero and full-scale adjustment procedures as opposed to the impractical best fit straight line guarantee.

This level of precision is achieved through the use of an advanced silicon-chromium (SiCr) R-2R resistor ladder network. This type of thin-film resistor eliminates the parasitic diode problems associated with diffused resistors to allow the applied reference voltage to range from −25V to 25V, independent of the logic supply voltage.

CMOS current switches and drive circuitry are used to achieve low power consumption (20 mW typical) and minimize output leakage current errors (10 nA maximum). Unique digital input circuitry maintains TTL compatible input threshold voltages over the full operating supply voltage range.

The DAC1218 and DAC1219 are direct replacements for the AD7541 series, AD7521 series, and AD7531 series with a significant improvement in the linearity specification. In applications where direct interface of the D to A converter to a microprocessor bus is desirable, the DAC1208 and DAC1230 series eliminate the need for additional interface logic.

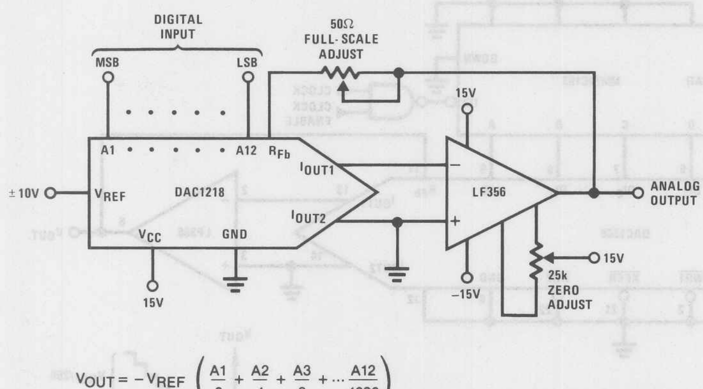
Features

- Linearity specified with zero and full-scale adjust only
- Logic inputs which meet TTL voltage level specs (1.4V logic threshold)
- Works with ±10V reference—full 4-quadrant multiplication
- All parts guaranteed 12-bit monotonic

Key Specifications

Current Settling Time	1 μs
Resolution	12 Bits
Linearity (Guaranteed over temperature)	12 Bits (DAC1218) 11 Bits (DAC1219)
Gain Tempco	1.5 ppm/°C
Low Power Dissipation	20 mW
Single Power Supply	5 V_{DC} to 15 V_{DC}

Typical Application

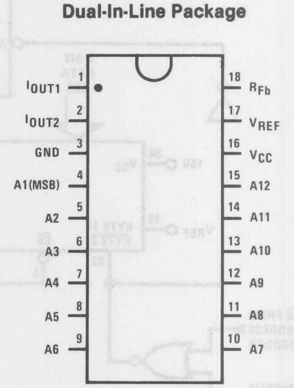


$$V_{OUT} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \ldots \frac{A12}{4096}\right)$$

where: AN = 1 if digital input is high
AN = 0 if digital input is low

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DAC1218LD, DAC1218LCD, DAC1219LD or DAC1219LCD
See NS Package D18A

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	17 V_{DC}
Voltage at Any Digital Input	V_{CC} to GND
Voltage at V_{REF} Input	± 25V
Storage Temperature Range	− 65°C to + 150°C
Package Dissipation at T_A = 25°C (Note 3)	500 mW
DC Voltage Applied to I_{OUT1} or I_{OUT2} (Note 4)	− 100 mV to V_{CC}
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Ratings

Temperature Range	
DAC1218LD, DAC1219LD	− 55°C to + 125°C
DAC1218LCD, DAC1219LCD	− 40°C to + 85°C
Range of V_{CC}	5 V_{DC} to 16 V_{DC}
Voltage at Any Digital Input	V_{CC} to GND

Electrical Characteristics T_A = 25°C, V_{REF} = 10.000 V_{DC}, V_{CC} = 11.4 V_{DC} to 15.75 V_{DC} unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units	Notes
Resolution		12	12	12	Bits	
Linearity Error (End Point Linearity)	Zero and Full-Scale Adjusted					4, 7
	$T_{MIN} < T_A < T_{MAX}$					6
	$-10V \le V_{REF} \le 10V$					5
	DAC1218			0.012	% of FSR	
	DAC1219			0.024	% of FSR	
Differential Non-Linearity	Zero and Full-Scale Adjusted					4, 7
	$T_{MIN} < T_A < T_{MAX}$					6
	$-10V \le V_{REF} \le 10V$					5
	DAC1218			0.012	% of FSR	
	DAC1219			0.024	% of FSR	
Monotonicity	$T_{MIN} < T_A < T_{MAX}$					4, 6
	$-10V \le V_{REF} \le 10V$	12	12	12	Bits	5
Gain Error	Using Internal R_{Fb} $-10V \le V_{REF} \le 10V$	− 0.2	− 0.01	0.0	% of FSR	5, 7
Gain Error Tempco	$T_{MIN} < T_A < T_{MAX}$					6, 7
	Using Internal R_{Fb}		± 1.3	± 6.0	ppm of FS/°C	9
Power Supply Rejection	All Digital Inputs High		± 3.0		ppm of FSR/V	7
Reference Input Resistance		10	15	20	kΩ	
Output Feedthrough Error	V_{REF} = 20 Vp-p, f = 100 kHz All Data Inputs Low		3		mVp-p	
	D Package		3		mVp-p	8
Output Capacitance	All Data Inputs High I_{OUT1}		200		pF	
	All Data Inputs High I_{OUT2}		70		pF	
	All Data Inputs Low I_{OUT1}		70		pF	
	All Data Inputs Low I_{OUT2}		200		pF	
Supply Current Drain	$T_{MIN} \le T_A \le T_{MAX}$		1.2	2.0	mA	6
Output Leakage Current	− 40°C to + 85°C					6, 10
I_{OUT1}	All Data Inputs Low			10	nA	
I_{OUT2}	All Data Inputs High			10	nA	
Output Leakage Current	− 55°C to + 125°C					
I_{OUT1}	All Data Inputs Low			100	nA	
I_{OUT2}	All Data Inputs High			100	nA	
Digital Input Threshold	$T_{MIN} \le T_A \le T_{MAX}$					6
	Low Threshold			0.8	V_{DC}	
	High Threshold	2.0			V_{DC}	
Digital Input Currents	$T_{MIN} \le T_A \le T_{MAX}$					6
	Digital Inputs < 0.8V		− 50	− 200	μA_{DC}	
	Digital Inputs > 2.0V		0.1	10	μA_{DC}	
t_S Current Settling Time	R_L = 100Ω, Output Settled to 0.01%, All Digital Inputs Switched Simultaneously		1		μs	

imply that the devices should be operated at these "Absolute Maximum" limits.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: This 500 mW specification applies for all packages. The low intrinsic power dissipation of this part (and the fact that there is no way to significantly modify the power dissipation) removes concern for heat sinking.

Note 4: Both I_{OUT1} and I_{OUT2} must go to ground or the virtual ground of an operational amplifier. The linearity error is degraded by approximately $V_{OS} \div V_{REF}$. For example, if $V_{REF} = 10V$ then a 1 mV offset, V_{OS}, on I_{OUT1} or I_{OUT2} will introduce an additional 0.01% linearity error.

Note 5: Guaranteed at $V_{REF} = \pm 10\ V_{DC}$ and $V_{REF} = \pm 1\ V_{DC}$.

Note 6: $T_{MIN} = -40°C$ and $T_{MAX} = 85°C$ for "LCD" suffix parts.

Note 7: The unit FSR stands for full-scale range. Linearity Error and Power Supply Rejection specs are based on this unit to eliminate dependence on a particular V_{REF} value to indicate the true performance of the part. The Linearity Error specification of the DAC1218 is 0.012% of FSR. This guarantees that after performing a zero and full-scale adjustment, the plot of the 4096 analog voltage outputs will each be within 0.012% × V_{REF} of a straight line which passes through zero and full-scale. The unit ppm of FSR (parts per million of full-scale range) and ppm of FS (parts per million of full-scale) are used for convenience to define specs of very small percentage values, typical of higher accuracy converters. 1 ppm of FSR = $V_{REF}/10^6$ is the conversion factor to provide an actual output voltage quantity. For example, the gain error tempco spec of ±6 ppm of FS/°C represents a worst-case full-scale gain error change with temperature from −40°C to +85°C of $\pm(6)(V_{REF}/10^6)(125°C)$ or $\pm 0.75\ (10^{-3})\ V_{REF}$ which is ±0.075% of V_{REF}.

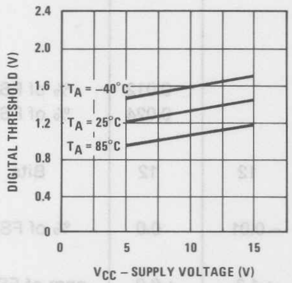
Note 8: To achieve this low feedthrough in the D package, the user must ground the metal lid. If the lid is left floating the feedthrough is typically 6 mV.

Note 9: Guaranteed by design but not tested.

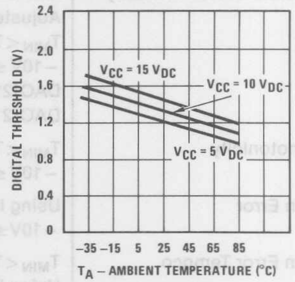
Note 10: A 10 nA leakage current with $R_{Fb} = 20k$ and $V_{REF} = 10V$ corresponds to a zero error of $(10 \times 10^{-9} \times 20 \times 10^3) \times 100\%$ 10V or 0.002% of FS.

Typical Performance Characteristics

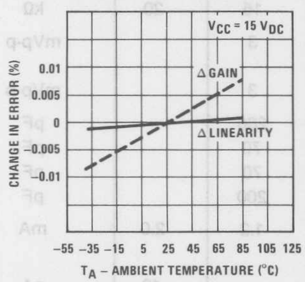
Digital Input Threshold vs V_{CC}



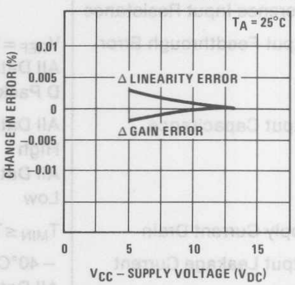
Digital Input Threshold vs Temperature



Gain and Linearity Error Variation vs Temperature



Gain and Linearity Error Variation vs Supply Voltage



Definition of Package Pinouts

A1 to A12: Digital Inputs. A12 is the least significant digital input (LSB) and A1 is the most significant digital input (MSB).

I_{OUT1}: DAC Current Output 1. I_{OUT1} is a maximum for a digital input of all 1s, and is zero for a digital input of all 0s.

I_{OUT2}: DAC Current Output 2. I_{OUT2} is a constant minus I_{OUT1}, or $I_{OUT1} + I_{OUT2}$ = constant (for a fixed reference voltage).

R_{Fb}: Feedback Resistor. The feedback resistor is provided on the IC chip for use as the shunt feedback resistor for the external op amp which is used to provide an output voltage for the DAC. This on-chip resistor should always be used (not an external resistor) since it matches the resistors which are used in the on-chip R-2R ladder and tracks these resistors over temperature.

V_{REF}: Reference Voltage Input. This input connects to an external precision voltage source to the internal R-2R ladder. V_{REF} can be selected over the range of 10V to −10V. This is also the analog voltage input for a 4-quadrant multiplying DAC application.

V_{CC}: Digital Supply Voltage. This is the power supply pin for the part. V_{CC} can be from 5 V_{DC} to 15 V_{DC}. Operation is optimum for 15 V_{DC}.

GND: Ground. This is the ground for the circuit.

Definition of Terms

Resolution: Resolution is defined as the reciprocal of the number of discrete steps in the DAC output. It is directly related to the number of switches or bits within the DAC. For example, the DAC1218 has 2^{12} or 4096 steps and therefore has 12-bit resolution.

Linearity Error: Linearity error is the maximum deviation from a *straight line passing through the endpoints of the DAC transfer characteristic.* It is measured after adjusting for zero and full-scale. Linearity error is a parameter intrinsic to the device and cannot be externally adjusted.

National's linearity test (a) and the best straight line test (b) used by other suppliers are illustrated below. The best straight line (b) requires a special zero and FS adjustment for each part, which is almost impossible for the user to determine. The end point test uses a standard zero FS adjustment procedure and is a much more stringent test for DAC linearity.

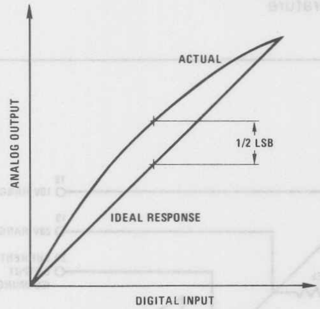
Power Supply Sensitivity: Power supply sensitivity is a measure of the effect of power supply changes on the DAC full-scale output.

Settling Time: Full-scale current settling time requires zero to full-scale or full-scale to zero output change. Settling time is the time required from a code transition until the DAC output reaches within ± 1/2 LSB of the final output value.

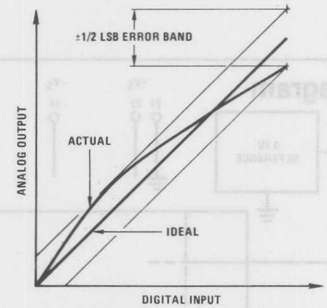
Full-Scale Error: Full-scale error is a measure of the output error between an ideal DAC and the actual device output. Ideally, for the DAC1218 full-scale is V_{REF}−1 LSB. For V_{REF} = 10V and unipolar operation, $V_{FULL\text{-}SCALE}$ = 10.0000V−2.44 mV = 9.9976V. Full-scale error is adjustable to zero.

Differential Non-Linearity: The difference between any two consecutive codes in the transfer curve from the theoretical 1 LSB is differential non-linearity.

Monotonic: If the output of a DAC increases for increasing digital input code, then the DAC is monotonic. A 12-bit DAC which is monotonic to 12 bits simply means that input increasing digital input codes will produce an increasing analog output.



a) End point test after zero and FS adjust



b) Shifting FS adjust to pass best straight line test

National Semiconductor

DAC1280A, DAC1280 12-Bit Digital-to-Analog Converters

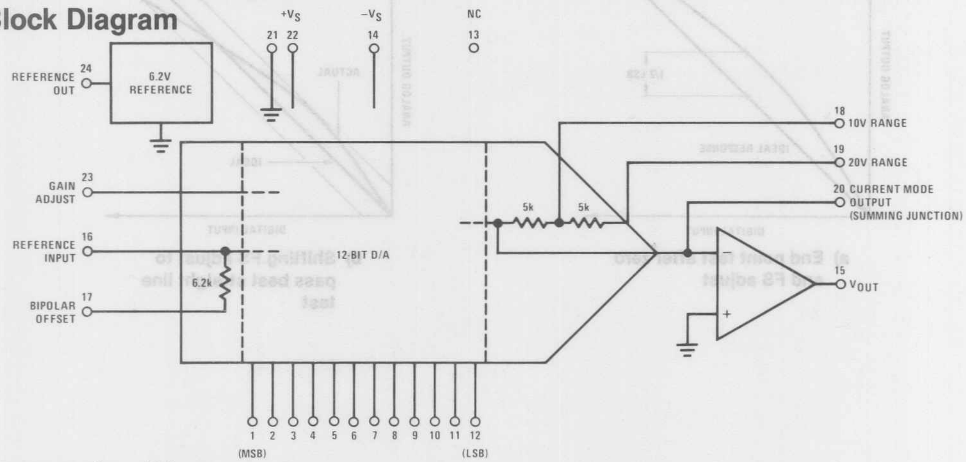
General Description

The DAC1280 series is a family of precision, low cost, fully self-contained digital-to-analog converters. The devices include 12 precision current switches, a 12-bit thin film resistor network, output amplifier, buffered internal reference, and several precision resistors, which allow the user to tailor his system needs to accommodate a variety of bipolar and unipolar output voltage and current ranges. Logic inputs are TTL, DTL and CMOS compatible, and are complementary binary (CBI) format. In all instances, a logic low (≤0.8V) turns a given bit ON, and a logic high (≥2V) turns a given bit OFF. Internally supplied resistor options provide low drift bipolar output voltage ranges of ±2.5V, ±5V, ±10V, and unipolar ranges of 0V to 5V or 0V to 10V. Current mode output is 0 mA to 2 mA.

Features

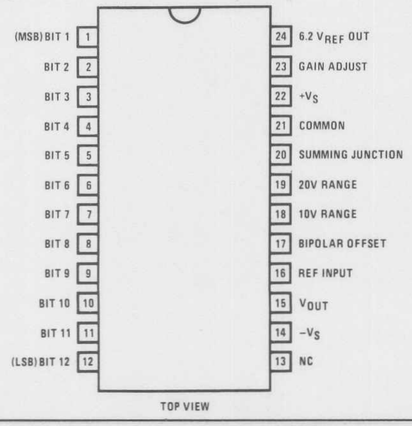
- Completely self-contained with internal reference and output amplifier
- High reliability exact replacement for DAC80-CBI-V or DAC80Z-CBI-V
- ±1/2 LSB linearity max over 0°C to 70°C temperature range for DAC1280A
- ±2.5V, ±5V, ±10V, 0V to 5V, 0V to 10V voltage outputs
- 0 mA to 2 mA current output
- Fast settling time: 300 ns current mode; 2.5 μs voltage mode
- Standard 24-pin IC package
- Low cost
- TTL CMOS compatible binary input logic over temperature

Block Diagram



Connection Diagram

Dual-In-Line Package



Order Number DAC1280ACD
See NS Package D24G

Absolute Maximum Ratings

Supply Voltage (V^+ and V^-)	± 18V
Current Output (Pin 20) Voltage Compliance	± 10V
Logic Input Voltage	− 0.7V, 10V
Reference Input Voltage (V_{REF})	0V, 18V
Short-Circuit Duration (Pins 15, 20 and 24)	Continuous
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	− 65°C to + 150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

$T_A = 0°C$ to 70°C, $V_S = \pm 11.4V$ to $\pm 15.75V$ for DAC1280A, $V_S = \pm 15V$ for DAC1280 unless otherwise noted.

Parameter	Conditions	DAC1280A Min	DAC1280A Typ (Note 1)	DAC1280A Max	DAC1280 Min	DAC1280 Typ (Note 1)	DAC1280 Max	Units
CONVERTER CHARACTERISTICS								
Resolution		12			12			Bits
Linearity Error	$T_A = 25°C$		± 1/4	± 1/2 ± 1/2		± 1/4	± 1 ± 2	LSB
Differential Non-Linearity			± 1/2	± 3/4		± 1/2		
Monotonicity		12			11	12		Bits
Full-Scale (Gain) Error	$T_A = 25°C$ (Note 2)		± 0.1	± 0.3		± 0.1		% FSR (Note 3)
Zero-Scale (Offset) Error	$T_A = 25°C$ (Note 2)		± 0.02	± 0.15		± 0.02		
Full-Scale (Gain) Tempco	Internal Reference External Constant Reference		± 15 ± 5	± 30 ± 7		± 15 ± 5		ppm/°C
Zero-Scale (Offset) Tempco	Unipolar Bipolar		± 1 ± 3	± 3 ± 10		± 1 ± 3		ppm FSR/°C
Total Bipolar Tempco (Note 4)	Includes Gain, Offset, and Linearity		± 10	± 20		± 10		
Total Error (Note 5)	Unipolar Bipolar		± 0.08 ± 0.06	± 0.15 ± 0.10		± 0.08 ± 0.06		% FSR
Output Voltage Range	Using Internally Supplied Resistors (Note 6)		± 2.5V, ± 5V, ± 10V, 0V to 5V, 0V to 10V					V
Output Voltage Swing	$R_L \geq 5\ k\Omega$, Pin 15	± 10			± 10			
Output Short Circuit Current	Pin 15	± 5	± 25	± 50	± 5	± 25	± 50	mA
Output Resistance	Pin 15, Closed Loop		0.05			0.05		Ω
Current Mode Output Range	Unipolar, Pin 20 Bipolar, Pin 20		0 to − 2 ± 1.0			0 to − 2 ± 1.0		mA
Current Mode Compliance				± 2.5			± 2.5	V
Current Mode Output Impedance	Unipolar Bipolar		2 1.5			2 1.5		kΩ
REFERENCE CHARACTERISTICS								
Reference Voltage	$I_{REF} \leq 2$ mA, $T_A = 25°C$	6.07	6.2	6.33		6.2		V
Tempco of Drift			± 10	± 20		± 10		ppm/°C
External Use Current				2.5			2.5	mA
Output Resistance			0.05	1.0		0.05	1.0	Ω

Parameter	Conditions	DAC1280A Min	DAC1280A Typ (Note 1)	DAC1280A Max	DAC1280 Min	DAC1280 Typ (Note 1)	DAC1280 Max	Units
DIGITAL AND DC CHARACTERISTICS								
Logic "1" Input Voltage (Bit OFF)		2.0			2.0			V
Logic "0" Input Voltage (Bit ON)				0.8			0.8	V
Logic "1" Input Current	$V_{IN} = 2.5V$		0.05	1		0.05	1	μA
Logic "0" Input Current	$V_{IN} = 0V$			−100			−100	μA
Power Supply Current	I^+, $T_A = 25°C$		10	18		10		mA
	I^-, $T_A = 25°C$		25	30		25		mA
Power Supply Sensitivity			0.001	0.002		0.001		% FSR/%V
AC CHARACTERISTICS								
Voltage Mode Settling Time	1 LSB Change		400			400		ns
	FSR Change 10V		2.5			2.5		μs
	FSR Change 20V		4			4		μs
Voltage Mode Slew Rate	$T_A = 25°C$	10	15			15		$V/\mu s$
Current Mode Settling Time	10Ω to 100Ω Load		300			300		ns

Note 1: All typical values are for $T_A = 25°C$.

Note 2: Externally adjustable to zero.

Note 3: FSR means "full-scale range" and is 20V for ± 10V range, 10V for ± 5V, etc.

Note 4: See paragraph 2.0 for definition.

Note 5: With gain and offset errors adjusted to zero at 25°C

Note 6: $\pm V_S$ must have absolute value 2V greater than V_{OUT}. Output voltage ranges −10V to +10V and 0V to +10V are not recommended with V_S less than 12V.

1.0 Definition of Terms

1.1 Accuracy

Accuracy of a D/A converter is the difference between the actual analog output that is measured when a given digital code is applied and the analog output that is expected with that code applied to the converter. Accuracy errors can be specified by the three parameters of gain or full-scale error, zero-scale or offset error, and linearity error.

1.2 Linearity Error

Linearity error is the maximum deviation from a *straight line passing through the endpoints of the DAC transfer characteristic.* It is measured after adjusting for zero and full-scale. Linearity error is a parameter intrinsic to the device and cannot be externally adjusted.

1.3 Differential Linearity Error and Monotonicity

Differential linearity error of a D/A converter is the deviation from an ideal 1 LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ± 1/2 LSB means that the output voltage step sizes can range from 1/2 LSB to 3/2 LSB when the input changes from one adjacent input state to the next. Monotonicity is guaranteed in the DAC1280A and DAC1280 to ensure that the analog output will not decrease with increasing input digital codes.

1.4 Gain Tempco

Gain tempco is a measure of the change in the full-scale range output over temperature expressed in parts per million per °C (ppm/°C).

1.5 Offset Tempco

Offset tempco is a measure of the actual change in output with all "1"s on the input over the specified temperature range. The offset is measured at 0°C, 25°C and 70°C. The maximum change in offset is referenced to the offset at 25°C and is divided by the temperature range. This offset change is expressed in parts per million of full-scale range per °C (ppm of FSR/°C).

1.6 Settling Time

Settling time for each DAC1280A or DAC1280 is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input *(Figures 1 and 2)*.

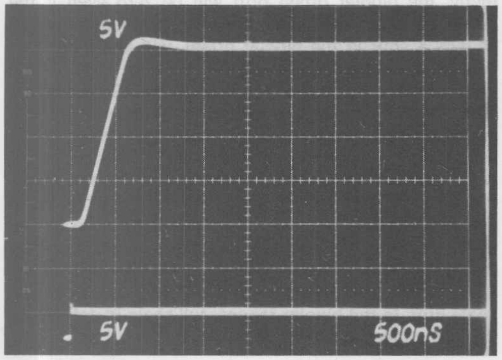


FIGURE 1. Voltage Mode Settling Time-FSR Change

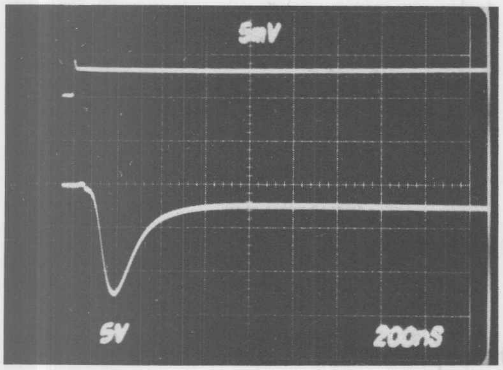


FIGURE 2. Voltage Mode Settling Time-1 LSB Change

Voltage Output. Three settling times are specified to ±0.01% of full-scale range (FSR); two for maximum full-scale range changes of 20V, 10V and one for a 1 LSB change. The 1 LSB change is measured at the major carry (0111...11 to 1000...00), the point at which the worst case settling time occurs.

Current Output. Settling time is specified to ±0.01% of FSR. This is given with a range of resistive loads: 10Ω to 100Ω.

1.7 Compliance

Compliance voltage is the maximum voltage swing allowed on the current output pin (pin 20). Note that the absolute current offset error with any DAC will be increased by an amount given by V_{OUT}/R_{OUT}. In many situations this will be a significant error term if the voltage on the current output pin is allowed to exceed a few millivolts.

1.8 Power Supply Sensitivity

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive, negative, or logic supplies about the nominal power supply voltages.

1.9 Reference Supply

The DAC1280A and DAC1280 are supplied with an internal 6.2V reference voltage supply. This voltage (pin 24) is accurate to ±2% and must be connected to the Reference Input (pin 16) for specified operation. This reference may also be used externally with external current drain limited to 2.5 mA. All gain adjustments should be made under constant load conditions.

2.0 Analyzing Device Accuracy Over the Temperature Range

For the purposes of temperature drift analysis, the major device components are shown in *Figure 3*. The reference element and buffer amplifier drifts are combined to give the total reference temperature coefficient, which is specified as ±20 ppm/°C maximum for the DAC1280A. The input reference current to the DAC, I_{REF}, is developed from the internal reference and will show the same drift rate as the reference voltage. The DAC output current, I_{DAC}, which is a function of the digital input code, is designed to track I_{REF}; if there is a slight mismatch in these currents over temperature, it will contribute to the gain TC. The bipolar offset resistor, R_{BP}, and gain setting resistor, R_{GAIN}, also have temperature coefficients which contribute to system drift errors. The input offset voltage drift of the output amplifier, OA, also contributes a small error.

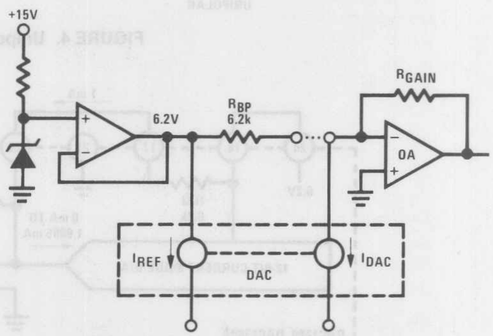


FIGURE 3. Bipolar Configuration

There are three types of drift errors over temperature: offset, gain, and linearity. Offset drift causes a vertical translation of the entire transfer curve; gain drift is a change in the slope of the curve; and linearity drift represents a change in the shape of the curve. The combination of these three drifts results in the complete specification for total error over temperature.

Total error is defined as the deviation from a true straight line transfer characteristic from exactly zero at a digital input which calls for zero output to a point which is defined as full-scale. A specification for total error over temperature assumes that both the zero and full-scale points have been trimmed for zero error at 25°C. Total error is normally expressed as a percentage of the full-scale range. In the bipolar situation, this means the total range from $-V_{FS}$ to $+V_{FS}$.

2.1 Monotonicity and Linearity

The initial linearity error and the differential linearity error guarantee monotonic performance over the range of 0°C to 70°C. It can therefore be assumed that linearity errors are insignificant in computation of total temperature errors.

2.2 Unipolar Errors

Temperature error analysis in the unipolar mode is straightforward: there is an offset drift and a gain drift. The offset drift, which comes from leakage currents and drift in the output amplifier, causes a linear shift in the transfer curve as shown in *Figure 4*. The gain drift causes a change in the slope of the curve and results from reference drift, DAC drift, and drift in R_{GAIN} relative to the DAC resistors.

2.3 Bipolar Range Errors

The analysis is slightly more complex in the bipolar mode. In this mode R_{BP} is connected to the summing node of the output amplifier (see *Figure 3*) to generate a current which exactly balances the current of the MSB so that the output voltage is zero with only the MSB on.

Note that if the DAC and application resistors track perfectly, the bipolar offset drift will be zero even if the reference drifts. A change in the reference voltage, which causes a shift in the bipolar offset, will also cause an equivalent change in I_{REF} and thus I_{DAC}, so that I_{DAC} will always be exactly balanced by I_{BP} with the MSB turned on. This effect is shown in *Figure 6.* The net effect of the reference drift then is simply to cause a rotation in the transfer around bipolar zero. However, consideration of second order effects (which are often overlooked) reveals the errors in the bipolar mode. The unipolar offset drifts discussed before will have the same effect on the bipolar offset. A mismatch of R_{BP} to the DAC resistors is usually the largest component of bipolar drift. Gain drift in the DAC also contributes to bipolar offset drift, as well as full-scale drift. In the bipolar ranges, full-scale is defined as the total range from $-V_{FS}$ to $+V_{FS}$.

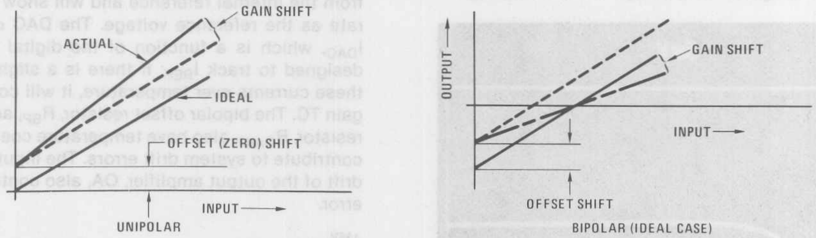
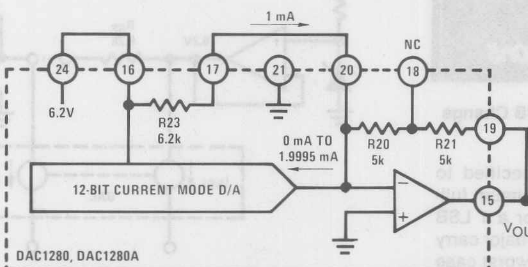
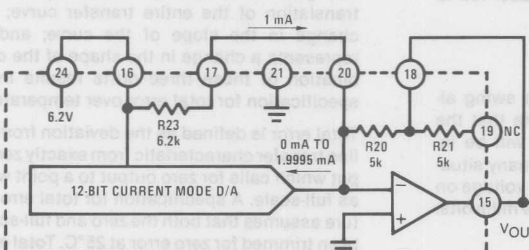


FIGURE 4. Unipolar and Bipolar Drifts



V_{OUT} = (0 mA to 1.9995 mA) (R20 + R21)–(6.2V/R23) (R21 + R22)
= (0 mA to 1.9995 mA) (10k)–(1 mA) (10k)
= −10V to +9.995V
1 LSB = 20V/4096 = 4.88 mV

FIGURE 5. ±10V Bipolar Operation



V_{OUT} = (0 mA to 1.9995 mA) (R20)–(R20/R23) (6.2V)
= (0 mA to 1.9995 mA) (5k)–(5k/6.2k) (6.2V)
= −5V to 4.9975V
1 LSB = 10V/4096 = 2.44 mV

FIGURE 6. ±5V Bipolar Operation

3.0 Applications and Functional Description

3.1 Voltage Mode Operation

The DAC1280A and DAC1280 D/As provide internal scaling resistors which permit a wide range of bipolar and unipolar output configurations. Bipolar output formats of ±2.5V, ±5V, ±10V and unipolar formats of 0V to 5V and 0V to 10V are possible using resistor strap options included within the device. Table I and *Figures 5, 6 and 7* summarize the proper pin connections required for these formats.

3.2 Current Mode Operation

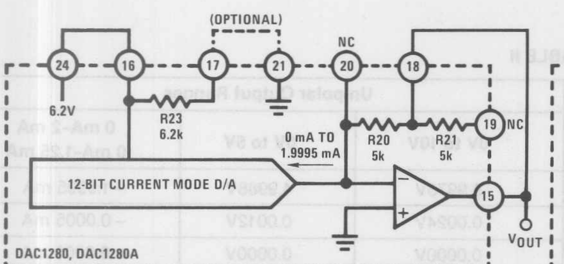
Current mode applications which make use of an external op amp, comparator, or a resistive load are possible with the DAC1280 series using pin 20. When an external op amp is used, the internal scaling resistors should be utilized to minimize full-scale drift. Configurations shown in Table I apply directly. *Figure 8* shows one application using an external fast operational amplifier.

Current mode operation into a resistive load or open circuit must account for the DACs nominal output resistance of 2k at pin 20. With this in mind, the output will swing 0V to −4V open circuit and about −1.5V to +1.5V with the bipolar offset resistor connected. An external load resistor may be used as part of the load, but there will be an error due to temperature coefficients mistracking.

TABLE I. Output Voltage/Current Ranges for DAC1280 Series

Output Voltage Range	Digital Input Code	Connect Pin 15 to	Connect Pin 16 to	Connect Pin 17 to	Connect Pin 19 to
±10V	Complementary Offset Binary	19	24	20	15
±5V	Complementary Offset Binary	18	24	20	NC
±2.5V	Complementary Offset Binary	18	24	20	20
10V	Complementary Binary	18	24	21*	NC
5V	Complementary Binary	18	24	21*	20
±1 mA	Complementary Offset Binary	NC	24	20	NC
−2 mA	Complementary Binary	NC	24	21*	NC

*Optional, no connection necessary



V_{OUT} = (0 mA to 1.9995 mA) (R20)
= (0 mA to 1.9995 mA) (5k)
= 0V to 9.9976V
1 LSB = 2.44 mV

FIGURE 7. 10V Unipolar Operation

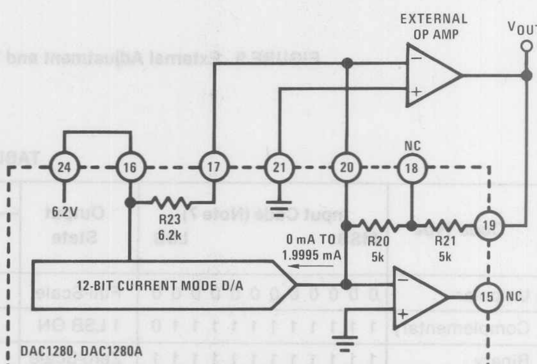


FIGURE 8. ±10V Bipolar Operation with External Operational Amplifier

using the circuit shown in *Figure 9*. Offset voltage should be adjusted first. A logic "1" (≥2V) should be applied to all logic inputs. In bipolar mode, the offset is adjusted to equal minus full-scale. In unipolar mode, the offset is adjusted to read 0V at the output. Full-scale is then adjusted by applying a logic "0" (≤0.8V) to all inputs for operation. The range of R1 and R2 shown in *Figure 9* is approximately ±0.2% of full-scale for the values shown.

A 30 second "warm-up" period should be allowed (after power turn-on) before making the above adjustments.

tary; i.e., a given bit is turned ON by an active low input. Table II summarizes input status for unipolar and bipolar codes.

3.5 Reference Supply

The DAC1280 series is supplied with an internal 6.2V reference regulator (pin 24). In order to obtain the specified unadjusted performance, the reference output (pin 24) should be connected to the reference input (pin 16). An external reference voltage may be used with the DAC1280 series if provision is made to calibrate full-scale as shown in *Figure 9*. Since the reference is buffered, it may be used externally at currents up to 2.5 mA.

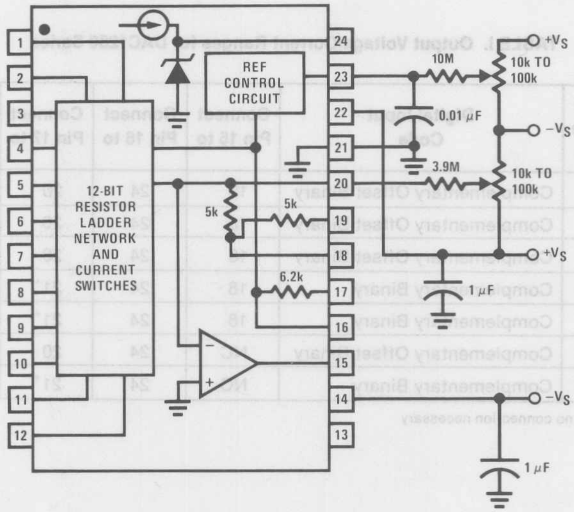


FIGURE 9. External Adjustment and Voltage Supply Connection Diagram

TABLE II

Code Type	Input Code (Note 7) MSB … LSB	Output State	Unipolar Output Ranges: 0V to 10V	0V to 5V	0 mA–2 mA / 0 mA–1.25 mA
Unipolar	0 0 0 0 0 0 0 0 0 0 0 0	Full-Scale	9.9976V	4.9988V	−1.9995 mA
Complementary	1 1 1 1 1 1 1 1 1 1 1 0	1 LSB ON	0.0024V	0.0012V	−0.0005 mA
Binary	1 1 1 1 1 1 1 1 1 1 1 1	Zero-Scale	0.0000V	0.0000V	0.0000 mA

Code Type	Input Code (Note 7) MSB … LSB	Output State	Bipolar Output Voltage Ranges: ±10V	±5V	±2.5V	±1 mA
Bipolar	0 0 0 0 0 0 0 0 0 0 0 0	Full-Scale	9.9951V	4.9976V	2.4988V	−0.9995 mA
Complementary	0 1 1 1 1 1 1 1 1 1 1 1	Half-Scale	0.0000V	0.0000V	0.0000V	0.0000 mA
Binary	1 1 1 1 1 1 1 1 1 1 1 0	1 LSB ON	−9.9951V	−4.9976V	−2.4988V	0.9995 mA
	1 1 1 1 1 1 1 1 1 1 1 1	Zero-Scale	−10.0000V	−5.0000V	−2.5000V	1.0000 mA

Note 7: Logic input sense is such that an active low ($V_{IN} \leq 0.8V$) turns a given bit ON and is represented as a logic "0" in the table.

3.6 Logic Input Compatibility

The design of the current mode switches in the DAC1280 series gives the device true TTL compatibility. It is TTL compatible over the entire operating temperature range and is independent of the reference voltage and V_{CC}. Furthermore, since the input breakdown ratings are in excess of 10V, the DAC1280 series may be driven directly from high (or low) voltage CMOS.

3.7 ±12 Volt Supply Operation

The DAC1280A will operate with supply voltages as low as ±11.4V. It is recommended that output voltage ranges −10V to +10V and 0V to 10V not be used with the DAC1280A if the supply voltages are ever less than the recommended ±12V. The output amplifier may saturate if $|V_{SUPPLY}| - |V_{OUT}\ \text{maximum}| < 2.0V$.

3.8 Power Supply Connections

For optimum performance power supply decoupling capacitors should be added as shown in the connection diagrams *(Figure 5)*. These capacitors (1 μF electrolytic recommended) should be located close to the DAC1280A or DAC1280. Electrolytic capacitors, if used, should be paralleled with 0.01 μF ceramic capacitors for optimum high frequency performance.

DAC1280A-I, DAC1280-I 12-Bit Digital-to-Analog Converters

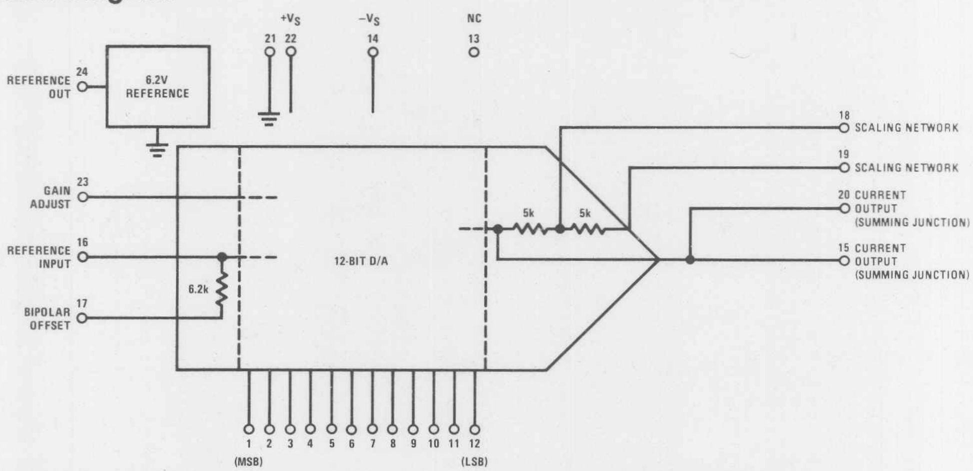
General Description

The DAC1280-I series is a family of precision, low cost, fully self-contained digital-to-analog converters. The devices include 12 precision current switches, a 12-bit thin film resistor network, buffered internal reference, and several precision resistors, which allow the user to tailor his system needs to accommodate a variety of bipolar and unipolar output voltage and current ranges. Logic inputs are TTL, DTL and CMOS compatible, and are complementary binary (CBI) format. In all instances, a logic low (≤0.8V) turns a given bit ON, and a logic high (≥2V) turns a given bit OFF. Internally supplied resistor options provide low drift bipolar output voltage ranges of ±2.5V, ±5V, ±10V, and unipolar ranges of 0V to 5V or 0V to 10V. Current mode output is 0 mA to 2 mA.

Features

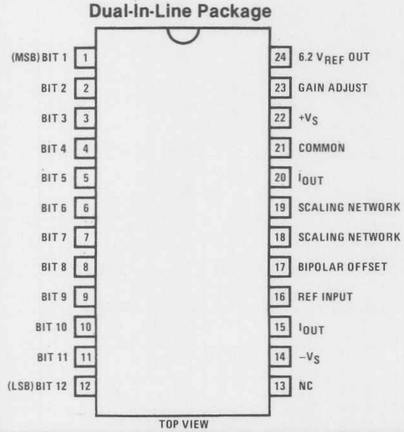
- Self-contained with internal reference
- High reliability replacement for DAC80-CBI-I or DAC80Z-CBI-I
- ±1/2 LSB linearity max over 0°C to 70°C temperature range for DAC1280A-I
- ±2.5V, ±5V, ±10V, 0V to 5V, 0V to 10V output voltage ranges with external op amp
- 0 mA to 2 mA current output
- Fast settling time: 300 ns current
- Standard 24-pin IC package
- Low cost
- TTL CMOS compatible binary input logic over temperature

Block Diagram



Connection Diagram

Dual-In-Line Package



Ordering Information

Temperature Range		0°C to 70°C
Linearity	0.01%	DAC1280AD-I (DAC80Z-CBI-I)
	0.05%	DAC1280HCD-I
Package		D24G

Absolute Maximum Ratings

Supply Voltage (V^+ and V^-)	± 18V
Current Output (Pins 15, 20) Voltage Compliance	± 10V
Logic Input Voltage	− 0.7V, 10V
Reference Input Voltage (V_{REF})	0V, 18V
Short-Circuit Duration (Pins 15, 20 and 24)	Continuous
Operating Temperature Range	− 25°C to + 85°C
Storage Temperature Range	− 65°C to + 150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

$T_A = 0°C$ to 70°C, $V_S = \pm 11.4V$ to $\pm 15.75V$ for DAC1280A-I, $V_S \geq \pm 15V$ for DAC1280-I unless otherwise noted.

Parameter	Conditions	DAC1280A-I Min	DAC1280A-I Typ (Note 1)	DAC1280A-I Max	DAC1280-I Min	DAC1280-I Typ (Note 1)	DAC1280-I Max	Units
CONVERTER CHARACTERISTICS								
Resolution		12			12			Bits
Linearity Error	$T_A = 25°C$		± 1/4	± 1/2		± 1/4	± 1	LSB
				± 1/2			± 2	
Differential Non-Linearity			± 1/2	± 3/4		± 1/2		
Monotonicity		12			11	12		Bits
Full-Scale (Gain) Error	$T_A = 25°C$ (Note 2)		± 0.1	± 0.3		± 0.1		% FSR (Note 3)
Zero-Scale (Offset) Error	$T_A = 25°C$ (Note 2)		± 0.02	± 0.15		± 0.02		
Full-Scale (Gain) Tempco	Internal Reference		± 15	± 30		± 15		ppm FSR/°C
	External Constant Reference		± 5	± 7		± 5		
Zero-Scale (Offset) Tempco	Unipolar		± 1	± 3		± 1		
	Bipolar		± 3	± 10		± 3		
Total Bipolar Tempco (Note 4)	Includes Gain, Offset, and Linearity		± 10	± 20		± 10		
Total Error (Note 5)	Unipolar		± 0.08	± 0.15		± 0.08		% FSR
	Bipolar		± 0.06	± 0.10		± 0.06		
Output Voltage Range	Using Internally Supplied Resistors, External Op Amp	± 2.5V, ± 5V, ± 10V, 0V to 5V, 0V to 10V						V
Current Mode Output Range	Unipolar, Pin 15		0 to − 2			0 to − 2		mA
	Bipolar, Pin 15		± 1.0			± 1.0		
Current Mode Compliance				± 2.5		± 2.5		V
Current Mode Output Impedance	Unipolar		2			2		kΩ
	Bipolar		1.5			1.5		
REFERENCE CHARACTERISTICS								
Reference Voltage	$I_{REF} \leq 2$ mA, $T_A = 25°C$	6.07	6.2	6.33		6.2		V
Tempco of Drift			± 10	± 20		± 10		ppm/°C
External Use Current				2.5			2.5	mA
Output Resistance			0.05	1.0		0.05	1.0	Ω

Parameter	Conditions	DAC1280A-I Min	DAC1280A-I Typ (Note 1)	DAC1280A-I Max	DAC1280-I Min	DAC1280-I Typ (Note 1)	DAC1280-I Max	Units
DIGITAL AND DC CHARACTERISTICS								
Logic "1" Input Voltage (Bit OFF)		2.0			2.0			V
Logic "0" Input Voltage (Bit ON)				0.8			0.8	V
Logic "1" Input Current	$V_{IN} = 2.5V$		0.05	1		0.05	1	μA
Logic "0" Input Current	$V_{IN} = 0V$			−100			−100	μA
Power Supply Current	I^+, $T_A = 25°C$ I^-, $T_A = 25°C$		10 25	18 30		10 25		mA
Power Supply Sensitivity			0.001	0.002		0.001		% FSR/%V
AC CHARACTERISTICS								
Current Mode Settling Time	10Ω to 100Ω Load		300			300		ns

Note 1: All typical values are for $T_A = 25°C$.

Note 2: Externally adjustable to zero.

Note 3: FSR means full-scale range and is 20V for ± 10V range, 10V for ± 5V, etc.

Note 4: See paragraph 1.6 for definition.

Note 5: With gain and offset errors adjusted to zero at 25°C.

1.0 Definition of Terms

1.1 ACCURACY

Accuracy of a D/A converter is the difference between the actual analog output that is measured when a given digital code is applied and the analog output that is expected with that code applied to the converter. Accuracy errors can be specified by the three parameters of gain or full-scale error, zero-scale or offset error, and linearity error.

1.2 LINEARITY ERROR

Linearity error is the maximum deviation from a *straight line passing through the endpoints of the DAC transfer characteristic.* It is measured after adjusting for zero and full-scale. Linearity error is a parameter intrinsic to the device and cannot be externally adjusted.

1.3 DIFFERENTIAL LINEARITY ERROR AND MONOTONICITY

Differential linearity error of a D/A converter is the deviation from an ideal 1 LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ± 1/2 LSB means that the output voltage step sizes can range from 1/2 LSB to 3/2 LSB when the input changes from one adjacent input state to the next. Monotonicity is guaranteed in the DAC1280A-I and DAC1280-I to ensure that the analog output will not decrease with increasing input digital codes.

1.4 GAIN TEMPCO

Gain tempco is a measure of the change in the full-scale range output over temperature expressed in parts per million per °C (ppm/°C). This test uses the internally supplied DAC, feedback and offset resistors.

1.5 OFFSET TEMPCO

Offset tempco is a measure of the actual change in output with all "1"s on the input over the specified temperature range. The offset is measured at 0°C, 25°C and 70°C. The maximum change in offset is referenced to the offset at 25°C and is divided by the temperature range. This offset change is expressed in parts per million of full-scale range per °C (ppm of FSR/°C).

1.6 TOTAL BIPOLAR TEMPCO

In the bipolar mode, the internal 6.2 kΩ resistor is connected to the current output pin which is the summing junction of the output amplifier (external). This resistor injects a current that exactly balances the output current of the DAC with only the MSB ON such that the output voltage of the amplifier is 0V.

If the internal resistors track perfectly, the cancellation effect is also perfect, even if the reference voltage drifts. Thus, any imperfection in resistor tracking gives rise to an error term.

The total bipolar mode tempco includes this tracking tempco as well as offset tempco and linearity tempco as defined above.

2.0 Functional Description

2.1 OFFSET AND FULL-SCALE ADJUST

The DAC1280-I series may be offset and full-scale adjusted using the circuit shown in *Figure 1*. Offset voltage should be adjusted first. A logic "1" (≥ 2V) should be applied to all logic inputs. In bipolar mode, the offset is adjusted to

equal minus full-scale. In unipolar mode, the offset is adjusted to read 0V at the output. Full-scale is then adjusted by applying a logic "0" (≤0.8V) to all inputs for operation. The range of adjustment shown in *Figure 1* is approximately ±0.2% of full-scale for the values shown.

A 30 second "warm-up" period should be allowed (after power turn-on) before making the above adjustments.

2.2 LOGIC INPUT CODING

The logic inputs to the DAC1280-I series are complementary; i.e., a given bit is turned ON by an active low input. Table I summarizes input status for unipolar and bipolar codes.

2.3 REFERENCE SUPPLY

The DAC1280-I series is supplied with an internal 6.2V reference regulator (pin 24). In order to obtain the specified unadjusted performance, the reference output (pin 24) should be connected to the reference input (pin 16). An external reference voltage may be used with the DAC1280-I series if provision is made to calibrate full-scale as shown in *Figure 1*. Since the reference is buffered, it may be used externally at currents up to 2.5 mA.

2.4 LOGIC INPUT COMPATIBILITY

The design of the current mode switches in the DAC1280-I series gives the device true TTL compatibility. It is TTL compatible over the entire operating temperature range and is independent of the reference voltage and V_{CC}. Furthermore, since the input breakdown ratings are in excess of 10V, the DAC1280-I series may be driven directly from high (or low) voltage CMOS.

2.5 ±12 VOLT SUPPLY OPERATION

The DAC1280A-I will operate with supply voltages as low as ±11.4V.

2.6 PIN 20 USAGE

Pin 20 is internally connected to pin 15; either may be used as the current output. Standard DAC80-CBI-I devices use pin 20 as an alternate feedback resistor tap; this tap is not available on the DAC1280A-I series.

2.7 POWER SUPPLY CONNECTIONS

For optimum performance power supply decoupling capacitors should be added as shown in the connection diagram. These capacitors (1 μF electrolytic recommended) should be located close to the DAC1280A-I or DAC1280-I. Electrolytic capacitors, if used, should be paralleled with 0.01 μF ceramic capacitors for optimum high frequency performance.

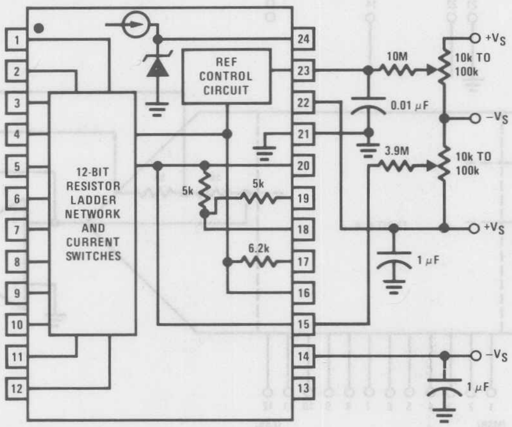


FIGURE 1. External Adjustment and Voltage Supply Connection Diagram

TABLE I

Code Type	Input Code (Note 6) MSB LSB	Output State	Unipolar Output Ranges 0 mA–2 mA 0 mA–1.25 mA
Unipolar	0 0 0 0 0 0 0 0 0 0 0 0	Full-Scale	−1.9995 mA
Complementary	1 1 1 1 1 1 1 1 1 1 1 0	1 LSB ON	−0.0005 mA
Binary	1 1 1 1 1 1 1 1 1 1 1 1	Zero-Scale	0.0000 mA
Code Type	**Input Code (Note 6) MSB LSB**	**Output State**	**Bipolar Output Ranges ±1 mA**
Bipolar	0 0 0 0 0 0 0 0 0 0 0 0	Full-Scale	−0.9995 mA
Complementary	0 1 1 1 1 1 1 1 1 1 1 1	Half-Scale	0.0000 mA
Binary	1 1 1 1 1 1 1 1 1 1 1 0	1 LSB ON	0.9995 mA
	1 1 1 1 1 1 1 1 1 1 1 1	Zero-Scale	1.0000 mA

Note 6: Logic input sense is such that an active low (V_{IN}≤0.8V) turns a given bit ON and is represented as a logic "0" in the table.

National Semiconductor

DAC1285A, DAC1285 (DAC85, DAC87) 12-Bit Digital-to-Analog Converters

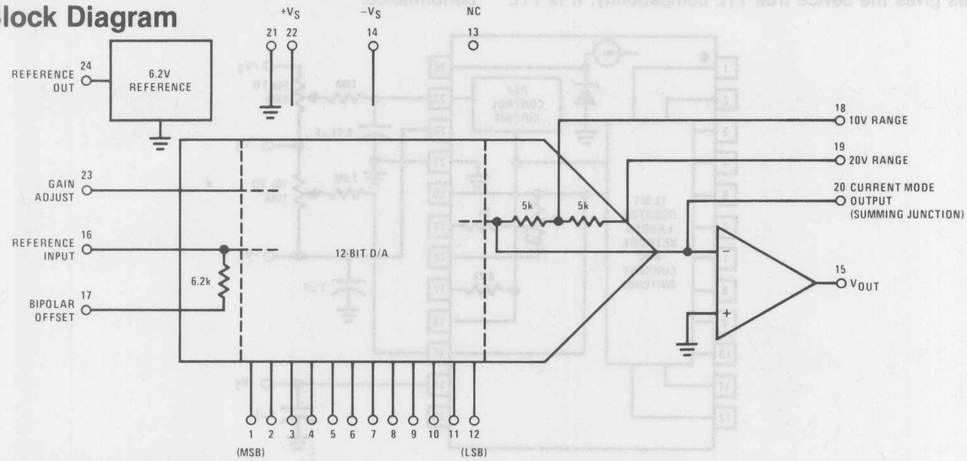
General Description

The DAC1285 series is a family of precision, low cost, fully self-contained digital-to-analog converters. The devices include 12 precision current switches, a 12-bit thin film resistor network, output amplifier, buffered internal reference, and several precision resistors, which allow the user to tailor his system needs to accommodate a variety of bipolar and unipolar output voltage and current ranges. Logic inputs are TTL, DTL and CMOS compatible, and are complementary binary (CBI) format. In all instances, a logic low (≤0.8V) turns a given bit ON, and a logic high (≥2V) turns a given bit OFF. Internally supplied resistor options provide low drift bipolar output voltage ranges of ±2.5V, ±5V, ±10V, and unipolar ranges of 0V to 5V or 0V to 10V. Current mode output is 0 mA to 2 mA.

Features

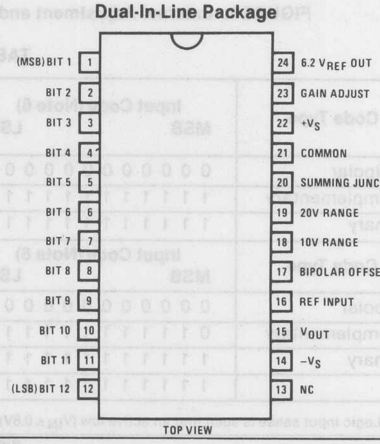
- Completely self-contained with internal reference and output amplifier
- High reliability exact replacement for DAC85-CBI-V, DAC85LD-CBI-V, and DAC87-CBI-V
- ±1/2 LSB linearity max over temperature range
- ±2.5V, ±5V, ±10V, 0V to 5V, 0V to 10V voltage outputs
- 0 mA to 2 mA current output
- Fast settling time: 300 ns current mode; 2.5 μs voltage mode
- Hermetic 24-pin IC package
- Low cost
- TTL CMOS compatible binary input logic over temperature
- Parameters guaranteed over operating temperature range −25°C to +85°C or −55°C to +125°C

Block Diagram



Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DAC1285ACD, DAC85LD-CBI-V, DAC1285HCD, DAC85-CBI-V, DAC1285AD or DAC87-CBI-V
See NS Package D24G

Absolute Maximum Ratings

Supply Voltage (V^+ and V^-)	±18V
Current Output (Pin 20) Compliance	±10V
Logic Input Voltage	−0.7V, 10V
Reference Input Voltage (V_{REF})	0V, 18V
Short-Circuit Duration (Pins 15, 20 and 24)	Continuous
Operating Temperature Range	
DAC1285A	−55°C to +125°C
DAC1285AC	−25°C to +85°C
DAC1285HC	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

$T_A = -55°C$ to $+125°C$ for DAC1285A and $-25°C$ to $+85°C$ for DAC1285AC and DAC1285HC, $V_S = \pm 11.4V$ to $\pm 15.75V$ for DAC1285A and DAC1285AC and $V_S = \pm 15V$ for DAC1285HC unless otherwise noted.

Parameter	Conditions	DAC1285A			DAC1285AC			DAC1285HC			Units
		Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
CONVERTER CHARACTERISTICS											
Resolution		12			12			12			Bits
Linearity Error	$T_A = 25°C$		±1/4	±1/2		±1/4	±1/2		±1/4	±1/2	LSB
				±3/4			±1/2			±1/2	
Differential Non-Linearity	$T_A = 25°C$		±1/2	±3/4		±1/2			±1/2		
				±1							
Monotonicity		12			12			12			Bits
Full-Scale (Gain) Error	$T_A = 25°C$ (Note 2)		±0.1	±0.2		±0.1			±0.1		% FSR (Note 3)
Zero-Scale (Offset) Error	$T_A = 25°C$ (Note 2)		±0.02	±0.1		±0.02			±0.02		
Full-Scale (Gain) Tempco	With Internal Reference		±10	±20		±10			±15	±30	ppm/°C
	Without Internal Reference		±5	±10		±5	±10		±5	±20	
Zero-Scale (Offset) Tempco	Unipolar		±1	±3		±1			±1		ppm FSR/°C
	Bipolar		±3	±10		±3	±5		±3	±10	
Total Bipolar Tempco (Note 4)	Includes Gain, Offset, and Linearity		±10	±30		±10			±10		
Total Error (Note 5)	Unipolar		±0.08	±0.3		±0.08			±0.08		% FSR
	Bipolar		±0.06	±0.24		±0.06			±0.06		
Output Voltage Range	Using Internally Supplied Resistors (Note 6)	±2.5V, ±5V, ±10V, 0V to 5V, 0V to 10V									V
Output Voltage Swing	$R_L \geq 5$ kΩ, Pin 15	±10			±10			±10			
Output Short Circuit Current	Pin 15	±5	±25	±50	±5	±25	±50	±5	±25	±50	mA
Output Impedance	Pin 15, Closed Loop		0.05			0.05			0.05		Ω
Current Mode Output Range	Unipolar, Pin 20		0 to −2			0 to −2			0 to −2		mA
	Bipolar, Pin 20		±1.0			±1.0			±1.0		
Current Mode Compliance				±2.5			±2.5			±2.5	V
Current Mode Output Impedance	Unipolar		2			2			2		kΩ
	Bipolar		1.5			1.5			1.5		
REFERENCE CHARACTERISTICS											
Reference Voltage	$I_{REF} \leq 2$ mA, $T_A = 25°C$	6.07	6.2	6.33	6.07	6.2	6.33		6.2		V
Tempco of Drift			±5	±10		±10	±20		±10	±20	ppm/°C
External Use Current				2.5			2.5			2.5	mA
Output Impedance			0.05	1.0		0.05	1.0		0.05	1.0	Ω

for DAC1285A and DAC1285AC and $V_S = \pm 15V$ for DAC1285HC unless otherwise noted.

Parameter	Conditions	DAC1285A, DAC1285AC			DAC1285HC			Units
		Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
DIGITAL AND DC CHARACTERISTICS								
Logic "1" Input Voltage (Bit OFF)		2.0			2.0			V
Logic "0" Input Voltage (Bit ON)				0.8			0.8	V
Logic "1" Input Current	$V_{IN} = 2.5V$		0.05	1		0.05	1	μA
Logic "0" Input Current	$V_{IN} = 0V$			−100			−100	μA
Power Supply Current	I^+, $T_A = 25°C$		10	18		10		mA
	I^-, $T_A = 25°C$		25	30		25		mA
Power Supply Sensitivity			0.001	0.002		0.001		% FSR/%V
AC CHARACTERISTICS								
Voltage Mode Settling Time	1 LSB Change		400			400		ns
	FSR Change 10V		2.5			2.5		μs
	FSR Change 20V		4			4		μs
Voltage Mode Slew Rate	$T_A = 25°C$	10	30			30		V/μs
Current Mode Settling Time	10Ω to 100Ω Load		300			300		ns

Note 1: All typical values are for $T_A = 25°C$.

Note 2: Externally adjustable to zero.

Note 3: FSR means "full-scale range" and is 20V for ±10V range, 10V for ±5V, etc.

Note 4: See paragraph 2.0 for definition.

Note 5: With gain and offset errors adjusted to zero at 25°C

Note 6: $\pm V_S$ must have absolute value 2V greater than V_{OUT}. Output voltage ranges −10V to +10V and 0V to +10V are not recommended with V_S less than ±12V.

1.0 Definition of Terms

1.1 Accuracy

Accuracy of a D/A converter is the difference between the actual analog output that is measured when a given digital code is applied and the analog output that is expected with that code applied to the converter. Accuracy errors can be specified by the three parameters of gain or full-scale error, zero-scale or offset error, and linearity error.

1.2 Linearity Error

Linearity error is the maximum deviation from a *straight line passing through the endpoints of the DAC transfer characteristic*. It is measured after adjusting for zero and full-scale. Linearity error is a parameter intrinsic to the device and cannot be externally adjusted.

1.3 Differential Linearity Error and Monotonicity

Differential linearity error of a D/A converter is the deviation from an ideal 1 LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2 LSB means that the output voltage step sizes can range from 1/2 LSB to 3/2 LSB when the input changes from one adjacent input state to the next. 12-bit monotonicity is guaranteed to ensure that the analog output will not decrease with increasing input digital codes.

1.4 Gain Tempco

Gain tempco is a measure of the change in the full-scale range output over temperature expressed in parts per million per °C (ppm/°C).

1.5 Offset Tempco

Offset tempco is a measure of the actual change in output with all "1"s on the input over the specified temperature range. The offset is measured at low and high temperature. The maximum change in offset is referenced to the offset at 25°C and is divided by the temperature range. This offset change is expressed in parts per million of full-scale range per °C (ppm of FSR/°C).

1.6 Settling Time

Settling time for each DAC1285 series part is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (*Figures 1 and 2*).

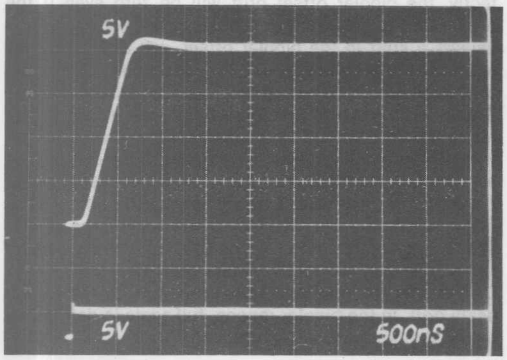


FIGURE 1. Voltage Mode Settling Time–FSR Change

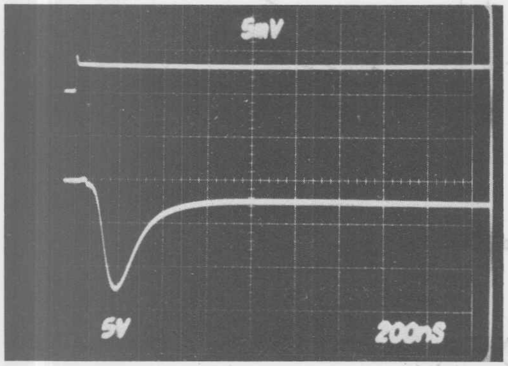


FIGURE 2. Voltage Mode Settling Time–1 LSB Change

Voltage Output. Three settling times are specified to ±0.01% of full-scale range (FSR); two for maximum full-scale range changes of 20V, 10V and one for a 1 LSB change. The 1 LSB change is measured at the major carry (0111...11 to 1000...00), the point at which the worst case settling time occurs.

Current Output. Settling time is specified to ±0.01% of FSR. This is given with a range of resistive loads: 10Ω to 100Ω.

1.7 Compliance

Compliance voltage is the maximum voltage swing allowed on the current output pin (pin 20). Note that the absolute current offset error with any DAC will be increased by an amount given by V_{OUT}/R_{OUT}. In many situations this will be a significant error term if the voltage on the current output pin is allowed to exceed a few millivolts.

1.8 Power Supply Sensitivity

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive, negative, or logic supplies about the nominal power supply voltages.

1.9 Reference Supply

The DAC1285 series are supplied with an internal 6.2V reference voltage supply. This voltage (pin 24) is accurate to ±2% and must be connected to the Reference Input (pin 16) for specified operation. This reference may also be used externally with external current drain limited to 2.5 mA. All gain adjustments should be made under constant load conditions.

2.0 Analyzing Device Accuracy Over the Temperature Range

For the purposes of temperature drift analysis, the major device components are shown in *Figure 3*. The reference element and buffer amplifier drifts are combined to give the total reference temperature coefficient, which is specified as a maximum. The input reference current to the DAC, I_{REF}, is developed from the internal reference and will show the same drift rate as the reference voltage. The DAC output current, I_{DAC}, which is a function of the digital input code, is designed to track I_{REF}; if there is a slight mismatch in these currents over temperature, it will contribute to the gain TC. The bipolar offset resistor, R_{BP}, and gain setting resistor, R_{GAIN}, also have temperature coefficients which contribute to system drift errors. The input offset voltage drift of the output amplifier, OA, also contributes a small error.

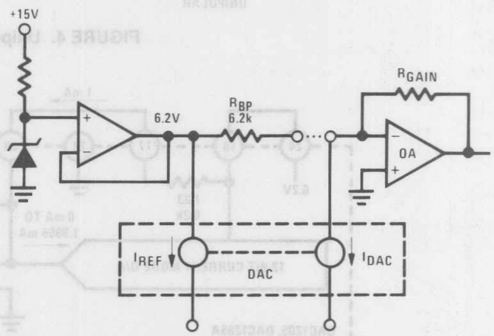


FIGURE 3. Bipolar Configuration

There are three types of drift errors over temperature: offset, gain, and linearity. Offset drift causes a vertical translation of the entire transfer curve; gain drift is a change in the slope of the curve; and linearity drift represents a change in the shape of the curve. The combination of these three drifts results in the complete specification for total error over temperature.

Total error is defined as the deviation from a true straight line transfer characteristic from exactly zero at a digital input which calls for zero output to a point which is defined as full-scale. A specification for total error over temperature assumes that both the zero and full-scale points have been trimmed for zero error at 25°C. Total error is normally expressed as a percentage of the full-scale range. In the bipolar situation, this means the total range from $-V_{FS}$ to $+V_{FS}$.

2.1 Monotonicity and Linearity

The initial linearity error and the differential linearity error guarantee monotonic performance over the operating temperature range. It can therefore be assumed that linearity errors are insignificant in computation of total temperature errors.

2.2 Unipolar Errors

Temperature error analysis in the unipolar mode is straightforward: there is an offset drift and a gain drift. The offset drift, which comes from leakage currents and drift in the output amplifier, causes a linear shift in the transfer curve as shown in *Figure 4*. The gain drift causes a change in the slope of the curve and results from reference drift, DAC drift, and drift in R_{GAIN} relative to the DAC resistors.

2.3 Bipolar Range Errors

The analysis is slightly more complex in the bipolar mode. In this mode R_{BP} is connected to the summing node of the output amplifier (see *Figure 3*) to generate a current which exactly balances the current of the MSB so that the output voltage is zero with only the MSB on.

Note that if the DAC and application resistors track perfectly, the bipolar offset drift will be zero even if the reference drifts. A change in the reference voltage, which causes a shift in the bipolar offset, will also cause an equivalent change in I_{REF} and thus I_{DAC}, so that I_{DAC} will always be exactly balanced by I_{BP} with the MSB turned on. This effect is shown in *Figure 6.* The net effect of the reference drift then is simply to cause a rotation in the transfer around bipolar zero. However, consideration of second order effects (which are often overlooked) reveals the errors in the bipolar mode. The unipolar offset drifts discussed before will have the same effect on the bipolar offset. A mismatch of R_{BP} to the DAC resistors is usually the largest component of bipolar drift. Gain drift in the DAC also contributes to bipolar offset drift, as well as full-scale drift. In the bipolar ranges, full-scale is defined as the total range from $-V_{FS}$ to $+V_{FS}$.

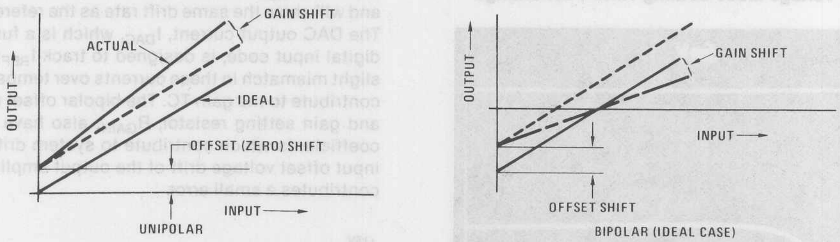
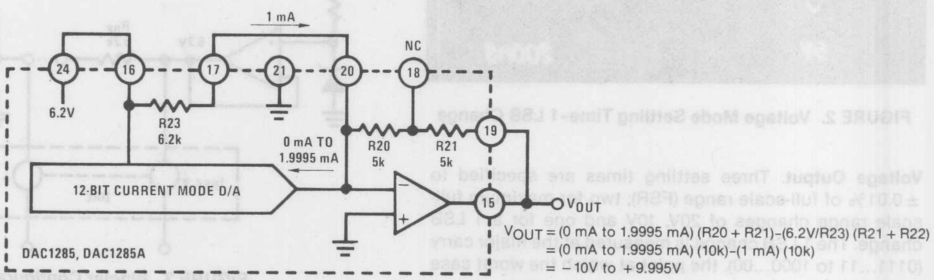


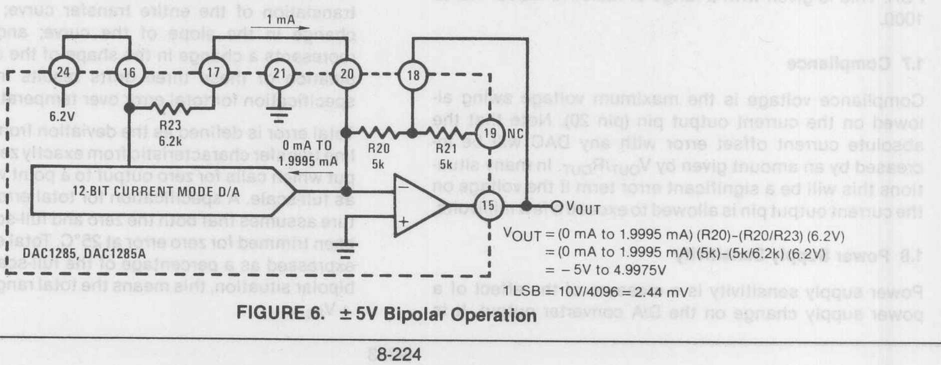
FIGURE 4. Unipolar and Bipolar Drifts



V_{OUT} = (0 mA to 1.9995 mA) (R20 + R21)-(6.2V/R23) (R21 + R22)
= (0 mA to 1.9995 mA) (10k)-(1 mA) (10k)
= −10V to +9.995V

1 LSB = 20V/4096 = 4.88 mV

FIGURE 5. ±10V Bipolar Operation



V_{OUT} = (0 mA to 1.9995 mA) (R20)-(R20/R23) (6.2V)
= (0 mA to 1.9995 mA) (5k)-(5k/6.2k) (6.2V)
= −5V to 4.9975V

1 LSB = 10V/4096 = 2.44 mV

FIGURE 6. ±5V Bipolar Operation

3.0 Applications and Functional Description

3.1 Voltage Mode Operation

These D/As provide internal scaling resistors which permit a wide range of bipolar and unipolar output configurations. Bipolar output formats of ± 2.5V, ± 5V, ± 10V and unipolar formats of 0V to 5V and 0V to 10V are possible using resistor strap options included within the device. Table I and *Figures 5, 6 and 7* summarize the proper pin connections required for these formats.

3.2 Current Mode Operation

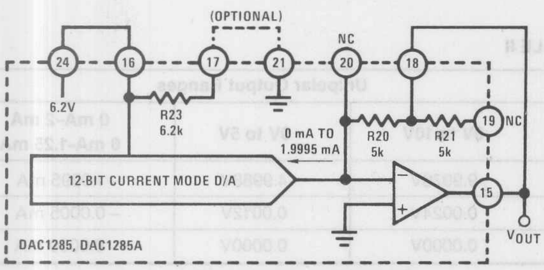
Current mode applications which make use of an external op amp, comparator, or a resistive load are possible with the DAC1285 series using pin 20. When an external op amp is used, the internal scaling resistors should be utilized to minimize full-scale drift. Configurations shown in Table I apply directly. *Figure 8* shows one application using an external fast operational amplifier.

Current mode operation into a resistive load or open circuit must account for the DACs nominal output resistance of 2k at pin 20. With this in mind, the output will swing 0V to − 4V open circuit and about − 1.5V to + 1.5V with the bipolar offset resistor connected. An external load resistor may be used as part of the load, but there will be an error due to temperature coefficients mistracking.

TABLE I. Output Voltage/Current Ranges for DAC1285 Series

Output Range	Digital Input Code	Connect Pin 15 to	Connect Pin 16 to	Connect Pin 17 to	Connect Pin 19 to
± 10V	Complementary Offset Binary	19	24	20	15
± 5V	Complementary Offset Binary	18	24	20	NC
± 2.5V	Complementary Offset Binary	18	24	20	20
10V	Complementary Binary	18	24	21*	NC
5V	Complementary Binary	18	24	21*	20
± 1 mA	Complementary Offset Binary	NC	24	20	NC
− 2 mA	Complementary Binary	NC	24	21*	NC

*Optional, no connection necessary



V_{OUT} = (0 mA to 1.9995 mA) (R20)
= (0 mA to 1.9995 mA) (5k)
= 0V to 9.9976V
1 LSB = 2.44 mV

FIGURE 7. 10V Unipolar Operation

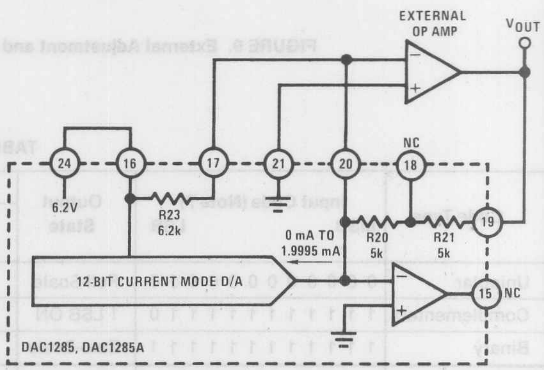


FIGURE 8. ± 10V Bipolar Operation with External Operational Amplifier

logic inputs. In bipolar mode, the offset is adjusted to equal minus full-scale. In unipolar mode, the offset is adjusted to read 0V at the output. Full-scale is then adjusted by applying a logic "0" (≤0.8V) to all inputs for operation. The range of R1 and R2 shown in *Figure 9* is approximately ±0.2% of full-scale for the values shown.

A 30 second "warm-up" period should be allowed (after power turn-on) before making the above adjustments.

codes.

3.5 Reference Supply

The DAC1285 series is supplied with an internal 6.2V reference regulator (pin 24). In order to obtain the specified unadjusted performance, the reference output (pin 24) should be connected to the reference input (pin 16). An external reference voltage may be used with the DAC1285 series if provision is made to calibrate full-scale as shown in *Figure 9*. Since the reference is buffered, it may be used externally at currents up to 2.5 mA.

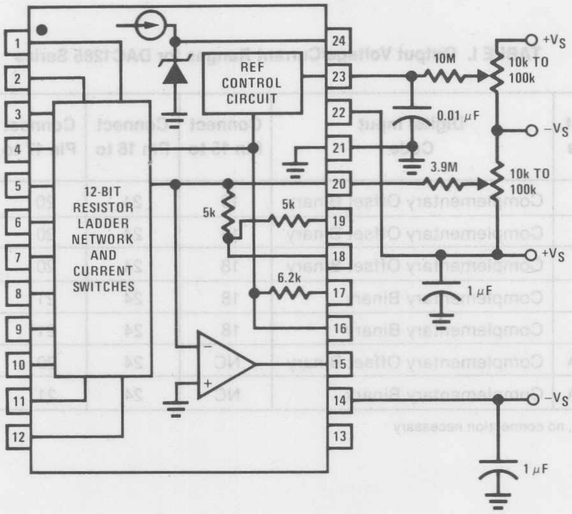


FIGURE 9. External Adjustment and Voltage Supply Connection Diagram

TABLE II

Code Type	Input Code (Note 7) MSB … LSB	Output State	Unipolar Output Ranges 0V to 10V	0V to 5V	0 mA–2 mA / 0 mA–1.25 mA
Unipolar	0 0 0 0 0 0 0 0 0 0 0 0	Full-Scale	9.9976V	4.9988V	−1.9995 mA
Complementary	1 1 1 1 1 1 1 1 1 1 1 0	1 LSB ON	0.0024V	0.0012V	−0.0005 mA
Binary	1 1 1 1 1 1 1 1 1 1 1 1	Zero-Scale	0.0000V	0.0000V	0.0000 mA

Code Type	Input Code (Note 7) MSB … LSB	Output State	Bipolar Output Voltage Ranges ±10V	±5V	±2.5V	±1 mA
Bipolar	0 0 0 0 0 0 0 0 0 0 0 0	Full-Scale	9.9951V	4.9976V	2.4988V	−0.9995 mA
Complementary	0 1 1 1 1 1 1 1 1 1 1 1	Half-Scale	0.0000V	0.0000V	0.0000V	0.0000 mA
Binary	1 1 1 1 1 1 1 1 1 1 1 0	1 LSB ON	−9.9951V	−4.9976V	−2.4988V	0.9995 mA
	1 1 1 1 1 1 1 1 1 1 1 1	Zero-Scale	−10.0000V	−5.0000V	−2.5000V	1.0000 mA

Note 7: Logic input sense is such that an active low (V_{IN} ≤0.8V) turns a given bit ON and is represented as a logic "0" in the table.

3.6 Logic Input Compatibility

The design of the current mode switches in the DAC1285 series gives the device true TTL compatibility. It is TTL compatible over the entire operating temperature range and is independent of the reference voltage and V_{CC}. Furthermore, since the input breakdown ratings are in excess of 10V, the DAC1285 series may be driven directly from high (or low) voltage CMOS.

3.7 ±12 Volt Supply Operation

These DACs will operate with supply voltages as low as ±11.4V. It is recommended that output voltage ranges −10V to +10V and 0V to 10V not be used if the supply voltages are ever less than the recommended ±12V. The output amplifier may saturate if $|V_{SUPPLY}| - |V_{OUT}$ maximum$| < 2.0V$.

3.8 Power Supply Connections

For optimum performance power supply decoupling capacitors should be added as shown in the connection diagrams *(Figure 9)*. These capacitors (1 μF electrolytic recommended) should be located close to the device. Electrolytic capacitors, if used, should be paralleled with 0.01 μF ceramic capacitors for optimum high frequency performance.

National Semiconductor

DM2502, DM2503, DM2504 Successive Approximation Registers

General Description

The DM2502, DM2503 and DM2504 are 8-bit and 12-bit TTL registers designed for use in successive approximation A/D converters. These devices contain all the logic and control circuits necessary in combination with a D/A converter to perform successive approximation analog-to-digital conversions.

The DM2502 has 8 bits with serial capability and is not expandable.

The DM2503 has 8 bits and is expandable without serial capability.

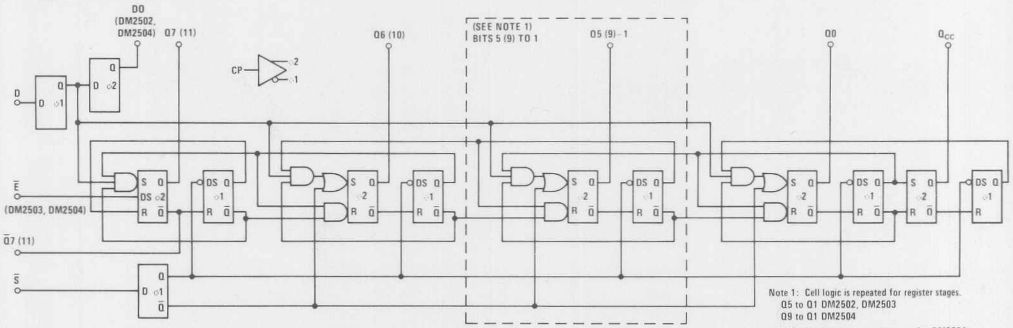
The DM2504 has 12 bits with serial capability and expandability.

All three devices are available in ceramic DIP, ceramic flatpak, and molded Epoxy-B DIPs. The DM2502, DM2503 and DM2504 operate over −55°C to +125°C; the DM2502C, DM2503C and DM2504C operate over 0°C to +70°C.

Features

- Complete logic for successive approximation A/D converters
- 8-bit and 12-bit registers
- Capable of short cycle or expanded operation
- Continuous or start-stop operation
- Compatible with D/A converters using any logic code
- Active low or active high logic outputs
- Use as general purpose serial-to-parallel converter or ring counter

Logic Diagram

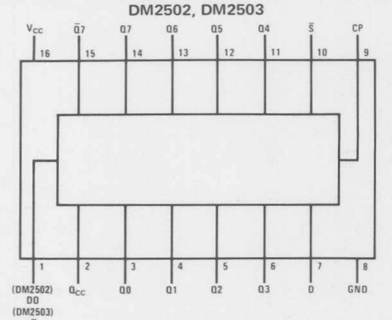


Note 1: Cell logic is repeated for register stages.
Q5 to Q1 DM2502, DM2503
Q9 to Q1 DM2504

Note 2: Numbers in parentheses are for DM2504.

Connection Diagrams (Dual-In-Line and Flat Packages)

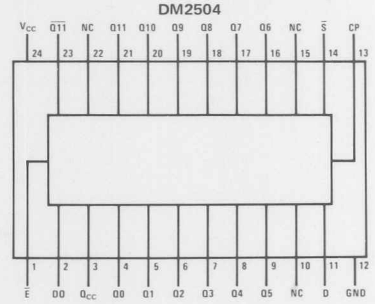
DM2502, DM2503



TOP VIEW

Order Number DM2502J DM2502CJ, DM2503J or DM2503CJ
See NS Package J16A
Order Number DM2502CN or DM2503CN
See NS Package N16A
Order Number DM2502W, DM2502CW, DM2503W, or DM2503CW
See NS Package W16A

DM2504



TOP VIEW

Order Number DM2504F or DM2504CF
See NS Package F24A

Order Number DM2504J or DM2504CJ
See NS Package J24A

Order Number DM2504CN
See NS Package N24A

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}			
DM2502C, DM2503C, DM2504C	4.75	5.25	V
DM2502, DM2503, DM2504	4.5	5.5	V
Temperature, T_A			
DM2502C, DM2503C, DM2504C	0	+70	°C
DM2502, DM2503, DM2504	–55	+125	°C

Electrical Characteristics (Notes 2 and 3) V_{CC} = 5.0V, T_A = 25°C, C_L = 15 pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage (V_{IH})	V_{CC} = Min	2.0			V
Logical "1" Input Current (I_{IH})	V_{CC} = Max				
CP Input	V_{IH} = 2.4V		6	40	μA
D, Ē, S̄ Inputs	V_{IH} = 2.4V		6	80	μA
All Inputs	V_{IH} = 5.5V			1.0	mA
Logical "0" Input Voltage (V_{IL})	V_{CC} = Min			0.8	V
Logical "0" Input Current (I_{IL})	V_{CC} = Max				
CP, S̄ Inputs	V_{IL} = 0.4V		–1.0	–1.6	mA
D, Ē Inputs	V_{IL} = 0.4V		–1.0	–3.2	mA
Logical "1" Output Voltage (V_{OH})	V_{CC} = Min, I_{OH} = –0.48 mA	2.4	3.6		V
Output Short Circuit Current (Note 4) (I_{OS})	V_{CC} = Max; V_{OUT} = 0.0V; Output High; CP, D, S̄, High; Ē Low	–10	–20	–45	mA
Logical "0" Output Voltage (V_{OL})	V_{CC} = Min, I_{OL} = 9.6 mA		0.2	0.4	V
Supply Current (I_{CC})	V_{CC} = Max, All Outputs Low				
DM2502C			65	95	mA
DM2502			65	85	mA
DM2503C			60	90	mA
DM2503			60	80	mA
DM2504C			90	124	mA
DM2504			90	110	mA
Propagation Delay to a Logical "0" From CP to Any Output (t_{pd0})		10	18	28	ns
Propagation Delay to a Logical "0" From Ē to Q7 (Q11) Output (t_{pd0})	CP High, S̄ Low DM2503, DM2503C, DM2504, DM2504C Only		16	24	ns
Propagation Delay to a Logical "1" From CP to Any Output (t_{pd1})		10	26	38	ns
Propagation Delay to a Logical "1" From Ē to Q7 (Q11) Output (t_{pd1})	CP High, S̄ Low DM2503, DM2503C, DM2504, DM2504C Only		13	19	ns
Set-Up Time Data Input ($t_{s(D)}$)		–10	4	8	ns
Set-Up Time Start Input ($t_{s(\bar{S})}$)		0	9	16	ns
Minimum Low CP Width (t_{PWL})			30	42	ns
Minimum High CP Width (t_{PWH})			17	24	ns
Maximum Clock Frequency (f_{MAX})		15	21		MHz

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the –55°C to +125°C temperature range for the DM2502, DM2503 and DM2504, and across the 0°C to +70°C range for the DM2502C, DM2503C and DM2504C. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

The registers consist of a set of master latches that act as the control elements in the device and change state on the input clock high-to-low transition and a set of slave latches that hold the register data and change on the input clock low-to-high transition. Externally the device acts as a special purpose serial-to-parallel converter that accepts data at the D input of the register and sends the data to the appropriate slave latch to appear at the register output and the DO output on the DM2502 and DM2504 when the clock goes from low-to-high. There are no restrictions on the data input; it can change state at any time except during a short interval centered about the clock low-to-high transition. At the same time that data enters the register bit the next less significant bit register is set to a low ready for the next iteration.

The register is reset by holding the $\overline{S}$ (Start) signal low during the clock low-to-high transition. The register synchronously resets to the state Q7 (11) low, and all the remaining register outputs high. The Q_{CC} (Conversion Complete) signal is also set high at this time. The $\overline{S}$ signal should not be brought back high until after the clock low-to-high transition in order to guarantee correct resetting. After the clock has gone high resetting the register, the $\overline{S}$ signal must be removed. On the next clock low-to-high transition the data on the D input is set into the Q7 (11) register bit and the Q6 (10) register bit is set to a low ready for the next clock cycle. On the next clock low-to-high transition data enters the Q6 (10) register bit and Q5 (9) is set to a low. This operation is repeated for each register bit in turn until the register has been filled. When the data goes into Q0, the Q_{CC} signal goes low, and the register is inhibited from further change until reset by a Start signal.

The DM2502, DM2503 and DM2504 have a specially tailored two-phase clock generator to provide non-overlapping two-phase clock pulses (i.e., the clock waveforms intersect below the thresholds of the gates clock input (such as from relatively weak comparator outputs), improper logic operation will not result.

LOGIC CODES

All three registers can be operated with various logic codes. Two's complement code is used by offsetting the comparator 1/2 full range + 1/2 LSB and using the complement of the MSB ($\overline{Q}7$ or $\overline{Q}11$) with a binary D/A converter. Offset binary is used in the same manner but with the MSB (Q7 or Q11). BCD D/A converters can be used with the addition of illegal code suppression logic.

ACTIVE HIGH OR ACTIVE LOW LOGIC

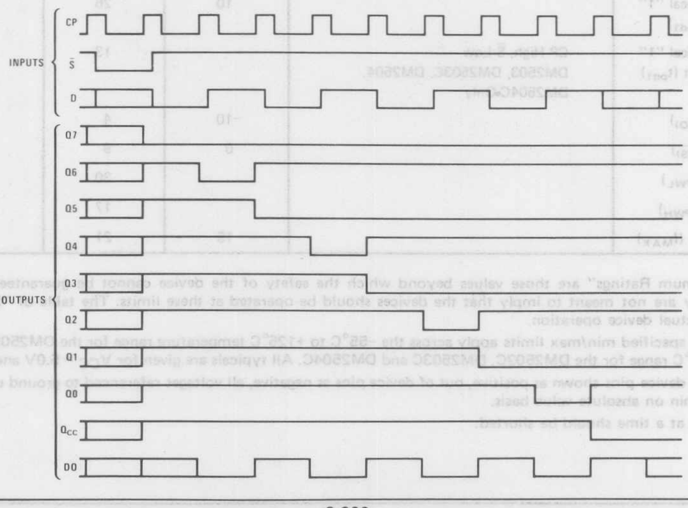
The register can be used with either D/A converters that require a low voltage level to turn on, or D/A converters that require a high voltage level to turn the switch on. If D/A converters are used which turn on with a low logic level, the resulting digital output from the register is active low. That is, a logic "1" is represented as a low voltage level. If D/A converters are used that turn on with a high logic level then the digital output is active high; a logic "1" is represented as a high voltage level.

EXPANDED OPERATION

An active low enable input, $\overline{E}$, on the DM2503 and DM2504 allows registers to be connected together to form a longer register by connecting the clock, D, and $\overline{S}$ inputs in parallel and connecting the Q_{CC} output of one register to the $\overline{E}$ input of the next less significant register. When the start signal resets the register, the $\overline{E}$ signal goes high, forcing the Q7 (11) bit high and inhibiting the register from accepting data until the previous register is full and its Q_{CC} goes low. If only one register is used the $\overline{E}$ input should be held at a low logic level.

Timing Diagram

DM2502, DM2503



Application Information (Continued)

SHORT CYCLE

If all bits are not required, the register may be truncated and conversion time saved by using a register output going low rather than the Q_{CC} signal to indicate the end of conversion. If the register is truncated and operated in the continuous conversion mode, a lock-up condition may occur on power turn-on. This condition can be avoided by making the start input the OR function of Q_{CC} and the appropriate register output.

COMPARATOR BIAS

To minimize the digital error below ±1/2 LSB, the comparator must be biased. If a D/A converter is used which requires a low voltage level to turn on, the comparator should be biased +1/2 LSB. If the D/A converter requires a high logic level to turn on, the comparator must be biased −1/2 LSB.

Definition of Terms

CP: The clock input of the register.

D: The serial data input of the register.

DO: The serial data out. (The D input delayed one bit).

$\overline{E}$: The register enable. This input is used to expand the length of the register and when high forces the Q7 (11) register output high and inhibits conversion. When not used for expansion the enable is held at a low logic level (ground).

Q_i i = 7 (11) to 0: The outputs of the register.

Q_{CC}: The conversion complete output. This output remains high during a conversion and goes low when a conversion is complete.

Q7 (11): The true output of the MSB of the register.

$\overline{Q7}$ (11): The complement output of the MSB of the register.

$\overline{S}$: The start input. If the start input is held low for at least a clock period the register will be reset to Q7 (11) low and all the remaining outputs high. A start pulse that is low for a shorter period of time can be used if it meets the set-up time requirements of the $\overline{S}$ input.

Truth Table

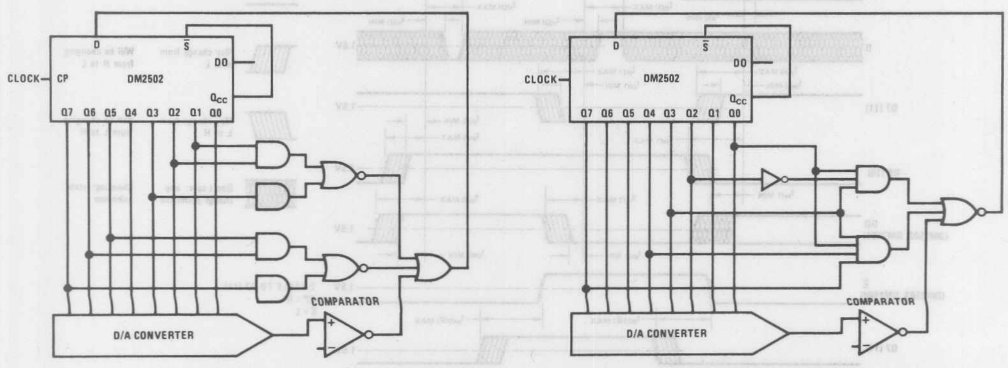
DM2502, DM2503

TIME	INPUTS			OUTPUTS[1]									
t_n	D	$\overline{S}$	$\overline{E}$[2]	DO[3]	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Q_{CC}
0	X	L	L	X	X	X	X	X	X	X	X	X	X
1	D7	H	L	X	L	H	H	H	H	H	H	H	H
2	D6	H	L	D7	D7	L	H	H	H	H	H	H	H
3	D5	H	L	D6	D7	D6	L	H	H	H	H	H	H
4	D4	H	L	D5	D7	D6	D5	L	H	H	H	H	H
5	D3	H	L	D4	D7	D6	D5	D4	L	H	H	H	H
6	D2	H	L	D3	D7	D6	D5	D4	D3	L	H	H	H
7	D1	H	L	D2	D7	D6	D5	D4	D3	D2	L	H	H
8	D0	H	L	D1	D7	D6	D5	D4	D3	D2	D1	L	H
9	X	H	L	D0	D7	D6	D5	D4	D3	D2	D1	D0	L
10	X	X	L	X	D7	D6	D5	D4	D3	D2	D1	D0	L
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC

Note 1: Truth table for DM2504 is extended to include 12 outputs.
Note 2: Truth table for DM2502 does not include $\overline{E}$ column or last line in truth table shown.
Note 3: Truth table for DM2503 does not include D0 column.

H = High Voltage Level
L = Low Voltage Level
X = Don't Care
NC = No Change

Typical Applications



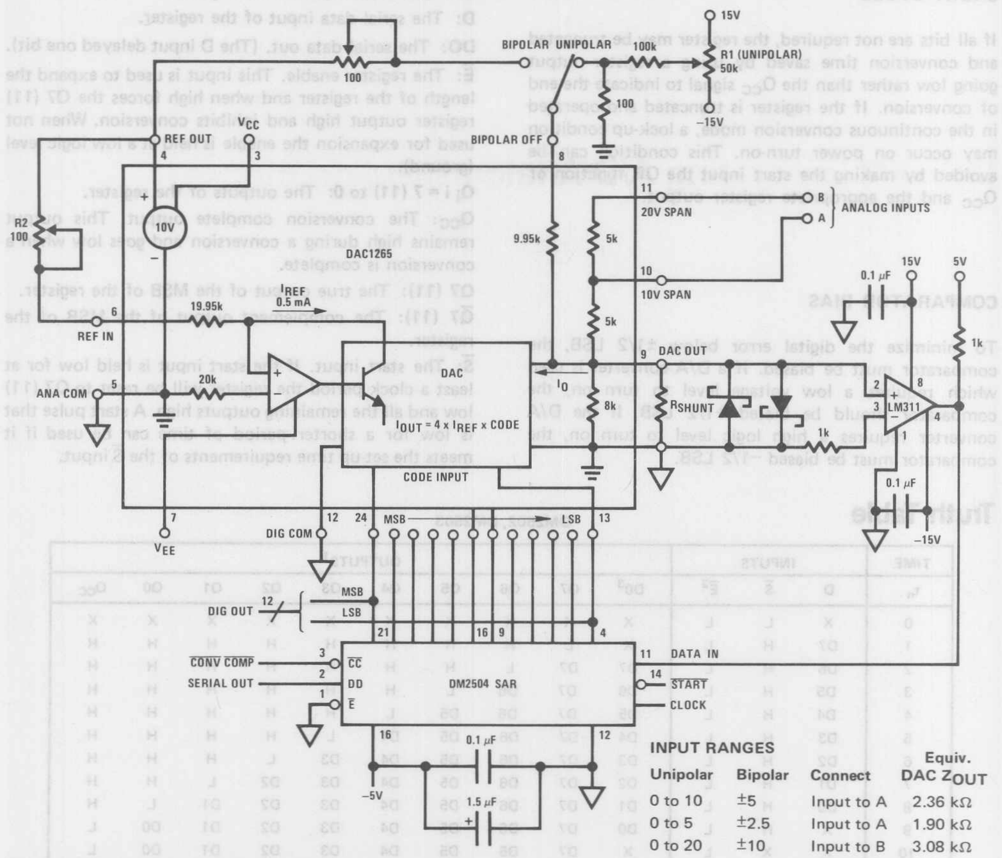
Active High

Active Low

BCD Illegal Code Suppression

Typical Applications (Continued)

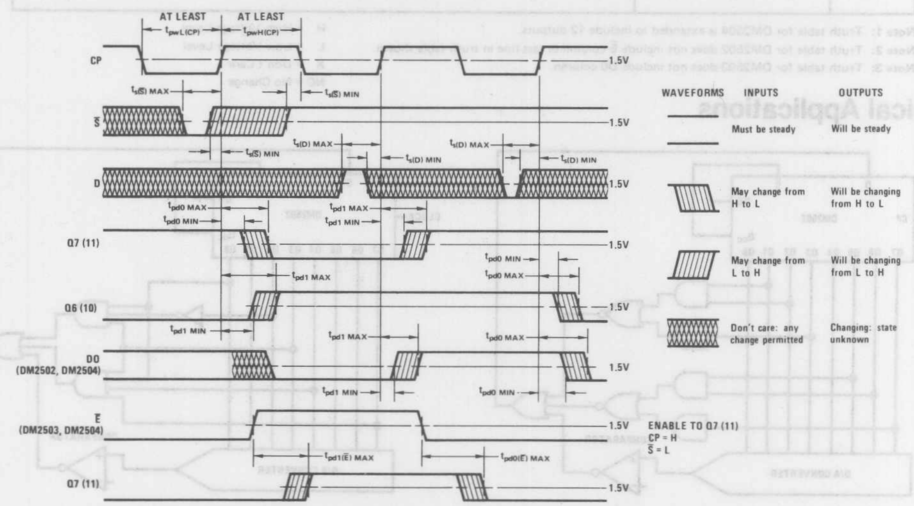
Fast Precision Analog-to-Digital Converter



INPUT RANGES

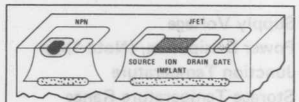
Unipolar	Bipolar	Connect	Equiv. DAC Z_{OUT}
0 to 10	±5	Input to A	2.36 kΩ
0 to 5	±2.5	Input to A	1.90 kΩ
0 to 20	±10	Input to B	3.08 kΩ
		B to DAC OUT	

Switching Time Waveforms



National Semiconductor

A to D, D to A



BI-FET Technology

LF13300 Integrating A/D Analog Building Block

General Description

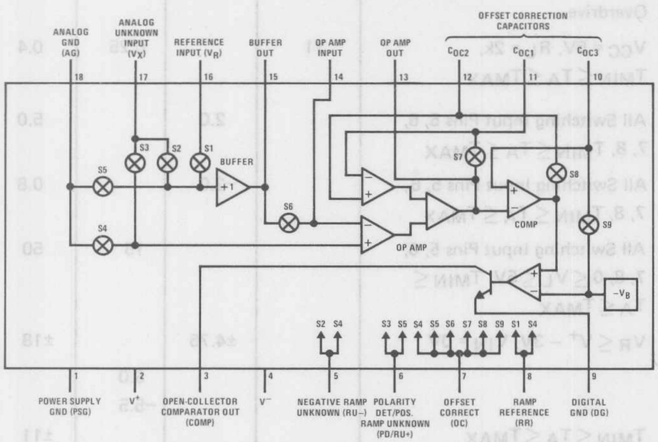
The LF13300 is the analog section of a precision integrating analog-to-digital (A/D) system. JFET and bipolar transistors (BI-FET) are combined on the same chip to provide a high input impedance unity gain buffer, comparator and integrator, along with 9 JFET analog switches. The LF13300 has sufficient resolution to construct up to a 4 1/2-digit Digital Panel Meter (DPM) or a 12-bit (plus sign) Data Acquisition System and is specifically designed for use with the ADB1200 12-bit binary building block.

*See ADB1200 data sheet for more information.

Features

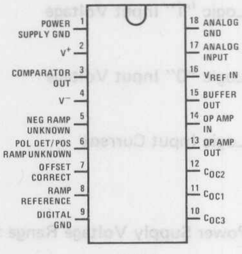
- Rugged JFETs allow blow-out free handling
- High input impedance 10,000 MΩ typ
- Automatic offset correction
- Analog circuitry can be physically and electrically isolated from high noise digital circuits
- Analog input range of ±11V with ±15V supplies
- Wide power supply voltage range ±5V to ±18V
- TTL and CMOS compatible logic
- Can interface directly with microprocessors
- Versatile: can be used as a 12-bit plus sign binary A/D, 4 1/2-digit, 3 3/4-digit and 3 1/2-digit Digital Panel Meter (DPM)
- Low cost

Block and Connection Diagrams



TOP VIEW

Dual-In-Line Package



TOP VIEW

Order Number LF13300D
See NS Package D18A

Junction Temperature	110°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 10 seconds)	300°C

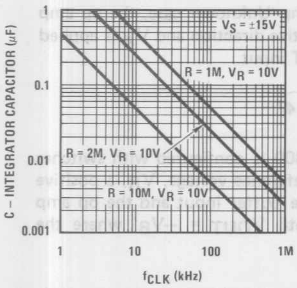
Electrical Characteristics ($V_S = \pm15V$, $T_A = 25°C$, unless otherwise noted)

PARAMETER	CONDITIONS	TEST CIRCUIT	LF13300 MIN	TYP	MAX	UNITS
Analog Input Current, I_{IN}	$V_X = 0$	1, 2		80	500	pA
	$T_{MIN} \le T_A \le T_{MAX}$				5	nA
Analog Input Voltage Range	V_X Adjusted until $\lvert I_{IN} \rvert \ge 10$ nA	1, 2			±11	V
Analog Input Resistance	$V_X = 0$	1, 2		10,000		MΩ
Reference Input Currents, I_R	$V_R = 10V$	3		1	100	nA
	$T_{MIN} \le T_A \le T_{MAX}$	3			10	μA
Reference Input Voltage Range	V_R Adjusted until $\lvert I_R \rvert \ge 10\ \mu A$	3	0		11	V
Reference Input Resistance	$V_R = 10V$	3		1000		MΩ
Offset Correction Voltage, $-V_B$		4		−12		V
Offset Correction		5		20	2000	pA
Input Current, I_{OC}		5			20	nA
Op Amp Slew Rate		6		10		V/μs
Op Amp Bandwidth		7		3		MHz
Buffer Slew Rate		9		25		V/μs
Comparator Response Time	200 μV Input Stop, 100 μV Overdrive	11		2.5		μs
Comparator Output Saturation Voltage	$V_{CC} = 5V$, $R_L = 2k$, $T_{MIN} \le T_A \le T_{MAX}$	11		0.25	0.4	V
Logic "1" Input Voltage	All Switching Input Pins 5, 6, 7, 8, $T_{MIN} \le T_A \le T_{MAX}$		2.0		5.0	V
Logic "0" Input Voltage	All Switching Input Pins 5, 6, 7, 8, $T_{MIN} \le T_A \le T_{MAX}$		−2.0		0.8	V
Logic Input Current	All Switching Input Pins 5, 6, 7, 8, $0 \le V_L \le 5V$, $T_{MIN} \le T_A \le T_{MAX}$			15	50	μA
Power Supply Voltage Range $\pm V_S$	$V_R \le V^+ - 3V$, $V_{IN} = 0V$		±4.75		±18	V
				3.0		mA
				−5.5		mA
	$T_{MIN} \le T_A \le T_{MAX}$				±11	mA

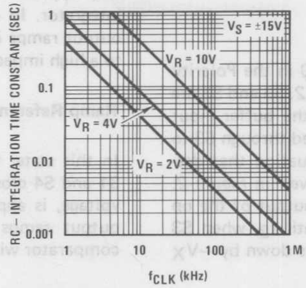
Note 1: For operating at elevated temperatures, the LF13300 in the dual-in-line package must be derated based on the thermal resistance of 100°C/W junction to ambient.

Typical Performance Characteristics

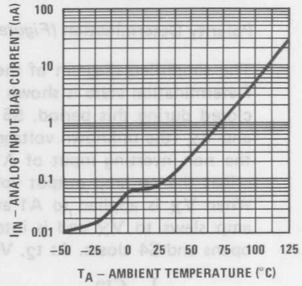
Integrator Capacitance, C vs f_{CLK} for Different Integrator Resistances, R



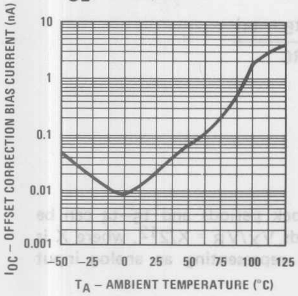
Integration Time Constant (RC) vs f_{CLK} for Different Reference Voltages, V_R



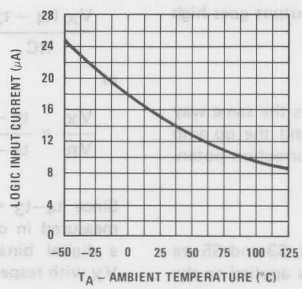
Analog Input Bias Current, I_{IN}, $V_X = 0V$, vs Temperature



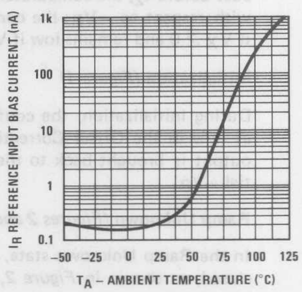
Offset Correction Bias Current, I_{OL}, vs Temperature



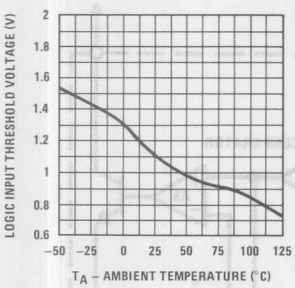
Logic Input Current vs Temperature



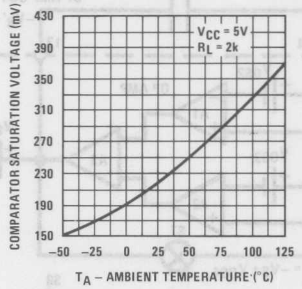
Reference Input Bias Current, I_R, vs Temperature



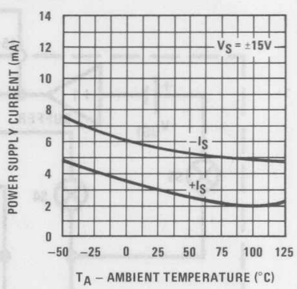
Logic Input Threshold Voltage vs Temperature



Comparator Saturation Voltage vs Temperature



Power Supply Current vs Temperature



Functional Description

The LF13300 goes through the following 5 states during normal cycle: 1) Offset Correction; 2) Polarity Determination; 3) Initialization; 4) Ramp Unknown; 5) Ramp Reference

Offset Correction Description *(Figure 1)*

The Offset Correction scheme will drive the input of the comparator to its switching threshold when the analog input is zero and the timing components, RC, are bypassed.

The Offset Correction input (OC) is driven high, closing switches S4–S9.

The offset voltages are assigned as follows: V_{OS1} – the input offset voltage of the buffer; V_{OS2} – the input offset voltage of A1; V_{OS3} – the input offset voltage of A2; V_{OS4} – the input offset voltage of the comparator.

S5 grounds the input of the buffer so that its output voltage is simply V_{OS1}. S6 bypasses R to keep the integration time constant, RC, from affecting the circuit operation. S4 makes the total equivalent input voltage to A1 be $-V_{OS1} - V_{OS2}$. S7 puts the op amp in a unity gain configuration with respect to the input of A2. S8 keeps the output voltage of the op amp at $-V_B + V_{OS4} = -V_B'$ (the Offset Correction potential) since the comparator is placed inside the loop. C3 samples the output of the $-V_B$ generator. The voltage at the non-inverting input of A2 is $-V_B - V_{OS1}$ –

Functional Description (Continued)

$V_{OS2} - V_{OS3} + V_{OS4} = V1$. Thus, the sum of the offsets is stored on C1, and the differential voltage across the comparator is zero.

Polarity Determination *(Figure 2)*

The simplified diagram of the LF13300 in the Polarity Determination state is shown in *Figure 2*. S5 and S3 are closed during this period. S5 grounds the buffer input and V_X (the unknown voltage) is applied through S3 to the non-inverting input of A1. The equation that describes the op amp output voltage is given in *Figure 2*. When V_X is applied to A1 at t_1, the output of the op amp slews to V_X and is integrated until t_2, when S3 opens and S4 closes. At t_2, V_{OUT} slews down by $-V_X$ leaving $\frac{1}{RC}\int_{t_2}^{t_2} V_X dt - V_B'$ at the op amp output.

Just before t_2, the comparator senses the op amp output with respect to $-V_B$; the comparator output goes high if $V_X > 0$ and remains low if $V_X \leq 0$.

Initialization *(Figure 1)*

During initialization, the configuration is the same way as it is in the Offset Correction state and the op amp output is brought back to the Offset Correction potential $-V_B'$.

Ramp Unknown *(Figures 2 and 3)*

In the Ramp Unknown state, if $V_X \geq 0$, S3 and S5 are closed, as shown in *Figure 2*, and V_X is applied to the + input of the integrator. If $V_X < 0$, the device is connected as in *Figure 3* with S2 and S4 closed. V_X is now applied through the buffer to the − input of the integrator. In either Ramp Unknown case, the op amp output ramps in the positive direction and V_X is applied to a high impedance JFET input.

Ramp Reference *(Figure 4)*

In this state, the LF13300 is configured with switches S1 and S4 closed. The reference voltage, V_R, a positive voltage, is applied to the buffer input and the op amp output ramps down until $V_{OUT} = -V_B'$ where the comparator will trip.

If V_X and V_R are assumed to be constant over their respective integration periods, the integrals of *Figure 4* are reduced to,

$$\frac{V_X(t_4 - t_3)}{RC} = \frac{V_R(t_5 - t_4)}{RC}$$

or

$$\frac{V_X}{V_R} = \frac{t_5 - t_4}{t_4 - t_3}.$$

Since $t_4 - t_3 = 4096$ clock periods and $t_5 - t_4$ can be measured in clock periods, $V_X/V_R = X/2^{12}$, where X is a digital binary output representing an analog input V_X with respect to V_R.

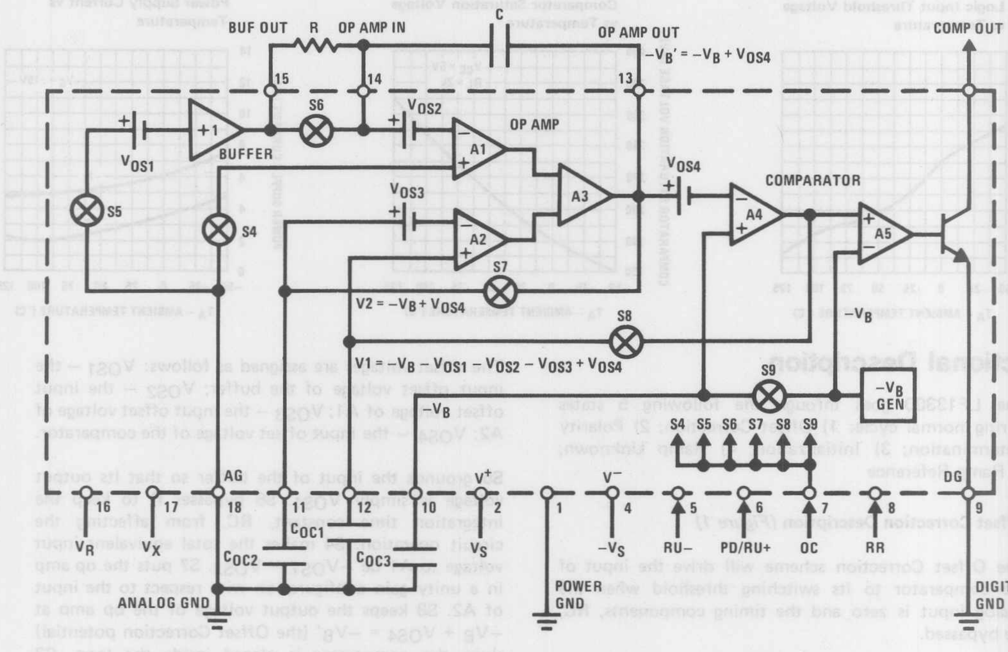


FIGURE 1. Offset Correction Circuit

Functional Description (Continued)

$$V_{OUT} = \begin{cases} -V_B' + V_X + \dfrac{1}{RC}\displaystyle\int_{t_3}^{t_4} V_X\,dt\text{: Ramp Unknown for } V_X \geq 0 \\ -V_B' + V_X + \dfrac{1}{RC}\displaystyle\int_{t_1}^{t_2} V_X\,dt\text{: Polarity Determination} \end{cases}$$

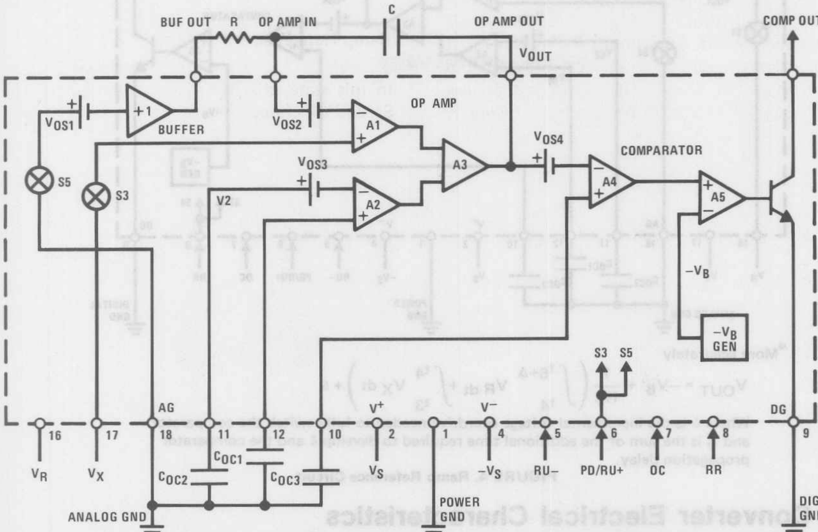


FIGURE 2. Polarity Determination Circuit or Ramp Unknown Circuit for $V_X \geq 0$

$$V_{OUT} = -V_B' + \frac{1}{RC}\int_{t_3}^{t_4} V_X\,dt\text{: Ramp Unknown for } V_X < 0$$

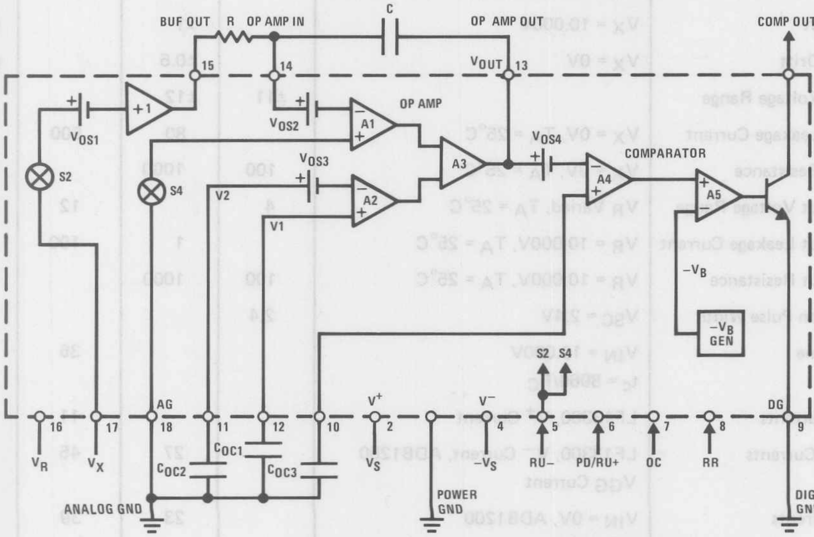
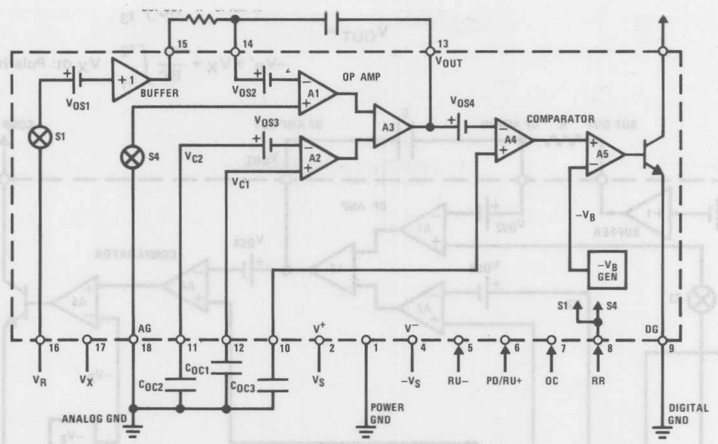


FIGURE 3. Ramp Unknown for $V_X < 0$



*More accurately

$$V_{OUT} = -V_B' + \frac{1}{RC}\left(\int_{t_4}^{t_5+\Delta} V_R\,dt + \int_{t_3}^{t_4} V_X\,dt\right) + \delta$$

Where δ is the incremental voltage overdrive needed to fully switch the comparator and Δ is the sum of the additional time required to develop δ and the comparator propagation delay.

FIGURE 4. Ramp Reference Circuit

12-Bit A/D Converter Electrical Characteristics

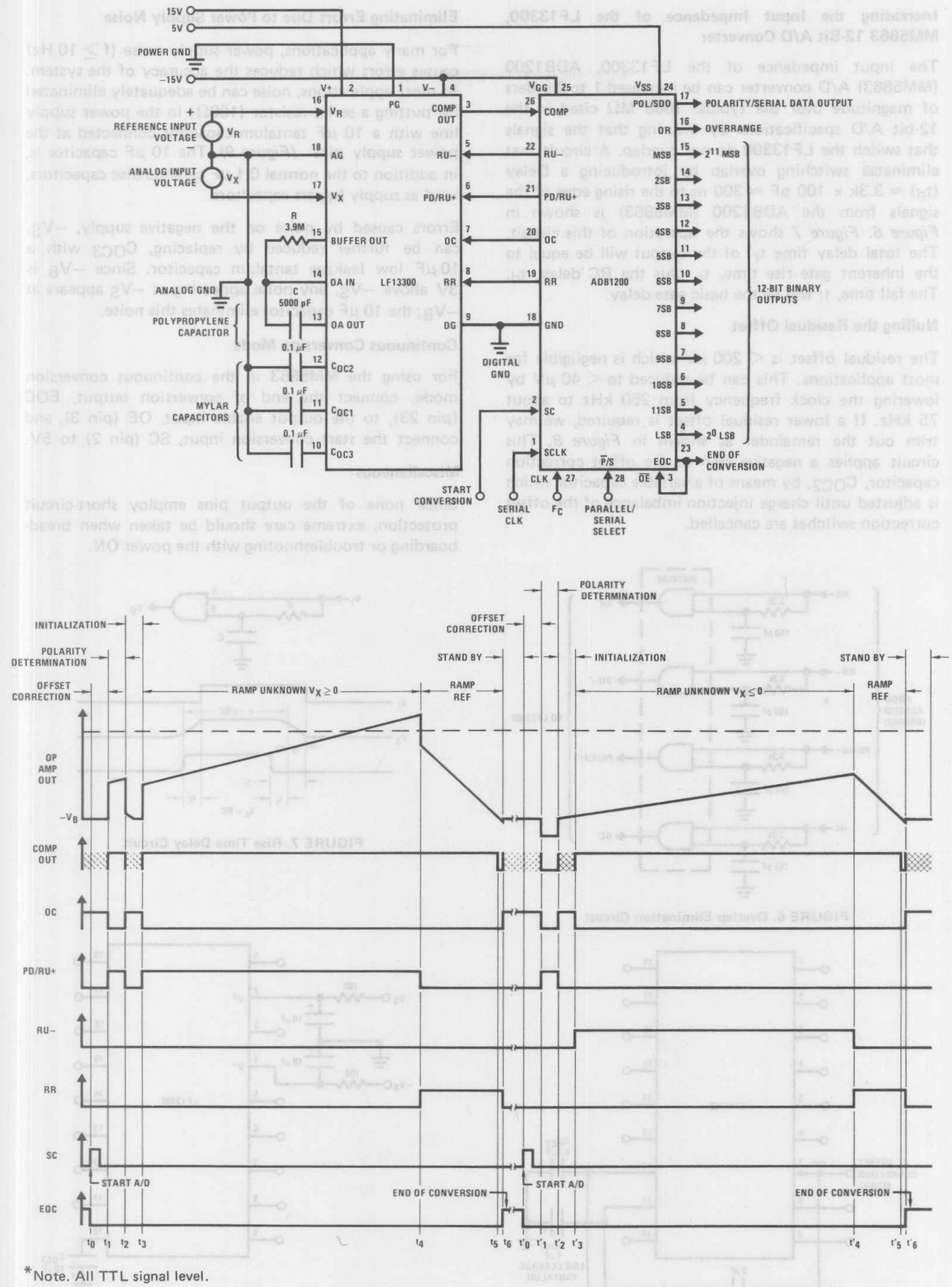
12-bit plus sign. (LF13300 with ADB1200). (V_R = 10.000V, F_C = 250 kHz, $0°C \le T_A \le +70°C$ unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution (Note 3)	V_R = 5.000V, $-10V \le V_X \le +10V$	13			Bits
	F_C = 125 kHz, T_A = 25°C	14			Bits
Non-Linearity			±1/8	±1/2	LSB
Ratiometric Gain Error (Def.)	V_X = ±10.000V, T_A = 25°C, (Note 2)		±1/2	±2	LSB
Gain Error Drift	V_X = 10.000V		±1		ppm/°C
Zero Reading Drift	V_X = 0V		±0.5		ppm/°C
Analog Input Voltage Range		±11	±12		V
Analog Input Leakage Current	V_X = 0V, T_A = 25°C		80	500	pA
Analog Input Resistance	V_X = 0V, T_A = 25°C	100	1000		MΩ
Reference Input Voltage Range	V_R Varied, T_A = 25°C	4		12	V
Reference Input Leakage Current	V_R = 10.000V, T_A = 25°C		1	100	nA
Reference Input Resistance	V_R = 10.000V, T_A = 25°C	100	1000		MΩ
Start Conversion Pulse Width	V_{SC} = 2.4V	2.4			μs
Conversion Time	V_{IN} = 10.000V t_c = 8960/F_C			36	ms
15V Supply Currents	LF13300, V^+ Current			11	mA
−15V Supply Currents	LF13300, V^- Current, ADB1200 V_{GG} Current		27	45	mA
5V Supply Currents	V_{IN} = 0V, ADB1200 V_{SS} Current		23	39	mA

Note 2: The A/D converter system must have been operational for a minimum of 30 seconds before this measurement is made. This is to relax the dielectric absorption effects of the integration capacitor, C.

Note 3: Polarity and Overrange outputs are considered as additional output bits.

12-Bit A/D Converter Circuit and Timing Diagrams



*Note. All TTL signal level.

FIGURE 5.

Application Hints

Increasing the Input Impedance of the LF13300, MM5863 12-Bit A/D Converter

The input impedance of the LF13300, ADB1200 (MM5863) A/D converter can be increased 1 to 2 orders of magnitude over the typical 1000 MΩ cited in the 12-bit A/D specifications by insuring that the signals that switch the LF13300 do not overlap. A circuit that eliminates switching overlap by introducing a Delay (t_d) ≈ 3.3k x 100 pF ≈ 300 ns to the rising edge of the signals from the ADB1200 (MM5863) is shown in *Figure 6. Figure 7* shows the operation of this circuit. The total delay time t_r' of the output will be equal to the inherent gate rise time, t_r, plus the RC delay, t_d. The fall time, t_f will be the basic gate delay.

Nulling the Residual Offset

The residual offset is < 200 μV which is negligible for most applications. This can be reduced to < 40 μV by lowering the clock frequency from 250 kHz to about 75 kHz. If a lower residual offset is required, we may trim out the remainder as shown in *Figure 8*. This circuit applies a negative step to the offset correction capacitor, C_{OC2}, by means of a variable capacitor which is adjusted until charge injection imbalance of the offset correction switches are cancelled.

Eliminating Errors Due to Power Supply Noise

For many applications, power supply noise (f ≥ 10 Hz) causes errors which reduces the accuracy of the system. In most applications, noise can be adequately eliminated by putting a series resistor (100Ω) in the power supply line with a 10 μF tantalum capacitor connected at the power supply pins *(Figure 9)*. The 10 μF capacitor is, in addition to the normal 0.1 μF ceramic disc capacitors, used as supply bypass capacitors.

Errors caused by noise on the negative supply, $-V_S$, can be further reduced by replacing, C_{OC3} with a 10 μF low leakage tantalum capacitor. Since $-V_B$ is 3V above $-V_S$, any noise appearing at $-V_S$ appears at $-V_B$; the 10 μF capacitor eliminates this noise.

Continuous Conversion Mode

For using the MM5863 in the continuous conversion mode, connect the end of conversion output, EOC (pin 23), to the output enable input, OE (pin 3), and connect the start conversion input, SC (pin 2) to 5V.

Miscellaneous

Since none of the output pins employ short-circuit protection, extreme care should be taken when breadboarding or troubleshooting with the power ON.

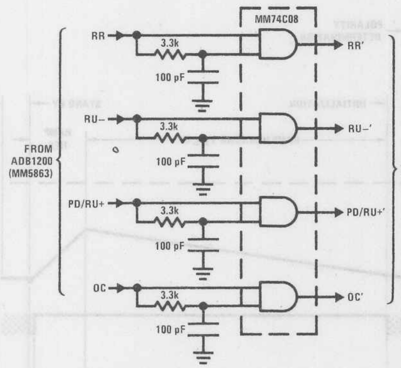


FIGURE 6. Overlap Elimination Circuit

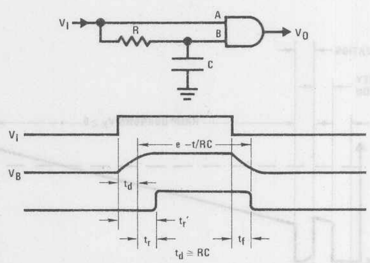


FIGURE 7. Rise Time Delay Circuit

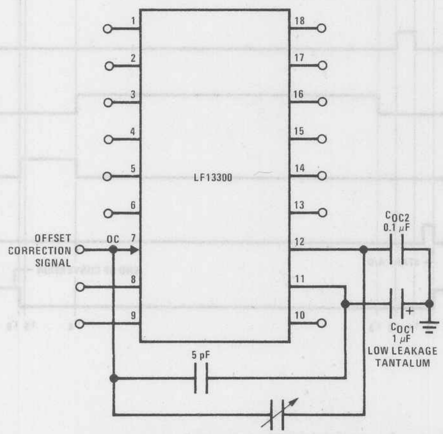


FIGURE 8. Residual Offset Nulling Circuit

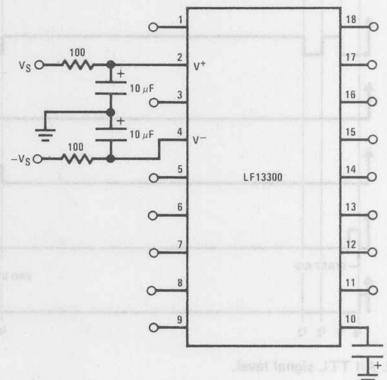


FIGURE 9. Power Supply Noise Reduction Circuit

Typical Applications

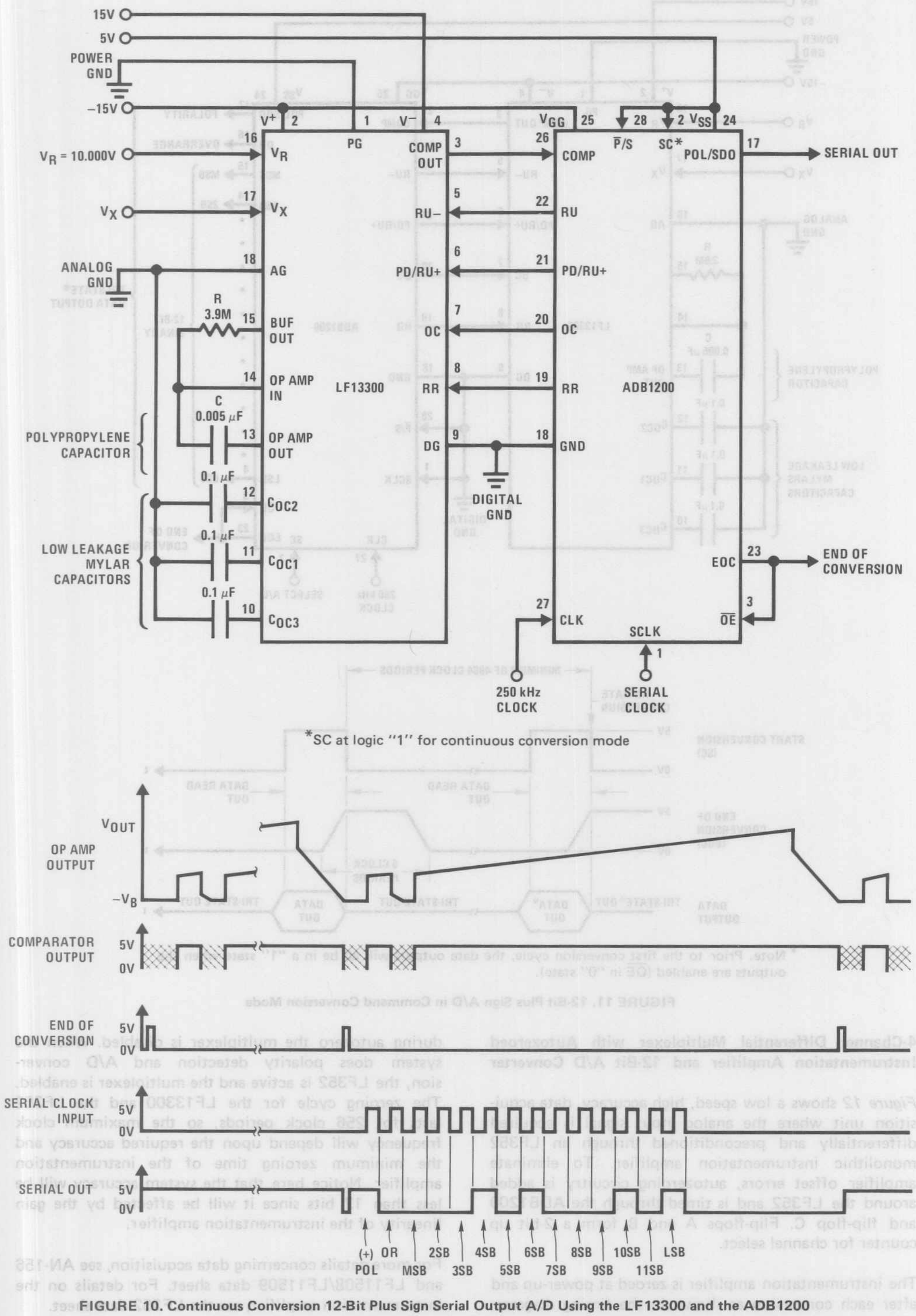
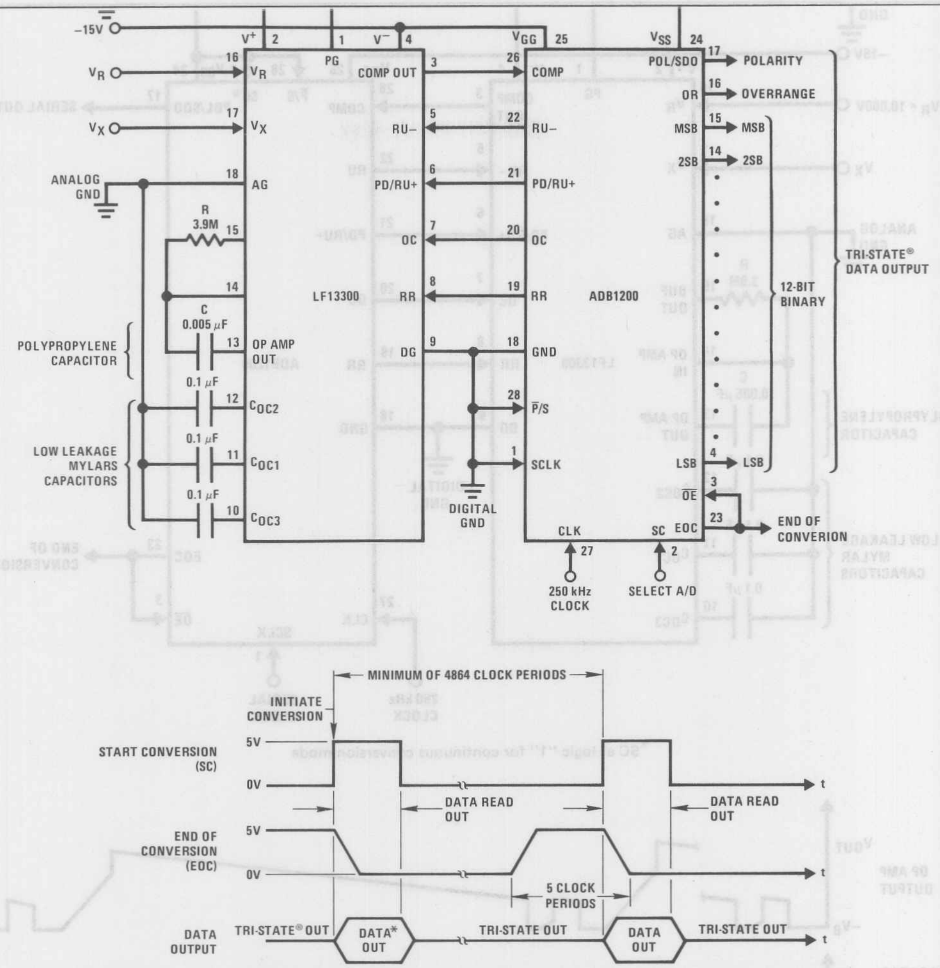


FIGURE 10. Continuous Conversion 12-Bit Plus Sign Serial Output A/D Using the LF13300 and the ADB1200



* Note. Prior to the first conversion cycle, the data outputs will all be in a "1" state when the outputs are enabled (O̅E̅ in "0" state).

FIGURE 11. 12-Bit Plus Sign A/D in Command Conversion Mode

4-Channel Differential Multiplexer with Autozeroed Instrumentation Amplifier and 12-Bit A/D Converter

Figure 12 shows a low speed, high accuracy, data acquisition unit where the analog input signal is acquired differentially and preconditioned through an LF352 monolithic instrumentation amplifier. To eliminate amplifier offset errors, autozeroing circuitry is added around the LF352 and is timed through the ADB1200 and flip-flop C. Flip-flops A and B form a 2-bit up counter for channel select.

The instrumentation amplifier is zeroed at power-up and after each conversion as shown in the timing diagram; during autozero the multiplexer is disabled. When the system does polarity detection and A/D conversion, the LF352 is active and the multiplexer is enabled. The zeroing cycle for the LF13300 and the LF352 lasts for 256 clock periods, so the maximum clock frequency will depend upon the required accuracy and the minimum zeroing time of the instrumentation amplifier. Notice here that the system accuracy will be less than 12 bits since it will be affected by the gain linearity of the instrumentation amplifier.

For more details concerning data acquisition, see AN-156 and LF11508/LF11509 data sheet. For details on the instrumentation amplifier, see the LF352 data sheet.

Typical Applications (Continued)

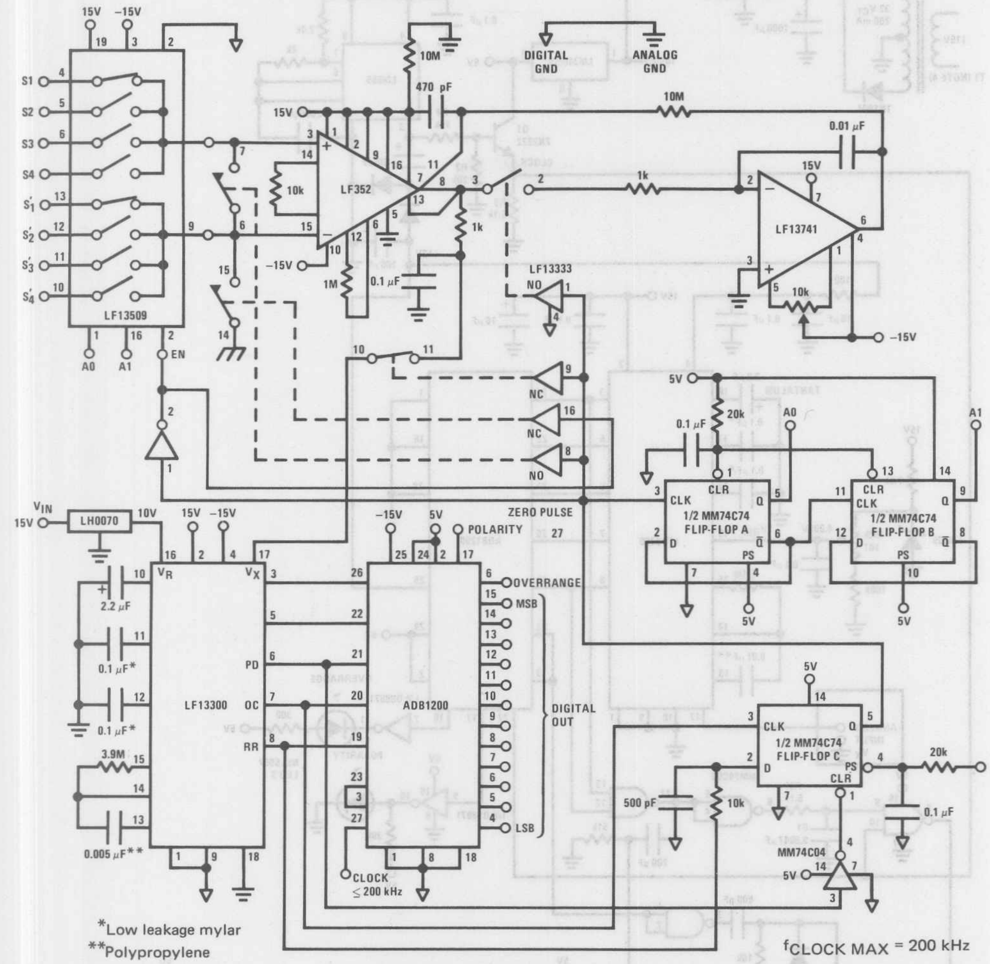


FIGURE 12. 4-Channel Differential Multiplexer with Autozeroed Instrumentation Amplifier and 12-Bit A/D Converter

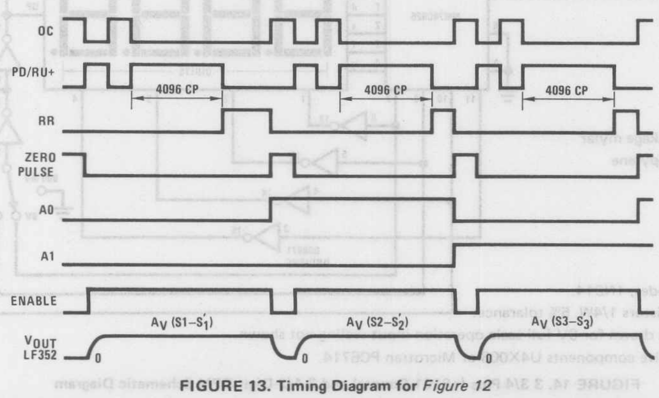
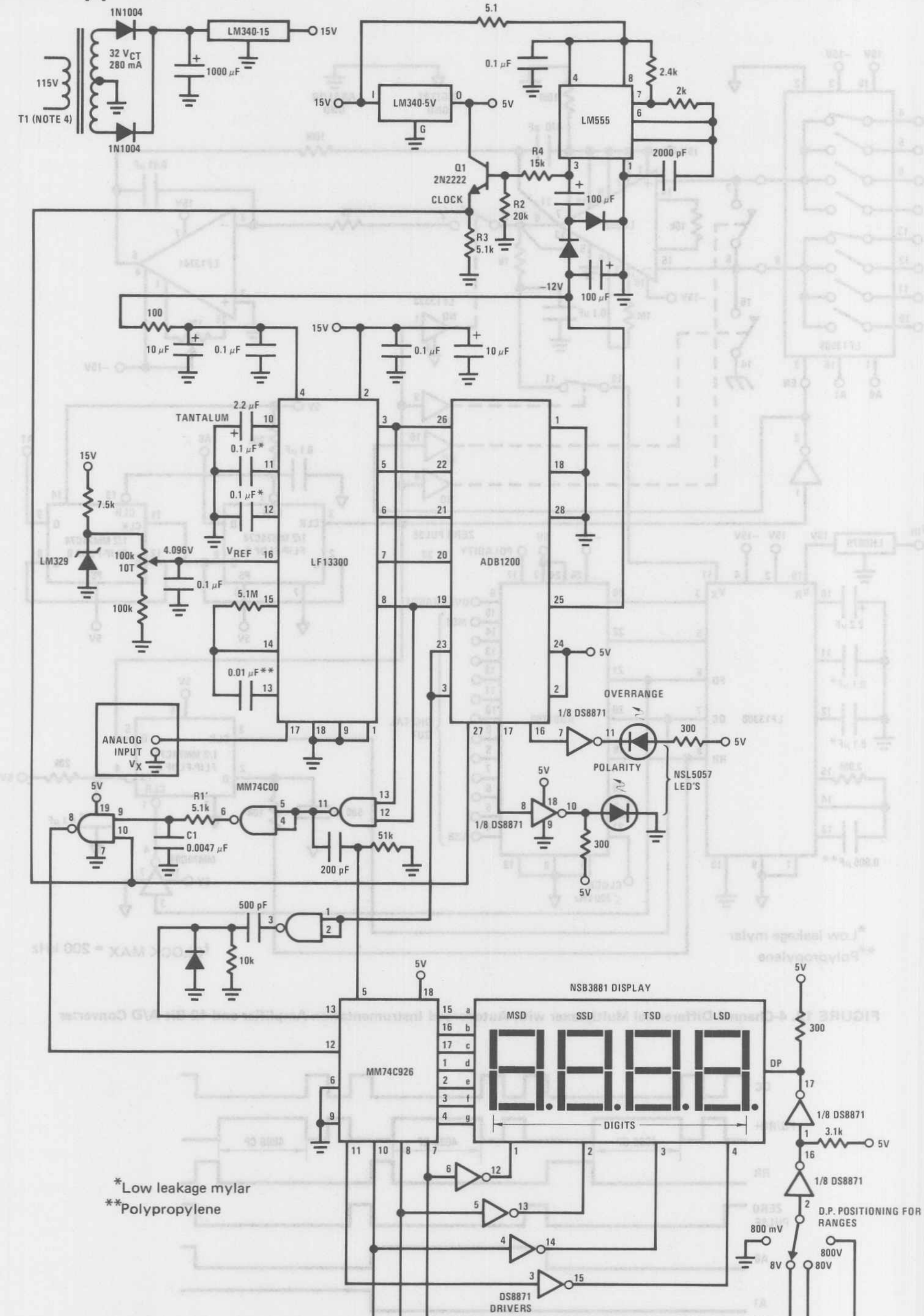


FIGURE 13. Timing Diagram for *Figure 12*

Typical Applications (Continued)



*Low leakage mylar
**Polypropylene

Note 1: All diodes, 1N914.

Note 2: All resistors 1/4W, 5% tolerance.

Note 3: Circuit drawn for 8V full scale operation input scaling not shown.

Note 4: Inductive components U4X003 or Microtran PC6714.

FIGURE 14. 3 3/4 Plus (±8191 Counts) and 3 1/2-Digit DPM Schematic Diagram

Typical Applications (Continued)

3 3/4 Plus Digit (±8191 Counts)/3 1/2-Digit (±1999 Counts) DPM

In this circuit of *Figure 14*, the LF13300 and ADB1200 interact as previously described. The CMOS counter (MM74C926, MM74C928) is connected to count clock pulses during the ramp reference cycle. The counts are latched into the display when the comparator output trips, (goes low), as shown in the timing diagram *Figure 15*.

The RC network consisting of R1 and C1 is a low pass filter that prohibits the fast transients that occur on the comparator output during Offset Correction from loading any erroneous counts into the counter.

The DPM is able to operate from a single 15V power supply with the aid of a dc-dc converter. The LM555 generates the negative voltages required in the circuit and also doubles as the clock. The combination of Q1, R2, R3 and R4 forms a level shift to convert the output swing of the LM555 to a 0V–5V swing that is compatible with the logic. The LM340–5 drops the incoming 15V to 5V for use by the logic circuits and the LED display.

This circuit can be a 3 3/4 plus digit DPM if the MM74C926 is used or a 3 1/2-digit DPM if the MM74C928 is used. These counters are pin compatible and physically interchangeable.

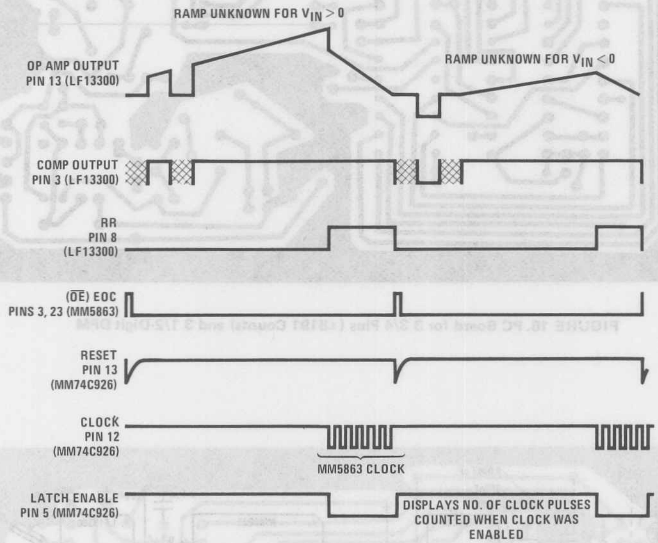


FIGURE 15. Timing Diagram for 3 3/4-Digit DVM

3 3/4-Digit DPM Electrical Characteristics

3 3/4 plus digits plus sign (±8191 counts) DPM system characteristics.

(Circuit as in *Figure 14*, V_S = ±15V, V_R = 4.096V, T_A = 25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution	$-8.2V \leq V_X \leq +8.2V$	16,382			Counts
Nonlinearity	V_{IN} = 4.000V		±1/8	±1/2	Counts
Ratiometric Gain Error	V_{IN} = 4.000V		±1/2	±2	Counts
Gain Error Drift	V_{IN} = 4.000V, $0°C \leq T_A \leq +70°C$		±1		ppm/°C
Zero Reading Drift	V_{IN} = 0V		±1		ppm/°C
Analog Input Voltage Range				±11	V
Reference Input Voltage Range	Reference Varied	0		+12	V
Analog Input Leakage Current	V_{IN} = 0V		80	500	pA
Reference Input Leakage Current			1	100	nA
Analog Input Resistance	V_{IN} = 0V		1000		MΩ
Conversion Time	V_{IN} = 4.000V, f_C = 125 kHz			74	ms

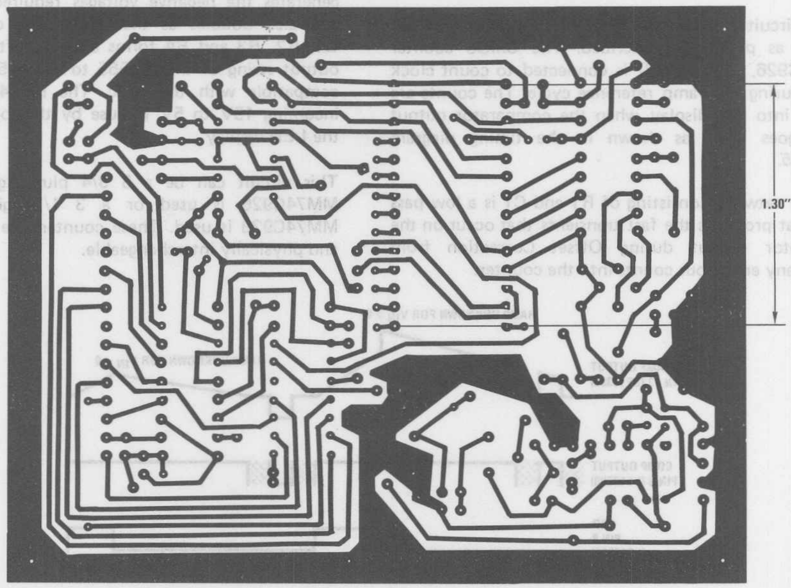


FIGURE 16. PC Board for 3 3/4 Plus (±8191 Counts) and 3 1/2-Digit DPM

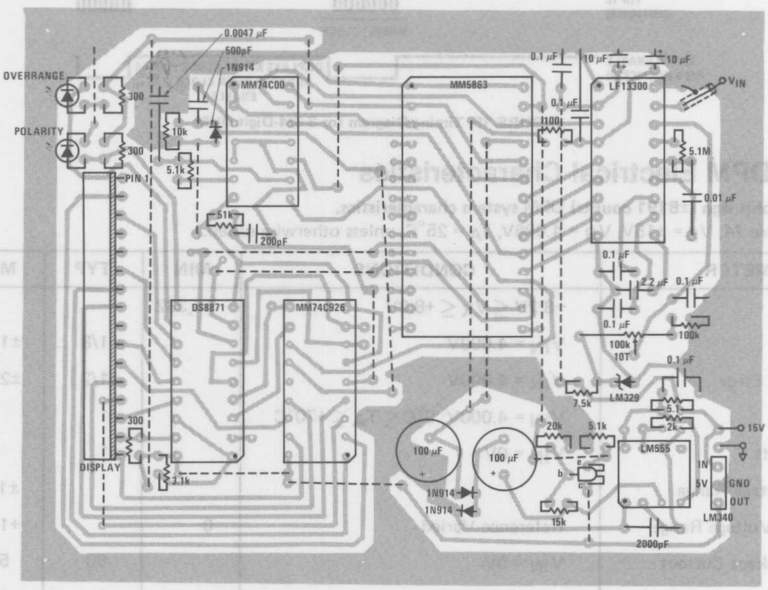
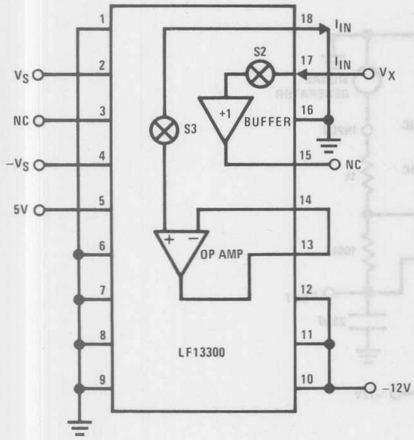


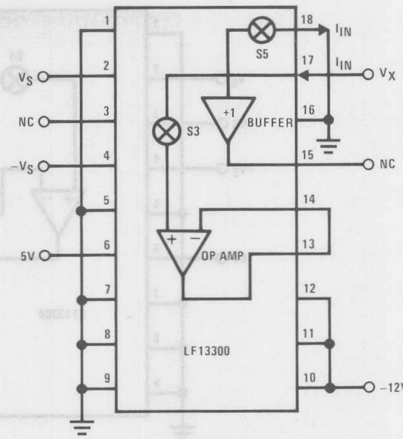
FIGURE 17. Stuffing Diagram for 3 3/4 Plus (±8191 Counts) and 3 1/2-Digit DPM

AC Test Circuits

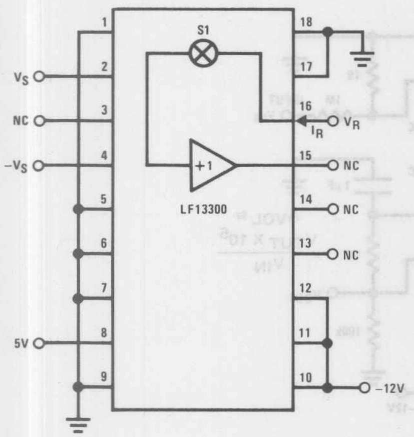
Test Circuit 1
Analog Input Characteristics Test with RU − High



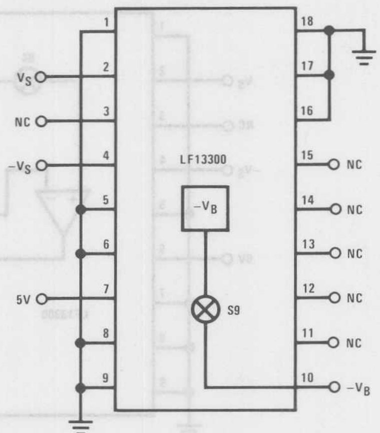
Test Circuit 2
Analog Input Characteristics Test with PD/RU+ High



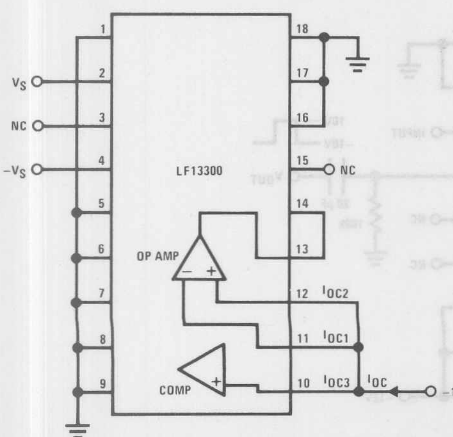
Test Circuit 3
Reference Input Characteristic Test with RR High



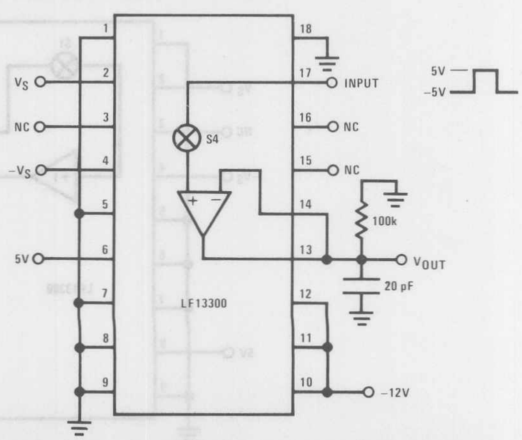
Test Circuit 4
−VB Voltage Measurement Test



Test Circuit 5
Offset Correction Input Current, I_{OC} Test

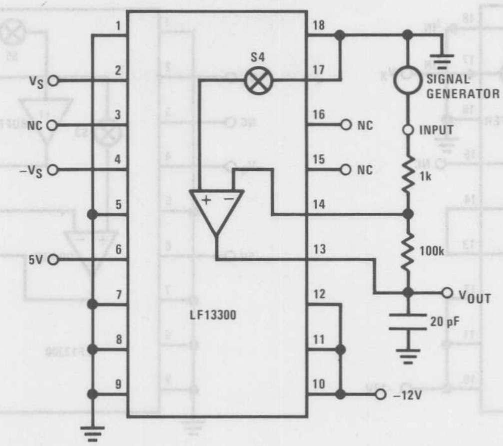


Test Circuit 6
Op Amp Slew Rate Test

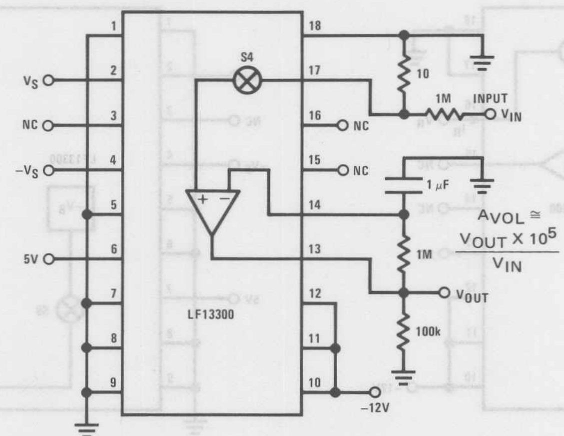


AC Test Circuits (Continued)

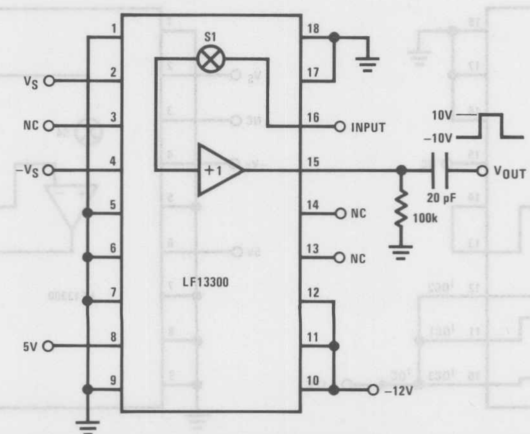
Test Circuit 7
Frequency Response Test



Test Circuit 8
Open Loop Gain Test

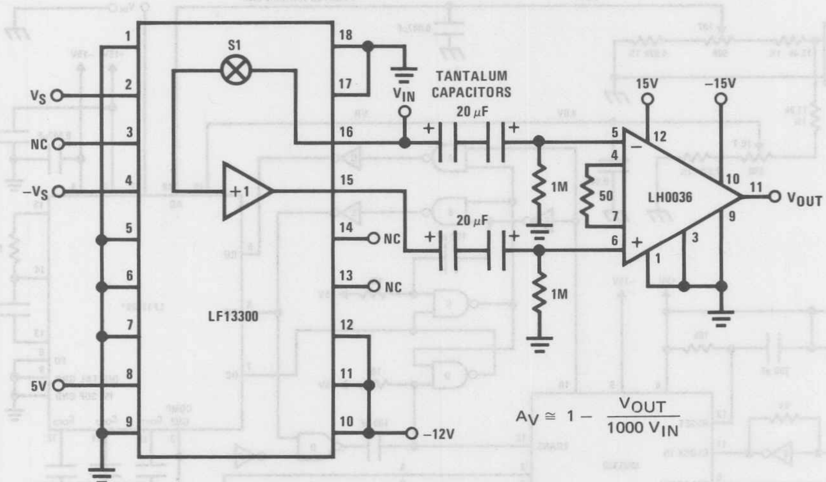


Test Circuit 9
Buffer Slew Rate Test

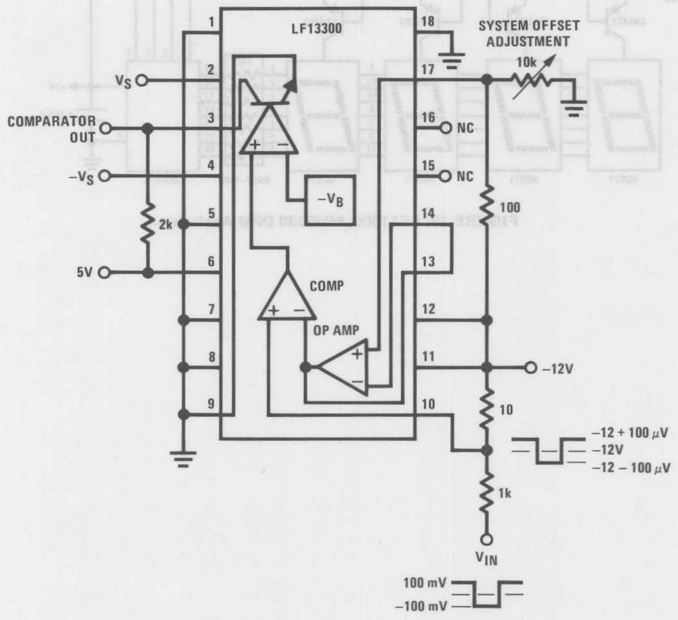


AC Test Circuits (Continued)

Test Circuit 10
Buffer Voltage Gain Test



Test Circuit 11
Comparator Response Time Test



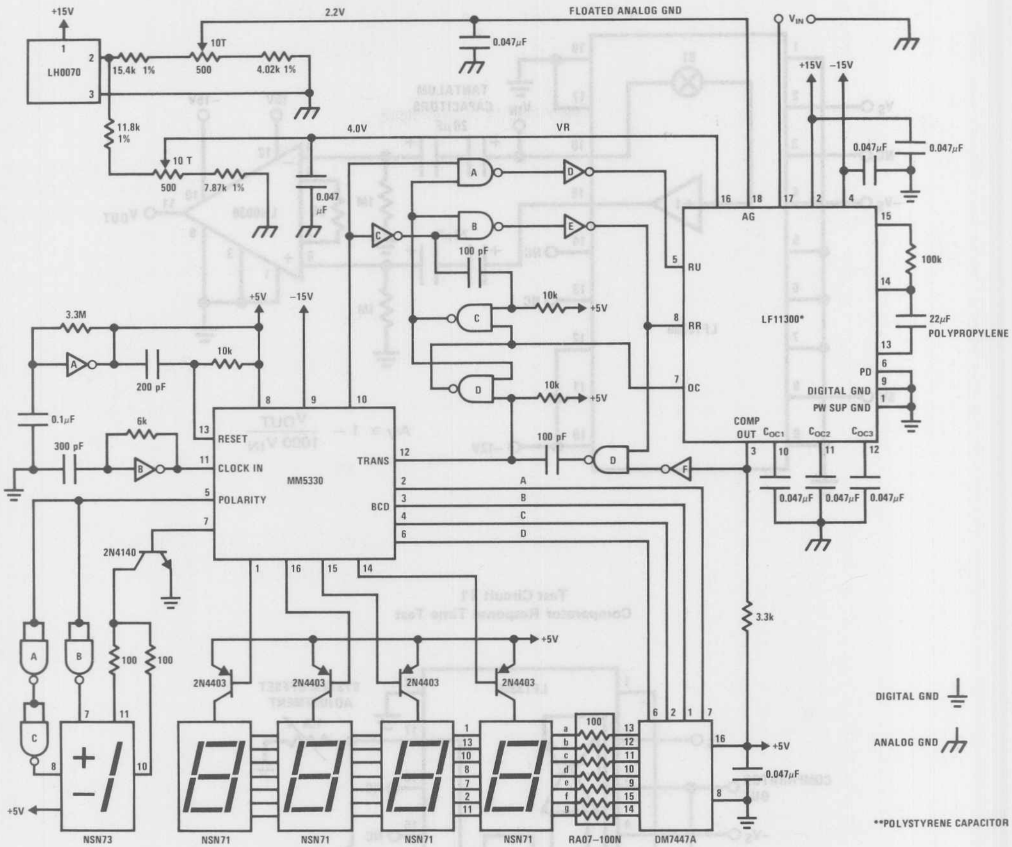


FIGURE 18. LF11300, MM5330 DPM Application

National Semiconductor

LM131A/LM131, LM231A/LM231, LM331A/LM331 Precision Voltage-to-Frequency Converters

General Description

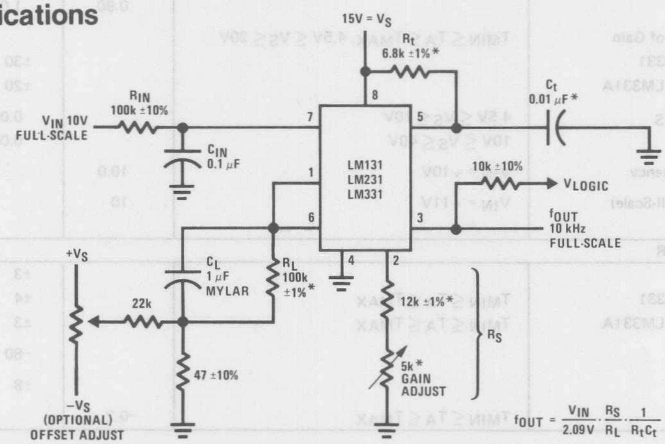
The LM131/LM231/LM331 family of voltage-to-frequency converters are ideally suited for use in simple low-cost circuits for analog-to-digital conversion, precision frequency-to-voltage conversion, long-term integration, linear frequency modulation or demodulation, and many other functions. The output when used as a voltage-to-frequency converter is a pulse train at a frequency precisely proportional to the applied input voltage. Thus, it provides all the inherent advantages of the voltage-to-frequency conversion techniques, and is easy to apply in all standard voltage-to-frequency converter applications. Further, the LM131A/LM231A/LM331A attains a new high level of accuracy versus temperature which could only be attained with expensive voltage-to-frequency modules. Additionally the LM131 is ideally suited for use in digital systems at low power supply voltages and can provide low-cost analog-to-digital conversion in microprocessor-controlled systems. And, the frequency from a battery powered voltage-to-frequency converter can be easily channeled through a simple photoisolator to provide isolation against high common mode levels.

The LM131/LM231/LM331 utilizes a new temperature-compensated band-gap reference circuit, to provide excellent accuracy over the full operating temperature range, at power supplies as low as 4.0V. The precision timer circuit has low bias currents without degrading the quick response necessary for 100 kHz voltage-to-frequency conversion. And the output is capable of driving 3 TTL loads, or a high voltage output up to 40V, yet is short-circuit-proof against V_{CC}.

Features

- Guaranteed linearity 0.01% max
- Improved performance in existing voltage-to-frequency conversion applications
- Split or single supply operation
- Operates on single 5V supply
- Pulse output compatible with all logic forms
- Excellent temperature stability, ±50 ppm/°C max
- Low power dissipation, 15 mW typical at 5V
- Wide dynamic range, 100 dB min at 10 kHz full scale frequency
- Wide range of full scale frequency, 1 Hz to 100 kHz
- Low cost

Typical Applications



*Use stable components with low temperature coefficients. See Typical Applications section.

FIGURE 1. Simple Stand-Alone Voltage-to-Frequency Converter with ±0.03% Typical Linearity (f = 10 Hz to 11 kHz)

LM131A/LM131, LM231A/LM231, LM331A/LM331

8

Absolute Maximum Ratings

	LM131A/LM131	LM231A/LM231	LM331A/LM331
Supply Voltage	40V	40V	40V
Output Short Circuit to Ground	Continuous	Continuous	Continuous
Output Short Circuit to V_{CC}	Continuous	Continuous	Continuous
Input Voltage	$-0.2V$ to $+V_S$	$-0.2V$ to $+V_S$	$-0.2V$ to $+V_S$
	T_{MIN} T_{MAX}	T_{MIN} T_{MAX}	T_{MIN} T_{MAX}
Operating Ambient Temperature Range	$-55^\circ C$ to $+125^\circ C$	$-25^\circ C$ to $+85^\circ C$	$0^\circ C$ to $+70^\circ C$
Power Dissipation (P_D at $25^\circ C$) and Thermal Resistance (θ_{jA})			
(H Package) P_D	670 mW	570 mW	570 mW
θ_{jA}	$150^\circ C/W$	$150^\circ C/W$	$150^\circ C/W$
(N Package) P_D		500 mW	500 mW
θ_{jA}		$155^\circ C/W$	$155^\circ C/W$

Electrical Characteristics $T_A = 25^\circ C$ unless otherwise specified. (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VFC Non-Linearity (Note 2)	$4.5V \leq V_S \leq 20V$		±0.003	±0.01	% Full-Scale
	$T_{MIN} \leq T_A \leq T_{MAX}$		±0.006	±0.02	% Full-Scale
In Circuit of *Figure 1*	$V_S = 15V$, f = 10 Hz to 11 kHz		±0.024	±0.14	% Full-Scale
Conversion Accuracy Scale Factor (Gain)	$V_{IN} = -10V$, $R_S = 14\ k\Omega$				
LM131, LM131A, LM231, LM231A		0.95	1.00	1.05	kHz/V
LM331, LM331A		0.90	1.00	1.10	kHz/V
Temperature Stability of Gain	$T_{MIN} \leq T_A \leq T_{MAX}$, $4.5V \leq V_S \leq 20V$				
LM131/LM231/LM331			±30	±150	ppm/°C
LM131A/LM231A/LM331A			±20	±50	ppm/°C
Change of Gain with V_S	$4.5V \leq V_S \leq 10V$		0.01	0.1	%/V
	$10V \leq V_S \leq 40V$		0.006	0.06	%/V
Rated Full-Scale Frequency	$V_{IN} = -10V$	10.0			kHz
Overrange (Beyond Full-Scale) Frequency	$V_{IN} = -11V$	10			%
INPUT COMPARATOR					
Offset Voltage			±3	±10	mV
LM131/LM231/LM331	$T_{MIN} \leq T_A \leq T_{MAX}$		±4	±14	mV
LM131A/LM231A/LM331A	$T_{MIN} \leq T_A \leq T_{MAX}$		±3	±10	mV
Bias Current			−80	−300	nA
Offset Current			±8	±100	nA
Common-Mode Range	$T_{MIN} \leq T_A \leq T_{MAX}$	−0.2		$V_{CC}-2.0$	V
TIMER					
Timer Threshold Voltage, Pin 5		0.63	0.667	0.70	$\times V_S$
Input Bias Current, Pin 5	$V_S = 15V$				
All Devices	$0V \leq V_{PIN\ 5} \leq 9.9V$		±10	±100	nA
LM131/LM231/LM331	$V_{PIN\ 5} = 10V$		200	1000	nA
LM131A/LM231A/LM331A	$V_{PIN\ 5} = 10V$		200	500	nA
$V_{SAT\ PIN\ 5}$ (Reset)	I = 5 mA		0.22	0.5	V

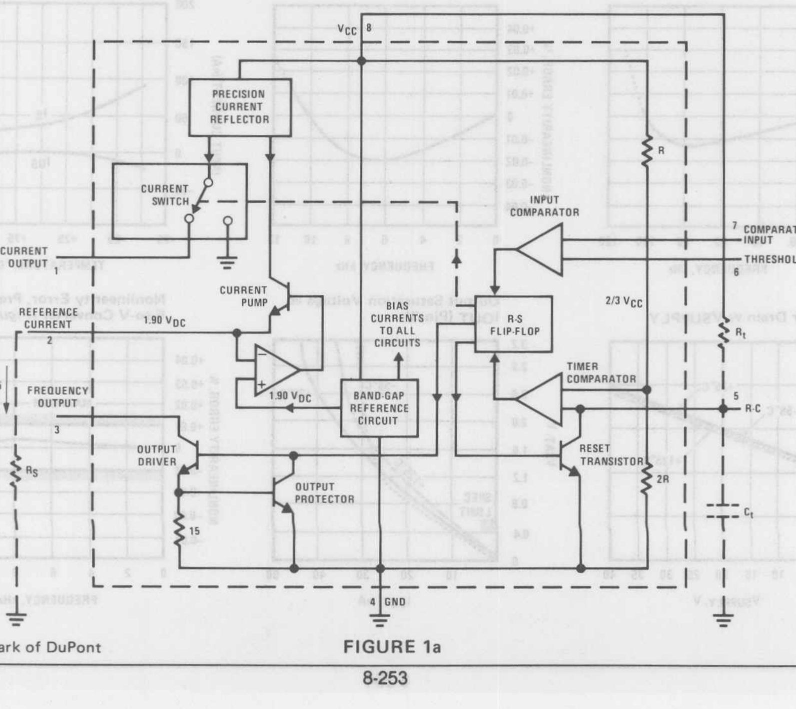
Electrical Characteristics (Continued) $T_A = 25^{\circ}C$ unless otherwise specified (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT SOURCE (Pin 1)					
Output Current	$R_S = 14\ k\Omega$, $V_{PIN\ 1} = 0$				
LM131, LM131A, LM231, LM231A		126	135	144	μA
LM331, LM331A		116	136	156	μA
Change with Voltage	$0V \leq V_{PIN\ 1} \leq 10V$		0.2	1.0	μA
Current Source OFF Leakage					
LM131, LM131A			0.01	1.0	nA
LM231, LM231A, LM331, LM331A			0.02	10.0	nA
All Devices	$T_A = T_{MAX}$		2.0	50.0	nA
Operating Range of Current (Typical)			(10 to 500)		μA
REFERENCE VOLTAGE (Pin 2)					
LM131, LM131A, LM231, LM231A		1.76	1.89	2.02	V_{DC}
LM331, LM331A		1.70	1.89	2.08	V_{DC}
Stability vs Temperature			±60		ppm/°C
Stability vs Time, 1000 Hours			±0.1		%
LOGIC OUTPUT (Pin 3)					
V_{SAT}	I = 5 mA		0.15	0.50	V
	I = 3.2 mA (2 TTL Loads), $T_{MIN} \leq T_A \leq T_{MAX}$		0.10	0.40	V
OFF Leakage			±0.05	1.0	μA
SUPPLY CURRENT					
LM131, LM131A, LM231,	$V_S = 5V$	2.0	3.0	4.0	mA
LM231A	$V_S = 40V$	2.5	4.0	6.0	mA
LM331, LM331A	$V_S = 5V$	1.5	3.0	6.0	mA
	$V_S = 40V$	2.0	4.0	8.0	mA

Note 1: All specifications apply in the circuit of *Figure 3*, with $4.0V \leq V_S \leq 40V$, unless otherwise noted.

Note 2: Nonlinearity is defined as the deviation of f_{OUT} from $V_{IN} \times (10\ kHz/-10\ V_{DC})$ when the circuit has been trimmed for zero error at 10 Hz and at 10 kHz, over the frequency range 1 Hz to 11 kHz. For the timing capacitor, C_T, use NPO ceramic, Teflon*, or polystyrene.

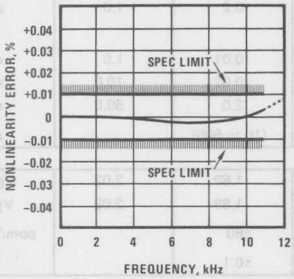
Functional Block Diagrams



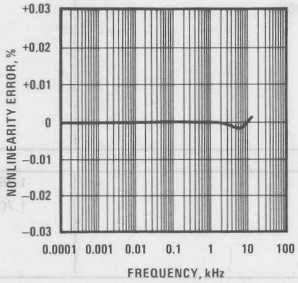
*Registered trademark of DuPont

FIGURE 1a

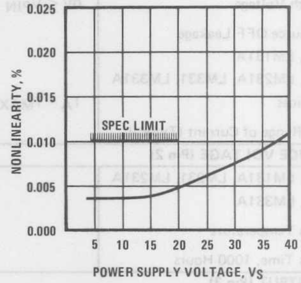
Nonlinearity Error, LM131 Family, as Precision V-to-F Converter *(Figure 3)*



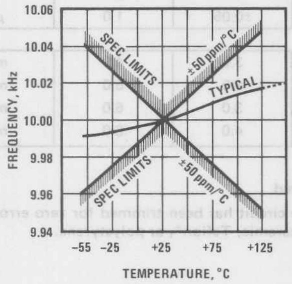
Nonlinearity Error, LM131 Family



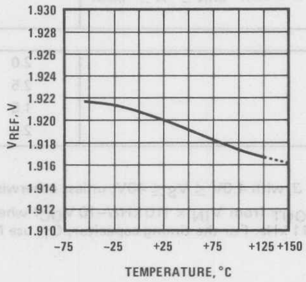
Nonlinearity vs Power Supply Voltage



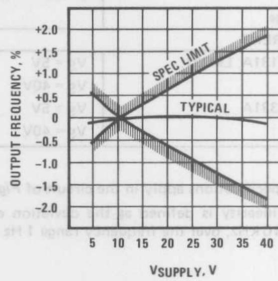
Frequency vs Temperature, LM131A



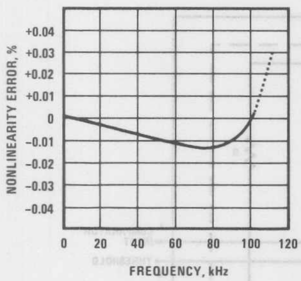
V_{REF} vs Temperature, LM131A



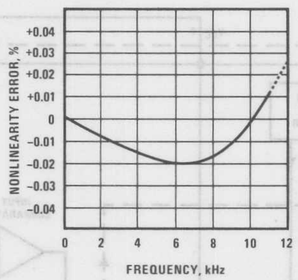
Output Frequency vs V_{SUPPLY}



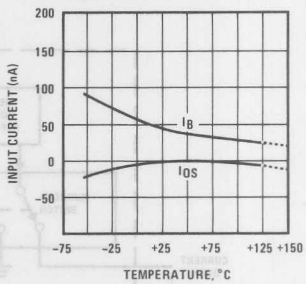
100kHz Nonlinearity Error, LM131 Family *(Figure 4)*



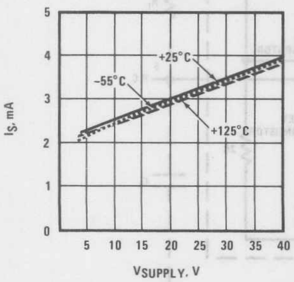
Nonlinearity Error, LM131 *(Figure 1)*



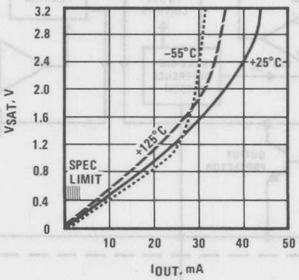
Input Current (Pins 6, 7) vs Temperature



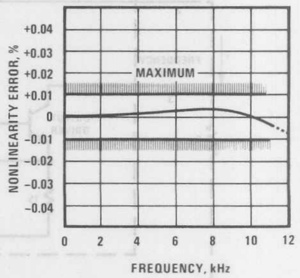
Power Drain vs V_{SUPPLY}



Output Saturation Voltage vs I_{OUT} (Pin 3)



Nonlinearity Error, Precision F-to-V Converter *(Figure 6)*



Typical Applications (Continued)

PRINCIPLES OF OPERATION OF A SIMPLIFIED VOLTAGE-TO-FREQUENCY CONVERTER

The LM131 is a monolithic circuit designed for accuracy and versatile operation when applied as a voltage-to-frequency (V-to-F) converter or as a frequency-to-voltage (F-to-V) converter. A simplified block diagram of the LM131 is shown in *Figure 2* and consists of a switched current source, input comparator, and 1-shot timer.

The operation of these blocks is best understood by going through the operating cycle of the basic V-to-F converter, *Figure 2*, which consists of the simplified block diagram of the LM131 and the various resistors and capacitors connected to it.

The voltage comparator compares a positive input voltage, V1, at pin 7 to the voltage, V_x, at pin 6. If V1 is greater, the comparator will trigger the 1-shot timer. The output of the timer will turn ON both the frequency output transistor and the switched current source for a period $t = 1.1\ R_tC_t$. During this period, the current i will flow out of the switched current source and provide a fixed amount of charge, $Q = i \times t$, into the capacitor, C_L. This will normally charge V_x up to a higher level than V1. At the end of the timing period, the current i will turn OFF, and the timer will reset itself.

Now there is no current flowing from pin 1, and the capacitor C_L will be gradually discharged by R_L until V_x falls to the level of V1. Then the comparator will trigger the timer and start another cycle.

The current flowing into C_L is exactly $I_{AVE} = i \times (1.1 \times R_tC_t) \times f$, and the current flowing out of C_L is exactly $V_x/R_L \cong V_{IN}/R_L$. If V_{IN} is doubled, the frequency will double to maintain this balance. Even a simple V-to-F converter can provide a frequency precisely proportional to its input voltage over a wide range of frequencies.

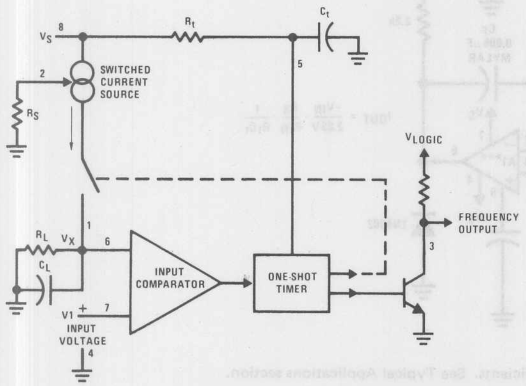


FIGURE 2. Simplified Block Diagram of Stand-Alone Voltage-to-Frequency Converter Showing LM131 and External Components

DETAIL OF OPERATION, FUNCTIONAL BLOCK DIAGRAM *(FIGURE 1a)*

The block diagram shows a band gap reference which provides a stable 1.9 V_{DC} output. This 1.9 V_{DC} is well regulated over a V_s range of 3.9V to 40V. It also has a flat, low temperature coefficient, and typically changes less than 1/2% over a 100°C temperature change.

The current pump circuit forces the voltage at pin 2 to be at 1.9V, and causes a current $i = 1.90V/R_s$ to flow. For $R_s = 14k$, $i = 135\ \mu A$. The precision current reflector provides a current equal to i to the current switch. The current switch switches the current to pin 1 or to ground depending on the state of the R_S flip-flop.

The timing function consists of an R_S flip-flop, and a timer comparator connected to the external R_tC_t network. When the input comparator detects a voltage at pin 7 higher than pin 6, it sets the R_S flip-flop which turns ON the current switch and the output driver transistor. When the voltage at pin 5 rises to 2/3 V_{CC}, the timer comparator causes the R_S flip-flop to reset. The reset transistor is then turned ON and the current switch is turned OFF.

However, if the input comparator still detects pin 7 higher than pin 6 when pin 5 crosses 2/3 V_{CC}, the flip-flop will not be reset, and the current at pin 1 will continue to flow, in its attempt to make the voltage at pin 6 higher than pin 7. This condition will usually apply under start-up conditions or in the case of an overload voltage at signal input. It should be noted that during this sort of overload, the output frequency will be 0; as soon as the signal is restored to the working range, the output frequency will be resumed.

The output driver transistor acts to saturate pin 3 with an ON resistance of about 50Ω. In case of overvoltage, the output current is actively limited to less than 50 mA.

The voltage at pin 2 is regulated at 1.90 V_{DC} for all values of i between 10 μA to 500 μA. It can be used as a voltage reference for other components, but care must be taken to ensure that current is not taken from it which could reduce the accuracy of the converter.

PRINCIPLES OF OPERATION OF BASIC VOLTAGE-TO-FREQUENCY CONVERTER *(FIGURE 1)*

The simple stand-alone V-to-F converter shown in *Figure 1* includes all the basic circuitry of *Figure 2* plus a few components for improved performance.

A resistor, $R_{IN} = 100\ k\Omega \pm 10\%$, has been added in the path to pin 7, so that the bias current at pin 7 (−80 nA typical) will cancel the effect of the bias current at pin 6 and help provide minimum frequency offset.

The resistance R_s at pin 2 is made up of a 12 kΩ fixed resistor plus a 5 kΩ (cermet, preferably) gain adjust rheostat. The function of this adjustment is to trim out the gain tolerance of the LM131, and the tolerance of R_t, R_L and C_t. For best results, all the components

Typical Applications (Continued)

should be stable low-temperature-coefficient components, such as metal-film resistors. The capacitor should have low dielectric absorption; depending on the temperature characteristics desired, NPO ceramic, polystyrene, Teflon* or polypropylene are best suited.

A capacitor is added from pin 7 to ground to act as a filter for V_{IN}. A value of 0.01 μF to 0.1 μF will be adequate in most cases; however, in cases where better filtering is required, a 1 μF capacitor can be used. When the RC time constants are matched at pin 6 and pin 7, a voltage step at V_{IN} will cause a step change in f_{OUT}. If C_{IN} is much less than C_L, a step at V_{IN} may cause f_{OUT} to stop momentarily.

A 47Ω resistor, in series with the 1 μF C_L, is added to give hysteresis effect which helps the input comparator provide the excellent linearity (0.03% typical).

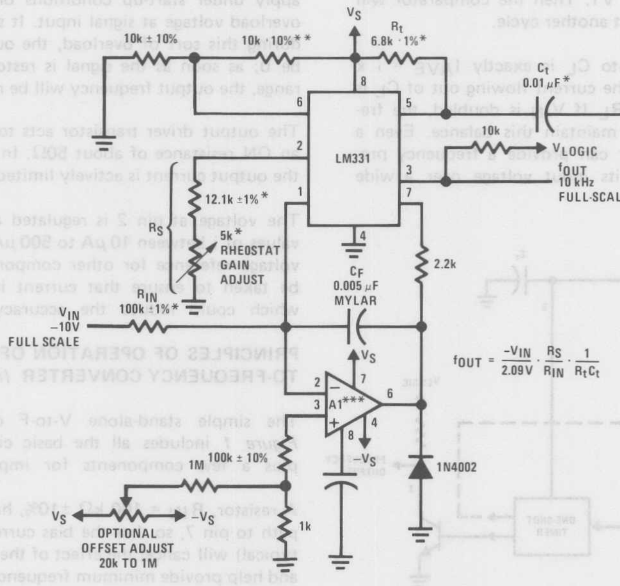
DETAIL OF OPERATION OF PRECISION V-TO-F CONVERTER *(FIGURE 3)*

In this circuit, integration is performed by using a conventional operational amplifier and feedback capacitor, C_F. When the integrator's output crosses the nominal threshold level at pin 6 of the LM131, the timing cycle is initiated. The average current fed into the op amp's summing point (pin 2) is i × (1.1 R_tC_t) × f which is perfectly balanced with $-V_{IN}/R_{IN}$. In this circuit, the voltage offset of the LM131 input comparator does not affect the offset or accuracy of the V-to-F converter as it does in the stand-alone V-to-F converter; nor does the LM131 bias current or offset current. Instead, the offset voltage and offset current of the operational amplifier are the only limits on how small the signal can be accurately converted. Since op amps with voltage offset well below 1 mV and offset currents well below 2 nA are available at low cost, this circuit is recommended for best accuracy for small signals. This circuit also responds immediately to any change of input signal (which a stand-alone circuit does not) so that the output frequency will be an accurate representation of V_{IN}, as quickly as 2 output pulses' spacing can be measured.

In the precision mode, excellent linearity is obtained because the current source (pin 1) is always at ground potential and that voltage does not vary with V_{IN} or f_{OUT}. (In the stand-alone V-to-F converter, a major cause of non-linearity is the output impedance at pin 1 which causes i to change as a function of V_{IN}).

The circuit of *Figure 4* operates in the same way as *Figure 3*, but with the necessary changes for high speed operation.

*Registered trademark of DuPont



*Use stable components with low temperature coefficients. See Typical Applications section.

**This resistor can be 5 kΩ or 10 kΩ for V_S = 8V to 22V, but must be 10 kΩ for V_S = 4.5V to 8V.

***Use low offset voltage and low offset current op amps for A1: recommended types LM108, LM308A, LF351B

FIGURE 3. Standard Test Circuit and Applications Circuit, Precision Voltage-to-Frequency Converter

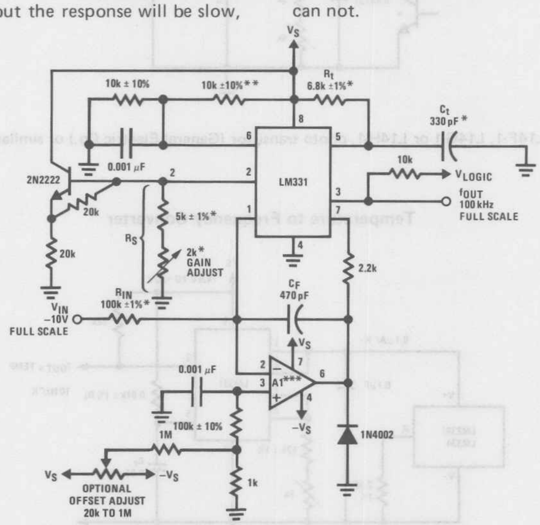
Typical Applications (Continued)

DETAILS OF OPERATION, FREQUENCY-TO-VOLTAGE CONVERTERS ***(FIGURES 5 AND 6)***

In these applications, a pulse input at f_{IN} is differentiated by a C-R network and the negative-going edge at pin 6 causes the input comparator to trigger the timer circuit. Just as with a V-to-F converter, the average current flowing out of pin 1 is $I_{AVERAGE} = i \times (1.1\ R_tC_t) \times f$.

In the simple circuit of *Figure 5*, this current is filtered in the network $R_L = 100\ k\Omega$ and $1\ \mu F$. The ripple will be less than 10 mV peak, but the response will be slow, with a 0.1 second time constant, and settling of 0.7 second to 0.1% accuracy.

In the precision circuit, an operational amplifier provides a buffered output and also acts as a 2-pole filter. The ripple will be less than 5 mV peak for all frequencies above 1 kHz, and the response time will be much quicker than in *Figure 5*. However, for input frequencies below 200 Hz, this circuit will have worse ripple than *Figure 5*. The engineering of the filter time-constants to get adequate response and small enough ripple simply requires a study of the compromises to be made. Inherently, V-to-F converter response can be fast, but F-to-V response can not.

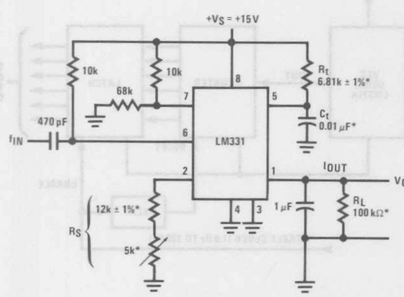


*Use stable components with low temperature coefficients. See Typical Applications section.

**This resistor can be 5 kΩ or 10 kΩ for V_S = 8V to 22V, but must be 10 kΩ for V_S = 4.5V to 8V.

***Use low offset voltage and low offset current op amps for A1: recommended types LF351B or LF356.

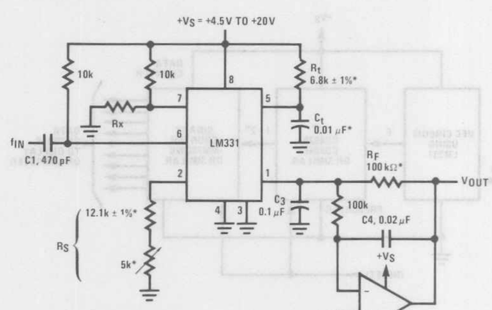
FIGURE 4. Precision Voltage-to-Frequency Converter, 100 kHz Full-Scale, ±0.03% Non-Linearity



$V_{OUT} = f_{IN} \times 2.09V \times \frac{R_L}{R_S} \times (R_tC_t)$

*Use stable components with low temperature coefficients.

FIGURE 5. Simple Frequency-to-Voltage Converter, 10 kHz Full-Scale, ±0.06% Non-Linearity



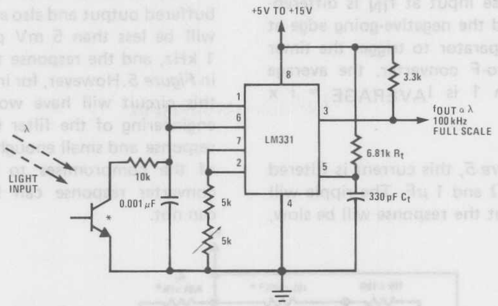
$V_{OUT} = -f_{IN} \times 2.09V \times \frac{R_F}{R_S} \times (R_tC_t)$

$\text{SELECT } R_X = \frac{(V_S - 2V)}{0.2\ mA}$

*Use stable components with low temperature coefficients.

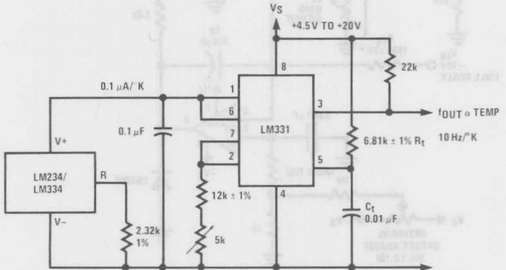
FIGURE 6. Precision Frequency-to-Voltage Converter, 10 kHz Full-Scale with 2-Pole Filter, ±0.01% Non-Linearity Maximum

Light Intensity to Frequency Converter

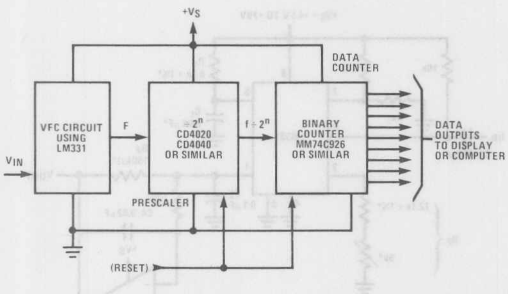


*L14F-1, L14G-1 or L14H-1, photo transistor (General Electric Co.) or similar

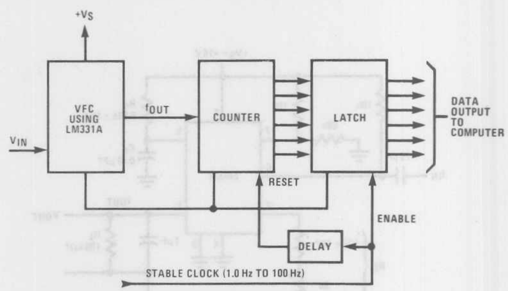
Temperature to Frequency Converter



Long-Term Digital Integrator Using VFC

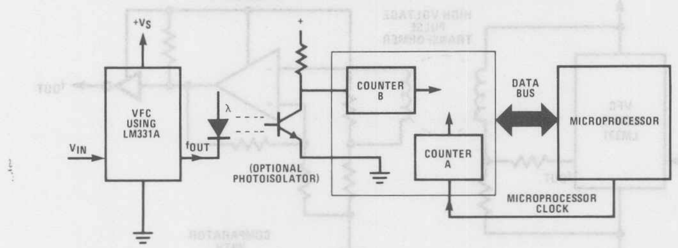


Basic Analog-to-Digital Converter Using Voltage-to-Frequency Converter

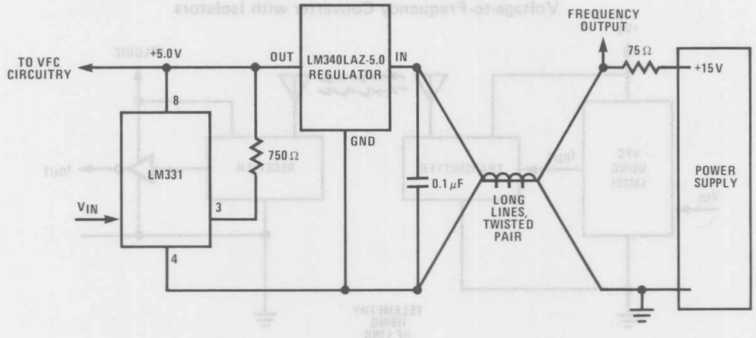


Typical Applications (Continued)

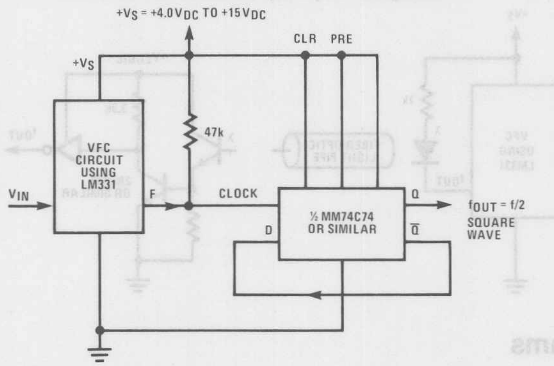
Analog-to-Digital Converter with Microprocessor



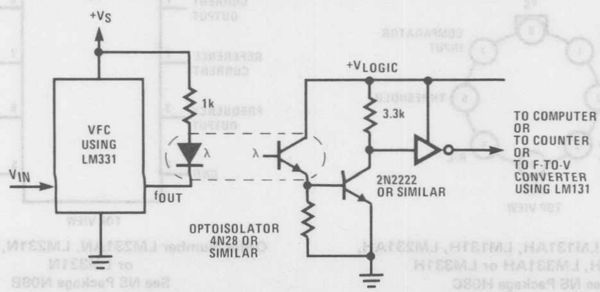
Remote Voltage-to-Frequency Converter with 2-Wire Transmitter and Receiver



Voltage-to-Frequency Converter with Square-Wave Output Using ÷2 Flip-Flop

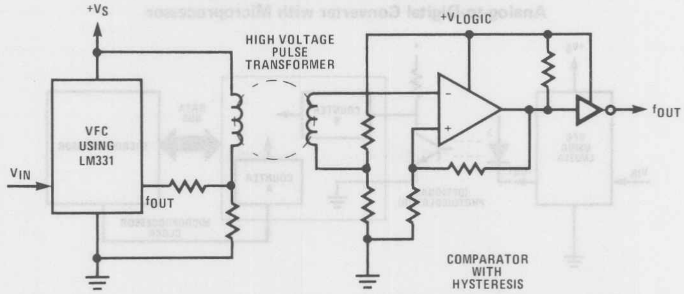


Voltage-to-Frequency Converter with Isolators

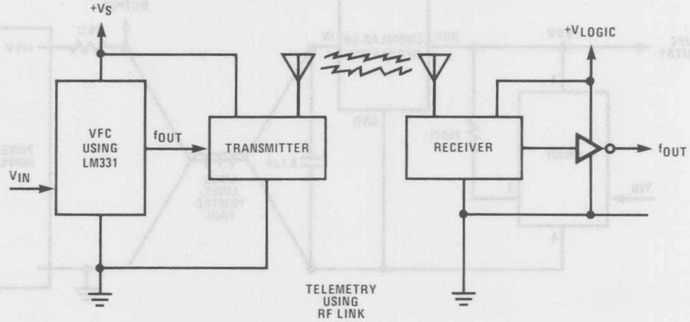


Typical Applications (Continued)

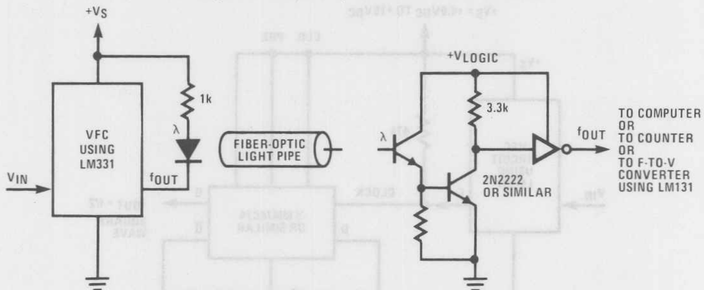
Voltage-to-Frequency Converter with Isolators



Voltage-to-Frequency Converter with Isolators

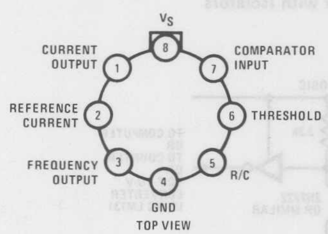


Voltage-to-Frequency Converter with Isolators



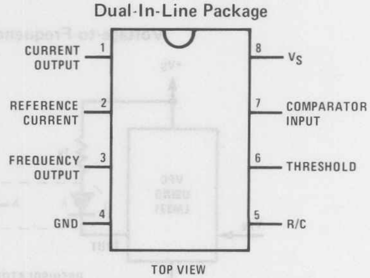
Connection Diagrams

Metal Can Package



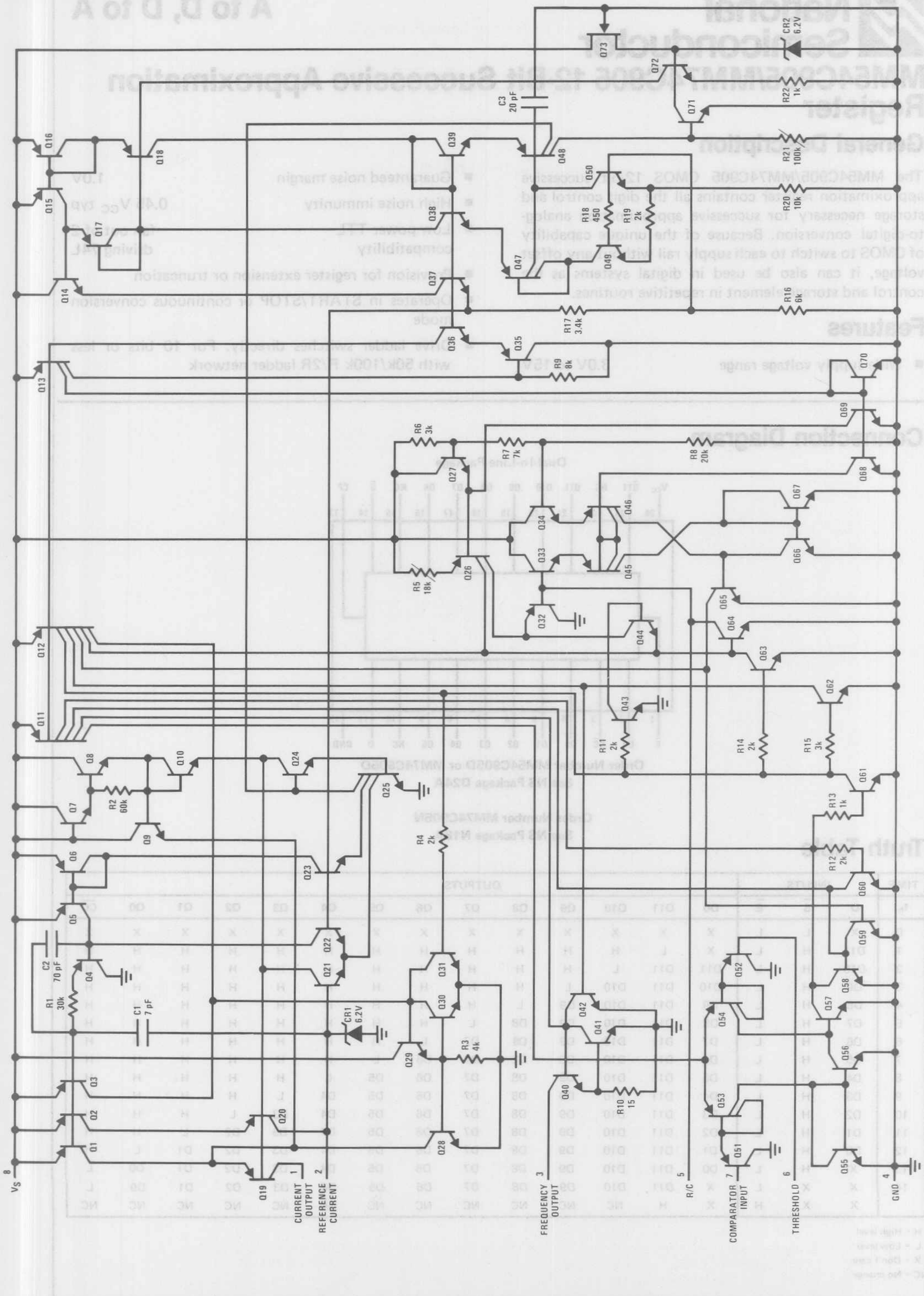
Order Number LM131AH, LM131H, LM231AH, LM231H, LM331AH or LM331H
See NS Package H08C

Dual-In-Line Package



Order Number LM231AN, LM231N, LM331AN, or LM331N
See NS Package N08B

Schematic Diagram



MM54C905/MM74C905 12-Bit Successive Approximation Register

General Description

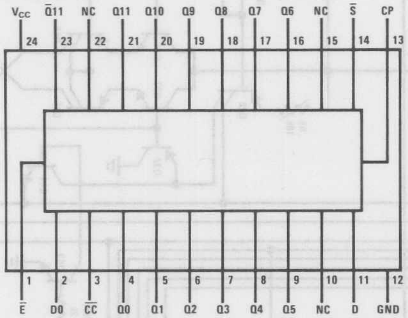
The MM54C905/MM74C905 CMOS 12-bit successive approximation register contains all the digit control and storage necessary for successive approximation analog-to-digital conversion. Because of the unique capability of CMOS to switch to each supply rail without any offset voltage, it can also be used in digital systems as the control and storage element in repetitive routines.

Features

- Wide supply voltage range 3.0V to 15V
- Guaranteed noise margin 1.0V
- High noise immunity 0.45 V_{CC} typ
- Low power TTL compatibility fan out of 2 driving 74L
- Provision for register extension or truncation
- Operates in START/STOP or continuous conversion mode
- Drive ladder switches directly. For 10 bits or less with 50k/100k R/2R ladder network

Connection Diagram

Dual-In-Line Package



Order Number MM54C905D or MM74C905D
See NS Package D24A

Order Number MM74C905N
See NS Package N18A

Truth Table

TIME	INPUTS			OUTPUTS													
t_n	D	$\overline{S}$	$\overline{E}$	D0	Q11	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	$\overline{CC}$
0	X	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X
1	D11	H	L	X	L	H	H	H	H	H	H	H	H	H	H	H	H
2	D10	H	L	D11	D11	L	H	H	H	H	H	H	H	H	H	H	H
3	D9	H	L	D10	D11	D10	L	H	H	H	H	H	H	H	H	H	H
4	D8	H	L	D9	D11	D10	D9	L	H	H	H	H	H	H	H	H	H
5	D7	H	L	D8	D11	D10	D9	D8	L	H	H	H	H	H	H	H	H
6	D6	H	L	D7	D11	D10	D9	D8	D7	L	H	H	H	H	H	H	H
7	D5	H	L	D6	D11	D10	D9	D8	D7	D6	L	H	H	H	H	H	H
8	D4	H	L	D5	D11	D10	D9	D8	D7	D6	D5	L	H	H	H	H	H
9	D3	H	L	D4	D11	D10	D9	D8	D7	D6	D5	D4	L	H	H	H	H
10	D2	H	L	D3	D11	D10	D9	D8	D7	D6	D5	D4	D3	L	H	H	H
11	D1	H	L	D2	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	L	H	H
12	D0	H	L	D1	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	L	H
13	X	H	L	D0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	L
14	X	X	L	X	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	L
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC

H = High level
L = Low level
X = Don't care
NC = No change

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} +0.3V
Operating Temperature Range	
MM54C905	−55°C to +125°C
MM74C905	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	16V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V V_{CC} = 10V	3.5 8.0			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V V_{CC} = 10V			1.5 2.0	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA V_{CC} = 10V, I_O = −10μA	4.5 9.0			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = 10μA V_{CC} = 10V, I_O = 10μA			0.5 1.0	V V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	300	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$) MM54C905 MM74C905	 V_{CC} = 4.5V V_{CC} = 4.75V	 V_{CC}−1.5 V_{CC}−1.5			 V V
Logical "0" Input Voltage ($V_{IN(0)}$) MM54C905 MM74C905	 V_{CC} = 4.5V V_{CC} = 4.75V			 0.8 0.8	 V V
Logical "1" Output Voltage ($V_{OUT(1)}$) MM54C905 MM74C905	 V_{CC} = 4.5V, I_O = −360μA V_{CC} = 4.75V, I_O = −360μA	 2.4 2.4			 V V
Logical "0" Output Voltage ($V_{OUT(0)}$) MM54C905 MM74C905	 V_{CC} = 4.5V, I_O = 360μA V_{CC} = 4.75V, I_O = 360μA			 0.4 0.4	 V V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V T_A = 25°C	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V T_A = 25°C	−8.0	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC} T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC} T_A = 25°C	8.0	16		mA
Q11–Q0 Outputs R_{SOURCE}	V_{CC} = 10V ±5% V_{OUT} = V_{CC} − 0.3V T_A = 25°C	150		350	Ω
R_{SINK}	V_{CC} = 10V ±5% V_{OUT} = 0.3V T_A = 25°C	80		230	Ω

AC Electrical Characteristics $T_A = 25^\circ C$, $C_L = 50$ pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time From Clock Input To Outputs (Q0–Q11) ($t_{pd(Q)}$)	$V_{CC} = 5.0V$		200	350	ns
	$V_{CC} = 10V$		80	150	ns
Propagation Delay Time From Clock Input To D_O ($t_{pd(D_O)}$)	$V_{CC} = 5.0V$		180	325	ns
	$V_{CC} = 10V$		70	125	ns
Propagation Delay Time From Register Enable ($\overline{E}$) To Output (Q11) ($t_{pd(\overline{E})}$)	$V_{CC} = 5.0V$		190	350	ns
	$V_{CC} = 10V$		75	150	ns
Propagation Delay Time From Clock To $\overline{CC}$ ($t_{pd(\overline{CC})}$)	$V_{CC} = 5.0V$		190	350	ns
	$V_{CC} = 10V$		75	0.50	ns
Data Input Set-Up Time (t_{DS})	$V_{CC} = 5.0V$	80			ns
	$V_{CC} = 10V$	30			ns
Start Input Set-Up Time (t_{SS})	$V_{CC} = 5.0V$	80			ns
	$V_{CC} = 10V$	30			ns
Minimum Clock Pulse Width (t_{PWL}, t_{PWH})	$V_{CC} = 5.0V$	250	125		ns
	$V_{CC} = 10V$	100	50		ns
Maximum Clock Rise and Fall Time (t_r, t_f)	$V_{CC} = 5.0V$			15	μs
	$V_{CC} = 10V$			5	μs
Maximum Clock Frequency (f_{MAX})	$V_{CC} = 5.0V$	2	4		MHz
	$V_{CC} = 10V$	5	10		MHz
Clock Input Capacitance (C_{CLK})	Clock Input (Note 2)		10		pF
Input Capacitance (C_{IN})	Any Other Input (Note 2)		5		pF
Power Dissipation Capacitance (C_{PD})	(Note 3)		100		pF

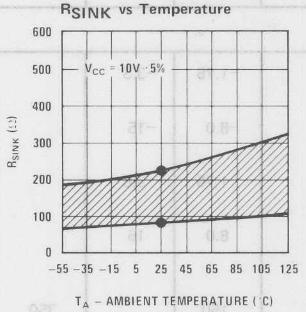
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

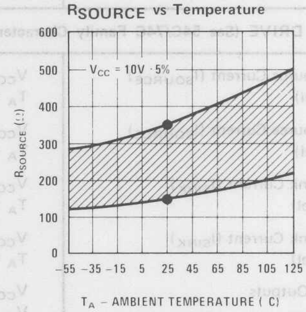
Typical Performance Characteristics

R_{SINK} vs Temperature



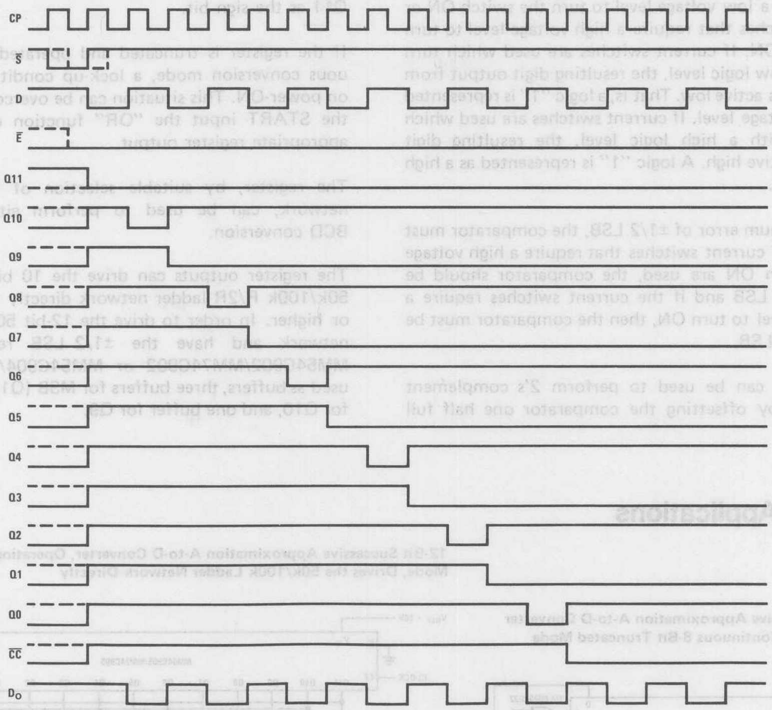
● These points are guaranteed by automatic testing.

R_{SOURCE} vs Temperature

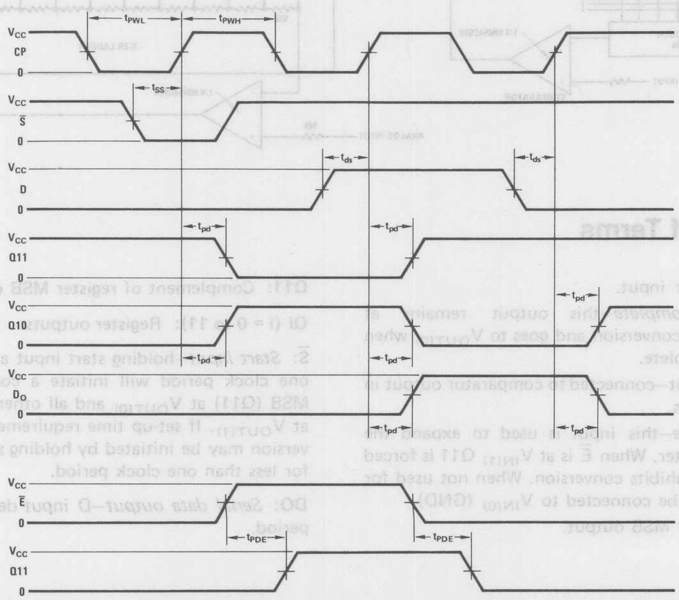


● These points are guaranteed by automatic testing.

Timing Diagram



Switching Time Waveforms



current switches that require a high voltage level to turn the switch ON. If current switches are used which turn ON with a low logic level, the resulting digit output from the register is active low. That is, a logic "1" is represented as a low voltage level. If current switches are used which turn ON with a high logic level, the resulting digit output is active high. A logic "1" is represented as a high voltage level.

For a maximum error of ±1/2 LSB, the comparator must be biased. If current switches that require a high voltage level to turn ON are used, the comparator should be biased +1/2 LSB and if the current switches require a low logic level to turn ON, then the comparator must be biased −1/2 LSB.

The register can be used to perform 2's complement conversion by offsetting the comparator one half full

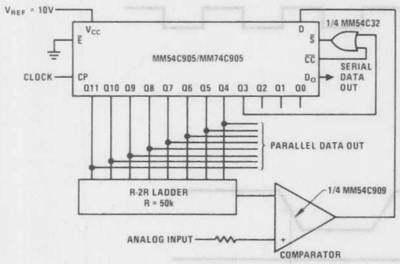
If the register is truncated and operated in the continuous conversion mode, a lock-up condition may occur on power-ON. This situation can be overcome by making the START input the "OR" function of $\overline{CC}$ and the appropriate register output.

The register, by suitable selection of register ladder network, can be used to perform either binary or BCD conversion.

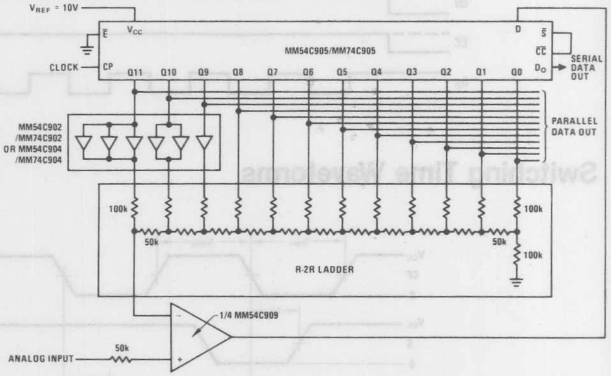
The register outputs can drive the 10 bits or less with 50k/100k R/2R ladder network directly for V_{CC} = 10V or higher. In order to drive the 12-bit 50k/100k ladder network and have the ±1/2 LSB resolution, the MM54C902/MM74C902 or MM54C904/MM74C904 is used as buffers, three buffers for MSB (Q11), two buffers for Q10, and one buffer for Q9.

Typical Applications

12-Bit Successive Approximation A-to-D Converter Operating in Continuous 8-Bit Truncated Mode



12-Bit Successive Approximation A-to-D Converter, Operating in Continuous Mode, Drives the 50k/100k Ladder Network Directly



Definition of Terms

CP: Register *clock* input.

$\overline{\text{CC}}$: *Conversion complete*—this output remains at $V_{OUT(1)}$ during a conversion and goes to $V_{OUT(0)}$ when conversion is complete.

D: Serial *data* input—connected to comparator output in A-to-D applications.

$\overline{\text{E}}$: *Register enable*—this input is used to expand the length of the register. When $\overline{E}$ is at $V_{IN(1)}$ Q11 is forced to $V_{OUT(1)}$ and inhibits conversion. When not used for expansion $\overline{E}$ must be connected to $V_{IN(0)}$ (GND).

Q11: True register MSB output.

$\overline{\text{Q11}}$: Complement of register MSB output.

Qi (i = 0 to 11): Register outputs.

$\overline{\text{S}}$: *Start input*—holding start input at $V_{IN(0)}$ for at least one clock period will initiate a conversion by setting MSB (Q11) at $V_{OUT(0)}$ and all other output (Q10—Q0) at $V_{OUT(1)}$. If set-up time requirements are met, a conversion may be initiated by holding start input at $V_{IN(0)}$ for less than one clock period.

DO: *Serial data output*—D input delayed by one clock period.

Section 9

Industrial Blocks
Functional
Automotive
Telecommunications
Monolithic Filters

9

Industrial Blocks: Functional/Automotive/ Telecommunications/Monolithic Filters

Section Contents

Section Contents (Continued)

9

Capacitor Saturation Voltage: The offset voltage remaining on the timing capacitor after capacitor discharge current has dropped to zero.

Collector Saturation Voltage: The collector to emitter voltage on the output transistor when it is in the "ON" state with specified sink current flowing into the collector terminal.

Common-Mode Rejection Ratio: The ratio of the change in input offset voltage to the peak-to-peak input voltage range.

Comparator Input Current: The average current flowing from the R/C pin during the timing cycle.

C_t: Timing capacitor connected between the R/C terminal and the ground terminal.

Emitter Saturation Voltage: The voltage across the output transistor when the collector is tied to V^+, the transistor is in the "ON" state, and the specified output current is flowing from the emitter terminal.

Input Bias Current: The average of the two input currents.

Input Offset Current: The difference in the current into the two input terminals when the supply (output) current is 4.0 mA.

Input Offset Voltage: The voltage which must be applied between the input terminals through equal resistances to obtain 4.0 mA of supply (output) current.

Input Resistance: The ratio of the change in input voltage to the change in input current at either input with the other input connected to 1.0 Vdc.

Input Voltage Range: The range of voltages on the input terminals for which the device operates within specifications.

Linearity: The deviation in output voltage from a straight line output over a specified temperature excursion.

Long Term Stability: The change of a particular parameter when operated at maximum temperature for 1000 hours.

Maximum Power Dissipation: The maximum total device dissipation for which the timer will operate within specifications.

Open Loop Output Resistance: The ratio of a specified supply (output) voltage change to the resulting change in supply (output) current at the specified current level.

Open Loop Transconductance: The ratio of the supply (output) current SPAN to the input voltage required to produce that SPAN.

Open Loop Supply Current: The supply current required with the signal amplifier A2 biased off (inverting input positive, non-inverting input negative) and no load on the V_{REF} terminal.

This represents a measure of the minimum low end signal current.

Output Leakage Current: The maximum current flowing into the collector of the output transistor when the transistor is in the "OFF" state.

Output Sink Current: The current available to flow into a load from a positive supply over a specified output voltage range.

Output Source Current: The current available to flow into a load from the output to V^-, over a specified output voltage range.

Output Voltage: The voltage referred to the V^+ terminal from the output terminal with the input and output connected. (This voltage is the temperature output of the LM3911 and so includes errors in the sensor section and op amp section.)

Power Supply Rejection Ratio: The ratio of the change in input offset voltage to the change in supply (output) voltage producing it.

Reference Voltage Line Regulation: The ratio of the change in V_{REF} to the peak-to-peak change in supply (output) voltage producing it.

Reference Voltage Load Regulation: The change in V_{REF} for a stipulated change in I_{REF}.

Reset Resistor: The equivalent resistor which may be used to calculate the discharge time of the timing capacitor, $t_{DISCHARGE} = (5)\ (C_t)\ (R_{RESET})$.

Reverse Breakdown Voltage: The voltage appearing between the V^+ and V^- terminals at a specified current.

R_t: Timing resistor connected between V_{REF} and the R/C terminal.

Temperature Stability: The percentage in output voltage for a thermal variation from room temperature to either temperature extreme.

Timing Ratio: The ratio of the firing voltage at the R/C pin to the reference voltage.

Trigger Current: The current flowing into or out of the trigger terminal at the specified trigger voltage.

Trigger Voltage: The voltage required at the trigger terminal to initiate a timing cycle, referenced to the ground pin.

National Semiconductor

LM122/LM222/LM322, LM2905/LM3905 Precision Timers

General Description

The LM122 series are precision timers that offer great versatility with high accuracy. They operate with unregulated supplies from 4.5V to 40V while maintaining constant timing periods from microseconds to hours. Internal logic and regulator circuits complement the basic timing function enabling the LM122 series to operate in many different applications with a minimum of external components.

The output of the timer is a floating transistor with built in current limiting. It can drive either ground referred or supply referred loads up to 40V and 50 mA. The floating nature of this output makes it ideal for interfacing, lamp or relay driving, and signal conditioning where an open collector or emitter is required. A "logic reverse" circuit can be programmed by the user to make the output transistor either "on" or "off" during the timing period.

The **trigger** input to the LM122 series has a threshold of 1.6V independent of supply voltage, but it is fully protected against inputs as high as ±40V – even when using a 5V supply. The circuitry reacts only to the rising edge of the trigger signal, and is immune to any trigger voltage during the timing periods.

An internal 3.15V regulator is included in the timer to reject supply voltage changes and to provide the user with a convenient reference for applications other than a basic timer. External loads up to 5 mA can be driven by the regulator. An internal 2V divider between the reference and ground sets the timing period to 1 RC. The timing period can be voltage controlled by driving this divider with an external source through the V_{ADJ} pin. Timing ratios of 50:1 can be easily achieved.

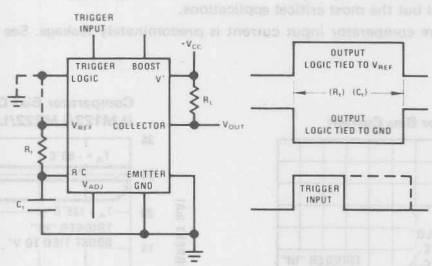
The comparator used in the LM122 utilizes high gain PNP input transistors to achieve 300 pA typical input bias current over a common mode range of 0V to 3V. A **boost** terminal allows the user to increase comparator operating current for timing periods less than 1 ms. This lets the timer operate over a 3μs to multi-hour timing range with excellent repeatability.

The LM122 operates over a temperature range of −55°C to +125°C. An electrically identical LM222 is specified from −25°C to +85°C, and the LM322 is specified from 0°C to +70°C. The LM2905/LM3905 are identical to the LM122 series except that the **boost** and V_{ADJ} pin options are not available, limiting minimum timing period to 1 ms.

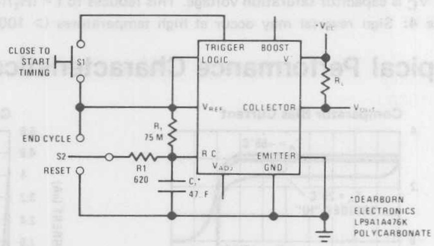
Features

- Immune to changes in trigger voltage during timing interval
- Timing periods from microseconds to hours
- Internal logic reversal
- Immune to power supply ripple during the timing interval
- Operates from 4.5V to 40V supplies
- Input protected to ±40V
- Floating transistor output with internal current limiting
- Internal regulated reference
- Timing period can be voltage controlled
- TTL compatible input and output

Typical Applications



Basic Timer-Collector Output and Timing Chart



One Hour Timer with Reset and Manual Cycle End

LM122/LM222/LM322/LM2905/LM3905

9

Absolute Maximum Ratings

Power Dissipation	500 mW
V^+ Voltage	40V
Collector Output Voltage	40V
V_{REF} Current	5 mA
Trigger Voltage	±40V
V_{ADJ} Voltage (Forced)	5V
Logic Reverse Voltage	5.5V
Output Short Circuit Duration (Note 1)	
Lead Temperature (Soldering, 10 sec)	300°C

Operating Temperature Range	
LM122	$-55°C \leq T_A \leq +125°C$
LM222	$-25°C \leq T_A \leq +85°C$
LM322	$0°C \leq T_A \leq +70°C$
LM2905	$-40°C \leq T_A \leq +85°C$
LM3905	$0°C \leq T_A \leq +70°C$

Electrical Characteristics (Note 2)

PARAMETER	CONDITIONS	LM122/LM222 MIN	LM122/LM222 TYP	LM122/LM222 MAX	LM322 MIN	LM322 TYP	LM322 MAX	LM2905/LM3905 MIN	LM2905/LM3905 TYP	LM2905/LM3905 MAX	UNITS
Timing Ratio	$T_A = 25°C$, $4.5V \leq V^+ \leq 40V$	0.626	0.632	0.638	0.620	0.632	0.644	0.620	0.632	0.644	
	Boost Tied to V^+, (Note 3)	0.620	0.632	0.644	0.620	0.632	0.644				
Comparator Input Current	$T_A = 25°C$, $4.5V \leq V^+ \leq 40V$		0.3	1.0		0.3	1.5		0.5	1.5	nA
	Boost Tied to V^+		30	100		30	100				nA
Trigger Voltage	$T_A = 25°C$, $4.5V \leq V^+ \leq 40V$	1.2	1.6	2	1.2	1.6	2	1.2	1.6	2	V
Trigger Current	$T_A = 25°C$, $V_{TRIG} = 2V$		25			25			25		μA
Supply Current	$T_A \geq 25°C$, $4.5V \leq V^+ \leq 40V$		2.5	4		2.5	4.5		2.5	4.5	mA
Timing Ratio	$4.5V \leq V^+ \leq 40V$	0.62		0.644	0.61		0.654	0.61		0.654	
	Boost Tied to V^+	0.62		0.644	0.61		0.654				
Comparator Input Current	$4.5V \leq V^+ \leq 40V$	−5		5	−2		2	−2.5		2.5	nA
	Boost Tied to V^+, (Note 4)			100			150				nA
Trigger Voltage	$4.5V \leq V^+ \leq 40V$	0.8		2.5	0.8		2.5	0.8		2.5	V
Trigger Current	$V_{TRIG} = 2.5V$			200			200			200	μA
Output Leakage Current	$V_{CE} = 40V$			1			5			5	μA
Capacitor Saturation Voltage	$R_t \geq 1\ M\Omega$		2.5			2.5			2.5		mV
	$R_t = 10\ k\Omega$		25			25			25		mV
Reset Resistance			150			150			150		Ω
Reference Voltage	$T_A = 25°C$	3	3.15	3.3	3	3.15	3.3	3	3.15	3.3	V
Reference Regulation	$0 \leq I_{OUT} \leq 3$ mA		20	50		20	50		20	50	mV
	$4.5V \leq V^+ \leq 40V$		6	25		6	25		6	25	mV
Collector Saturation Voltage	$I_L = 8$ mA		0.25	0.4		0.25	0.4		0.25	0.4	V
	$I_L = 50$ mA		0.7	1.4		0.7	1.4		0.7	1.4	V
Emitter Saturation Voltage	$T_A = 25°C$, $I_L = 3$ mA		1.8	2.2		1.8	2.2		1.8	2.2	V
	$T_A = 25°C$, $I_L = 50$ mA		2.1	3		2.1	3		2.1	3	V
Average Temperature Coefficient of Timing Ratio			0.003			0.003			0.003		%/°C
Minimum Trigger Width	$V_{TRIG} = 3V$		0.25			0.25			0.25		μs

Note 1: Continuous output shorts are not allowed. Short circuit duration at ambient temperatures up to 40°C may be calculated from $t = 120/V_{CE}$ seconds, where V_{CE} is the collector to emitter voltage across the output transistor during the short.

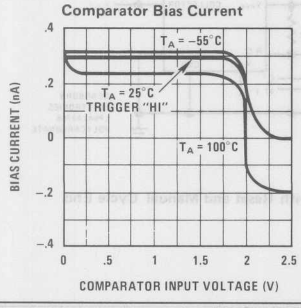
Note 2: These specifications apply for $T_{AMIN} \leq T_A \leq T_{AMAX}$ unless otherwise noted.

Note 3: Output pulse width can be calculated from the following equation: $t = (R_t)(C_t)[1 - 2(0.632 - r) - V_C/V_{REF})$ where r is timing ratio and V_C is capacitor saturation voltage. This reduces to $t = (R_t)(C_t)$ for all but the most critical applications.

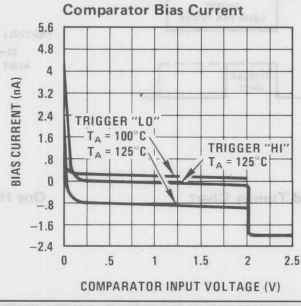
Note 4: Sign reversal may occur at high temperatures (> 100°C) where comparator input current is predominately leakage. See typical curves.

Typical Performance Characteristics

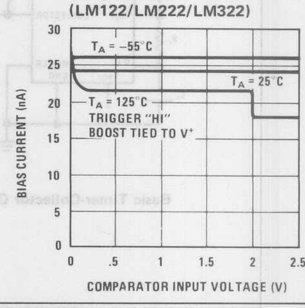
Comparator Bias Current



Comparator Bias Current

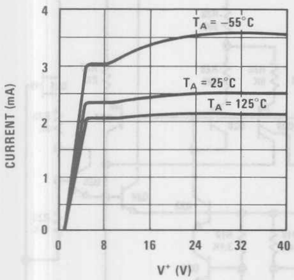


Comparator Bias Current (LM122/LM222/LM322)

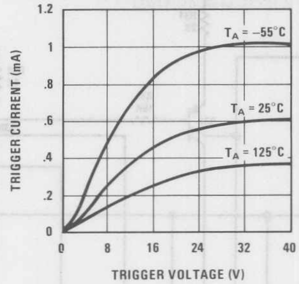


Typical Performance Characteristics (Continued)

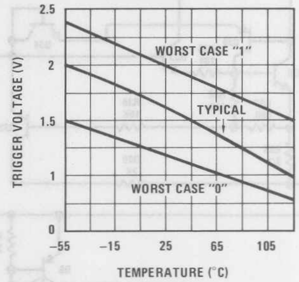
Supply Current



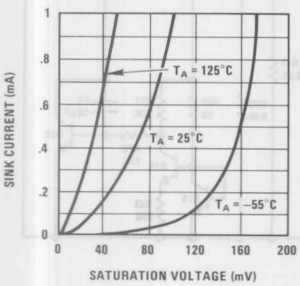
Trigger Input Characteristics



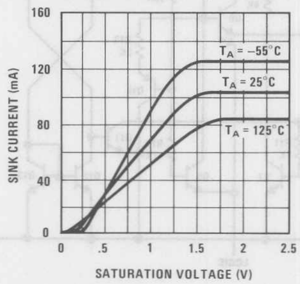
Trigger Threshold



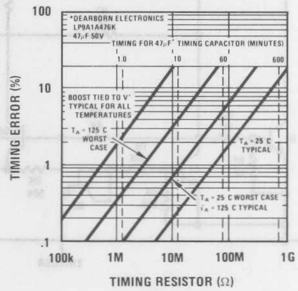
Output Transistor Saturation Characteristics at Low Currents



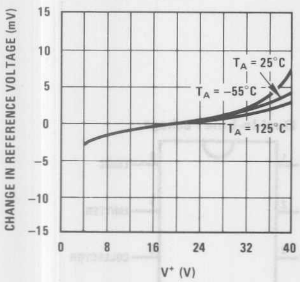
Collector Output Saturation Characteristics at High Current



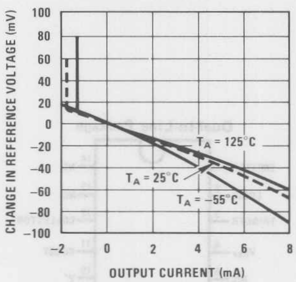
Timing Error Due to Comparator Bias Current



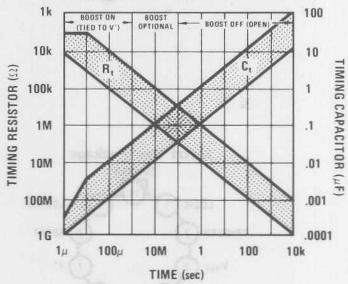
Reference Regulation



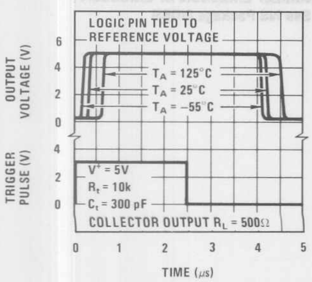
Reference Regulation



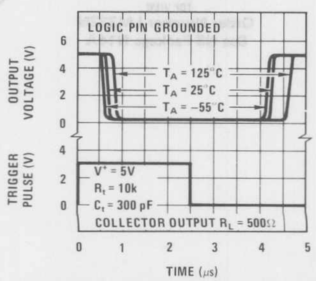
Suggested Timing Components



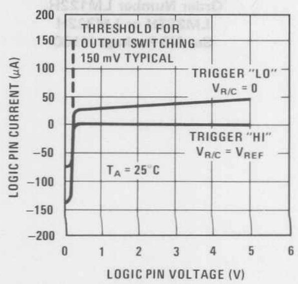
Short Output Pulse (LM122/LM222/LM322)

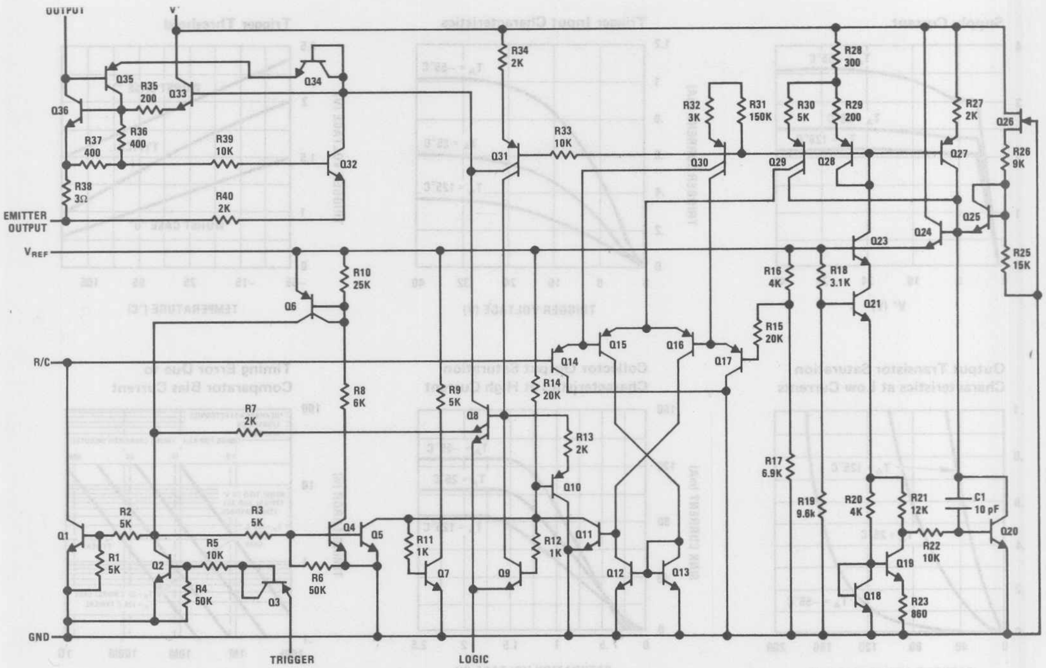


Short Output Pulse (LM122/LM222/LM322)



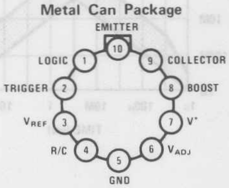
Logic Pin Characteristics





Connection Diagrams

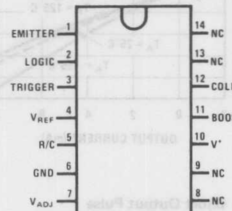
Metal Can Package



TOP VIEW

Order Number LM122H, LM222H or LM322H
See NS Package H10C

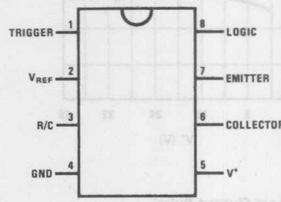
Dual-In-Line Package



TOP VIEW

Order Number LM322N
See NS Package N14A

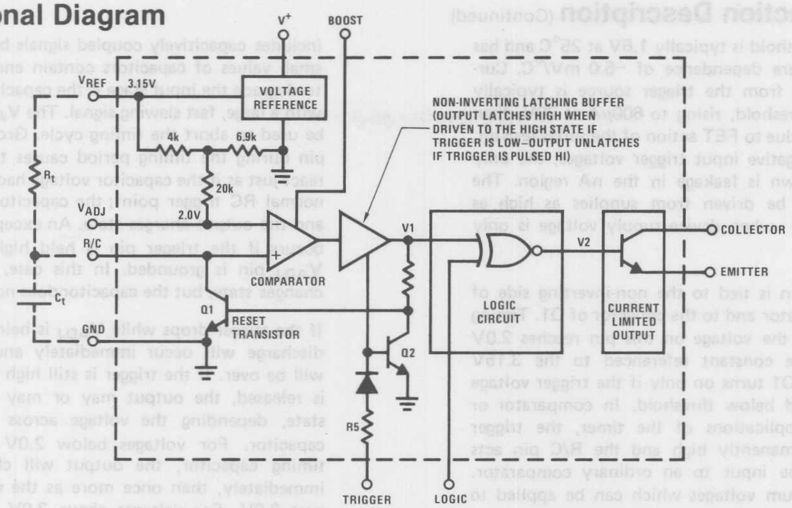
Dual-In-Line Package



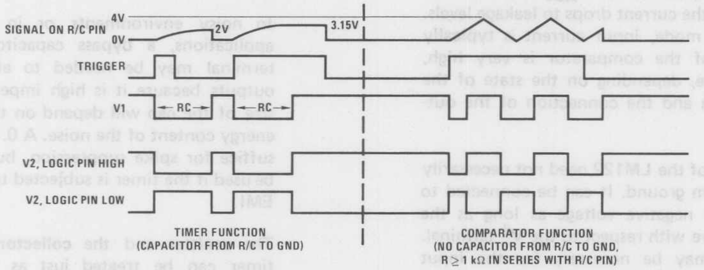
TOP VIEW

Order Number LM2905N or LM3905N
See NS Package N08B

Functional Diagram



Timing Diagram



Pin Function Description

One of the main features of the LM122 is its great versatility. Since this device is unique, a description of the functions and limitations of each pin is in order. This will make it much easier to follow the discussion of the various applications presented in this note.

V^+ is the positive supply terminal of the LM122. When using a single supply, this terminal may be driven by any voltage between 4.5V and 40V. The effect of supply variations on timing period is less than 0.005%/V, so supplies with high ripple content may be used without causing pulse width changes. Supply bypassing V^+ is not generally needed but may be necessary when driving highly reactive loads. Quiescent current drawn from the V^+ terminal is typically 2.5 mA, independent of the supply voltage. Of course, additional current will be drawn if the reference is externally loaded.

The V_{REF} pin is the output of a 3.15V series regulator referenced to the ground pin. Up to 5.0 mA can be drawn from this pin for driving external networks. In most applications the timing resistor is tied to V_{REF}, but it need not be in situations where a more linear charging current is required. The regulated voltage is very useful in applications where the LM122 is not used as a timer; such as switching regulators, variable reference comparators, and temperature controllers. Typical temperature drift of the reference is less than 0.01%/°C.

The **trigger** terminal is used to start a timing cycle (see functional diagram). Initially, Q1 is saturated, C_t is discharged and the latching buffer output (V1) is latched high. A trigger pulse unlatches the buffer, V1 goes low and turns Q1 off. The timing capacitor C_t connected from R/C to GND will begin to charge. When the voltage at the R/C terminal reaches the 2.0V threshold of the comparator, the comparator toggles, latching the buffer output (V1) in the high state. This turns on Q1, discharges the capacitor C_t and the cycle is ready to begin again.

If the **trigger** is held high as the timing period ends, the comparator will toggle and V1 will go high exactly as before. However, V1 will not be latched and the capacitor will not discharge until the trigger again goes low. When the trigger goes low, V1 remains high but is now latched.

Pin Function Description (Continued)

Trigger threshold is typically 1.6V at 25°C and has a temperature dependence of −5.0 mV/°C. Current drawn from the **trigger** source is typically 20μA at threshold, rising to 600μA at 30V, then leveling off due to FET action of the series resistor, R5. For negative input trigger voltages, the only current drawn is leakage in the nA region. The **trigger** can be driven from supplies as high as ±40V, even when device supply voltage is only 5V.

The **R/C** pin is tied to the non-inverting side of the comparator and to the collector of Q1. Timing ends when the voltage on this pin reaches 2.0V (1 RC time constant referenced to the 3.15V regulator). Q1 turns on only if the trigger voltage has dropped below threshold. In comparator or regulator applications of the timer, the trigger is held permanently high and the R/C pin acts just like the input to an ordinary comparator. The maximum voltages which can be applied to this pin are +5.5V and −0.7V. Current from the **R/C** pin is typically 300 pA when the voltage is negative with respect to the V_{ADJ} terminal. For higher voltages, the current drops to leakage levels. In the boosted mode, input current is typically 30 nA. Gain of the comparator is very high, 200,000 or more, depending on the state of the logic reverse pin and the connection of the output transistor.

The **ground** pin of the LM122 need not necessarily be tied to system ground. It can be connected to any positive or negative voltage as long as the supply is negative with respect to the V^+ terminal. Level shifting may be necessary for the input **trigger** if the **trigger** voltage is referred to system ground. This can be done by capacitive coupling or by actual resistive or active level shifting. One point must be kept in mind; the emitter output must not be held above the **ground** terminal with a low source impedance. This could occur, for instance, if the emitter were grounded when the **ground** pin of the LM122 was tied to a negative supply.

The terminal labeled V_{ADJ} is tied to one side of the comparator and to a voltage divider between V_{REF} and **ground**. The divider voltage is set at 63.2% of V_{REF} with respect to ground—exactly one RC time constant. The impedance of the divider is increased to about 30k with a series resistor to present a minimum load on external signals tied to V_{ADJ}. This resistor is a pinched type with a typical variation in nominal value of −50%, +100%. and a TC of 0.7%/°C. For this reason, external signals (typically a pot between V_{REF} and **ground**) connected to V_{ADJ} should have a source resistance as low as possible. For small changes in V_{ADJ}, up to several kΩ is all right, but for large variations, 250Ω or less should be maintained. This can be accomplished with a 1k pot, since the maximum impedance from the wiper is 250Ω. If a voltage is forced on V_{ADJ} from a hard source, voltage should be limited to −0.5, and +5.0V, or current limited to ±1.0 mA. This includes capacitively coupled signals because even small values of capacitors contain enough energy to degrade the input stage if the capacitor is driven with a large, fast slewing signal. The V_{ADJ} pin may be used to abort the timing cycle. Grounding this pin during the timing period causes the timer to react just as if the capacitor voltage had reached its normal RC trigger point; the capacitor discharges and the output charges state. An exception to this occurs if the trigger pin is held high when the V_{ADJ}, pin is grounded. In this case, the output changes state, but the capacitor does not discharge.

If the trigger drops while V_{ADJ} is being held low, discharge will occur immediately and the cycle will be over. If the trigger is still high when V_{ADJ} is released, the output may or may not change state, depending the voltage across the timing capacitor. For voltages below 2.0V across the timing capacitor, the output will change state immediately, then once more as the voltage rises past 2.0V. For voltages above 2.0V, no change will occur in the output. This pin is not available on the LM2905/LM3905.

In noisy environments or in comparator-type applications, a bypass capacitor on the V_{ADJ} terminal may be needed to eliminate spurious outputs because it is high impedance point. The size of the cap will depend on the frequency and energy content of the noise. A 0.1μF will generally suffice for spike suppression, but several μF may be used if the timer is subjected to high level 60 Hz EMI.

The **emitter** and the **collector** outputs of the timer can be treated just as if they were an ordinary transistor with 40V minimum collector-emitter breakdown voltage. Normally, the **emitter** is tied to the **ground** pin and the signal is taken from the **collector**, or the **collector** is tied to V^+ and the signal is taken from the **emitter**. Variations on these basic connections are possible. The **collector** can be tied to any positive voltage up to 40V when the signal is taken from the **emitter**. However, the **emitter** will not be pulled higher than the supply voltage on the V^+ pin. Connecting the **collector** to a voltage less than the V^+ voltage is allowed The **emitter** should not be connected to a low impedance load other than that to which the ground pin is tied. The transistor has built-in current limiting with a typical knee current of 120 mA. Temporary short circuits are allowed; even with **collector-emitter** voltages up to 40V. The power x time product, however, must not exceed 15 watt-seconds for power levels above the maximum rating of the package. A short to 30V, for instance, can not be held for more than 4 seconds. These levels are based on 40°C maximum initial chip temperature. When driving inductive loads, always use a clamp diode to protect the transistor from inductive kick-back.

A **boost** pin is provided on the LM122 to increase the speed of the internal comparator. The comparator is normally operated at low current levels for lowest possible input current.

Pin Function Description (Continued)

For timing periods less than 1 ms, where low input current is not needed, comparator operating current can be increased several orders of magnitude. Shorting the boost terminal to V^+ increases the emitter current of the vertical PNP drivers in the differential stage from 25 nA to 5μA. This pin is not available on the LM2905/LM3905.

With the timer in the unboosted state, timing periods are accurate down to about 1 ms. In the boosted mode, loss of accuracy due to comparator speed is only about 800 ns, so timing periods of several microseconds can be used. The 800 ns error is relatively insensitive to temperature, so temperature coefficient of pulse width is still good.

The **Logic** pin is used to reverse the signal appearing at the output transistor. An open or "high" condition on the **logic** pin programs the output transistor to be "off" during the timing period and "on" all other times. Grounding the **logic** pin reverses the sequence to make the transistor "on" during the timing period. Threshold for the **logic** pin is typically 100 mV with 150μA flowing out of the terminal. If an active drive to the **logic** pin is desired, a saturated transistor drive is recommended, either with a discrete transistor or the open collector output of integrated logic. A maximum V_{SAT} of 25 mV at 200μA is required. Minimum and maximum voltages that may appear on the **logic** pin are 0 and +5.0, respectively.

Typical Applications (Continued)

Basic Timers

Figure 1 is a basic timer using the collector output. R_t and C_t set the time interval with R_L as the load. During the timing interval the output may be either high or low depending on the connection of the logic pin. Timing waveforms are shown in the sketch along side *Figure 1*. Note that the trigger pulse may be either shorter or longer than the output pulse width.

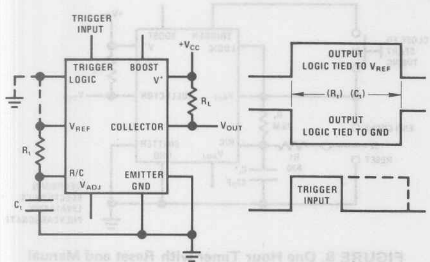


FIGURE 1. Basic Timer-Collector Output and Timing Chart

Figure 2 is again a basic timer, but with the output taken from the emitter of the output transistor. As with the collector output, either a high or low condition may be obtained during the timing period.

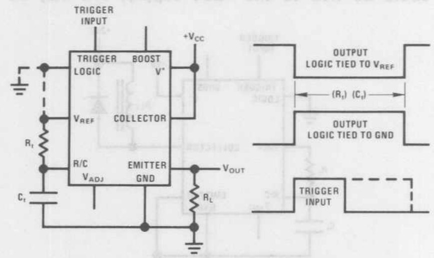


FIGURE 2. Basic Timer-Emitter Output and Timing Chart

Simulating a Thermal Delay Relay

Figure 3 is an application where the LM122 is used to simulate a thermal delay relay which prevents power from being applied to other circuitry until the supply has been on for some time. The relay remains de-energized for R_t C_t seconds after V_{CC} is applied, then closes and stays energized until V_{CC} is turned off. *Figure 4* is a similar circuit except that the relay is energized as soon as V_{CC} is applied. R_t C_t seconds later, the relay is de-energized and stays off until the V_{CC} supply is recycled.

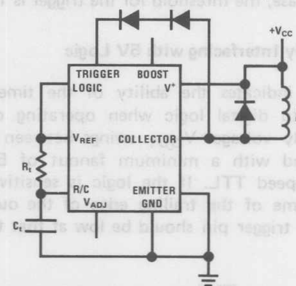


FIGURE 3. Time Out on Power Up (Relay Energized R_tC_t Seconds After V_{CC} is Applied)

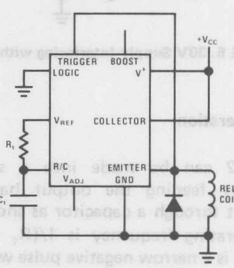


FIGURE 4. Time Out on Power Up (Relay Energized *Until* R_tC_t Seconds After V_{CC} is Applied)

+5V Supply Driving 28V Relay

Figure 5 shows the timer interfacing 5V logic to a high voltage relay. Although the V^+ terminal could be tied to the +28V supply, this may be

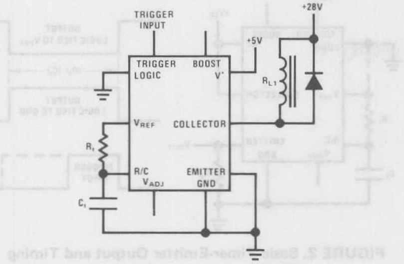


FIGURE 5. 5V Logic Supply Driving 28V Relay

an unnecessary waste of power in the IC or require extra wiring if the LM122 is on a logic card. In either case, the threshold for the trigger is 1.6V.

30V Supply Interfacing with 5V Logic

Figure 6 indicates the ability of the timer to interface to digital logic when operating off a high supply voltage. V_{OUT} swings between +5V and ground with a minimum fanout of 5 for medium speed TTL. If the logic is sensitive to rise/fall time of the trailing edge of the output pulse, the trigger pin should be low at that time.

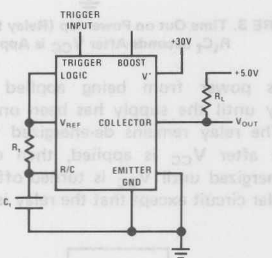


FIGURE 6. 30V Supply Interfacing with 5V Logic

Astable Operation

The LM122 can be made into a self-starting oscillator by feeding the output back to the trigger input through a capacitor as shown in *Figure 7*. Operating frequency is $1/(R_t + R_1)(C_t)$. The output is a narrow negative pulse whose width is approximately $2R_2\ C_f$. For optimum frequency stability, C_f should be as small as possible. The minimum value is determined by the time required to discharge C_t through the internal discharge transistor. A conservative value for C_f can be chosen from the graph included with *Figure 20*. For frequencies below 1 kHz, the frequency error introduced by C_f is a few tenths of one percent or less for $R_t \geq 500k$.

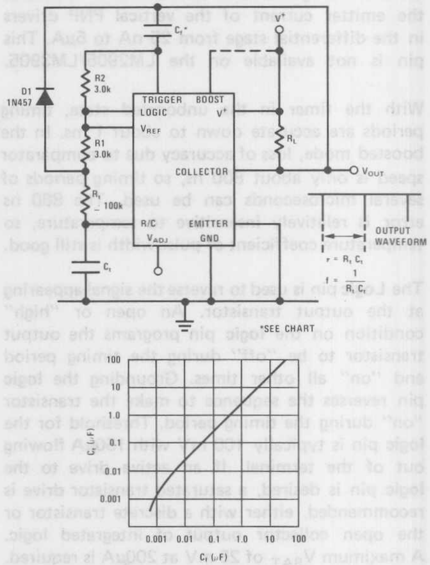


FIGURE 7. Oscillator

One Hour Timer with Reset and Manual Cycle End

Figure 8 shows the LM122 connected as a one hour timer with manual controls for start, reset, and cycle end. S1 starts timing, but has no effect after timing has started. S2 is a center off switch which can either end the cycle prematurely with the appropriate change in output state and discharging of C_t, or cause C_t to be reset to 0V without a change in output. In the latter case, a new timing period starts as soon as S2 is released.

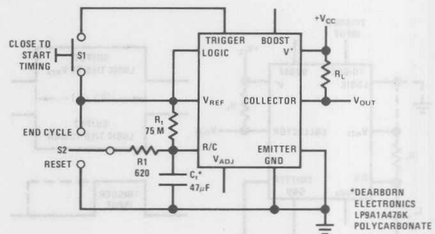


FIGURE 8. One Hour Timer with Reset and Manual Cycle End

The average charging current through R_t is about 30 nA, so some attention must be paid to parts layout to prevent stray leakage paths. The suggested timing capacitor has a typical self time constant of 300 hours and a guaranteed minimum of 25 hours at +25°C. Other capacitor types may be used if sufficient data is available on their leakage characteristics.

Typical Applications (Continued)

Two Terminal Time Delay Switch

The LM122 can be used as a two terminal time delay switch if an "on" voltage drop of 2V to 3V can be tolerated. In *Figure 9*, the timer is used to drive a relay "on" $R_t \cdot C_t$ seconds after application of power. "off" current of the switch is 4 mA maximum, and "on" current can be as high as 50 mA.

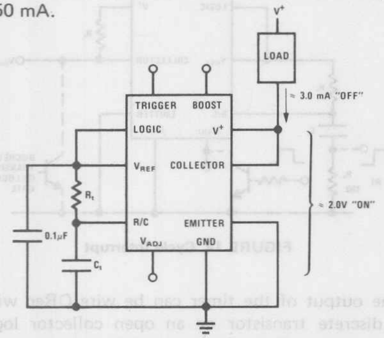


FIGURE 9. 2-Terminal Time Delay Switch

Zero Power Dissipation Between Timing Intervals

In some applications it is desirable to reduce supply current drain to zero between timing cycles. In *Figure 10* This is accomplished by using an external PNP as a latch to drive the V^+ pin of the timer.

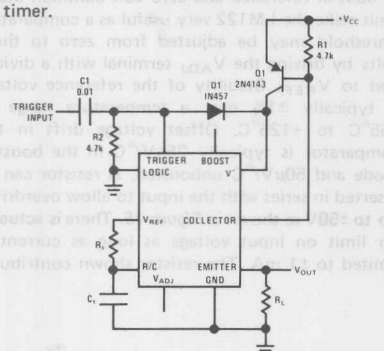


FIGURE 10. Zero Power Dissipation Between Timing Intervals

Between timing periods Q1 is off and no supply current is drawn. When a trigger pulse of 5V minimum amplitude is received, the LM122 output transistor and Q1 latch for the duration of the timing period. D1 prevents the step on the V^+ pin from coupling back into the trigger pin. If the trigger input is a short pulse, C1 and R2 may be eliminated. R_L must have a minimum value of $(V_{CC})/(2.5\ mA)$.

Frequency to Voltage Converter

An accurate frequency to voltage converter can be made with the LM122 by averaging output pulses with a simple one pole filter as shown in *Figure 11*. Pulse width is adjusted with R2 to provide initial calibration at 10 kHz. The collector of the output transistor is tied to V_{REF}, giving constant amplitude pulses equal to V_{REF} at the emitter output. R4 and C1 filter the pulses to give a dc output equal to, $(R_t)(C_t)(V_{REF})(f)$. Linearity is about 0.2% for a 0V to 1V output. If better linearity is desired R5 can be tied to the summing node of an op amp which has the filter in the feedback path. If a low output impedance is desired, a unity gain buffer such as the LM110 can be tied to the output. An analog meter can be driven directly by placing it in series with R5 to ground. A series RC network across the meter to provide damping will improve response at very low frequencies.

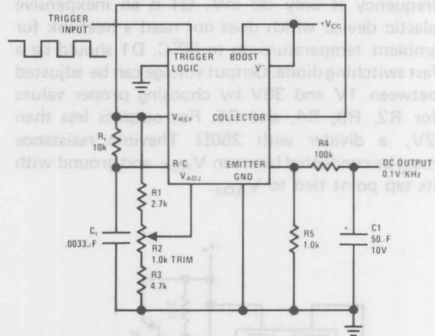


FIGURE 11. Frequency to Voltage Converter.(Tachometer) Output Independent of Supply Voltage

Pulse Width Detector

By driving the logic terminal of the LM122 simultaneous to the trigger input, a simple, accurate pulse width detector can be made *(Figure 12).*

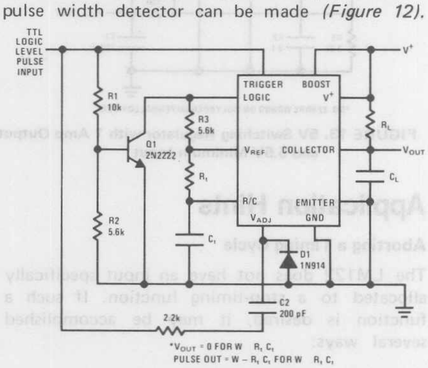


FIGURE 12. Pulse Width Detector

In this application the logic terminal is normally held high by R3. When a trigger pulse is received, Q1 is turned on, driving the logic terminal to ground. The result of triggering the timer and reversing the logic at the same time is that the output does not change from its initial low condition. The only time the output will change states is when the trigger input stays high longer than one time period set by R_t and C_t. The output pulse width is equal to the input trigger width minus $R_t \cdot C_t$. C2 insures no output pulse for short (< RC) trigger pulses by prematurely resetting the timing capacitor when the trigger pulse drops. C_L filters the narrow spikes which would occur at the output due to propagation delays during switching.

Typical Applications (Continued)

5V Switching Regulator

Figure 13 is an application where the LM122 does not use its timing function. A switching regulator is made using the internal reference and comparator to drive a PNP transistor switch. Features of this circuit include a 5.5V minimum input voltage at 1A output current, low part count, and good efficiency (> 75%) for input voltages to 10V. Line and load regulation are less than 0.5% and output ripple at the switching frequency is only 30 mV. Q1 is an inexpensive plastic device which does not need a heatsink for ambient temperature up to 50°C. D1 should be a fast switching diode. Output voltage can be adjusted between 1V and 30V by choosing proper values for R2, R3, R4, and R5. For outputs less than 2V, a divider with 250Ω Thevinin resistance must be connected between V_{REF} and ground with its tap point tied to V_{ADJ}.

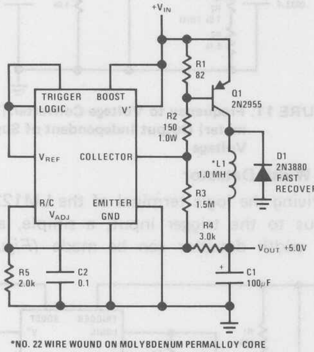


FIGURE 13. 5V Switching Regulator with 1 Amp Output and 5.5V Minimum Input

Application Hints

Aborting a Timing Cycle

The LM122 does not have an input specifically allocated to a stop-timing function. If such a function is desired, it may be accomplished several ways:

- Ground V_{ADJ}
- Raise R/C more positive than V_{ADJ}
- Wire "OR" the output

Grounding V_{ADJ} will end the timing cycle just as if the timing capacitor had reached its normal discharge point. A new timing cycle can be started by the trigger terminal as soon as the ground is released. A switching transistor is best for driving V_{ADJ} to as near ground as possible. Worst case sink current is about 300µA.

A timing cycle may also be ended by a positive pulse to a resistor ($R \le R_t/100$) in series with the timing capacitor. The pulse amplitude must be at least equal to V_{ADJ} (2.0V), but should not exceed 5.0V. When the timing capacitor discharges, a negative spike of up to 2.0V will occur across the resistor, so some caution must be used if the drive pulse is used for other circuitry.

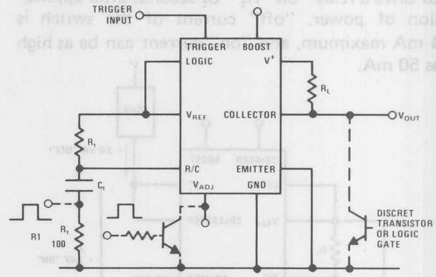


FIGURE 14. Cycle Interrupt

The output of the timer can be wire ORed with a discrete transistor or an open collector logic gate output. This allows overriding of the timer output, but does not cause the timer to be reset until its normal cycle time has elapsed.

Using the LM122 as a Comparator

A built-in reference and zero volt common mode limit make the LM122 very useful as a comparator. Threshold may be adjusted from zero to three volts by driving the V_{ADJ} terminal with a divider tied to V_{REF}. Stability of the reference voltage is typically ±1% over a temperature range of −55°C to +125°C. Offset voltage drift in the comparator is typically 25µV/°C in the boosted mode and 50µV/°C unboosted. A resistor can be inserted in series with the input to allow overdrives up to ±50V as shown in *Figure 15*. There is actually no limit on input voltage as long as current is limited to ±1 mA. The resistor shown contributes

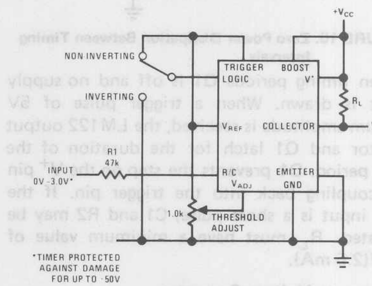


FIGURE 15. Comparator with 0V to 3V Threshold

a worst case of 5 mV to initial offset. In the unboosted mode, the error drops to 0.25 mV maximum. The capability of operating off a single 5V supply with internal reference should make this comparator very useful.

Application Hints (Continued)

Eliminating Timing Cycle Upon Initial Application of Power

The LM122 will normally start a timing cycle (with no trigger input) when V^+ is first turned on. If this characteristic is undesirable, it can be defeated by tying the timing capacitor to V_{REF} instead of ground as shown in *Figure 16.* This connection does not affect operation of the timer in any other way. If an electrolytic timing capacitor is used, be sure the negative end is tied to the R/C pin and the positive end to V_{REF}. A 1.0 kΩ resistor should be included in series with the timing capacitor to limit the surge current load on V_{REF} when the capacitor is discharged.

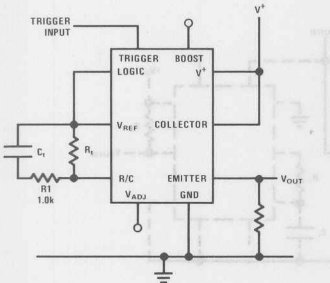
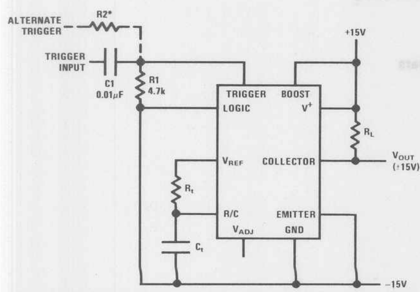


FIGURE 16. Eliminating Initial Timing Cycle

Using Dual Supplies

The LM122 can be operated off dual supplies as shown in *Figure 17.* The only limitation is that the emitter terminal cannot be tied to ground, it must either drive a load referred to V^- or be actually tied to V^- as shown. Although capacitive coupling is shown for the trigger input (to allow 5V triggering), a resistor can be substituted for C1. R2 must be chosen to give proper level shifting between the trigger signal and the trigger pin of the timer. Worst case "lo" on the trigger pin (with respect to V^-) is 0.8V, and worst case "high" is 2.5V. R2 may be calculated from the divider equation with R1 to give these levels.



*SELECT FOR PROPER LEVEL SHIFT
EMITTER TERMINAL OR EMITTER LOAD MUST BE TIED TO GND PIN OF TIMER.

FIGURE 17. Operating Off Dual Supplies

Linearizing the Charging Sweep

In some applications (such as a linear pulse width modulator) it may be desirable to have the timing capacitor charge from a constant current source. A simple way to accomplish this is shown in *Figure 18.*

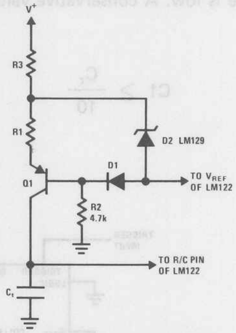


FIGURE 18. Temperature Compensated Linear Charging Sweep

Q1 converts the current through R1 to a current source independent of the voltage across C_t. R2, R3, D1, and D2 are added to make the current through R1 independent of supply variations and temperature changes. (D2 is a low TC type) D2 and R3 can be omitted if the V^+ supply is stable and D1 and R2 can be omitted also if temperature stability if not critical. With D1, D2, R2 and R3 omitted, the current through R1 will change about 0.015%/°C with a 15V supply and 0.1%/°C with a 5.0V supply.

Triggering with Negative Edge

Although the LM122 is triggered by a positive going trigger signal, a differentiator tied to a normally "high" trigger will result in negative edge triggering. In *Figure 19,* R1 serves the dual purpose of holding the trigger pin normally high and differentiating the input trigger pulse coupled through C1. The timing diagram included with Figure 21 shows that triggering actually occurs a short time after the negative going trigger, while positive going triggers have no effect. The delay time between a negative trigger signal and actual

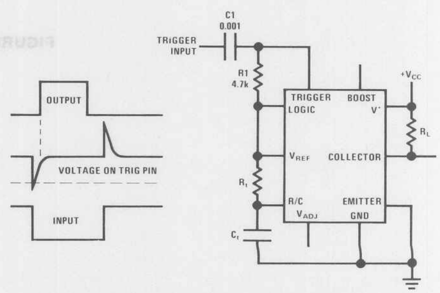


FIGURE 19. Timer Triggered by Negative Edge of Input Pulse

or about 2.5 to 7.5μs with the values shown. This time will have to be increased for C_t larger than 0.01μF because C_t is charged to V_{REF} whenever the trigger pin is kept high and must reset itself during the short time that the trigger pin voltage is low. A conservative value for C1 is:

$$C1 \geq \frac{C_t}{10}$$

The LM122 can be connected as a chain of timers quite easily with no interface required. In *Figure 20A and 20B*, two possible connections are shown. In both cases, the output of the timer is low during the timing period so that the positive going signal at the end of timing period can trigger the next timer. There is no limitation on the timing period of one timer with respect to any other timer before or after it, because the trigger input to any timer can be high or low when that timer ends its timing period.

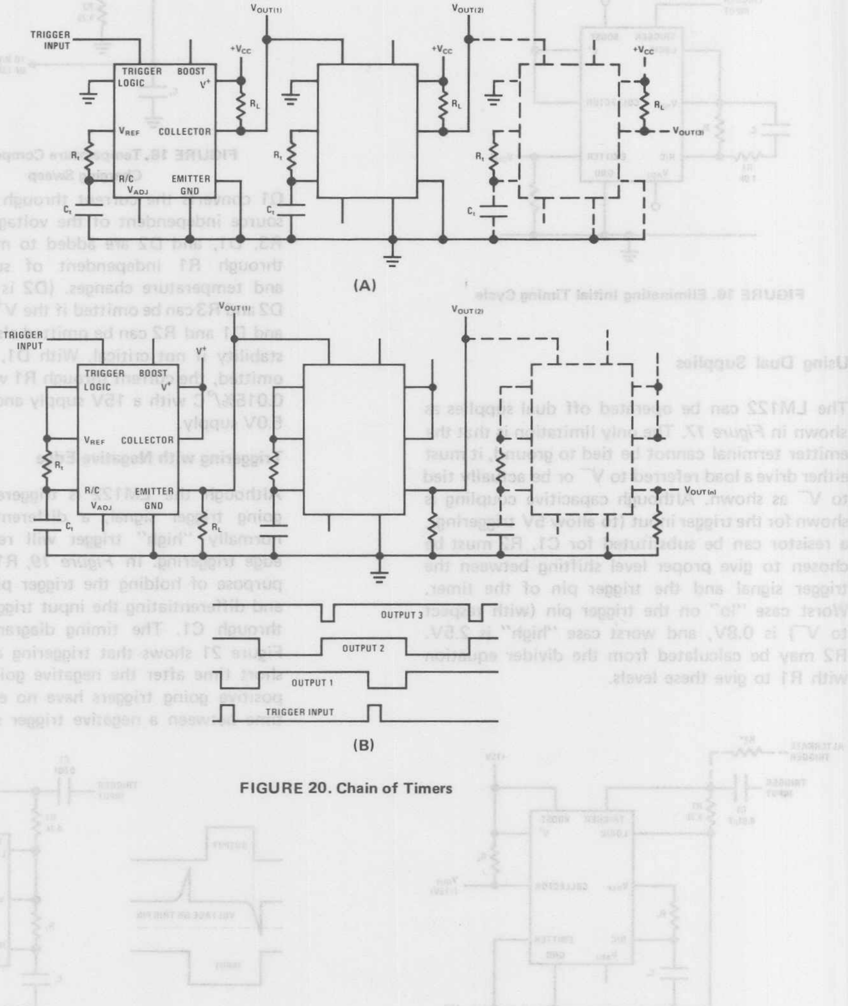


FIGURE 20. Chain of Timers

National Semiconductor

LM134/LM234/LM334 3-Terminal Adjustable Current Sources

General Description

The LM134/LM234/LM334 are 3-terminal adjustable current sources featuring 10,000:1 range in operating current, excellent current regulation and a wide dynamic voltage range of 1V to 40V. Current is established with one external resistor and no other parts are required. Initial current accuracy is ±3%. The LM134/LM234/LM334 are true floating current sources with no separate power supply connections. In addition, reverse applied voltages of up to 20V will draw only a few microamperes of current, allowing the devices to act as both a rectifier and current source in AC applications.

The sense voltage used to establish operating current in the LM134 is 64 mV at 25°C and is directly proportional to absolute temperature (°K). The simplest one external resistor connection, then, generates a current with ≈+0.33%/°C temperature dependence. Zero drift operation can be obtained by adding one extra resistor and a diode.

Applications for the new current sources include bias networks, surge protection, low power reference, ramp generation LED driver, and temperature sensing The LM134-3/LM234-3 and LM134-6/LM234-6 are specified as true temperature sensors with guaranteed initial accuracy of ±3°C and ±6°C, respectively. These devices are ideal in remote sense applications because series resistance in long wire runs does not affect accuracy. In addition, only 2 wires are required.

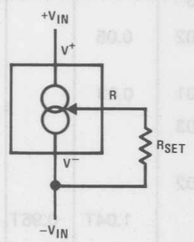
The LM134 is guaranteed over a temperature range of −55°C to +125°C, the LM234 from −25°C to +100°C and the LM334 from 0°C to +70°C. These devices are available in TO-46 hermetic and TO-92 plastic packages.

Features

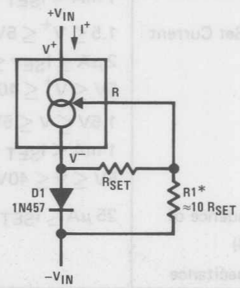
- Operates from 1V to 40V
- 0.02%/V current regulation
- Programmable from 1 μA to 10 mA
- True 2-terminal operation
- Available as fully specified temperature sensor
- ±3% initial accuracy

Typical Applications

Basic 2-Terminal Current Source

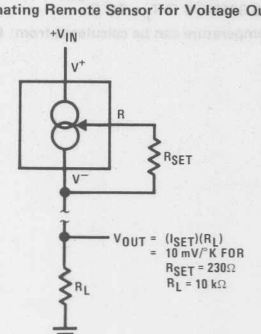


Zero Temperature Coefficient Current Source

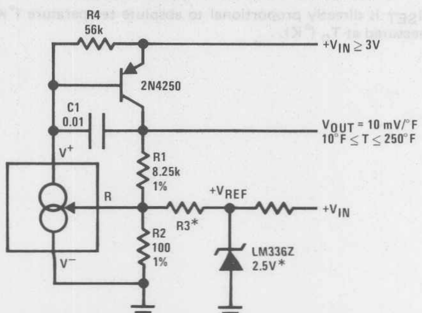


*Select ratio of R1 to R_{SET} to obtain zero drift. $I^+ \approx 2\ I_{SET}$

Terminating Remote Sensor for Voltage Output



Ground Referred Fahrenheit Thermometer



*Select R3 = V_{REF}/583 μA. V_{REF} may be any stable positive voltage ≥ 2V
Trim R3 to calibrate

Absolute Maximum Ratings

V^+ to V^- Forward Voltage	
LM134/LM234	40V
LM334/LM134-3/LM134-6/LM234-3/LM234-6	30V
V^+ to V^- Reverse Voltage	20V
R Pin to V^- Voltage	5V
Set Current	10 mA
Power Dissipation	200 mW
Operating Temperature Range	
LM134/LM134-3/LM134-6	-55°C to $+125^\circ$C
LM234/LM234-3/LM234-6	-25°C to $+100^\circ$C
LM334	0°C to $+70^\circ$C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	LM134/LM234			LM334			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Set Current Error, $V^+ = 2.5V$, (Note 2)	$10\ \mu A \leq I_{SET} \leq 1\ mA$			3			6	%
	$1\ mA < I_{SET} \leq 5\ mA$			5			8	%
	$2\ \mu A \leq I_{SET} < 10\ \mu A$			8			12	%
Ratio of Set Current to V^- Current	$10\ \mu A \leq I_{SET} \leq 1\ mA$	14	18	23	14	18	26	
	$1\ mA \leq I_{SET} \leq 5\ mA$		14			14		
	$2\ \mu A \leq I_{SET} \leq 10\ \mu A$		18	23	14	18	26	
Minimum Operating Voltage	$2\ \mu A \leq I_{SET} \leq 100\ \mu A$		0.8			0.8		V
	$100\ \mu A < I_{SET} \leq 1\ mA$		0.9			0.9		V
	$1\ mA < I_{SET} \leq 5\ mA$		1.0			1.0		V
Average Change in Set Current with Input Voltage	$1.5 \leq V^+ \leq 5V$		0.02	0.05		0.02	0.1	%/V
	$2\ \mu A \leq I_{SET} \leq 1\ mA$							
	$5V \leq V^+ \leq 40V$		0.01	0.03		0.01	0.05	%/V
	$1.5V \leq V \leq 5V$		0.03			0.03		%/V
	$1\ mA < I_{SET} \leq 5\ mA$							
	$5V \leq V \leq 40V$		0.02			0.02		%/V
Temperature Dependence of Set Current (Note 3)	$25\ \mu A \leq I_{SET} \leq 1\ mA$	0.96T	T	1.04T	0.96T	T	1.04T	
Effective Shunt Capacitance			15			15		pF

Note 1: Unless otherwise specified, tests are performed at $T_j = 25^\circ C$ with pulse testing so that junction temperature does not change during test.

Note 2: Set current is the current flowing into the V^+ pin. It is determined by the following formula: $I_{SET} = 67.7\ mV/R_{SET}$ (@ 25°C). Set current error is expressed as a percent deviation from this amount. I_{SET} increases at 0.336%/°C @ $T_j = 25^\circ C$.

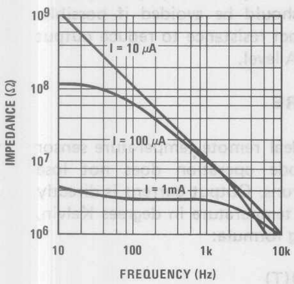
Note 3: I_{SET} is directly proportional to absolute temperature (°K). I_{SET} at any temperature can be calculated from: $I_{SET} = I_o\ (T/T_o)$ where I_o is I_{SET} measured at T_o (°K).

Electrical Characteristics (Continued) (Note 1)

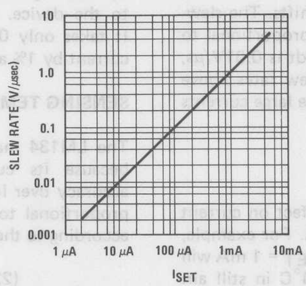
PARAMETER	CONDITIONS	LM134-3, LM234-3 MIN	TYP	MAX	LM134-6, LM234-6 MIN	TYP	MAX	UNITS
Set Current Error, $V^+ = 2.5V$, (Note 2)	$100\ \mu A \leq I_{SET} \leq 1\ mA$, $T_j = 25°C$		±1				±2	%
Equivalent Temperature Error			±3				±6	°C
Ratio of Set Current to V^- Current	$100\ \mu A \leq I_{SET} \leq 1\ mA$	14	18	26	14	18	26	
Minimum Operating Voltage	$100\ \mu A\ I_{SET} \leq 1\ mA$		0.9			0.9		V
Average Change in Set Current with Input Voltage	$1.5 \leq V^+ \leq 5V$, $100\ \mu A \leq I_{SET} \leq 1\ mA$		0.02	0.05		0.02	0.1	%/V
	$5V \leq V^+ \leq 30V$		0.01	0.03		0.01	0.05	%/V
Temperature Dependence of Set Current (Note 3)	$100\ \mu A \leq I_{SET} \leq 1\ mA$	0.98T	T	1.02T	0.97T	T	1.03T	
and Equivalent Slope Error			±2			±3		%
Effective Shunt Capacitance			15			15		pF

Typical Performance Characteristics

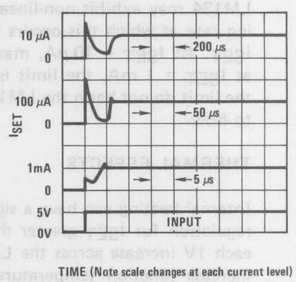
Output Impedance



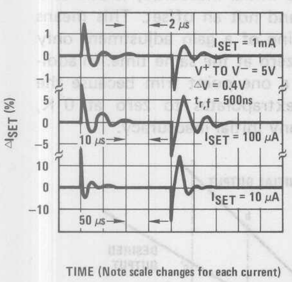
Maximum Slew Rate for Linear Operation



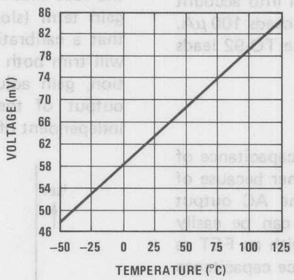
Start-Up



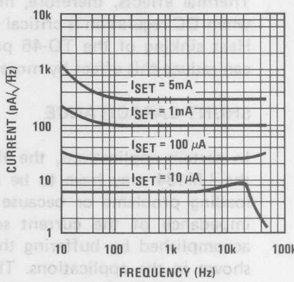
Transient Response



Voltage Across R_{SET}

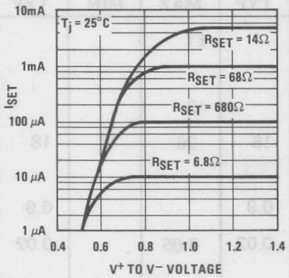


Current Noise

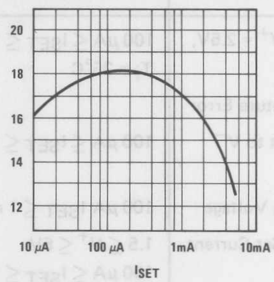


Typical Performance Characteristics (Continued)

Turn-On Voltage



Ratio of I_{SET} to V^- Current



Application Hints

The LM134 has been designed for ease of application, but a general discussion of design features is presented here to familiarize the designer with device characteristics which may not be immediately obvious. These include the effects of slewing, power dissipation, capacitance, noise, and contact resistance.

SLEW RATE

At slew rates above a given threshold (see curve), the LM134 may exhibit non-linear current shifts. The slewing rate at which this occurs is directly proportional to I_{SET}. At $I_{SET} = 10\,\mu A$, maximum dV/dt is $0.01V/\mu s$; at $I_{SET} = 1$ mA, the limit is $1V/\mu s$. Slew rates above the limit do not harm the LM134, or cause large currents to flow.

THERMAL EFFECTS

Internal heating can have a significant effect on current regulation for I_{SET} greater than 100 μA. For example, each 1V increase across the LM134 at $I_{SET} = 1$ mA will increase junction temperature by $\approx 0.4°C$ in still air. Output current (I_{SET}) has a temperature coefficient of $\approx 0.33\%/°C$, so the change in current due to temperature rise will be (0.4)(0.33) = 0.132%. This is a 10:1 degradation in regulation compared to true electrical effects. Thermal effects, therefore, must be taken into account when DC regulation is critical and I_{SET} exceeds 100 μA. Heat sinking of the TO-46 package or the TO-92 leads can reduce this effect by more than 3:1.

SHUNT CAPACITANCE

In certain applications, the 15 pF shunt capacitance of the LM134 may have to be reduced, either because of loading problems or because it limits the AC output impedance of the current source. This can be easily accomplished by buffering the LM134 with an FET as shown in the applications. This can reduce capacitance to less than 3 pF and improve regulation by at least an order of magnitude. DC characteristics (with the exception of minimum input voltage), are not affected.

NOISE

Current noise generated by the LM134 is approximately 4 times the shot noise of a transistor. If the LM134 is used as an active load for a transistor amplifier, input referred noise will be increased by about 12 dB. In many cases, this is acceptable and a single stage amplifier can be built with a voltage gain exceeding 2000.

LEAD RESISTANCE

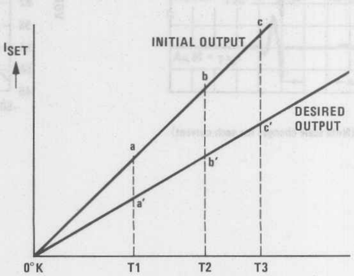
The sense voltage which determines operating current of the LM134 is less than 100 mV. At this level, thermocouple or lead resistance effects should be minimized by locating the current setting resistor physically close to the device. Sockets should be avoided if possible. It takes only 0.7Ω contact resistance to reduce output current by 1% at the 1 mA level.

SENSING TEMPERATURE

The LM134 makes an ideal remote temperature sensor because its current mode operation does not lose accuracy over long wire runs. Output current is directly proportional to absolute temperature in degrees Kelvin, according to the following formula:

$$I_{SET} = \frac{(227\,\mu V/°K)(T)}{R_{SET}}$$

Calibration of the LM134 is greatly simplified because of the fact that most of the initial inaccuracy is due to a gain term (slope error) and not an offset. This means that a calibration consisting of a gain adjustment only will trim both slope and zero at the same time. In addition, gain adjustment is a one point trim because the output of the LM134 extrapolates to zero at 0°K, independent of R_{SET} or any initial inaccuracy.



This property of the LM134 is illustrated in the accompanying graph. Line abc is the sensor current before

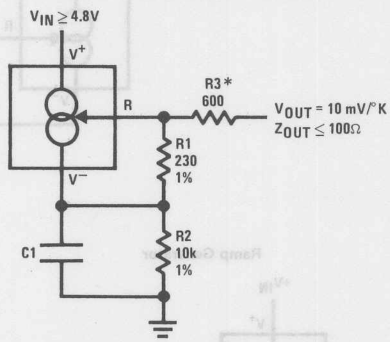
Application Hints (Continued)

trimming. Line a'b'c' is the desired output. A gain trim done at T2 will move the output from b to b' and will simultaneously correct the slope so that the output at T1 and T3 will be correct. This gain trim can be done on R_{SET} or on the load resistor used to terminate the LM134. Slope error after trim will normally be less than ±1%. To maintain this accuracy, however, a low temperature coefficient resistor must be used for R_{SET}.

A 33 ppm/°C drift of R_{SET} will give a 1% slope error because the resistor will normally see about the same temperature variations as the LM134. Separating R_{SET} from the LM134 requires 3 wires and has lead resistance problems, so is not normally recommended. Metal film resistors with less than 20 ppm/°C drift are readily available. Wire wound resistors may also be used where best stability is required.

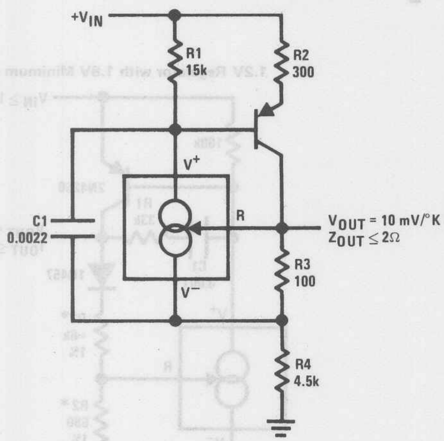
Typical Applications (Continued)

Low Output Impedance Thermometer

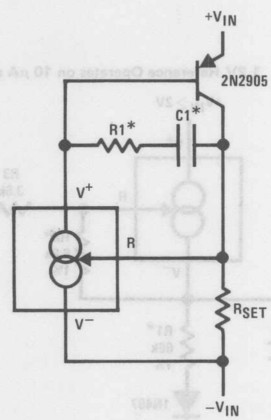


*Output impedance of the LM134 at the "R" pin is approximately $\frac{-R_o\ \Omega}{16}$, where R_o is the equivalent external resistance connected to the V^- pin. This negative resistance can be reduced by a factor of 5 or more by inserting an equivalent resistor in series with the output.

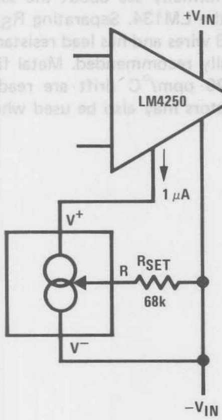
Low Output Impedance Thermometer

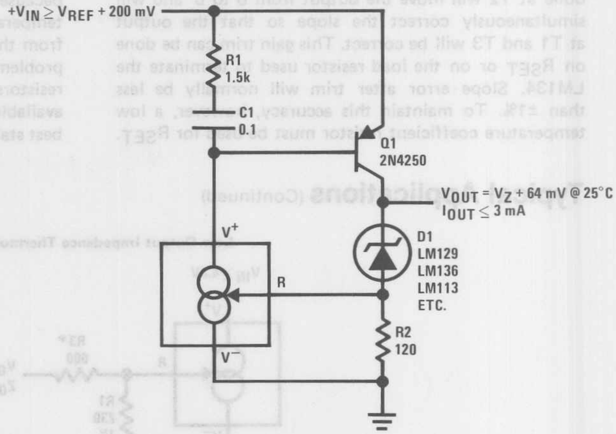


Higher Output Current

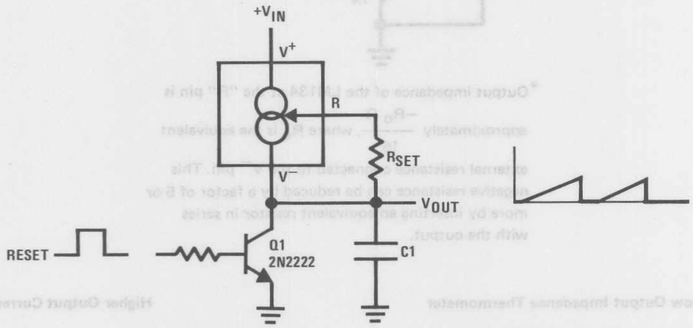


*Select R1 and C1 for optimum stability

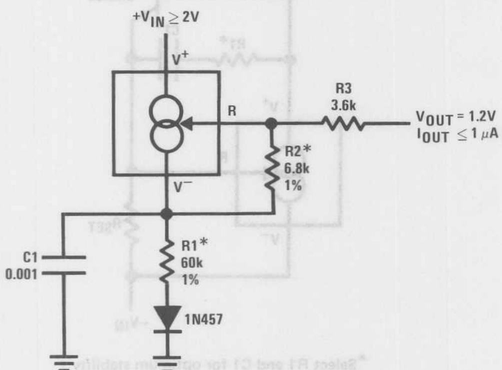




Ramp Generator

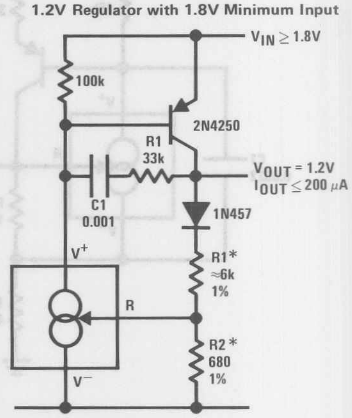


1.2V Reference Operates on 10 μA and 2V



*Select ratio of R1 to R2 to obtain zero temperature drift

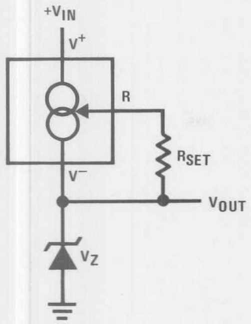
1.2V Regulator with 1.8V Minimum Input



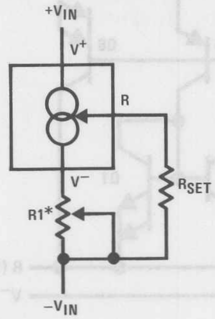
*Select ratio of R1 to R2 for zero temperature drift

Typical Applications (Continued)

Zener Biasing

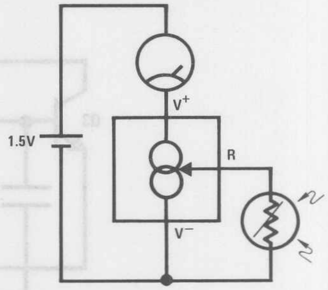


Alternate Trimming Technique

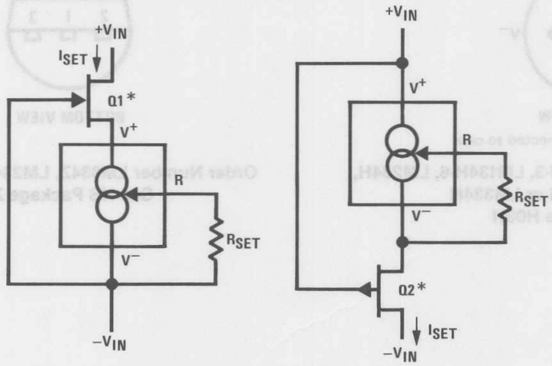


*For ±10% adjustment, select R_{SET} 10% high, and make R1 ≈ 3 R_{SET}

Buffer for Photoconductive Cell

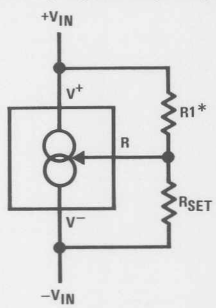


FET Cascoding for Low Capacitance and/or Ultra High Output Impedance



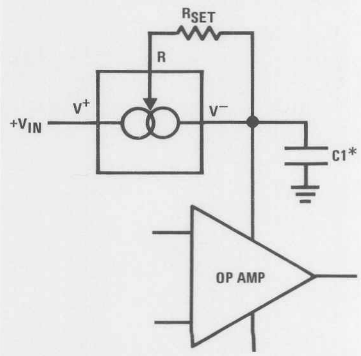
*Select Q1 or Q2 to ensure at least 1V across the LM134. $V_P\ (1 - I_{SET}/I_{DSS}) \geq 1.2V$.

Generating Negative Output Impedance



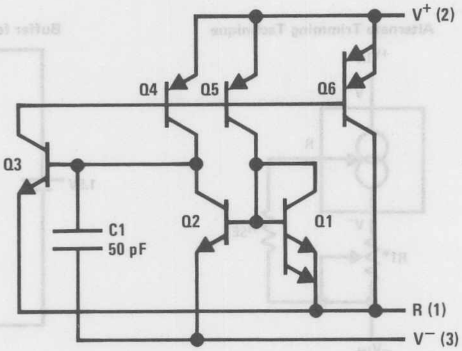
*$Z_{OUT} \approx -16 \cdot R1$ ($R1/V_{IN}$ must not exceed I_{SET})

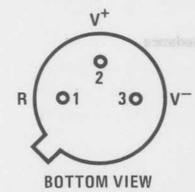
In-Line Current Limiter



*Use minimum value required to ensure stability of protected device. This minimizes inrush current to a direct short.

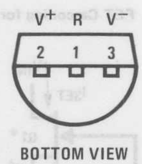
Schematic and Connection Diagrams





Pin 3 is electrically connected to case

Order Number LM134H, LM134H-3, LM134H-6, LM234H, LM234H-3, LM234H-6 or LM334H
See NS Package H03H



Order Number LM334Z, LM234Z-3 or LM234Z-6
See NS Package Z03A

LM135/LM235/LM335, LM135A/LM235A/LM335A Precision Temperature Sensors

General Description

The LM135 series are precision, easily-calibrated, integrated circuit temperature sensors. Operating as a 2-terminal zener, the LM135 has a breakdown voltage directly proportional to absolute temperature at +10 mV/°K. With less than 1Ω dynamic impedance the device operates over a current range of 400 μA to 5 mA with virtually no change in performance. When calibrated at 25°C the LM135 has typically less than 1°C error over 100°C temperature range. Unlike other sensors the LM135 has a linear output.

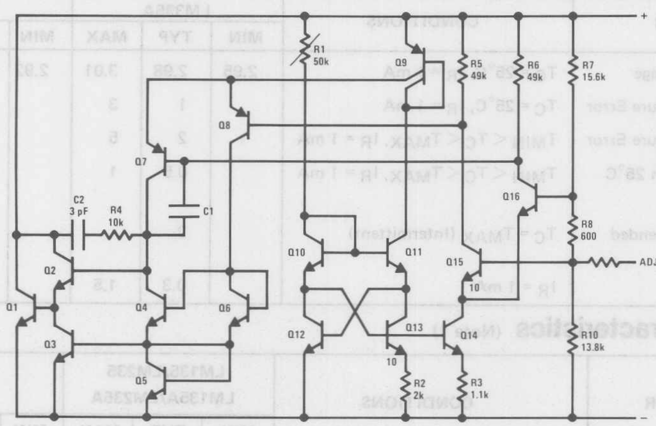
Applications for the LM135 include almost any type of temperature sensing over a −55°C to +150°C temperature range. The low impedance and linear output make interfacing to readout or control circuitry especially easy.

The LM135 operates over a −55°C to +150°C temperature range while the LM235 operates over a −40°C to +125°C temperature range. The LM335 operates from −40°C to +100°C. The LM135/LM235/LM335 are available packaged in hermetic TO-46 transistor packages while the LM335 is also available in plastic TO-92 packages.

Features

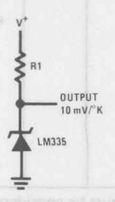
- Directly calibrated in °Kelvin
- 1°C initial accuracy available
- Operates from 400 μA to 5 mA
- Less than 1Ω dynamic impedance
- Easily calibrated
- Wide operating temperature range
- 200°C overrange
- Low cost

Schematic Diagram

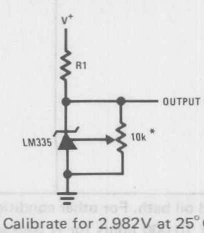


Typical Applications

Basic Temperature Sensor

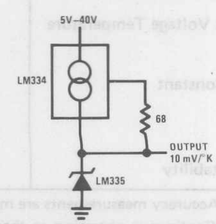


Calibrated Sensor



*Calibrate for 2.982V at 25°C

Wide Operating Supply



Absolute Maximum Ratings

Reverse Current		15 mA
Forward Current		10 mA
Storage Temperature		
TO-46 Package		$-60^\circ C$ to $+180^\circ C$
TO-92 Package		$-60^\circ C$ to $+150^\circ C$
Specified Operating Temperature Range		
	Continuous	**Intermittent (Note 2)**
LM135, LM135A	$-55^\circ C$ to $+150^\circ C$	$150^\circ C$ to $200^\circ C$
LM235, LM235A	$-40^\circ C$ to $+125^\circ C$	$125^\circ C$ to $150^\circ C$
LM335, LM335A	$-40^\circ C$ to $+100^\circ C$	$100^\circ C$ to $125^\circ C$
Lead Temperature (Soldering, 10 seconds)		$300^\circ C$

Temperature Accuracy LM135/LM235, LM135A/LM235A (Note 1)

PARAMETER	CONDITIONS	LM135A/LM235A			LM135/LM235			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Operating Output Voltage	$T_C = 25^\circ C$, $I_R = 1$ mA	2.97	2.98	2.99	2.95	2.98	3.01	V
Uncalibrated Temperature Error	$T_C = 25^\circ C$, $I_R = 1$ mA		0.5	1		1	3	°C
Uncalibrated Temperature Error	$T_{MIN} < T_C < T_{MAX}$, $I_R = 1$ mA		1.3	2.7		2	5	°C
Temperature Error with 25°C Calibration	$T_{MIN} < T_C < T_{MAX}$, $I_R = 1$ mA		0.3	1		0.5	1.5	°C
Calibrated Error at Extended Temperatures	$T_C = T_{MAX}$ (Intermittent)		2			2		°C
Non-Linearity	$I_R = 1$ mA		0.3	0.5		0.3	1	°C

Temperature Accuracy LM335, LM335A (Note 1)

PARAMETER	CONDITIONS	LM335A			LM335			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Operating Output Voltage	$T_C = 25^\circ C$, $I_R = 1$ mA	2.95	2.98	3.01	2.92	2.98	3.04	V
Uncalibrated Temperature Error	$T_C = 25^\circ C$, $I_R = 1$ mA		1	3		2	6	°C
Uncalibrated Temperature Error	$T_{MIN} < T_C < T_{MAX}$, $I_R = 1$ mA		2	5		4	9	°C
Temperature Error with 25°C Calibration	$T_{MIN} < T_C < T_{MAX}$, $I_R = 1$ mA		0.5	1		1	2	°C
Calibrated Error at Extended Temperatures	$T_C = T_{MAX}$ (Intermittent)		2			2		°C
Non-Linearity	$I_R = 1$ mA		0.3	1.5		0.3	1.5	°C

Electrical Characteristics (Note 1)

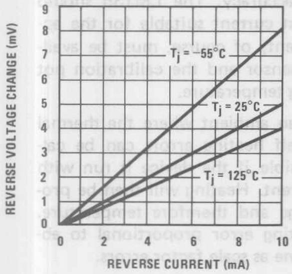
PARAMETER	CONDITIONS	LM135/LM235 LM135A/LM235A			LM335 LM335A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Operating Output Voltage Change with Current	$400\ \mu A < I_R < 5$ mA At Constant Temperature		2.5	10		3	14	mV
Dynamic Impedance	$I_R = 1$ mA		0.5			0.6		Ω
Output Voltage Temperature Drift			+10			+10		mV/°C
Time Constant	Still Air		80			80		sec
	100 ft/Min Air		10			10		sec
	Stirred Oil		1			1		sec
Time Stability	$T_C = 125^\circ C$		0.2			0.2		°C/khr

Note 1: Accuracy measurements are made in a well-stirred oil bath. For other conditions, self heating must be considered.

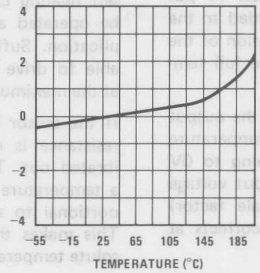
Note 2: Continuous operation at these temperatures for 10,000 hours for H package and 5,000 hours for Z package may decrease life expectancy of the device.

Typical Performance Characteristics

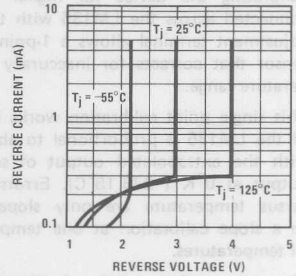
Reverse Voltage Change



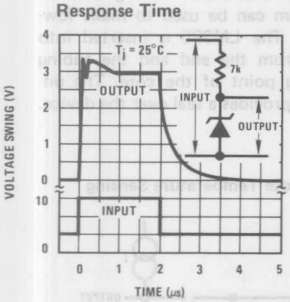
Calibrated Error



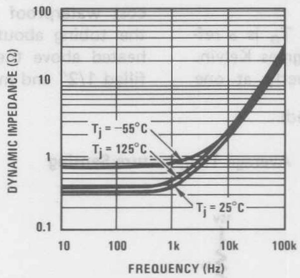
Reverse Characteristics



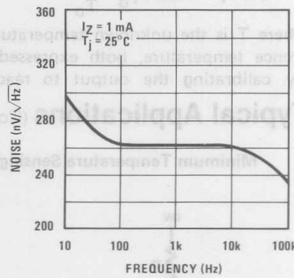
Response Time



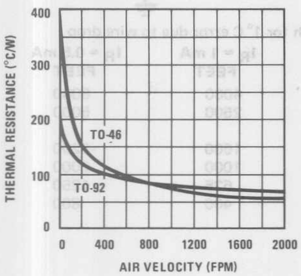
Dynamic Impedance



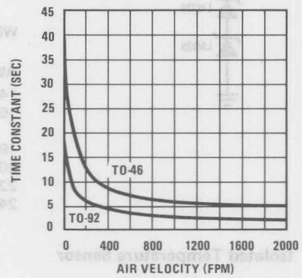
Noise Voltage



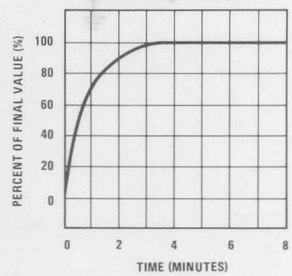
Thermal Resistance Junction to Air



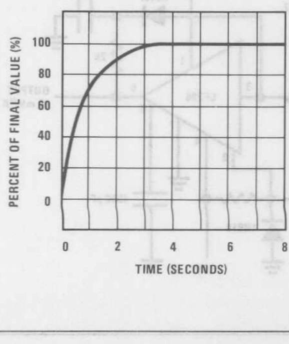
Thermal Time Constant



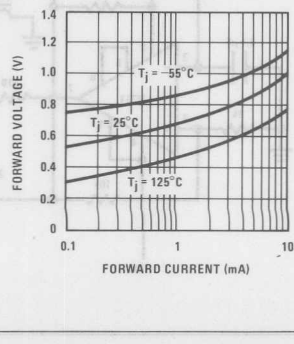
Thermal Response in Still Air



Thermal Response in Stirred Oil Bath



Forward Characteristics



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calibrating the device for higher accuracies. A pot connected across the LM135 with the arm tied to the adjustment terminal allows a 1-point calibration of the sensor that corrects for inaccuracy over the full temperature range.

This single point calibration works because the output of the LM135 is proportional to absolute temperature with the extrapolated output of sensor going to 0V output at 0°K (−273.15°C). Errors in output voltage versus temperature are only slope (or scale factor) so a slope calibration at one temperature corrects at all temperatures.

The output of the device (calibrated or uncalibrated) can be expressed as:

$$V_{OUT_T} = V_{OUT_{T_O}} \times \frac{T}{T_O}$$

where T is the unknown temperature and T_O is a reference temperature, both expressed in degrees Kelvin. By calibrating the output to read correctly at one

must be taken. Like any temperature sensing device, self heating can reduce accuracy. The LM135 should be operated at the lowest current suitable for the application. Sufficient current, of course, must be available to drive both the sensor and the calibration pot at the maximum operating temperature.

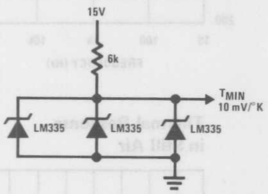
If the sensor is used in an ambient where the thermal resistance is constant, self heating errors can be calibrated out. This is possible if the device is run with a temperature stable current. Heating will then be proportional to zener voltage and therefore temperature. This makes the self heating error proportional to absolute temperature the same as scale factor errors.

WATERPROOFING SENSORS

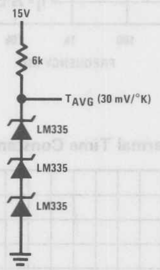
Meltable inner core heat shrinkable tubing such as manufactured by Raychem can be used to make low-cost waterproof sensors. The LM335 is inserted into the tubing about 1/2″ from the end and the tubing heated above the melting point of the core. The unfilled 1/2″ end melts and provides a seal over the device.

Typical Applications (Continued)

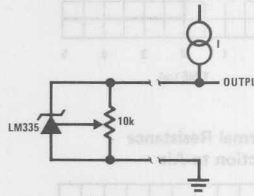
Minimum Temperature Sensing



Average Temperature Sensing



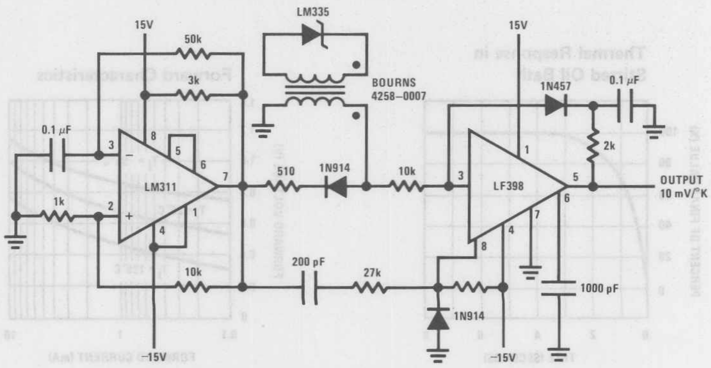
Remote Temperature Sensing



Wire length for 1° C error due to wire drop

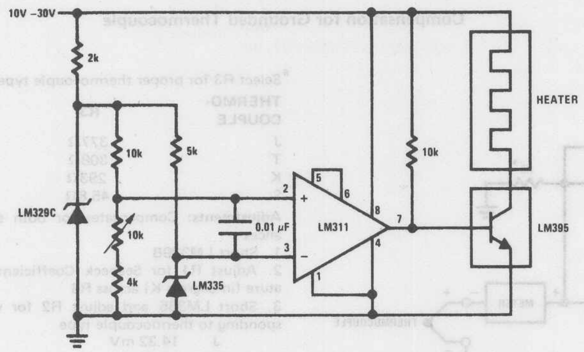
AWG	I_R = 1 mA FEET	I_R = 0.5 mA FEET
14	4000	8000
16	2500	5000
18	1600	3200
20	1000	2000
22	625	1250
24	400	800

Isolated Temperature Sensor

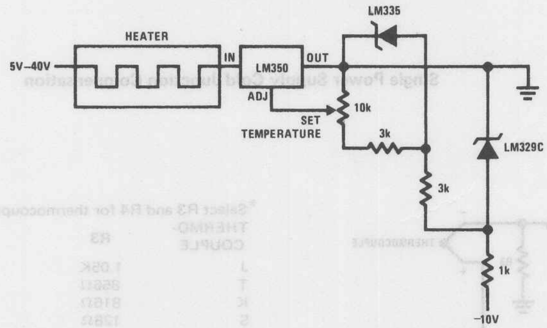


Typical Applications (Continued)

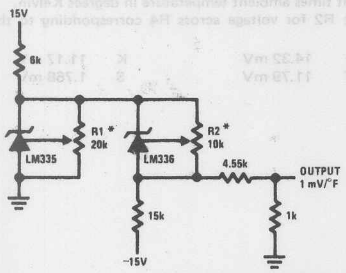
Simple Temperature Controller



Simple Temperature Control

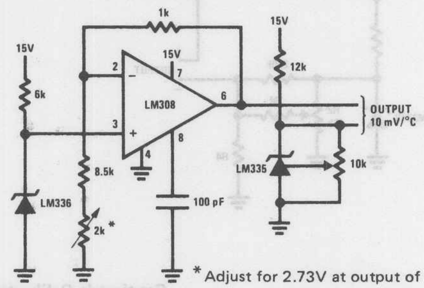


Ground Referred Fahrenheit Thermometer



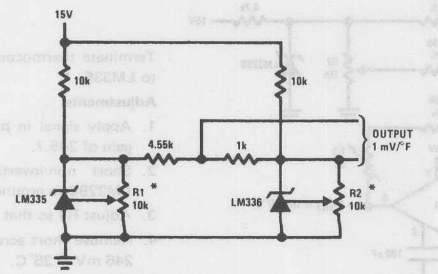
*Adjust R2 for 2.554V across LM336.
Adjust R1 for correct output.

Centigrade Thermometer



*Adjust for 2.73V at output of LM308

Fahrenheit Thermometer

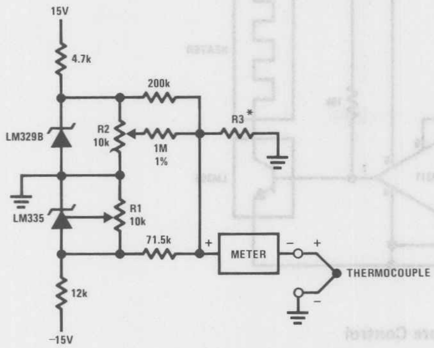


*To calibrate adjust R2 for 2.554V across LM336.
Adjust R1 for correct output.

Typical Applications (Continued)

THERMOCOUPLE COLD JUNCTION COMPENSATION

Compensation for Grounded Thermocouple



*Select R3 for proper thermocouple type

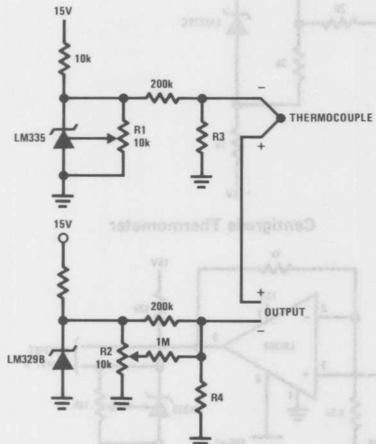
THERMO-COUPLE	R3	SEEBECK COEFFICIENT
J	377Ω	52.3 μV/°C
T	308Ω	42.8 μV/°C
K	293Ω	40.8 μV/°C
S	45.8Ω	6.4 μV/°C

Adjustments: Compensates for both sensor and resistor tolerances

1. Short LM329B
2. Adjust R1 for Seebeck Coefficient times ambient temperature (in degrees K) across R3
3. Short LM335 and adjust R2 for voltage across R3 corresponding to thermocouple type

J	14.32 mV	K	11.17 mV
T	11.79 mV	S	1.768 mV

Single Power Supply Cold Junction Compensation



*Select R3 and R4 for thermocouple type

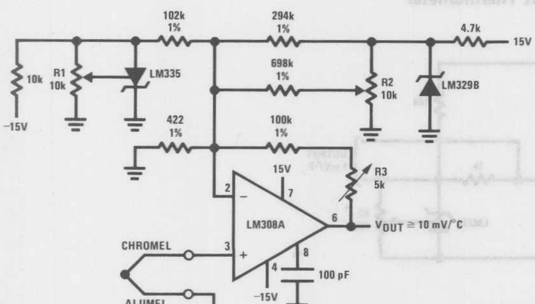
THERMO-COUPLE	R3	R4	SEEBECK COEFFICIENT
J	1.05K	385Ω	52.3 μV/°C
T	856Ω	315Ω	42.8 μV/°C
K	816Ω	300Ω	40.8 μV/°C
S	128Ω	46.3Ω	6.4 μV/°C

Adjustments:

1. Adjust R1 for the voltage across R3 equal to the Seebeck Coefficient times ambient temperature in degrees Kelvin.
2. Adjust R2 for voltage across R4 corresponding to thermocouple

J	14.32 mV	K	11.17 mV
T	11.79 mV	S	1.768 mV

Centigrade Calibrated Thermocouple Thermometer



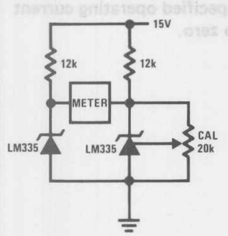
Terminate thermocouple reference junction in close proximity to LM335.

Adjustments:

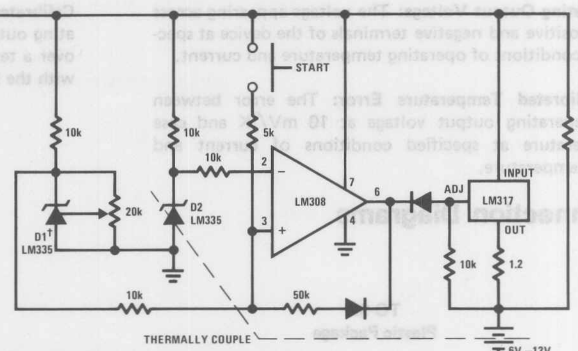
1. Apply signal in place of thermocouple and adjust R3 for a gain of 245.7.
2. Short non-inverting input of LM308A and output of LM329B to ground.
3. Adjust R1 so that V_{OUT} = 2.982V @ 25°C.
4. Remove short across LM329B and adjust R2 so that V_{OUT} = 246 mV @ 25°C.
5. Remove short across thermocouple.

Typical Applications (Continued)

Differential Temperature Sensor

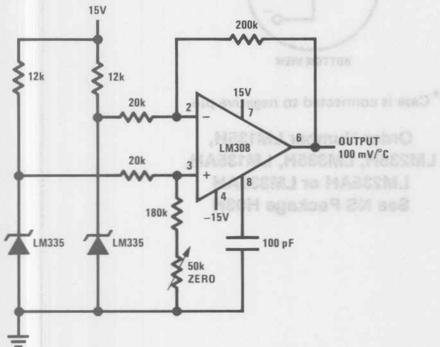


Fast Charger for Nickel-Cadmium Batteries

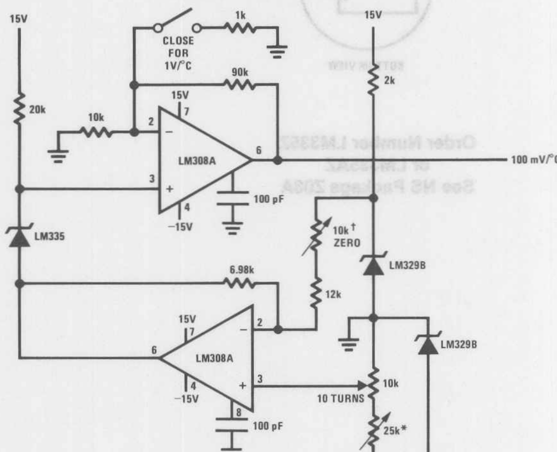


†Adjust D1 to 50 mV greater V_Z than D2.
Charge terminates on 5°C temperature rise. Couple D2 to battery.

Differential Temperature Sensor



Variable Offset Thermometer‡

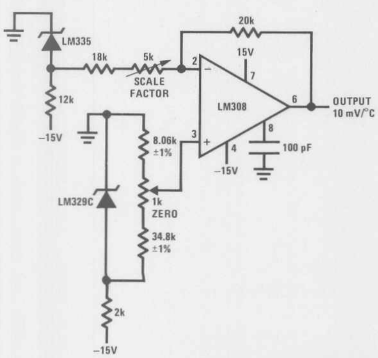


†Adjust for zero with sensor at 0°C and 10T pot set at 0°C

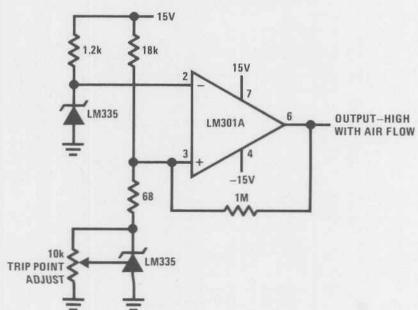
*Adjust for zero output with 10T pot set at 100°C and sensor at 100°C

‡Output reads difference between temperature and dial setting of 10T pot

Ground Referred Centigrade Thermometer



Air Flow Detector*



*Self heating is used to detect air flow

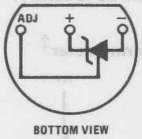
the positive and negative terminals of the device at specified conditions of operating temperature and current.

Uncalibrated Temperature Error: The error between the operating output voltage at 10 mV/°K and case temperature at specified conditions of current and case temperature.

ating output voltage and case temperature at 10 mV/°K over a temperature range at a specified operating current with the 25°C error adjusted to zero.

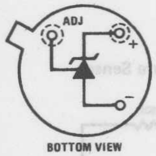
Connection Diagrams

TO-92
Plastic Package



Order Number LM335Z or LM335AZ
See NS Package Z03A

TO-46
Metal Can Package*



*Case is connected to negative pin

Order Number LM135H, LM235H, LM335H, LM135AH, LM235AH or LM335AH
See NS Package H03H

National Semiconductor

LM555/LM555C Timer

General Description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200 mA or drive TTL circuits.

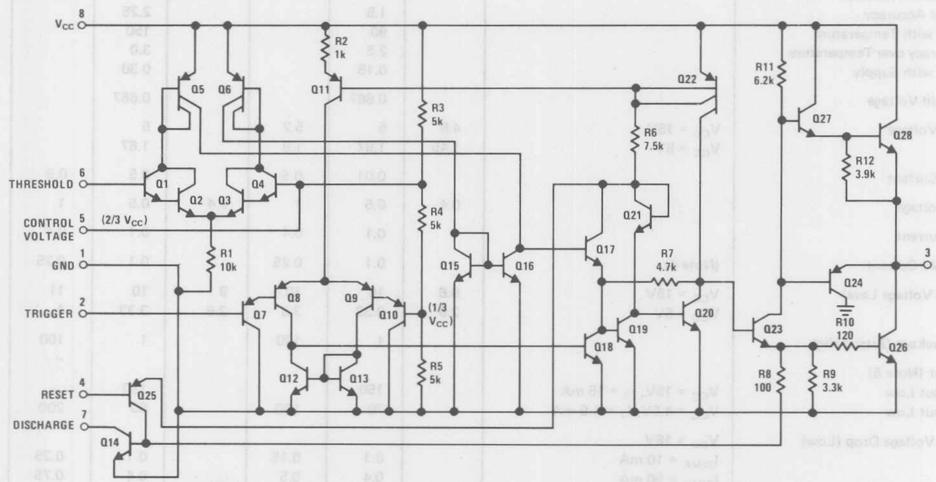
Features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output

Applications

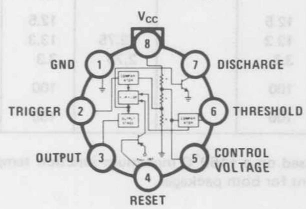
- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

Schematic Diagram



Connection Diagrams

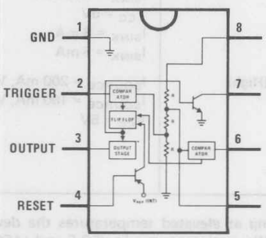
Metal Can Package



TOP VIEW

Order Number LM555H, LM555CH
See NS Package H08C

Dual-In-Line Package



TOP VIEW

Order Number LM555CN
See NS Package N08B
Order Number LM555J or LM555CJ
See NS Package J08A

Absolute Maximum Ratings

Supply Voltage	+18V
Power Dissipation (Note 1)	600 mW
Operating Temperature Ranges	
LM555C	0°C to +70°C
LM555	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (T_A = 25°C, V_{CC} = +5V to +15V, unless otherwise specified)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LM555			LM555C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage		4.5		18	4.5		16	V
Supply Current	V_{CC} = 5V, $R_L = \infty$		3	5		3	6	mA
	V_{CC} = 15V, $R_L = \infty$		10	12		10	15	mA
	(Low State) (Note 2)							
Timing Error, Monostable								
Initial Accuracy			0.5			1		%
Drift with Temperature	R_A, R_B = 1k to 100 k,		30			50		ppm/°C
	C = 0.1μF, (Note 3)							
Accuracy over Temperature			1.5			1.5		%
Drift with Supply			0.05			0.1		%/V
Timing Error, Astable								
Initial Accuracy			1.5			2.25		%
Drift with Temperature			90			150		ppm/°C
Accuracy over Temperature			2.5			3.0		%
Drift with Supply			0.15			0.30		%/V
Threshold Voltage			0.667			0.667		x V_{CC}
Trigger Voltage	V_{CC} = 15V	4.8	5	5.2		5		V
	V_{CC} = 5V	1.45	1.67	1.9		1.67		V
Trigger Current			0.01	0.5		0.5	0.9	μA
Reset Voltage		0.4	0.5	1	0.4	0.5	1	V
Reset Current			0.1	0.4		0.1	0.4	mA
Threshold Current	(Note 4)		0.1	0.25		0.1	0.25	μA
Control Voltage Level	V_{CC} = 15V	9.6	10	10.4	9	10	11	V
	V_{CC} = 5V	2.9	3.33	3.8	2.6	3.33	4	V
Pin 7 Leakage Output High			1	100		1	100	nA
Pin 7 Sat (Note 5)								
Output Low	V_{CC} = 15V, I_7 = 15 mA		150			180		mV
Output Low	V_{CC} = 4.5V, I_7 = 4.5 mA		70	100		80	200	mV
Output Voltage Drop (Low)	V_{CC} = 15V							
	I_{SINK} = 10 mA		0.1	0.15		0.1	0.25	V
	I_{SINK} = 50 mA		0.4	0.5		0.4	0.75	V
	I_{SINK} = 100 mA		2	2.2		2	2.5	V
	I_{SINK} = 200 mA		2.5			2.5		V
	V_{CC} = 5V							
	I_{SINK} = 8 mA		0.1	0.25				V
	I_{SINK} = 5 mA					0.25	0.35	V
Output Voltage Drop (High)	I_{SOURCE} = 200 mA, V_{CC} = 15V		12.5			12.5		V
	I_{SOURCE} = 100 mA, V_{CC} = 15V	13	13.3		12.75	13.3		V
	V_{CC} = 5V	3	3.3		2.75	3.3		V
Rise Time of Output			100			100		ns
Fall Time of Output			100			100		ns

Note 1: For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of +45°C/W junction to case for TO-5 and +150°C/W junction to ambient for both packages.

Note 2: Supply current when output high typically 1 mA less at V_{CC} = 5V.

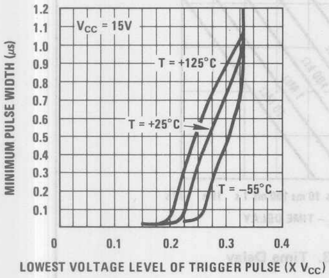
Note 3: Tested at V_{CC} = 5V and V_{CC} = 15V.

Note 4: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total ($R_A + R_B$) is 20 MΩ.

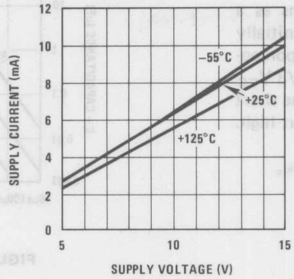
Note 5: No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.

Typical Performance Characteristics

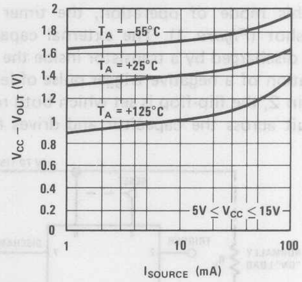
Minimum Pulse Width Required for Triggering



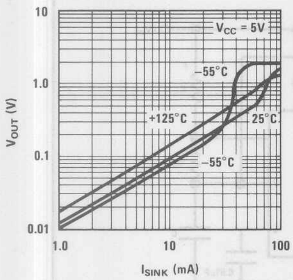
Supply Current vs Supply Voltage



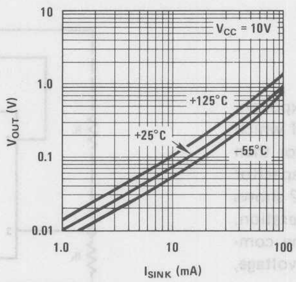
High Output Voltage vs Output Source Current



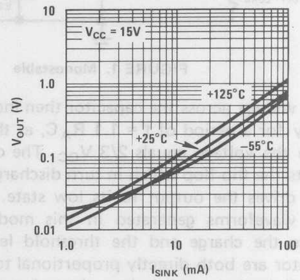
Low Output Voltage vs Output Sink Current



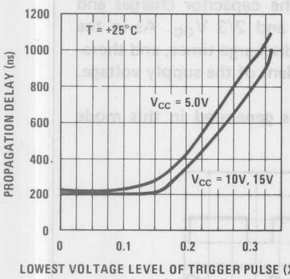
Low Output Voltage vs Output Sink Current



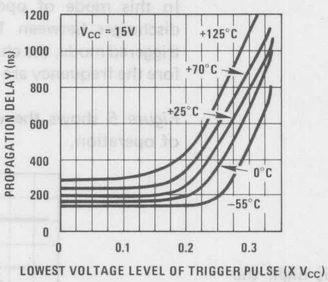
Low Output Voltage vs Output Sink Current



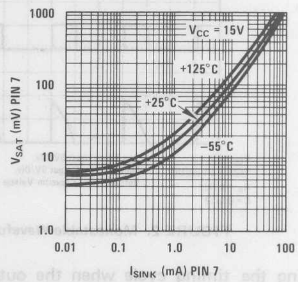
Output Propagation Delay vs Voltage Level of Trigger Pulse



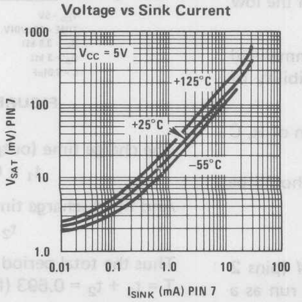
Output Propagation Delay vs Voltage Level of Trigger Pulse



Discharge Transistor (Pin 7) Voltage vs Sink Current



Discharge Transistor (Pin 7) Voltage vs Sink Current



In this mode of operation, the timer functions as a one-shot (*Figure 1*). The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than 1/3 V_{CC} to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.

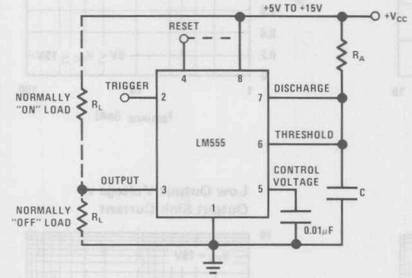


FIGURE 1. Monostable

The voltage across the capacitor then increases exponentially for a period of t = 1.1 R_AC, at the end of which time the voltage equals 2/3 V_{CC}. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. *Figure 2* shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing internal is independent of supply.

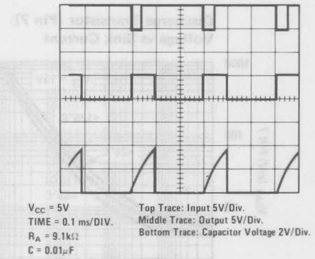


FIGURE 2. Monostable Waveforms

During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.

Figure 3 is a nomograph for easy determination of R, C values for various time delays.

NOTE: In monostable operation, the trigger should be driven high before the end of timing cycle.

ASTABLE OPERATION

If the circuit is connected as shown in *Figure 4* (pins 2 and 6 connected) it will trigger itself and free run as a

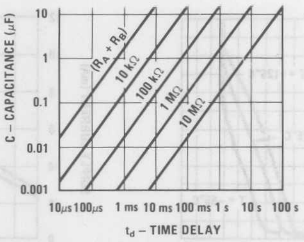


FIGURE 3. Time Delay

multivibrator. The external capacitor charges through $R_A + R_B$ and discharges through R_B. Thus the duty cycle may be precisely set by the ratio of these two resistors.

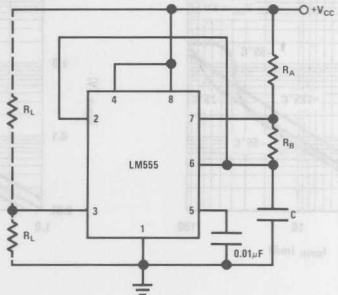


FIGURE 4. Astable

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Figure 5 shows the waveforms generated in this mode of operation.

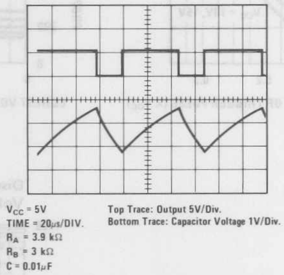


FIGURE 5. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693\ (R_A + R_B)\ C$$

And the discharge time (output low) by:

$$t_2 = 0.693\ (R_B)\ C$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693\ (R_A + 2R_B)\ C$$

Applications Information (Continued)

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2\,R_B)\,C}$$

Figure 6 may be used for quick determination of these RC values.

The duty cycle is: $$D = \frac{R_B}{R_A + 2R_B}$$

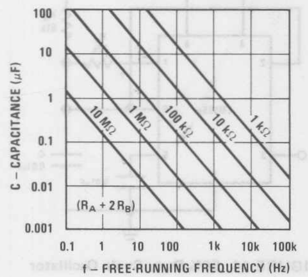


FIGURE 6. Free Running Frequency

FREQUENCY DIVIDER

The monostable circuit of *Figure 1* can be used as a frequency divider by adjusting the length of the timing cycle. *Figure 7* shows the waveforms generated in a divide by three circuit.

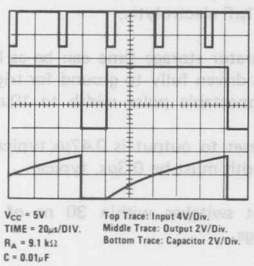


FIGURE 7. Frequency Divider

PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. *Figure 8* shows the circuit, and in *Figure 9* are some waveform examples.

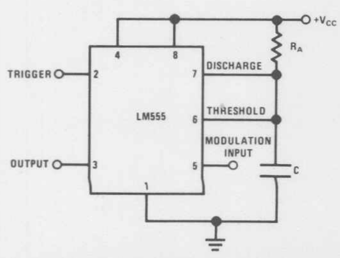


FIGURE 8. Pulse Width Modulator

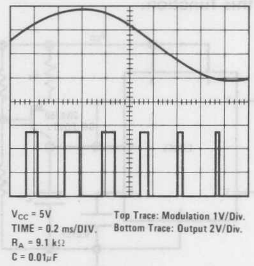


FIGURE 9. Pulse Width Modulator

PULSE POSITION MODULATOR

This application uses the timer connected for astable operation, as in *Figure 10,* with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. *Figure 11* shows the waveforms generated for a triangle wave modulation signal.

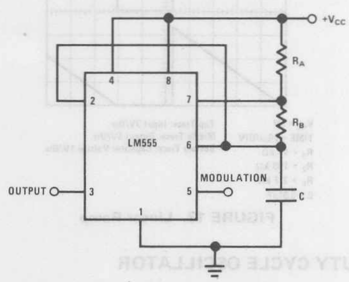


FIGURE 10. Pulse Position Modulator

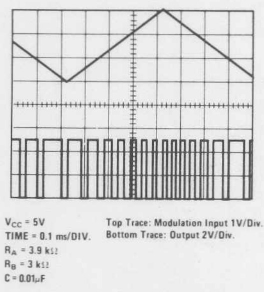


FIGURE 11. Pulse Position Modulator

LINEAR RAMP

When the pullup resistor, R_A, in the monostable circuit is replaced by a constant current source, a linear ramp is

Applications Information (Continued)

generated. *Figure 12* shows a circuit configuration that will perform this function.

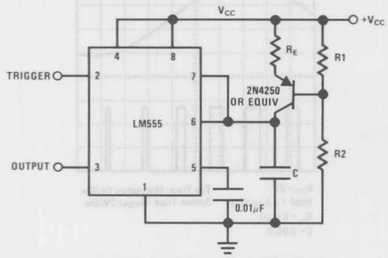


FIGURE 12.

Figure 13 shows waveforms generated by the linear ramp.

The time interval is given by:

$$T = \frac{2/3\ V_{CC}\ R_E\ (R_1 + R_2)\ C}{R_1\ V_{CC} - V_{BE}\ (R_1 + R_2)}$$

$$V_{BE} \simeq 0.6V$$

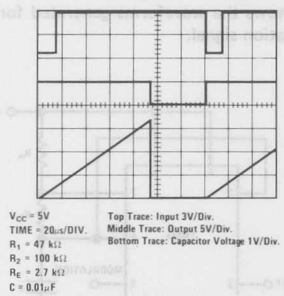


FIGURE 13. Linear Ramp

50% DUTY CYCLE OSCILLATOR

For a 50% duty cycle, the resistors R_A and R_B may be connected as in *Figure 14*. The time period for the output high is the same as previous, $t_1 = 0.693\ R_A\ C$. For the output low it is $t_2 =$

$$[(R_A\ R_B)/(R_A + R_B)]\ CLn \left[\frac{R_B - 2R_A}{2R_B - R_A}\right]$$

Thus the frequency of oscillation is $f = \dfrac{1}{t_1 + t_2}$

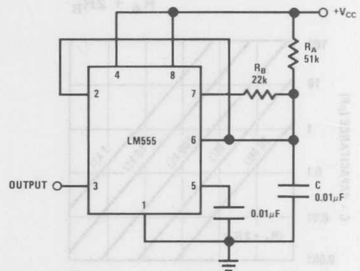


FIGURE 14. 50% Duty Cycle Oscillator

Note that this circuit will not oscillate if R_B is greater than 1/2 R_A because the junction of R_A and R_B cannot bring pin 2 down to 1/3 V_{CC} and trigger the lower comparator.

ADDITIONAL INFORMATION

Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1µF in parallel with 1µF electrolytic.

Lower comparator storage time can be as long as 10µs when pin 2 is driven fully to ground for triggering. This limits the monostable pulse width to 10µs minimum.

Delay time reset to output is 0.47µs typical. Minimum reset pulse width must be 0.3µs, typical.

Pin 7 current switches within 30 ns of the output (pin 3) voltage.

LM556/LM556C Dual Timer

General Description

The LM556 Dual timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. The 556 is a dual 555. Timing is provided by an external resistor and capacitor for each timing function. The two timers operate independently of each other sharing only V_{CC} and ground. The circuits may be triggered and reset on falling waveforms. The output structures may sink or source 200 mA.

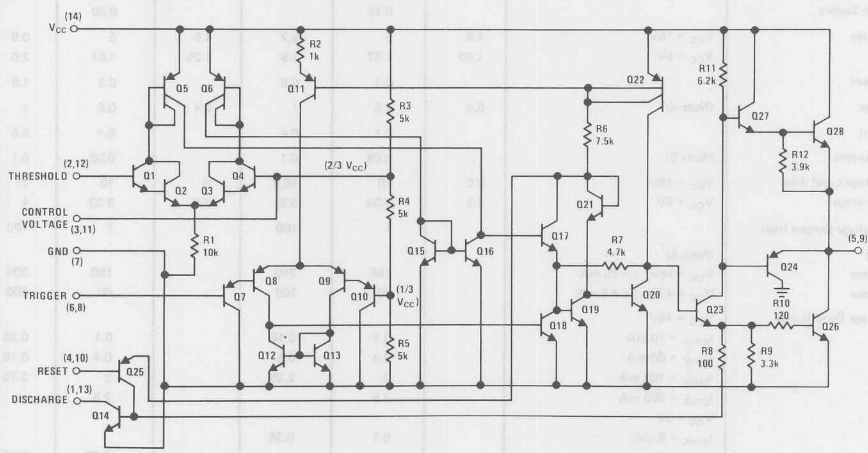
Features

- Direct replacement for SE556/NE556
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Replaces two 555 timers
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output

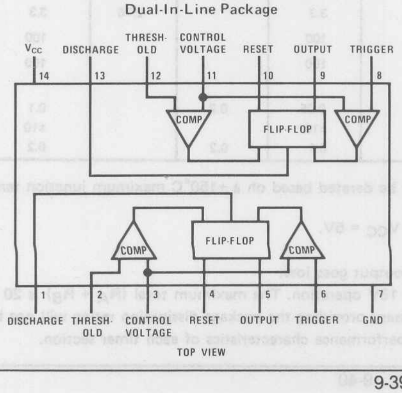
Applications

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

Schematic Diagram



Connection Diagram



Order Number LM556CN
See NS Package N14A

Order Number LM556J or LM556CJ
See NS Package J14A

Operating Temperature Ranges	
LM556C	0°C to +70°C
LM556	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (T_A = 25°C, V_{CC} = +5V to +15V, unless otherwise specified)

PARAMETER	CONDITIONS	LM556 MIN	LM556 TYP	LM556 MAX	LM556C MIN	LM556C TYP	LM556C MAX	UNITS
Supply Voltage		4.5		18	4.5		16	V
Supply Current	V_{CC} = 5V, $R_L = \infty$		3	5		3	6	mA
(Each Timer Section)	V_{CC} = 15V, $R_L = \infty$		10	11		10	14	mA
	(Low State) (Note 2)							
Timing Error, Monostable								
Initial Accuracy			0.5			0.75		%
Drift With Temperature	R_A, R_B = 1k to 100k, C = 0.1μF, (Note 3)		30			50		ppm/°C
Accuracy Over Temperature			1.5			1.5		%
Drift with Supply			0.05			0.1		%/V
Timing Error, Astable								
Initial Accuracy			1.5			2.25		%
Drift With Temperature			90			150		ppm/°C
Accuracy Over Temperature			2.5			3.0		%
Drift With Supply			0.15			0.30		%/V
Trigger Voltage	V_{CC} = 15V	4.8	5	5.2	4.5	5	0.5	V
	V_{CC} = 5V	1.45	1.67	1.9	1.25	1.67	2.0	V
Trigger Current			0.1	0.5		0.2	1.0	μA
Reset Voltage	(Note 4)	0.4	0.5	1	0.4	0.5	1	V
Reset Current			0.1	0.4		0.1	0.6	mA
Threshold Current	(Note 5)		0.03	0.1		0.03	0.1	μA
Control Voltage Level And	V_{CC} = 15V	9.6	10	10.4	9	10	11	V
Threshold Voltage	V_{CC} = 5V	2.9	3.33	3.8	2.6	3.33	4	V
Pin 1, 13 Leakage Output High			1	100		1	100	nA
Pin 1, 13 Sat	(Note 6)							
Output Low	V_{CC} = 15V, I = 15 mA		150	240		180	300	mV
Output Low	V_{CC} = 4.5V, I = 4.5 mA		70	100		80	200	mV
Output Voltage Drop (Low)	V_{CC} = 15V							
	I_{SINK} = 10 mA		0.1	0.15		0.1	0.25	V
	I_{SINK} = 50 mA		0.4	0.5		0.4	0.75	V
	I_{SINK} = 100 mA		2	2.25		2	2.75	V
	I_{SINK} = 200 mA		2.5			2.5		V
	V_{CC} = 5V							
	I_{SINK} = 8 mA		0.1	0.25				V
	I_{SINK} = 5 mA					0.25	0.35	V
Output Voltage Drop (High)	I_{SOURCE} = 200 mA, V_{CC} = 15V		12.5			12.5		V
	I_{SOURCE} = 100 mA, V_{CC} = 15V	13	13.3		12.75	13.3		V
	V_{CC} = 5V	3	3.3		2.75	3.3		V
Rise Time of Output			100			100		ns
Fall Time of Output			100			100		ns
Matching Characteristics	(Note 7)							
Initial Timing Accuracy			0.05	0.2		0.1	2.0	%
Timing Drift With Temperature			±10			±10		ppm/°C
Drift With Supply Voltage			0.1	0.2		0.2	0.5	%/V

Note 1: For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of +150°C/W junction to ambient for both packages.

Note 2: Supply current when output high typically 1 mA less at V_{CC} = 5V.

Note 3: Tested at V_{CC} = 5V and V_{CC} = 15V.

Note 4: As reset voltage lowers, timing is inhibited and then the output goes low.

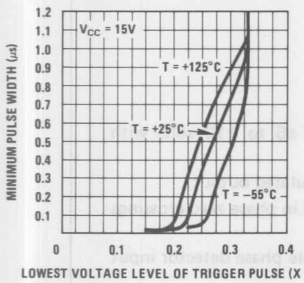
Note 5: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total ($R_A + R_B$) is 20 MΩ.

Note 6: No protection against excessive pin 1, 13 current is necessary providing the package dissipation rating will not be exceeded.

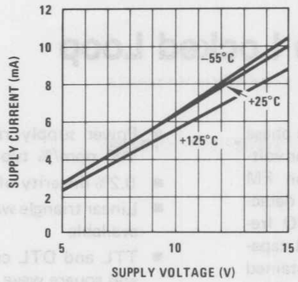
Note 7: Matching characteristics refer to the difference between performance characteristics of each timer section.

Typical Performance Characteristics

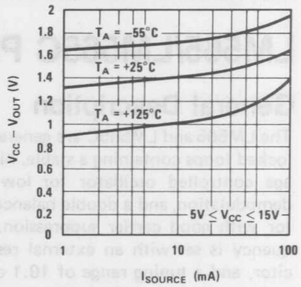
Minimum Pulse Width Required for Triggering



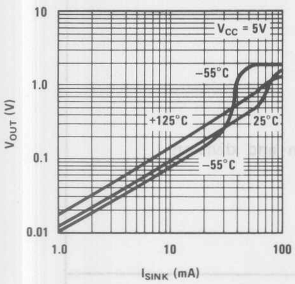
Supply Current vs Supply Voltage (Each Section)



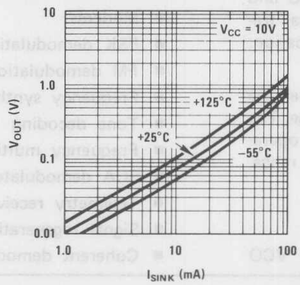
High Output Voltage vs Output Source Current



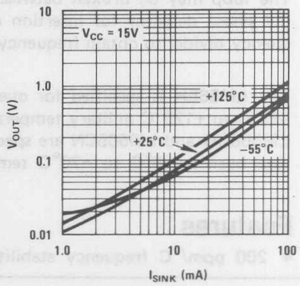
Low Output Voltage vs Output Sink Current



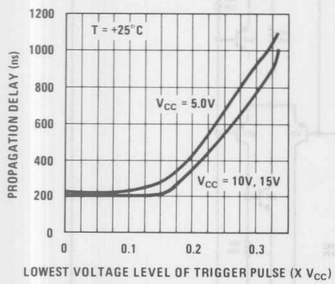
Low Output Voltage vs Output Sink Current



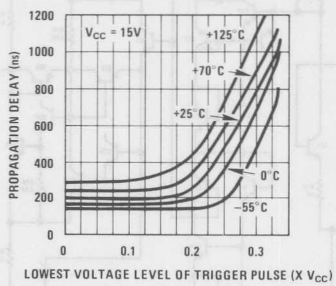
Low Output Voltage vs Output Sink Current



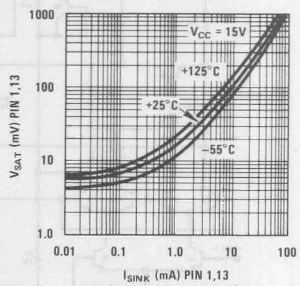
Output Propagation Delay vs Voltage Level of Trigger Pulse



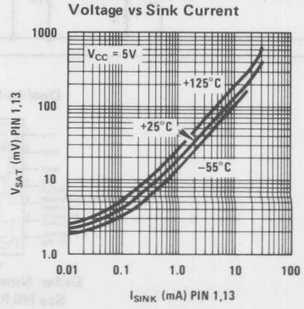
Output Propagation Delay vs Voltage Level of Trigger Pulse



Discharge Transistor (Pin 1,13) Voltage vs Sink Current



Discharge Transistor (Pin 1,13) Voltage vs Sink Current



9

National Semiconductor

Industrial Blocks

LM565/LM565C Phase Locked Loop

General Description

The LM565 and LM565C are general purpose phase locked loops containing a stable, highly linear voltage controlled oscillator for low distortion FM demodulation, and a double balanced phase detector with good carrier suppression. The VCO frequency is set with an external resistor and capacitor, and a tuning range of 10:1 can be obtained with the same capacitor. The characteristics of the closed loop system—bandwidth, response speed, capture and pull in range—may be adjusted over a wide range with an external resistor and capacitor. The loop may be broken between the VCO and the phase detector for insertion of a digital frequency divider to obtain frequency multiplication.

The LM565H is specified for operation over the −55°C to +125°C military temperature range. The LM565CH and LM565CN are specified for operation over the 0°C to +70°C temperature range.

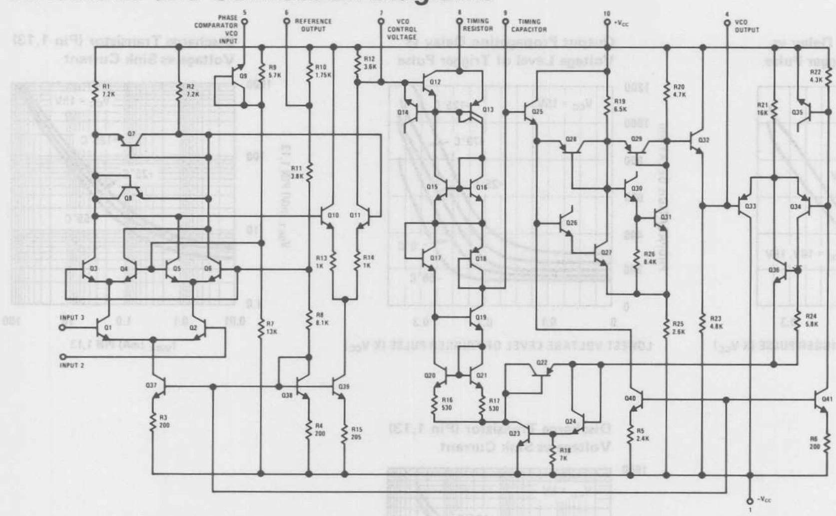
Features

- 200 ppm/°C frequency stability of the VCO
- Power supply range of ±5 to ±12 volts with 100 ppm/% typical
- 0.2% linearity of demodulated output
- Linear triangle wave with in phase zero crossings available
- TTL and DTL compatible phase detector input and square wave output
- Adjustable hold in range from ±1% to > ±60%.

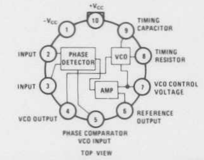
Applications

- Data and tape synchronization
- Modems
- FSK demodulation
- FM demodulation
- Frequency synthesizer
- Tone decoding
- Frequency multiplication and division
- SCA demodulators
- Telemetry receivers
- Signal regeneration
- Coherent demodulators.

Schematic and Connection Diagrams

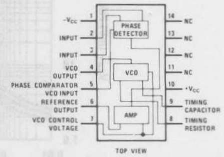


Metal Can Package



Order Number LM565H or LM565CH
See NS Package H10C

Dual-In-Line Package



Order Number LM565CN
See NS Package N14A

Absolute Maximum Ratings

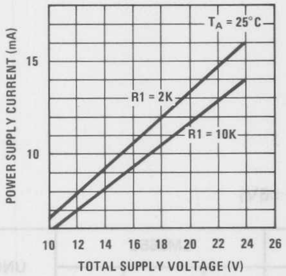
Supply Voltage		±12V
Power Dissipation (Note 1)		300 mW
Differential Input Voltage		±1V
Operating Temperature Range	LM565H	−55°C to +125°C
	LM565CH, LM565CN	0°C to 70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

Electrical Characteristics (AC Test Circuit, $T_A = 25°C$, $V_C = \pm 6V$)

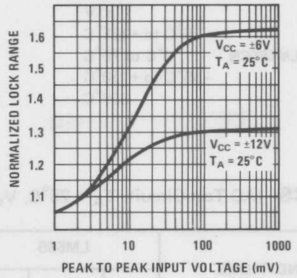
PARAMETER	CONDITIONS	LM565			LM565C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Power Supply Current			8.0	12.5		8.0	12.5	mA
Input Impedance (Pins 2, 3)	$-4V < V_2, V_3 < 0V$	7	10			5		kΩ
VCO Maximum Operating Frequency	$C_o = 2.7$ pF	300	500		250	500		kHz
Operating Frequency Temperature Coefficient			−100	300		−200	500	ppm/°C
Frequency Drift with Supply Voltage			0.01	0.1		0.05	0.2	%/V
Triangle Wave Output Voltage		2	2.4	3	2	2.4	3	$V_{p\text{-}p}$
Triangle Wave Output Linearity			0.2	0.75		0.5	1	%
Square Wave Output Level		4.7	5.4		4.7	5.4		$V_{p\text{-}p}$
Output Impedance (Pin 4)			5			5		kΩ
Square Wave Duty Cycle		45	50	55	40	50	60	%
Square Wave Rise Time			20	100		20		ns
Square Wave Fall Time			50	200		50		ns
Output Current Sink (Pin 4)		0.6	1		0.6	1		mA
VCO Sensitivity	$f_o = 10$ kHz	6400	6600	6800	6000	6600	7200	Hz/V
Demodulated Output Voltage (Pin 7)	±10% Frequency Deviation	250	300	350	200	300	400	mV_{pp}
Total Harmonic Distortion	±10% Frequency Deviation		0.2	0.75		0.2	1.5	%
Output Impedance (Pin 7)			3.5			3.5		kΩ
DC Level (Pin 7)		4.25	4.5	4.75	4.0	4.5	5.0	V
Output Offset Voltage $\lvert V_7 - V_6 \rvert$			30	100		50	200	mV
Temperature Drift of $\lvert V_7 - V_6 \rvert$			500			500		µV/°C
AM Rejection		30	40			40		dB
Phase Detector Sensitivity K_D		0.6	.68	0.9	0.55	.68	0.95	V/radian

Note 1: The maximum junction temperature of the LM565 is 150°C, while that of the LM565C and LM565CN is 100°C. For operation at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W junction to ambient or 45°C/W junction to case. Thermal resistance of the dual-in-line package is 100°C/W.

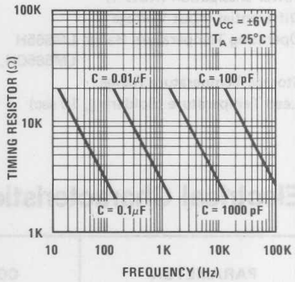
Power Supply Current as a Function of Supply Voltage



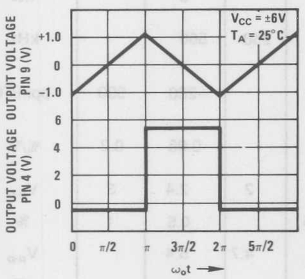
Lock Range as a Function of Input Voltage



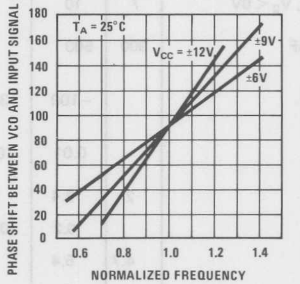
VCO Frequency



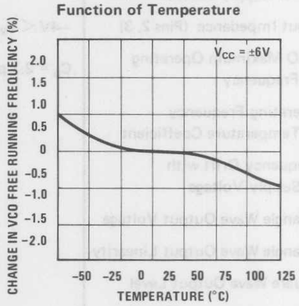
Oscillator Output Waveforms



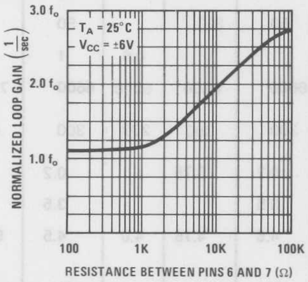
Phase Shift vs Frequency



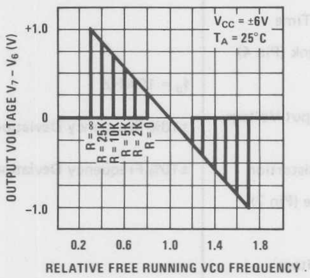
VCO Frequency as a Function of Temperature



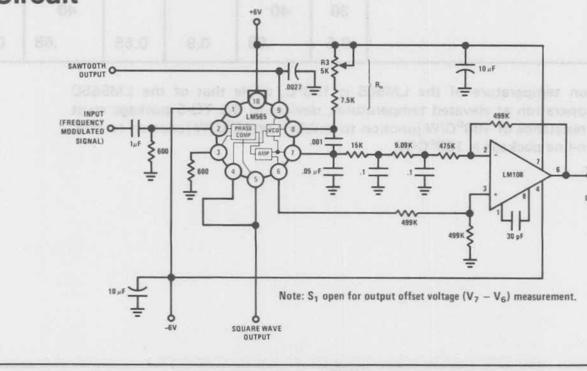
Loop Gain vs Load Resistance



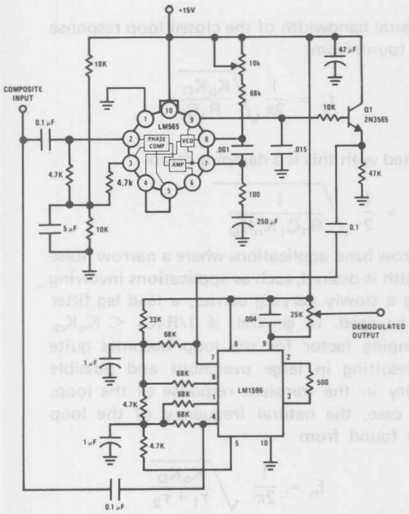
Hold in Range as a Function of R_{6-7}



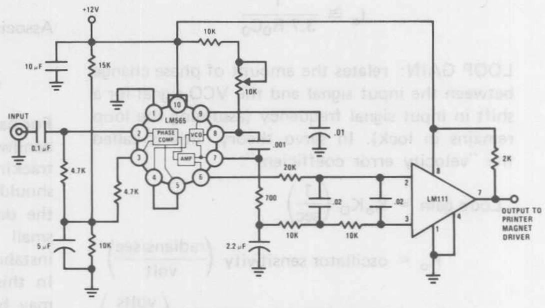
AC Test Circuit



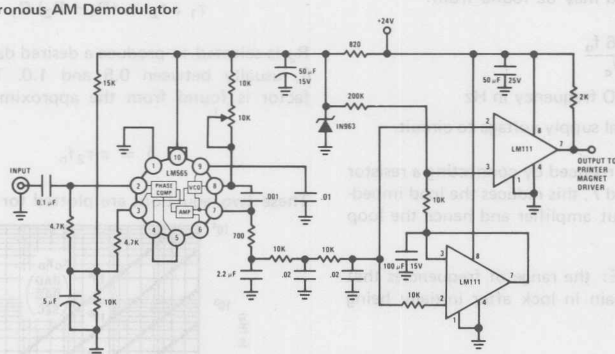
Typical Applications



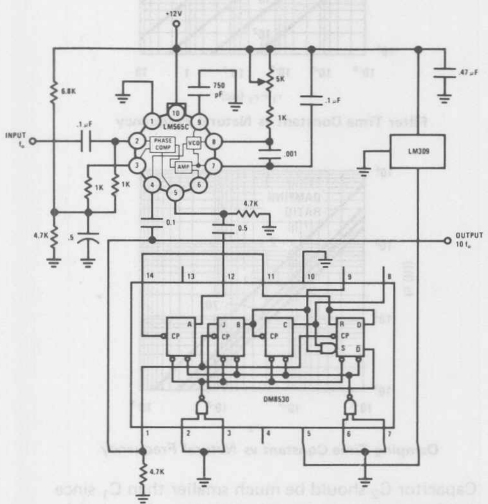
2400 Hz Synchronous AM Demodulator



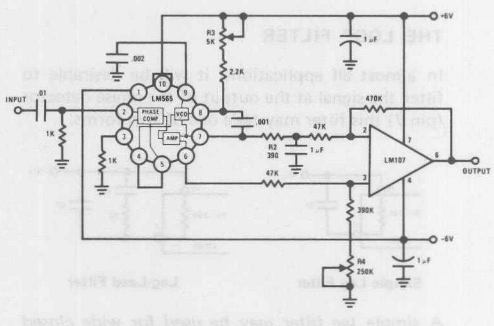
FSK Demodulator (2025-2225 cps)



FSK Demodulator with DC Restoration.



Frequency Multiplier (x10)



IRIG Channel 13 Demodulator

Applications Information

In designing with phase locked loops such as the LM565, the important parameters of interest are:

FREE RUNNING FREQUENCY

$$f_o \cong \frac{1}{3.7\ R_0 C_0}$$

LOOP GAIN: relates the amount of phase change between the input signal and the VCO signal for a shift in input signal frequency (assuming the loop remains in lock). In servo theory, this is called the "velocity error coefficient".

$$\text{Loop gain} = K_o K_D \left(\frac{1}{\text{sec}}\right)$$

$$K_o = \text{oscillator sensitivity} \left(\frac{\text{radians/sec}}{\text{volt}}\right)$$

$$K_D = \text{phase detector sensitivity} \left(\frac{\text{volts}}{\text{radian}}\right)$$

The loop gain of the LM565 is dependent on supply voltage, and may be found from:

$$K_o K_D = \frac{33.6\ f_o}{V_c}$$

f_o = VCO frequency in Hz

V_c = total supply voltage to circuit.

Loop gain may be reduced by connecting a resistor between pins 6 and 7; this reduces the load impedance on the output amplifier and hence the loop gain.

HOLD IN RANGE: the range of frequencies that the loop will remain in lock after initially being locked.

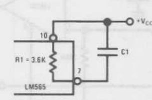
$$f_H = \pm \frac{8\ f_o}{V_c}$$

f_o = free running frequency of VCO

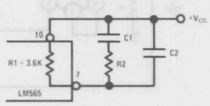
V_c = total supply voltage to the circuit.

THE LOOP FILTER

In almost all applications, it will be desirable to filter the signal at the output of the phase detector (pin 7) this filter may take one of two forms:



Simple Lag Filter



Lag-Lead Filter

A simple lag filter may be used for wide closed loop bandwidth applications such as modulation following where the frequency deviation of the carrier is fairly high (greater than 10%), or where wideband modulating signals must be followed.

The natural bandwidth of the closed loop response may be found from:

$$f_n = \frac{1}{2\pi}\sqrt{\frac{K_o K_D}{R_1 C_1}}$$

Associated with this is a damping factor:

$$\delta = \frac{1}{2}\sqrt{\frac{1}{R_1 C_1 K_o K_D}}$$

For narrow band applications where a narrow noise bandwidth is desired, such as applications involving tracking a slowly varying carrier, a lead lag filter should be used. In general, if $1/R_1C_1 < K_oK_d$, the damping factor for the loop becomes quite small resulting in large overshoot and possible instability in the transient response of the loop. In this case, the natural frequency of the loop may be found from

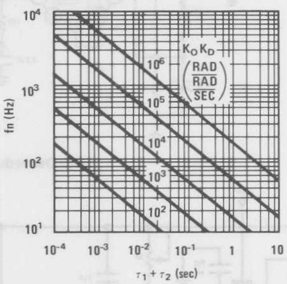
$$f_n = \frac{1}{2\pi}\sqrt{\frac{K_o K_D}{\tau_1 + \tau_2}}$$

$$\tau_1 + \tau_2 = (R_1 + R_2)\ C_1$$

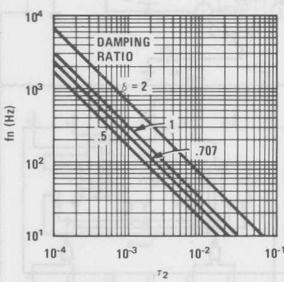
R_2 is selected to produce a desired damping factor δ, usually between 0.5 and 1.0. The damping factor is found from the approximation:

$$\delta \simeq \pi \tau_2 f_n$$

These two equations are plotted for convenience.



Filter Time Constant vs Natural Frequency



Damping Time Constant vs Natural Frequency

Capacitor C_2 should be much smaller than C_1 since its function is to provide filtering of carrier. In general $C_2 \leq 0.1\ C_1$.

National Semiconductor

Industrial Blocks

LM566/LM566C Voltage Controlled Oscillator

General Description

The LM566/LM566C are general purpose voltage controlled oscillators which may be used to generate square and triangular waves, the frequency of which is a very linear function of a control voltage. The frequency is also a function of an external resistor and capacitor.

The LM566 is specified for operation over the $-55^{\circ}C$ to $+125^{\circ}C$ military temperature range. The LM566C is specified for operation over the $0^{\circ}C$ to $+70^{\circ}C$ temperature range.

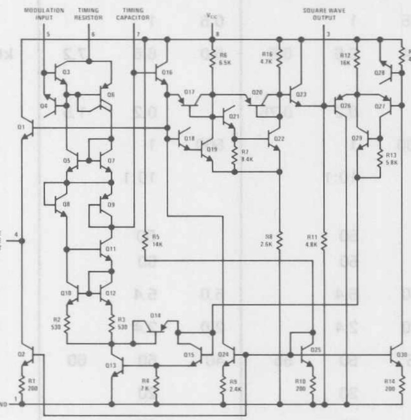
Features

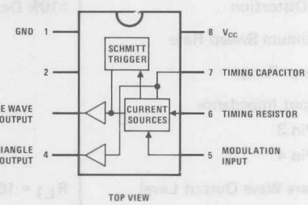
- Wide supply voltage range: 10 to 24 volts
- Very linear modulation characteristics
- High temperature stability
- Excellent supply voltage rejection
- 10 to 1 frequency range with fixed capacitor
- Frequency programmable by means of current, voltage, resistor or capacitor.

Applications

- FM modulation
- Signal generation
- Function generation
- Frequency shift keying
- Tone generation

Schematic and Connection Diagrams

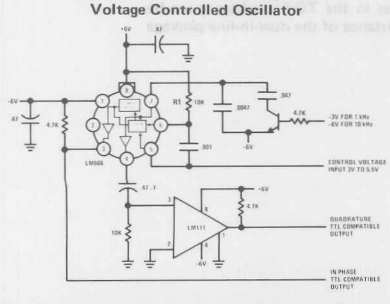




Order Number LM566CN
See NS Package N08B

Typical Application

1 kHz and 10 kHz TTL Compatible Voltage Controlled Oscillator



Applications Information

The LM566 may be operated from either a single supply as shown in this test circuit, or from a split (±) power supply. When operating from a split supply, the square wave output (pin 4) is TTL compatible (2 mA current sink) with the addition of a 4.7 kΩ resistor from pin 3 to ground.

A .001 μF capacitor is connected between pins 5 and 6 to prevent parasitic oscillations that may occur during VCO switching.

$$f_O = \frac{2(V^+ - V_5)}{R_1 C_1 V^+}$$

where

$2K < R_1 < 20K$

and V_5 is voltage between pin 5 and pin 1

Power Supply Voltage		26V
Power Dissipation (Note 1)		300 mW
Operating Temperature Range	LM566	-55°C to +125°C
	LM566C	0°C to 70°C
Lead Temperature (Soldering, 10 sec)		300°C

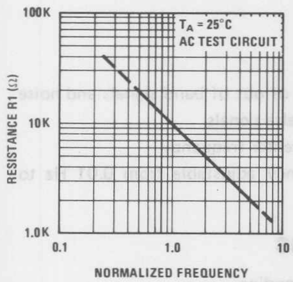
Electrical Characteristics V_{CC} = 12V, T_A = 25°C, AC Test Circuit

PARAMETER	CONDITIONS	LM566			LM566C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Maximum Operating Frequency	R0 = 2k C0 = 2.7 pF		1			1		MHz
Input Voltage Range Pin 5		3/4 V_{CC}		V_{CC}	3/4 V_{CC}		V_{CC}	
Average Temperature Coefficient of Operating Frequency			100			200		ppm/°C
Supply Voltage Rejection	10–20V		0.1	1		0.1	2	%/V
Input Impedance Pin 5		0.5	1		0.5	1		MΩ
VCO Sensitivity	For Pin 5, From 8–10V, f_O = 10 kHz	6.4	6.6	6.8	6.0	6.6	7.2	kHz/V
FM Distortion	±10% Deviation		0.2	0.75		0.2	1.5	%
Maximum Sweep Rate		800	1		500	1		MHz
Sweep Range			10:1			10:1		
Output Impedance								
Pin 3			50			50		Ω
Pin 4			50			50		Ω
Square Wave Output Level	R_{L1} = 10k	5.0	5.4		5.0	5.4		Vp-p
Triangle Wave Output Level	R_{L2} = 10k	2.0	2.4		2.0	2.4		Vp-p
Square Wave Duty Cycle		45	50	55	40	50	60	%
Square Wave Rise Time			20			20		ns
Square Wave Fall Time			50			50		ns
Triangle Wave Linearity	+1V Segment at 1/2 V_{CC}		0.2	0.75		0.5	1	%

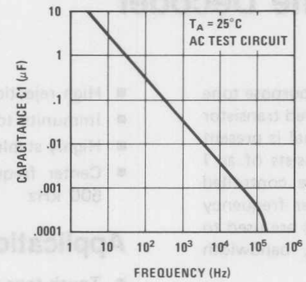
Note 1: The maximum junction temperature of the LM566 is 150°C, while that of the LM566C is 100°C. For operating at elevated junction temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W. The thermal resistance of the dual-in-line package is 100°C/W.

Typical Performance Characteristics

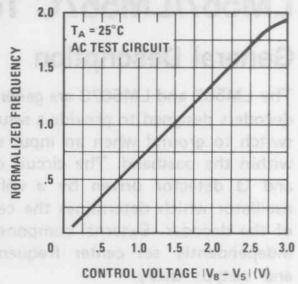
Operating Frequency as a Function of Timing Resistor



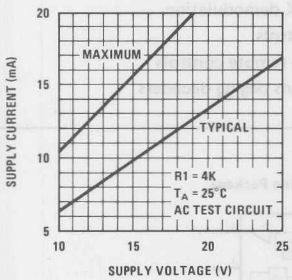
Operating Frequency as a Function of Timing Capacitor



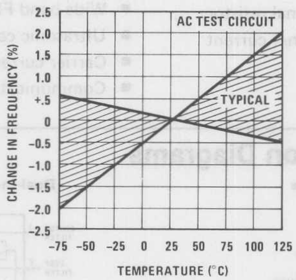
Normalized Frequency as a Function of Control Voltage



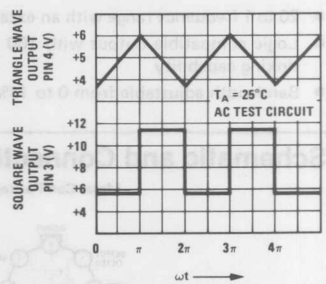
Power Supply Current



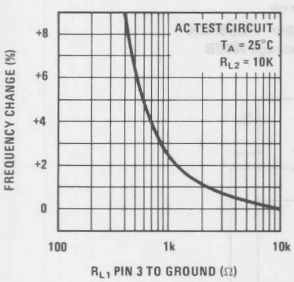
Temperature Stability



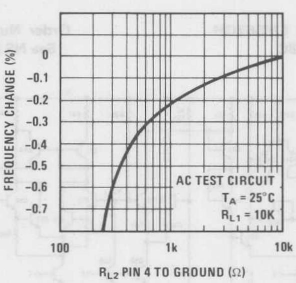
VCO Waveforms



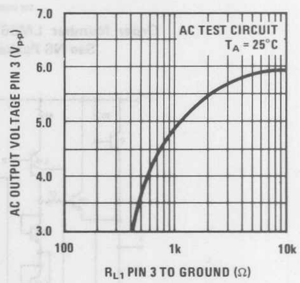
Frequency Stability vs Load Resistance (Square Wave Output)



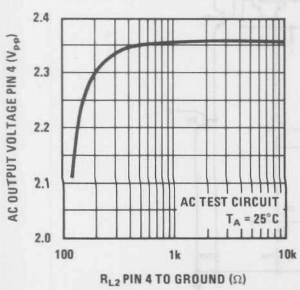
Frequency Stability vs Load Impedance (Triangle Output)



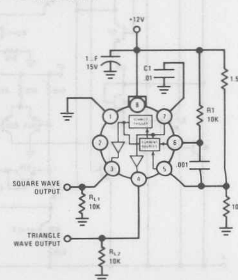
Square Wave Output Characteristics



Triangle Wave Output Characteristics



AC Test Circuit



National Semiconductor

Industrial Blocks

LM567/LM567C Tone Decoder

General Description

The LM567 and LM567C are general purpose tone decoders designed to provide a saturated transistor switch to ground when an input signal is present within the passband. The circuit consists of an I and Q detector driven by a voltage controlled oscillator which determines the center frequency of the decoder. External components are used to independently set center frequency, bandwidth and output delay.

Features

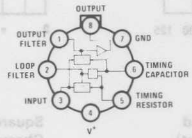
- 20 to 1 frequency range with an external resistor
- Logic compatible output with 100 mA current sinking capability
- Bandwidth adjustable from 0 to 14%
- High rejection of out of band signals and noise
- Immunity to false signals
- Highly stable center frequency
- Center frequency adjustable from 0.01 Hz to 500 kHz

Applications

- Touch tone decoding
- Precision oscillator
- Frequency monitoring and control
- Wide band FSK demodulation
- Ultrasonic controls
- Carrier current remote controls
- Communications paging decoders

Schematic and Connection Diagrams

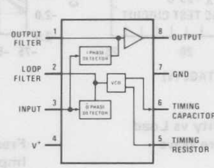
Metal Can Package



TOP VIEW

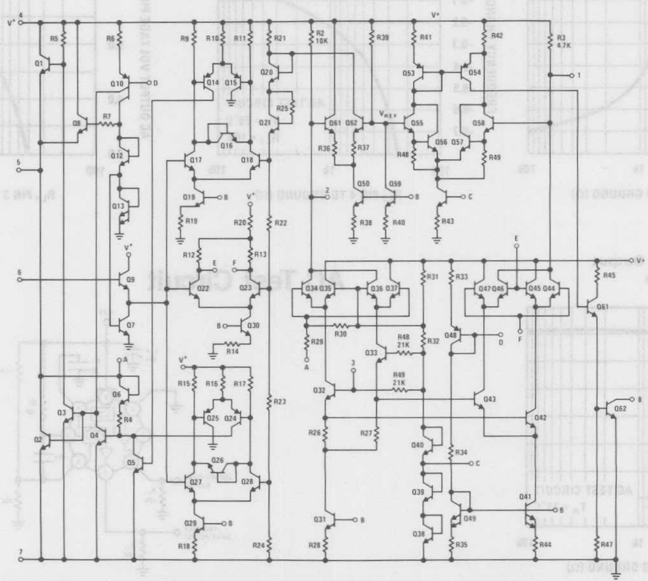
Order Number LM567H or LM567CH
See NS Package H08C

Dual-In-Line Package



TOP VIEW

Order Number LM567CN
See NS Package N08B



Absolute Maximum Ratings

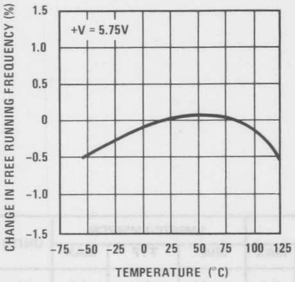
Supply Voltage Pin	10V
Power Dissipation (Note 1)	300 mW
V_8	15V
V_3	−10V
V_3	V_8 + 0.5V
Storage Temperature Range	−65°C to +150°C

Electrical Characteristics (AC Test Circuit, T_A = 25°C, V_C = 5V)

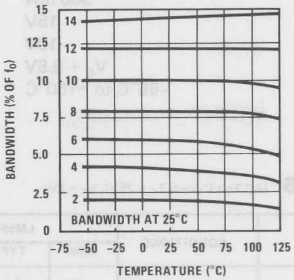
PARAMETERS	CONDITIONS	LM567			LM567C/LM567CN			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Power Supply Voltage Range		4.75	5.0	9.0	4.75	5.0	9.0	V
Power Supply Current Quiescent	R_L = 20k		6	8		7	10	mA
Power Supply Current Activated	R_L = 20k		11	13		12	15	mA
Input Resistance		18	20	22	15	20	25	kΩ
Smallest Detectable Input Voltage	I_L = 100 mA, $f_i = f_o$		20	25		20	25	mVrms
Largest No Output Input Voltage	I_C = 100 mA, $f_i = f_o$	10	15		10	15		mVrms
Largest Simultaneous Outband Signal to Inband Signal Ratio			6			6		dB
Minimum Input Signal to Wideband Noise Ratio	B_n = 140 kHz		−6			−6		dB
Largest Detection Bandwidth		12	14	16	10	14	18	% of f_o
Largest Detection Bandwidth Skew			1	2		2	3	% of f_o
Largest Detection Bandwidth Variation with Temperature			±0.1	0.25		±0.1	0.5	%/°C
Largest Detection Bandwidth Variation with Supply Voltage	4.75V – 6.75V		±1	±2		±1	±5	%V
Highest Center Frequency		100	500		100	500		kHz
Center Frequency Stability	$0 < T_A < 70$		35 ± 60			35 ± 60		ppm/°C
	$-55 < T_A < +125$		35 ± 140			35 ± 140		ppm/°C
Center Frequency Shift with Supply Voltage	4.75V – 6.75V		0.5	1.0		0.4	2.0	%/V
Fastest ON-OFF Cycling Rate			f_o/20			f_o/20		
Output Leakage Current	V_8 = 15V		0.01	25		0.01	25	μA
Output Saturation Voltage	e_i = 25 mV, I_8 = 30 mA		0.2	0.4		0.2	0.4	V
	e_i = 25 mV, I_8 = 100 mA		0.6	1.0		0.6	1.0	
Output Fall Time			30			30		ns
Output Rise Time			150			150		ns

Note 1: The maximum junction temperature of the LM567 is 150°C, while that of the LM567C and LM567CN is 100°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient or 45°C/W, junction to case. For the DIP the device must be derated based on a thermal resistance of 187°C/W, junction to ambient.

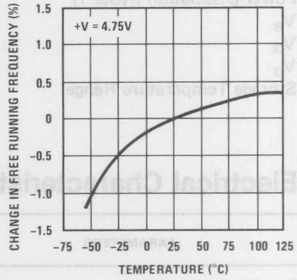
Typical Frequency Drift with Temperature (Mean and S.D.)



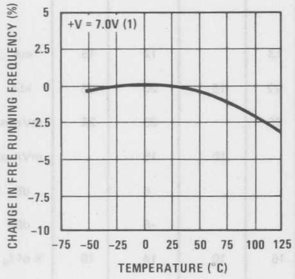
Typical Bandwidth Variation with Temperature



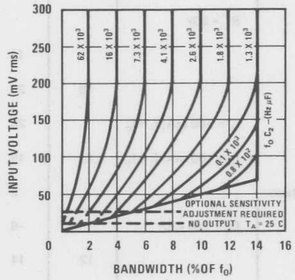
Typical Frequency Drift with (Mean and S.D.) Temperature



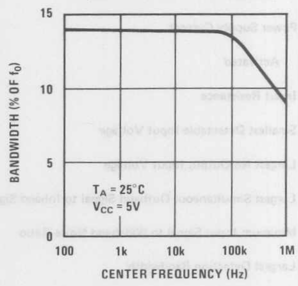
Typical Frequency Drift with Temperature (Mean and S.D.)



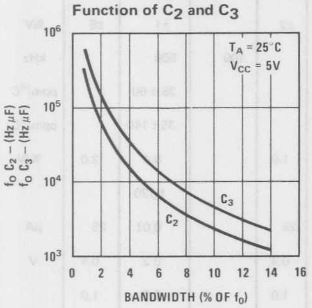
Bandwidth vs Input Signal Amplitude



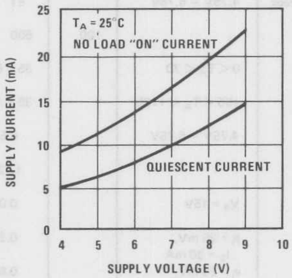
Largest Detection Bandwidth



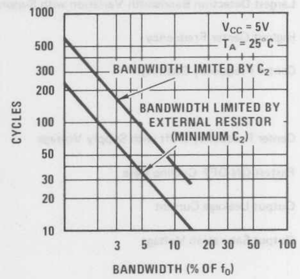
Detection Bandwidth as a Function of C_2 and C_3



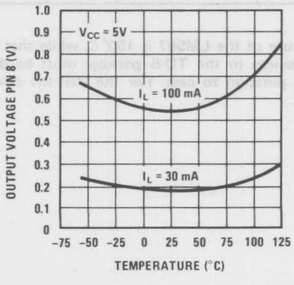
Typical Supply Current vs Supply Voltage



Greatest Number of Cycles Before Output

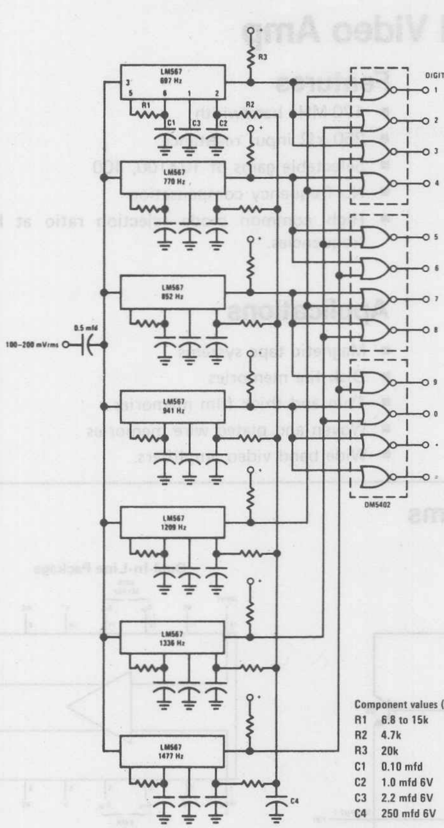


Typical Output Voltage vs Temperature



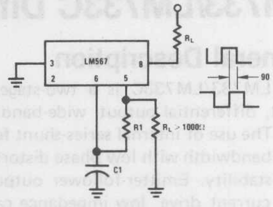
Typical Applications

Touch-Tone Decoder



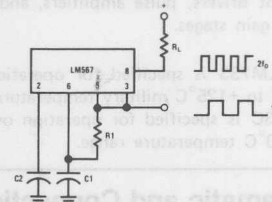
Component values (typ)		
R1	6.8 to 15k	
R2	4.7k	
R3	20k	
C1	0.10 mfd	
C2	1.0 mfd 6V	
C3	2.2 mfd 6V	
C4	250 mfd 6V	

Oscillator with Quadrature Output

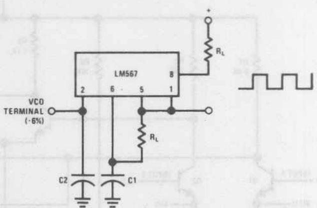


Connect pin 3 to 2.8V to invert output.

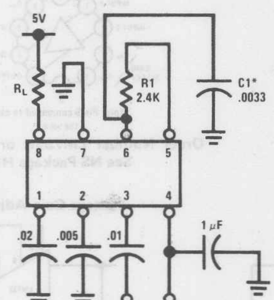
Oscillator with Double Frequency Output



Precision Oscillator Drive 100 mA Loads



AC Test Circuit



f_i = 100 kHz +5V
*Note: Adjust for f_o = 100 kHz.

Applications Information

The center frequency of the tone decoder is equal to the free running frequency of the VCO. This is given by

$$f_o \cong \frac{1}{1.1 R_1 C_1}$$

The bandwidth of the filter may be found from the approximation

$$BW = 1070 \sqrt{\frac{V_i}{f_o C_2}} \quad \text{in \% of } f_o$$

Where:

V_i = Input voltage (volts rms), $V_i \leq 200$ mV

C_2 = Capacitance at Pin 2 (μF)

National Semiconductor

Industrial Blocks

LM733/LM733C Differential Video Amp

General Description

The LM733/LM733C is a two-stage, differential input, differential output, wide-band video amplifier. The use of internal series-shunt feedback gives wide bandwidth with low phase distortion and high gain stability. Emitter-follower outputs provide a high current drive, low impedance capability. It's 120 MHz bandwidth and selectable gains of 10, 100, and 400, without need for frequency compensation, make it a very useful circuit for memory element drivers, pulse amplifiers, and wide band linear gain stages.

The LM733 is specified for operation over the −55°C to +125°C military temperature range. The LM733C is specified for operation over the 0°C to +70°C temperature range.

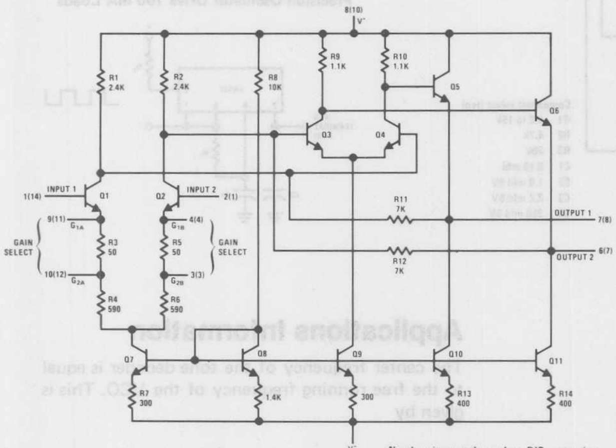
Features

- 120 MHz bandwidth
- 250 kΩ input resistance
- Selectable gains of 10, 100, 400
- No frequency compensation
- High common mode rejection ratio at high frequencies.

Applications

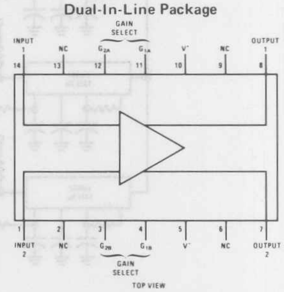
- Magnetic tape systems
- Disk file memories
- Thin and thick film memories
- Woven and plated wire memories
- Wide band video amplifiers.

Schematic and Connection Diagrams



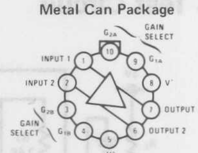
Numbers in parentheses show DIP connections.

Dual-In-Line Package



Order Number LM733CN
See NS Package N14A

Metal Can Package

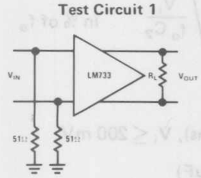


Note: Pin 5 connected to case.
TOP VIEW

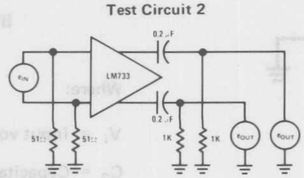
Order Number LM733H or LM733CH
See NS Package H10D

Test Circuits

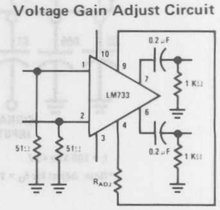
Test Circuit 1



Test Circuit 2



Voltage Gain Adjust Circuit



$V_S = 6V$, $T_A = 25°C$
(Pin numbers apply to TO-5 package)

Absolute Maximum Ratings

Differential Input Voltage	±5V
Common Mode Input Voltage	±6V
V_{CC}	±8V
Output Current	10 mA
Power Dissipation (Note 1)	500 mW
Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range LM733	−55°C to +125°C
LM733C	0°C to +70°C
Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics (T_A = 25°C, unless otherwise specified, see test circuits, V_S = ±6.0V)

CHARACTERISTICS	TEST CIRCUIT	TEST CONDITIONS	LM733			LM733C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Differential Voltage Gain									
Gain 1 (Note 2)			300	400	500	250	400	600	
Gain 2 (Note 3)	1	R_L = 2 kΩ V_{OUT} = 3 $V_{p\text{-}p}$	90	100	110	80	100	120	
Gain 3 (Note 4)			9.0	10	11	8.0	10	12	
Bandwidth									
Gain 1				40			40		MHz
Gain 2	2			90			90		MHz
Gain 3				120			120		MHz
Rise Time									
Gain 1		V_{OUT} = 1 $V_{p\text{-}p}$		10.5			10.5		ns
Gain 2	2			4.5	10		4.5	12	ns
Gain 3				2.5			2.5		ns
Propagation Delay		V_{OUT} = 1 $V_{p\text{-}p}$							
Gain 1				7.5			7.5		ns
Gain 2	2			6.0	10		6.0	10	ns
Gain 3				3.6			3.6		ns
Input Resistance									
Gain 1				4.0			4.0		kΩ
Gain 2			20	30		10	30		kΩ
Gain 3				250			250		kΩ
Input Capacitance		Gain 2		2.0			2.0		pF
Input Offset Current				0.4	3.0		0.4	5.0	μA
Input Bias Current				9.0	20		9.0	30	μA
Input Noise Voltage		BW = 1 kHz to 10 MHz		12			12		μVrms
Input Voltage Range	1		±1.0			±1.0			V
Common Mode Rejection Ratio									
Gain 2	1	V_{CM} = ±1V f ≤ 100 kHz	60	86		60	86		dB
Gain 2		V_{CM} = ±1V f = 5 MHz		60			60		dB
Supply Voltage Rejection Ratio									
Gain 2	1	ΔV_S = ±0.5V	50	70		50	70		dB
Output Offset Voltage									
Gain 1	1	R_L = ∞		0.6	1.5		0.6	1.5	V
Gain 2 and 3				0.35	1.0		0.35	1.5	V
Output Common Mode Voltage	1	R_L = ∞	2.4	2.9	3.4	2.4	2.9	3.4	V
Output Voltage Swing	1	R_L = 2k	3.0	4.0		3.0	4.0		
Output Sink Current			2.5	3.6		2.5	3.6		mA
Output Resistance				20			20		Ω
Power Supply Current	1	R_L = ∞		18	24		18	24	mA

Differential Voltage Gain									
Gain 1			200		600	250		600	
Gain 2	1	$R_L = 2\ k\Omega$, $V_{OUT} = 3\ V_{P\text{-}P}$	80		120	80		120	
Gain 3			8.0		12.0	8.0		12.0	
Input Resistance Gain 2			8			8			kΩ
Input Offset Current					5			6	μA
Input Bias Current					40			40	μA
Input Voltage Range	1		±1			±1			V
Common Mode Rejection Ratio									
Gain 2	1	$V_{CM} = \pm1V$, $f \leq 100\ kHz$	50			50			dB
Supply Voltage Rejection Ratio									
Gain 2	1	$\Delta V_S = \pm0.5V$	50			50			dB
Output Offset Voltage									
Gain 1	1	$R_L = \infty$			1.5			1.5	V
Gain 2 and 3					1.2			1.5	V
Output Voltage Swing	1	$R_L = 2k$	2.5			2.8			V_{PP}
Output Sink Current			2.2			2.5			mA
Power Supply Current	1	$R_L = \infty$			27			27	mA

Note 1: The maximum junction temperature of the LM733 is 150°C, while that of the LM733C is 100°C. For operation at elevated temperatures devices in the TO-100 package must be derated based on a thermal resistance of 150°C/W junction to ambient or 45°C/W junction to case. Thermal resistance of the dual-in-line package is 100°C/W.

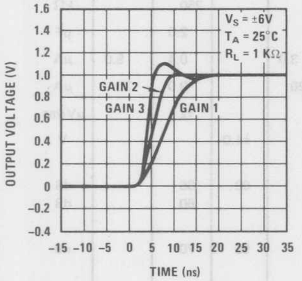
Note 2: Pins G1A and G1B connected together.

Note 3: Pins G2A and G2B connected together.

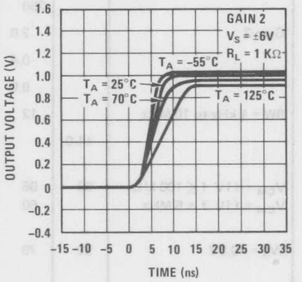
Note 4: Gain select pins open.

Typical Performance Characteristics

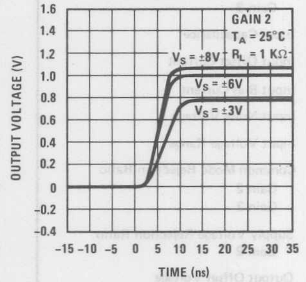
Pulse Response



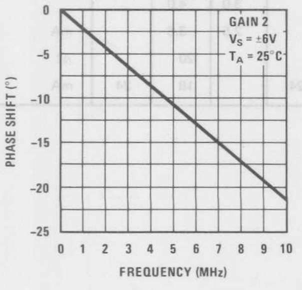
Pulse Response vs Temperature



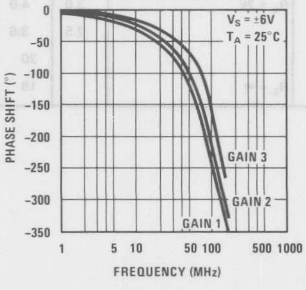
Pulse Response vs Supply Voltage



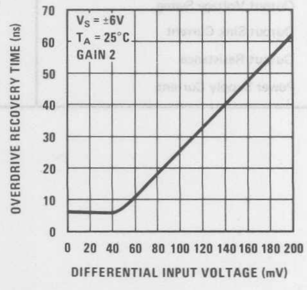
Phase Shift vs Frequency



Phase Shift vs Frequency

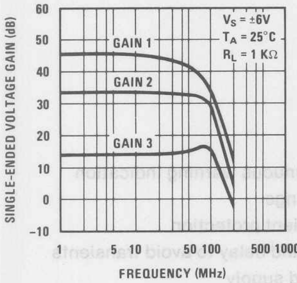


Differential Overdrive Recovery Time

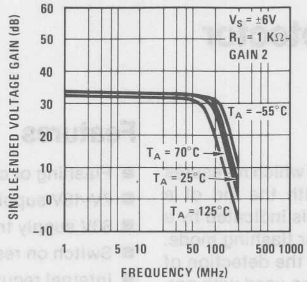


Typical Performance Characteristics (Continued)

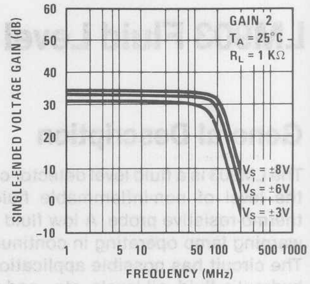
Voltage Gain vs Frequency



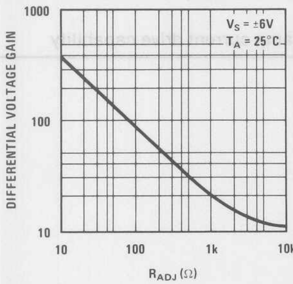
Gain vs Frequency Temperature



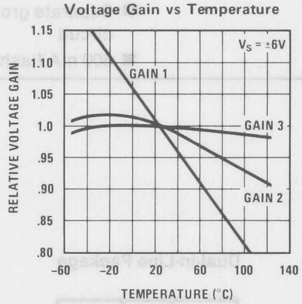
Gain vs Frequency vs Supply Voltage



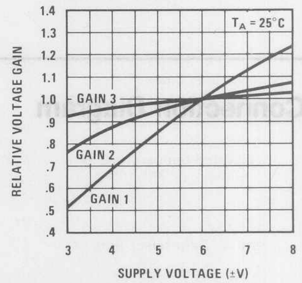
Voltage Gain vs R_{ADJ}



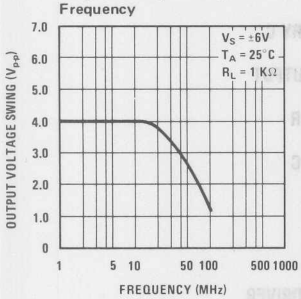
Voltage Gain vs Temperature



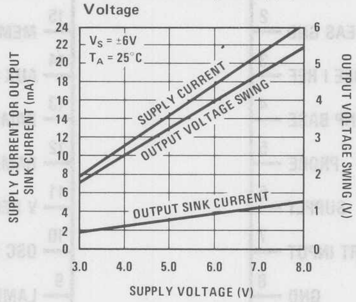
Voltage Gain vs Supply Voltage



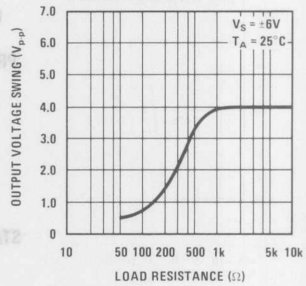
Output Voltage Swing vs Frequency



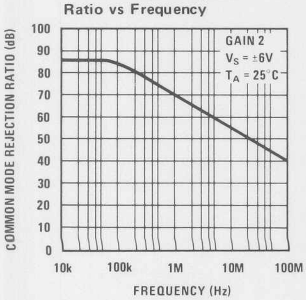
Supply Current, Output Voltage and Current Swing vs Supply Voltage



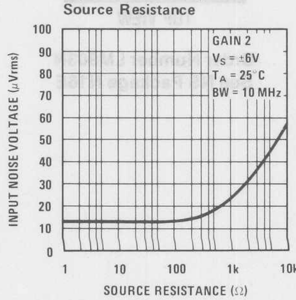
Output Voltage Swing vs Load Resistance



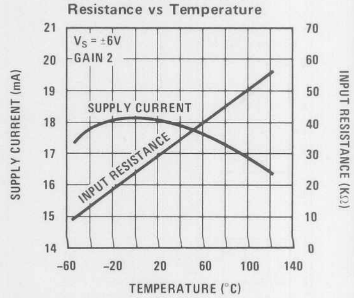
Common Mode Rejection Ratio vs Frequency



Input Noise Voltage vs Source Resistance



Supply Current and Input Resistance vs Temperature



National Semiconductor

LM903 Fluid Level Detector

General Description

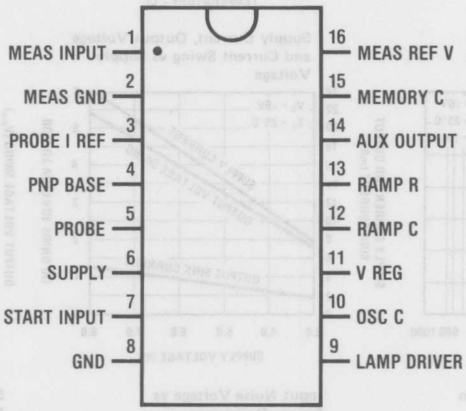
The LM903 is a fluid level detector circuit which measures the level of non-inflammable fluids with the aid of a thermo-resistive probe. A low fluid level is indicated by a warning lamp operating in continuous or flashing mode. The circuit has possible applications in the detection of hydraulic fluid, oil levels, etc., and may be used with partially conducting fluids.

Features

- Flashing or continuous warning indication
- 7V–18V supply range
- 80V supply transient protection
- Switch on reset and delay to avoid transients
- Internal regulated supply
- Warning threshold externally adjustable
- Short and open circuit probe detection
- Separate ground pins for lamp drive and measurement circuit
- 600 mA flashing lamp current drive capability

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number LM903N
See NS Package N16E

Absolute Maximum Ratings

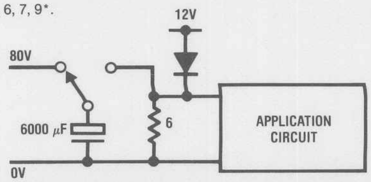
Supply Voltage, V6	18V	Operating Temperature Range	−40°C to +80°C
Start Input, V7	18V	Storage Temperature Range	−40°C to +150°C
Probe Current Reference, V3	18V	Maximum Junction Temperature	150°C
Pulse Voltage to Pins 3, 6, 7, 9 (Note 1)	80V −10 ms	Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

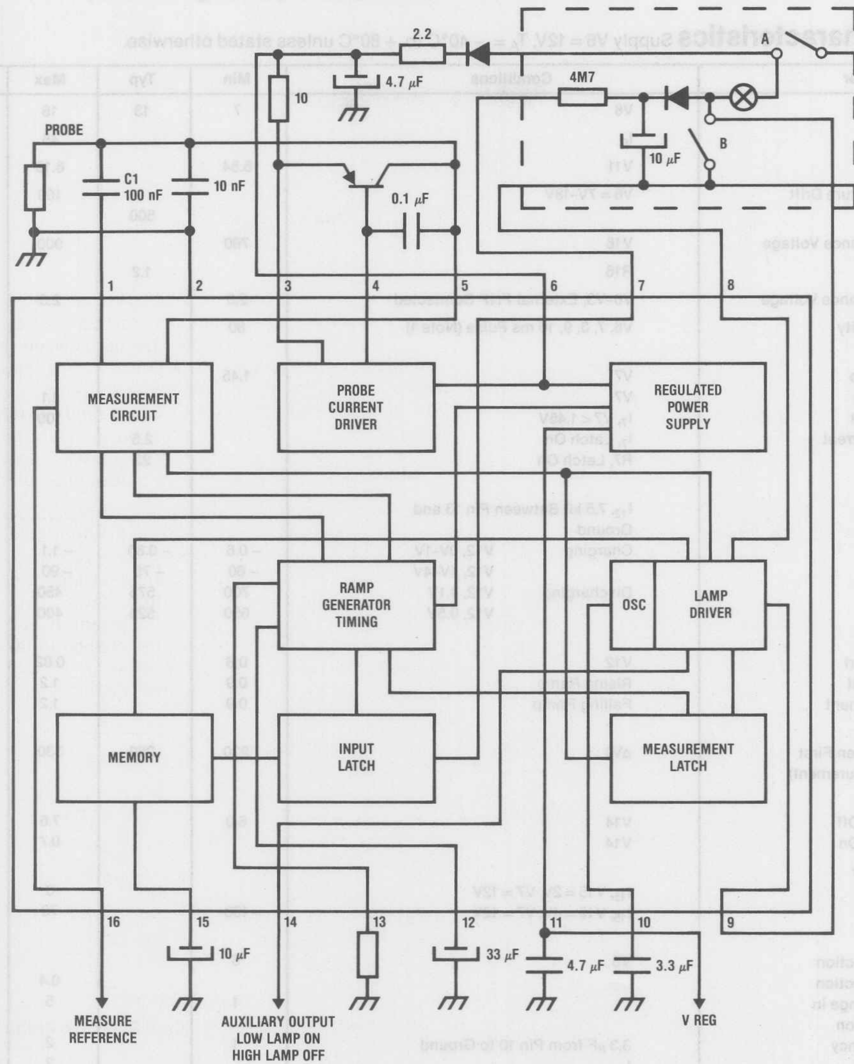
Supply V6 = 12V, T_A = −40°C to +80°C unless stated otherwise.

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage	V6	7	13	18	V
Supply Current	I_6			45	mA
Regulated Voltage	V11	5.54		6.15	V
Regulation Temperature Drift	V6 = 7V–18V			100	mV
			500		μV/°C
Measurement Reference Voltage	V16	790		900	mV
Input Resistance	R16		1.2		kΩ
Probe Current Reference Voltage	V6-V3, External PNP Connected	2.0		2.3	V
Overvoltage Capability	V6, 7, 3, 9, 10 ms Pulse (Note 1)	80			V
Starting Latch					
High Input Voltage	V7	1.45			V
Low Input Voltage	V7			1.1	V
High Input Current	I_7, V7 < 1.45V			100	nA
Latch Holding Current	I_7, Latch On		2.5		mA
R_{IN}	R7, Latch On		22		kΩ
Ramp					
Ramp Current	I_{12}, 7.5 kΩ Between Pin 13 and Ground				
	Charging V12, 0V–1V	−0.6	−0.85	−1.1	mA
	V12, 1V–4V	−60	−75	−90	μA
	Discharging V12, 4.1V	700	575	450	μA
	V12, 0.5V	650	525	400	μA
Ramp Thresholds					
Probe Current Start	V12	0.6		0.82	V
First Measurement	Rising Ramp	0.9		1.2	V
Second Measurement	Falling Ramp	0.9		1.2	V
Alarm Level (Difference Between First and Second Measurement)	ΔV1	230	280	330	mV
Auxiliary Output					
Output for Lamp Off	V14	6.0		7.6	V
Output for Lamp On	V14			0.7	V
Memory Comparator					
Leakage Current	I_{15}, V15 = 2V, V7 = 12V			3	μA
Charging Current	I_{15}, V15 = 4V, V7 = 12V	−130		−70	μA
Probe Voltages					
Open Circuit Detection	V5	6			V
Short Circuit Detection				0.4	V
Probe Voltage Range in Normal Operation		1		5	V
Oscillator Frequency	3.3 μF from Pin 10 to Ground	1		2	Hz
Pin 1 Leakage	I_1			3	nA
Pin 1 External Capacitor			0.1		μF
Lamp Driver					
Saturation Resistance	R9		2		Ω
Maximum Current	Flashing Mode			600	mA

Note 1: Test circuit for overvoltage capability pins 3, 6, 7, 9*.



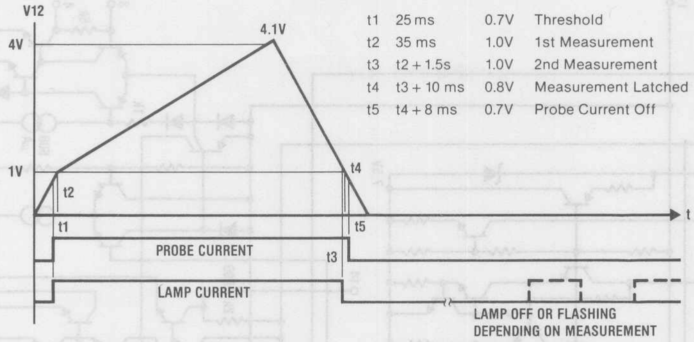
*In lamp on condition, I_9 must be limited to less than 2A.



Memory capacitor on pin 15 is set
High — Lamp off
Low — Lamp on

Circuit Timing Diagram

t1	25 ms	0.7V	Threshold
t2	35 ms	1.0V	1st Measurement
t3	t2 + 1.5s	1.0V	2nd Measurement
t4	t3 + 10 ms	0.8V	Measurement Latched
t5	t4 + 8 ms	0.7V	Probe Current Off



Circuit Operation

A measurement is initiated when the supply is applied, provided the control input pin 7 is low. Once a measurement is commenced, pin 7 is latched low and the ramp capacitor on pin 12 begins to charge. After 25 ms when switch-on transients have subsided, a constant current is applied to the thermo-resistive probe. The value of probe current, which is supplied by an external PNP transistor, is set by an external resistor across an internally generated 2V reference. The lamp current is applied at the start of probe current.

35 ms after switch-on, the voltage across the probe is sampled and held on external capacitor C1 (leakage current at pin 1 less than 1 nA). After a further 1.5 seconds the difference between the present probe voltage and the initial probe voltage is measured, multiplied by 3 and compared with a reference voltage of 780 mV (externally adjustable via pin 16). If the amplified voltage difference is less than the reference voltage the lamp is switched off, otherwise the lamp commences flashing at 1 Hz to 2 Hz. 10 ms later the measurement latch operates to store the result and after a further 8 ms the probe current is switched off.

A second measurement can only be initiated by interrupting the supply. An external CR can be arranged on pin 7 to prevent a second measurement attempt for 1 minute. The measurement condition stored in the latch will control the lamp.

PROBES

The circuit effectively measures the thermal resistance of the probe. This varies depending on the surrounding medium *(Figure 1)*. It is necessary to be able to heat the probe with the current applied and, for there to be sufficient change in resistance with the temperature change, to provide the voltage to be measured.

Probes require resistance wire with a high resistivity and temperature coefficient. Nickel cobalt alloy resistance wires are available with resistivity of 50 $\mu\Omega$cm and temperature coefficient of 3300 ppm which can be made into suitable probes. Wires used in probes for use in liquids must be designed to drain freely to avoid clogging. A possible arrangement is shown in *Figure 2*.

The probe voltage has to be greater than 0.7V to prevent short circuit probe detection less than 5V to avoid open circuit detection. With a 200 mA probe current this gives a probe resistance range of 4Ω to 25Ω. This low value makes it possible to use the probe in partially conducting fluids.

Using resistance wire of 50 $\mu\Omega$cm resistivity, 8 cm of 0.08 mm (40 AWG) give approximately 8Ω at 25°C. Such a probe will give about 500 mV change between first and second measurements in air, and 100 mV change with oil, hydraulic fluid, etc., in the application circuit. With an alarm threshold of 280 mV (typ) lack of fluid can readily be detected. As the probe current, measurement reference and measurement period are all externally adjustable, there is freedom to use different probes and fluids.

Another possibility is the use of high temperature coefficient resistors made for special applications and positive temperature coefficient thermistors. The encapsulation must have a sufficiently low thermal resistance so as not to mask the change due to the different surrounding mediums, and the thermal time constant must be quick enough to enable the temperature change to take place between the two measurements. The ramp timing could be adjusted to assist this. Probes in liquids must be able to drain freely.

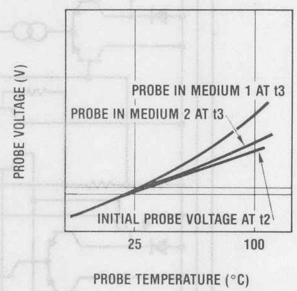


FIGURE 1. Typical Thermo-Resistive Probe

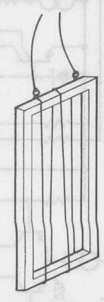
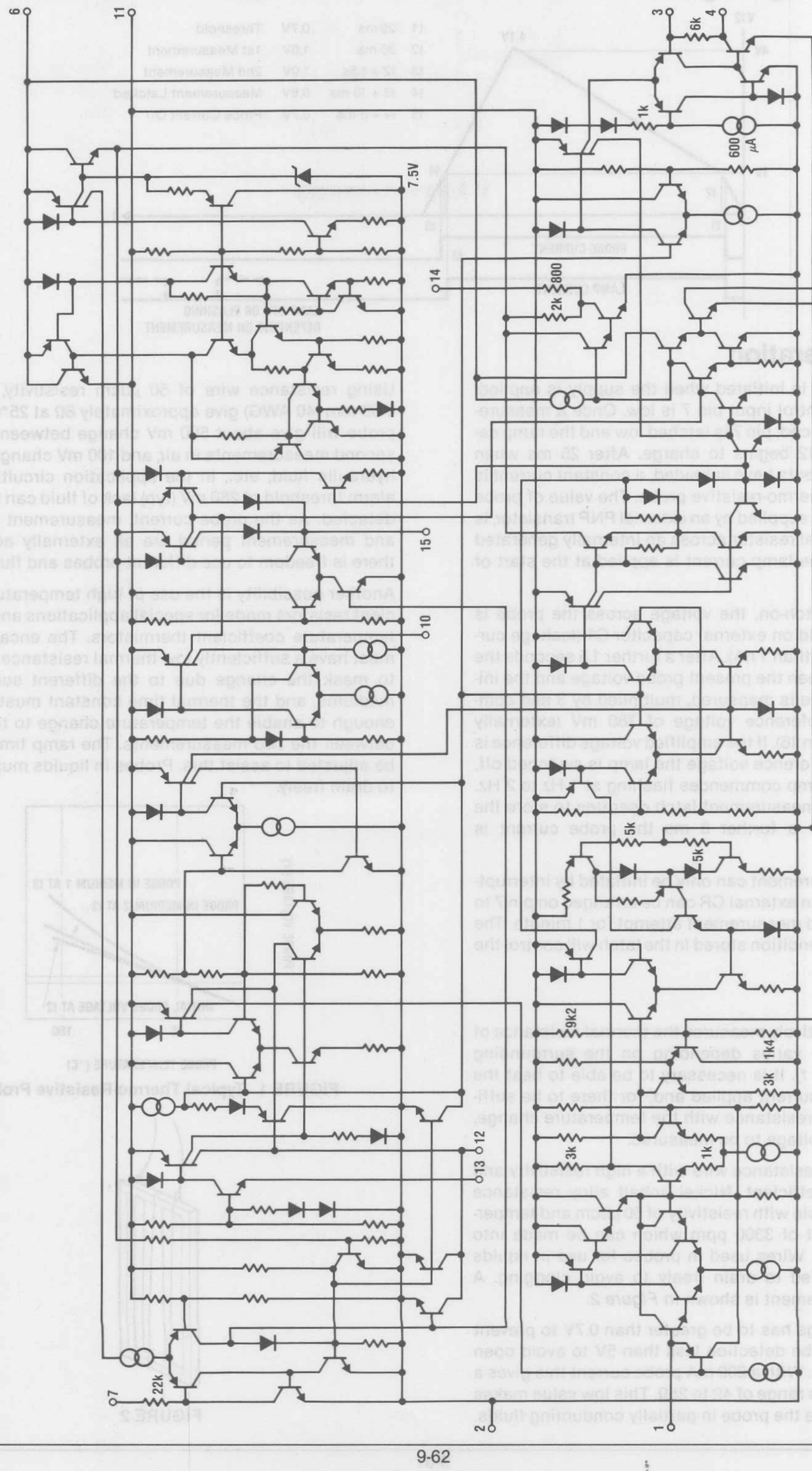


FIGURE 2

Equivalent Schematic Diagram



Application Hints

INTERNAL COMBUSTION ENGINE OIL LEVEL

The basic system provides a single shot measurement when the supply is applied and has a primary application in automotive oil, hydraulic fluid and coolant monitoring. Particularly in the case of engine oil level, a valid measurement is only possible before the oil is disturbed. The application circuit shown is arranged such that the measurement is made when the ignition is switched on via switch A. Switch B is the oil pressure sensor and is closed before the engine starts, keeping pin 7 low and enabling the measurement.

STALLING AND RESTART PROTECTION

The 4M7 resistor and 10 μF capacitor connected to pin 7 provide the restart protection. When oil pressure builds up, switch B opens and the 10 μF capacitor charges through the bulb. At switch-off, the capacitor discharges slowly and is capable of preventing a low state on pin 7 for 1 minute. Unless pin 7 is low, a new measurement can not be made and the previous measurement result stored in the memory capacitor on pin 15 is used to control the output.

MEMORY

The pin 15 memory output goes high if a correct measurement is made (lamp off). If the power is removed, pin 15 leakage is less than 3 μA and the memory status is retained for some time. Provided pin 15 voltage does not fall below 3V, the memory capacitor will be refreshed on powering up again. There is no internal pull down on detecting an incorrect measurement. If it is required to use pin 15 as an output indicating the measurement result, an external pull down resistor and buffer will be required.

CONTINUOUS WARNING LAMP

The lamp can be arranged to light continuously by disabling the oscillator with a resistor of 150k or less, connected between pins 10 and 11.

REPETITIVE MEASUREMENTS

Measurements may be repeated by strobing the supply to pin 6. The probe current regulator transistor must have the same supply as pin 6, but the warning lamp can be permanently powered. The lamp will light during each measurement and will flash in between measurements when incorrect conditions are detected.

ALTERNATIVE APPLICATIONS

Gas flow detection: The cooling effect of gas flowing over a probe could be used to provide a warning signal from the LM903 in the event of gas failure.

Automatic top up: With the LM903 strobed continuously, the output may be stored, buffered, and used to drive solenoid valves to correct a fluid level as required.

National Semiconductor

LM909 Remote Control Receiver

General Description

The LM909 is a remote control receiver and decoder for frequencies up to 40 MHz. The circuit consists of an RF amplifier, AGC, detector, phase lock loop for tone decoding, level detection and switching to push-pull output stages suitable for driving small motors directly. The circuit can be optimized for use with various modulation schemes by adjusting external PLL and demodulation filter components. This device is especially suited to low cost model control applications.

Features

- Good RF sensitivity
- PLL tone demodulator
- Large AGC range
- Outputs capable of 1A surges and 0.6A continuous operation
- Wide supply voltage range
- Internally stabilized supply
- Flip-flop defines reference on PLL
- Four functions–e.g., left/right, forward/reverse capability
- Thermal shutdown overload protection

Typical Application Circuit

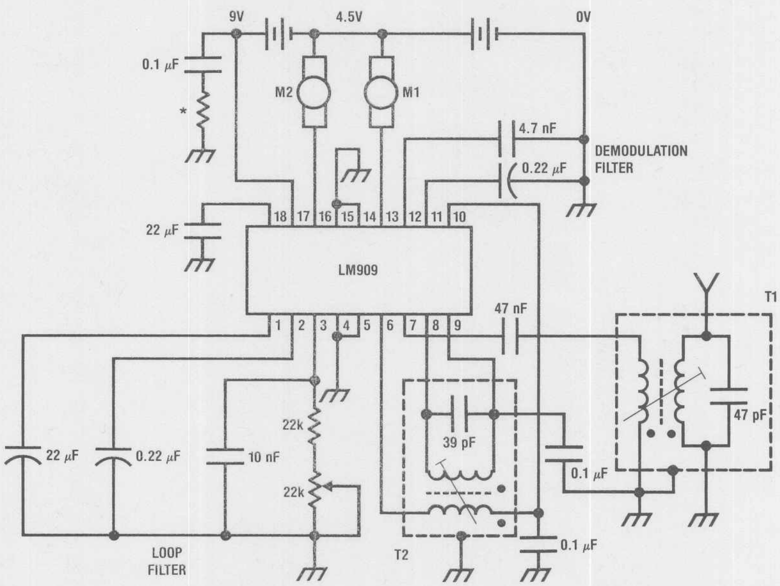


FIGURE 1

T1 Primary 10T
Secondary 4T
T2 Primary 12T
Secondary 2T
5mm Former
* 10Ω–91Ω for better stability and when using an IC socket, see Application Notes.

Absolute Maximum Ratings

Supply Voltage (Pin 17)	14V
RF Input Voltage (Pin 7)	1 Vp-p
Power Dissipation (Note 1)	2W
Operating Temperature Range	0°C to +70°C
Maximum Junction Temperature	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics $V_S = 9V$, $T_A = 25°C$ unless otherwise stated.

	Parameter	Conditions	Min	Typ	Max	Units
V17	Supply Voltage Range		5	9	14	V
I_{17}	Supply Current	$I_{16} = 0$, $I_{13} = 0$ (Note 2)		45	60	mA
V9	Internally Regulated Voltage		2.6	2.8	3.0	V
	Internal Line Regulation	V17 = 5V to 14V		9		mV/V
RECEIVER AND AGC CIRCUIT						
V7	RF Input Sensitivity Pin 7	f = 27 MHz, 100% Mod, 1 kHz (Note 3)		15		μVrms
R7	Input Resistance Pin 7	f = 27 MHz		1.2		kΩ
C7	Input Capacitance Pin 7			10		pF
V6	Input Sensitivity Pin 6	As for Pin 7		120		μVrms
R6	Input Resistance Pin 6			2.2		kΩ
C6	Input Capacitance Pin 6			7		pF
ΔV7	AGC Range	For 10 dB Output Change f = 27 MHz, 100% Mod, 1 kHz		50		dB
V12	Demodulated Output	100% Mod, 1 kHz @ 200 μVrms RF		100		mVp-p
VCO						
f3	Free Running Frequency	$C_{PIN\,3} = 10$ nF, $R_{PIN\,3} = 33k$		11		kHz
	Tuning Range	@ $f_o = 11$ kHz, $C_{PIN\,3} = 10$ nF $R_{PIN\,3} = 22$ kΩ to 44 kΩ		±2		kHz
	Frequency Drift with Supply Voltage	$f_o = 11$ kHz V17 = 5V to 14V		0.1		%/V
	Control Sensitivity	$f_o = 11$ kHz		1.7		kHz/V
	Frequency Drift with Temperature	Temperature Range 0°C to 70°C		4		Hz/°C
PLL						
Δf12	Capture Range	V12 = 100 mVp-p, $f_o = 5.5$ kHz (VCO = 11 kHz)		±800		Hz
Δf12	Holding Range	V12 = 100 mVp-p, $f_o = 5.5$ kHz (VCO = 11 kHz)		±1000		Hz
	Recovered Signal at Pin 2 (Loop Filter)	Pin 12 = 5.5 kHz, 100 mVp-p ±600 Hz Deviation		1.2		Vp-p
V2	DC Level Pin 2		2.5	2.75	3.0	V
DECODER						
V2	Pin 2 Threshold for Pin 1 Sourcing Current			2.45		V
V2	Pin 2 Threshold for Pin 18 Sourcing Current			3.05		V
$I_{1,\,18}$	Pin 1, 18 Charge Current			600		μA
R1, 18	Internal Discharge Resistance of Pins 1 and 18			6.5		kΩ

Electrical Characteristics (Continued) $V_S = 9V$, $T_A = 25°C$ unless otherwise stated.

Parameter		Conditions	Min	Typ	Max	Units
OUTPUT STAGES						
V1	Threshold Voltage for V16 Low	V18 < 0.35V		0.35		V
V18	Threshold Voltage for V16 High	V1 < 0.35V		0.35		V
V1, 18	Threshold Voltage for V13 Low			1.5		V
V1, 18	Threshold Voltage for V13 High			2.75		V
R13, 16	Output Resistance V13, V16 High	$I_{13, 16} = -500$ mA (Sourcing)		2		Ω
R13, 16	Output Resistance V13, V16 Low	$I_{13, 16} = 500$ mA (Sinking)		1		Ω

Note 1: Above 25°C ambient, derate based on $T_j(max) = 150°C$ and a thermal resistance of 85°C/W, junction to ambient.

Note 2: The supply current is virtually constant over the 5V–14V supply range (no signal conditions).

Note 3: For 50 mVp-p recovered audio at pin 12 and RF input terminated in 50Ω.

Typical Performance Characteristics

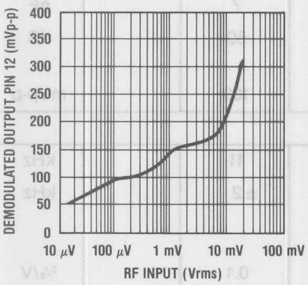


FIGURE 2. Demodulated Output vs RF Input

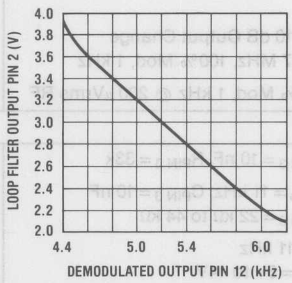


FIGURE 3. PLL Transfer Characteristics

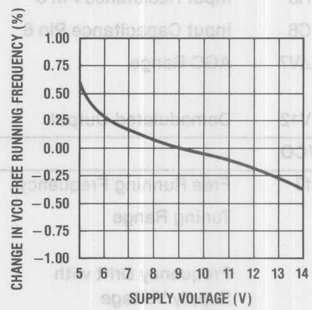


FIGURE 4. VCO Supply Sensitivity

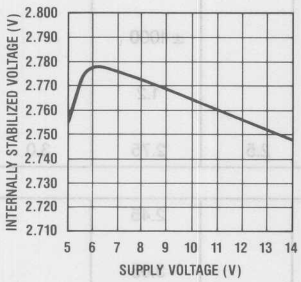


FIGURE 5. Stabilized Voltage vs Supply Voltage

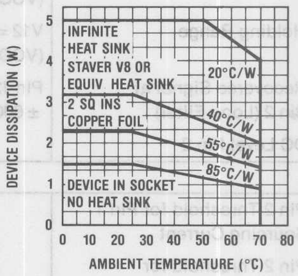


FIGURE 6. Allowable Device Dissipation vs Ambient Temperature

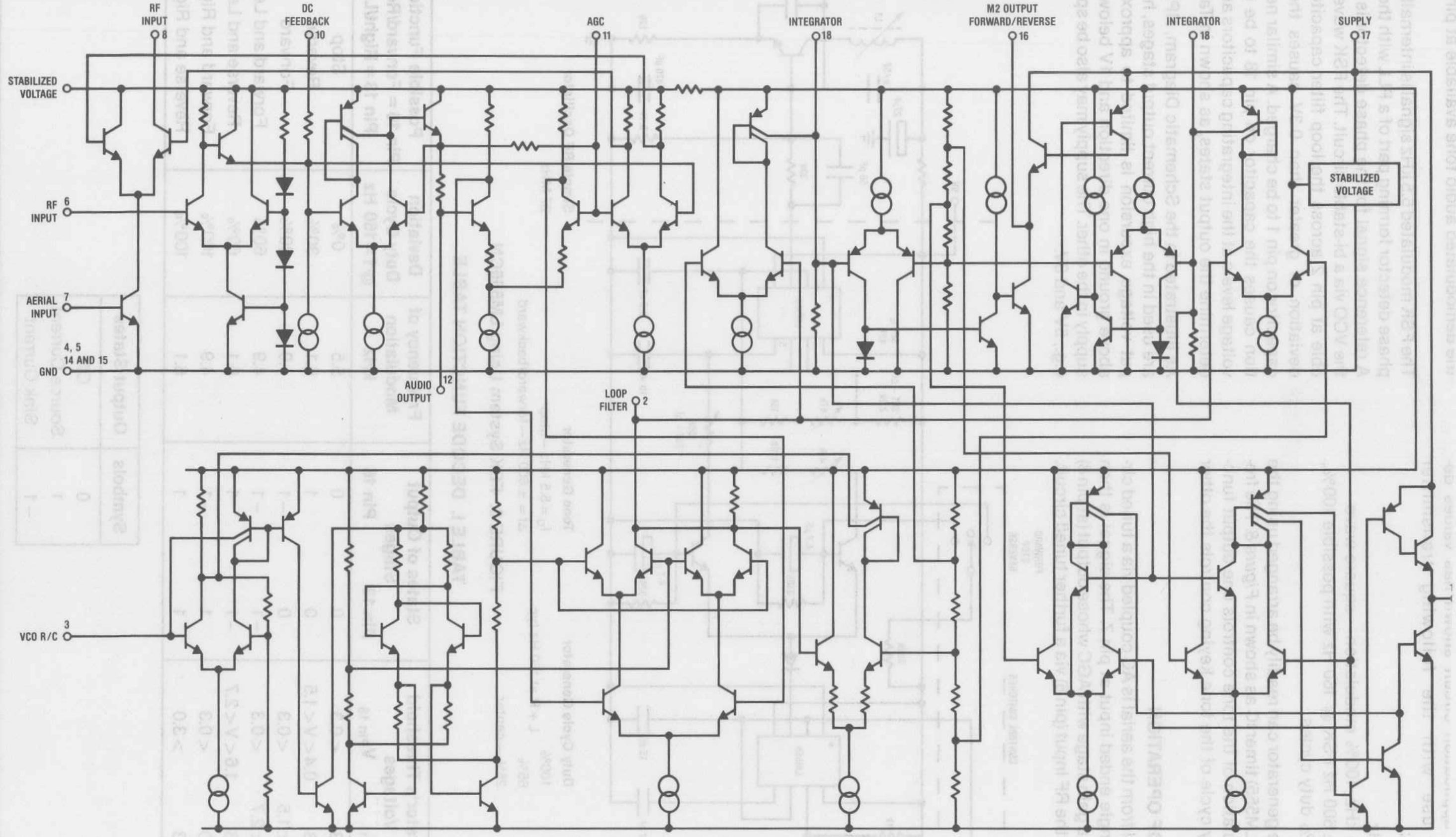

RF INPUT 8
DC FEEDBACK 10
AGC 11
INTEGRATOR 18
M2 OUTPUT FORWARD/REVERSE 16
INTEGRATOR 18
SUPPLY 17
STABILIZED VOLTAGE
STABILIZED VOLTAGE
RF 6 INPUT
AERIAL 7 INPUT
4, 5 14 AND 15 GND
AUDIO OUTPUT 12
LOOP FILTER 2
VCO R/C 3

FIGURE 7

Application Notes

TYPICAL SYSTEM

The receiver application circuit shown has values designed for use with the following transmitter specification:

f RF 27 MHz
f TONE 5.5 kHz, 100% modulation—square wave
Δf TONE ±600 Hz FSK @ 160 Hz with possible 100%, 60% or 30% duty cycles

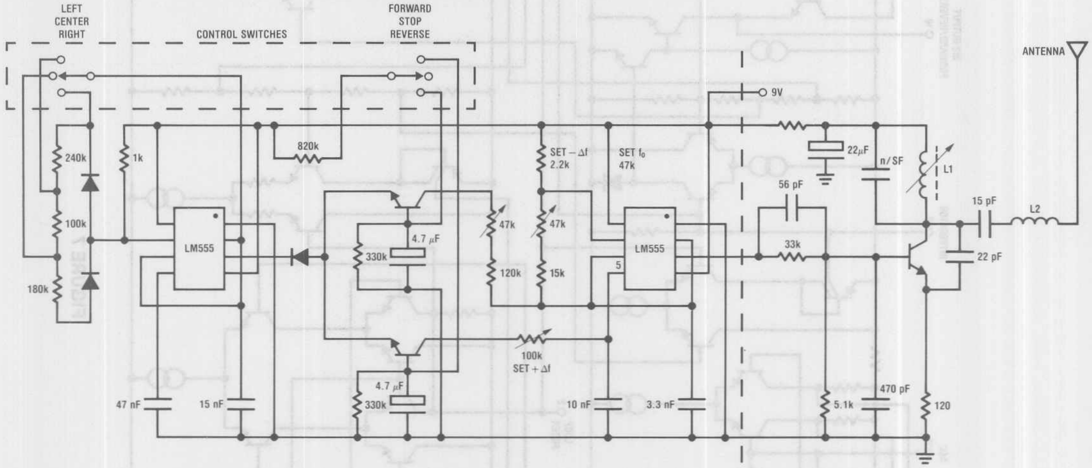
A simple tone generator can readily be arranged using the LM556 (dual LM555) timer IC as shown in *Figure 8.* The frequency modulation of the tone controls one output function. The duty cycle of the tone keying controls the other function.

PRINCIPLE OF OPERATION

The RF signal from the aerial is AC coupled via a tuned circuit to the single ended input at pin 7. The signal is then processed in a gain stage with AGC whose output (at pin 8) can be fed to the RF input (pin 6) via a further tuned circuit. There then follows a fixed gain block and detector, with the demodulated audio tone available at pin 12.

The FSK modulated 5.5 kHz signal is internally applied to a phase detector forming part of a PLL with the 11 kHz VCO. A reference signal for the phase detector is derived from the VCO via a bi-stable circuit. The FSK waveform is available at pin 2 across the loop filter capacitor. A positive deviation of greater than 0.3V causes the integrating capacitor on pin 1 to be charged. A similar negative deviation causes the capacitor on pin 18 to be charged. The voltage levels at the integrating capacitors are decoded to determine the output states, as shown in Table I.

As illustrated in the Schematic Diagram, NPN transistors are used in the high current output stages, hence the output voltage excursion is limited to approximately 0.3V above ground in one direction and 1V below the positive supply in the other. The supply may also be split unequally, e.g., 6V and 3V.



Duty Cycle Generator
100%
65% L + R at 150 Hz typ
25%—center

Tone Generator
f_O = 5.5 kHz—stop
Δf = ±600 Hz—forward/backward

Simple RF Oscillator
27 MHz

FIGURE 8. FSK System Using LM556CN

TABLE I. DECODE FUNCTION TABLE

Integrator's Threshold Voltages $V_{Pin\ 1}$	$V_{Pin\ 18}$	States of Output Stages Pin 13	Pin 16	Frequency of Modulation kHz	Deviation Duty Cycle @ f = 160 Hz	Possible Functions Pin 16 = Forward/Reverse Pin 13 = Right/Left
< 0.3	< 0.3	0	0	5.5	0%	Stop
< 0.3	0.4 < V < 1.5	0	1	6.1	30%	Reverse
0.4 < V < 1.5	< 0.3	0	−1	4.9	30%	Forward
1.6 < V < 2.7	< 0.3	−1	−1	4.9	60%	Forward and Left
< 0.3	1.6 < V < 2.7	−1	1	6.1	60%	Reverse and Left
> 3.0	< 0.3	1	−1	4.9	100%	Forward and Right
< 0.3	> 3.0	1	1	6.1	100%	Reverse and Right

Symbols	Output States
0	Off
1	Source Current
−1	Sink Current

National Semiconductor

LM1014/LM1014A Motor Speed Regulator

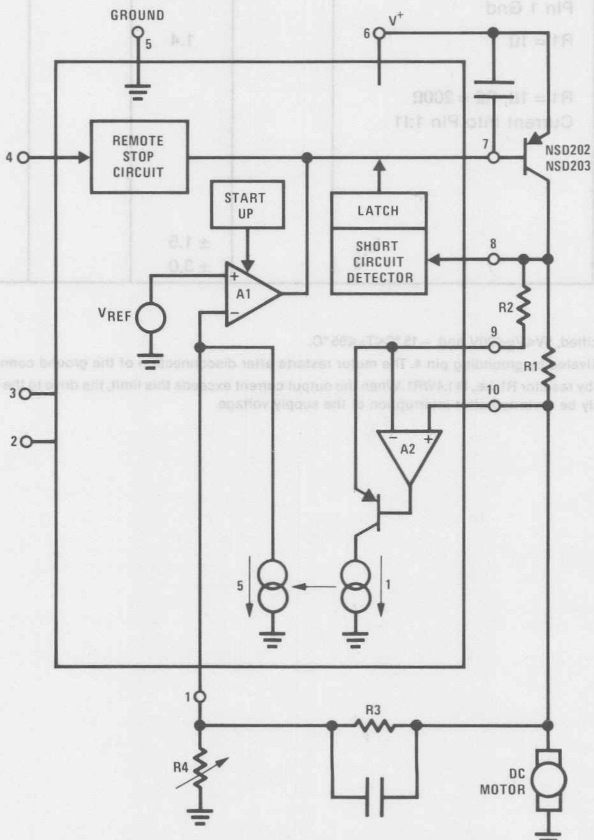
General Description

The LM1014 is a monolithic integrated circuit specifically designed to provide a low cost motor speed regulator for low voltage DC motors.

Features

- 5V to 20V operating voltage range
- Short circuit protection
- Externally selectable temperature coefficient
- Remote pause control
- Saturation voltage 0.1V
- Motor connected to ground for ease of RF suppression
- Motor torque compensation
- Low current consumption

Functional Block Diagram and Typical Connection



Operating Temperature Range	−20 to +70°C
Storage Temperature Range	−65 to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 1)

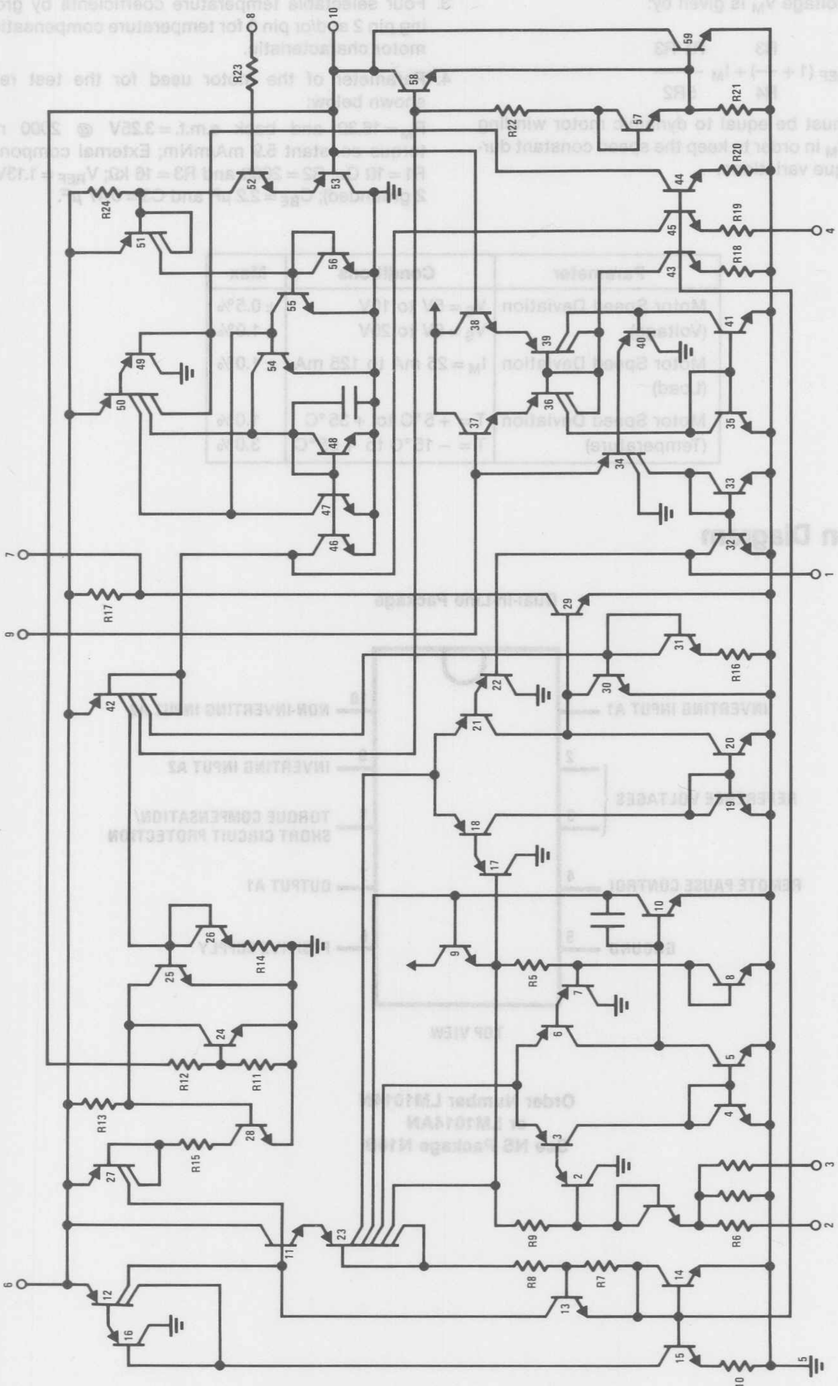
Parameter	Conditions	Min	Typ	Max	Units	Comments
Supply Voltage Range		5.0		20.0	V	
Supply Current	Current into Pin 6		6.0	8.0	mA	
Reference Voltages	Pin 2 and 3 Open		0.93		V	−1.0 mV/°C
	Pin 2 Gnd, Pin 3 Open		1.13		V	−0.3 mV/°C
	Pin 2 Open, Pin 3 Gnd		1.33		V	0.3 mV/°C
	Pin 2 and 3 Gnd		1.53		V	1.0 mV/°C
Line Regulation of Reference Voltage	$V_S = 5V$ to $V_S = 20V$ Pin 1			2.0	% V_{REF}	LM1014
				1.0	% V_{REF}	LM1014A
Remote Stop Current	Current into Pin 4 When Grounded		125	200	μA	Note 2
Output Current A1	$V_S = 5V$ Pin 1 Gnd	15	40		mA	Current into Pin 7
Short Circuit Current Limit	R1 = 1Ω		1.4		A	Note 3
Motor Sense Current Deviation	R1 = 1Ω, R2 = 200Ω Current into Pin 1:I1					(I1/Im − 1) Exclusive of External Components Tolerances
			±1.5		%	LM1014A
			±3.0		%	LM1014

Note 1: Unless otherwise specified, $5V \leq V_S \leq 20V$ and $-15°C \leq T_A \leq 55°C$.

Note 2: The remote stop is activated by grounding pin 4. The motor restarts after disconnection of the ground connection.

Note 3: The current limit is set by resistor R1, i.e., $I \cong 1.4V/R1$. When the output current exceeds this limit, the drive to the output transistor is switched off by a latch circuit. The motor can only be restarted after interruption of the supply voltage.

Schematic Diagram



Typical Performance Characteristics/Application

1. The output voltage V_M is given by:

$$V_M = V_{REF}\left(1 + \frac{R3}{R4}\right) + I_M \frac{R1\,R3}{5R2}$$

2. R1 R3/5R2 must be equal to dynamic motor winding resistance R_M in order to keep the speed constant during load torque variations.

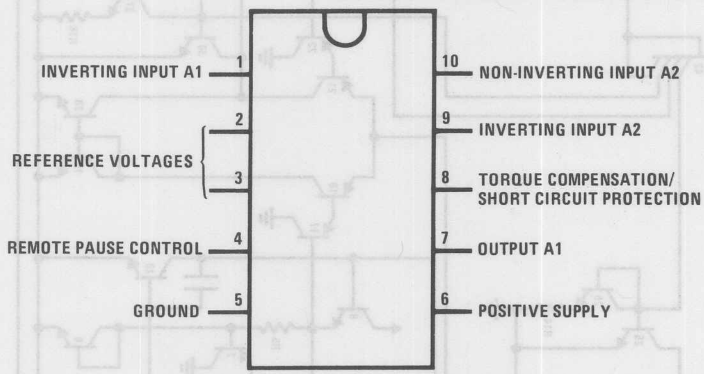
3. Four selectable temperature coefficients by grounding pin 2 and/or pin 3 for temperature compensation of motor characteristic.

4. Parameter of the motor used for the test results shown below:
   $R_M = 16.3\Omega$ and back e.m.f. = 3.25V @ 2000 r.p.m.; torque constant 5.9 mA/mNm; External components: R1 = 1Ω Cu, R2 = 200Ω and R3 = 16 kΩ; $V_{REF} = 1.13V$ (pin 2 grounded); $C_{BE} = 2.2\ \mu F$ and C3 = 0.47 μF.

Parameter	Conditions	Max
Motor Speed Deviation (Voltage)	V_S = 5V to 10V V_S = 5V to 20V	± 0.5% ± 1.0%
Motor Speed Deviation (Load)	I_M = 25 mA to 125 mA	± 1.0%
Motor Speed Deviation (Temperature)	T = +5°C to +35°C T = −15°C to +55°C	1.0% 3.0%

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number LM1014N
or LM1014AN
See NS Package N10B

National Semiconductor

LM1801 Smoke Detector

General Description

The LM1801 is designed to provide the functions of an ionization type smoke detector as specified by UL217. Though primarily designed to operate from a 9V alkaline battery, provision is made for operation at supplies up to 14V and for line operation.

Low battery threshold, alarm threshold, hysteresis and stand-by current drain are externally programmed by resistors. The LM1801 includes a power transistor capable of directly driving a typical 85 dB horn. The ionization chamber requires an external FET buffer.

A parallel alarm output is provided to enable up to 8 similar detectors to be connected in parallel. In this mode, a fault on the line cannot prevent local operation. The low battery alarm signal is confined to the local unit.

A 6V regulated output is provided for the chamber and FET supply and a second output with a different temperature coefficient is available for the alarm threshold potentiometer. This allows compensation of JFET drift.

Features

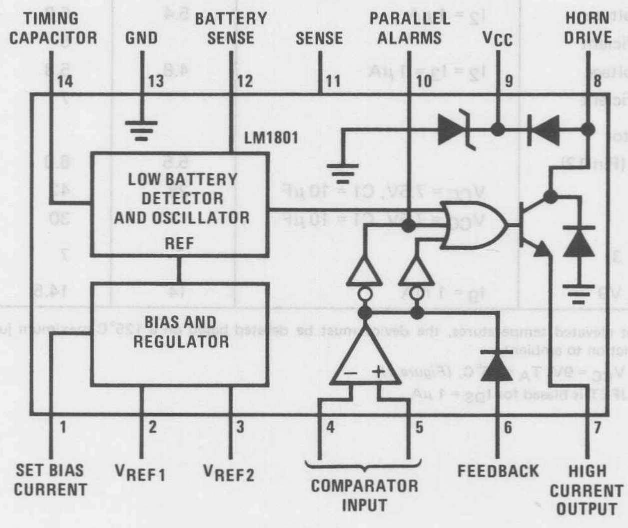
- UL component recognized
- 9V to 14V operation
- Direct drive to horn
- Clamp diodes on chip
- Internal zener for line operation
- JFET and MOSFET compatible
- Parallel alarm capability
- Low stand-by current drain

Applications

- Domestic smoke detectors
- Line operated smoke detectors
- Gas detectors
- Intrusion alarms
- Battery operated detectors

Block and Connection Diagram

Dual-In-Line Package



Order Number LM1801N
See NS Package N14A

Supply Voltage	14V
Input Voltage	−0.3V to 14V
Input Differential Voltage	±14V
Power Dissipation (Note 1)	300 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Comparator					
Input Offset Voltage			3	15	mV
Input Bias Current			3	10	nA
Input Offset Current			0.5	3	nA
Pin 6 Output Low	$I_{SINK} = 100\ \mu A$		1.5	2.0	V
Output Stage (Pin 8)					
Leakage Current			45	500	nA
Saturation Voltage	$I_8 = 200$ mA		0.9	1.3	V
Saturation Voltage	$I_8 = 500$ mA		1.8		V
Common Alarm Line (Pin 10)					
Drive Capabilities	$V4 > V5$				
Output Voltage High		6.0	6.5		V
Output Current	$V10 = 0.0V$	4.0	6.5		mA
Driver Requirements	$V5 > V4$				
Input Voltage			3.6		V
Input Current	$V8 = 1.5V$, $I_8 = 200$ mA		0.4		mA
Regulator					
Pin 2 Reference Voltage	$I_2 = 1\ \mu A$	5.4	5.8	6.4	V
Temperature Coefficient			5		mV/°C
Pin 3 Reference Voltage	$I_2 = I_3 = 1\ \mu A$	4.8	5.3	5.8	V
Temperature Coefficient			7		mV/°C
Battery Check Oscillator					
Threshold Voltage (Pin 12)		5.5	6.0	6.5	V
Period	$V_{CC} = 7.5V$, $C1 = 10\ \mu F$	28	42	50	Sec
Beep Pulse Width	$V_{CC} = 7.5V$, $C1 = 10\ \mu F$		30		ms
Supply Current (Note 3)			7	9	µA
Zener Clamp Voltage, V9	$I_9 = 1$ mA	14	14.5	17	V

Note 1: For operating at elevated temperatures, the device must be derated based on a 125°C maximum junction temperature and a thermal resistance of 187°C/W junction to ambient.

Note 2: $R_{SET} = 10\ M\Omega$, $V_{CC} = 9V$, $T_A = 25°C$, *(Figure 1)*.

Note 3: Stand-by mode. JFET is biased for $I_{DS} = 1\ \mu A$.

In normal operation the stand-by current drain is nominally 6 times the set current at pin 1. The voltage at pin 1 is 2 diode drops below the positive supply voltage. The total stand-by current drain of the smoke detector will include, in addition to the above, the current drawn by the external circuits connected at pins 2, 3 and 12. These comprise the resistive dividers used to set the low battery threshold and alarm threshold plus the bias current in the ionization chamber and FET buffer.

The low battery threshold is set by R1 and R2 *(Figure 1)*. Select these values so that the voltage at pin 12 is equal to the oscillator trip voltage when the battery voltage is 5.2V.

Hysteresis can be provided by R5, giving an added degree of noise immunity in high noise environments.

Figure 2 is a suggested PC board layout for the circuit of *Figure 1*.

Parallel operation of 2 or more units is easily achieved with a pair of wires connecting pin 10 of each unit and ground. In this mode, every alarm will sound should any single unit detect smoke.

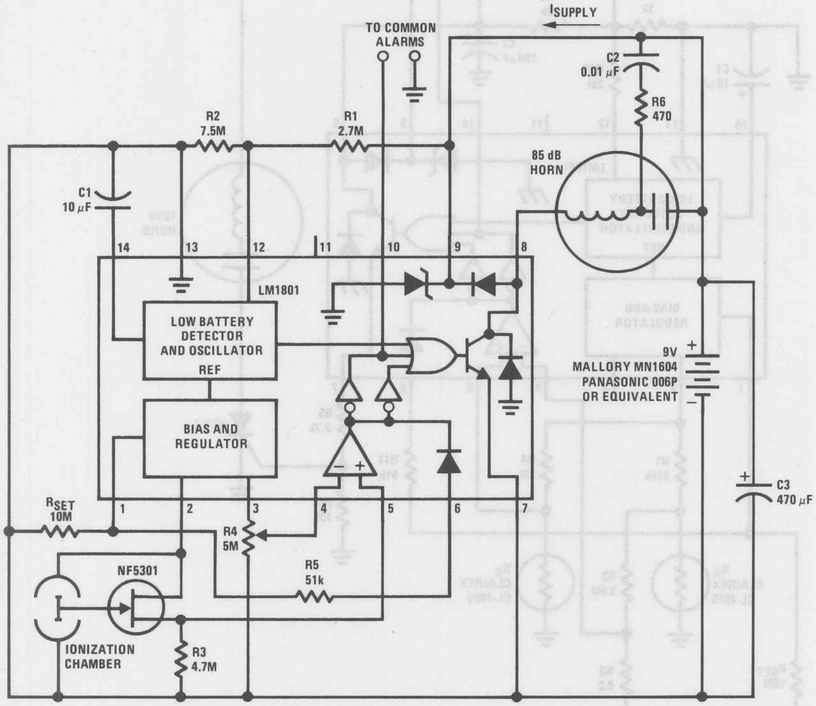


FIGURE 1. 9V Battery Operated Ionization Type Smoke Detector

9

Application Hints (Continued)

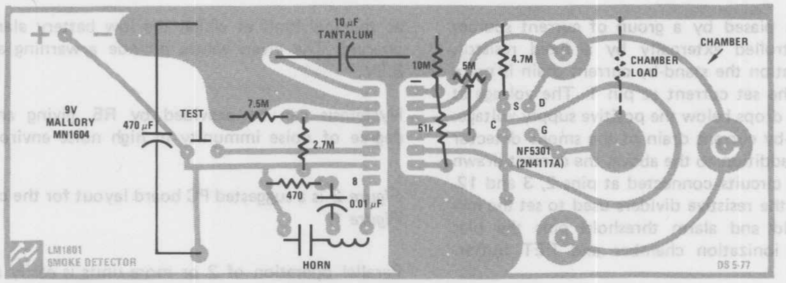


FIGURE 2. Smoke Detector PC Board Layout (Not to Scale)

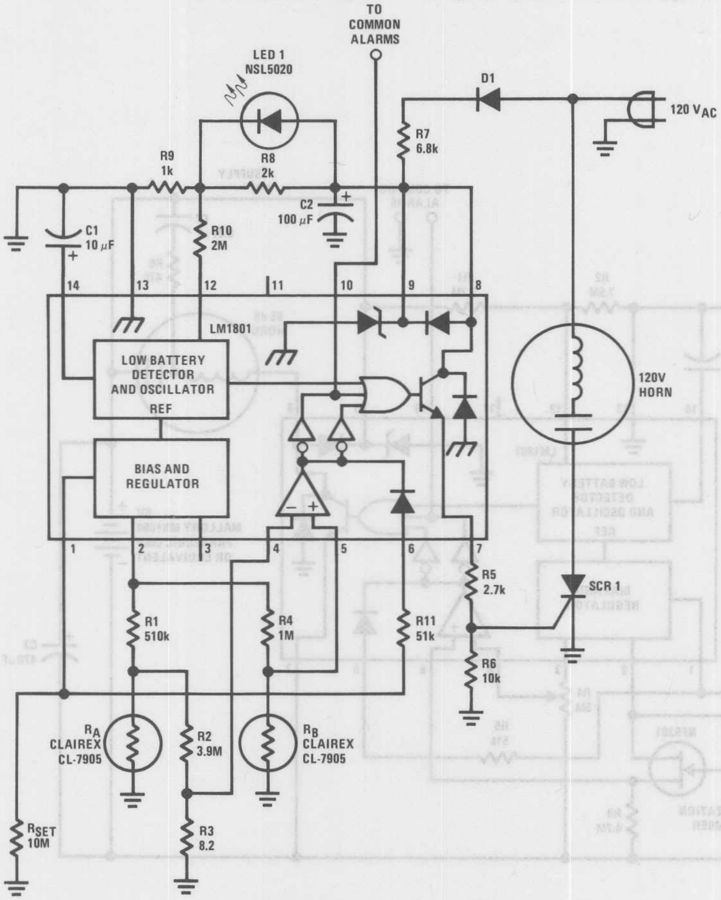


FIGURE 3. Line-Operated Photo-Electric Smoke Alarm Using Light Sensitive Resistor (Includes Detection of Open-Circuited LED)

National Semiconductor

LM1812 Ultrasonic Transceiver

General Description

The LM1812 is a general purpose ultrasonic transceiver designed for use in a variety of ranging, sensing, and communications applications. The chip contains a pulse-modulated class C transmitter, a high gain receiver, a pulse modulation detector, and noise rejection circuitry.

A single LC network defines the operating frequency for both the transmitter and receiver. The class C transmitter output drives up to 1A (12W) peak at frequencies up to 325 kHz. The externally programmed receiver gain provides a detection sensitivity of 200 μVp-p. Detection circuitry included on-chip is capable of rejecting impulse noise with external programming. The detector output sinks up to 1A.

Applications include sonar systems, non-contact ranging, and acoustical data links, in both liquid and gas ambients.

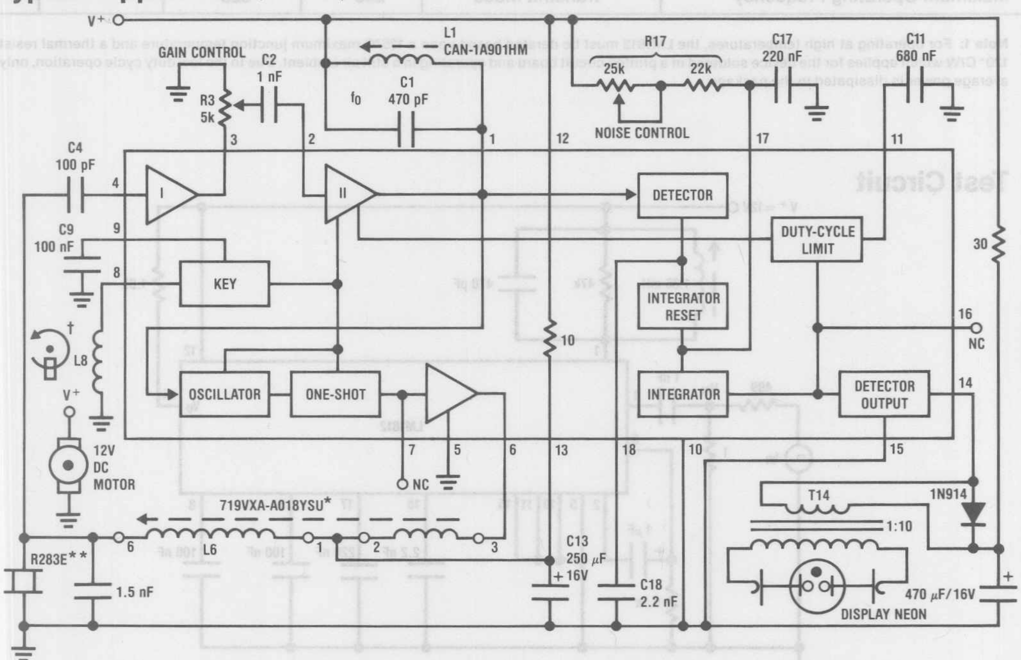
Features

- One or two-transducer operation
- Transducers interchangeable without realignment
- No external transistors
- Impulse noise rejection
- No heat sinking
- Protection circuitry included
- Detector output drives 1A peak load
- Ranges in excess of 100 feet in water, 20 feet in air
- 12W peak transmit power

Applications

- Liquid level measurement
- Sonar
- Surface profiling
- Data links
- Hydroacoustic communications
- Non-contact sensing
- Industrial process control

Typical Application ($V^+ = 12V$)



†Note: Echo returns are displayed by a neon lamp on a motor driven disc. Connections to the neon are made through brushes and slip rings. Rotating with and counterbalancing the neon lamp is a permanent magnet whose field induces a pulse in a stationary coil (L8) as it passes by. This pulse keys the LM1812's transmitter.

*Available from Toko America, Inc., 5520 West Touhy Avenue, Skokie, Illinois 60077 Tel. (312) 677-3640

**Available from Massa Products Corporation, 280 Lincoln Street, Hingham, Massachusetts 02043 Tel. (617) 749-4800

FIGURE 1. 200 kHz Depth Sounder, 5 Feet to 100 Feet

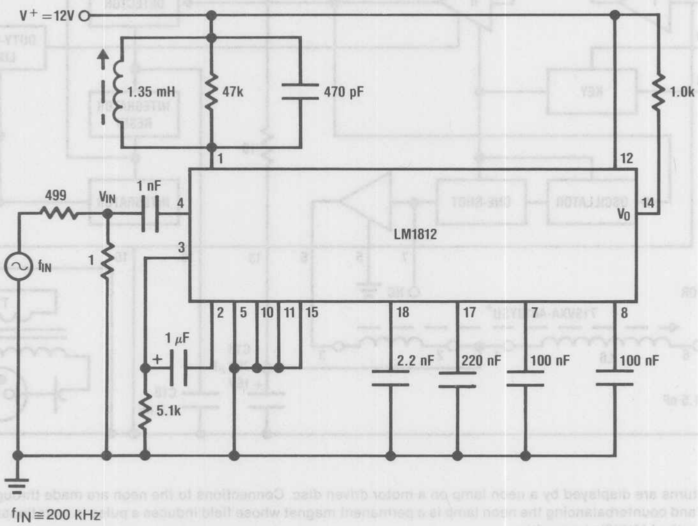
Peak Current (Pins 6, 14)	1A
Input Current (Pins 4, 8)	50 mA
Operating Temperature	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics ($V^+ = 12V$, $T_A = 25°C$, unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
Input Sensitivity	*Figure 2*		200	600	μVp-p
Transmitter Output, V_{SAT}	$I_6 = 1A$		1.3	3	V
Transmitter Output Leakage	V6 = 36V V8 = 0V		0.01	1	mA
Detector Output, V_{SAT}	$I_{14} = 1A$		1.5	3	V
Detector Output Leakage	V14 = 36V		0.01	1	mA
Transmitter Key Threshold	$I_8 = 1$ mA	0.55	0.7	0.9	V
Supply Current	$I_1 + I_{12}$ Receive Mode	5	8.5	20	mA
V8 for Receive Mode				0.3	V
Maximum Operating Frequency	Transmit Mode	200	325		kHz

Note 1: For operating at high temperatures, the LM1812 must be derated based upon a 125°C maximum junction temperature and a thermal resistance of 120° C/W which applies for the device soldered in a printed circuit board and operating in a still air ambient. Due to the low duty cycle operation, only a small average power is dissipated in the package.

Test Circuit



$f_{IN} \cong 200$ kHz

Input sensitivity = minimum V_{IN} for V_O to go low

FIGURE 2. Sensitivity Test Circuit

Application Hints

EXTERNAL COMPONENT DESCRIPTIONS

Pin	Component	Typical Values	Pin Description	Component Function
1	L1, C1	500 μH–50 mH 250 pF–2.2 nF	Second gain stage output/ transmitter oscillator	Set the operating frequency (f_O) for the transmit oscillator and receiver
2	C2	500 pF–10 nF	Second gain stage input	Couples first and second gain stage
3	R3	5.1 kΩ	First gain stage output	Terminates emitter-follower output
4	C4	100 pF–10 nF	First gain stage input	Input coupling for the first gain stage
6	L6	50 μH–10 mH	Transmitter output	Matches LM1812 to the transducer
7	—	—	Transmitter driver	—
8	R8	1 kΩ–10 kΩ	Transmitter key	Current limiter for keying pulses up to 12V
9	C9	100 nF–10 μF	Receiver second stage delay	Sets the receiver turn-on delay after transmit (*Figure 10*)
11	C11	220 nF–2.2 μF	Detector output duty cycle limit	Limits the duty cycle of the detector output (short to ground to defeat)
13	C13	100 μF–1000 μF	Transmitter supply decoupling	Decouples the transmitter power supply
14	T14	$L_P \geq 50$ mH $N_S/N_P \cong 10$	Detector output	Drives neon display lamp
16	—	—	Output driver	—
17	R17, C17	22k–Open 10 nF–10 μF	Pulse integrator	Controls integration time constant (*Figure 13*)
18	C18	1 nF–100 μF	Pulse integrator reset	Controls integrator reset time constant (*Figure 14*)

TRANSDUCERS

The most common transducer used with the LM1812 is the piezo-ceramic type which is electrically similar to a quartz crystal. Piezo-ceramic transducers are resistive at only two frequencies, termed the resonant and antiresonant (f_r, f_a) frequencies. Elsewhere these transducers exhibit some reactance as shown in *Figure 3*.

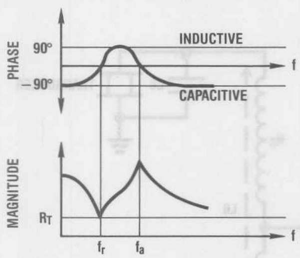


FIGURE 3. Phase and Magnitude of Transducer Impedance

For transmitting (to maximize electrical to mechanical efficiency), the transducer should be operated at its resonant frequency. For receiving (to maximize mechanical to electrical efficiency), optimum operation is at antiresonance. In two-transducer systems the resonant frequency of the transmit transducer is matched to the antiresonant frequency of the receiver.

The LM1812 is primarily used with a single transducer performing both transmit and receive functions. In this mode, maximum echo sensitivity will occur at a frequency close to resonance.

Transducer ringing is a troublesome phenomenon of single transducer systems. After a transducer has been electrically driven in the transmit mode, some time is required for the mechanical vibrations to stop. Depending on the amount of damping, this ringing may last from 10 to 1000 cycles. This mechanical ring produces an electrical signal strong enough (>200 μVp-p) to hold the detector ON, thus masking any echo signals occurring during this time.

A solution to this ring problem is to vary the receiver gain from a minimum, just after transmit, to a maximum, when the ring signal has dropped below the full-gain detection threshold. Since near-range echo signals are much stronger than ring signals, close echoes will still be detected in spite of the reduced gain.

The gain is varied by attenuating the signal between pins 2 and 3 of the LM1812. *Figure 4* shows such an arrangement.

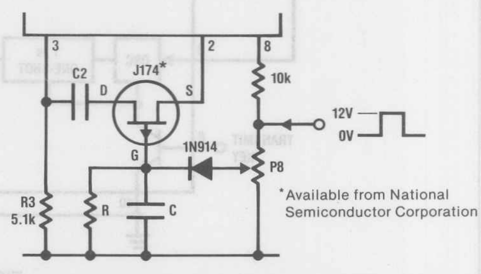


FIGURE 4. Time Variable FET Attenuator

Application Hints (Continued)

An externally generated 12V pulse (*Figure 17*) keys the transmitter and activates the attenuator. This pulse charges C to a voltage set by P8, turning the FET OFF. C slowly discharges through R, decreasing the gate voltage, which in turn decreases the attenuation of the signal passing from pin 3 to pin 2. R and C are selected so that the FET is not completely turned ON until all detectable ringing has stopped. The duration of the ring is rarely specified by the transducer manufacturer and must be experimentally determined.

When designing an ultrasonic ranging system, three *transducer* parameters are very important:

1) resonant impedance (R_T in *Figure 3b*)
2) maximum peak-to-peak voltage
3) resonant frequency, f_r

This data, used in conjunction with the curves given in *Figure 6*, results in a functional output stage design.

TRANSMITTER

The transmitter (*Figure 5*) consists of an oscillator, a 1 μs one-shot, and a power amplifier.

When the transmitter is keyed ON at pin 8 the L1-C1 tank is switched to the oscillator mode. An on-chip 1 μs one-shot is triggered with each cycle of the oscillator and, in turn, drives a power amplifier. This one-shot has a reset time of 2 μs, limiting the maximum operating frequency to about 325 kHz. A transformer couples the transducer to the output stage.

The oscillator frequency is set by L1-C1 and can be calculated from

$$f_O = \frac{1}{2\pi\sqrt{L1C1}}$$

The L1-C1 tank must have a minimum R_P of 10 kΩ where

$$R_P = 2\pi f_O Q L1$$

and Q = unloaded Q of L1-C1 tank.

The output transformer (L6) is designed with the aid of *Figure 6*. Curves are shown for two common frequencies: 40 kHz and 200 kHz. For a given load impedance (R_T, *Figure 3b*), a turns ratio for L6 is determined. In order not to exceed the transducer's specifications, the peak-to-peak output voltage may need to be adjusted using the equation:

$$Vp\text{-}p = 2V^+ \left(\frac{N_S}{N_P}\right)$$

To ensure that the output stage is not overloaded, a current measurement must be made at pin 6. While the first few pulses of each transmit period may reach 2A or 3A, the steady-state current spikes must not exceed 1A. Current spikes are reduced by decreasing the turns ratio of L6.

The secondary of L6 tunes with C6 at the operating frequency, f_O.

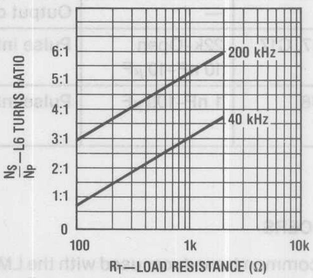


FIGURE 6. L6 Turns Ratio vs Load Resistance

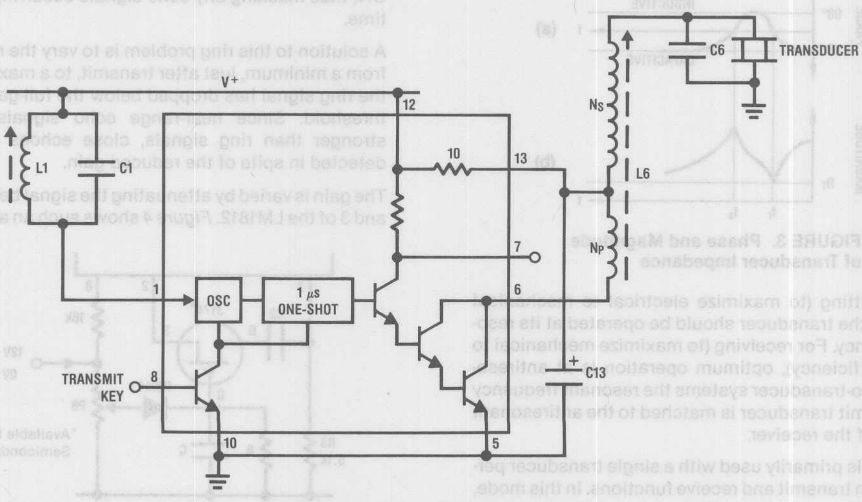


FIGURE 5. Transmitter

Application Hints (Continued)

Where additional power is desired, a pulse amplifier or a pulse stretcher can be used as shown in *Figure 7*. The pulse amplifier (*Figure 7a*) increases output current up to 5A. The pulse stretcher (*Figure 7b*) increases output current *and* pulse width. The wider pulse of *Figure 7b* is especially useful at lower frequencies where the relatively narrow 1 μs pulse creates a large peak current demand for a given power level. Pulse width as a function of R is plotted in *Figure 8*.

Pin 8 performs the function of switching the LM1812 into either the transmit or receive mode. When pin 8 is held high, the chip is in the transmit mode. When held low, it is in the receive mode. The input current at pin 8 should be designed to operate within a 1 mA–10 mA range.

RECEIVER

The receiver section (*Figure 9*) contains two separate gain stages.

In some applications large voltages are applied across the transducer during transmit. Since the receiver input is coupled to the transducer, some protection is necessary to limit the input current spikes to less than 50 mA. Where the voltage across the transducer is less than 200 Vp-p, a C4 reactance of 5 kΩ at the operating frequency is adequate protection. Above 200 Vp-p, a 5 kΩ resistor should be inserted in series with C4.

Since the L1-C1 tank circuit is shared with the oscillator, both the transmitter and receiver are always tuned to the same frequency. The second stage voltage gain is given by:

$$A_V = \frac{Q}{70}\sqrt{\frac{L1}{C1}}$$

where Q = unloaded Q of L1-C1 tank.

When the LM1812 is in the transmit mode, the second gain stage is turned OFF. When switching back to the receive mode, the gain stage does not turn ON immediately, but instead turns ON after a slight delay as programmed by C9. This delay blanks the receiver (and therefore the detector) momentarily, giving the transducer time to stop ringing.

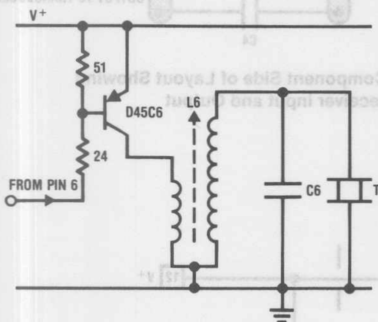


FIGURE 7a. Pulse Amplifier

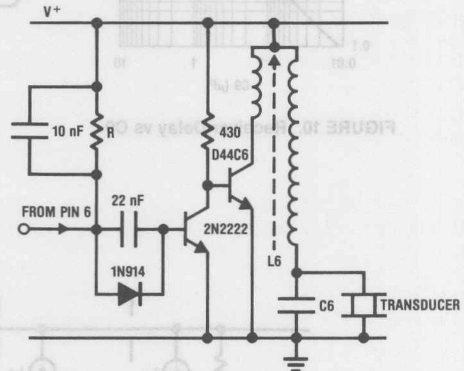


FIGURE 7b. Pulse Stretcher

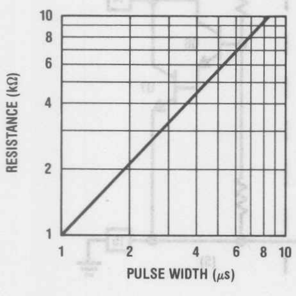


FIGURE 8. Pulse Stretcher Resistance vs Pulse Width

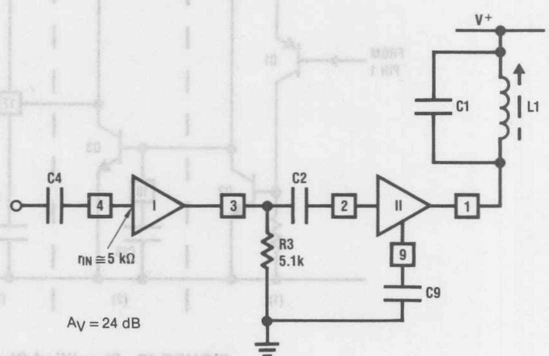


FIGURE 9. Receiver Section

Delay as a function of C9 is plotted in *Figure 10*. The second gain stage may be shut OFF independently of pin 8 by pulling pin 9 low.

Due to the high gain of the receiver, care must be taken to avoid oscillations. Oscillation problems are reduced by keeping the components associated with pins 1 and 4 well separated (*Figure 11*). The transducer must be connected to the circuit with shielded cable. This not only helps avoid oscillation, but also reduces electrical noise pick-up. As a last resort, receiver gain can be reduced with R3 as in *Figure 1*.

PULSE DETECTOR

The pulse detector circuitry (*Figure 12*) consists of five distinct stages: 1) threshold detector, 2) pulse integrator reset, 3) pulse integrator, 4) output driver, 5) power output stage.

The detector (Q1, Q2) switches on all pin 1 signals that exceed 1.4 Vp-p. Since noise pulses are also detected, filtering is done by an integrator stage, C17 and R17, whose time constant is typically 10% to 50% of the transmit time. Integration starts when Q3 turns OFF, which occurs at the same moment Q1 and Q2 detect a signal. Pins 16 and 14 go low after the integration delay.

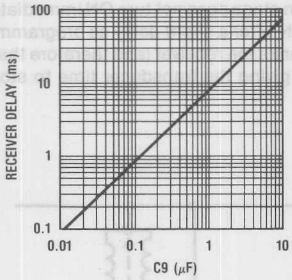


FIGURE 10. Receiver Delay vs C9

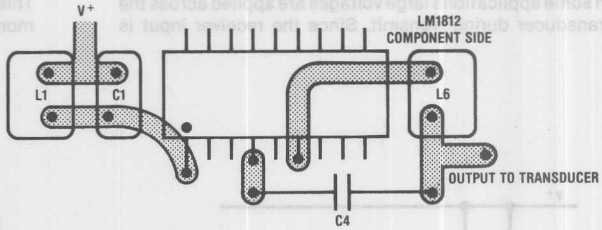


FIGURE 11. Component Side of Layout Showing Isolation of Receiver Input and Output

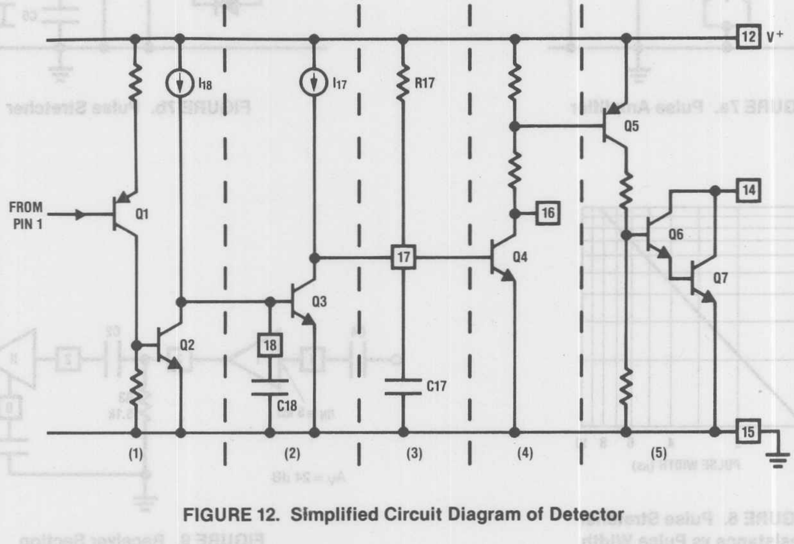


FIGURE 12. Simplified Circuit Diagram of Detector

Application Hints (Continued)

When the voltage at pin 1 becomes too small to activate the detector (<1.4 Vp-p), the integrator is reset by Q3 after a delay introduced by C18. A delay of 1 to 10 cycles of the transmitted frequency is typical. These integration and reset delays, as a function of the external component values, are shown in *Figures 13 and 14*.

Pin 16 provides a CMOS compatible logic output. For driving high-intensity displays, pin 14 will sink up to 1A. When driving a transformer such as T14 in *Figure 1*, it is possible for the primary current to integrate up to destructive levels under conditions of multiple echo reception. Pin 11 is employed to protect the power output (pin 14). C11 integrates an internal current source while pin 14 is low. When V11 reaches a 0.7V threshold, the second gain stage is turned OFF. With the receiver OFF, no signal will be applied to the detector, and pin 14 will turn OFF. After another delay C11 is discharged and the receiver is then again activated. With C11 = 680 nF and a continuous echo return, the receiver will cycle ON and OFF every 6 ms. This function can be defeated by grounding pin 11.

TYPICAL OPERATION

Figure 15 shows typical waveforms at pins 1 and 16 for 200 kHz operation, with pin 9 left open. The pin 1 oscillator signal (5 Vp-p) lasts for 200 μs. The next 900 μs show a ring signal so strong that it is clipped by the receiver. The exponential nature of the decaying ring is seen for the next 500 μs. An echo return appears at 3.9 ms. Note that the detector is held low during the transmit period and for the duration of the ring.

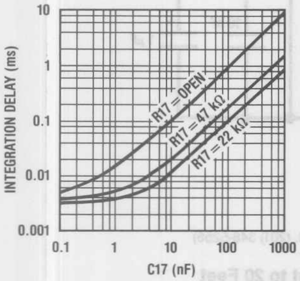


FIGURE 13. Integration Delay vs C17

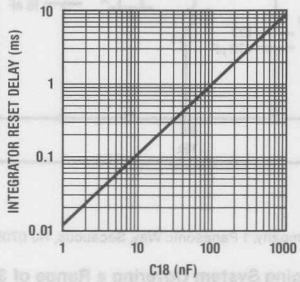


FIGURE 14. Integrator Reset Delay vs C18

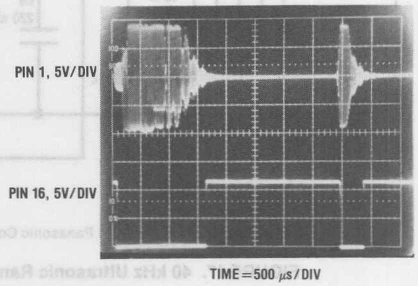
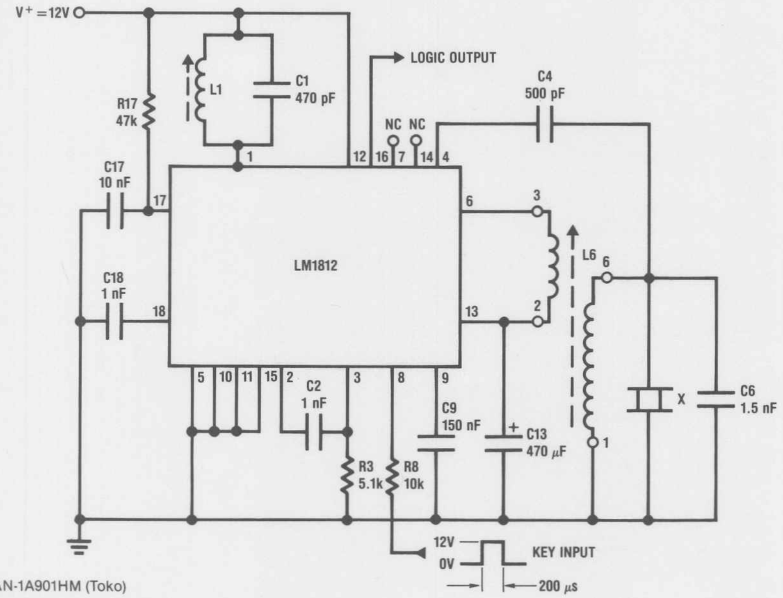


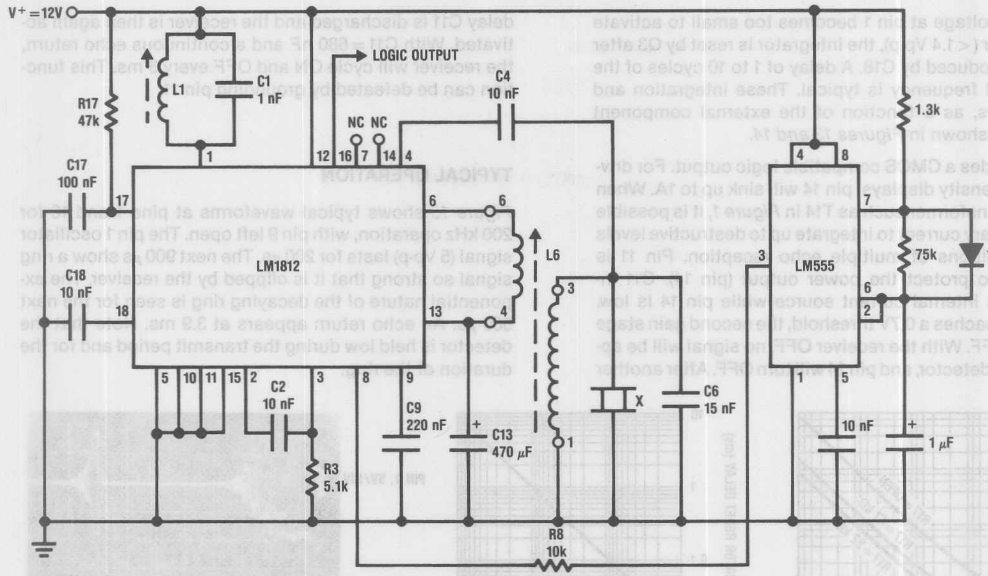
FIGURE 15. Typical Transmit/Receive Waveforms



L1 = CAN-1A901HM (Toko)
L6 = 719VXA-A018YSU (Toko)
X = R283E (Massa Products)

FIGURE 16. 200 kHz Ultrasonic Ranging System for 4 Inches to 6 Feet in Air

Application Hints (Continued)



L1 = CLN-2A900HM (Toko)
L6 = 719VXA-A017AO (Toko)
X = EFR-OAB40K4 (available from Panasonic Company, 1 Panasonic Way, Secaucus, NJ 07094, Tel. (201) 348-5256)

FIGURE 17. 40 kHz Ultrasonic Ranging System Covering a Range of 3 Feet to 20 Feet

LM1815 Adaptive Sense Amplifier

General Description

The LM1815 is an adaptive sense amplifier and default gating circuit for motor control applications. The sense amplifier provides a one-shot pulse output whose leading edge coincides with the negative-going zero crossing of a ground referenced input signal such as from a variable reluctance magnetic pick-up coil.

In normal operation, this timing reference signal is processed (delayed) externally and returned to the LM1815. A logic input is then able to select either the timing reference or the processed signal for transmission to the output driver stage.

The adaptive sense amplifier operates with a positive-going threshold which is derived by peak detecting the incoming signal and dividing this down. Thus the input hysteresis varies with input signal amplitude. This enables the circuit to sense in situations where the high speed noise is greater than the low speed signal amplitude. Minimum input signal is 100 mVp-p.

Features

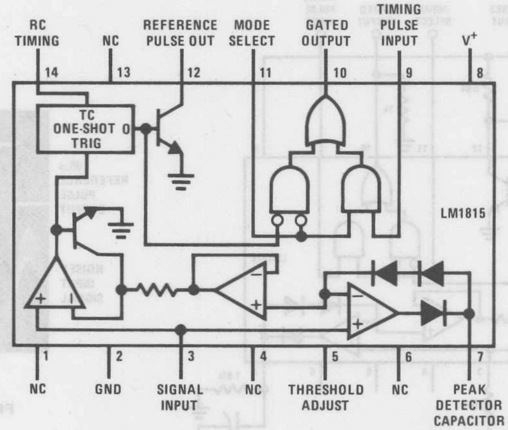
- Adaptive hysteresis
- Single supply operation
- Ground referenced input
- True zero crossing timing reference
- Operates from 2V to 12V supply voltage
- Handles inputs from 100 mV to over 120V with external resistor
- CMOS compatible logic

Applications

- Position sensing with notched wheels
- Zero crossing switch
- Motor speed control
- Tachometer
- Engine testing

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number LM1815N
See NS Package N14A

Absolute Maximum Ratings

Supply Voltage	12V
Power Dissipation (Note 1)	230 mW
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 2)	125°C
Input Current	±30 mA

Electrical Characteristics (T_A = 25°C, V_{CC} = 10V, unless otherwise specified, see *Figure 1*)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage		2.5	10	12	V
Supply Current	f_{IN} = 500 Hz, Pin 9 = 2V, Pin 11 = 0.8V		3.6		mA
Reference Pulse Width	f_{IN} = 1 Hz to 2 kHz	70	100	130	μs
Input Bias Current	V_{IN} = 2V, (Pin 9 and Pin 11)			5	μA
Input Bias Current	V_{IN} = 0V dc, (Pin 3)		200		nA
Input Impedance	V_{IN} = 5Vrms, (Note 3)	12	20	28	kΩ
Zero Crossing Threshold	V_{IN} = 100 mVp-p, (Pin 3)			25	mV
Logic Threshold	(Pin 9 and Pin 11)	0.8	1.1	2.0	V
V_{OUT} High	R_L = 1 kΩ, (Pin 10)	7.5	8.6		V
V_{OUT} Low	I_{SINK} = 0.1 mA, (Pin 10)		0.3	0.4	V
Input Arming Threshold	Pin 5 Open, $V_{IN} \leq$ 135 mVp-p	45		60	mV
	Pin 5 Open, $V_{IN} \geq$ 230 mVp-p	40	80	90	% of V_3 Pk
	Pin 5 to V^+	250			mV
	Pin 5 to Gnd	−25		25	mV
Output Leakage Pin 12	V_{12} = 11V		0.01	10	μA
Saturation Voltage P12	I_{12} = 2 mA		0.2	0.4	V

Note 1: Derate at 5.7 mW/°C for ambient temperatures above 85°C. This applies when the device is soldered into a printed circuit board, operating in still air ambient.

Note 2: Temporary excursions to 150°C can be tolerated.

Note 3: Measured at input to external 18 kΩ resistor. IC contains 1 kΩ in series with a diode to attenuate the input signal.

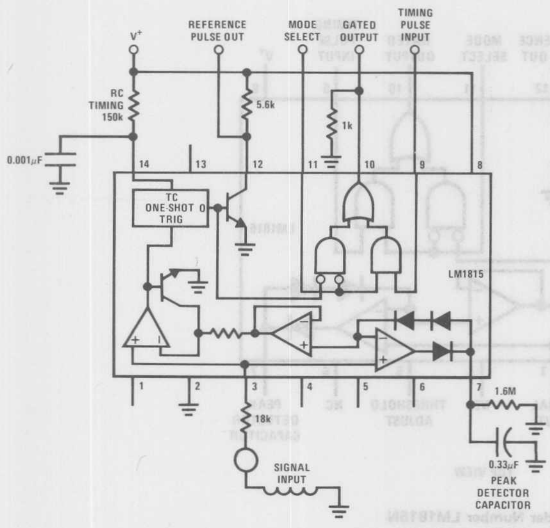


FIGURE 1. LM1815 Adaptive Sense Amplifier

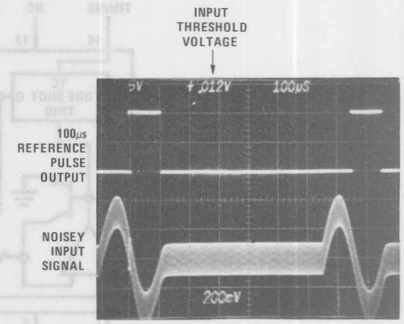
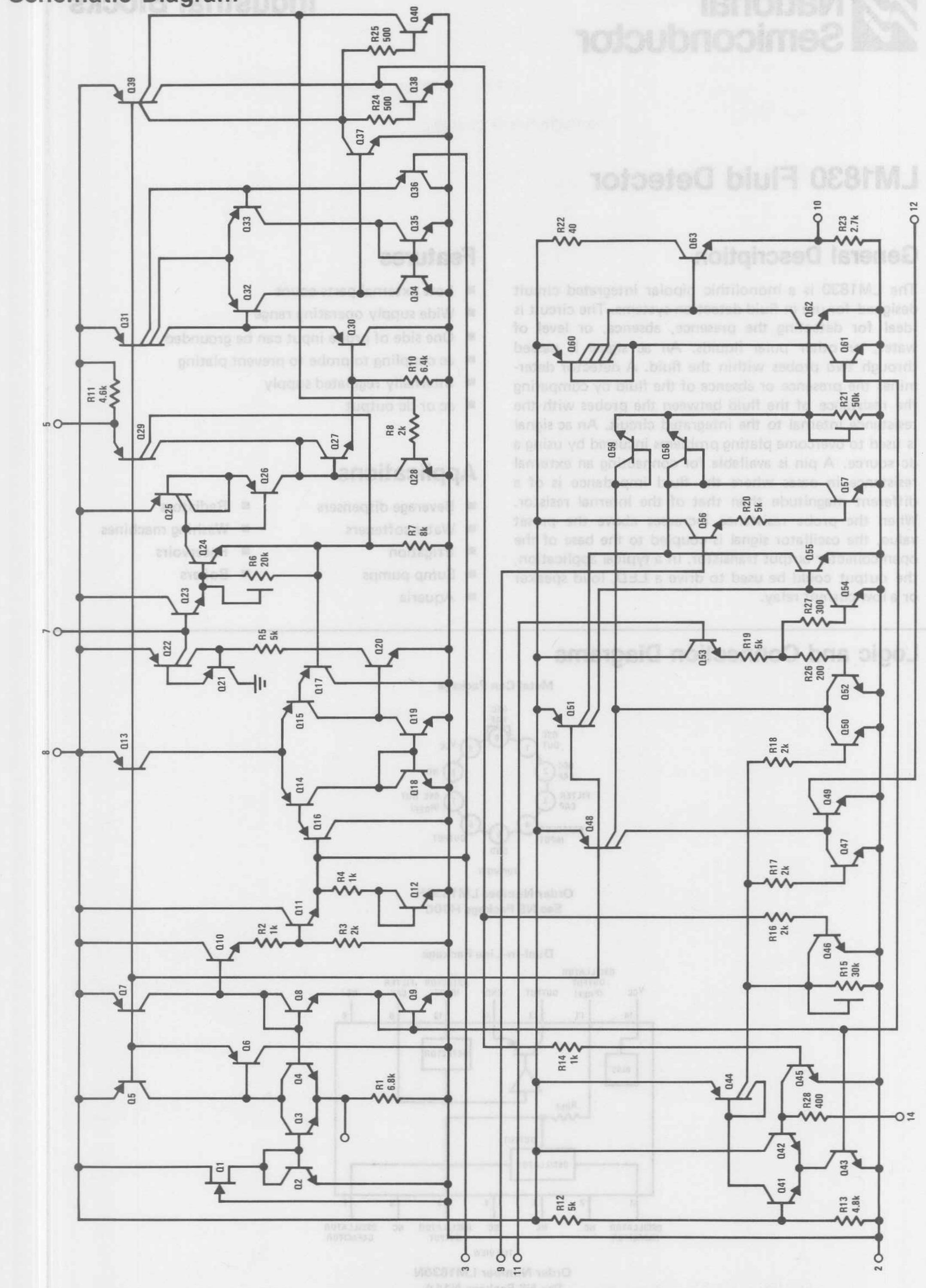


FIGURE 2. LM1815 Oscillograms

Schematic Diagram



LM1830 Fluid Detector

General Description

The LM1830 is a monolithic bipolar integrated circuit designed for use in fluid detection systems. The circuit is ideal for detecting the presence, absence, or level of water, or other polar liquids. An ac signal is passed through two probes within the fluid. A detector determines the presence or absence of the fluid by comparing the resistance of the fluid between the probes with the resistance internal to the integrated circuit. An ac signal is used to overcome plating problems incurred by using a dc source. A pin is available for connecting an external resistance in cases where the fluid impedance is of a different magnitude than that of the internal resistor. When the probe resistance increases above the preset value, the oscillator signal is coupled to the base of the open-collector output transistor. In a typical application, the output could be used to drive a LED, loud speaker or a low current relay.

Features

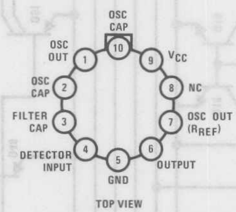
- Low external parts count
- Wide supply operating range
- One side of probe input can be grounded
- ac coupling to probe to prevent plating
- Internally regulated supply
- ac or dc output

Applications

- Beverage dispensers
- Water softeners
- Irrigation
- Sump pumps
- Aquaria
- Radiators
- Washing machines
- Reservoirs
- Boilers

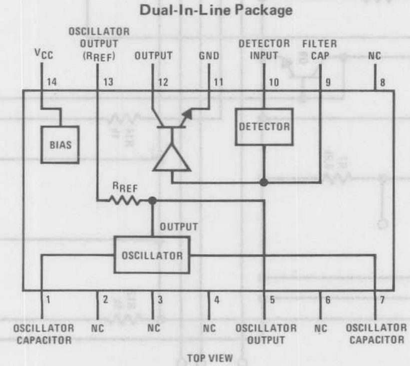
Logic and Connection Diagrams

Metal Can Package



Order Number LM1830H
See NS Package H10C

Dual-In-Line Package



Order Number LM1830N
See NS Package N14A

Absolute Maximum Ratings

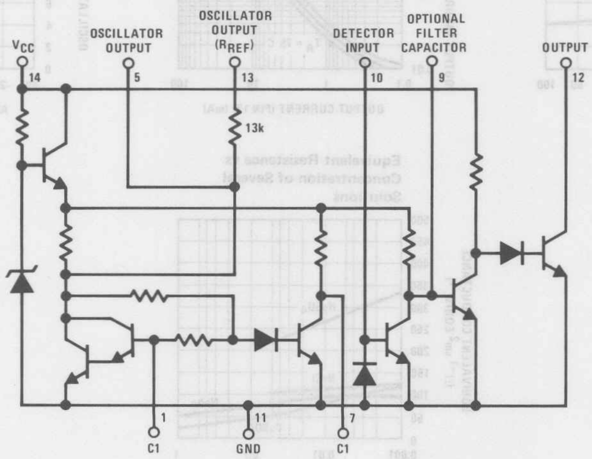
Supply Voltage	28V
Power Dissipation (Note 1)	300 mW
Output Sink Current	20 mA
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−40°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics ($V^+ = 16V$, $T_A = 25°C$ unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current			5.5	10	mA
Oscillator Output Voltage					
Low			1.1		V
High			4.2		V
Internal Reference Resistor		8	13	25	kΩ
Detector Threshold Voltage			680		mV
Detector Threshold Resistance		5	10	15	kΩ
Output Saturation Voltage	$I_O = 10$ mA		0.5	2.0	V
Output Leakage	$V_{PIN\ 12} = 16V$			10	μA
Oscillator Frequency	C1 = 0.001μF	4	7	12	kHz

Note 1: The maximum junction temperature rating of the LM1830N is 150°C. For operation at elevated temperatures, devices in the dual-in-line plastic package must be derated based on a thermal resistance of 175°C/W.

Schematic Diagram



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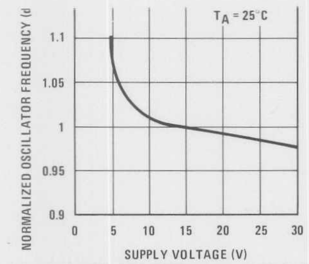
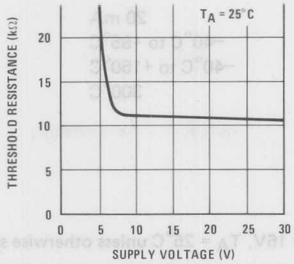
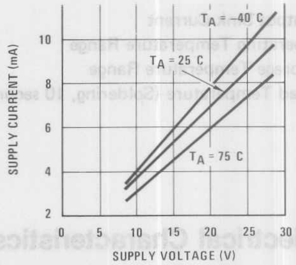
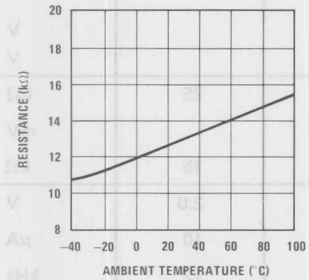


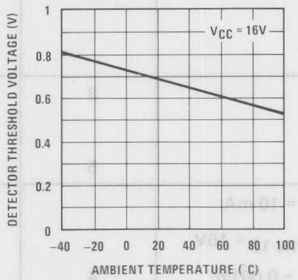




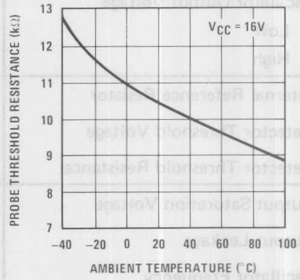
Reference Resistor vs Ambient Temperature



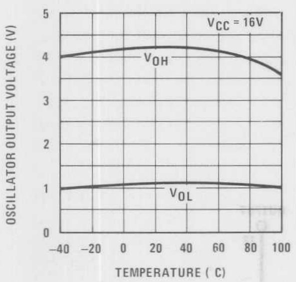
Detector Threshold Voltage vs Temperature



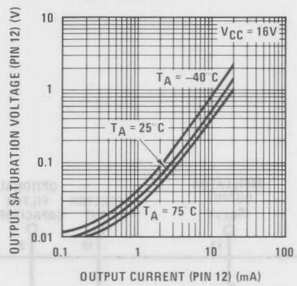
Probe Threshold Resistance vs Temperature



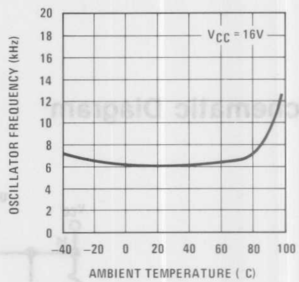
Oscillator V_{OH} and V_{OL} vs Ambient Temperature



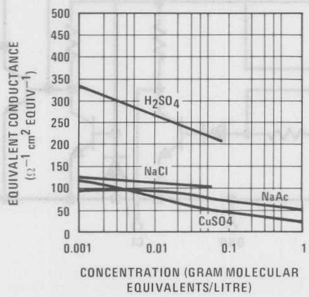
Output Saturation Voltage vs Output Current



Oscillator Frequency vs Ambient Temperature



Equivalent Resistance vs Concentration of Several Solutions



Application Hints

The LM1830 requires only an external capacitor to complete the oscillator circuit. The frequency of oscillation is inversely proportional to the external capacitor value. Using 0.001μF capacitor, the output frequency is approximately 6 kHz. The output from the oscillator is available at pin 5. In normal applications, the output is taken from pin 13 so that the internal 13k resistor can be used to compare with the probe resistance. Pin13 is coupled to the probe by a blocking capacitor so that there is no net dc on the probe.

Since the output amplitude from the oscillator is approximately 4 V_{BE}, the detector (which is an emitter base junction) will be turned "ON" when the probe resistance to ground is equal to the internal 13 kΩ resistor. An internal diode across the detector emitter base junction provides symmetrical limiting of the detector input signal so that the probe is excited with ±2 V_{BE} from a 13 kΩ source. In cases where the 13 kΩ resistor is not compatible with the probe resistance range, an external resistor may be added by coupling the probe to pin 5 through the external resistor as shown in *Figure 2*. The collector of the detecting transistor is brought out to pin 9 enabling a filter capacitor to be connected so that the output will switch "ON" or "OFF" depending on the probe resistance. If this capacitor is omitted, the output will be switched at approximately 50% duty cycle when the probe resistance exceeds the reference resistance. This can be useful when an audio output is required and the output transistor can be used to directly drive a loud speaker. In addition, LED indicators do not require dc excitation. Therefore, the cost of a capacitor for filtering can be saved.

In the case of inductive loads or incandescent lamp loads, it is recommended that a filter capacitor be employed.

In a typical application where the device is employed for sensing low water level in a tank, a simple steel probe may be inserted in the top of the tank with the tank grounded. Then when the water level drops below the tip of the probe, the resistance will rise between the probe and the tank and the alarm will be operated. This is illustrated in *Figure 3*. In situations where a non-conductive container is used, the probe may be designed in a number of ways. In some cases a simple phono plug can be employed. Other probe designs include conductive parallel strips on printed circuit boards.

It is possible to calculate the resistance of any aqueous solution of an electrolyte for different concentrations, provided the dimensions of the electrodes and their spacing is known.

The resistance of a simple parallel plate probe is given by:

$$R = \frac{1000}{c.p} \cdot \frac{d}{A} \ \Omega$$

where A = area of plates (cm^2)
d = separation of plates (cm)
c = concentration (gm. mol. equivalent/litre)
p = equivalent conductance (Ω^{-1} cm^2 equiv.$^{-1}$)

(An equivalent is the number of moles of a substance that gives one mole of positive charge and one mole of negative charge. For example, one mole of NaCl gives Na^+ + Cl^- so the equivalent is 1. One mole of $CaCl_2$ gives Ca^{++} + $2Cl^-$ so the equivalent is 1/2.)

Usually the probe dimensions are not measured physically, but the ratio d/A is determined by measuring the resistance of a cell of known concentration c and equivalent conductance of 1. A graph of common solutions and their equivalent conductances is shown for reference. The data was derived from D.A. MacInnes, "The Principles of Electrochemistry," Reinhold Publishing Corp., New York., 1939.

In automotive and other applications where the power source is known to contain significant transient voltages, the internal regulator on the LM1830 allows protection to be provided by the simple means of using a series resistor in the power supply line as illustrated in *Figure 4*. If the output load is required to be returned directly to the power supply because of the high current required, it will be necessary to provide protection for the output transistor if the voltages are expected to exceed the data sheet limits.

Although the LM1830 is designed primarily for use in sensing conductive fluids, it can be used with any variable resistance device, such as light dependent resistor or thermistor or resistive position transducer.

The following table lists some common fluids which may and may not be detected by resistive probe techniques.

Conductive Fluids	Non-Conductive Fluids
City water	Pure water
Sea water	Gasoline
Copper sulphate solution	Oil
Weak acid	Brake fluid
Weak base	Alcohol
Household ammonia	Ethylene glycol
Water and glycol mixture	Paraffin
Wet soil	Dry soil
Coffee	Whiskey

Application Hints (Continued)

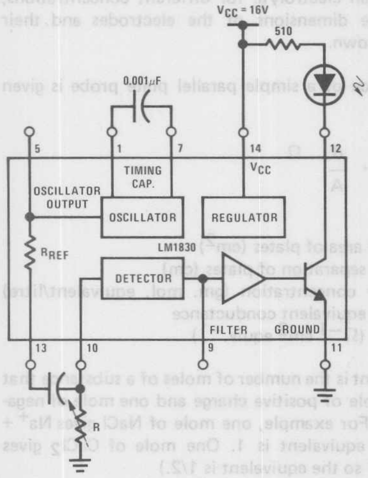


FIGURE 1. Test Circuit

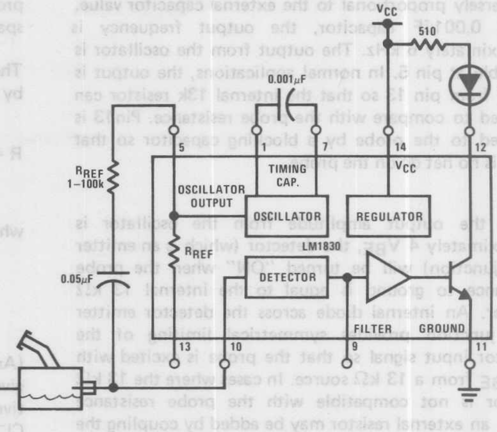


FIGURE 2. Application Using External Reference Resistor

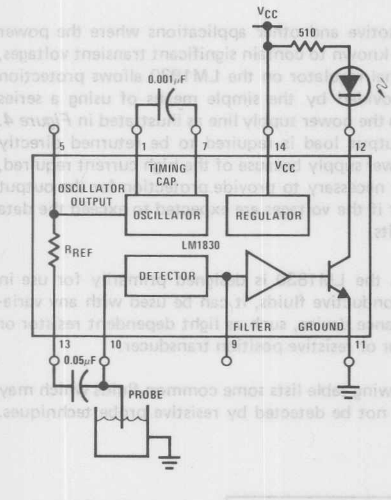
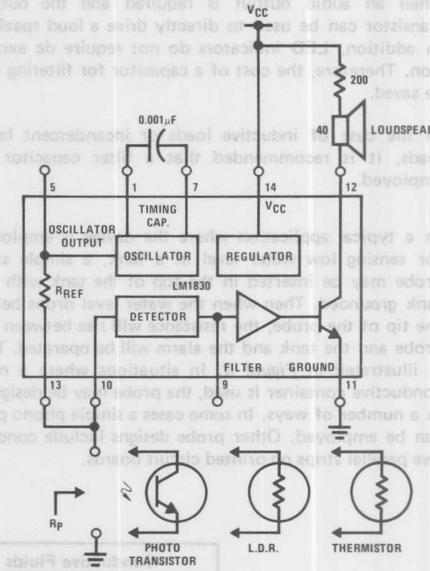


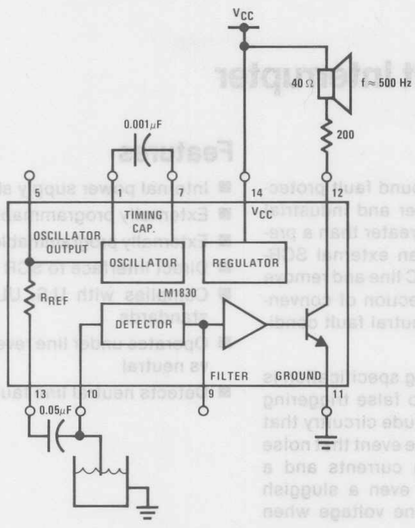
FIGURE 3. Basic Low Level Warning Device with LED Indication



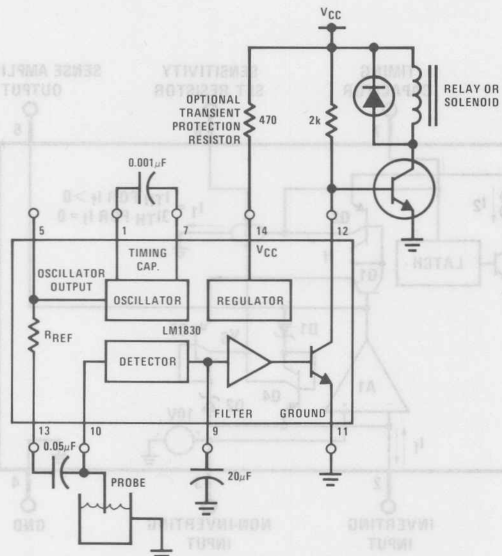
Output is activated when $R_P \gtrsim 1/3\ R_{REF}$

FIGURE 4. Direct Coupled Applications

Typical Applications



Low Level Warning with Audio Output



The output is suitable for driving a sump pump or opening a drain valve, etc.

High Level Warning Device

LM1851 Ground Fault Interrupter

General Description

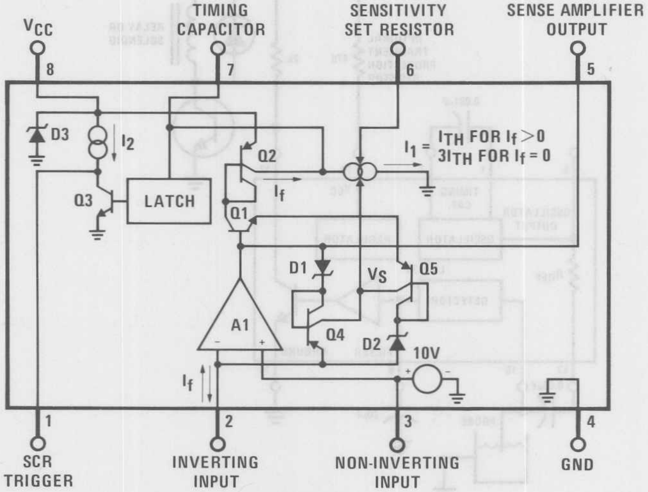
The LM1851 is designed to provide ground fault protection for AC power outlets in consumer and industrial environments. Ground fault currents greater than a presettable threshold value will trigger an external SCR-driven circuit breaker to interrupt the AC line and remove the fault condition. In addition to detection of conventional hot wire to ground faults, the neutral fault condition is also detected.

Full advantage of the U.S. UL943 timing specification is taken to insure maximum immunity to false triggering due to line noise. Special features include circuitry that rapidly resets the timing capacitor in the event that noise pulses introduce unwanted charging currents and a memory circuit that allows firing of even a sluggish breaker on either half-cycle of the line voltage when external full-wave rectification is used.

Features

- Internal power supply shunt regulator
- Externally programmable fault current threshold
- Externally programmable fault current integration time
- Direct interface to SCR
- Complies with U.S. UL943, yet adaptable to other standards
- Operates under line reversal; both load vs line and hot vs neutral
- Detects neutral line faults

Block and Connection Diagram



TOP VIEW

Order Number LM1851N
See NS Package N08B

Absolute Maximum Ratings

Supply Current	19 mA
Power Dissipation (Note 1)	570 mW
Operating Temperature Range	−40°C to +70°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics $T_A = 25°C$, $I_{SS} = 5$ mA

Parameter	Conditions	Min	Typ	Max	Units
Power Supply Shunt Regulator Voltage	Pin 8, Average Value	22	26	30	V
Latch Trigger Voltage	Pin 7	15	17.5	20	V
Sensitivity Set Voltage	Pin 8 to Pin 6	6	7	8.2	V
Output Drive Current	Pin 1, With Fault	0.5	1	2.4	mA
Output Saturation Voltage	Pin 1, Without Fault		100	240	mV
Output Saturation Resistance	Pin 1, Without Fault		100		Ω
Output External Current Sinking Capability	Pin 1, Without Fault, $V_{pin\ 1}$ Held to 0.3V, Note 4	2.0	5		mA
Noise Integration Sink Current Ratio	Pin 7, Ratio of Discharge Currents Between No Fault and Fault Conditions	2.0	2.8	3.6	μA/μA

AC Electrical Characteristics $T_A = 25°C$, $I_{SS} = 5$ mA

Parameter	Conditions	Min	Typ	Max	Units
Normal Fault Current Sensitivity	*Figure 1*, Note 3	3	5	7	mA
Grounded Neutral Fault Resistance Sensitivity	*Figure 2*	3			Ω
Normal Fault Trip Time	500Ω Fault, *Figure 3*, Note 2		18		ms
Normal Fault with Grounded Neutral Fault Trip Time	500Ω Normal Fault, 2Ω Neutral, *Figure 3* Note 2		18		ms

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 125°C maximum junction temperature and a thermal resistance of 175°C/W junction to ambient.

Note 2: Average of 10 trials.

Note 3: Required UL sensitivity tolerance is such that external trimming of LM1851 sensitivity will be necessary.

Note 4: This externally applied current is in addition to the internal "output drive current" source.

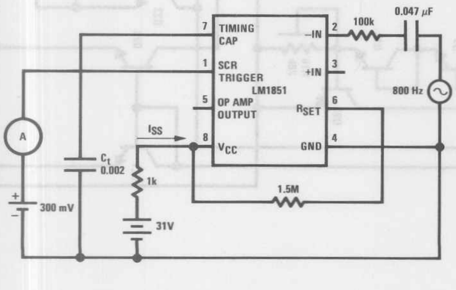


FIGURE 1. Normal Fault Sensitivity Test Circuit

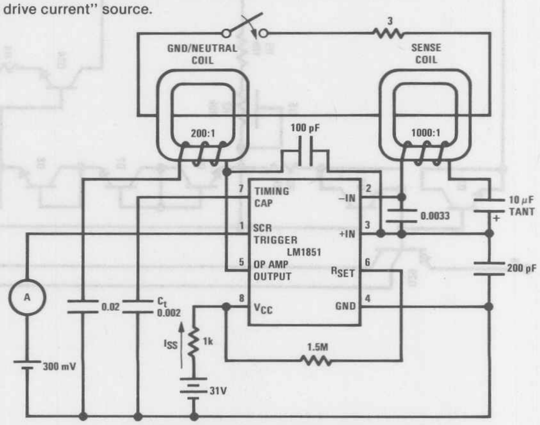
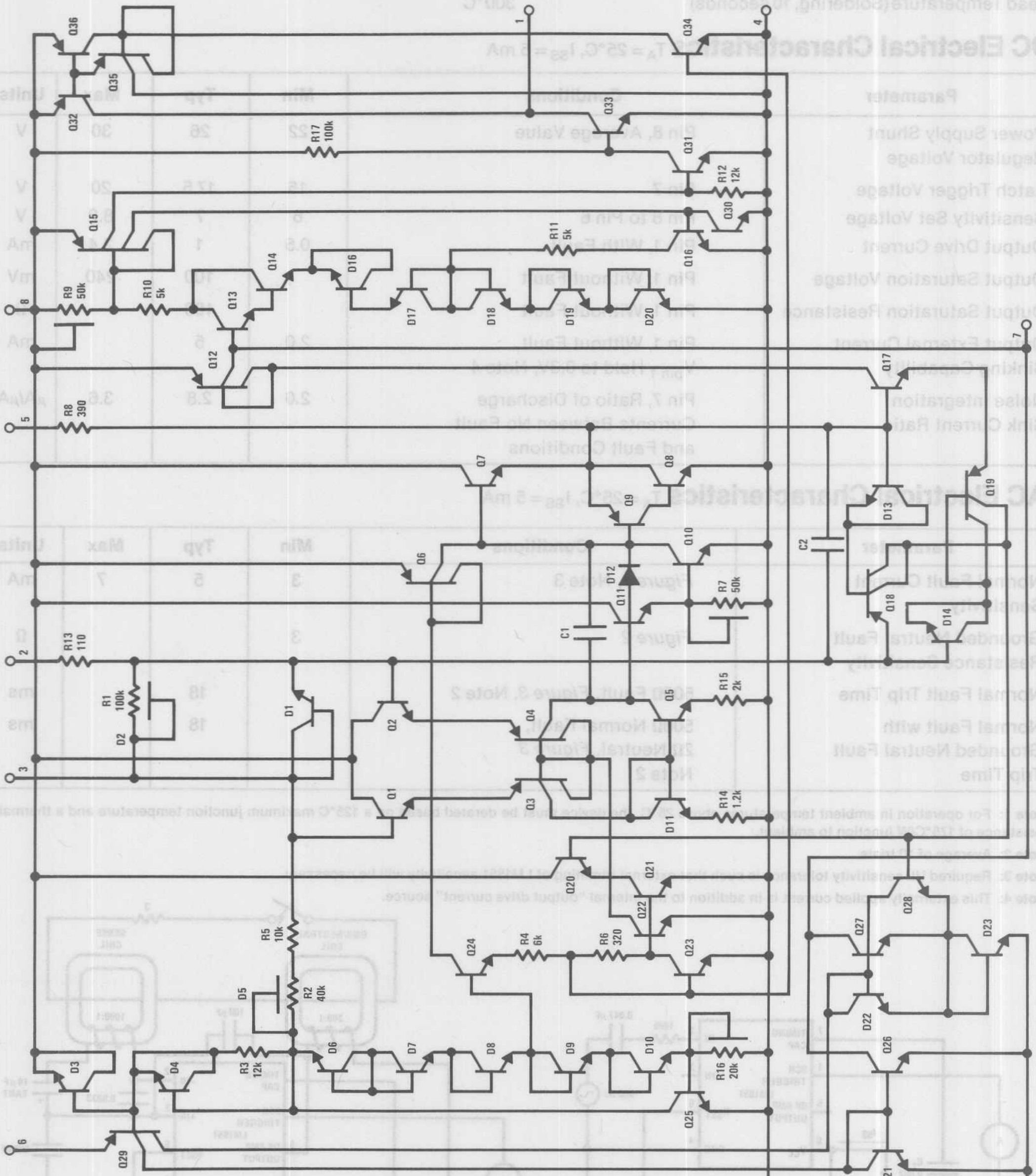


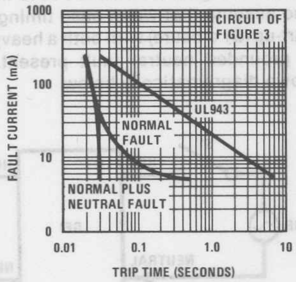
FIGURE 2. Grounded Neutral Fault Sensitivity Test Circuit

Internal Schematic Diagram

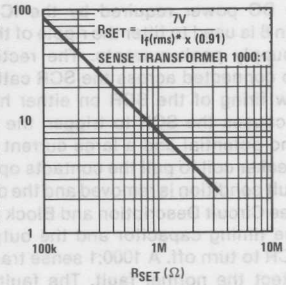


Typical Performance Characteristics

Average Trip Time vs Fault Current

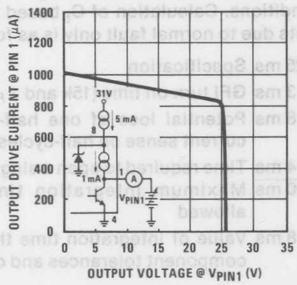


Normal Fault Current Threshold vs R_{SET}

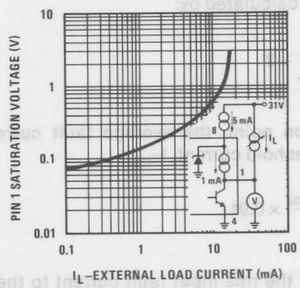


* See Block Diagram

Output Drive Current vs Output Voltage



Pin 1 Saturation Voltage vs External Load Current, I_L



Circuit Description

(Refer to Block and Connection Diagram)

The LM1851 operates from 26V as set by an internal shunt regulator, D3. In the absence of a fault ($I_f = 0$) the feedback path status signal (V_S) is correspondingly zero. Under these conditions the capacitor discharge current, I_1, sits quiescently at three times its threshold value, I_{TH}, so that noise induced charge on the timing capacitor will be rapidly removed. When a fault current, I_f, is induced in the secondary of the external sense transformer, the operational amplifier, A1, uses feedback to force a virtual ground at the input as it extracts I_f. The presence of I_f during either half-cycle will cause V_S to go high, which in turn changes I_1 from $3I_{TH}$ to I_{TH}. Although I_{TH} discharges the timing capacitor during both half-cycles of the line, I_f only charges the capacitor during the half-cycle in which I_f exits pin 2. Thus during one half-cycle $I_f - I_{TH}$ charges the timing capacitor, while during the other half-cycle I_{TH} discharges it. When the capacitor voltage reaches 17.5V, the latch engages and turns off Q3 permitting I_2 to drive the gate of an SCR.

Typical ground fault interrupter circuits are shown in *Figures 3 and 4.* They were both designed to operate on 120V AC line voltage with 5 mA normal fault sensitivity, and differ only in the technique used for grounded neutral detection. The "dormant oscillator" approach of *Figure 3* will be used as a design example.

A full-wave rectifier bridge and a 15k/2W resistor are used to supply the DC power required by the IC. A 1 μF capacitor at pin 8 is used to filter the ripple of the supply voltage and supply peak currents. The rectified line voltage is also connected across the SCR cathode and anode to allow firing of the SCR on either half-cycle. When a fault causes the SCR to trigger, the anode is taken to ground potential and a large current can flow through the breaker coil to pull the contacts open. Once opened, the fault condition is removed and the discharge current $3I_{TH}$ (see Circuit Description and Block Diagram) resets both the timing capacitor and the output latch causing the SCR to turn off. A 1000:1 sense transformer is used to detect the normal fault. The fault current, which is basically the difference current between the hot and neutral lines, is stepped down by 1000 and fed into the input pins of the operational amplifier through a 10 μF capacitor. The 0.0033 μF capacitor between pin 2 and pin 3 and the 200 pF between pins 3 and 4 are added to obtain better noise immunity. The normal fault sensitivity is determined by the timing capacitor discharging current, I_{TH}. I_{TH} can be calculated by:

$$I_{TH} = \frac{7V}{R_{SET}} \div 2 \qquad (1)$$

At the decision point, the average fault current just equals the threshold current, I_{TH}.

$$I_{TH} = \frac{I_{f(rms)}}{2} \times 0.91 \qquad (2)$$

where $I_{f(rms)}$ is the rms input fault current to the operational amp and the factor of 2 is due to the fact that I_f charges the timing capacitor only during one half-cycle, while I_{TH} discharges the capacitor continuously. The factor 0.91 converts the rms value to an average value. Combining equations (1) and (2) we have

$$R_{SET} = \frac{7V}{I_{f(rms)} \times 0.91} \qquad (3)$$

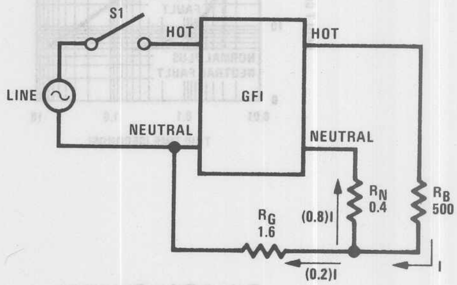
For example, to obtain 5 mA(rms) sensitivity for the circuit in *Figure 3* we have:

$$R_{SET} = \frac{7V}{\left(\frac{5\text{ mA} \times 0.91}{1000}\right)} = 1.5\text{ M}\Omega \qquad (4)$$

The correct value for R_{SET} can also be determined from the characteristic curve that plots equation (3). Note that this is an approximate calculation, the exact value of R_{SET} depends on the specific sense transformer used and LM1851 tolerances. Inasmuch as UL943 specifies a sensitivity "window" of 4 mA–6 mA, provision should be made to adjust R_{SET} on a per-product basis.

Independent of setting sensitivity, the desired integration time can be obtained through proper selection of the timing capacitor, C_t. Due to the large number of variables involved, proper selection of C_t is best done empirically. The following design example, then, should only be used as a guideline.

Assume the goal is to meet UL943 timing requirements. Also assume that worst case timing occurs during GFI start-up (S1 closure) with both a heavy normal fault and a 2Ω grounded neutral fault present. This situation is shown diagramatically below.



UL943 specifies ≤25 ms average trip time under these conditions. Calculation of C_t based upon charging currents due to normal fault only is as follows:

≤25 ms	Specification
−3 ms	GFI turn-on time (15k and 1 μF)
−8 ms	Potential loss of one half-cycle due to fault current sense on half-cycles only
−4 ms	Time required to open a sluggish circuit breaker
≤10 ms	Maximum integration time that could be allowed
8 ms	Value of integration time that accommodates component tolerances and other variables

$$C_t = \frac{I \times T}{V} \qquad (5)$$

where T = integration time
V = threshold voltage

I = average fault current into C_t

$$I = \underbrace{\left(\frac{120\text{ VAC(rms)}}{R_B}\right)}_{\substack{\text{heavy fault}\\ \text{current generated}\\ \text{(swamps } I_{TH})}} \times \underbrace{\left(\frac{R_N}{R_G + R_N}\right)}_{\substack{\text{portion of}\\ \text{fault current}\\ \text{shunted}\\ \text{around GFI}}}$$

$$\times \underbrace{\left(\frac{1\text{ turn}}{1000\text{ turns}}\right)}_{\substack{\text{current}\\ \text{division of}\\ \text{input sense}\\ \text{transformer}}} \times \underbrace{\left(\frac{1}{2}\right)}_{\substack{C_t\text{ charging}\\ \text{on half-}\\ \text{cycles only}}} \times \underbrace{(0.91)}_{\substack{\text{rms to}\\ \text{average}\\ \text{conversion}}} \qquad (6)$$

Application Circuits (Continued)

therefore:

$$C_t = \frac{\left[\left(\frac{120}{500}\right) \times \left(\frac{0.4}{1.6 + 0.4}\right) \times \left(\frac{1}{1000}\right) \times \left(\frac{1}{2}\right) \times (0.91)\right] \times 0.008}{17.5} \tag{7}$$

$$C_t = 0.01\ \mu F$$

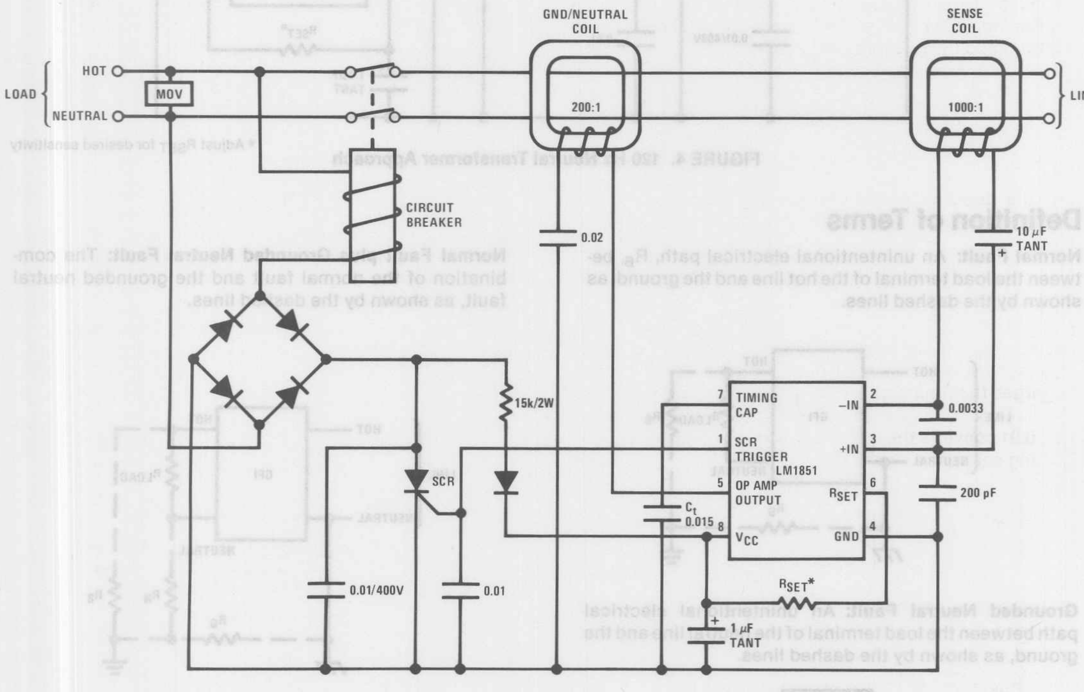
In practice, the actual value of C_t will have to be modified to include the effects of the neutral loop oscillation upon the net charging current. The effect of neutral loop induced currents is difficult to quantize, but typically they sum with normal fault currents, thus allowing a larger value of C_t. For UL943 requirements, 0.015 μF has been found to be the best compromise between timing and noise.

For those GFI standards not requiring grounded neutral detection, a still larger value of capacitor can be used and better noise immunity obtained. The larger capacitor can be accommodated because R_N and R_G are not present, allowing the full fault current, I, to enter the GFI.

The sense amplifier is capacitively coupled to a 200-turn coil in order to detect the grounded neutral fault. Choice of proper coil polarities causes a positive feedback loop to close in the presence of a low resistance grounded neutral fault and results in oscillation of the input amplifier. The timing capacitor receives charging current due to rectification of the oscillatory feedback currents caused by Q1 (see Block Diagram) only conducting on one half-cycle of the line. Eventually the capacitor voltage reaches threshold and the SCR is triggered.

In *Figure 4,* grounded neutral detection is accomplished by feeding the neutral coil with 120 Hz energy continuously and allowing some of this energy to couple into the sense transformer during conditions of neutral fault.

Typical Applications



* Adjust R_{SET} for 5 mA sensitivity

FIGURE 3. Dormant Oscillator Approach

Typical Applications (Continued)

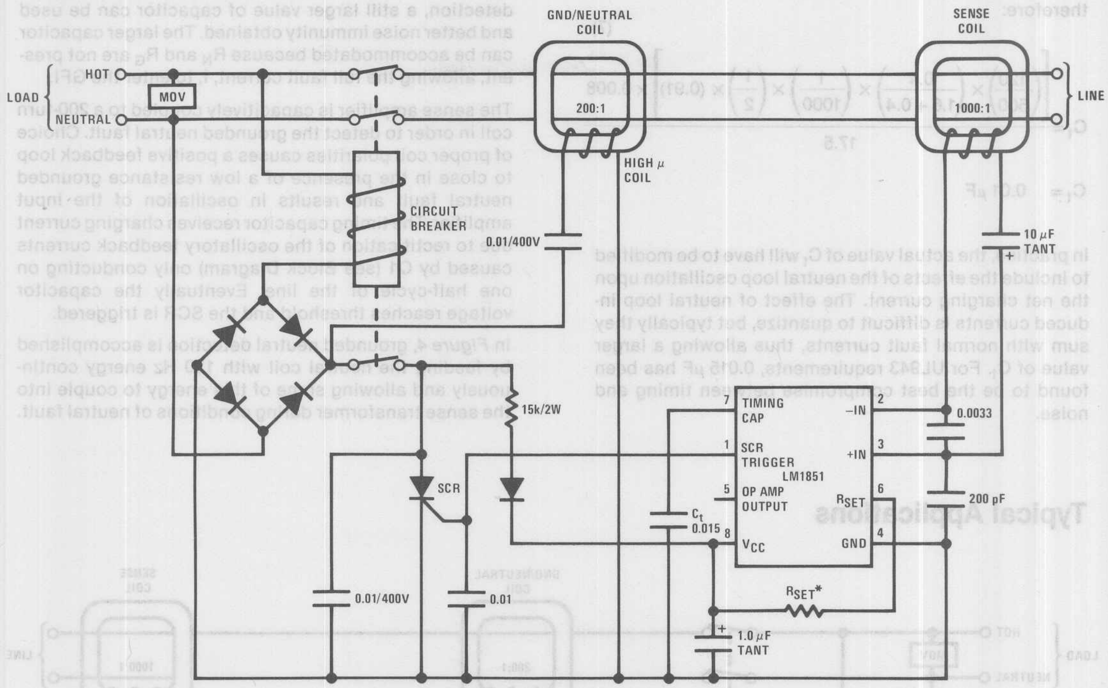
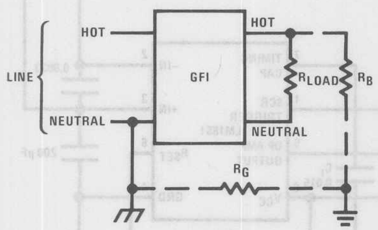


FIGURE 4. 120 Hz Neutral Transformer Approach

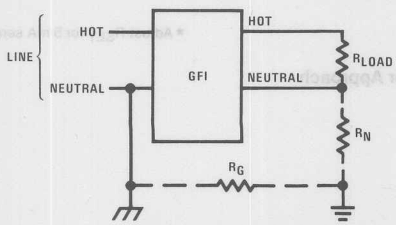
* Adjust R_{SET} for desired sensitivity

Definition of Terms

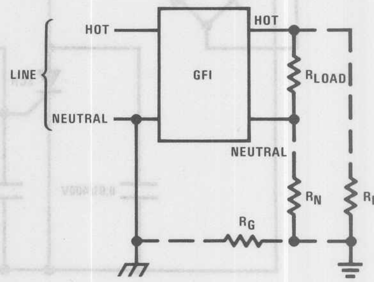
Normal Fault: An unintentional electrical path, R_B, between the load terminal of the hot line and the ground, as shown by the dashed lines.



Grounded Neutral Fault: An unintentional electrical path between the load terminal of the neutral line and the ground, as shown by the dashed lines.



Normal Fault plus Grounded Neutral Fault: The combination of the normal fault and the grounded neutral fault, as shown by the dashed lines.



National Semiconductor

Industrial Blocks

LM1871 RC Encoder/Transmitter

General Description

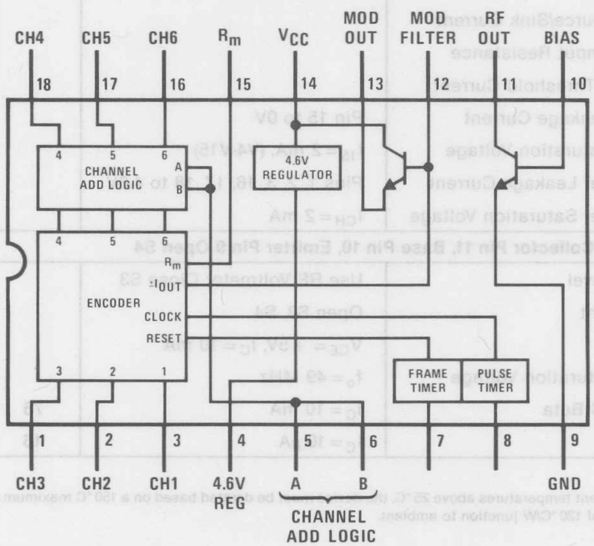
The LM1871 is a complete six-channel digital proportional encoder and RF transmitter intended for use as a low power, non-voice, unlicensed communication device at carrier frequencies of 27 MHz or 49 MHz with a field strength of 10,000 μV/meter at 3 meters. In addition to radio controlled hobby, toy and industrial applications, the encoder section can provide a serial input of six words for hard wired, infra-red or fiber optic communication links. Channel add logic is provided to control the number of encoded channels from three to six, allowing increased design flexibility. When used with the LM1872 RC receiver/decoder, a low cost RF linked encoder and decoder system provides two analog and two ON/OFF decoded channels.

Features

- Low current 9V battery operation
- On-chip RF oscillator/transmitter
- One timing capacitor for six proportional channels
- Programmable number of channels
- Regulated RF output power
- External modulator bandwidth control
- On-chip 4.6V regulator
- Up to 80 MHz carrier frequency operation

Block and Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number LM1871N
See NS Package N18A

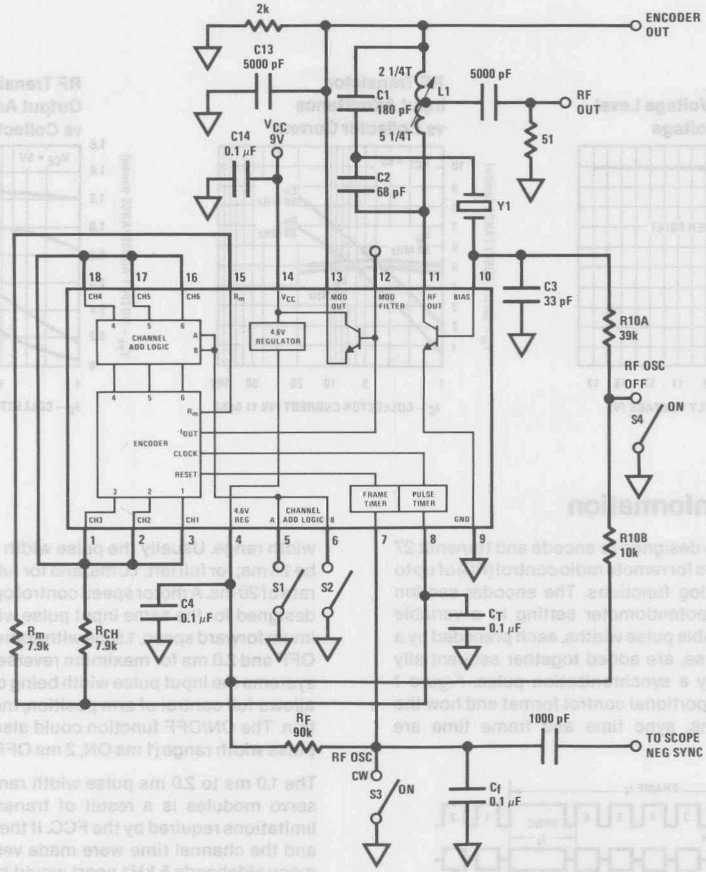
DC Current Out of Pin 13	25 mA
Package Dissipation (Note 1)	1.0W
Pin 4 Externally Forced	6V
Operating Temperature Range	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics $T_A = 25°C$, $V_{CC} = +9V$, see Test Circuit and Waveforms

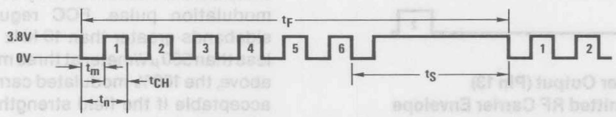
	Parameter	Conditions	Min	Typ	Max	Units
Encoder Section, Close S1, S2, S4 Open S3						
V14	Supply Voltage		4.5	9	15	V
I_{14}	Supply Current	Encoder Only	10	14	22	mA
V4	Reference Voltage		4.1	4.6	5.1	V
t_f	Frame Time	$t_f = R_F C_F + 0.63 R_{MOD} C_T$	8	9.5	10.5	ms
t_m	Mod Time	$t_m = 0.63 R_{MOD} C_T$	0.4	0.5	0.6	ms
t_{ch}	Channel Time	$t_{ch} = 0.63 R_{CH} C_T$	0.4	0.5	0.6	ms
t_s	Sync Time, T_x Channels 1-6	Close S1, Close S2		3.5		ms
t_s	Sync Time, T_x Channels 1-5	Open S1, Close S2		4.5		ms
t_s	Sync Time, T_x Channels 1-4	Close S1, Open S2		5.5		ms
t_s	Sync Time, T_x Channels 1-3	Open S1, Open S2		6.5		ms
Δt_n	Supply Rejection, $t_m + t_{CH}$	ΔV_{CC} 6V to 12V		0.1		%/V
ΔV13	Encoder Output Swing			3.8		V_{p-p}
ΔV12	Mod Filter Output Swing			3.8		V_{p-p}
I_{12}	Mod Filter Source/Sink Current			0.5		± mA
$R_{IN(8)}$	Pulse Timer Input Resistance			27		MΩ
$I_{TH(7)}$	Frame Timer Threshold Current			0.1		μA
$I_{LEAK(15)}$	Mod Timer Leakage Current	Pin 15 to 0V		0.01	1	μA
$V_{SAT(15)}$	Mod Timer Saturation Voltage	$I_{15} = 2$ mA, (V4-V15)		120	240	mV
$I_{LEAK(CH)}$	Channel Timer Leakage Current	Pins 1, 2, 3, 16, 17, 18 to 4.6V		0.06	1	μA
$V_{SAT(CH)}$	Channel Timer Saturation Voltage	$I_{CH} = 2$ mA		120	240	mV
RF Oscillator Section, Collector Pin 11, Base Pin 10, Emitter Pin 9 Open S4						
V_{OUT}	RF Output Level	Use RF Voltmeter Close S3		400		mV_{RMS}
I_{14}	Supply Current	Open S3, S4		30		mA
f_t	Transistor	$V_{CE} = +5V$, $I_C = 10$ mA		520		MHz
$V_{SAT(11)}$	Transistor Saturation Voltage	$f_o = 49$ MHz		800		mV
H_{FE}	Transistor DC Beta	$I_C = 10$ mA	75	150	300	
LV_{CEO}		$I_C = 10\ \mu A$	16	20		V

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a package thermal resistance of 120°C/W junction to ambient.

Test Circuit and Switching Time Waveforms



Note: Test circuit has been configured for evaluation by oscilloscope. Use 1% timing components. R_M, R_{CH}, R_F, C_T



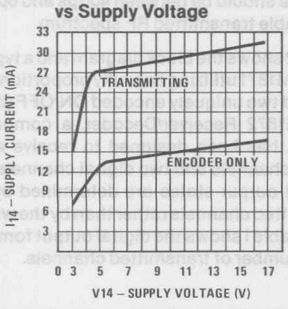
L1: Toko E523LN-7210019 type MC117 7 1/2 turns with tap 2 1/4 turns from top

Y1: 49.86 MHz crystal 3rd overtone

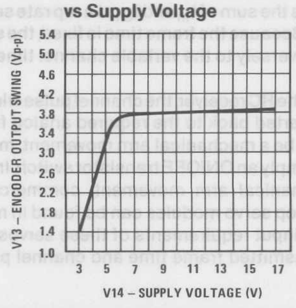
Encoder output (pin 13) close S1, S2, S4, 0.5 ms/div sweep

Typical Performance Characteristics

Supply Current vs Supply Voltage

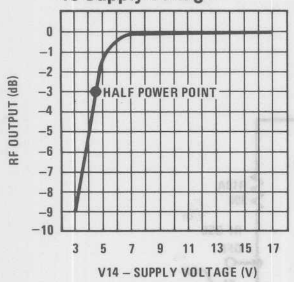


Encoder Output Swing vs Supply Voltage

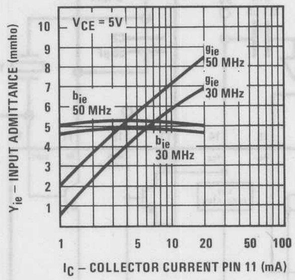


Typical Performance Characteristics (Continued)

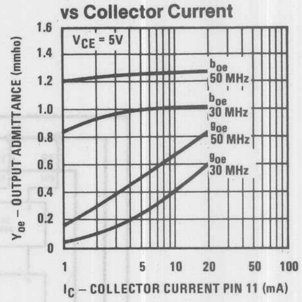
RF Output Voltage Level vs Supply Voltage



RF Transistor Input Admittance vs Collector Current



RF Transistor Output Admittance vs Collector Current



Applications Information

The LM1871 has been designed to encode and transmit 27 MHz or 49 MHz carriers for remote radio control (RC) of up to six independent analog functions. The encoder section converts a variable potentiometer setting to a variable pulse width. The variable pulse widths, each preceded by a fixed modulation pulse, are added together sequentially and then followed by a synchronization pulse. *Figure 1* shows the digital proportional control format and how the channel pulse widths, sync time and frame time are defined.

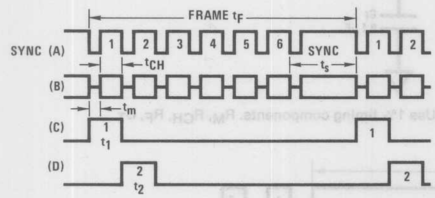


FIGURE 1. (A) Encoder Output (Pin 13)
(B) Transmitted RF Carrier Envelope
(C) Typical Receiver Channel 1 Output
(D) Typical Receiver Channel 2 Output

Figure 1 (A) shows the encoder output waveform. The modulation time (t_m) is fixed while the channel time (t_{ch}) is the variable pulse width. In *Figure 1* (C, D) the recovered channel pulse (t_n) is the sum of t_m and t_{ch} at a rep rate set by the frame time (t_f). Because the frame time is fixed, the sync time (t_s) will vary inversely to the variable channel times.

After detection by the RC receiver, the channel pulse widths must now be converted back to the required analog functions, which might be a mechanical arm movement, motor speed control or simply an ON/OFF transistor switch. In the case of the mechanical arm movement, commercially available closed loop servo modules can be found in most hobby shops. The input requirements of these servos will determine the transmitted frame time and channel pulse width range. Usually the pulse width for arm at center will be 1.5 ms; for full left, 1.0 ms; and for full right, 2.0 ms, at a rep rate of 20 ms. A motor speed control open loop servo can be designed for the same input pulse widths: 1.0 ms for maximum forward speed, 1.5 ms with some dead band for motor OFF and 2.0 ms for maximum reverse speed. In both servo systems the input pulse width being continuously variable allows full control of arm position, motor speed and direction. The ON/OFF function could also use the same input pulse width range (1 ms ON, 2 ms OFF).

The 1.0 ms to 2.0 ms pulse width range required by most servo modules is a result of transmitted RF spectrum limitations required by the FCC. If the modulation time (t_m) and the channel time were made very short (≅10μs each) many sidebands 5 kHz apart would be generated on each side of the center frequency. The amplitude and number of sidebands are determined by the depth and duration of the modulation pulse. FCC regulations require that all sidebands greater than 10 kHz from center frequency be less than 500μV/meter at three meters. In the example cited above, the 100% modulated carrier spectrum would not be acceptable if the field strength of the carrier was 10,000 μV/meter at three meters. If the modulation and channel times were made much longer (≅10 ms each) the transmitted spectrum would be acceptable but now the frame time would be longer than desirable for optimum servo designs. When the received channel pulse widths are between 1.0 ms and 2.0 ms at a frame rate of 20 ms the modulation time should be between 400 μs and 600 μs to insure an acceptable transmitted RF spectrum.

Figure 2 shows the block diagram and a typical application of the LM1871 utilizing two fully proportional (analog) channels and two uniquely encoded ON/OFF (digital) channels. The LM1872 Receiver/Decoder, a companion IC to the LM1871, has been designed to receive and decode two analog channels and two digital channels. The two digital channel output states are determined by the number of transmitted channels rather than by the width of a channel pulse. Table I shows the digital output format as a function of the number of transmitted channels.

Applications Information (Continued)

Note: See *Figure 4* for RF components.

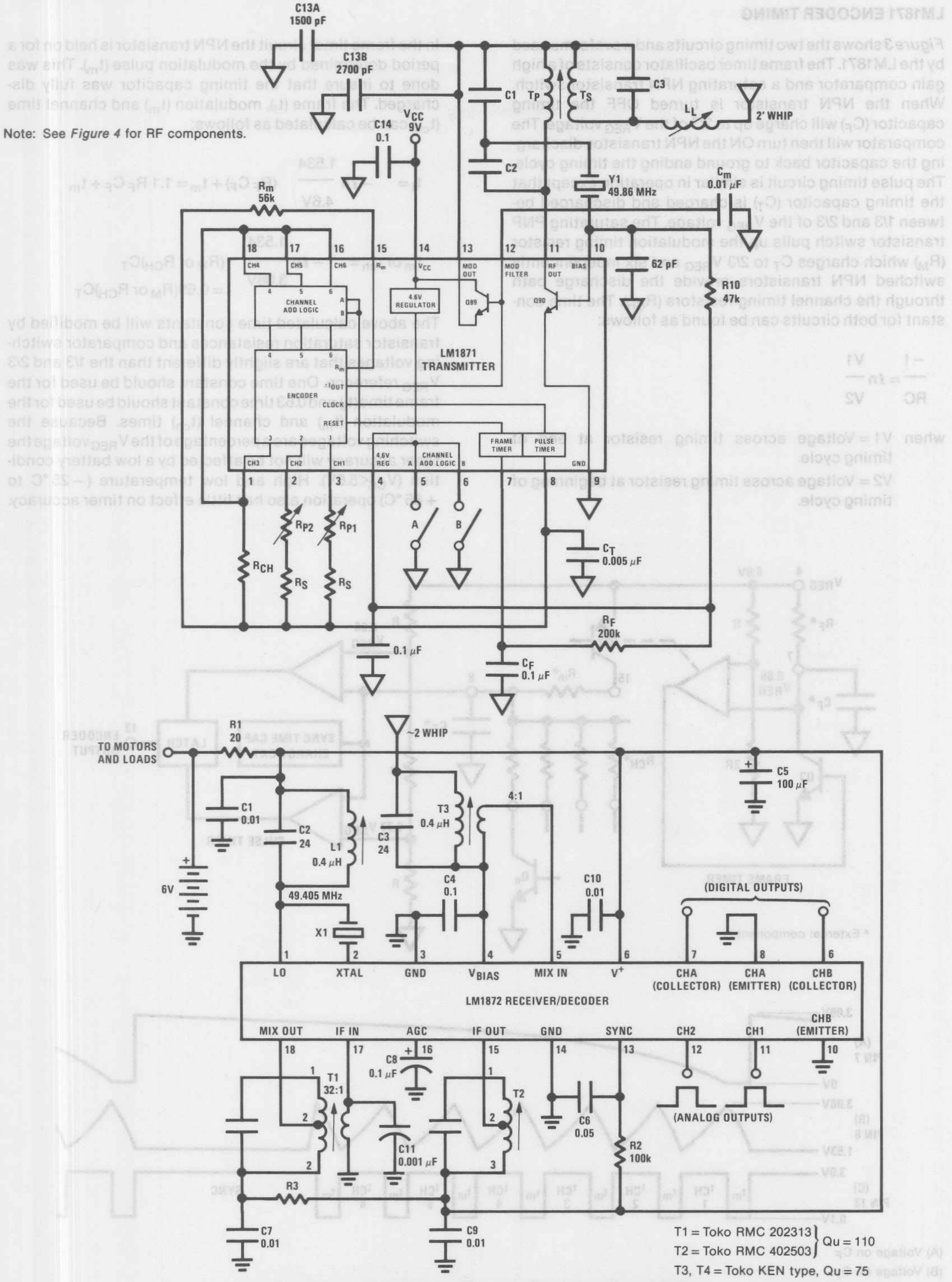


FIGURE 2. Two Channel Analog/Two Channel Digital Transmitter/Receiver Application

Figure 3 shows the two timing circuits and waveforms used by the LM1871. The frame timer oscillator consists of a high gain comparator and a saturating NPN transistor switch. When the NPN transistor is turned OFF the timing capacitor (C_F) will charge up to 2/3 of the V_{REG} voltage. The comparator will then turn ON the NPN transistor, discharging the capacitor back to ground ending the timing cycle. The pulse timing circuit is similar in operation except that the timing capacitor (C_T) is charged and discharged between 1/3 and 2/3 of the V_{REG} voltage. The saturating PNP transistor switch pulls up the modulation timing resistor (R_M) which charges C_T to 2/3 V_{REG} and six independently switched NPN transistors provide the discharge path through the channel timing resistors (R_{CH}). The time constant for both circuits can be found as follows:

$$\frac{-t}{RC} = \ell n \frac{V1}{V2}$$

when V1 = Voltage across timing resistor at end of timing cycle.

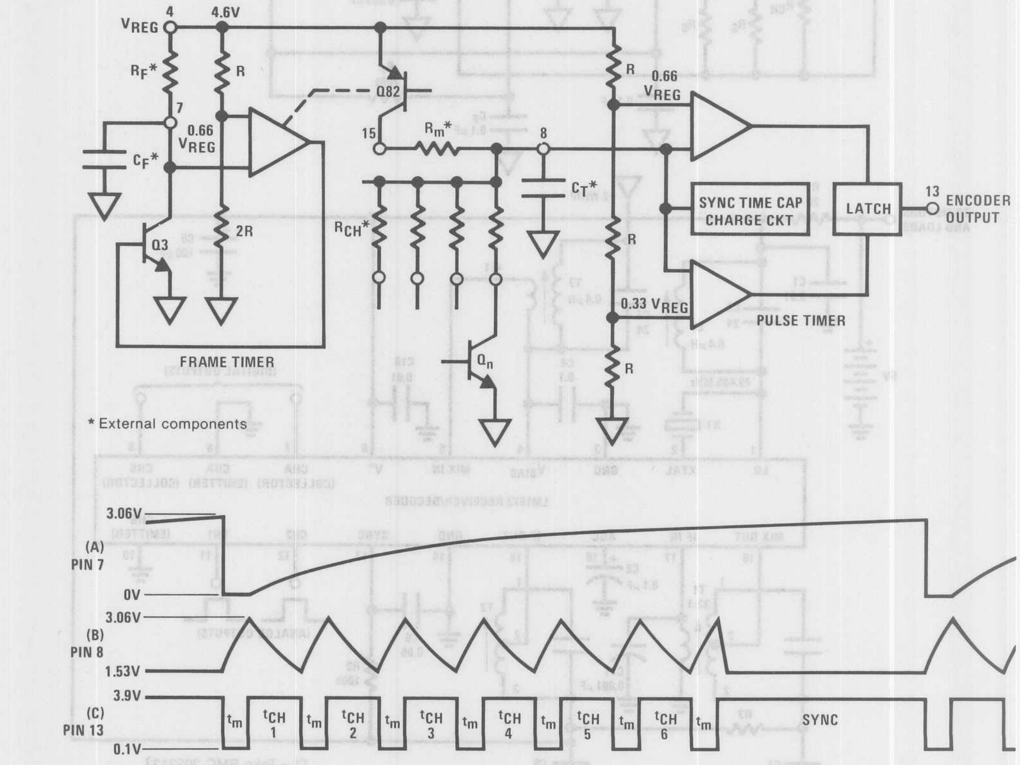
V2 = Voltage across timing resistor at beginning of timing cycle.

In the frame timer circuit the NPN transistor is held on for a period determined by the modulation pulse (t_m). This was done to insure that the timing capacitor was fully discharged. The frame (t_f), modulation (t_m) and channel time (t_{ch}) can be calculated as follows:

$$t_f = -\ell n \frac{1.534}{4.6V} (R_F C_F) + t_m = 1.1\, R_F C_F + t_m$$

$$t_m \text{ or } t_{ch} = -\ell n \frac{1.534}{3.06V} (R_M \text{ or } R_{CH})C_T = 0.69(R_M \text{ or } R_{CH})C_T$$

The above calculated time constants will be modified by transistor saturation resistances and comparator switching voltages that are slightly different than the 1/3 and 2/3 V_{REG} reference. One time constant should be used for the frame time (t_f) and 0.63 time constant should be used for the modulation (t_m) and channel (t_{ch}) times. Because the switching voltages are a percentage of the V_{REG} voltage the timer accuracy will not be affected by a low battery condition (V_{CC}<5.6V). High and low temperature (−25°C to +85°C) operation also has little effect on timer accuracy.



(A) Voltage on C_F
(B) Voltage on C_T
(C) Encoder pulse train output

FIGURE 3. Simplified Encoder Timing Circuits and Waveforms

Applications Information (Continued)

The accuracy and temperature characteristics of the external components will determine the total accuracy of the system. The capacitors should be NPO ceramics or other low-drift types.

As an example the following procedure can be used to determine the external timing components required for *Figure 2*.

Given: Frame time (t_f) = 20 ms
Modulation time (t_m) = 500 μs
Recovered pulse width (t_n) range = 1.0 ms to 2.0 ms with trim capability
Non variable channel pulse width (t_n) = 1.0 ms

1. Frame Timer Components

Choose $C_F = 0.1\ \mu F \pm 10\%$

$$R_F = \frac{t_f - t_m}{C_T} = \frac{20\text{ ms} - 0.50\text{ ms}}{0.1\ \mu F} = 195\text{ k}\Omega\ (200\text{ k}\Omega)$$

2. Modulation Time Components

Choose $C_T = 0.01\ \mu F \pm 10\%$

$$R_M = \frac{t_m}{0.63C_T} = \frac{500 \times 10^{-6}}{(0.63)(1 \times 10^{-8})} = 79.36\text{ k}\Omega\ (82\text{ k}\Omega)$$

3. Non-Variable Channel (3 through 6) Component

$t_{ch} = t_n - t_m = 1.0\text{ ms} - 0.50\text{ ms} = 500\ \mu s$

$$R_{CH} = \frac{t_{ch}}{0.63C_T} = \frac{500 \times 10^{-6}}{(0.63)(1 \times 10^{-8})} = 79.36\text{ k}\Omega\ (82\text{k})$$

4. Variable Channel 1 (t1) and Channel 2 (t2) Components

When the R_P wiper arm varies across the full potentiometer range, ($\Delta R = 0\Omega$ to R_P value) R_S is found for 0Ω and minimum t_n pulse width.

$$R_S = \frac{t_n - t_m}{0.63C_T} = \frac{1\text{ ms} - 0.50\text{ ms}}{(0.63)(1 \times 10^{-8})} = 79.36\text{ k}\Omega\ (82\text{k})$$

$R_P(\Delta R)$ is found for maximum t_n pulse width.

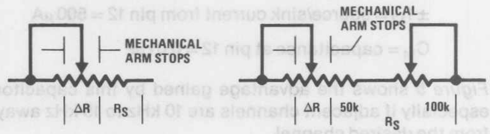
$$R_P = \frac{t_n - t_m}{0.63C_T} - R_S = \frac{2\text{ ms} - 0.50\text{ ms}}{(0.63)(1 \times 10^{-8})} - 82\text{ k}\Omega = 156\text{ k}\Omega$$

The R_P value could have been chosen first and a C_T calculated. Usually the 270° to 320° angle of potentiometer rotation is inconvenient especially if it is desired to spring return the control to center, or if lever type knobs are required. A 500 kΩ potentiometer that has 300° of end to end wiper arm rotation could be used if mechanical stops limit this range.

$$\text{Required angle of rotation} = \frac{(300°)(156\text{ k}\Omega)}{500\text{ k}\Omega} = 93.6°$$

In most applications the resistor and capacitor tolerances prevent sufficient system accuracy without mechanical or electrical trimming of the analog channel pulse widths. If a 500k potentiometer is used, two trim methods can be utilized. R_S can also be included as part of the potentiometer resistance.

Rotate Potentiometer Body for Mechanical Trim **Adjust R_S Potentiometer for Electrical Trim**



$\Delta R = 156\text{ k}\Omega$, $R_S = 82\text{ k}\Omega$

If $t_n = 1.5\text{ ms} \pm 30\%$ is required:

$$\pm R_{TRIM} = 0.3\ \frac{\Delta R}{2} + R_S = 48\text{ k}\Omega$$

$$\text{Required Body Rotation} = \frac{(300°)(48\text{k})}{500\text{k}} = \pm 28.8°$$

Channel Add Logic

Table I shows the number of transmitted channels as a function of pin 5 and pin 6 conditions. The threshold voltage for both pins is ≅0.7V. When grounded, the pins are sourcing ≅300 μA from the internal pull up resistors. External voltages may be applied to these pins but should be below the V_{REG} voltage by at least one volt and not less than the pin 9 ground.

TABLE I. DIGITAL CHANNEL OUTPUT FORMAT AS A FUNCTION OF TRANSMITTED CHANNELS

LM1871 Channel Add Logic Pin Conditions		Number of Channels Transmitted	LM1872 Receiver Digital Outputs	
Pin 5 (A)	Pin 6 (B)		A	B
OPEN	OPEN	3	OFF	OFF
GND	OPEN	4	ON	OFF
OPEN	GND	5	OFF	ON
GND	GND	6	ON	ON

Applications Information (Continued)

Modulator and Crystal Oscillator/Transmitter Circuit (*Figure 4*)

The modulator and oscillator consist of but two NPN transistors whose operation is quite straightforward. The base of the modulator transistor is driven by a bidirectional current source with the voltage range for the high condition limited by a saturating PNP collector to the pin 4 V_{REG} voltage and low condition limited by a saturating NPN collector in series with a diode to ground. A current source of $\pm 500\ \mu A$ was chosen to provide a means for external modulator bandwidth control. When a capacitor is used at this node the transmitted RF carrier is made to slew ON and OFF at a time determined by:

Modulation slew time (t_{ms})

$$= \frac{(\Delta V12)(C_M)}{I_{12}} = \frac{(3.8V)(0.01\ \mu F)}{500\ \mu A} = 76\ \mu s$$

when $\Delta V12$ = peak to peak voltage swing of pin 12 = 3.8V

$\pm I_{12}$ = source/sink current from pin 12 = 500 μA

C_M = capacitance at pin 12 = 0.01 μF

Figure 5 shows the advantage gained by this capacitor especially if adjacent channels are 10 kHz to 15 kHz away from the desired channel.

The crystal oscillator/transmitter transistor is configured to oscillate in a class C mode with the conduction angle being approximately 140° to 160°. Resistor R10 provides the base bias current from the pin 4 V_{REG} voltage. This resistor value has been optimized for most RC applications. When the emitter of the modulation transistor is high (≅3.8V) the collector and tank coil are pulled up into the active range of the oscillator transistor. RF feedback to the base is via the series mode crystal which determines the oscillator frequency. Because third overtone crystals are used for 27 MHz or 49 MHz applications a tuned collector load must be used to guarantee operation at the correct frequency. Tuning the LC tank, while having little effect on oscillator frequency, will control the conduction angle and oscillator efficiency. Tuning the LC tank for minimum V_{CC} supply current while observing the carrier envelope on an oscilloscope would be the best alignment method.

For most RC applications the carrier ON to OFF ratio must be as high as possible to ensure precise pulse width detection at the receiver. If we were to look at the base of the oscillator transistor we would see that the crystal is still oscillating during the time that the carrier is OFF (t_m). This is because of the high Q characteristic (10k to 30k) of crystals in this application. We can roughly calculate the number of cycles required for a decay or rise in amplitude for one time constant (63% of final value) by:

$$\text{Number of cycles} = \frac{Q}{0.63\pi}$$

At 49 MHz this will be 15k cycles or 300 μs for a crystal Q of 30k. At 27 MHz this time will be 560 μs for the same crystal Q. If long carrier OFF times were required the oscillator start up time would as a result also be quite long. The shorter carrier OFF times overcome one problem but do suggest that the crystal be isolated from the antenna circuit. During the carrier OFF time the base of the modulator transistor is held approximately 0.9V above ground such that the emitter still supplies current to the now saturated collector of the oscillator transistor. Both ends of the LC tank circuit now "see" a low impedance to ground. Further isolation is provided by the split tuning capacitor.

Component	27 MHz	49 MHz
T_P	2 Turns	6 Turns
T_S	3 Turns	1 Turn
L1	TOKO KXN K4636 BJF	TOKO KEN K4635 BJE
L_L	MILLER #4611	MILLER #9330-10
C_A	5.4 pF	6.2 pF
R_A	1.15Ω	3.78Ω
C1	1000 pF	220 pF
C2	680 pF	47 pF
C3	20 pF	33 pF
R10	24k	47k

Use TOKO form #51-0116-02 and #30 wire or #51-0178 and #32 wire

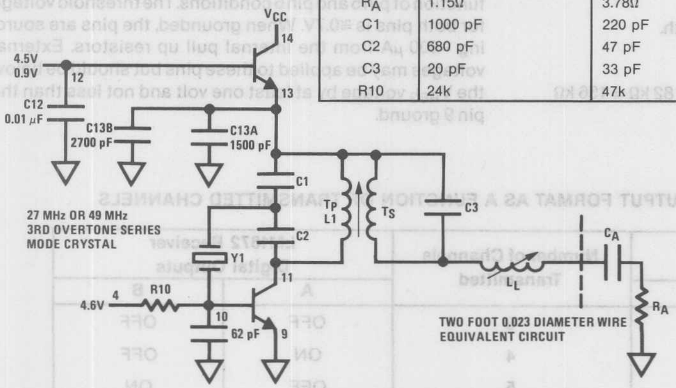


FIGURE 4. 27 MHz and 49 MHz RF Oscillator/Transmitter

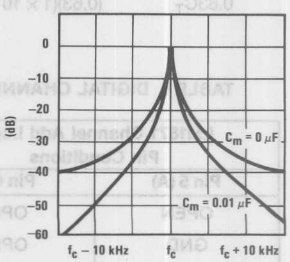


FIGURE 5. Envelope of Transmitted Spectrum for Circuit in *Figure 2*

Applications Information (Continued)

If the printed circuit board shown in *Figure 6* is to be reproduced, it is recommended that the layout be followed as closely as possible. The positions of pin 13 decoupling capacitors and coil components tend to be critical in regard to undesired harmonic emissions. Short lead ceramic disc capacitors and short decoupled traces are recommended. A number of boards with this configuration have successfully met all requirements of the FCC as perceived only by National Semiconductor. Final approval of any unlicensed transmitter is granted only by the FCC via certified test measurements.

Field Strength Measurements

As noted above the maximum radiated RF energy of an unlicensed transmitter operating in the 27 MHz or 49 MHz frequency band must not be greater than 10 kμV per meter at a distance of 3 meters from the transmitting antenna. In addition to the carrier amplitude requirement, all sidebands greater than 10 kHz from the carrier and all other emissions (harmonic or spurious) must be less than 500 μV per meter at a distance of 3 meters.

The term used for electrical field intensity (V/meter at 3 meters) refers to the open circuit voltage induced at the output of a resonant half-wave dipole antenna in a single dimensional one meter field, 3 meters distant from the transmitter under test. When making field intensity measurements, the antenna length must be adjusted for resonance at each frequency of interest and the induced voltage made proportional to the one meter reference length. The induced voltage value must not include losses caused by the insertion of a 1:1 balun transformer (−6 dB) or loading (−6 dB) and mismatch (72Ω to 50Ω, −1.7 dB) of the voltage measuring instrument. We can now relate the induced voltage (V_{IN}) to a measured voltage (V_{MEA}) by:

$$V_{MEA} = \frac{V_{IN}\,L}{\text{Losses}} \text{ or } V_{IN} = \frac{(V_{MEA})(\text{Losses})}{L}$$

where: V_{MEA} = Voltage measured by a spectrum analyzer or calibrated receiver.

V_{IN} = Field intensity (volts/meter).

L = Half-wave length of antenna in meters.

Losses = All mismatch, loading and insertion losses. (In this case = 13.7 dB = 4.87)

The length of a half-wave dipole antenna is found by:

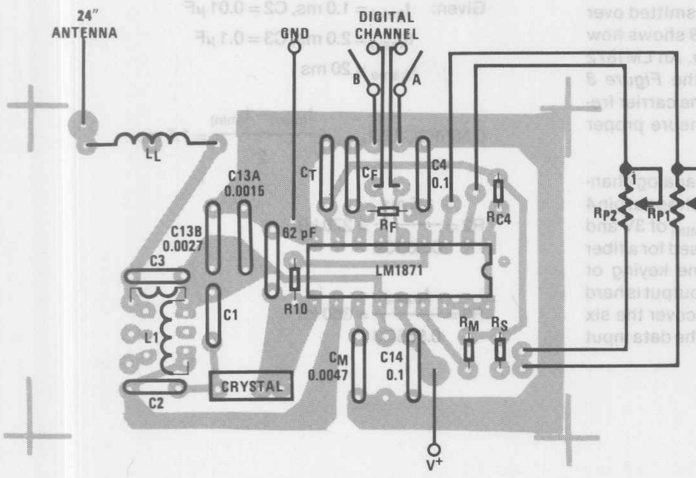
$$L = \frac{Ck}{2f} \text{ meters}$$

where: C = Speed of light in a vacuum.

k = A constant related to antenna length to width ratios, end effects and surface effects. Use k = 0.96 for practical antenna rods 5/16" in diameter.

f = Frequency of interest.

$$\text{Simplified: } L = \frac{144}{f\text{ MHz}} \text{ meters}$$



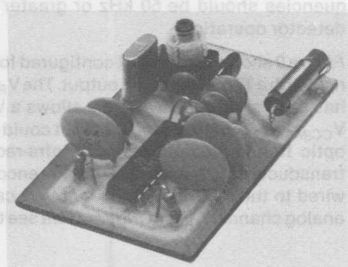


FIGURE 6

Now that we have a way in interpreting the field strength measurements we must deal with the technique used in making these measurements. Usually all measurements are done outside on a flat area away from trees, buildings, buried pipes or whatever. The test transmitter is placed on a wooden stool or table approximately 3 feet high such that the vertical antenna is in a vertical position. The receiving dipole is adjusted for the frequency of interest and orientated to the same plane as the transmitter and placed 3 meters from the transmitter. The dipole may be mounted on a wooden pole or ladder such that the height of the antenna can easily be changed. The antenna length must always be symmetrical about the center tapping balun transformer. The operator and his test equipment must be "behind" the dipole by some 3 or more feet. If it is desired to have the operator at a much more distant location the transmission line must be characterized for additional losses. A number of measurements should be made at each frequency for different heights and orientations of both the transmitting and receiving antennas. The highest reading should be considered the correct reading. In addition to fundamental, sidebands and harmonic emissions, the frequency spectrum from 25 to 1000 MHz should also be scanned for spurious emissions greater than 50μV/meter at 3 meters.

Additional Applications

Figure 2 shows a typical application of the LM1872 Receiver/Decoder. The LM1872 consists of a crystal controlled local oscillator, IF amplifier, AGC, detector, decoder logic and digital channel output drivers. The supply voltage range of 2.5V min to 7V max was chosen to allow battery operation by four "C" or "D" cells.

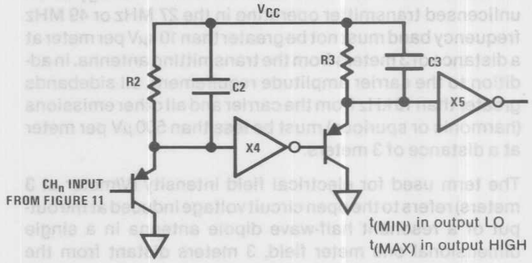
Figure 7 shows how the LM1871 encoder can be used to frequency shift a 200 kHz carrier that is transmitted over the 110V AC line in a home or office. *Figure 8* shows how ON/OFF carrier modulation is also possible. An LM1872 could be used as a receiver/decoder for the *Figure 8* transmitter circuit. When using an LM1872 the carrier frequencies should be 50 kHz or greater to insure proper detector operation.

Figure 9 shows the LM1871 configured for six analog channels with a TTL compatible output. The V_{REG} voltage at pin 4 has been shorted to V_{CC}. This allows a $V_{CC(MIN)}$ of 3V and $V_{CC(MAX)}$ of 6V. The encoder output could be used for a fiber optic transmitter/receiver link, infra-red, tone keying or transducer carrier modulation. If the encoder output is hard wired to the *Figure 10* serial input we can recover the six analog channels. From *Figure 11* we see that the data input will appear during the sync time which is always longer than any channel time (t_n). Inverter X1 will discharge C1 each time the input goes high. During the longer sync time C1 will charge up to the 1/2 V_{CC} threshold of X2 and via X3 provide the data input. The R and C components are calculated by:

$$t_{data\ delay} = 0.565\ R1C1$$

If large values of C1 (>0.01 μF) are required the diode D1 should be replaced by a PNP transistor with the base on X1 output, emitter to X2 input and collector to ground.

In applications requiring ON/OFF decoding of a channel pulse width the circuit shown below could be used.



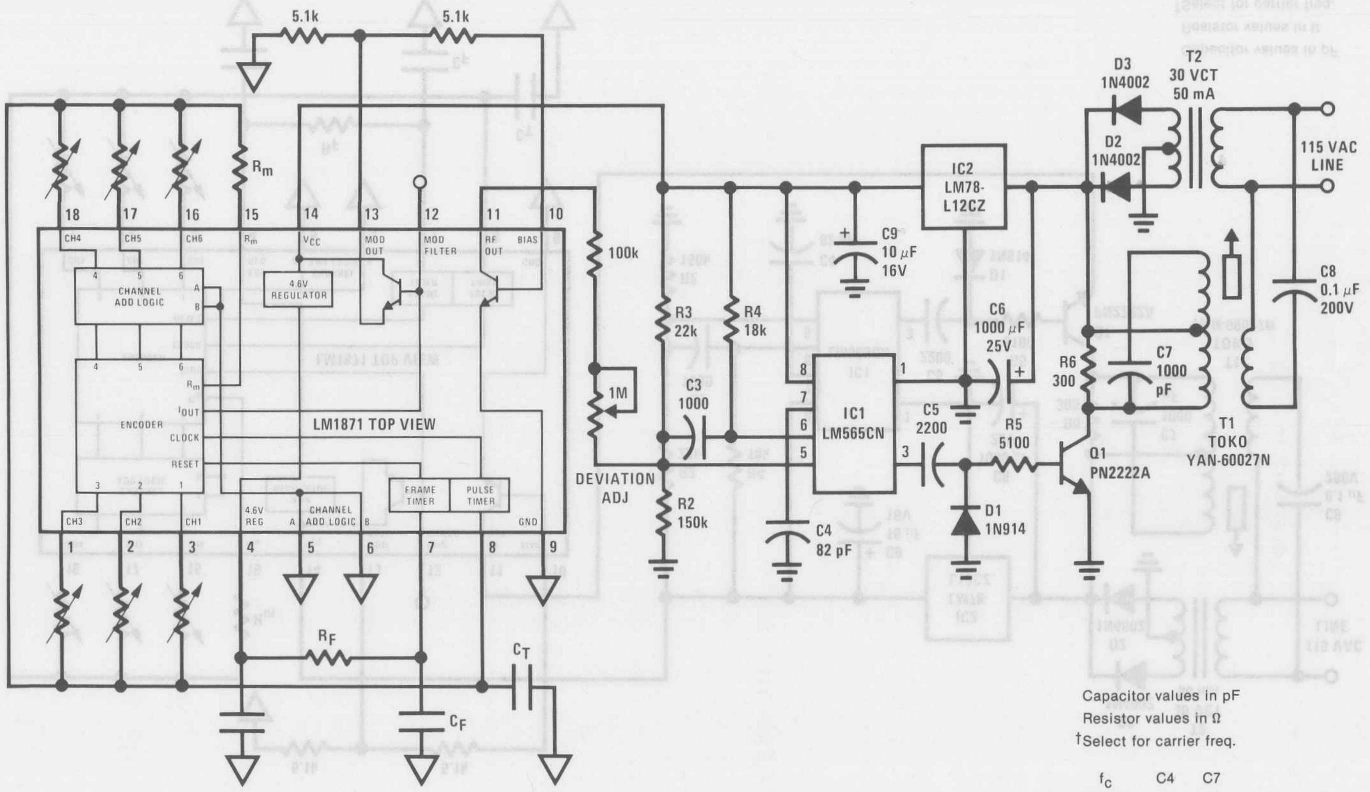
If the recovered channel pulse width is short ($t_{(min)}$) R2 and C2 are selected such that the input to inverter X4 does not rise to the 1/2 V_{CC} threshold. The output of X4 will be high and the output of X5 will be low. A longer input pulse ($t_{(max)}$) will allow the output of X4 to go low pulling the input of X5 low. R3 and C3 are selected such that the input to X5 will not rise past the 1/2 V_{CC} threshold during the remainder of the frame time. The R and c values are found by:

Given: $t_{(min)} = 1.0$ ms, $C2 = 0.01\ \mu F$
$t_{(max)} = 2.0$ ms, $C3 = 0.1\ \mu F$
$t_{frame} = 20$ ms

$$0.565R2C2 = t_{(min)} + \frac{t_{(max)} - t_{(min)}}{2} = 1.5\text{ ms}$$

$$R2 = \frac{1.5\text{ ms}}{0.565C2} = 270\text{ k}\Omega$$

$$R3 = \frac{t_{frame}}{0.565C3} = 360\text{ k}\Omega$$

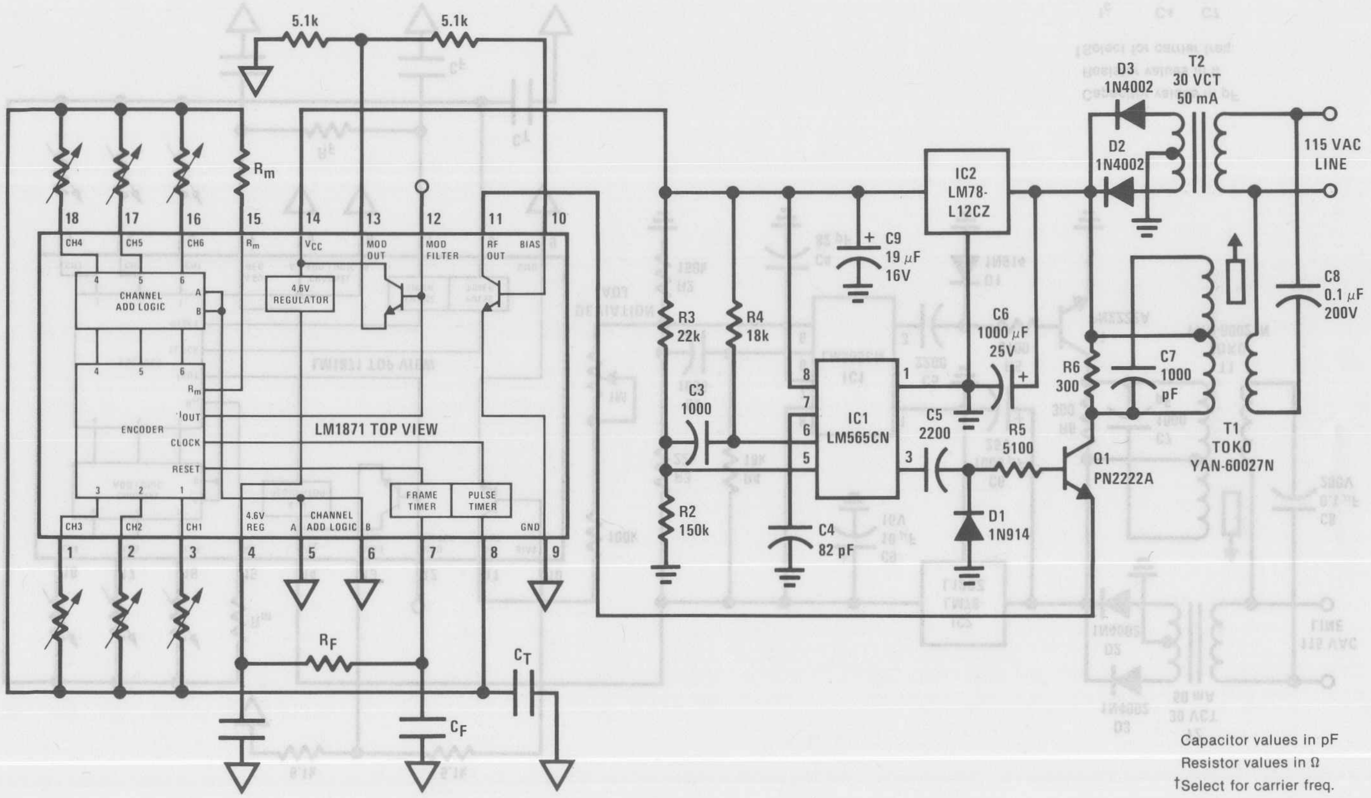


Capacitor values in pF
Resistor values in Ω
†Select for carrier freq.

f_C	C4	C7
200 kHz	82	1000
100 kHz	160	3900

Note: See AN-146 for additional information

FIGURE 7. LM1871, LM566 200 kHz Line Carrier Transmitter with FSK Carrier Modulation



Capacitor values in pF
Resistor values in Ω
†Select for carrier freq.

f_C	C4	C7
200 kHz	82	1000
100 kHz	160	3900

FIGURE 8. LM1871, LM566 200 kHz Line Carrier Transmitter with ON/OFF Carrier Modulation

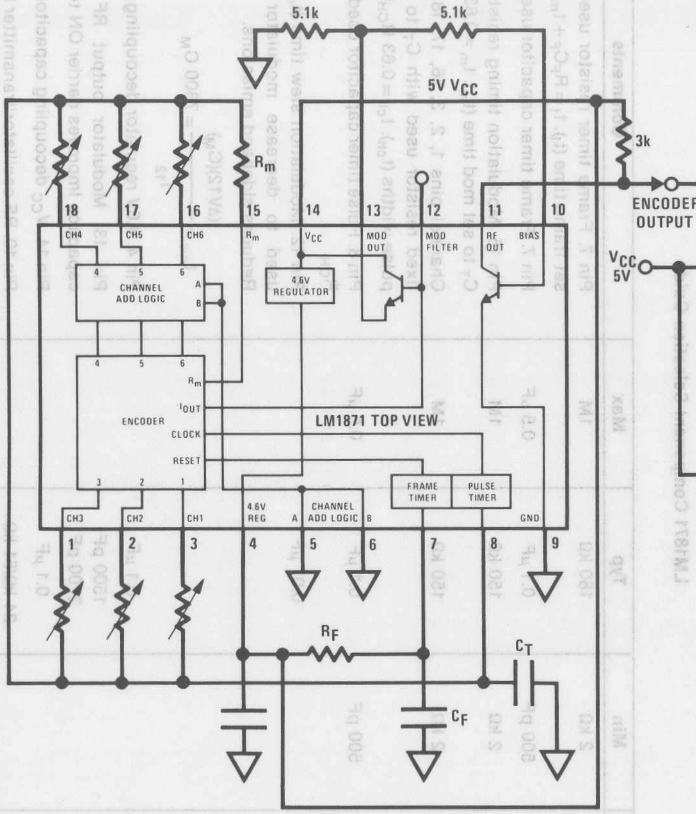
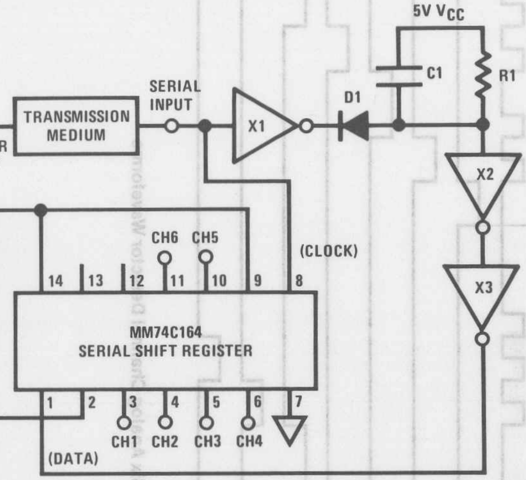


FIGURE 9. LM1871 Six Analog Channel Encoder with TTL Compatible Output



$t_{data\ delay} = 0.565\ RC$

Note: See *Figure 11* for Timing Waveforms

FIGURE 10. Six Analog Channel Detector

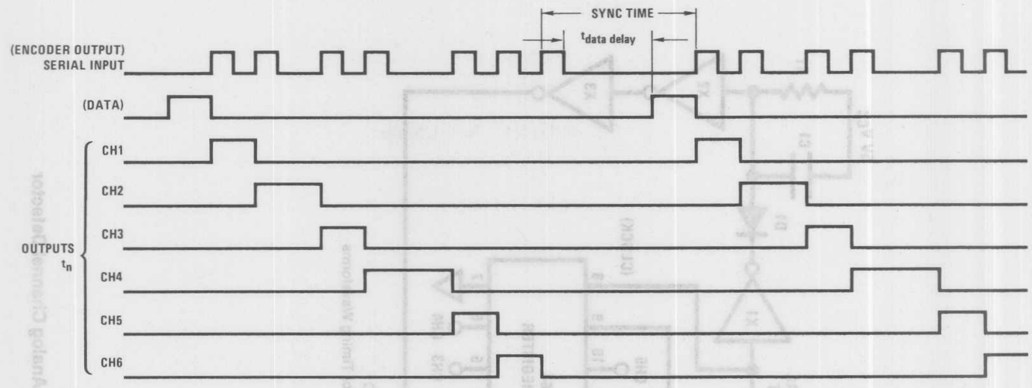


FIGURE 11. Six Analog Channel Detector Waveforms

LM1871 Component Selection Guide

Component	Min	Typ	Max	Comments
R_F	2 kΩ	180 kΩ	1M	Pin 7. Frame timer resistor used with C_F to set frame time (t_f). $t_f = R_FC_F + t_m$.
C_F	500 pF	0.1 μF	0.5 μF	Pin 7. Frame timer capacitor used with R_F.
R_M	2 kΩ	150 kΩ	1M	Pin 15. Modulation timing resistor used with C_T to set mod time (t_m). $t_m = 0.63\ R_MC_T$.
R_{CH}	2 kΩ	150 kΩ	1M	Channel pins 1, 2, 3, 16, 17, 18. Variable or fixed resistor used with C_T to set channel pulse widths (t_{ch}). $t_{ch} = 0.63\ R_{CH}C_T$.
C_T	500 pF	0.1 μF	0.5 μF	Pin 8. Pulse timer capacitor used with R_M and R_{CH}.
C_M		0.01 μF		Pin 12. Modulation slew time (t_{ms}) capacitor used to decrease modulator bandwidth. Reduces sideband emissions. $t_{ms} = \frac{(\Delta V12)(C_M)}{I_{12}} = 7600\ C_M$
C4		0.1 μF		Pin 4. 4.6V regulator decoupling capacitor.
C13A C13B		1500 pF 2700 pF		Pin 13. Modulator output RF decoupling capacitor. Improves carrier ON to OFF ratio.
C14		0.1 μF		Pin 14. V_{CC} decoupling capacitor.
R10		24 kΩ/51 kΩ		Pin 10. RF oscillator/transmitter bias resistor.

Note: See *Figure 4* for RF components. All timing capacitors should be low-drift (NPO) types.

Schematic Diagram

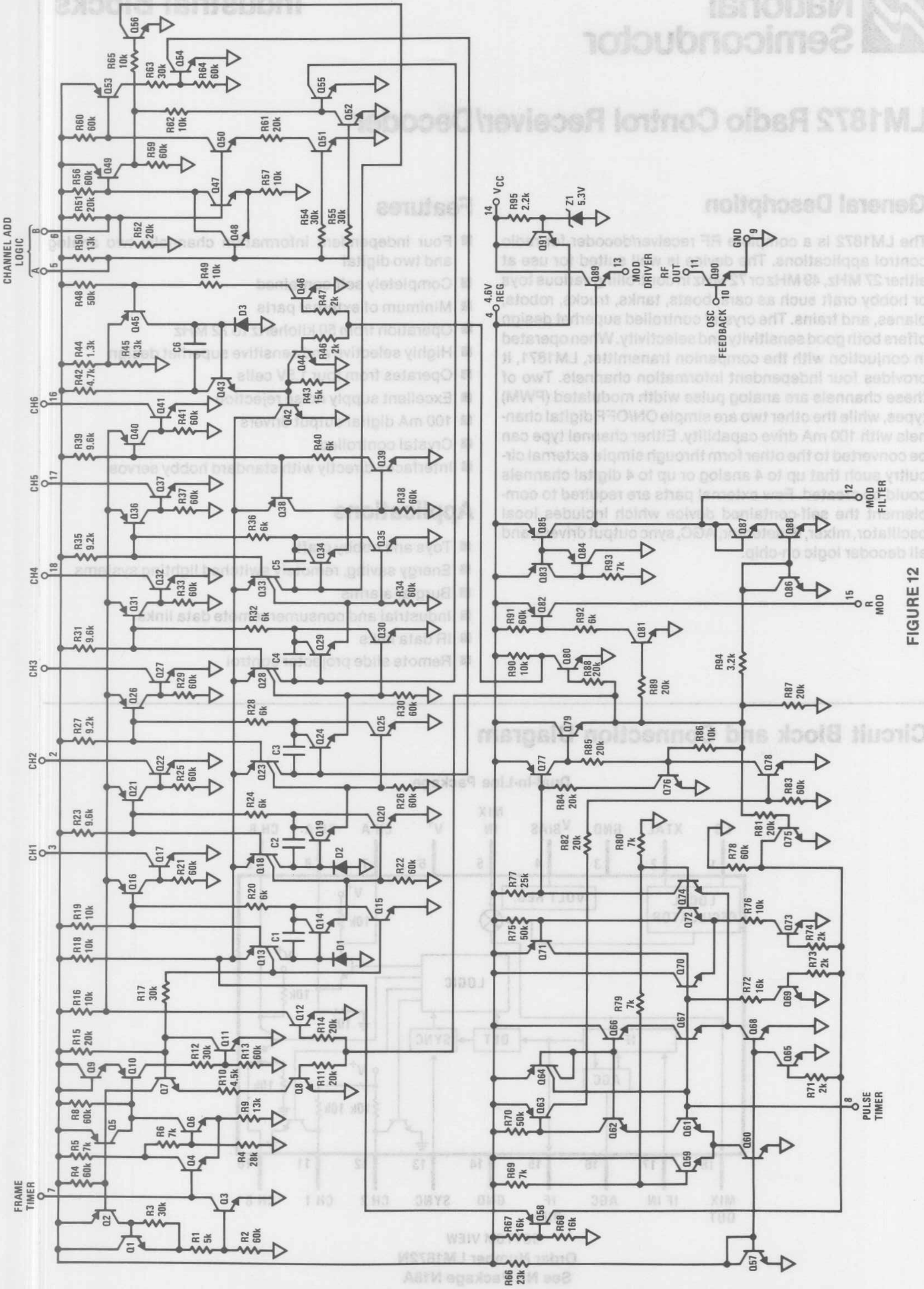


FIGURE 12

National Semiconductor

Industrial Blocks

LM1872 Radio Control Receiver/Decoder

General Description

The LM1872 is a complete RF receiver/decoder for radio control applications. The device is well suited for use at either 27 MHz, 49 MHz or 72 MHz in controlling various toys or hobby craft such as cars, boats, tanks, trucks, robots, planes, and trains. The crystal controlled superhet design offers both good sensitivity and selectivity. When operated in conjuction with the companion transmitter, LM1871, it provides four independent information channels. Two of these channels are analog pulse width modulated (PWM) types, while the other two are simple ON/OFF digital channels with 100 mA drive capability. Either channel type can be converted to the other form through simple external circuitry such that up to 4 analog or up to 4 digital channels could be created. Few external parts are required to complement the self-contained device which includes local oscillator, mixer, IF detector, AGC, sync output drivers, and all decoder logic on-chip.

Features

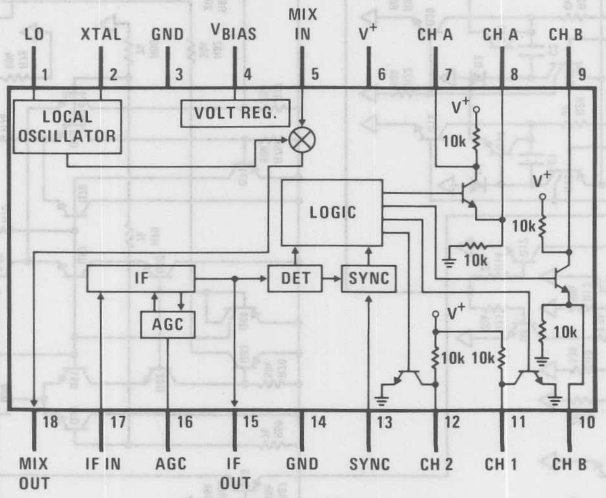
- Four independent information channels; two analog and two digital
- Completely self-contained
- Minimum of external parts
- Operation from 50 kilohertz to 72 MHz
- Highly selective and sensitive superhet design
- Operates from four 1.5V cells
- Excellent supply noise rejection
- 100 mA digital output drivers
- Crystal controlled
- Interfaces directly with standard hobby servos

Applications

- Toys and hobby craft
- Energy saving, remotely switched lighting systems
- Burglar alarms
- Industrial and consumer remote data links
- IR data links
- Remote slide projector control

Circuit Block and Connection Diagram

Dual-In-Line Package



BOTTOM VIEW

Order Number LM1872N

See NS Package N18A

Absolute Maximum Ratings

Supply Voltage	7V
Package Dissipation (Note 2)	1000 mW
Voltage @ Pin 7, 8, 9, 10, 11 or 12	V^+
Operating Temperature Range	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

$V^+ = 6V$, $T_A = 25°C$, Test Circuit of *Figure 1*, $f_{LO} = 49.890$ MHz, $f_{IF} = 455$ kHz unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage	Functional for $V_{IN} = 100\ \mu V$	2.5	6	7	V
Supply Current	CH A & B Off	9	13	18	mA
	CH A & B On		27		mA
V_{BIAS}	@ Pin 4	1.85	2.1	2.35	V
Sync Timer Threshold	@ Pin 13, Going from Low to High Voltage	$V^+/2 - 0.4$	$V^+/2$	$V^+/2 + 0.3$	V
Digital Channels A and B					
Saturation Voltage	@ Pins 7 & 9, $R_L = 100\Omega$		0.4	0.7	V
Saturation Resistance	@ Pins 7 & 9		7		Ω
Source Current	@ Pins 8 & 10, $V_{Pin\ 8\ \&\ Pin\ 10} \leq 1V$	100			mA
Collector Pull-Up Resistance	Pin 7 & Pin 9 to V^+	5	10	20	kΩ
Emitter Pull-Down Resistance	Pin 8 & Pin 10 to GND	5	10	20	kΩ
Analog Channels 1 and 2					
Saturation Voltage	@ Pins 11 & 12, $R_L = 2\ k\Omega$		0.45	0.7	V
Saturation Resistance	@ Pins 11 & 12		160		Ω
Collector Pull-up Resistance	Pin 11 & Pin 12 to V^+	5	10	20	kΩ

AC Electrical Characteristics

Parameter	Conditions	Min	Typ	Max	Units
RF Sensitivity	For "Solid" Decoded Outputs (Note 1)		22	39	μV
RF Sensitivity	Circuit of *Figure 5* @ 49 MHz with Antenna Simulation Network of *Figure 6*		12		μV
Voltage Gain	Pin 5 to Pin 15		58		dB
PSRR of RF Sensitivity	$3V \leq V^+ \leq 6V$		−1		%Δ/V
BW	3 dB Down @ Pin 15		3.2		kHz
Noise	Referred to Input, Pin 5, $V_{IN} = 0$		0.35		μVrms
	Referred to IF, Pin 15, $V_{IN} = 0$		0.28		mVrms
AGC Threshold	Onset of AGC Relative to RF Input, V_{IN}, @ Pin 5		88		μV
	Relative to IF Output @ Pin 15	$V^+ + 0.07$	$V^+ + 0.100$	$V^+ + 0.13$	V
Mixer Conversion Transconductance	From Pin 5 to Pin 18 @ 1 MHz	2.9	4.0	6.9	mmhos
	@ 27 MHz		3.7		mmhos
	@ 49 MHz		3.5		mmhos
Mixer Input Impedance	Pin 5 to Pin 4 @ 49 MHz (See Curves)		20 kΩ + 5 pF		

Parameter	Conditions	Min	Typ	Max	Units
Mixer Output Impedance	Pin 18 to GND		250		kΩ
IF Transconductance	Pin 17 to Pin 15 (AGC Off) @ 455 kHz	2.6	4.1	5.6	mmhos
IF Input Impedance	Pin 17 to GND		5500		Ω
IF Output Impedance	Pin 15 to GND (AGC Off) (AGC On)		800 2		kΩ MΩ
IF Carrier Level	@ Pin 15, $V_{IN} = 100\ \mu V$ (AGC On)		70		mVrms
Detector Threshold	Relative to RF Input, V_{IN}, @ Pin 5		20		μV
	Relative to IF Output @ Pin 15	$V^+ + 0.015$	$V^+ + 0.025$	$V^+ + 0.040$	V
Analog Pulse Width Accuracy	Ratio of Received Pulse Width @ Pins 11 & 12 to Transmitted Pulse Width @ Pin 5 for $V_{IN} = 100\ \mu V$	0.95	1.0	1.05	ms/ms

Note 1: The criteria for the outputs to be considered "solid" are as follows:

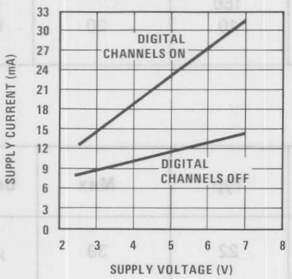
DIGITAL: In order to check the decoding section, four RF frames are inputted in sequence with the proper codes to exercise all four possible logical output combinations at pins 7 and 9. For each frame the proper output logic state must exist.

ANALOG: Each analog pulse width (measured at pins 11 & 12) in any of the above four successive frames must not vary more than ± 5% from the pulse widths obtained for $V_{IN} = 100\ \mu V$.

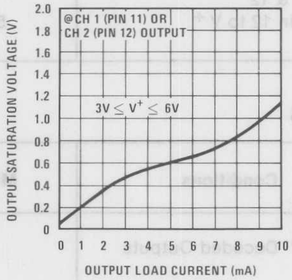
Note 2: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a package thermal resistance of 120°C/W, junction to ambient.

Typical Performance Characteristics

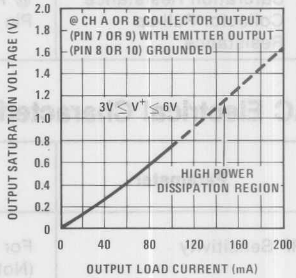
Supply Current vs Supply Voltage



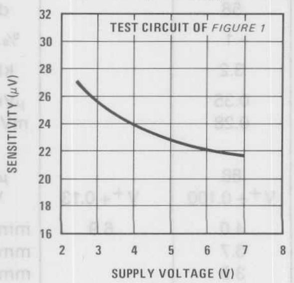
Analog Channel Output Voltage vs Load Current



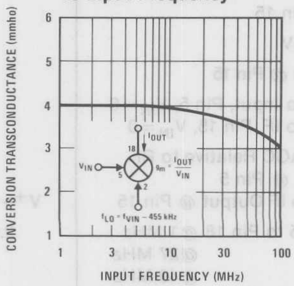
Digital Channel Collector Output Voltage vs Load Current



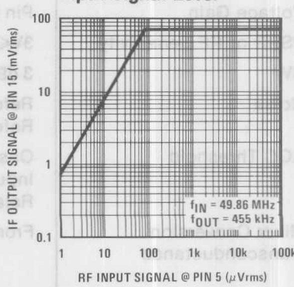
Sensitivity vs Supply Voltage



Mixer Transconductance (g_m) vs Input Frequency

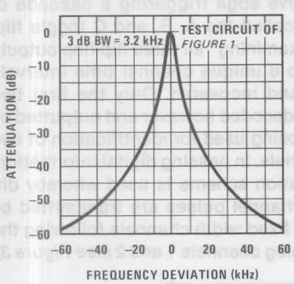


IF Output Signal Level vs RF Input Signal Level

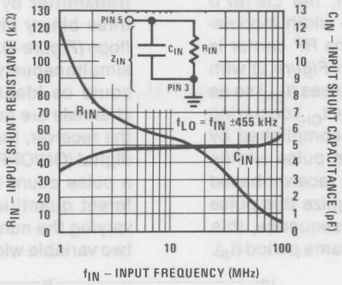


Typical Performance Characteristics (Continued)

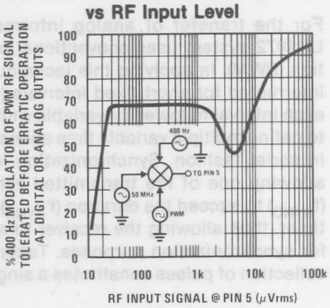
IF Bandpass Response



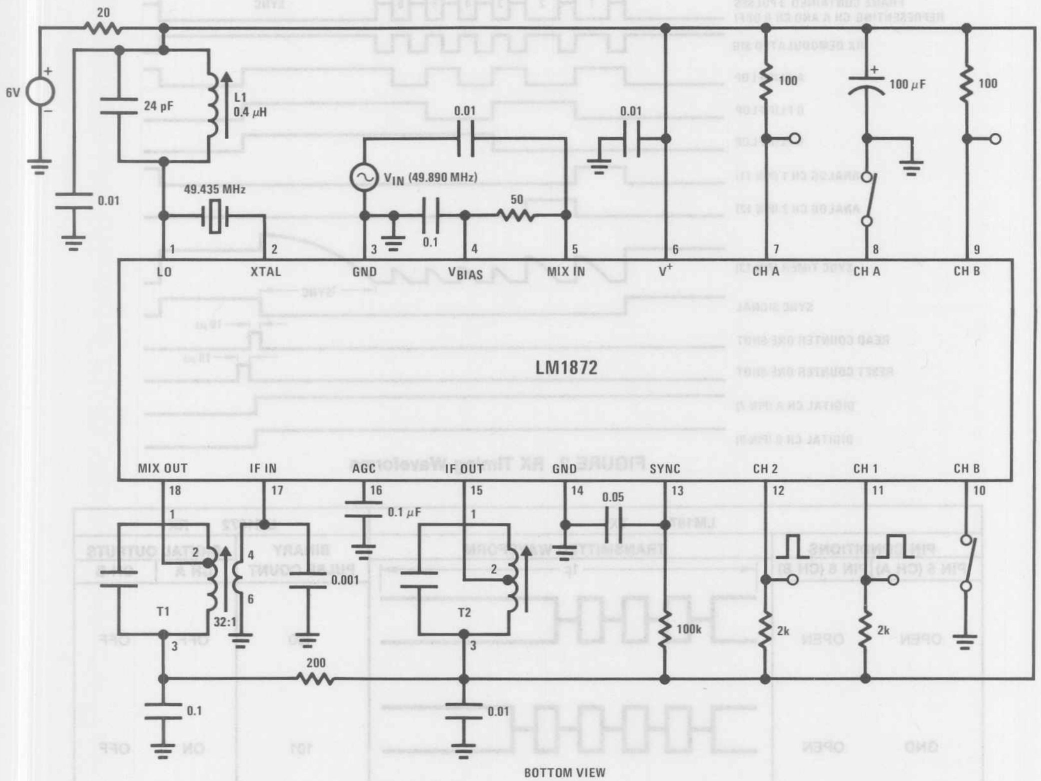
Equivalent Mixer Input Shunt Resistance and Capacitance vs Frequency



Receiver AM Rejection vs RF Input Level



Test Circuit



L1 = Toko* 10k type (KEN-4028 DZ); 6T

T1 = Toko* 10 EZC type (RMC 202313 NO), Qu = 110
Pin 1–2, 131T; pin 2–3, 33T
Pin 1–3, 164T; pin 4–6, 5T

T2 = Toko* 10 EZC type (RMC 402503 NO), Qu = 110
Pin 1–2, 98T; pin 2–3, 66T
Pin 1–3, 164T; pin 4–6, 8T

* Toko America, Inc.
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Skokie, Ill. 60077
(312)677-3640 Tlx: 72-4372

FIGURE 1. Test Circuit

Circuit Description

The following discussion is best understood by referring to *Figures 2, 3, 4, and 5.*

SYSTEM ENCODING AND DECODING SCHEME

For the transfer of analog information, the LM1871/LM1872 system uses conventional pulse width modulation (PWM). In applying this technique, the RF carrier is interrupted for short fixed intervals (t_M in *Figure 2*) with each interval followed by variable width pulses (t_{CH}) so as to define multiple variable time spans ($t_M + t_{CH}$) occurring in serial fashion. Synchronization is accomplished by allowing one of the transmitted variable pulse widths (t_{SYNC}) to exceed the duration (t'_{SYNC}) of a receiver-based timer, thus allowing the receiver to recognize this pulse for synchronization purposes. Taken in sequence, this collection of pulses constitutes a single frame period (t_F).

The LM1871 transmitter is equipped to transmit up to *six* channels which the companion LM1872 receiver uses to derive 2 analog and 2 digital channels. The receiver decodes the demodulated RF waveform from the transmitter by negative edge triggering a cascade of three binary dividers called the A, B, and C toggle flip-flops *(Figure 4)*. By "examining" all three flip-flop outputs simultaneously, up to 6 unique channel time intervals could be identified and recovered. Only the first two channels are actually decoded however and outputted by the receiver, the rest being used for identification of two digital (ON/OFF) channels. In passing digital information, a pulse count modulation scheme is used whereby different quantities of channel pulses are transmitted by varying the number of fixed width channels following the two variable width analog channels 1 and 2 *(see Figure 3)*.

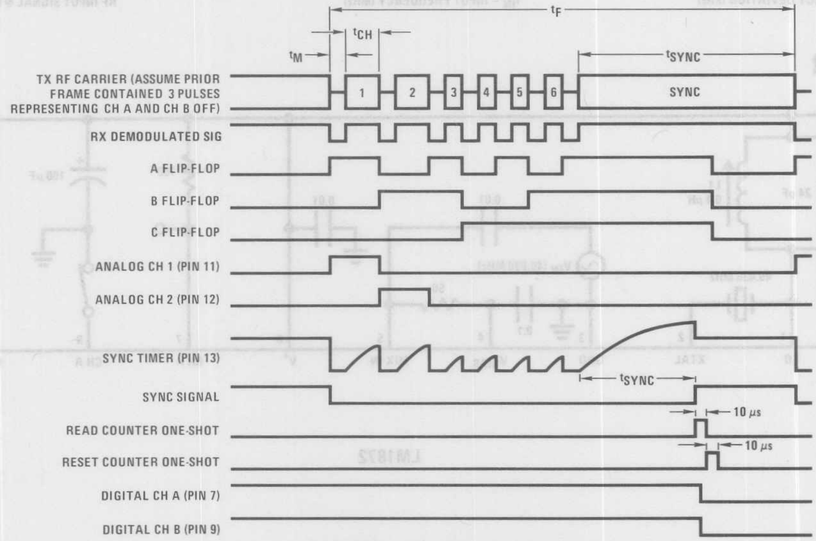


FIGURE 2. RX Timing Waveforms

		LM1871 TX	LM1872 RX		
PIN CONDITIONS		TRANSMITTED WAVEFORM	BINARY	DIGITAL OUTPUTS	
PIN 5 (CH A)	PIN 6 (CH B)	t_F	PULSE COUNT	CH A	CH B
OPEN	OPEN		100	OFF	OFF
GND	OPEN		101	ON	OFF
OPEN	GND		110	OFF	ON
GND	GND		111	ON	ON

FIGURE 3. Digital Channel Encoding and Decoding via Pulse Count Modulation

Circuit Description (Continued)

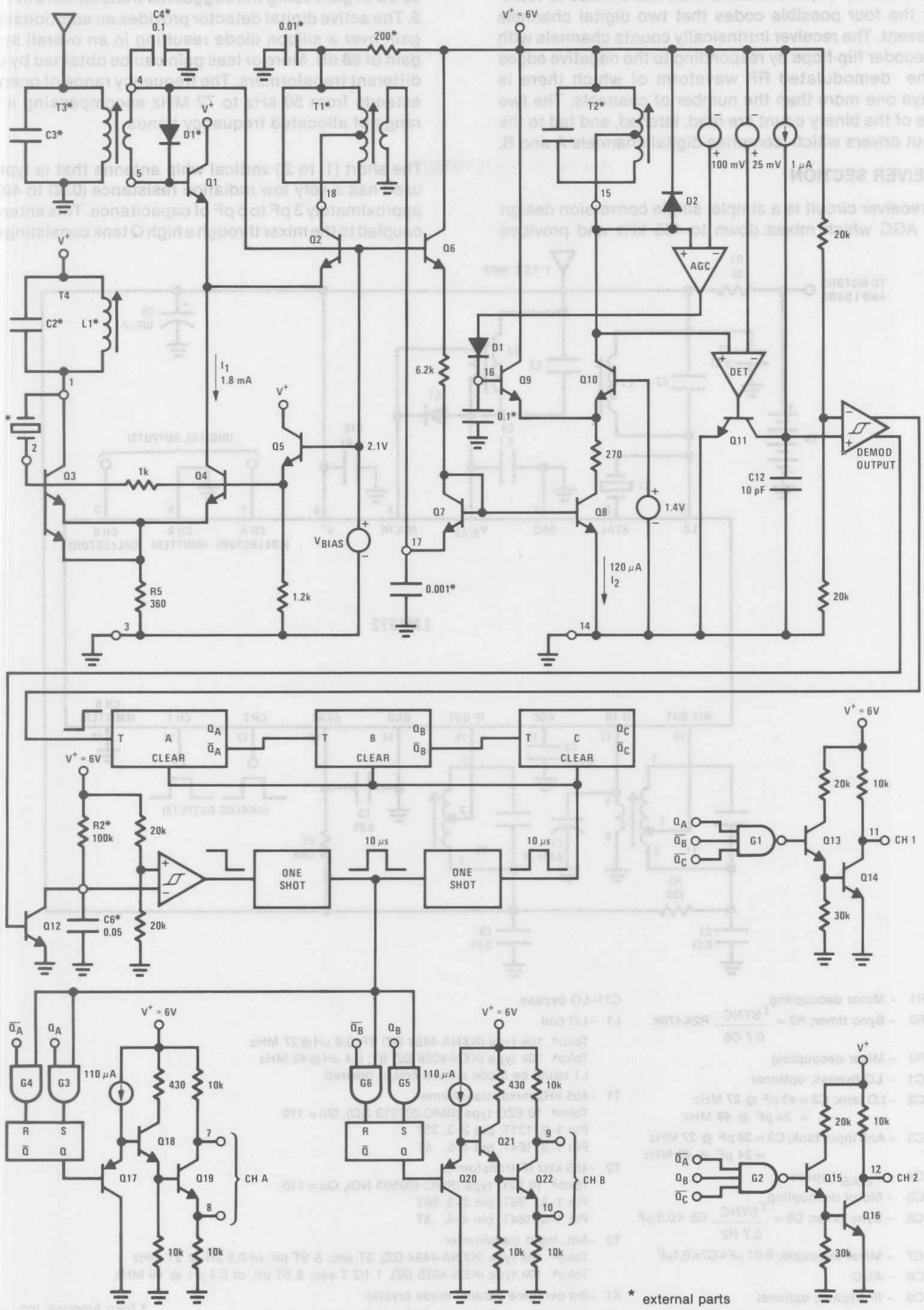


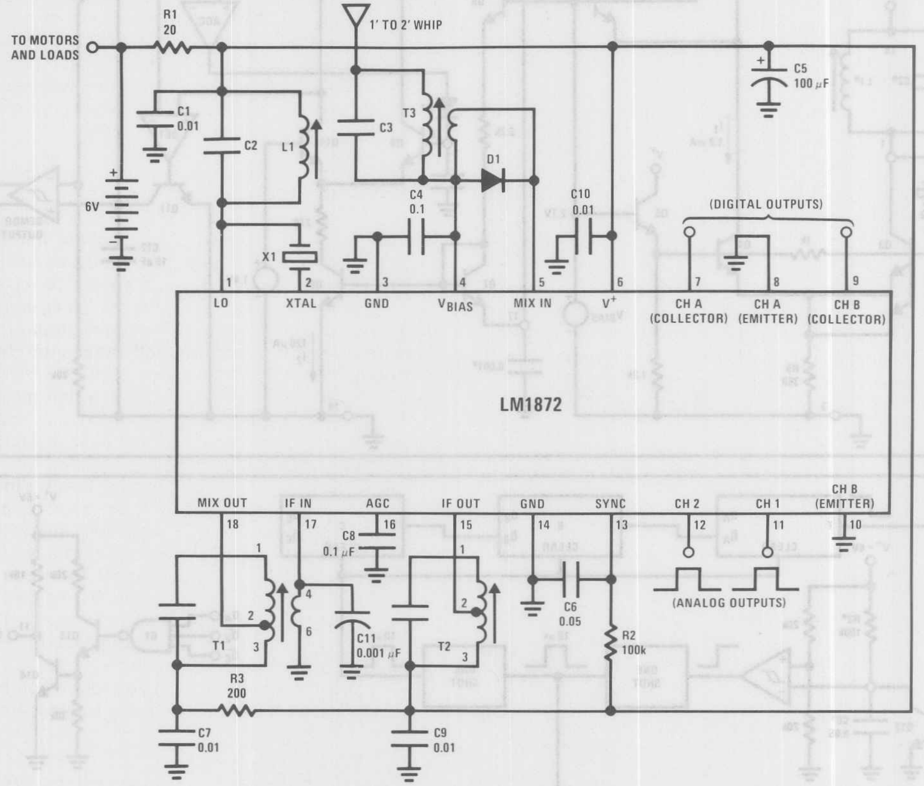
FIGURE 4. Simplified Schematic Diagram

sent the four possible codes that two digital channels represent. The receiver intrinsically counts channels with its decoder flip-flops by responding to the negative edges of the demodulated RF waveform of which there is always one more than the number of channels. The two LSBs of the binary count are read, latched, and fed to the output drivers which comprise digital channels A and B.

RECEIVER SECTION

The receiver circuit is a simple, single conversion design with AGC which mixes down to 455 kHz and provides 5. The active digital detector provides an additional 30 dB gain over a silicon diode resulting in an overall system gain of 88 dB. More or less gain can be obtained by using different transformers. The frequency range of operation extends from 50 kHz to 72 MHz encompassing a wide range of allocated frequency bands.

The short (1′ to 2′) vertical whip antenna that is typically used has a very low radiation resistance (0.5Ω to 4Ω) and approximately 3 pF to 5 pF of capacitance. This antenna is coupled to the mixer through a high Q tank consisting of C3



R1 - Motor decoupling
R2 - Sync timer; $R2 = \frac{t'_{SYNC}}{0.7\ C6}$, R2≤470k
R3 - Mixer decoupling
C1 - LO bypass; optional
C2 - LO tank; C2 = 43 pF @ 27 MHz
= 24 pF @ 49 MHz
C3 - Ant. input tank; C3 = 39 pF @ 27 MHz
= 24 pF @ 49 MHz
C4 - V_{BIAS} bypass
C5 - Motor decoupling
C6 - Sync timer; $C6 = \frac{t'_{SYNC}}{0.7\ R2}$, C6 ≤0.5 μF
C7 - Mixer decouple; 0.01 μF≤C7≤0.1μF
C8 - AGC
C9 - IF bypass; optional
C10 - V^+ bypass; 0.01 μF≤C10≤0.1μF
C11-LO bypass
L1 -LO coil
Toko* 10k type (KXNA-4434 DZ) 9T; 0.8 μH@27 MHz
Toko* 10k type (KEN-4028 DZ) 6T; 0.4 μH@49 MHz
L1 could be made a fixed coil, if desired.
T1 -455 kHz mixer transformer
Toko* 10 EZC type (RMC-202313 NO), Qu = 110
Pin 1-2, 131T; pin 2-3, 33T
Pin 1-3, 164T; pin 4-6, 5T
T2 -455 kHz IF transformer
Toko* 10 EZC type (RMC-402503 NO), Qu = 110
Pin 1-2, 98T; pin 2-3, 66T
Pin 1-3, 164T; pin 4-6, 8T
T3 -Ant. input transformer
Toko* 10k type (KXNA-4434 DZ), 3T sec. & 9T pri. of 0.8 μH @ 27 MHz
Toko* 10k type (KEN-4028 DZ), 1 1/2 T sec. & 6T pri. of 0.4 μH @ 49 MHz
X1 -3rd overtone parallel-mode crystal
D1 -Electrostatic discharge (ESD) protection

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Skokie, Ill. 60077
(312)677-3640 Tlx: 72-4372

FIGURE 5. Typical Application Circuit for 27 MHz or 49 MHz

and T3. This tank effectively keeps strong out-of-band signals such as FM and TV broadcast from cross-modulating with the desired signal. When operating at 49 MHz or 72 MHz, CB interference is also effectively minimized. Image rejection is relatively low, however, being only 7 dB @ 49 MHz, but this does not present a problem due to the usual absence of strong interfering signals 910 kHz below the desired signal.

The antenna signal is stepped down and DC coupled to the mixer which consists of the emitter-coupled pair Q1 and Q2. Emitter-follower, Q1, feeds the common-base device, Q2, while effectively buffering the antenna from the LO energy delivered by Q4. Mixer transconductance is 4 mmhos at low frequency (1 MHz) falling to 3.3 mmhos at the upper end (72 MHz).

The local oscillator utilizes an emitter coupled pair, Q3 and Q4, for accurate control of mixer drive, I_1. Quiescently, Q3 and Q4 share I_1 set by 0.69V/R5, but healthy voltage swings at pin 2 due to oscillation of Q3 implement thorough switching of the differential pair. As a result, the full 1.8 mA of drive "tailgates" (switches) the mixer emitter coupled pair, Q1 and Q2. This current is well regulated from supply voltage changes by the V_{BIAS} circuitry. The TC of V_{BIAS} is positive by design in order to impress a positive TC on I_1 so as to compensate for the temperature dependence of bipolar transconductance in the mixer. Inasmuch as Q4 operates as an emitter-gated, common-base-connected device, excellent isolation between local oscillator and mixer is obtained. As long as pin 4 is properly bypassed, Q5 presents a low impedance to the base of Q4, resulting in low oscillator noise. The oscillator easily operates up to 72 MHz with overtone crystals operating parallel mode.

The mixer signal is stepped down from the high Q mixer tank, T1, and DC coupled to the IF via a secondary winding. The IF stage consists of Q7, Q8 and Q10 and delivers a transconductance of 4 mmhos @ 455 kHz. The quiescent current, I_2, is set at 120 μA by V_{BIAS} and a 6.2k resistor. Again, the positive TC of V_{BIAS} is used to compensate for the temperature dependence of transconductance. The impedance at the IF output, pin 15, is very high (≥800k) permitting the IF transformer, T2, to operate at near unloaded Q (110). The overall 3 dB bandwidth of the receiver section is 3.2 kHz (see characteristic curves); this is narrow enough to permit adjacent channel operation without interference yet wide enough to pass the 500 μs modulation pulses (t_M in *Figure 2*).

The IF signal is DC coupled to the digital detector which consists of a high gain precision comparator, a 30 μs integrator, and a supply-referred 25 mV voltage reference. Whenever the peak IF signal exceeds 25 mV, the comparator drives Q11 to reset the digital envelope detector capacitor, C12. Since it takes 30 μs for the 1 μA current source to ramp C12 to the 3V ($V^+/2$) necessary to fire the Schmitt trigger, the presence of 455 kHz carrier (period = 2.2 μs) greater than 25 mVp will prevent C12 from ever reaching this threshold. When the carrier drops out, the Schmitt trigger will respond 30 μs later. This delay (like that associated with the burst response of the 455 kHz IF tanks) is constant over the time interval of interest. Thus, it is of no consequence to timing accuracy because the LM1872 responds only to negative edges in the decoder.

AGC is provided only to the IF; the mixer having sufficient overload recovery for the magnitude of signals available from a properly operating (i.e. good carrier ON/OFF ratio) 10,000 μV/m transmitter. The AGC differential amplifier regulates the peak carrier level to 100 mV by comparing it to an internal 100 mV supply-referred voltage reference. The resultant error signal is amplified and drives Q9 via rectifier diode, D1, to shunt current away from Q10. C8 provides compensation for the AGC loop which spans a 70 dB range. The 100 mV AGC reference is accurately ratioed to the 25 mV detector reference to permit a controlled amount of brief carrier loss before dropping below detector threshold. Once into AGC, typically 60% amplitude modulation of the PWM carrier is possible before the detector will recognize the interference (see characteristic curves). This kind of noise immunity is invaluable when the troublesome effects of other physically close toys or walkie-talkies on the same or adjacent frequencies are encountered.

DECODER SECTION

The purpose of the decoder is to extract the time information from the carrier for the analog channels and the pulse count information for the digital channels. The core of the decoder is a three-stage binary counter chain comprising flip-flops A, B, and C. The demodulated output from the detector Schmitt-trigger drives both the counter chain and the sync timer (Q12, R2, C6, and another Schmitt trigger). When the RF carrier drops out for the first modulation pulse, t_M, the falling edge advances the counter (see *Figure 2*.) During the t_M interval the sync timer capacitor is held low by Q12. When the carrier comes up again for the variable channel interval, t_{CH}, C6 begins to ramp towards threshold ($V^+/2$) but is unable to reach it in the short time that is available. At the end of the t_{CH} period the carrier drops out again, the counter advances one more, and the sequence is repeated for the second analog channel. To decode the two analog channels, 3-input NAND gates G1 and G2 examine the counter chain binary output so as to identify the time slots that represent those channels. Decoded in this manner, the output pulse width equals the sum of t_M, a fixed pulse, and t_{CH}, a variable width pulse. A Darlington output driver interfaces this repetitive pulse to standard hobby servos.

Following the transmission of the second analog channel, a variable quantity from one to four, of fixed width pulses (500 μs) are transmitted that contain the digital channel information. Up until the end of the pulse group frame period, t_F, the decoder responds as if these fixed pulses were analog channels but delivers no outputs. At the conclusion of the frame the sync pulse, t_{SYNC}, is sent. Since t_{SYNC} is always made longer than the sync timer period (t'_{SYNC} = 3.5 ms), the sync timer will output a sync signal to the first of two cascaded 10 μs one-shots. The first one-shot enables AND gates G3→G6 to read the A and B flip-flops of the counter into a pair of RS latches. The state of flip-flop A, for example, is then stored and buffered to drive 100 mA sink or source at the channel A digital output. An identical parallel path allows the state of flip-flop B to appear at the channel B power output. Upon conclusion of the 10 μs read pulse, another 10 μs one-shot is triggered that resets the counter to be ready for the next frame.

Application Hints

A typical application circuit for either 27 MHz or 49 MHz is shown in *Figure 5*. Using the recommended antenna input networks and driving the circuit through the antenna simulation network of *Figure 6*, a solid decoded output occurs for 10 μV and 12 μV input signals at 27 MHz and 49 MHz respectively.

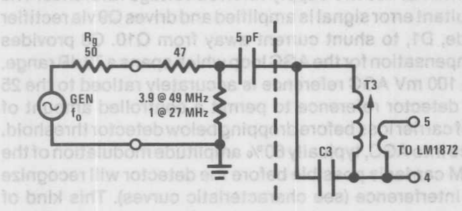


FIGURE 6. Antenna Simulation Network

This sensitivity has been determined empirically to be optimum for toy vehicle applications. Less gain will reduce range unacceptably and more gain will increase susceptibility to noise. However, should the application require greater range (>50m for a land vehicle, for example), either the antenna could be lengthened beyond 2′ and/or receiver sensitivity could be improved. There are a number of ways to alter the sensitivity of the receiver. Decreasing the turns ratio of input transformer, T3, for example, will couple more signal into the mixer at the expense of lower tank Q due to mixer loading. Moving the primary tap on mixer transformer, T1, further from the supply side and/or decreasing the primary to secondary turns ratio will also increase gain. For example, just changing T1 from a 32:1 primary to secondary ratio to a 5:1 turns ratio (Toko #RMC202202) will double 49 MHz sensitivity (6 μV vs 12 μV). Mixer tank Q will be affected but overall 3 dB BW will remain largely unchanged. The primary tap on the IF transformer, T2, can also be adjusted (further from the supply side) for higher gain, but it is possible to cause the AGC loop to oscillate with this method.

Narrow overall bandwidth is important for good receiver operation. The 3.2 kHz 3 dB bandwidth of the circuit in *Figure 5* is just wide enough to pass 500 μs carrier dropout pulses, t_M, yet narrow enough to hold down electrical noise and reject potentially interfering adjacent channels. In the 49 MHz band, the five frequencies available are only 15 kHz apart. Should only two frequencies be used simultaneously, these channels could be chosen 60 kHz apart. Should three frequencies be used, the spacing could be no more than 30 kHz. At four or five frequencies, 15 kHz spacings must be dealt with, making narrow bandwidth highly desirable. Even at 27 MHz, where allocated frequencies are 50 kHz apart, the proliferation of CB stations only 10 kHz away represents a formidable source of interference. The response of the circuit of *Figure 5* is 34 dB and 56 dB down at 15 kHz and 50 kHz away, respectively (see characteristic curves).

The sync timer should have a timeout, t'_{SYNC}, set longer than the longest channel pulse transmitted, but shorter than the shortest sync pulse, t_{SYNC}, transmitted. Using the component values in *Figure 5*, t'_{SYNC}, = 3.5 ms, which works well with a transmitted synce pulse, $t_{SYNC} \geq 5$ ms.

Numerous bypass capacitors appear in the circuit of *Figure* 5, not all of which may be necessary for good stability and performance. A low cost approach may eliminate one or more of the capacitors C1, C9, C10, and C11. The cleaner and tighter the PCB layout used, the more likely is the case that bypass capacitors can be eliminated. In the case of marginal board stability, increasing the size of capacitors C7, C9, and C10 to 0.1 μF may prove helpful. If the PCB layout and parts loading diagram shown in *Figure 7* is used, the circuit will be quite stable up to 72 MHz.

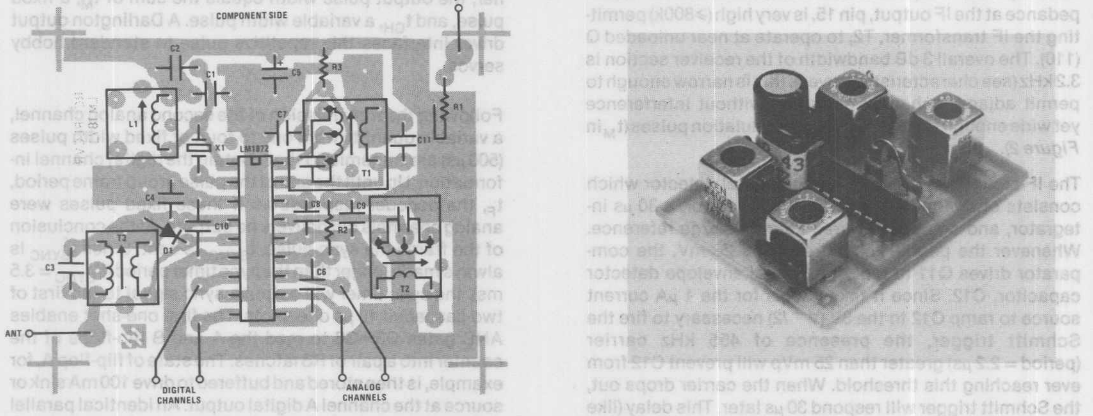


FIGURE 7. PCB Layout, Stuffing Diagram and Complete RX Module for Typical Application Circuit of *Figure 5*

Application Hints (Continued)

The digital channel output devices have significant drive capability; they can typically sink 100 mA and posses a 7Ω saturation resistance. Through their emitters they can source 100 mA up to 1V above ground for driving grounded NPNs and SCRs. Unfortunately, this kind of drive capability can cause thermally induced chip destruction unless total power dissipation is limited to less than 1000 mW. It is good practice and highly recommended to allow the digital output devices to fully saturate at all times (sinking or sourcing) and to limit the current at saturation to no more than 100 mA. For extra drive the two digital outputs can always be summed by connecting pin 7 to pin 9.

The IF frequency is not constrained to be 455 kHz. Operation is limited on the high end to about 1 MHz due to the frequency response limitations of the active detector. The low end is limited to about 50 kHz due to the envelope detector integration time *(Figure 4)*.

Receiver Alignment

The receiver alignment procedure is relatively straightforward because of an absence of interaction between the adjustments. First, the oscillator is tuned by adjusting L1 while monitoring the LO signal at pin 2 with a low capacity (≅10 pF) probe. During tuning the amplitude will rise, peak, and then abruptly quit. Adjust the coil away from the quitting point and just below the amplitude peak.

In order to properly tune T1, T2, and T3, the RF signal must be provided through the receiver antenna by the specific transmitter which is to be used with that specific receiver. This is because the crystals which are commonly used with these systems may have tolerances as loose as ±0.01%. At 49 MHz the resultant ±5 kHz deviation could easily put the incoming signal out of the 3.2 kHz receiver IF bandpass. The signal should be coupled through the receiving antenna to ensure proper loading of the T3 input tank.

Alignment is easier with a defeated AGC, which is accomplished by merely grounding pin 16. The amplitude of the 455 kHz signal at pin 15 is used to guide alignment. Care should be exercised that the signal swing not exceed roughly 400 mVp or diode, D2, in *Figure 4* will threshold and clamp the waveform. Also note that a standard 10 pF probe at pin 15 will shift the IF tank frequency an undesirable 2 kHz. Unless a lower capacity probe is available, it is recommended that the signal be monitored at the unused secondary of T2. Although the signal amplitude would be down by a factor of 8.25 relative to pin 15, up to 50 pF probe capacitance could be tolerated with negligible frequency shift.

The incoming signal is obtained by removing the antenna from the transmitter and then locating the transmitter at a sufficient distance from the receiver to give a convenient signal level (≤400 mVp) at pin 15. T3, T1, and T2 are then tuned for maximum signal.

Applications

Operation at 72 MHz

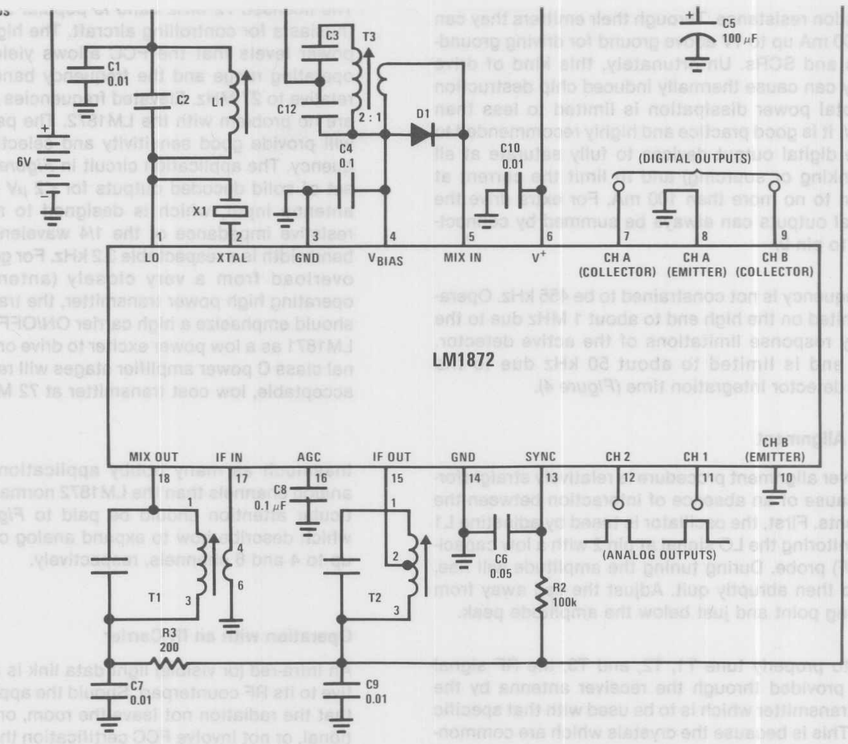
The licensed 72 MHz band is popular among hobby enthusiasts for controlling aircraft. The higher transmitted power levels that the FCC allows yield much greater operating range and the frequency band is uncluttered relative to 27 MHz. Elevated frequencies such as 72 MHz are no problem with the LM1872. The part is stable and will provide good sensitivity and selectivity at that frequency. The application circuit in *Figure 8* will provide a set of solid decoded outputs for <2 μV of signal at the antenna input, which is designed to match the 100Ω resistive impedance of the 1/4 wavelength antenna. IF bandwidth is a respectable 3.2 kHz. For good immunity to overload from a very closely (antennas touching) operating high power transmitter, the transmitter design should emphasize a high carrier ON/OFF ratio. Using the LM1871 as a low power exciter to drive one or more external class C power amplifier stages will result in a simple, acceptable, low cost transmitter at 72 MHz.

Inasmuch as many hobby applications require more analog channels than the LM1872 normally provides, particular attention should be paid to *Figures 10 and 12* which describe how to expand analog channel capacity up to 4 and 6 channels, respectively.

Operation with an IR Carrier

An infra-red (or visible) light data link is a useful alternative to its RF counterpart. Should the application demand that the radiation not leave the room, or that it be directional, or not involve FCC certification then a light carrier should be given consideration. The principal drawbacks to this approach include short range (≤20 ft.) and high transmitter power consumption. There is little that can be done to dramatically improve range, but short burst-type operation of the transmitter will still permit battery operation.

The information link *(Figure 9a)* consists of a light carrier amplitude modulated by a 455 kHz subcarrier. The subcarrier in turn is modulated by the normal Pulse Width/Pulse Count Scheme produced be the LM1871 encoder. A husky, focused LED is used as the transmitter running Class A 100% modulated with an average current drain of 50 mA to 500 mA depending upon range requirements. The detector consists of a large area silicon PN or PIN photodiode for good sensitivity. The LM1872 will directly interface to such a diode and give very good performance. Only a few nanoamps of photo current from D1 are required to threshold the detector. Ambient light rejection is excellent due to the very narrow bandwidth (≅3 kHz) that results from the use of three high Q 455 kHz transformers, T1, T2, and T3. Note that the LO has been defeated and the mixer runs as a conventional 455 kHz amplifier. Otherwise, circuit operation is the same as if an RF carrier were being received.



R1 – Motor decoupling

R2 – Sync timer; $R2 = \frac{t_{SYNC}}{0.7\ C6}$, $R2 \leq 470k$

R3 – Mixer decoupling

C1 – LO bypass; optional

C2 – LO tank; C2 = 22 pF @ 72 MHz

C3 – Ant. input tank; C3 = 24 pF @ 72 MHz

C4 – V_{BIAS} bypass

C5 – Motor decoupling

C6 – Sync timer; $C6 = \frac{t_{SYNC}}{0.7\ R2}$, $C6 \leq 0.5\ \mu F$

C7 – Mixer decouple; $0.01\ \mu F \leq C7 \leq 0.1\ \mu F$

C8 – AGC

C9 – IF bypass; optional

C10 – V^+ bypass; $0.01\ \mu F \leq C10 \leq 0.1\ \mu F$

C12 – Ant. input tank; C12 = 160 pF @ 72 MHz

L1 – LO coil
Toko* 10k type (KENC) 4T; 0.2 μH @ 72 MHz
L1 could be made a fixed coil, if desired.

T1 – 455 kHz mixer transformer
Toko* 10 EZC type (RMC-502182), Qu = 110
Pin 1–2, 82T; pin 2–3, 82T
Pin 1–3, 164T; pin 4–6, 30T

T2 – 455 kHz IF transformer
Toko* 10 EZC type (RMC-502503), Qu = 110
Pin 1–2, 82T; pin 2–3, 82T
Pin 1–3, 164T; pin 4–6, 8T

T3 – Ant. input transformer
Toko 10k type (KENC), 4T sec. & 2T pri. of 0.2 μH @ 72 MHz

X1 – 5th overtone crystal, parallel-mode, 72 MHz

D1 – Electrostatic discharge (ESD) protection

* Toko America, Inc.
5520 West Touhy Ave.
Skokie, Ill. 60077
(312)677-3640 Tlx: 72-4372

FIGURE 8. 72 MHz Receiver Circuit

In a practical remote data link, the transmitter could be battery operated and set up to transmit for brief intervals only in order to save power. The brief transmission could be used to set or reset the digital output latches in the LM1872 and /or command new motor positions via the analog channels. After transmission, the commands would be stored electrically in the case of the digital channels and the mechanically in the case of the analog channels.

As a final note, if the case of D1 is connected to the anode rather than the cathode, the circuit of *Figure 9b* should be used at the input to maintain electromagnetic shielding.

Applications (Continued)

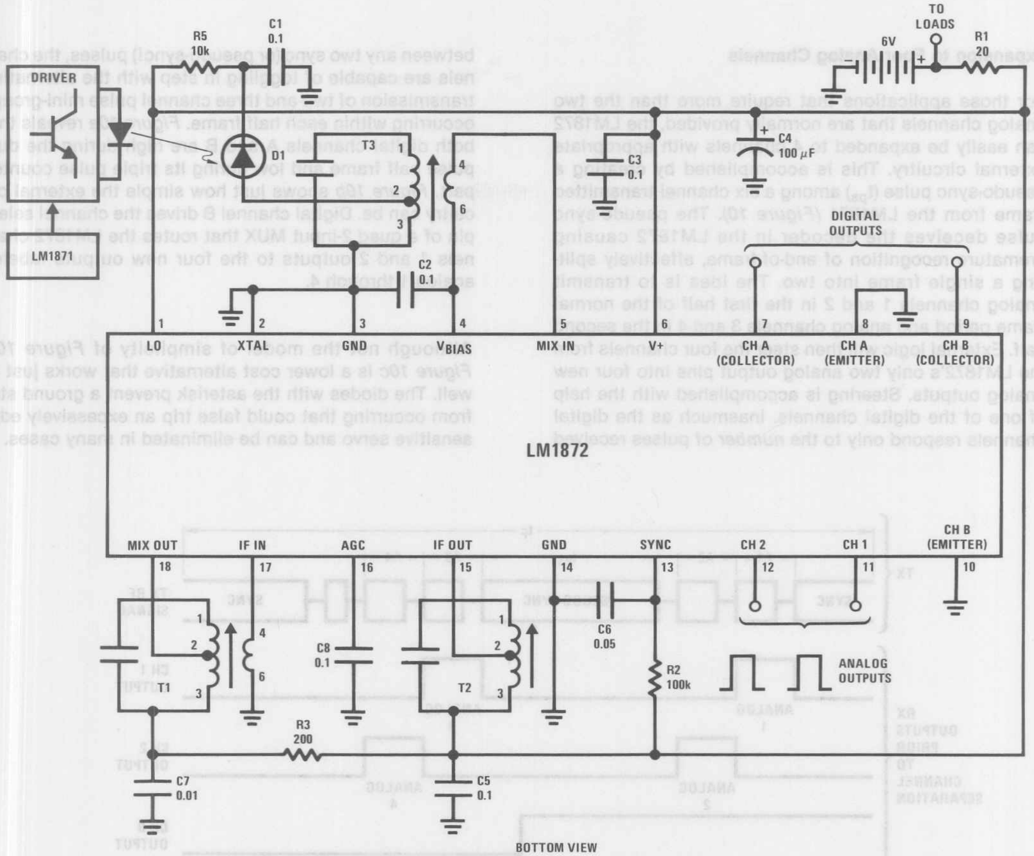


FIGURE 9a. IR Type Data Link

R1 – Load decoupling

R2 – Sync timer; $R2 = \frac{t}{0.7\ C6}$, $R2 \leq 470k$

R3 – Preamp decoupling

R5 – Photodiode decoupling

C1 – Photodiode decoupling

C2 – V_{BIAS} bypass

C3 – V^+ bypass

C4 – Load decoupling

C5 – IF bypass; optional

C6 – Sync timer; $C6 = \frac{t'_{SYNC}}{0.7\ R2}$, $C6 \leq 0.5\ \mu F$

C7 – Preamp decoupling

C8 – AGC

T1 – 455 kHz preamp transformer
Toko* 10 EZC type (RMC-502182), Qu = 110
Pin 1-2, 82T; pin 2-3, 82T
Pin 1-3, 164T; pin 4-6, 30T

T2 – 455 kHz IF transformer
Toko* 10 EZC type (RMC-402503), Qu = 110
Pin 1-2, 98T; pin 2-3, 66T
Pin 1-3, 164T; pin 4-6, 8T

T3 – 455 kHz input transformer
Toko* 10 EZC type (RMC-202313), Qu = 110
Pin 1-2, 131T; pin 2-3, 33T
Pin 1-3, 164T; pin 4-6, 5T

D1 – PN or PIN Silicon Photodiode

	Photodiode, D1	Active Area (cm^2)
Vactec	VTS 5088	0.18
Vactec	VTS 6089	0.52
UDT	PIN 6D or 6 DP	0.20
UDT	PIN 220 DP	2.0
Siemens	BPY 12	0.20

* Toko America, Inc.
5520 West Touhy Ave.
Skokie, Ill. 60077
(312)677-3640 Tlx: 72-4372

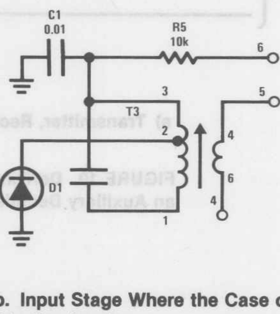


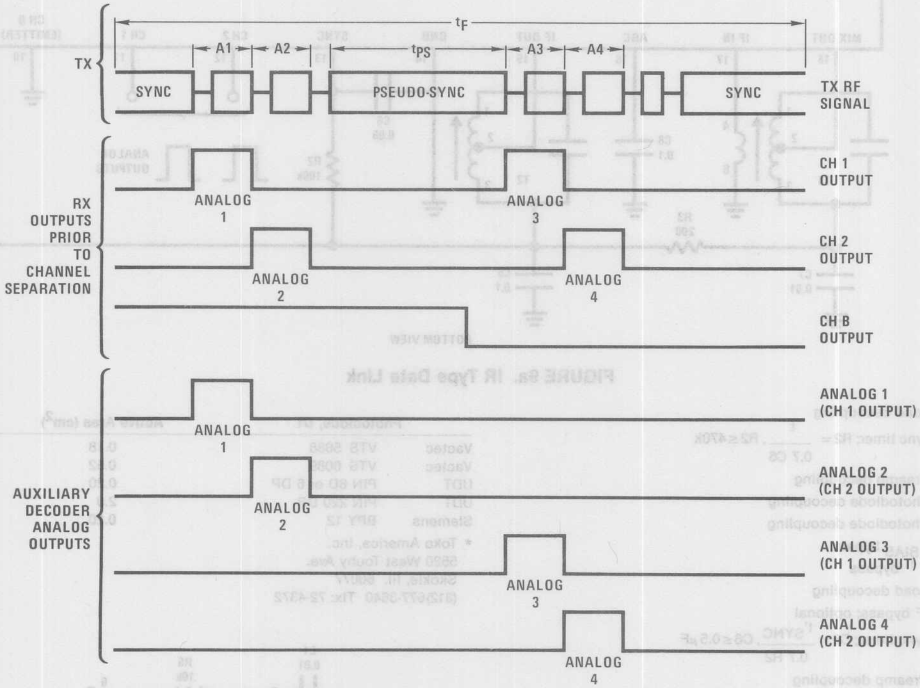
FIGURE 9b. Input Stage Where the Case of D1 is Connected to the Anode

Applications (Continued)

Expansion to Four Analog Channels

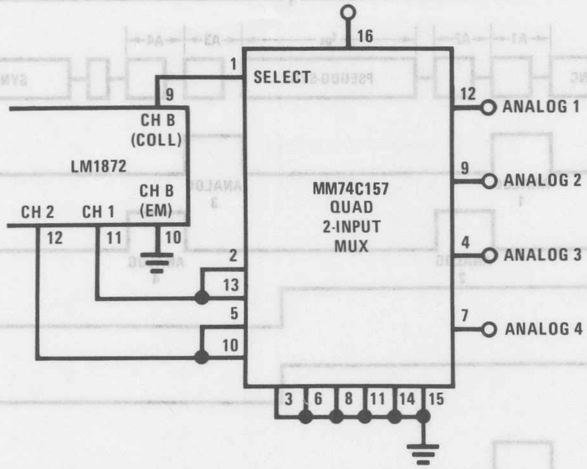
For those applications that require more than the two analog channels that are normally provided, the LM1872 can easily be expanded to 4 channels with appropriate external circuitry. This is accomplished by creating a pseudo-sync pulse (t_{PS}) among a six channel transmitted frame from the LM1871 *(Figure 10)*. The pseudo-sync pulse deceives the decoder in the LM1872 causing premature recognition of end-of-frame, effectively splitting a single frame into two. The idea is to transmit analog channels 1 and 2 in the first half of the normal frame period and analog channels 3 and 4 in the second half. External logic will then steer the four channels from the LM1872's only two analog output pins into four new analog outputs. Steering is accomplished with the help of one of the digital channels. Inasmuch as the digital channels respond only to the *number* of pulses received between any two sync (or pseudo-sync!) pulses, the channels are capable of toggling in step with the alternating transmission of two and three channel pulse mini-groups occurring within each half frame. *Figure 10a* reveals that both digital channels A and B are high during the dual pulse half frame and low during its triple pulse counterpart. *Figure 10b* shows just how simple the external circuitry can be. Digital channel B drives the channel select pin of a quad 2-input MUX that routes the LM1872 channels 1 and 2 outputs to the four new outputs labeled analog 1 through 4.

Although not the model of simplicity of *Figure 10b*, *Figure 10c* is a lower cost alternative that works just as well. The diodes with the asterisk prevent a ground step from occurring that could false trip an excessively edge sensitive servo and can be eliminated in many cases.

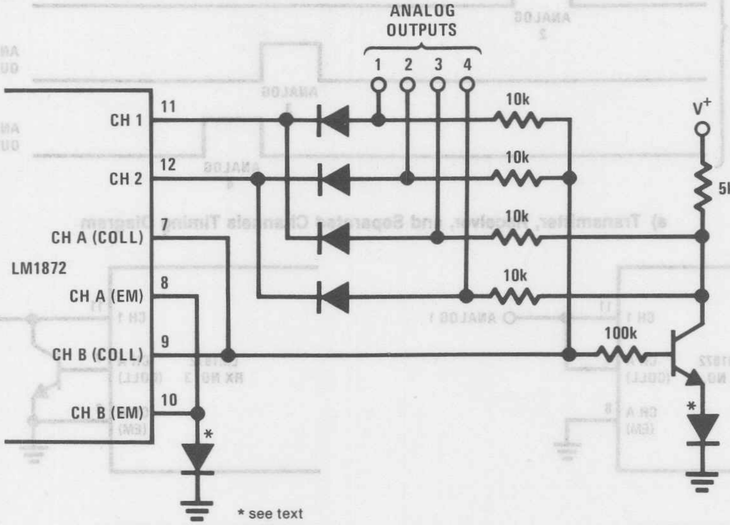


a) Transmitter, Receiver, and Auxiliary Decoder Timing Diagram

FIGURE 10. Deriving Four Analog Channels Through the Use of an Auxiliary Decoder



b) Simple Decoding of Four Analog Channels with CMOS

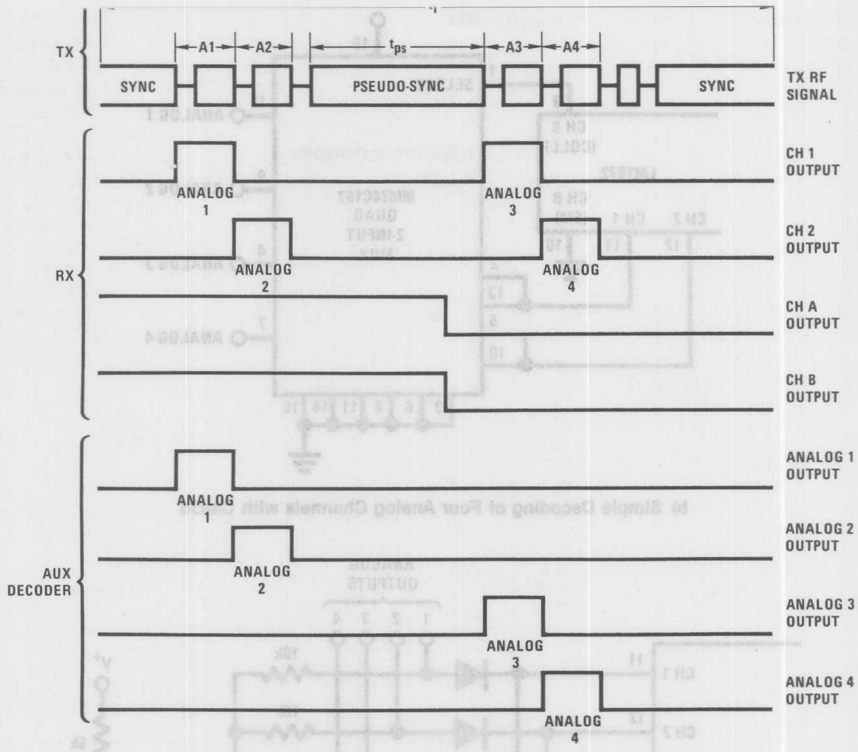


c) Low-Cost Decoding of Four Analog Channels with DTL

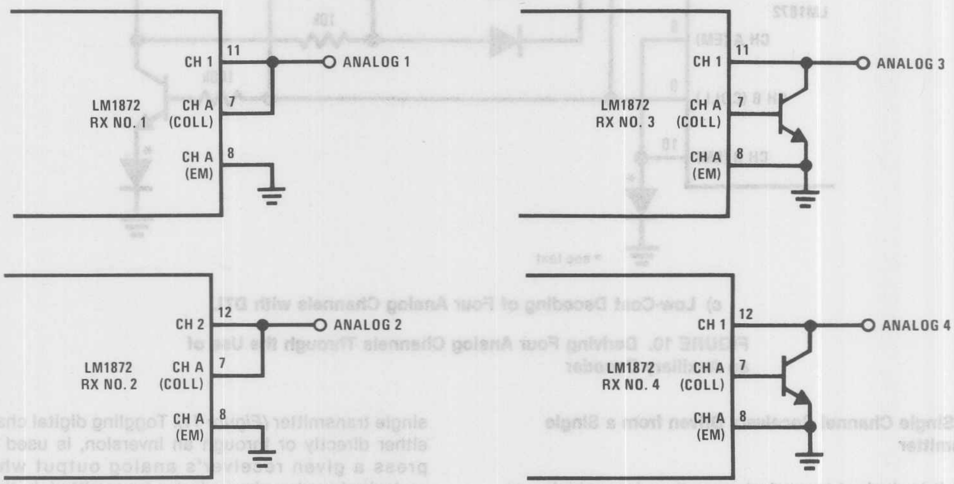
FIGURE 10. Deriving Four Analog Channels Through the Use of an Auxiliary Decoder

Four Single Channel Receivers Driven from a Single Transmitter

When it is desired to control more than two vehicles or remote stations with the analog information from a single transmitter, the LM1872 can be put to the task. By utilizing the frame splitting technique previously described in *Figure 10*, up to four independent single analog channel receivers can be made to operate from a single transmitter *(Figure 11)*. Toggling digital channel A, either directly or through an inversion, is used to suppress a given receiver's analog output when the undesired analog channels are transmitted. In this manner, only the desired analog channel is outputted at each receiver. The amount of external circuitry required to do this is minimal; two receivers require a single transistor apiece while the other two receivers need no extra parts at all.



a) Transmitter, Receiver, and Separated Channels Timing Diagram



b) Simple Channel Separation with Two External Transistors

FIGURE 11. Obtaining Four Independent Single Analog Channel Receivers from a Single Common Transmitter

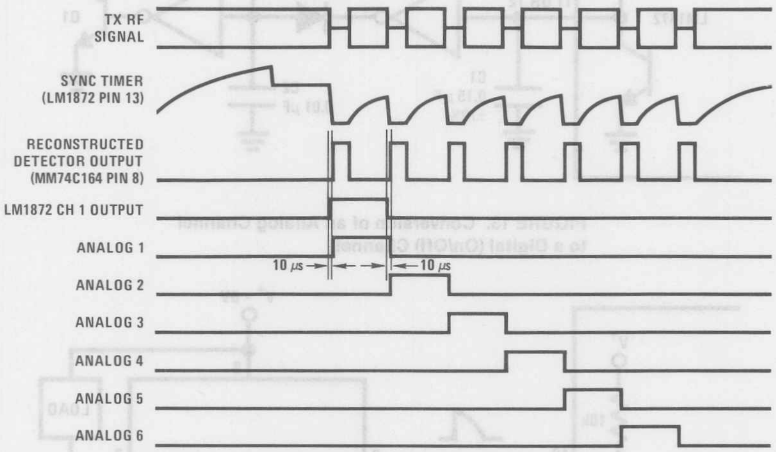
Applications (Continued)

Expansion to Six Analog Channels

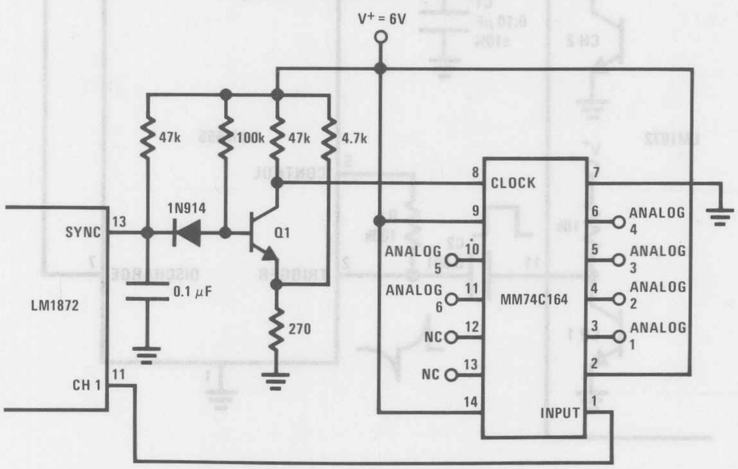
Still greater analog capacity can be obtained with an outboard auxiliary decoder. The LM1872, a simple comparator, and an 8-bit parallel-out serial shift register comprise a six analog channel receiver/decoder *(Figure 12)*. The one transistor comparator reconstructs the detector output of the LM1872 from the sync timer waveform and feeds it to the clock input of the shift register. The channel 1 output then loads a "one" into the register and the clock shifts the "one" down the line of analog channel outputs in accordance with the time information from the detector output. Note that the reconstructed detector waveform lags the channel 1 output very slightly (≅10 μs) due to the finite slope of the sync capacitor discharge edge. This delay is very important as it insures that channel 1 is high when the clock strikes initially (thus loading a "1") and low for each subsequent positive clock edge (thus preventing the loading of extraneous "1's").

Converting an Analog Channel to a Digital Channel

Either analog channel can be converted to a digital channel with the aid of a low cost CMOS hex inverter *(Figure 13)*. The internal 10k resistor and external capacitor, C1, set a time constant (1 ms) that falls between a short (0.5 ms) and a long (2 ms) transmitted pulse option. For pulses longer than 1 ms, the first inverter will pull low momentarily once each frame. Repetitive discharges of C2 prevent it from ever reaching threshold ($V^+/2$) because the R1 C2 time constant is set longer (70 ms) than the frame period. With the inverter input below threshold, Q1 will energize the load. For analog output pulses shorter than 1 ms, the first inverter will back bias D1 allowing C2 to ramp past threshold and Q1 to go off. For extra output drive, the remaining inverters in the package can be paralleled to drive Q1. Alternatively, for light loads Q1 can be eliminated altogether.



a) Six Channel Timing Diagram



b) Six Channel Auxiliary Decoder

FIGURE 12. Deriving Six Analog Channels

Applications (Continued)

Where only one of the two available analog channels needs conversion to a digital format, the LM555 approach offers simplicity combined with up to 150 mA of output drive *(Figure 14)*. The trailing edge of CH 1's output pulse is used to reset the timer in preparation for comparing CH 2's pulse width to the time constant (1.1 ms) set by the internal 10k resistor and C1. For CH 2 pulse widths greater than 1.1 ms C1 ramps to threshold, setting an internal latch in the LM555 and causing the load to be energized. Due to the timing of the reset pulse, however, the LM555 output will go high again for 1.1 ms during the next pulse comparison cycle thus producing an ON state duty cycle of about 95%. For most commonly encountered loads such as motors, solenoids, lamps, and horns, this is of little consequence. The OFF state duty cycle is 100%.

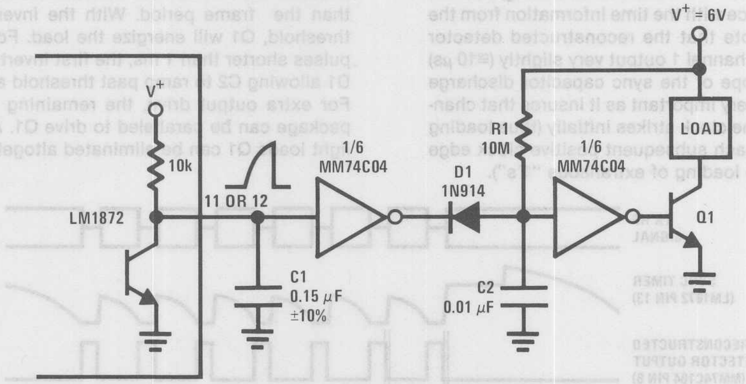


FIGURE 13. Conversion of an Analog Channel to a Digital (On/Off) Channel

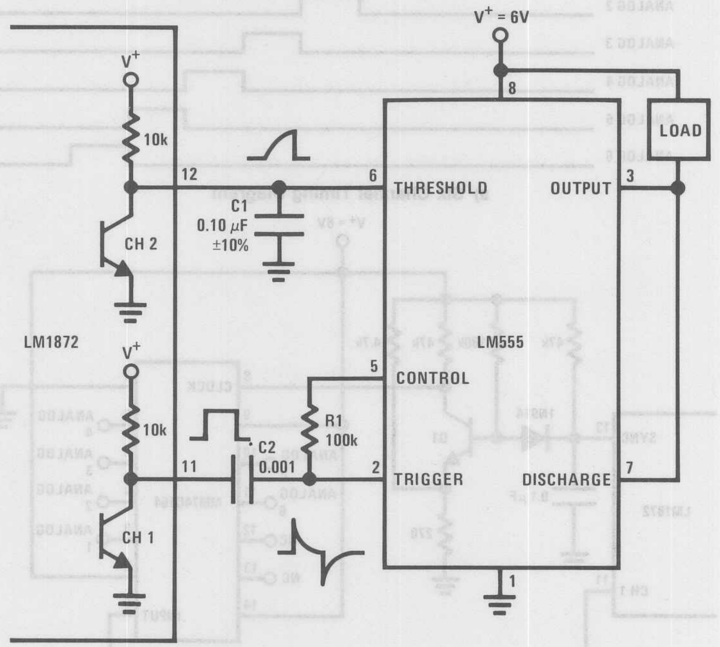


FIGURE 14. Simple Conversion of an Analog to a Digital Channel

Applications (Continued)

Bridge Driving a Motor

The two digital channels can be used to propel a car forward, off, and reverse without the need for a costly servo *(Figure 16)*. The 100 mA digital output capability is used to drive a bridge of four transistors with Q5 added as a protection device. Should an erroneous command to power both sides of the bridge occur (as may happen due to noise with the car out of range) the large motor drive transistors would fight one another resulting in the thermal destruction of one or more of those devices. But Q5 will disable the left side of the bridge whenever the right side is powered preventing the problem from ever occurring. The motor noise suppression network shown has proven to be especially effective in reducing electrical noise and is therefore highly recommended.

Noise Integration of a Digital Channel

Commonly available inexpensive DC motors are a formidable source of electromagnetic interference. Radiation can come from the power feed leads and/or directly from the brushes. Usually proper lead dress and board orientation coupled with a good filter network (see *Figure 16*) will eliminate any problems. In particularly stubborn cases of motor interference, the digital channels may experience more objectionable interference than the analog channels. This is generally not because the digital channels are more susceptible, but rather because the type of load they typically drive (i.e. a horn) will make more of a nuisance of itself than a typical analog load (i.e. a steering servo) when subjected to interference.

Straightforward time integration of the digital channel outputs works very well with any type or degree of motor interference. The simple circuits of *Figure 17* integrate over a period of about three frames (70 ms) and have approximately equal delay either going off or coming on.

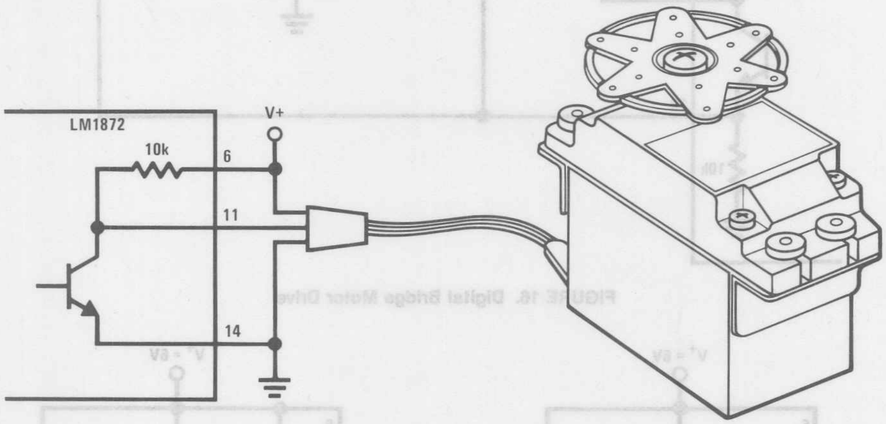


FIGURE 15. Interfacing Directly to Standard Hobby Servos

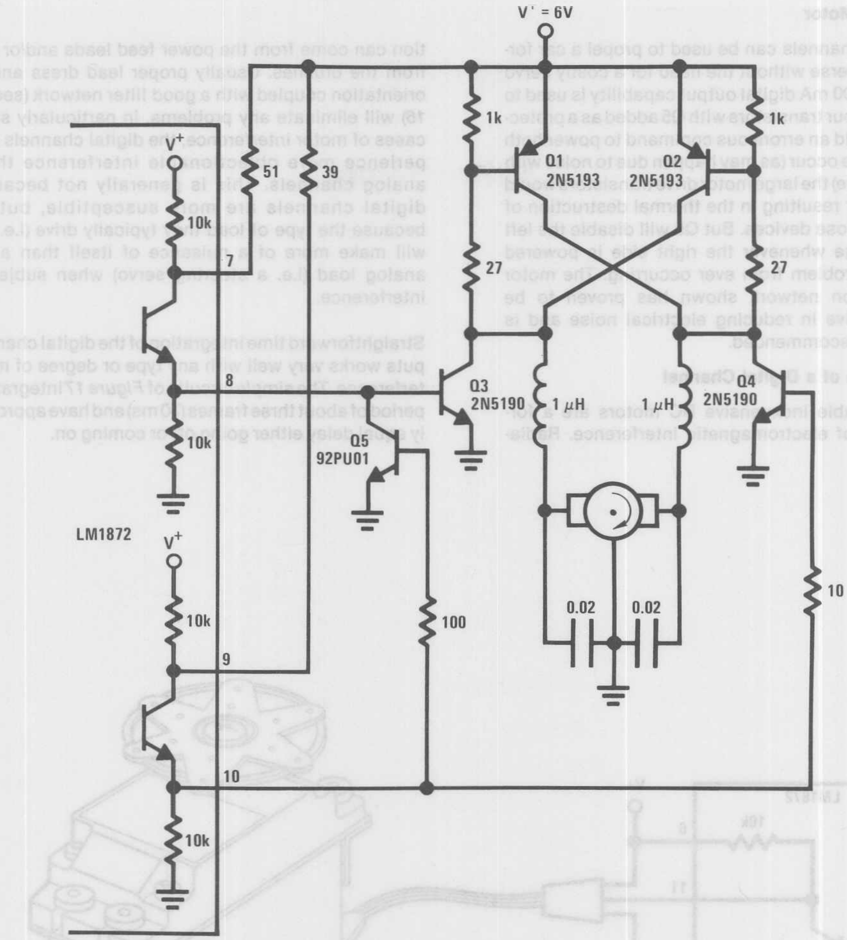
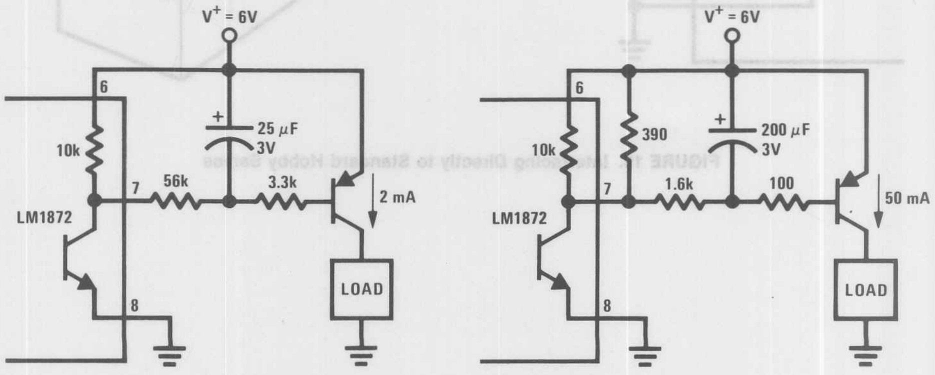


FIGURE 16. Digital Bridge Motor Drive



a) Low Current Load

b) High Current Load

FIGURE 17. Integrating a Digital Channel Output to Achieve Noise Immunity

National Semiconductor

LM2907, LM2917 Frequency to Voltage Converter

General Description

The LM2907, LM2917 series are monolithic frequency to voltage converters with a high gain op amp/comparator designed to operate a relay, lamp, or other load when the input frequency reaches or exceeds a selected rate. The tachometer uses a charge pump technique and offers frequency doubling for low ripple, full input protection in two versions (LM2907-8, LM2917-8) and its output swings to ground for a zero frequency input.

Advantages

- Output swings to ground for zero frequency input
- Easy to use; $V_{OUT} = f_{IN} \times V_{CC} \times R1 \times C1$
- Only one RC network provides frequency doubling
- Zener regulator on chip allows accurate and stable frequency to voltage or current conversion. (LM2917)

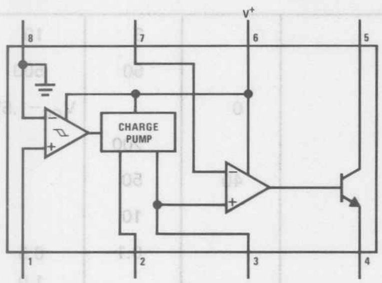
Features

- Ground referenced tachometer input interfaces directly with variable reluctance magnetic pickups
- Op amp/comparator has floating transistor output
- 50 mA sink or source to operate relays, solenoids, meters, or LEDs
- Frequency doubling for low ripple
- Tachometer has built-in hysteresis with either differential input or ground referenced input
- Built-in zener on LM2917
- ±0.3% linearity typical
- Ground referenced tachometer is fully protected from damage due to swings above V_{CC} and below ground

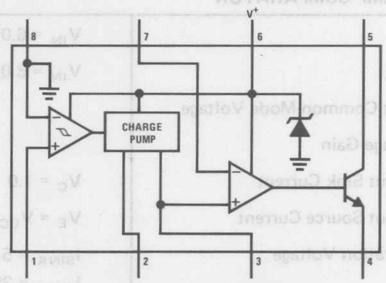
Applications

- Over/under speed sensing
- Frequency to voltage conversion (tachometer)
- Speedometers
- Breaker point dwell meters
- Hand-held tachometer
- Speed governors
- Cruise control
- Automotive door lock control
- Clutch control
- Horn control
- Touch or sound switches

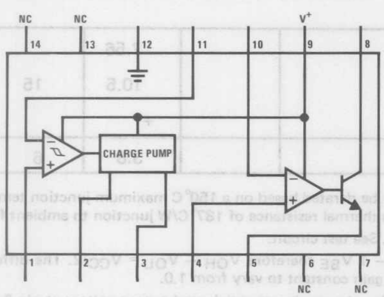
Block and Connection Diagrams Dual-In-Line Packages, Top Views



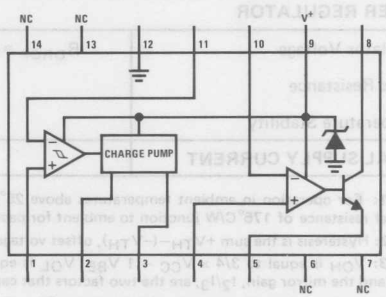
Order Number LM2907N-8
See NS Package N08B



Order Number LM2917N-8
See NS Package N08B



Order Number LM2907J
See NS Package J14A
Order Number LM2907N
See NS Package N14A



Order Number LM2917J
See NS Package J14A
Order Number LM2917N
See NS Package N14A

Absolute Maximum Ratings (Note 1)

Supply Voltage	28V
Supply Current (Zener Options)	25 mA
Collector Voltage	28V
Differential Input Voltage	
Tachometer	28V
Op Amp/Comparator	28V
Input Voltage Range	
Tachometer LM2907-8, LM2917-8	±28V
LM2907, LM2917	0.0V to +28V
Op Amp/Comparator	0.0V to +28V
Power Dissipation	500 mW
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics V_{CC} = 12 V_{DC}, T_A = 25°C, see test circuit

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TACHOMETER					
Input Thresholds	V_{IN} = 250 mVp-p @ 1 kHz (Note 2)	±10	±15	±40	mV
Hysteresis	V_{IN} = 250 mVp-p @ 1 kHz (Note 2)		30		mV
Offset Voltage	V_{IN} = 250 mVp-p @ 1 kHz (Note 2)				
LM2907/LM2917			3.5	10	mV
LM2907-8/LM2917-8			5	15	mV
Input Bias Current	V_{IN} = ±50 mV_{DC}		0.1	1	μA
V_{OH} Pin 2	V_{IN} = +125 mV_{DC} (Note 3)		8.3		V
V_{OL} Pin 2	V_{IN} = −125 mV_{DC} (Note 3)		2.3		V
Output Current; I_2, I_3	V2 = V3 = 6.0V (Note 4)	140	180	240	μA
Leakage Current; I_3	I2 = 0, V3 = 0			0.1	μA
Gain Constant, K	(Note 3)	0.9	1.0	1.1	
Linearity	f_{IN} = 1 kHz, 5 kHz, 10 kHz, (Note 5)	−1.0	0.3	+1.0	%
OP/AMP COMPARATOR					
V_{OS}	V_{IN} = 6.0V		3	10	mV
I_{BIAS}	V_{IN} = 6.0V		50	500	nA
Input Common-Mode Voltage		0		V_{CC}−1.5V	V
Voltage Gain			200		V/mV
Output Sink Current	V_C = 1.0	40	50		mA
Output Source Current	V_E = V_{CC} − 2.0		10		mA
Saturation Voltage	I_{SINK} = 5 mA		0.1	0.5	V
	I_{SINK} = 20 mA			1.0	V
	I_{SINK} = 50 mA		1.0	1.5	V
ZENER REGULATOR					
Regulator Voltage	R_{DROP} = 470Ω		7.56		V
Series Resistance			10.5	15	Ω
Temperature Stability			+1		mV/°C
TOTAL SUPPLY CURRENT			3.8	6	mA

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 175°C/W junction to ambient for package 22 and 16 or a thermal resistance of 187°C/W junction to ambient for package 20.

Note 2: Hysteresis is the sum $+V_{TH}-(-V_{TH})$, offset voltage is their difference. See test circuit.

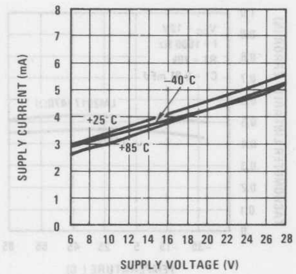
Note 3: V_{OH} is equal to 3/4 x V_{CC} − 1 V_{BE}, V_{OL} is equal to 1/4 x V_{CC} − 1 V_{BE} therefore $V_{OH} - V_{OL} = V_{CC}/2$. The difference, $V_{OH} - V_{OL}$, and the mirror gain, I_2/I_3, are the two factors that cause the tachometer gain constant to vary from 1.0.

Note 4: Be sure when choosing the time constant R1 x C1 that R1 is such that the maximum anticipated output voltage at pin 3 can be reached with I_3 x R1. The maximum value for R1 is limited by the output resistance of pin 3 which is greater than 10 MΩ typically.

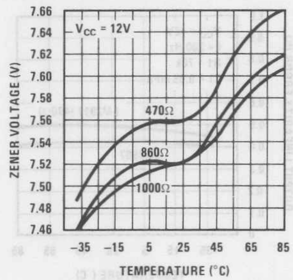
Note 5: Nonlinearity is defined as the deviation of V_{out} (@ pin 3) for f_{IN} = 5 kHz from a straight line defined by the V_{OUT} @ 1 kHz and V_{OUT} @ 10 kHz. C1 = 1000 pF, R1 = 68k and C2 = 0.22 mFd.

Typical Performance Characteristics

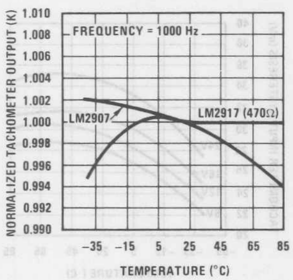
Total Supply Current



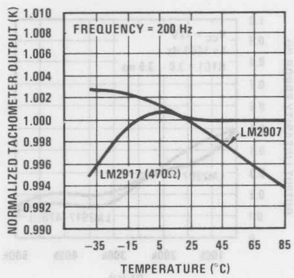
Zener Voltage vs Temperature



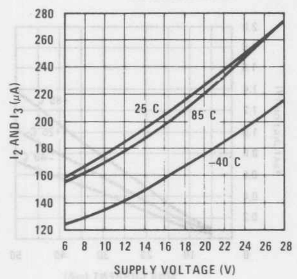
Normalized Tachometer Output vs Temperature



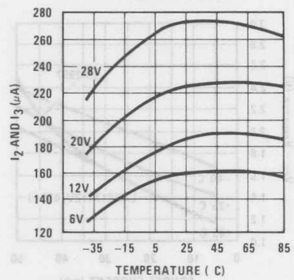
Normalized Tachometer Output vs Temperature



Tachometer Currents I_2 and I_3 vs Supply Voltage

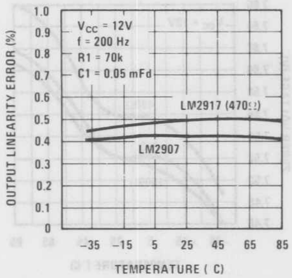


Tachometer Currents I_2 and I_3 vs Temperature

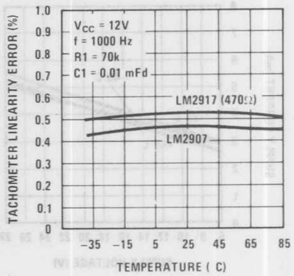


9

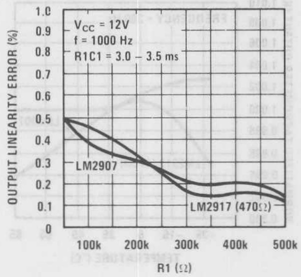
Tachometer Linearity vs Temperature



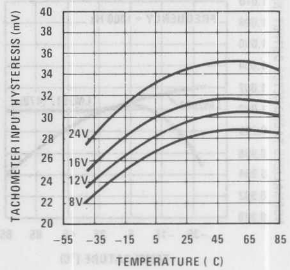
Tachometer Linearity vs Temperature



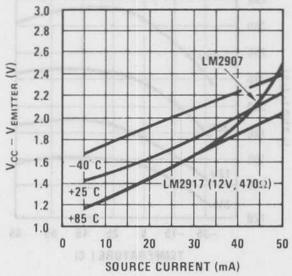
Tachometer Linearity vs R1



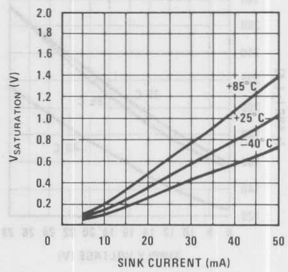
Tachometer Input Hysteresis vs Temperature



Op Amp Output Transistor Characteristics



Op Amp Output Transistor Characteristics



General Description (Continued)

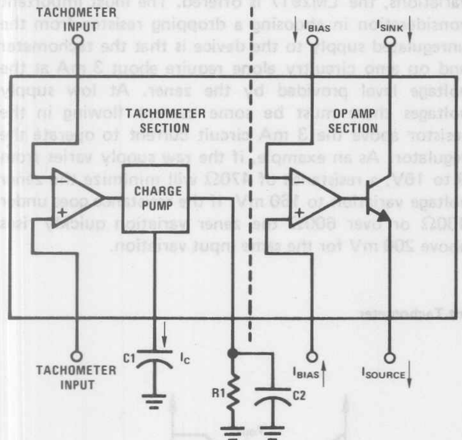
The op amp/comparator is fully compatible with the tachometer and has a floating transistor as its output. This feature allows either a ground or supply referred load of up to 50 mA. The collector may be taken above V_{CC} up to a maximum V_{CE} of 28V.

The two basic configurations offered include an 8-pin device with a *ground referenced tachometer* input and an internal connection between the tachometer output and the op amp non-inverting input. This version is well suited for single speed or frequency switching or fully buffered frequency to voltage conversion applications.

The more versatile configurations provide differential tachometer input and uncommitted op amp inputs. With this version the tachometer input may be floated and the op amp becomes suitable for active filter conditioning of the tachometer output.

Both of these configurations are available with an active shunt regulator connected across the power leads. The regulator clamps the supply such that stable frequency to voltage and frequency to current operations are possible with any supply voltage and a suitable resistor.

Test Circuit and Waveform



Tachometer Input Threshold Measurement

Applications Information

The LM2907 series of tachometer circuits is designed for minimum external part count applications and maximum versatility. In order to fully exploit its features and advantages let's examine its theory of operation. The first stage of operation is a differential amplifier driving a positive feedback flip-flop circuit. The input threshold voltage is the amount of differential input voltage at which the output of this stage changes state. Two options (LM2907-8, LM2917-8) have one input internally grounded so that an input signal must swing above and below ground and exceed the input thresholds to produce an output. This is offered specifically for magnetic variable reluctance pickups which typically provide a single-ended ac output. This single input is also fully protected against voltage swings to ±28V, which are easily attained with these types of pickups.

The differential input options (LM2907, LM2917) give the user the option of setting his own input switching level and still have the hysteresis around that level for excellent noise rejection in any application. Of course in order to allow the inputs to attain common-mode voltages above ground, input protection is removed and neither input should be taken outside the limits of the supply voltage being used. It is very important that an input not go below ground without some resistance in its lead to limit the current that will then flow in the epi-substrate diode.

Following the input stage is the charge pump where the input frequency is converted to a dc voltage. To do this requires one timing capacitor, one output resistor, and an integrating or filter capacitor. When the input stage changes state (due to a suitable zero crossing or differential voltage on the input) the timing capacitor is either charged or discharged linearly between two voltages whose difference is $V_{CC}/2$. Then in one half cycle of the input frequency or a time equal to $1/2\ f_{IN}$ the change in charge on the timing capacitor is equal to $V_{CC}/2 \times C1$. The average amount of current pumped into or out of the capacitor then is:

$$\frac{\Delta Q}{T} = i_{c(AVG)} = C1 \times \frac{V_{CC}}{2} \times (2f_{IN}) = V_{CC} \times f_{IN} \times C1$$

The output circuit mirrors this current very accurately into the load resistor R1, connected to ground, such that if the pulses of current are integrated with a filter

Applications Information (Continued)

capacitor, then, $V_O = i_c \times R1$, and the total conversion equation becomes:

$$V_O = V_{CC} \times f_{IN} \times C1 \times R1 \times K$$

Where K is the gain constant—typically 1.0.

The size of C2 is dependent only on the amount of ripple voltage allowable and the required response time.

CHOOSING R1 AND C1

There are some limitations on the choice of R1 and C1 which should be considered for optimum performance. The timing capacitor also provides internal compensation for the charge pump and should be kept larger than 100 pF for very accurate operation. Smaller values can cause an error current on R1, especially at low temperatures. Several considerations must be met when choosing R1. The output current at pin 3 is internally fixed and therefore $V_O/R1$ must be less than or equal to this value. If R1 is too large, it can become a significant fraction of the output impedance at pin 3 which degrades linearity. Also output ripple voltage must be considered and the size of C2 is affected by R1. An expression that describes the ripple content on pin 3 for a single R1C2 combination is:

$$V_{RIPPLE} = \frac{V_{CC}}{2} \times \frac{C1}{C2} \times \left(1 - \frac{V_{CC} \times f_{IN} \times C1}{I_2}\right) \text{pk–pk}$$

It appears R1 can be chosen independent of ripple, however response time, or the time it takes V_{OUT} to stabilize at a new voltage increases as the size of C2 increases so a compromise between ripple, response time, and linearity must be chosen carefully.

As a final consideration, the maximum attainable input frequency is determined by V_{CC}, C1 and I_2:

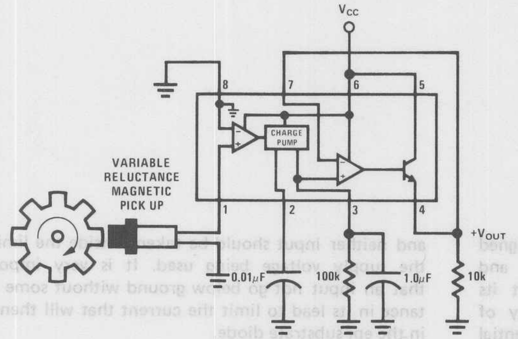
$$f_{MAX} = \frac{I_2}{C1 \times V_{CC}}$$

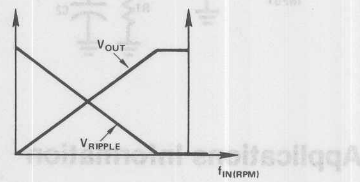
USING ZENER REGULATED OPTIONS (LM2917)

For those applications where an output voltage or current must be obtained independent of supply voltage variations, the LM2917 is offered. The most important consideration in choosing a dropping resistor from the unregulated supply to the device is that the tachometer and op amp circuitry alone require about 3 mA at the voltage level provided by the zener. At low supply voltages there must be some current flowing in the resistor above the 3 mA circuit current to operate the regulator. As an example, if the raw supply varies from 9 to 16V, a resistance of 470Ω will minimize the zener voltage variation to 160 mV. If the resistance goes under 400Ω or over 600Ω the zener variation quickly rises above 200 mV for the same input variation.

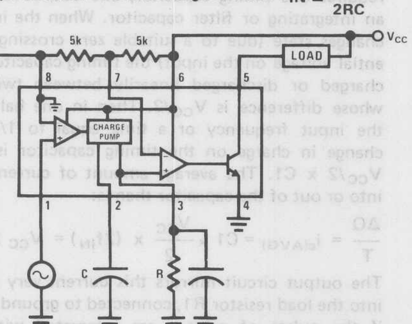
Typical Applications

Minimum Component Tachometer

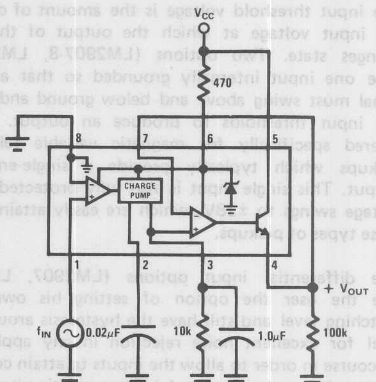




"Speed Switch" Load is Energized When $f_{IN} \geq \frac{1}{2RC}$

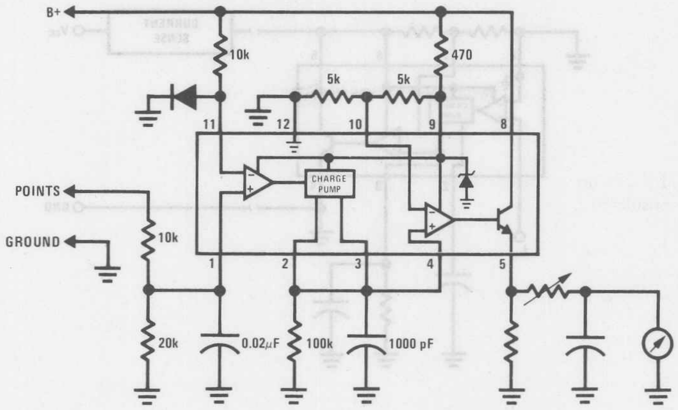


Zener Regulated Frequency to Voltage Converter

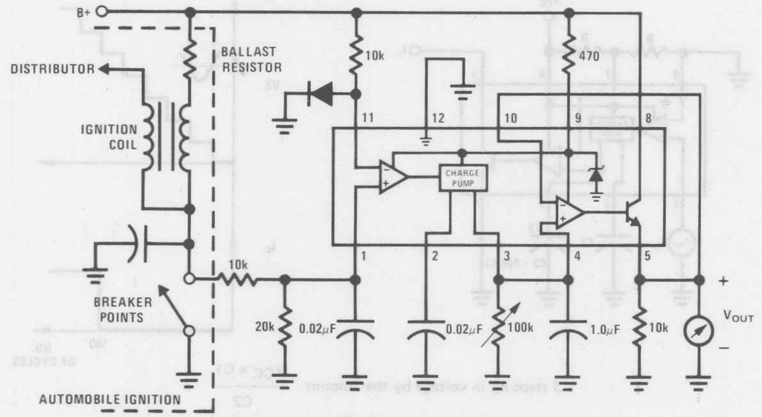


Typical Applications (Continued)

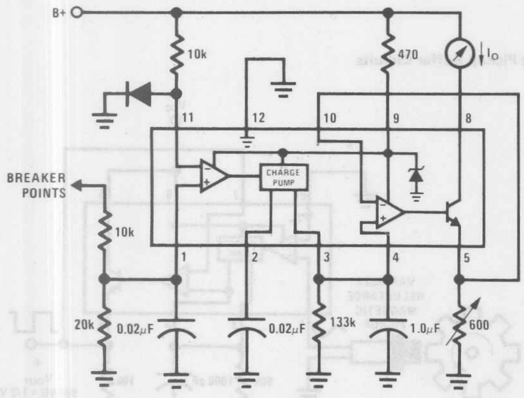
Breaker Point Dwell Meter



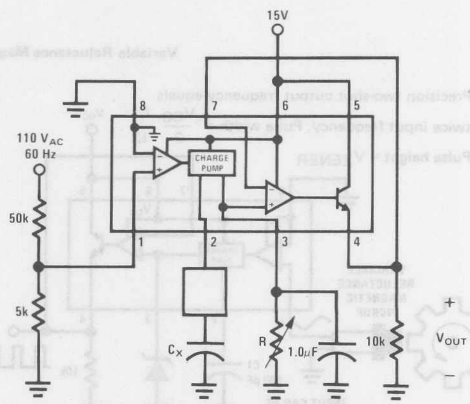
Voltage Driven Meter Indicating Engine RPM
V_O = 6V @ 400 Hz or 6000 ERPM (8 Cylinder Engine)



Current Driven Meter Indicating Engine RPM
I_o = 10 mA @ 300 Hz or 6000 ERPM (6 Cylinder Engine)

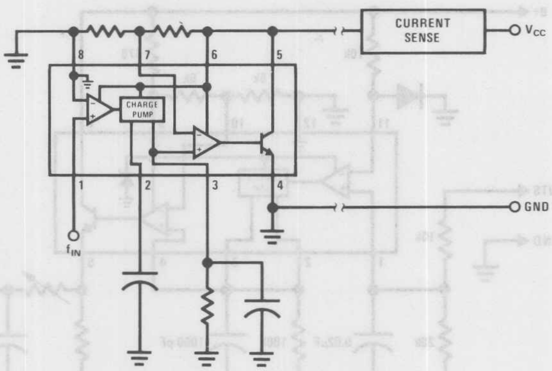


Capacitance Meter
V_{OUT} = 1–10V for C_X = 0.01 to 0.1 mFd
(R = 111k)

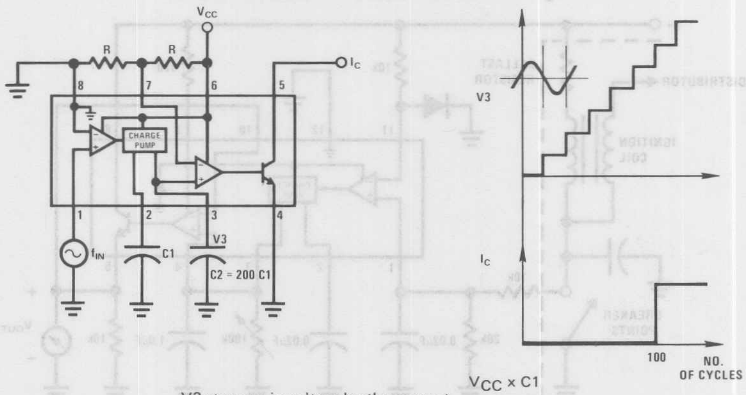


Typical Applications (Continued)

Two-Wire Remote Speed Switch



100 Cycle Delay Switch



V3 steps up in voltage by the amount $\dfrac{V_{CC} \times C1}{C2}$

for each complete input cycle (2 zero crossings)

Example:

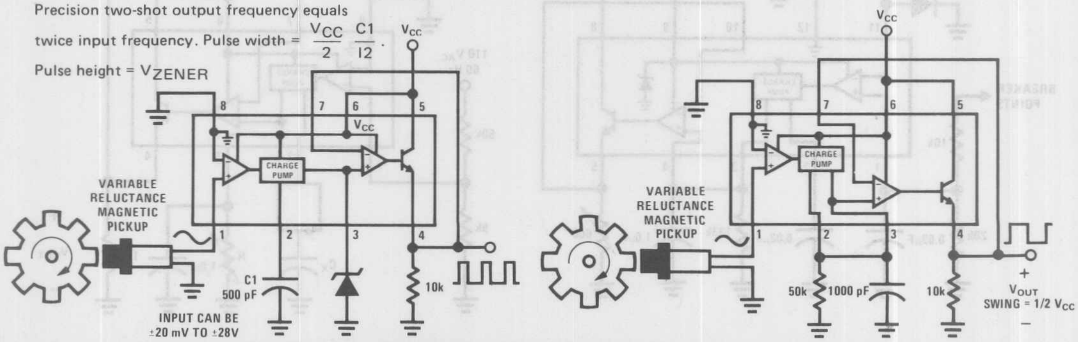
If C2 = 200 C1 after 100 consecutive input cycles.

V3 = 1/2 V_{CC}

Variable Reluctance Magnetic Pickup Buffer Circuits

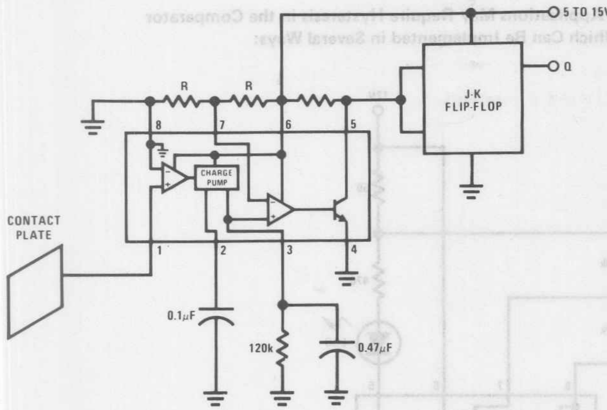
Precision two-shot output frequency equals twice input frequency. Pulse width = $\dfrac{V_{CC}}{2} \cdot \dfrac{C1}{I2}$.

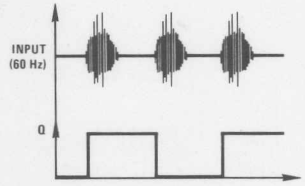
Pulse height = V_{ZENER}



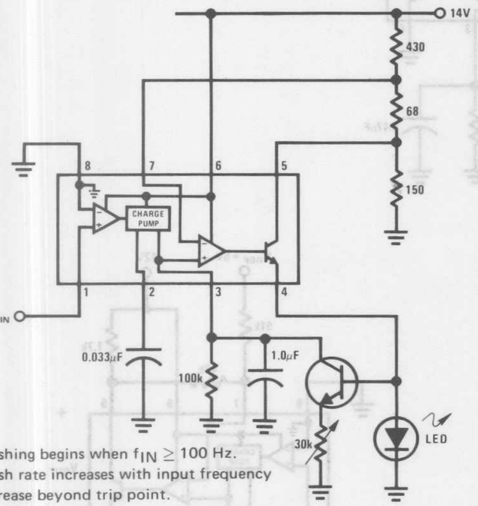
Typical Applications (Continued)

Finger Touch or Contact Switch



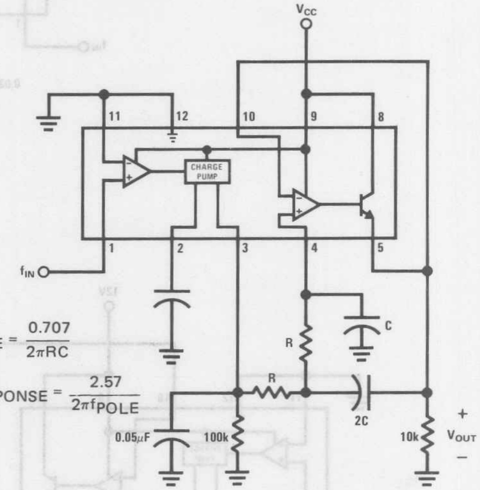


Flashing LED Indicates Overspeed



Flashing begins when $f_{IN} \geq 100$ Hz.
Flash rate increases with input frequency increase beyond trip point.

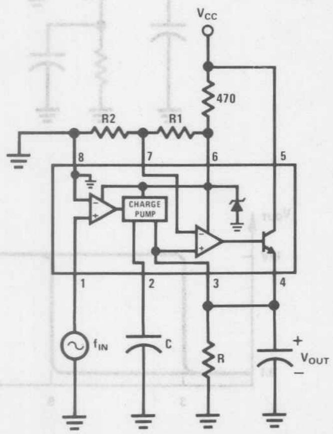
Frequency to Voltage Converter with 2 Pole Butterworth Filter to Reduce Ripple

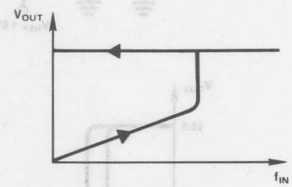


$$f_{POLE} = \frac{0.707}{2\pi RC}$$

$$\tau_{RESPONSE} = \frac{2.57}{2\pi f_{POLE}}$$

Overspeed Latch



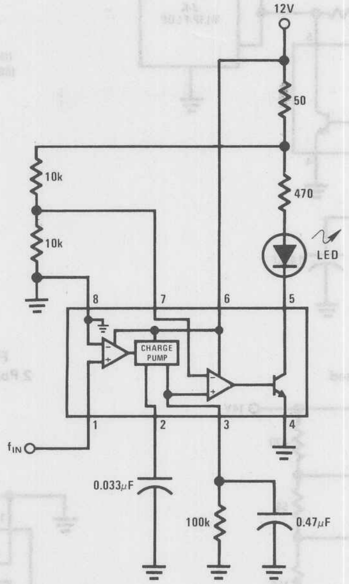


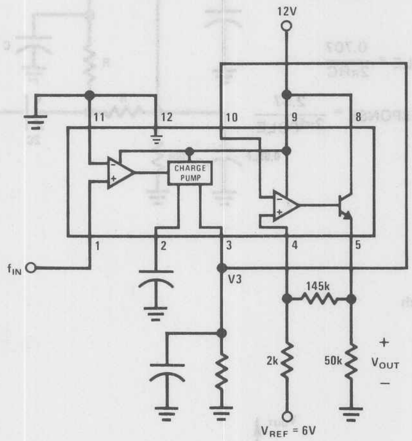
Output latches when

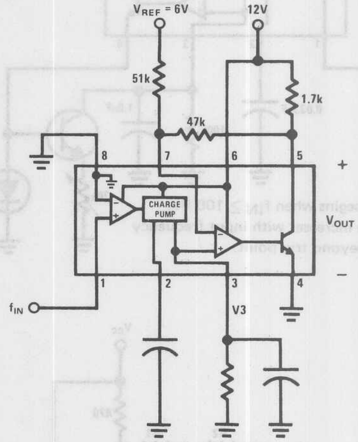
$$f_{IN} = \frac{R2}{R1 + R2} \; \frac{1}{RC}$$

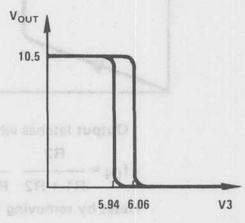
Reset by removing V_{CC}.

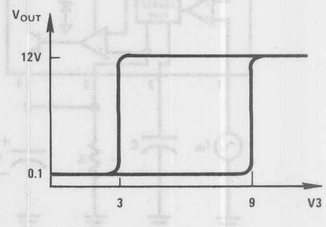
Function Which Can Be Implemented in Several Ways:



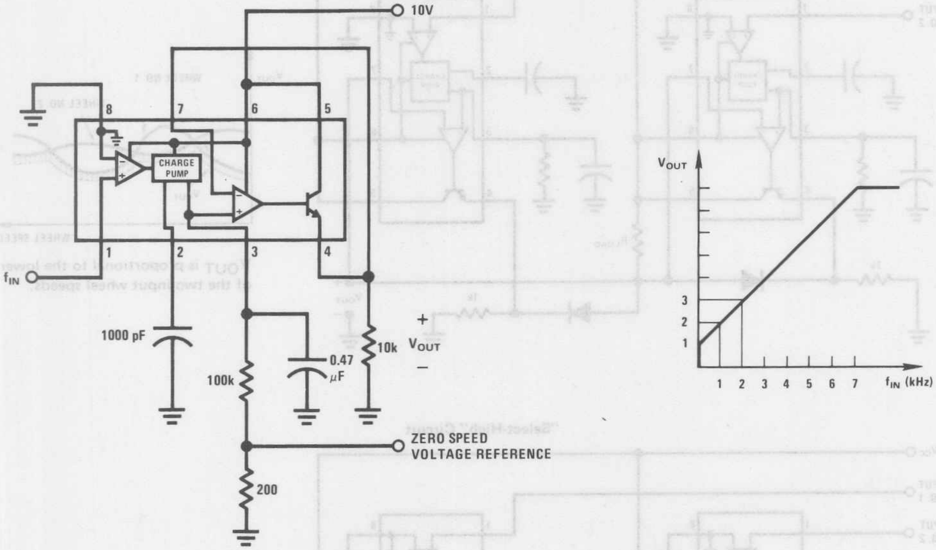




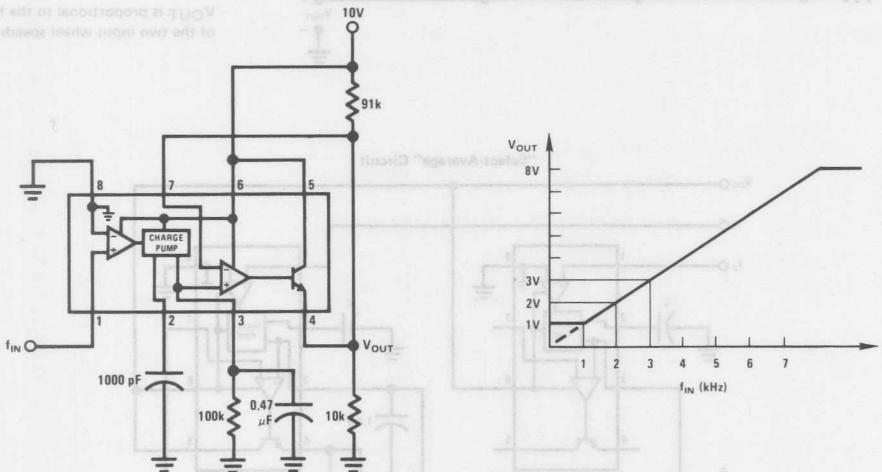




Changing the Output Voltage for an Input Frequency of Zero



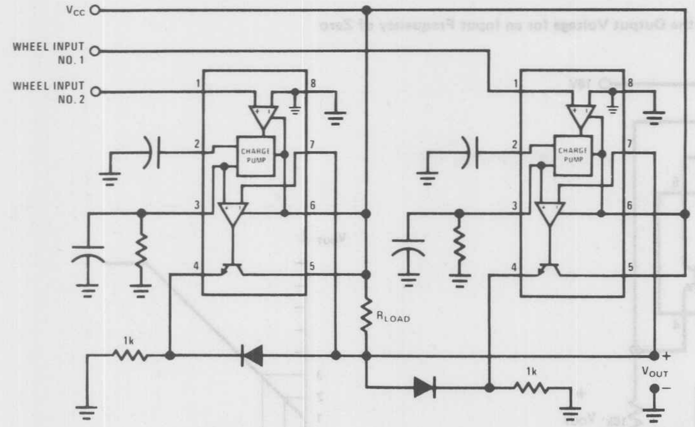
Changing Tachometer Gain Curve or Clamping the Minimum Output Voltage

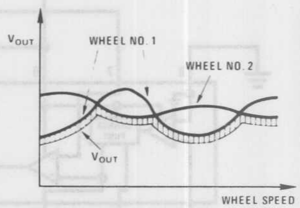


9

Anti-Skid Circuit Functions

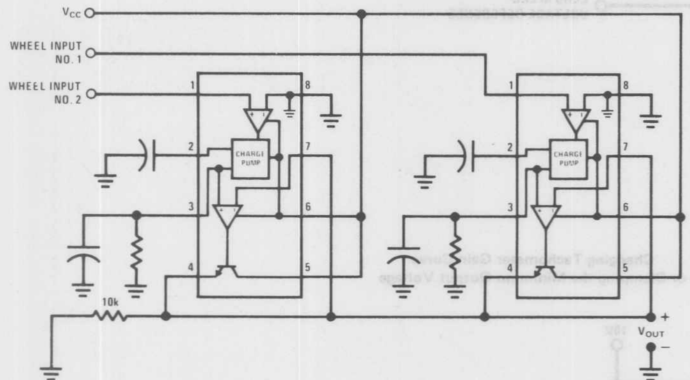
"Select-Low" Circuit

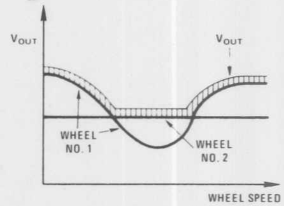




V_{OUT} is proportional to the lower of the two input wheel speeds.

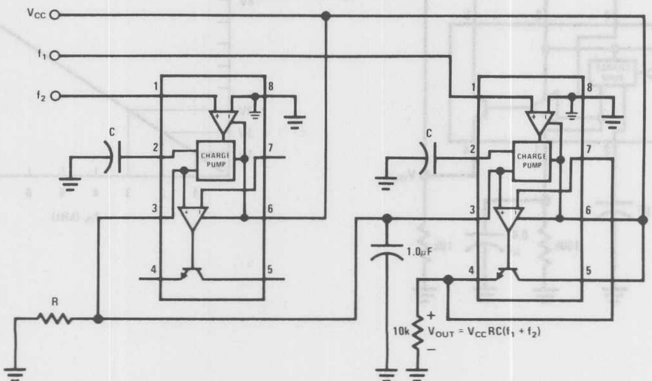
"Select-High" Circuit



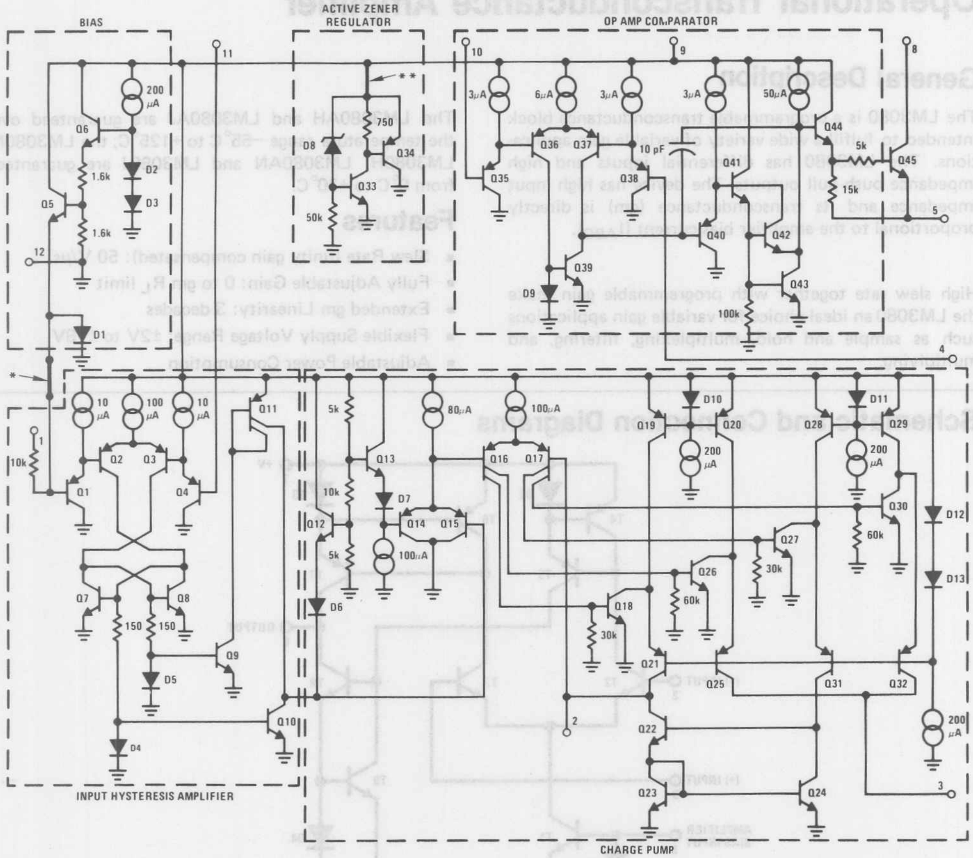


V_{OUT} is proportional to the higher of the two input wheel speeds.

"Select-Average" Circuit



Equivalent Schematic Diagram



* **Note:** This connection made on LM2907-8 and LM2917-8 only.

* * **Note:** This connection made on LM2917 and LM2917-8 only.

LM3080/LM3080A Operational Transconductance Amplifier

General Description

The LM3080 is a programmable transconductance block intended to fulfill a wide variety of variable gain applications. The LM3080 has differential inputs and high impedance push-pull outputs. The device has high input impedance and its transconductance (gm) is directly proportional to the amplifier bias current (I_{ABC}).

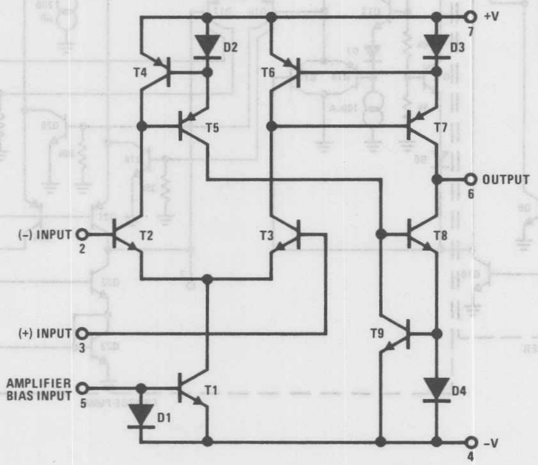
High slew rate together with programmable gain make the LM3080 an ideal choice for variable gain applications such as sample and hold, multiplexing, filtering, and multiplying.

The LM3080AH and LM3080AJ are guaranteed over the temperature range −55°C to +125°C; the LM3080N, LM3080H, LM3080AN and LM3080J are guaranteed from 0°C to +70°C.

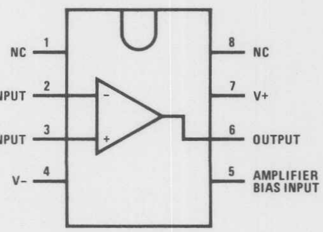
Features

- Slew Rate (unity gain compensated): 50 V/µs
- Fully Adjustable Gain: 0 to gm R_L limit
- Extended gm Linearity: 3 decades
- Flexible Supply Voltage Range: ±2V to ±18V
- Adjustable Power Consumption

Schematic and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number LM3080AJ or LM3080J
See NS Package J08A

Order Number LM3080AN
See NS Package N08B

LM3080A	±22 V
Power Dissipation	250 mW
Differential Input Voltage	±5 V
Amplifier Bias Current (I_{ABC})	2 mA
DC Input Voltage	$+V_S$ to $-V_S$
Output Short Circuit Duration	Indefinite
Operating Temperature Range	
LM3080N, LM3080H, LM3080AN or LM3080J	0°C to +70°C
LM3080AH or LM3080AJ	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

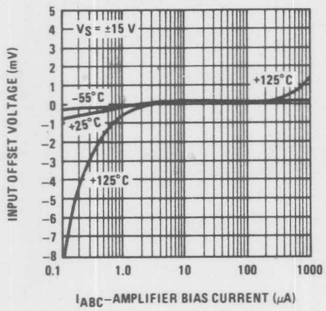
Electrical Characteristics (Note 1)

Parameter	Conditions	LM3080			LM3080A			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage			0.4	5		0.4	2	mV
	Over Specified Temperature Range			6			5	mV
	$I_{ABC} = 5\,\mu A$		0.3			0.3	2	mV
Input Offset Voltage Change	$5\,\mu A \leq I_{ABC} \leq 500\,\mu A$		0.1			0.1	3	mV
Input Offset Current			0.1	0.6		0.1	0.6	µA
Input Bias Current			0.4	5		0.4	5	µA
	Over Specified Temperature Range		1	7		1	8	µA
Forward Transconductance (gm)		6700	9600	13000	7700	9600	12000	µmho
	Over Specified Temperature Range	5400			4000			µmho
Peak Output Current	$R_L = 0$, $I_{ABC} = 5\,\mu A$		5		3	5	7	µA
	$R_L = 0$	350	500	650	350	500	650	µA
	$R_L = 0$ Over Specified Temperature Range	300			300			µA
Peak Output Voltage								
Positive	$R_L = \infty$, $5\,\mu A \leq I_{ABC} \leq 500\,\mu A$	+12	+14.2		+12	+14.2		V
Negative	$R_L = \infty$, $5\,\mu A \leq I_{ABC} \leq 500\,\mu A$	−12	−14.4		−12	−14.4		V
Amplifier Supply Current			1.1			1.1		mA
Input Offset Voltage Sensitivity								
Positive	$\Delta V_{OFFSET}/\Delta V+$		20	150		20	150	µV/V
Negative	$\Delta V_{OFFSET}/\Delta V-$		20	150		20	150	µV/V
Common Mode Rejection Ratio		80	110		80	110		dB
Common Mode Range		±12	±14		±12	±14		V
Input Resistance		10	26		10	26		kΩ
Magnitude of Leakage Current	$I_{ABC} = 0$		0.2	100		0.2	5	nA
Differential Input Current	$I_{ABC} = 0$, Input = ±4 V		0.02	100		0.02	5	nA
Open Loop Bandwidth			2			2		MHz
Slew Rate	Unity Gain Compensated		50			50		V/µs

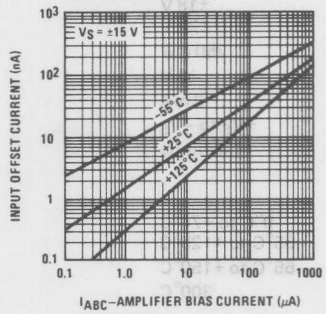
Note 1: These specifications apply for $V_S = \pm 15$ V and $T_A = 25°C$, amplifier bias current (I_{ABC}) = 500 µA, unless otherwise specified.
Note 2: Selections to supply voltage above ±22V, contact the factory.

Typical Performance Characteristics

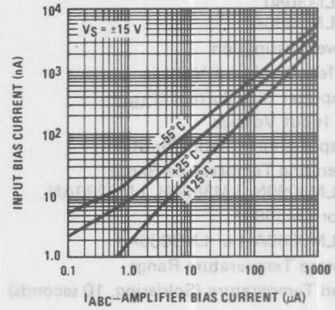
Input Offset Voltage



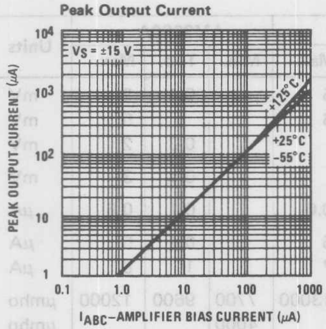
Input Offset Current



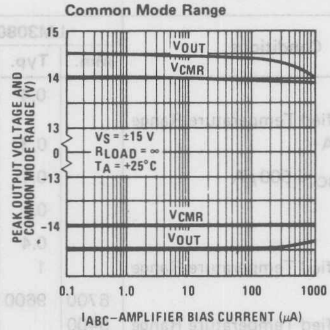
Input Bias Current



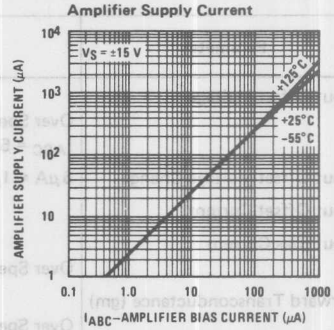
Peak Output Current



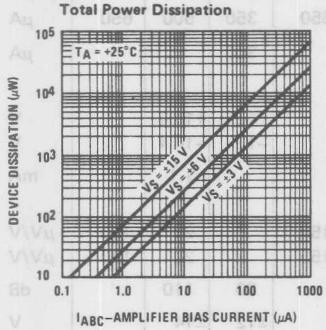
Peak Output Voltage and Common Mode Range



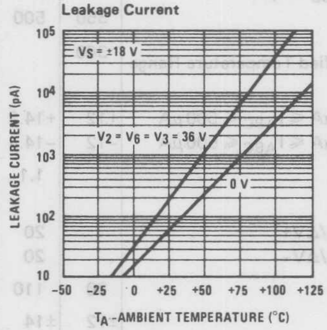
Amplifier Supply Current



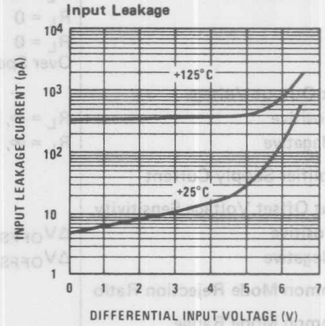
Total Power Dissipation



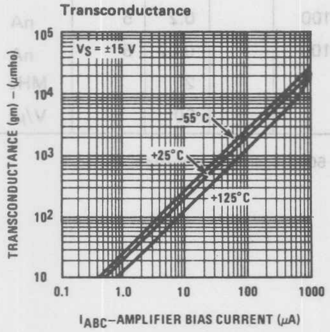
Leakage Current



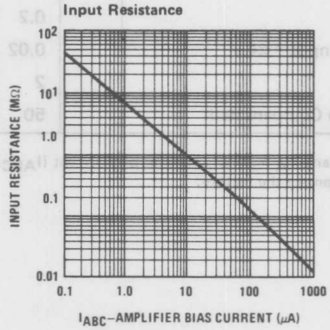
Input Leakage



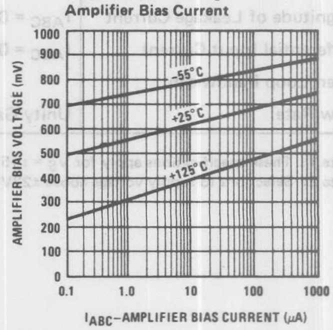
Transconductance



Input Resistance

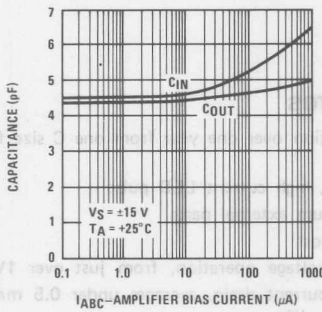


Amplifier Bias Voltage vs Amplifier Bias Current

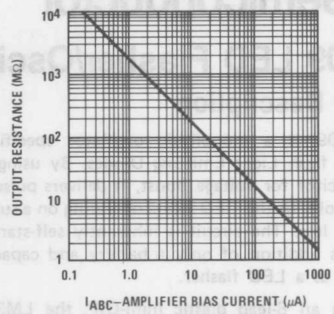


Typical Performance Characteristics (Continued)

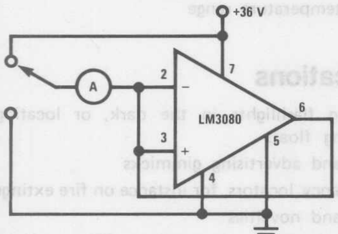
Input and Output Capacitance



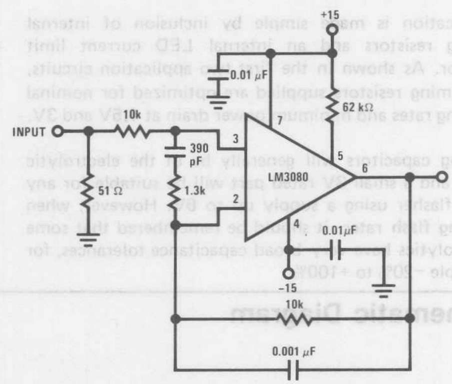
Output Resistance



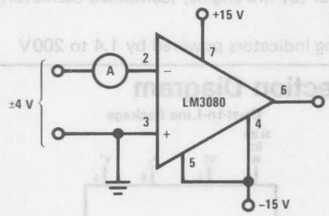
Leakage Current Test Circuit



Unity Gain Follower



Differential Input Current Test Circuit



National Semiconductor

LM3909 LED Flasher/Oscillator

General Description

The LM3909 is a monolithic oscillator specifically designed to flash Light Emitting Diodes. By using the timing capacitor for voltage boost, it delivers pulses of 2 or more volts to the LED while operating on a supply of 1.5V or less. The circuit is inherently self-starting, and requires addition of only a battery and capacitor to function as a LED flasher.

Packaged in an 8-lead plastic mini-DIP, the LM3909 will operate over the extended consumer temperature range of −25°C to +70°C. It has been optimized for low power drain and operation from weak batteries so that continuous operation life exceeds that expected from battery rating.

Application is made simple by inclusion of internal timing resistors and an internal LED current limit resistor. As shown in the first two application circuits, the timing resistors supplied are optimized for nominal flashing rates and minimum power drain at 1.5V and 3V.

Timing capacitors will generally be of the electrolytic type, and a small 3V rated part will be suitable for any LED flasher using a supply up to 6V. However, when picking flash rates, it should be remembered that some electrolytics have very broad capacitance tolerances, for example −20% to +100%.

Features

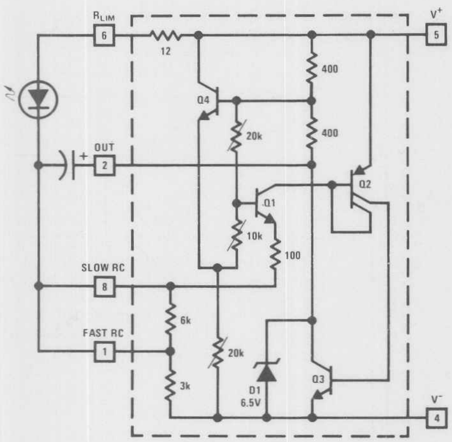
- Operation over one year from one C size flashlight cell
- Bright, high current LED pulse
- Minimum external parts
- Low cost
- Low voltage operation, from just over 1V to 5V
- Low current drain, averages under 0.5 mA during battery life
- Powerful; as an oscillator directly drives an 8Ω speaker
- Wide temperature range

Applications

- Finding flashlights in the dark, or locating boat mooring floats
- Sales and advertising gimmicks
- Emergency locators, for instance on fire extinguishers
- Toys and novelties
- Electronic applications such as trigger and sawtooth generators
- Siren for toy fire engine, (combined oscillator, speaker driver)
- Warning indicators powered by 1.4 to 200V

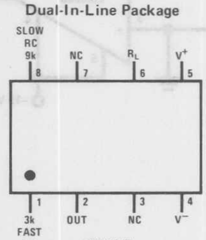
Schematic Diagram

Typical 1.5V Flasher



Connection Diagram

Dual-In-Line Package

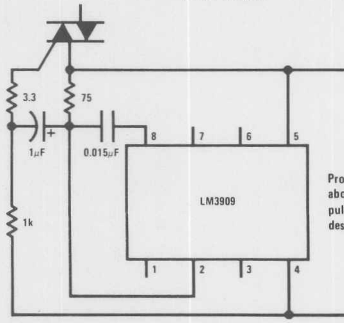


Order Number LM3909N
See NS Package N08B

Typical Application

(See applications notes on page 9-153)

Triac Trigger



Absolute Maximum Ratings

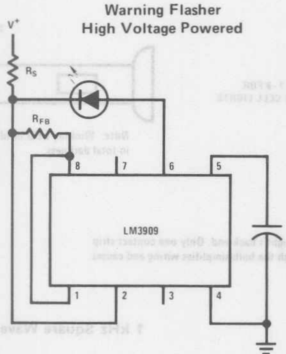
Power Dissipation	500 mW
V^+ Voltage	6.4V
Operating Temperature Range	−25°C to +70°C

Electrical Characteristics

PARAMETER	CONDITIONS (Applications Note 3)	MIN	TYP	MAX	UNITS
Supply Voltage	(In Oscillation)	1.15		6.0	V
Operating Current			0.55	0.75	mA
Flash Frequency	300µF, 5% Capacitor	0.65	1.0	1.3	Hz
High Flash Frequency	0.30µF, 5% Capacitor		1.1		kHz
Compatible LED Forward Drop	1 mA Forward Current	1.35		2.1	V
Peak LED Current	350µF Capacitor		45		mA
Pulse Width	350µF Capacitors at 1/2 Amplitude		6.0		ms

Additional Typical Applications (See applications notes below.)

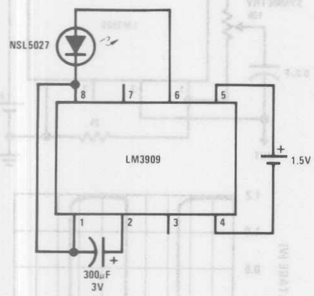
Warning Flasher
High Voltage Powered



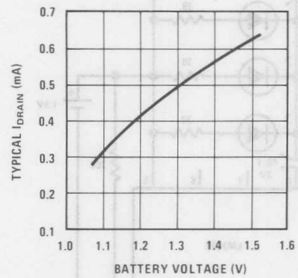
Typical Operating Conditions

V^+	NOMINAL FLASH Hz	C_T	R_S	R_{FB}	V^+_{RANGE}
6V	2	400µF	1k	1.5k	5–25V
15V	2	180µF	3.9k	1k	13–50V
100V	1.7	180µF	43k 1W	1k	85–200V

1.5V Flasher



Note: Nominal flash rate: 1 Hz.



Estimated Battery Life
(Continuous 1.5V Flasher Operation)

SIZE CELL	TYPE	
	STANDARD	ALKALINE
AA	3 months	6 months
C	7 months	15 months
D	1.3 years	2.6 years

Note: Estimates are made from our tests and manufacturers data. Conditions are fresh batteries and room temperature. Clad or "leak-proof" batteries are recommended for any application of five months or more. Nickel Cadmium cells are not recommended.

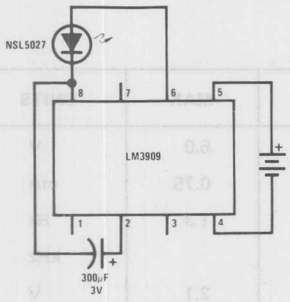
APPLICATIONS NOTES

Note 1: All capacitors shown are electrolytic unless marked otherwise.

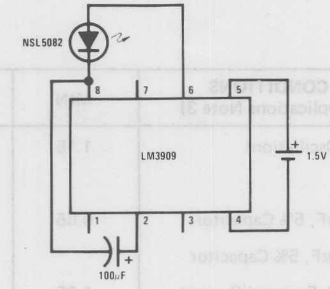
Note 2: Flash rates and frequencies assume a ±5% capacitor tolerance. Electrolytics may vary −20% to +100% of their stated value.

Note 3: Unless noted, measurements above are made with a 1.4V supply, a 25°C ambient temperature, and a LED with a forward drop of 1.5V to 1.7V at 1 mA forward current.

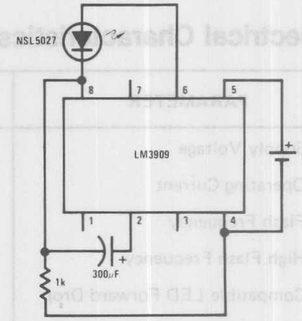
Note 4: Occasionally a flasher circuit will fail to oscillate due to a LED defect that may be missed because it only reduces light output 10% or so. Such LEDs can be identified by a large increase in conduction between 0.9V and 1.2V.



Note: Nominal flash rate: 1 Hz. Average I_{DRAIN} = 0.77 mA.

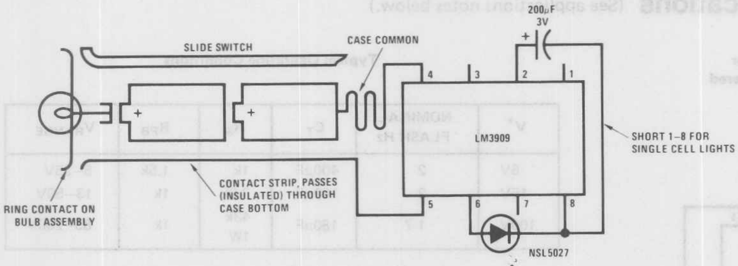


Note: Nominal flash rate: 1.1 Hz. Average I_{DRAIN} = 0.32 mA.



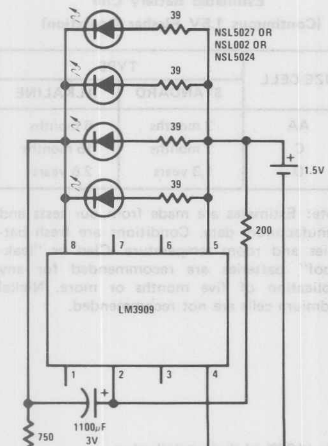
Note: Nominal flash rate: 2.6 Hz. Average I_{DRAIN} = 1.2 mA.

Flashlight Finder



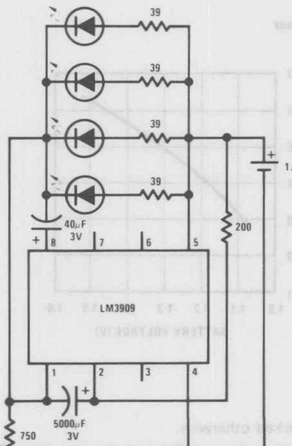
Note: LM3909, capacitor, and LED are installed in a white translucent cap on the flashlight's back end. Only one contact strip (in addition to the case connection) is needed for flasher power. Drawing current through the bulb simplifies wiring and causes negligible loss since bulb resistance cold is typically less than 2Ω.

4 Parallel LEDs



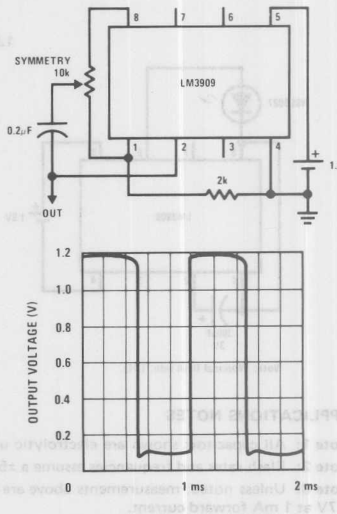
Note: Nominal flash rate: 1.3 Hz. Average I_{DRAIN} = 2 mA.

High Efficiency Parallel Circuit



Note. Nominal flash rate: 1.5 Hz. Average I_{DRAIN} = 1.5 mA.

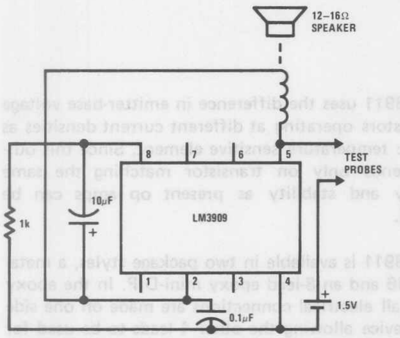
1 kHz Square Wave Oscillator



Note: Output voltage through a 10k load to ground.

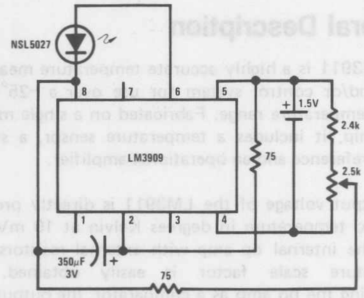
Typical Applications (Continued) (See applications notes on page 9-153)

"Buzz Box" Continuity and Coil Checker



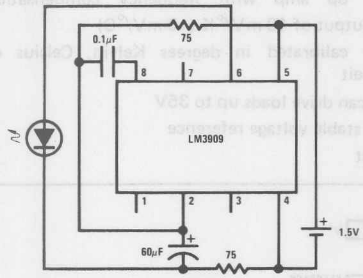
Note: Differences between shorts, coils, and a few ohms of resistance can be heard.

Variable Flasher



Note: Flash rate: 0–20 Hz.

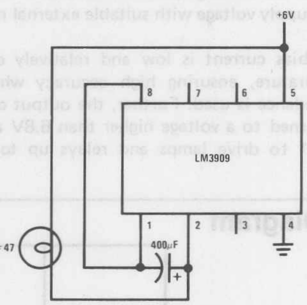
LED Booster



Note: High efficiency, 4 mA drain.

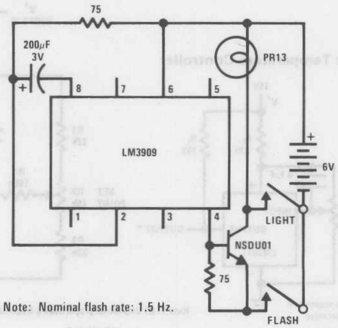
Note: Continuous appearing light obtained by supplying short, high current, pulses (2 kHz) to LEDs with higher than battery voltage available.

Incandescent Bulb Flasher



Note: Flash rate: 1.5 Hz.

Emergency Lantern/Flasher



Note: Nominal flash rate: 1.5 Hz.

National Semiconductor

LM3911 Temperature Controller

General Description

The LM3911 is a highly accurate temperature measurement and/or control system for use over a −25°C to +85°C temperature range. Fabricated on a single monolithic chip, it includes a temperature sensor, a stable voltage reference and an operational amplifier.

The output voltage of the LM3911 is directly proportional to temperature in degrees Kelvin at 10 mV/°K. Using the internal op amp with external resistors any temperature scale factor is easily obtained. By connecting the op amp as a comparator, the output will switch as the temperature transverses the set-point making the device useful as an on-off temperature controller.

An active shunt regulator is connected across the power leads of the LM3911 to provide a stable 6.8V voltage reference for the sensing system. This allows the use of any power supply voltage with suitable external resistors.

The input bias current is low and relatively constant with temperature, ensuring high accuracy when high source impedance is used. Further, the output collector can be returned to a voltage higher than 6.8V allowing the LM3911 to drive lamps and relays up to a 35V supply.

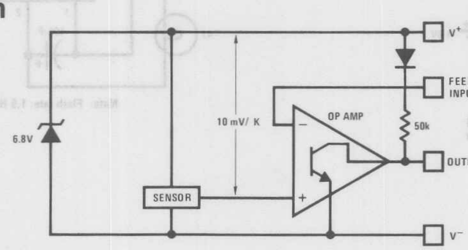
The LM3911 uses the difference in emitter-base voltage of transistors operating at different current densities as the basic temperature sensitive element. Since this output depends only on transistor matching the same reliability and stability as present op amps can be expected.

The LM3911 is available in two package styles, a metal can TO-46 and an 8-lead epoxy mini-DIP. In the epoxy package all electrical connections are made on one side of the device allowing the other 4 leads to be used for attaching the LM3911 to the temperature source. The LM3911 is rated for operation over a −25°C to +85°C temperature range.

Features

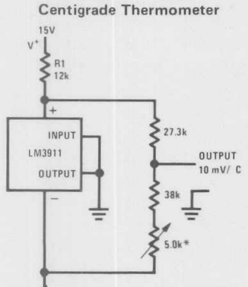
- Uncalibrated accuracy ±10°C
- Internal op amp with frequency compensation
- Linear output of 10 mV/°K (10 mV/°C)
- Can be calibrated in degrees Kelvin, Celsius or Fahrenheit
- Output can drive loads up to 35V
- Internal stable voltage reference
- Low cost

Block Diagram



Typical Applications

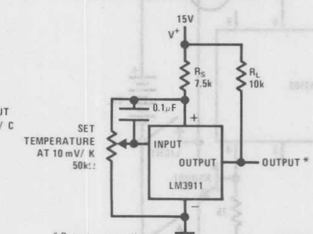
Ground Referred Centigrade Thermometer



R1 = 1000 (V+ − 3.0V)
R2 = 500 (V− − 4.0V)

* Trims out initial zener tolerance. Set output to read C

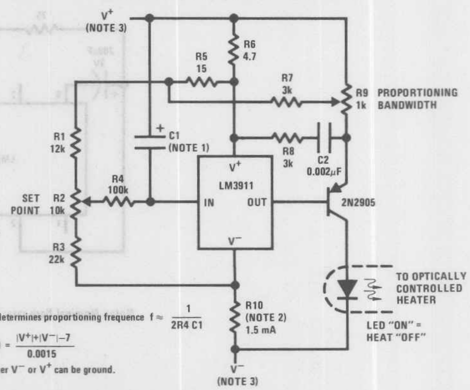
Basic Temperature Controller



* Output goes negative on temperature increase

$R_S = (V^+ - 6.8V)$ kΩ

Proportioning Temperature Controller



Note 1: C1 determines proportioning frequence $f \approx \frac{1}{2R4\,C1}$

Note 2: $R10 = \frac{|V^+| + |V^-| - 7}{0.0015}$

Note 3: Either V− or V+ can be ground.

Absolute Maximum Ratings

Supply Current (Externally Set)	10 mA	Operating Temperature Range	−25°C to +85°C
Output Collector Voltage, V^{++}	36V	Storage Temperature Range	−65°C to +150°C
Feedback Input Voltage Range	0V to +7.0V	Lead Temperature (Soldering, 10 seconds)	300°C
Output Short Circuit Duration	Indefinite		

Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SENSOR					
Output Voltage	$T_A = -25°C$, (Note 2)	2.36	2.48	2.60	V
Output Voltage	$T_A = 25°C$, (Note 2)	2.88	2.98	3.08	V
Output Voltage	$T_A = 85°C$, (Note 2)	3.46	3.58	3.70	V
Linearity	$\Delta T = 100°C$		0.5	2	%
Long-Term Stability			0.3		%
Repeatability			0.3		%
VOLTAGE REFERENCE					
Reverse Breakdown Voltage	$1\ mA \leq I_Z \leq 5\ mA$	6.55	6.85	7.25	V
Reverse Breakdown Voltage Change With Current	$1\ mA \leq I_Z \leq 5\ mA$		10	35	mV
Temperature Stability			20	85	mV
Dynamic Impedance	$I_Z = 1\ mA$		3.0		Ω
RMS Noise Voltage	$10\ Hz \leq f \leq 10\ kHz$		30		μV
Long Term Stability	$T_A = +85°C$		6.0		mV
OP AMP					
Input Bias Current	$T_A = +25°C$		35	150	nA
Input Bias Current			45	250	nA
Voltage Gain	$R_L = 36k$, $V^{++} = 36V$	2500	15000		V/V
Output Leakage Current	$T_A = 25°C$ (Note 3)		0.2	2	μA
Output Leakage Current	(Note 3)		1.0	8	μA
Output Source Current	$V_{OUT} \leq 3.70$	10			μA
Output Sink Current	$1V \leq V_{OUT} \leq 36V$	2.0			mA

Note 1: These specifications apply for $-25°C \leq T_A \leq +85°C$ and $0.9\ mA \leq I_{SUPPLY} \leq 1.1\ mA$ unless otherwise specified; $C_L \leq 50\ pF$.

Note 2: The output voltage applies to the basic thermometer configuration with the output and input terminals shorted and a load resistance of ≥ 1.0 MΩ. This is the feedback sense voltage and includes errors in both the sensor and op amp. This voltage is specified for the sensor in a rapidly stirred oil bath. The output is referred to V^+.

Note 3: The output leakage current is specified with ≥ 100 mV overdrive. Since this voltage changes with temperature, the voltage drive for turn-off changes and is defined as V_{OUT} (with output and input shorted) −100 mV. This specification applies for $V_{OUT} = 36V$.

Application Hints

Although the LM3911 is designed to be totally trouble-free, certain precautions should be taken to insure the best possible performance.

As with any temperature sensor, internal power dissipation will raise the sensor's temperature above ambient. Nominal suggested operating current for the shunt regulator is 1.0 mA and causes 7.0 mW of power dissipation. In free, still, air this raises the package temperature by about 1.2°K. Although the regulator will operate at higher reverse currents and the output will drive loads up to 5.0 mA, these higher currents will raise the sensor temperature to about 19°K above ambient—degrading accuracy. Therefore, the sensor should be operated at the lowest possible power level.

With moving air, liquid or surface temperature sensing, self-heating is not as great a problem since the measured media will conduct the heat from the sensor. Also, there are many small heat sinks designed for transistors which will improve heat transfer to the sensor from the surrounding medium. A small finned clip-on heat sink is quite effective in free-air. It should be mentioned that the LM3911 die is on the base of the package and therefore coupling to the base is preferrable.

The internal reference regulator provides a temperature stable voltage for offsetting the output or setting a comparison point in temperature controllers. However, since this reference is at the same temperature as the sensor temperature changes will also cause reference drift. For application where maximum accuracy is needed an external reference should be used. Of course, for fixed temperature controllers the internal reference is adequate.

Typical Performance Characteristics

Temperature Conversion

$$T_{CENTIGRADE} = T_C$$

$$T_{FAHRENHEIT} = T_F$$

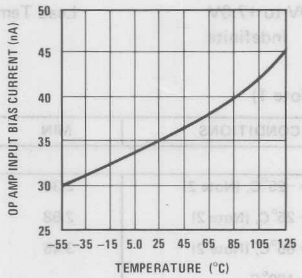
$$T_{KELVIN} = T_K$$

$$T_K = T_C + 273$$

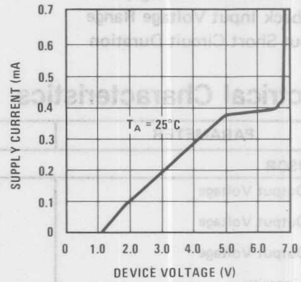
$$T_C = (40 + T_F)\ \frac{5}{9}\ - 40$$

$$T_F = (40 + T_C)\ \frac{9}{5}\ - 40$$

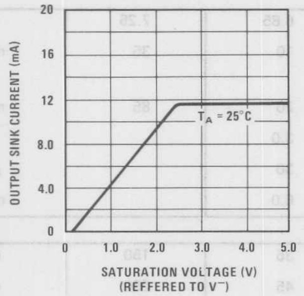
Op Amp Input Current



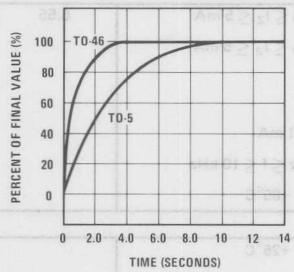
Power Supply Current



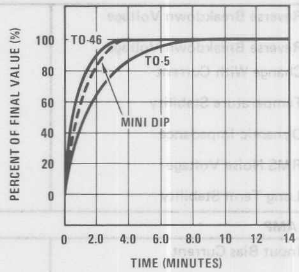
Output Saturation Voltage



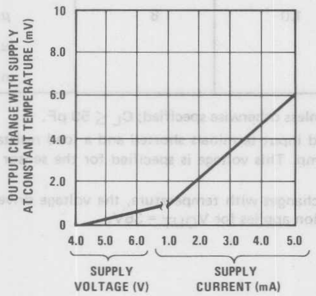
Thermal Time Constant in Stirred Oil Bath



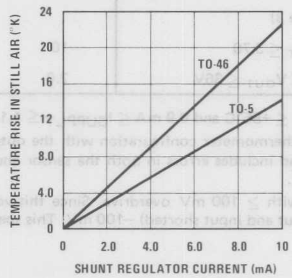
Thermal Time Constant in Still Air



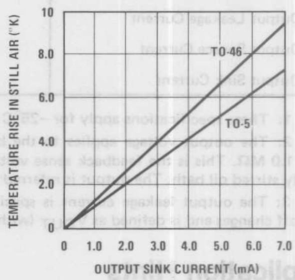
Supply Sensitivity



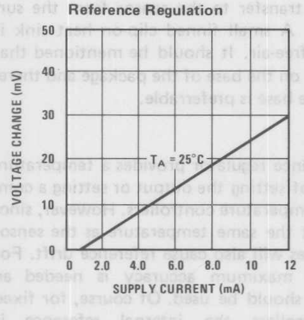
Device Temperature Rise



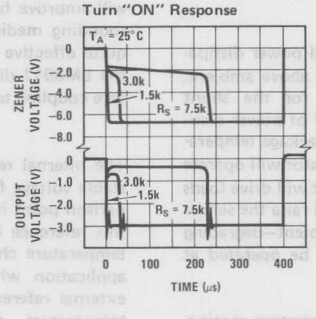
Device Temperature Rise



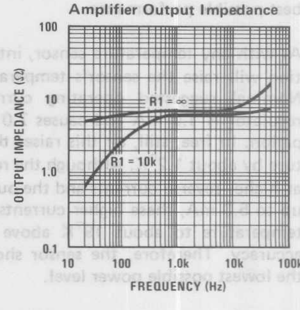
Reference Regulation



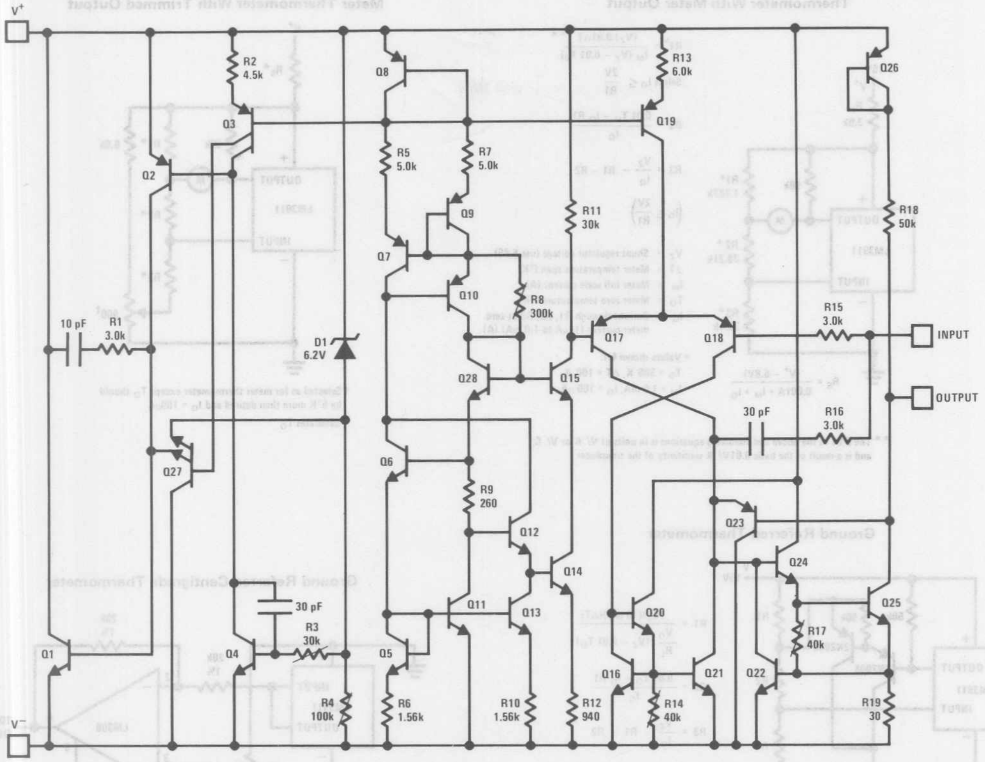
Turn "ON" Response



Amplifier Output Impedance

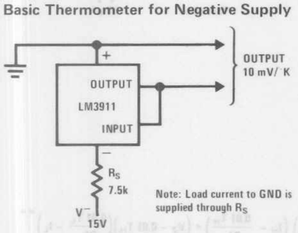


Schematic Diagram



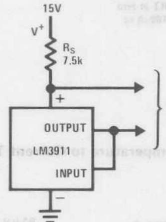
Typical Applications (Continued)

Basic Thermometer for Negative Supply



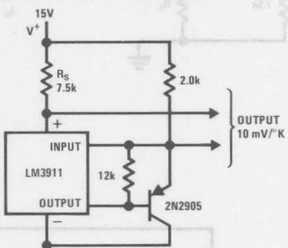
$R_S = (V^- - 6.8V) \times 10^3\Omega$

Basic Thermometer for Positive Supply



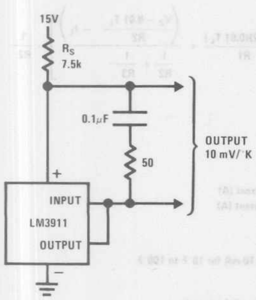
$R_S = (V^- - 6.8V) \times 10^3\Omega$

Increasing Gain and Output Drive

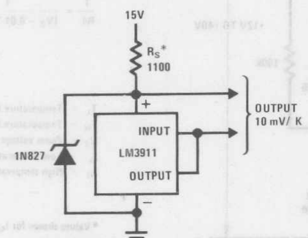


$R_S = (V^+ - 6.8V) \times 10^3\Omega$

External Frequency Compensation for Greater Stability when Driving Capacitive Loads

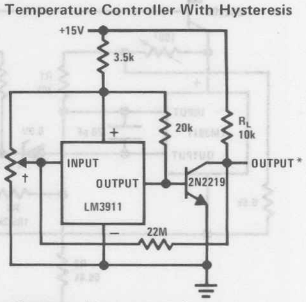


Operating With External Zener for Lower Power Dissipation and Ambient Reference



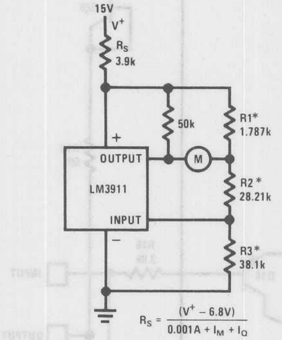
* Depends on Zener current.

Temperature Controller With Hysteresis



* Output goes positive on temperature increase

†Set temperature



$$R1 = \frac{\ldots}{I_M (V_Z - 0.01\,T_O)}$$

Select $I_Q \le \frac{2V}{R1}$

$$R2 = \frac{0.01\,T_O - I_Q\,R1}{I_Q}$$

$$R3 = \frac{V_Z}{I_Q} - R1 - R2$$

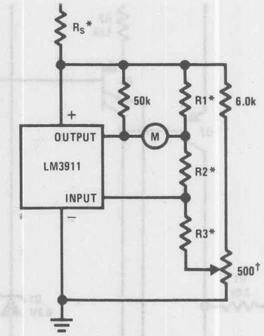
$$\left(I_Q \le \frac{2V}{R1}\right)$$

V_Z = Shunt regulator voltage (use 6.85)
ΔT = Meter temperature span (°K)
I_M = Meter full scale current (A)
T_O = Meter zero temperature (°K)
I_Q = Current through R1, R2, R3 at zero meter current (10μA to 1.0 mA) (A)

*Values shown for:
T_O = 300°K, ΔT = 100°K,
I_M = 1.0 mA, I_Q = 100 μA

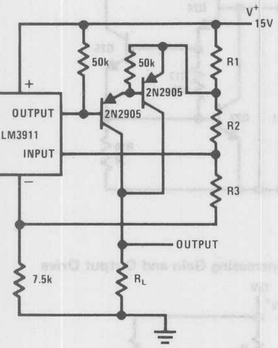
$$R_S = \frac{(V^+ - 6.8V)}{0.001A + I_M + I_Q}$$

**The 0.01 in the above and following equations is in units of V/°K or V/°C, and is a result of the basic 0.01V/°K sensitivity of the transducer



*Selected as for meter thermometer except T_O should be 5°K more than desired and I_Q = 100μA
†Calibrates T_O

Ground Referred Thermometer



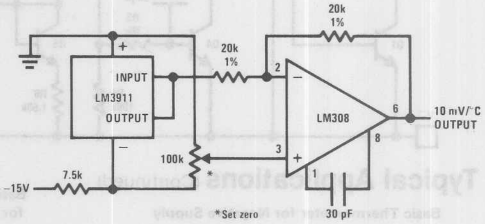
$$R1 = \frac{(V_Z)(10\text{ mV})(\Delta T)}{\frac{V_O}{R_L}(V_Z - 0.01\,T_O)}$$

$$R2 = \frac{0.01\,T_O - I_Q\,R1}{I_Q}$$

$$R3 = \frac{V_Z}{I_Q} - R1 - R2$$

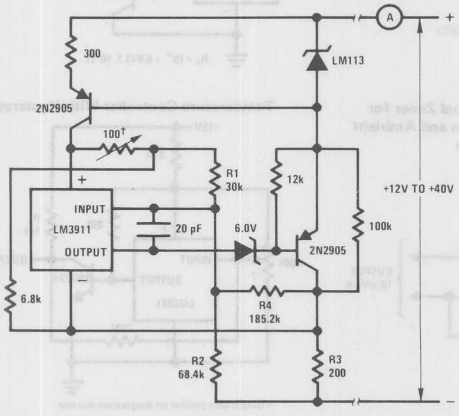
V_Z = Shunt regulator voltage
ΔT = Temperature span (°K)
T_O = Temperature for zero output (°K)
V_O = Full scale output voltage $\le$ 10V
I_Q = Current through R1, R2, R3 at zero output voltage (typically 100μA to 1.0 mA)

Ground Referred Centigrade Thermometer



*Set zero

Two Terminal Temperature to Current Transducer*



$$R2\,(\Omega) = \frac{\left(V_Z - 0.01\,T_L\right)\left(I_H - \frac{0.01\,T_H}{R1}\right) + \left(V_Z - 0.01\,T_H\right)\left(\frac{0.01\,T_L}{R1} - I_L\right)}{\frac{0.01}{R1\,R3}\left[T_H\,(V_Z - 0.01\,T_L) - T_L\,(V_Z - 0.01\,T_H)\right]}^{**}$$

$$R3\,(\Omega) \ge \frac{V_Z\left(\frac{T_H}{T_L} - 1\right)}{I_H - \frac{I_L\,T_H}{T_L}}$$

$$\frac{1}{R4} = \frac{1}{(V_Z - 0.01\,T_L)(R2)}\left[\frac{(R2)(0.01\,T_L)}{R1} + \frac{\left(\frac{V_Z - 0.01\,T_L}{R2} - I_L\right)}{\frac{1}{R2} + \frac{1}{R3}}\right] - \frac{1}{R2}$$

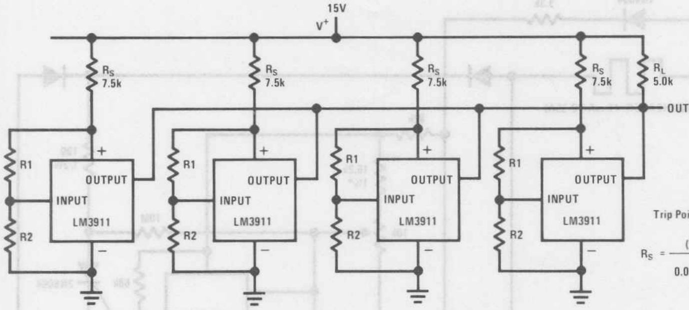
T_L = Temperature for I_L (°K)
T_H = Temperature for I_H (°K)
V_Z = Zener voltage (V)
I_L = Low temperature output current (A)
I_H = High temperature output current (A)

*Values shown for I_{OUT} = 1 mA to 10 mA for 10°F to 100°F
†Set temperature

**The 0.01 in the above and following equations is in units of V/°K or V/°C, and is a result of the basic 0.01V/°K sensitivity of the transducer

Typical Applications (Continued)

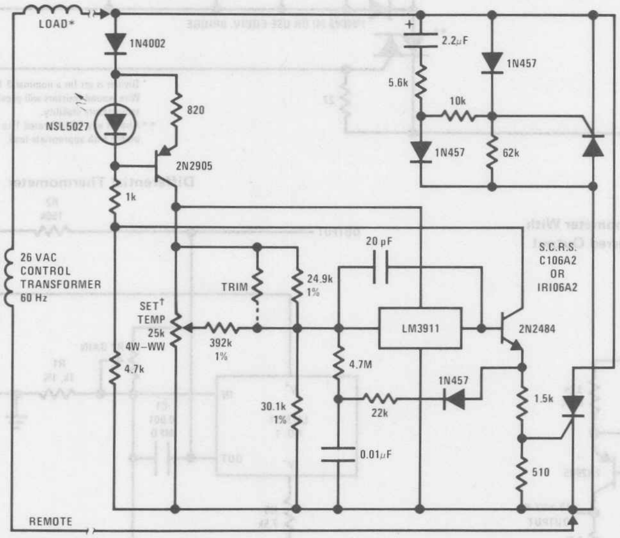
Over Temperature Detectors With Common Output



$$\text{Trip Point} = V_Z \frac{R1}{R1 + R2}$$

$$R_S = \frac{(V^+ - 6.8V)}{0.001A + \frac{6.8V}{R1 + R2}}$$

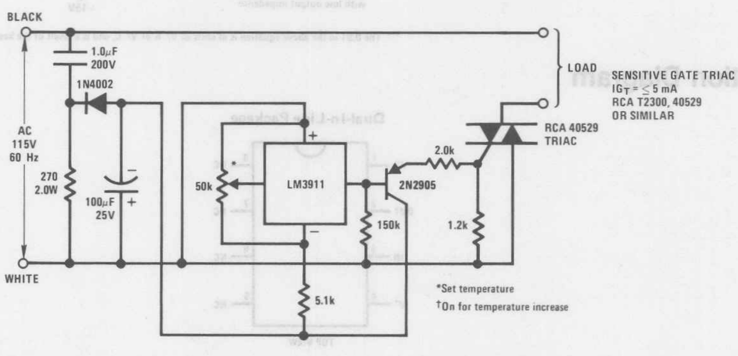
Two-Wire Remote A.C. Electronic Thermostat (Gas or Oil Furnace Control)



* Solenoid or 6–15W heater

†Pot will provide about a 50°F to 90°F setting range. The trim resistor (100k) is selected to bring 70°F near the middle of the pot rotation.

SCR heating, by proper positioning, can preheat the sensor giving control anticipation as is presently used in many home thermostats.

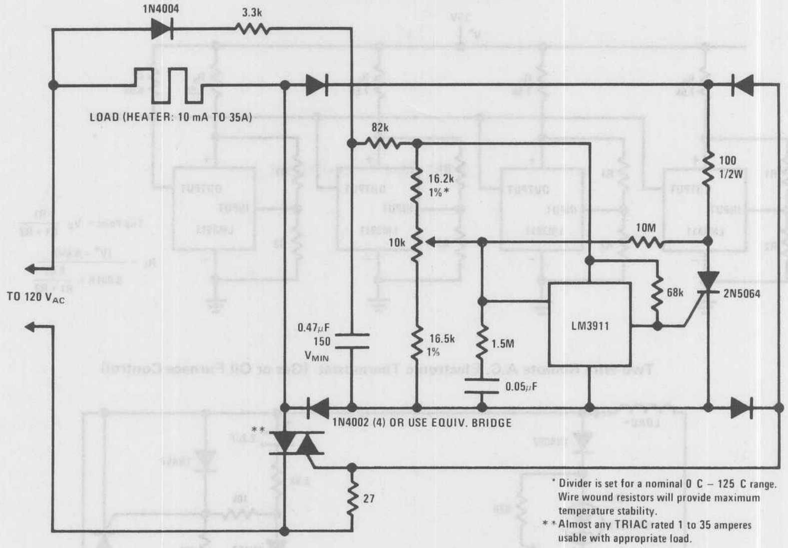


*Set temperature

†On for temperature increase

Typical Applications (Continued)

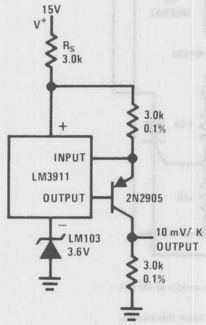
Three-Wire Electronic Thermostat



* Divider is set for a nominal 0°C – 125°C range. Wire wound resistors will provide maximum temperature stability.

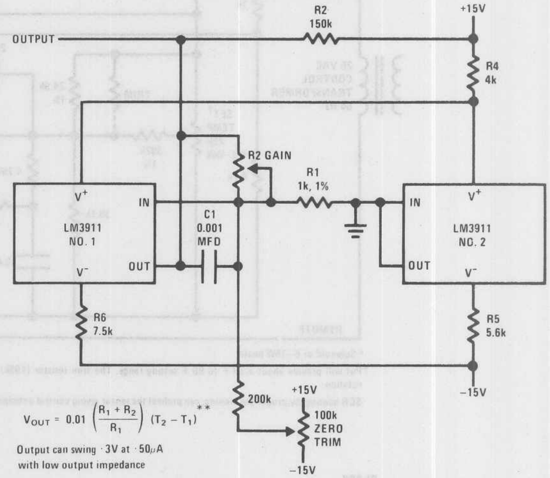
** Almost any TRIAC rated 1 to 35 amperes usable with appropriate load.

Kelvin Thermometer With Ground Referred Output



$$R_S = \frac{V_S^{+} - 6.8V \times 10^{3}\Omega}{2}$$

Differential Thermometer



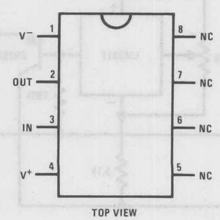
$$V_{OUT} = 0.01 \left(\frac{R_1 + R_2}{R_1}\right)(T_2 - T_1)^{**}$$

Output can swing ±3V at ±50μA with low output impedance

** The 0.01 in the above equation is in units of V/°K or V/°C, and is a result of the basic 0.01 V/°K sensitivity of the transducer

Connection Diagram

Dual-In-Line Package



Order Number LM3911N
See NS Package N08B

National Semiconductor

Industrial Blocks

LM3914 Dot/Bar Display Driver

General Description

The LM3914 is a monolithic integrated circuit that senses analog voltage levels and drives 10 LEDs, providing a linear analog display. A single pin changes the display from a moving dot to a bar graph. Current drive to the LEDs is regulated and programmable, eliminating the need for resistors. This feature is one that allows operation of the whole system from less than 3V.

The circuit contains its own adjustable reference and accurate 10-step voltage divider. The low-bias-current input buffer accepts signals down to ground, or V^-, yet needs no protection against inputs of 35V above or below ground. The buffer drives 10 individual comparators referenced to the precision divider. Indication non-linearity can thus be held typically to 1/2%, even over a wide temperature range.

Versatility was designed into the LM3914 so that controller, visual alarm, and expanded scale functions are easily added on to the display system. The circuit can drive LEDs of many colors, or low-current incandescent lamps. Many LM3914s can be "chained" to form displays of 20 to over 100 segments. Both ends of the voltage divider are externally available so that 2 drivers can be made into a zero-center meter.

The LM3914 is very easy to apply as an analog meter circuit. A 1.2V full-scale meter requires only 1 resistor and a single 3V to 15V supply in addition to the 10 display LEDs. If the 1 resistor is a pot, it becomes the LED brightness control. The simplified block diagram illustrates this extremely simple external circuitry.

When in the dot mode, there is a small amount of overlap or "fade" (about 1 mV) between segments. This assures that at no time will all LEDs be "OFF", and thus any ambiguous display is avoided. Various novel displays are possible.

Much of the display flexibility derives from the fact that all outputs are individual, DC regulated currents. Various effects can be achieved by modulating these currents. The individual outputs can drive a transistor as well as a LED at the same time, so controller functions including "staging" control can be performed. The LM3914 can also act as a programmer, or sequencer.

Features

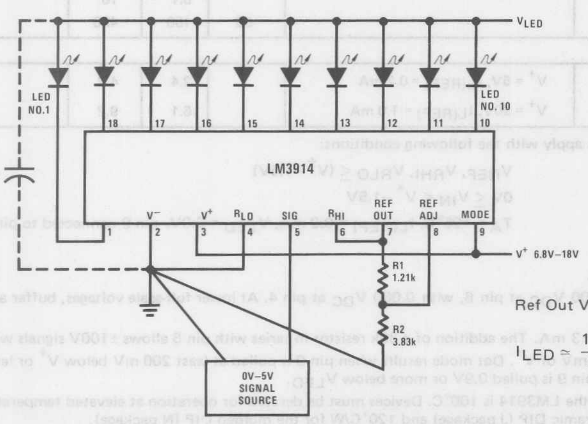
- Drives LEDs, LCDs or vacuum fluorescents
- Bar or dot display mode externally selectable by user
- Expandable to displays of 100 steps
- Internal voltage reference from 1.2V to 12V
- Operates with single supply of less than 3V
- Inputs operate down to ground
- Output current programmable from 2 to 30 mA
- No multiplex switching or interaction between outputs
- Input withstands ±35V without damage or false outputs
- LED driver outputs are current regulated, open-collectors
- Outputs can interface with TTL or CMOS logic
- The internal 10-step divider is floating and can be referenced to a wide range of voltages

The LM3914 is rated for operation from 0°C to +70°C. The LM3914N is available in an 18-lead molded (N) package and the LM3914J comes in the 18-lead ceramic DIP.

The following typical application illustrates adjusting of the reference to a desired value, and proper grounding for accurate operation, and avoiding oscillations.

Typical Applications

0V to 5V Bar Graph Meter



Note 1: Grounding method is typical of *all* uses. The 2.2 µF tantalum or 10 µF aluminum electrolytic capacitor is needed if leads to the LED supply are 6" or longer.

$$\text{Ref Out V} = 1.25\left(1 + \frac{R2}{R1}\right)$$

$$I_{LED} \simeq \frac{12.5}{R1}$$

Molded DIP (N)	625 mW	Reference Load Current	10 mA
Supply Voltage	25V	Storage Temperature Range	−55°C to +150°C
Voltage on Output Drivers	25V	Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS (Note 1)	MIN	TYP	MAX	UNITS
COMPARATOR					
Offset Voltage, Buffer and First Comparator	$0V \leq V_{RLO} = V_{RHI} \leq 12V$, $I_{LED} = 1$ mA		3	10	mV
Offset Voltage, Buffer and Any Other Comparator	$0V \leq V_{RLO} = V_{RHI} \leq 12V$, $I_{LED} = 1$ mA		3	15	mV
Gain ($\Delta I_{LED}/\Delta V_{IN}$)	$I_{L(REF)} = 2$ mA, $I_{LED} = 10$ mA	3	8		mA/mV
Input Bias Current (at Pin 5)	$0V \leq V_{IN} \leq V^+ -1.5V$		10	50	nA
Input Signal Overvoltage	No Change in Display	−35		35	V
VOLTAGE-DIVIDER					
Divider Resistance	Total, Pin 6 to 4	6.5	10	15	kΩ
Accuracy	(Note 2)		0.5	2	%
VOLTAGE REFERENCE					
Output Voltage	$0.1\text{ mA} \leq I_{L(REF)} \leq 4$ mA, $V^+ = V_{LED} = 5V$	1.2	1.28	1.34	V
Line Regulation	$3V \leq V^+ \leq 18V$		0.01	0.03	%/V
Load Regulation	$0.1\text{ mA} \leq I_{L(REF)} \leq 4$ mA, $V^+ = V_{LED} = 5V$		0.4	2	%
Output Voltage Change With Temperature	$0°C \leq T_A \leq +70°C$, $I_{L(REF)} = 1$ mA, $V^+ = 5V$		1		%
Adjust Pin Current			75	120	μA
OUTPUT DRIVERS					
LED Current	$V^+ = V_{LED} = 5V$, $I_{L(REF)} = 1$ mA	7	10	13	mA
LED Current Difference (Between Largest and Smallest LED Currents)	$V_{LED} = 5V$, $I_{LED} = 2$ mA		0.12	0.4	mA
	$V_{LED} = 5V$, $I_{LED} = 20$ mA		1.2	3	mA
LED Current Regulation	$2V \leq V_{LED} \leq 17V$ $I_{LED} = 2$ mA		0.1	0.25	mA
	$I_{LED} = 20$ mA		1	3	mA
Dropout Voltage	$I_{LED(ON)} = 20$ mA, $V_{LED} = 5V$, $\Delta I_{LED} = 2$ mA			1.5	V
Saturation Voltage	$I_{LED} = 2.0$ mA, $I_{L(REF)} = 0.4$ mA		0.15	0.4	V
Output Leakage, Each Collector	(Bar Mode) (Note 4)		0.1	10	μA
Output Leakage	(Dot Mode) (Note 4)				
Pins 10–18			0.1	10	μA
Pin 1		60	150	450	μA
SUPPLY CURRENT					
Standby Supply Current (All Outputs Off)	$V^+ = 5V$, $I_{L(REF)} = 0.2$ mA		2.4	4.2	mA
	$V^+ = 20V$, $I_{L(REF)} = 1.0$ mA		6.1	9.2	mA

Note 1: Unless otherwise stated, all specifications apply with the following conditions:

$3\ V_{DC} \leq V^+ \leq 20\ V_{DC}$ $\quad$ $V_{REF}, V_{RHI}, V_{RLO} \leq (V^+ -1.5V)$

$3\ V_{DC} \leq V_{LED} \leq V^+$ $\quad$ $0V \leq V_{IN} \leq V^+ -1.5V$

$-0.015V \leq V_{RLO} \leq 12\ V_{DC}$ $\quad$ $T_A = +25°C$, $I_{L(REF)} = 0.2$ mA, $V_{LED} = 3.0V$, pin 9 connected to pin 3 (Bar Mode).

$-0.015V \leq V_{RHI} \leq 12\ V_{DC}$

For higher power dissipations, pulse testing is used.

Note 2: Accuracy is measured referred to $+10.000\ V_{DC}$ at pin 6, with $0.000\ V_{DC}$ at pin 4. At lower full-scale voltages, buffer and comparator offset voltage may add significant error.

Note 3: Pin 5 input current must be limited to ±3 mA. The addition of a 39k resistor in series with pin 5 allows ±100V signals without damage.

Note 4: Bar mode results when pin 9 is within 20 mV of V^+. Dot mode results when pin 9 is pulled at least 200 mV below V^+ or left open circuit. LED No. 10 (pin 10 output current) is disabled if pin 9 is pulled 0.9V or more below V_{LED}.

Note 5: The maximum junction temperature of the LM3914 is 100°C. Devices must be derated for operation at elevated temperatures. Junction to ambient thermal resistance is 75°C/W for the ceramic DIP (J package) and 120°C/W for the molded DIP (N package).

Definition of Terms

Accuracy: The difference between the observed threshold voltage and the ideal threshold voltage for each comparator. Specified and tested with 10V across the internal voltage divider so that resistor ratio matching error predominates over comparator offset voltage.

Adjust Pin Current: Current flowing out of the reference adjust pin when the reference amplifier is in the linear region.

Comparator Gain: The ratio of the change in output current (I_{LED}) to the change in input voltage (V_{IN}) required to produce it for a comparator in the linear region.

Dropout Voltage: The voltage measured at the current source outputs required to make the output current fall by 10%.

Input Bias Current: Current flowing out of the signal input when the input buffer is in the linear region.

LED Current Regulation: The change in output current over the specified range of LED supply voltage (V_{LED}) as measured at the current source outputs. As the forward voltage of an LED does not change significantly with a small change in forward current, this is equivalent to changing the voltage at the LED anodes by the same amount.

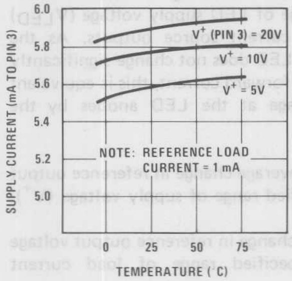
Line Regulation: The average change in reference output voltage over the specified range of supply voltage (V^+).

Load Regulation: The change in reference output voltage (V_{REF}) over the specified range of load current ($I_{L(REF)}$).

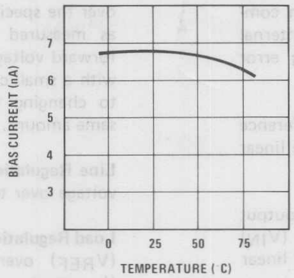
Offset Voltage: The differential input voltage which must be applied to each comparator to bias the output in the linear region. Most significant error when the voltage across the internal voltage divider is small. Specified and tested with pin 6 voltage (V_{RHI}) equal to pin 4 voltage (V_{RLO}).

Typical Performance Characteristics

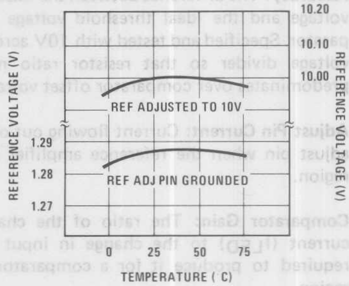
Supply Current vs Temperature



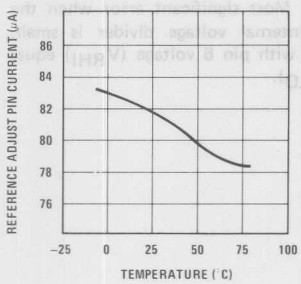
Operating Input Bias Current vs Temperature



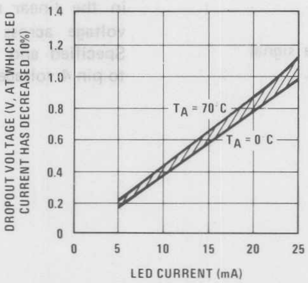
Reference Voltage vs Temperature



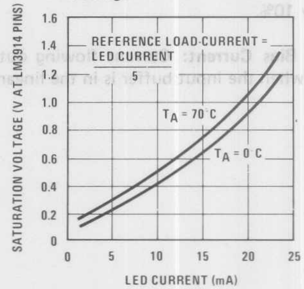
Reference Adjust Pin Current vs Temperature



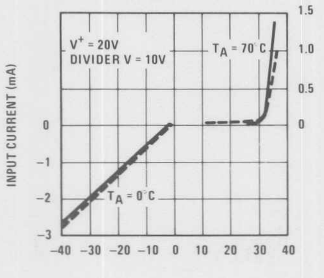
LED Current-Regulation Dropout



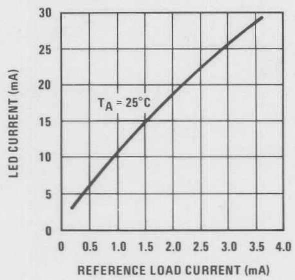
LED Driver Saturation Voltage



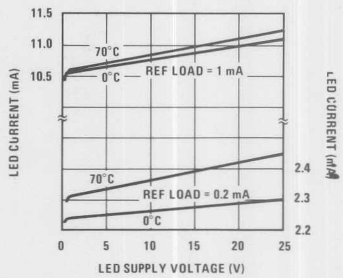
Input Current Beyond Signal Range (Pin 5)



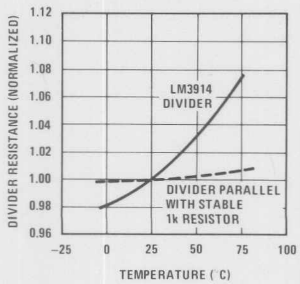
LED Current vs Reference Loading



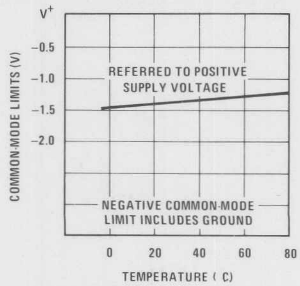
LED Driver Current Regulation



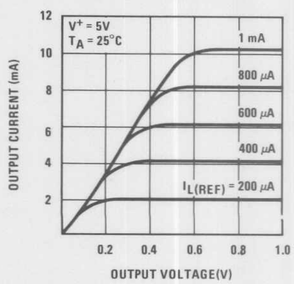
Total Divider Resistance vs Temperature



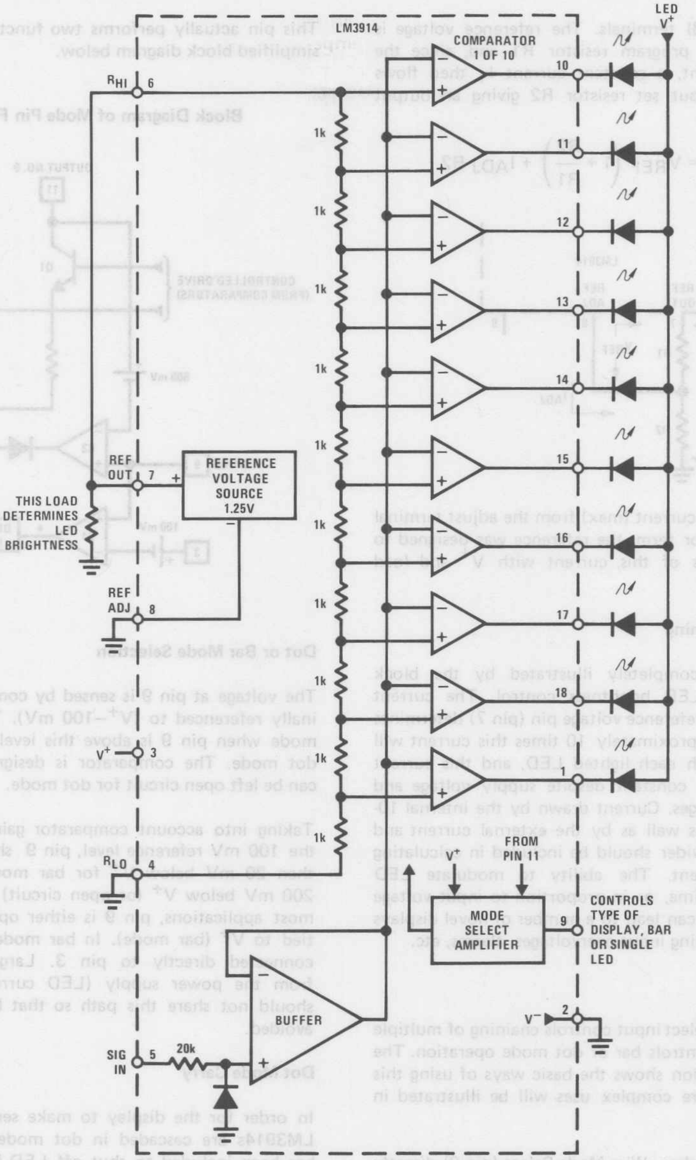
Common-Mode Limits



Output Characteristics



Block Diagram (Showing Simplest Application)



Functional Description

The simplified LM3914 block diagram is to give the general idea of the circuit's operation. A high input impedance buffer operates with signals from ground to 12V, and is protected against reverse and overvoltage signals. The signal is then applied to a series of 10 comparators; each of which is biased to a different comparison level by the resistor string.

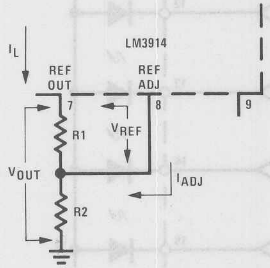
In the example illustrated, the resistor string is connected to the internal 1.25V reference voltage. In this case, for each 125 mV that the input signal increases, a comparator will switch on another indicating LED. This resistor divider can be connected between any 2 voltages, providing that they are 1.5V below V^+ and no less than V^-. If an expanded scale meter display is desired, the total divider voltage can be as little as 200 mV. Expanded-scale meter displays are more accurate and the segments light uniformly only if bar mode is used. At 50 mV or more per step, dot mode is usable.

Internal Voltage Reference

The reference is designed to be adjustable and develops a nominal 1.25V between the REF OUT (pin 7) and

through the output set resistor R2 giving an output voltage of:

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}\,R2$$



Since the 120 μA current (max) from the adjust terminal represents an error term, the reference was designed to minimize changes of this current with V^+ and load changes.

Current Programming

A feature not completely illustrated by the block diagram is the LED brightness control. The current drawn out of the reference voltage pin (pin 7) determines LED current. Approximately 10 times this current will be drawn through each lighted LED, and this current will be relatively constant despite supply voltage and temperature changes. Current drawn by the internal 10-resistor divider, as well as by the external current and voltage-setting divider should be included in calculating LED drive current. The ability to modulate LED brightness with time, or in proportion to input voltage and other signals can lead to a number of novel displays or ways of indicating input overvoltages, alarms, etc.

Mode Pin Use

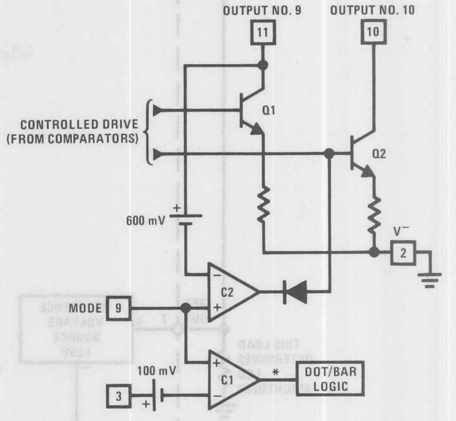
Pin 9, the Mode Select input controls chaining of multiple LM3914s, and controls bar or dot mode operation. The following tabulation shows the basic ways of using this input. Other more complex uses will be illustrated in the applications.

Bar Graph Display: Wire Mode Select (pin 9) *directly* to pin 3 (V^+ pin).

Dot Display, Single LM3914 Driver: Leave the Mode Select pin open circuit.

Dot Display, 20 or More LEDs: Connect pin 9 of the *first* driver in the series (i.e., the one with the lowest input voltage comparison points) to pin 1 of the next higher LM3914 driver. Continue connecting pin 9 of lower input drivers to pin 1 of higher input drivers for 30, 40, or more LED displays. The last LM3914 driver in the chain will have pin 9 wired to pin 11. All previous drivers should have a 20k resistor in parallel with LED No. 9 (pin 11 to V_{LED}).

Block Diagram of Mode Pin Function



*High for bar

Dot or Bar Mode Selection

The voltage at pin 9 is sensed by comparator C1, nominally referenced to (V^+−100 mV). The chip is in bar mode when pin 9 is above this level; otherwise it's in dot mode. The comparator is designed so that pin 9 can be left open circuit for dot mode.

Taking into account comparator gain and variation in the 100 mV reference level, pin 9 should be no more than 20 mV below V^+ for bar mode and more than 200 mV below V^+ (or open circuit) for dot mode. In most applications, pin 9 is either open (dot mode) or tied to V^+ (bar mode). In bar mode, pin 9 should be connected directly to pin 3. Large currents drawn from the power supply (LED current, for example) should not share this path so that large IR drops are avoided.

Dot Mode Carry

In order for the display to make sense when multiple LM3914s are cascaded in dot mode, special circuitry has been included to shut off LED No. 10 of the first device when LED No. 1 of the second device comes on. The connection for cascading in dot mode has already been described and is depicted on the following page.

As long as the input signal voltage is below the threshold of the second LM3914, LED No. 11 is off. Pin 9 of LM3914 No. 1 thus sees effectively an open circuit so the chip is in dot mode. As soon as the input voltage reaches the threshold of LED No. 11, pin 9 of LM3914 No. 1 is pulled an LED drop (1.5V or more) below V_{LED}. This condition is sensed by comparator C2, referenced 600 mV below V_{LED}. This forces the output of C2 low, which shuts off output transistor Q2, extinguishing LED No. 10.

Mode Pin Functional Description (Continued)

V_{LED} is sensed via the 20k resistor connected to pin 11. The very small current (less than 100 μA) that is diverted from LED No. 9 does not noticeably affect its intensity.

An auxiliary current source at pin 1 keeps at least 100 μA flowing through LED No. 11 even if the input voltage rises high enough to extinguish the LED. This ensures that pin 9 of LM3914 No. 1 is held low enough to force LED No. 10 off when *any* higher LED is illuminated. While 100 μA does not normally produce significant LED illumination, it may be noticeable when using high-efficiency LEDs in a dark environment. If this is bothersome, the simple cure is to shunt LED No. 11 with a 10k resistor. The 1V IR drop is more than the 900 mV worst case required to hold off LED No. 10 yet small enough that LED No. 11 does not conduct significantly.

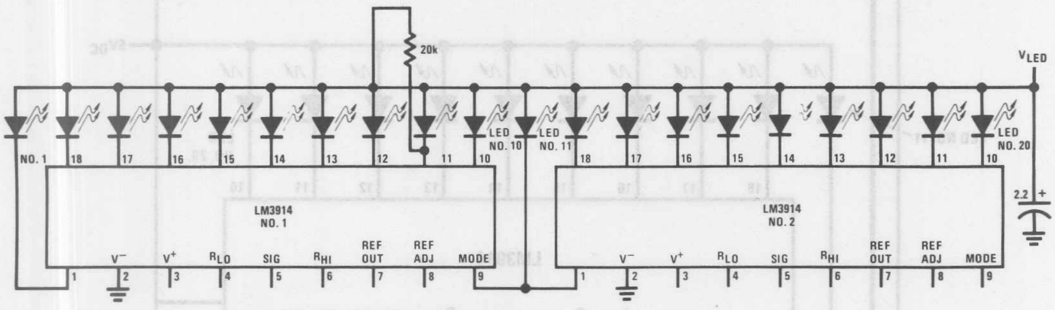
Other Device Characteristics

The LM3914 is relatively low-powered itself, and since any number of LEDs can be powered from about 3V, it is a very efficient display driver. Typical standby supply current (all LEDs OFF) is 1.6 mA (2.5 mA max). However, any reference loading adds 4 times that current drain to the V^+ (pin 3) supply input. For example, an LM3914 with a 1 mA reference pin load (1.3k), would supply almost 10 mA to every LED while drawing only 10 mA from its V^+ pin supply. At full-scale, the IC is typically drawing less than 10% of the current supplied to the display.

The display driver does not have built-in hysteresis so that the display does not jump instantly from one LED to the next. Under rapidly changing signal conditions, this cuts down high frequency noise and often an annoying flicker. An "overlap" is built in so that at no time between segments are all LEDs completely OFF in the dot mode. Generally 1 LED fades in while the other fades out over a mV or more of range (Note 2). The change may be much more rapid between LED No. 10 of one device and LED No. 1 of a *second* device "chained" to the first.

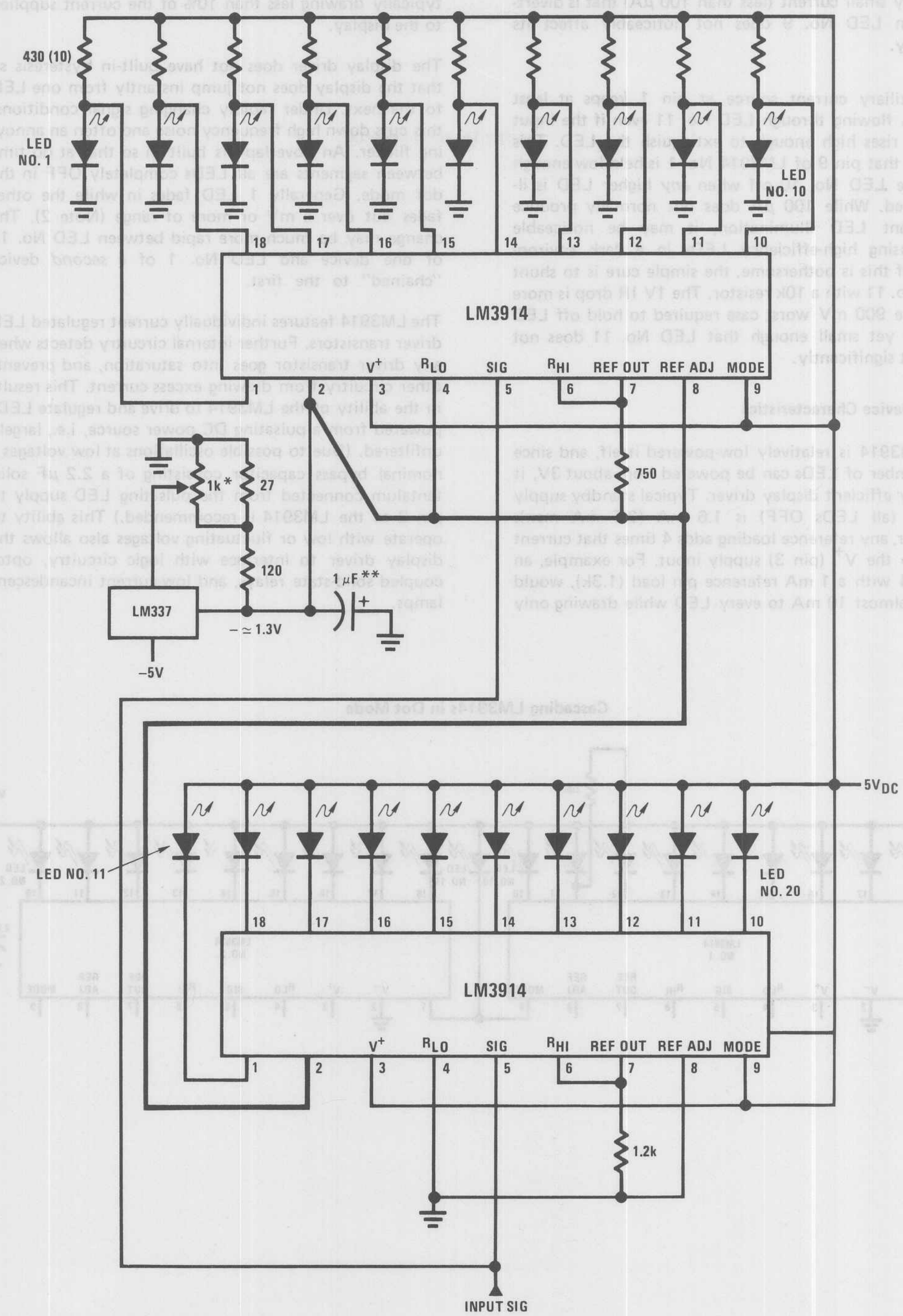
The LM3914 features individually current regulated LED driver transistors. Further internal circuitry detects when any driver transistor goes into saturation, and prevents other circuitry from drawing excess current. This results in the ability of the LM3914 to drive and regulate LEDs powered from a pulsating DC power source, i.e., largely unfiltered. (Due to possible oscillations at low voltages a nominal bypass capacitor consisting of a 2.2 μF solid tantalum connected from the pulsating LED supply to pin 2 of the LM3914 is recommended.) This ability to operate with low or fluctuating voltages also allows the display driver to interface with logic circuitry, opto-coupled solid-state relays, and low-current incandescent lamps.

Cascading LM3914s in Dot Mode



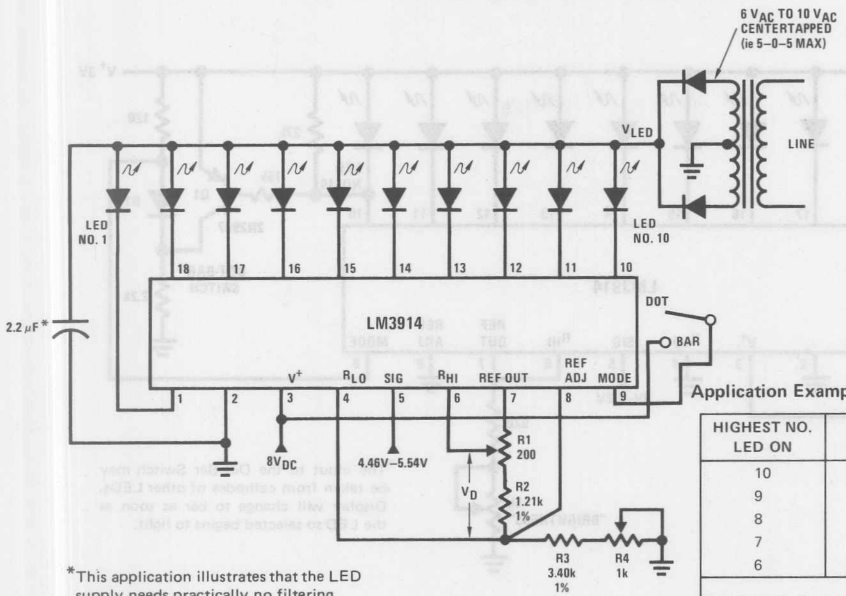
Typical Applications (Continued)

Zero-Center Meter, 20-Segment



Typical Applications (Continued)

Expanded Scale Meter, Dot or Bar



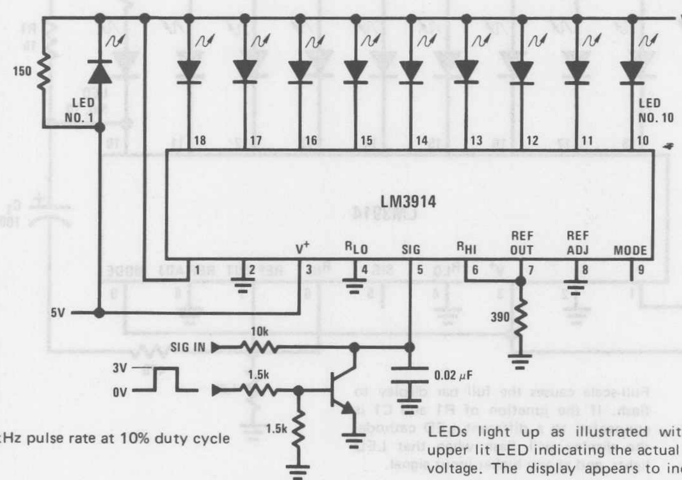
*This application illustrates that the LED supply needs practically no filtering

Calibration: With a precision meter between pins 4 and 6 adjust R1 for voltage V_D of 1.20V. Apply 4.94V to pin 5, and adjust R4 until LED No. 5 just lights. The adjustments are non-interacting.

Application Example: Grading 5V Regulators

HIGHEST NO. LED ON	COLOR	VOUT(MIN)
10	Red	5.54
9	Red	5.42
8	Yellow	5.30
7	Green	5.18
6	Green	5.06
	5V	
5	Green	4.94
4	Green	4.82
3	Yellow	4.7
2	Red	4.58
1	Red	4.46

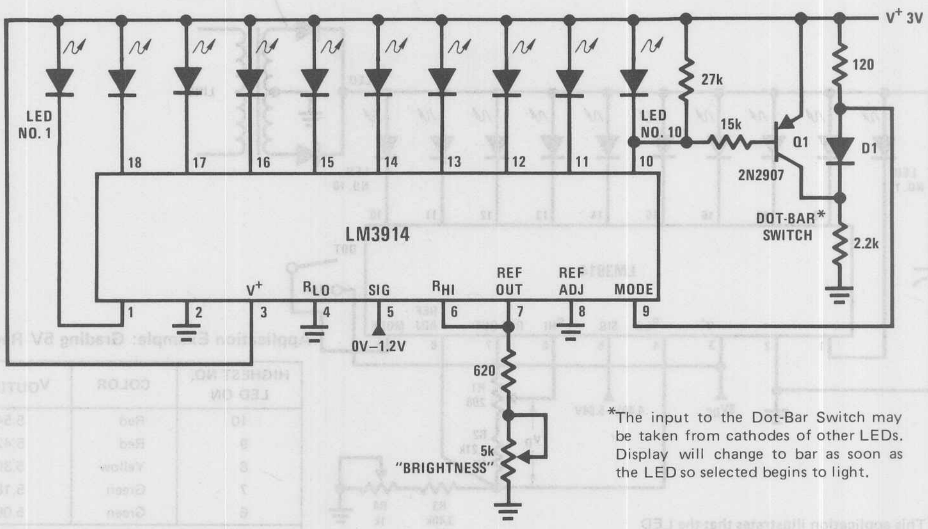
"Exclamation Point" Display



1 kHz pulse rate at 10% duty cycle

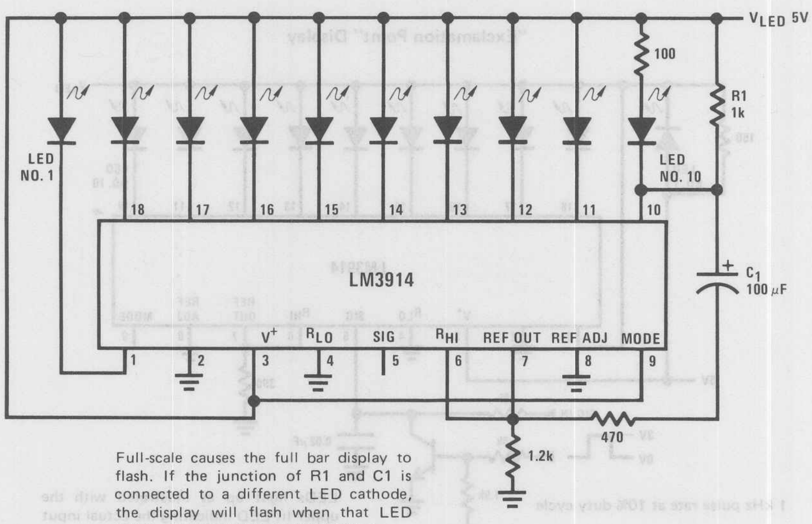
LEDs light up as illustrated with the upper lit LED indicating the actual input voltage. The display appears to increase resolution and provides an analog indication of overrange.

Indicator and Alarm, Full-Scale Changes Display From Dot to Bar



*The input to the Dot-Bar Switch may be taken from cathodes of other LEDs. Display will change to bar as soon as the LED so selected begins to light.

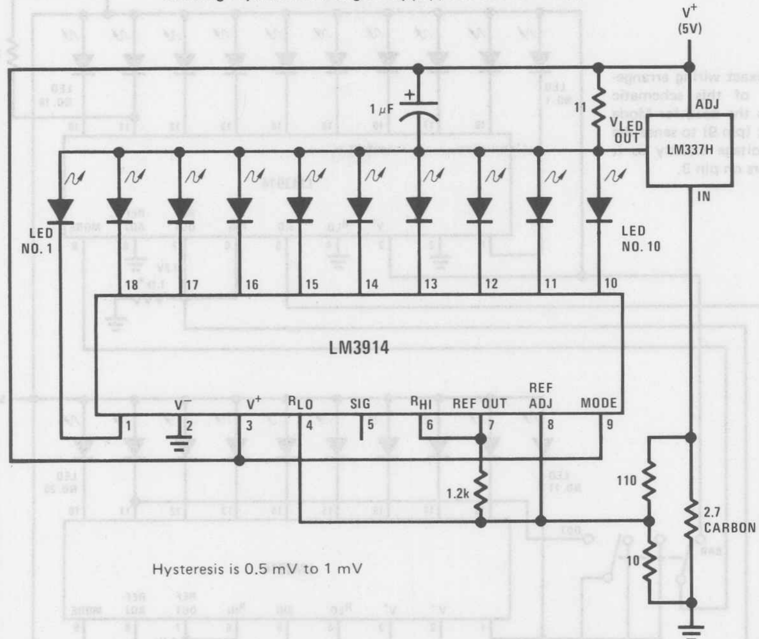
Bar Display with Alarm Flasher



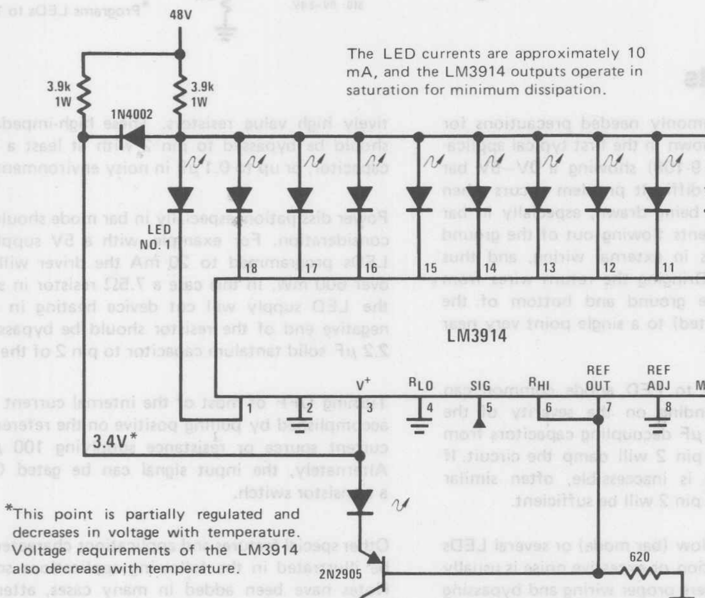
Full-scale causes the full bar display to flash. If the junction of R1 and C1 is connected to a different LED cathode, the display will flash when that LED lights, and at any higher input signal.

Typical Applications (Continued)

Adding Hysteresis (Single Supply, Bar Mode Only)



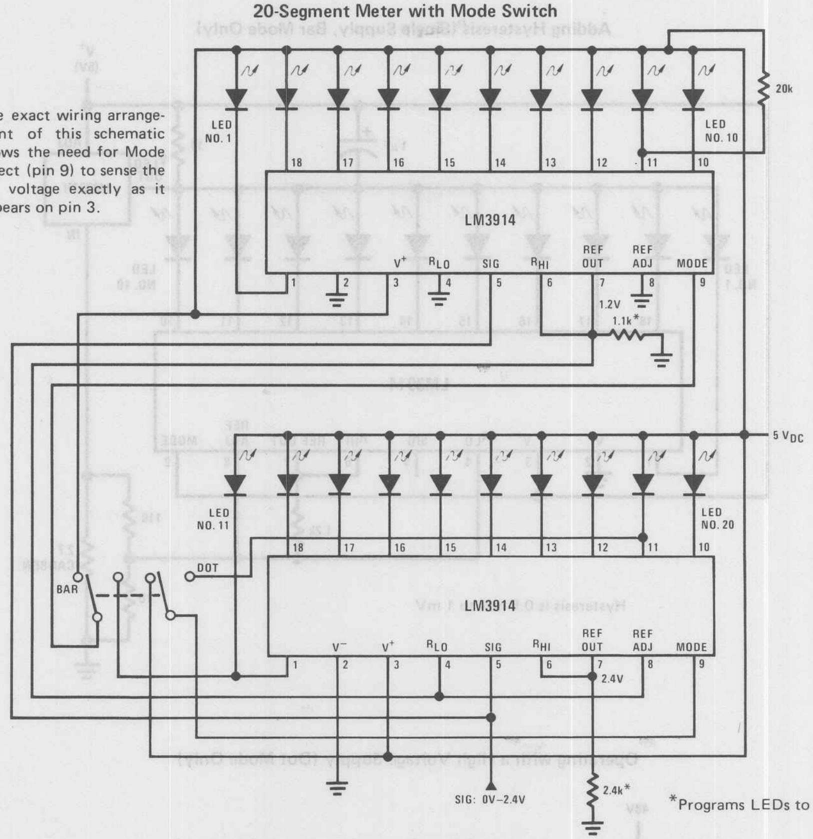
Operating with a High Voltage Supply (Dot Mode Only)



Typical Applications (Continued)

20-Segment Meter with Mode Switch

*The exact wiring arrangement of this schematic shows the need for Mode Select (pin 9) to sense the V^+ voltage exactly as it appears on pin 3.



*Programs LEDs to 10 mA

Application Hints

Three of the most commonly needed precautions for using the LM3914 are shown in the first typical application drawing (see page 9-108) showing a 0V–5V bar graph meter. The most difficult problem occurs when large LED currents are being drawn, especially in bar graph mode. These currents flowing out of the ground pin cause voltage drops in external wiring, and thus errors and oscillations. Bringing the return wires from signal sources, reference ground and bottom of the resistor string (as illustrated) to a single point very near pin 2 is the best solution.

Long wires from V_{LED} to LED anode common can cause oscillations. Depending on the severity of the problem 0.05 μF to 2.2 μF decoupling capacitors from LED anode common to pin 2 will damp the circuit. If LED anode line wiring is inaccessible, often similar decoupling from pin 1 to pin 2 will be sufficient.

If LED turn ON seems slow (bar mode) or several LEDs light (dot mode), oscillation or excessive noise is usually the problem. In cases where proper wiring and bypassing fail to stop oscillations, V^+ voltage at pin 3 is usually below suggested limits (see Note 2, page 9-108). Expanded scale meter applications may have one or both ends of the internal voltage divider terminated at relatively high value resistors. These high-impedance ends should be bypassed to pin 2 with at least a 0.001 μF capacitor, or up to 0.1 μF in noisy environments.

Power dissipation, especially in bar mode should be given consideration. For example, with a 5V supply and all LEDs programmed to 20 mA the driver will dissipate over 600 mW. In this case a 7.5Ω resistor in series with the LED supply will cut device heating in half. The negative end of the resistor should be bypassed with a 2.2 μF solid tantalum capacitor to pin 2 of the LM3914.

Turning OFF of most of the internal current sources is accomplished by pulling positive on the reference with a current source or resistance supplying 100 μA or so. Alternately, the input signal can be gated OFF with a transistor switch.

Other special features and applications characteristics will be illustrated in the following applications schematics. Notes have been added in many cases, attempting to cover any special procedures or unusual characteristics of these applications. A special section called "Application Tips for the LM3914 Adjustable Reference" has been included with these schematics.

Application Hints (Continued)

APPLICATION TIPS FOR THE LM3914s ADJUSTABLE REFERENCE

Greatly Expanded Scale (Bar Mode Only)

Placing the LM3914s internal resistor divider in parallel with a section (≃230Ω) of a stable, low resistance divider greatly reduces voltage changes due to IC resistor value changes with temperature. Voltage V_1 should be trimmed to 1.1V first by use of R2. Then the voltage V_2 across the IC divider string can be adjusted to 200 mV, using R5 without affecting V_1. LED current will be approximately 10 mA.

Non-Interacting Adjustments for Expanded Scale Meter (4.5V to 5V, Bar *or* Dot Mode)

This arrangement allows independent adjustment of LED brightness regardless of meter span and zero adjustments.

First, V_1 is adjusted to 5V, using R2. Then the span (voltage across R4) can be adjusted to exactly 0.5V using R6 without affecting the previous adjustment.

R9 programs LED currents within a range of 2.2 mA to 20 mA after the above settings are made.

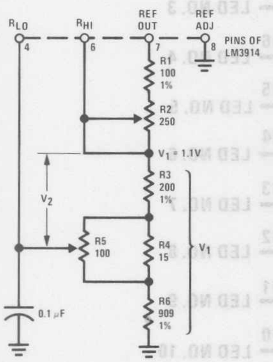
Adjusting Linearity of Several Stacked Dividers

Three internal voltage dividers are shown connected in series to provide a 30-step display. If the resulting analog meter is to be accurate and linear the voltage on each divider must be adjusted, preferably without affecting any other adjustments. To do this, adjust R2 first, so that the voltage across R5 is exactly 1V. Then the voltages across R3 and R4 can be independently adjusted by shunting each with selected resistors of 6 kΩ or higher resistance. This is possible because the reference of LM3914 No. 3 is acting as a constant current source.

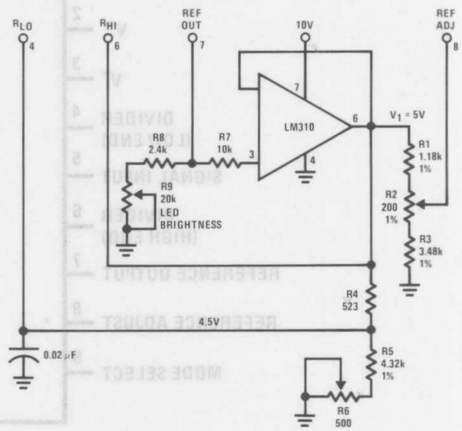
The references associated with LM3914s No. 1 and No. 2 should have their Ref Adj pins (pin 8) wired to ground, and their Ref Outputs loaded by a 620Ω resistor to ground. This makes available similar 20 mA current outputs to all the LEDs in the system.

If an independent LED brightness control is desired (as in the previous application), a unity gain buffer, such as the LM310, should be placed between pin 7 and R1, similar to the previous application.

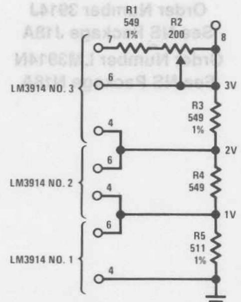
Greatly Expanded Scale (Bar Mode Only)



Non-Interacting Adjustments for Expanded Scale Meter (4.5V to 5V, Bar *or* Dot Mode)



Adjusting Linearity of Several Stacked Dividers

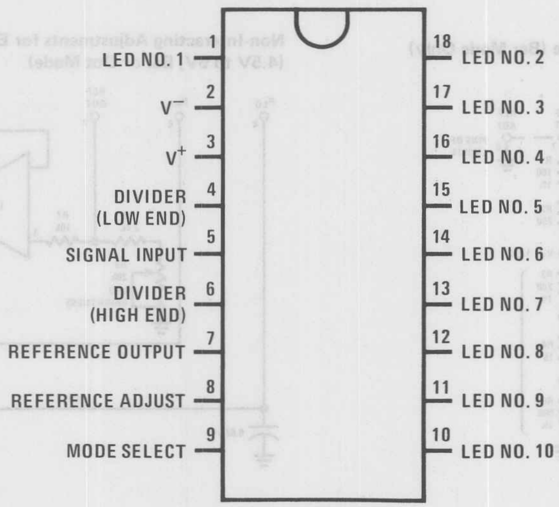


Other Applications

- "Slow" – fade bar or dot display (doubles resolution)
- 20-step meter with single pot brightness control
- 10-step (or multiples) programmer
- Multi-step or "staging" controller
- Combined controller and process deviation meter
- Direction and rate indicator (to add to DVMs)
- Exclamation point display for power saving
- Graduations can be added to dot displays. Dimly light every other LED using a resistor to ground
- Electronic "meter-relay"–display could be circle or semi-circle
- Moving "hole" display–indicator LED is dark, rest of bar lit
- Drives vacuum-fluorescent and LCDs using added passive parts

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number 3914J
See NS Package J18A
Order Number LM3914N
See NS Package N18A

National Semiconductor

LM3915 Dot/Bar Display Driver

General Description

The LM3915 is a monolithic integrated circuit that senses analog voltage levels and drives ten LEDs, LCDs or vacuum fluorescent displays, providing a logarithmic 3 dB/step analog display. One pin changes the display from a bar graph to a moving dot display. LED current drive is regulated and programmable, eliminating the need for current limiting resistors. The whole display system can operate from a single supply as low as 3V or as high as 25V.

The IC contains an adjustable voltage reference and an accurate ten-step voltage divider. The high-impedance input buffer accepts signals down to ground and up to within 1.5V of the positive supply. Further, it needs no protection against inputs of ±35V. The input buffer drives 10 individual comparators referenced to the precision divider. Accuracy is typically better than 1 dB.

The LM3915's 3 dB/step display is suited for signals with wide dynamic range, such as audio level, power, light intensity or vibration. Audio applications include average or peak level indicators, power meters and RF signal strength meters. Replacing conventional meters with an LED bar graph results in a faster responding, more rugged display with high visibility that retains the ease of interpretation of an analog display.

The LM3915 is extremely easy to apply. A 1.2V full-scale meter requires only one resistor in addition to the ten LEDs. One more resistor programs the full-scale anywhere from 1.2V to 12V independent of supply voltage. LED brightness is easily controlled with a single pot.

The LM3915 is very versatile. The outputs can drive LCDs, vacuum fluorescents and incandescent bulbs as well as LEDs of any color. Multiple devices can be cascaded for a dot or bar mode display with a range of 60 or 90 dB. LM3915s can also be cascaded with LM3914s for a linear/log display or with LM3916s for an extended-range VU meter.

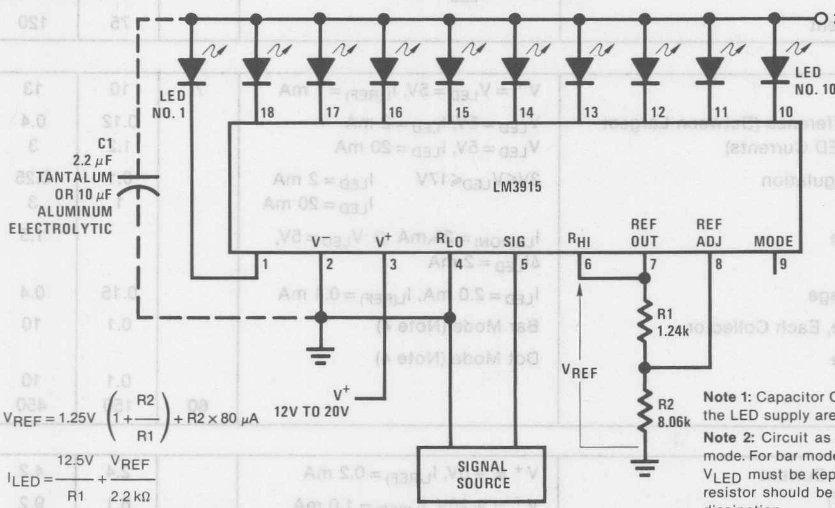
Features

- 3 dB/step, 30 dB range
- Drives LEDs, LCDs, or vacuum fluorescents
- Bar or dot display mode externally selectable by user
- Expandable to displays of 90 dB
- Internal voltage reference from 1.2V to 12V
- Operates with single supply of 3V to 25V
- Inputs operate down to ground
- Output current programmable from 1 mA to 30 mA
- Input withstands ±35V without damage or false outputs
- Outputs are current regulated, open collectors
- Directly drives TTL or CMOS
- The internal 10-step divider is floating and can be referenced to a wide range of voltages

The LM3915 is rated for operation from 0°C to +70°C. The LM3915N is available in an 18-lead molded DIP package and the LM3915J comes in the 18-lead ceramic DIP.

Typical Applications

0V to 10V Log Display



$$V_{REF} = 1.25V\left(1 + \frac{R2}{R1}\right) + R2 \times 80\,\mu A$$

$$I_{LED} = \frac{12.5V}{R1} + \frac{V_{REF}}{2.2\,k\Omega}$$

Note 1: Capacitor C1 is required if leads to the LED supply are 6" or longer.

Note 2: Circuit as shown is wired for dot mode. For bar mode, connect pin 9 to pin 3. V_{LED} must be kept below 7V or dropping resistor should be used to limit IC power dissipation.

Power Dissipation (Note 5)	
Ceramic DIP(J)	1W
Molded DIP(N)	625 mW
Supply Voltage	25V
Voltage on Output Drivers	25V
Input Signal Overvoltage (Note 3)	± 35V
Divider Voltage	− 100 mV to V^+
Reference Load Current	10 mA
Storage Temperature Range	− 55°C to + 150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 1)

Parameter	Conditions (Note 1)	Min	Typ	Max	Units
Comparators					
Offset Voltage, Buffer and First Comparator	$0V \leq V_{RLO} = V_{RHI} \leq 12V$, $I_{LED} = 1$ mA		3	10	mV
Offset Voltage, Buffer and Any Other Comparator	$0V \leq V_{RLO} = V_{RHI} \leq 12V$, $I_{LED} = 1$ mA		3	15	mV
Gain ($\Delta I_{LED}/\Delta V_{IN}$)	$I_{L(REF)} = 2$ mA, $I_{LED} = 10$ mA	3	8		mA/mV
Input Bias Current (at Pin 5)	$0V \leq V_{IN} \leq (V^+ - 1.5V)$		10	50	nA
Input Signal Overvoltage	No Change in Display	−35		35	V
Voltage-Divider					
Divider Resistance	Total, Pin 6 to 4	15	22	30	kΩ
Relative Accuracy (Input Change Between Any Two Threshold Points)	(Note 2)	2.0	3.0	4.0	dB
Absolute Accuracy at Each Threshold Point	(Note 2)				
	$V_{IN} = -3, -6$ dB	−0.5		+0.5	dB
	$V_{IN} = -9$ dB	−0.5		+0.65	dB
	$V_{IN} = -12, -15, -18$ dB	−0.5		+1.0	dB
	$V_{IN} = -21, -24, -27$ dB	−0.5		+1.5	dB
Voltage Reference					
Output Voltage	$0.1 \text{ mA} \leq I_{L(REF)} \leq 4$ mA, $V^+ = V_{LED} = 5V$	1.2	1.28	1.34	V
Line Regulation	$3V \leq V^+ \leq 18V$		0.01	0.03	%/V
Load Regulation	$0.1 \text{ mA} \leq I_{L(REF)} \leq 4$ mA, $V^+ = V_{LED} = 5V$		0.4	2	%
Output Voltage Change with Temperature	$0°C \leq T_A \leq +70°C$, $I_{L(REF)} = 1$ mA, $V^+ = V_{LED} = 5V$		1		%
Adjust Pin Current			75	120	μA
Output Drivers					
LED Current	$V^+ = V_{LED} = 5V$, $I_{L(REF)} = 1$ mA	7	10	13	mA
LED Current Difference (Between Largest and Smallest LED Currents)	$V_{LED} = 5V$, $I_{LED} = 2$ mA		0.12	0.4	mA
	$V_{LED} = 5V$, $I_{LED} = 20$ mA		1.2	3	mA
LED Current Regulation	$2V \leq V_{LED} \leq 17V$ $I_{LED} = 2$ mA		0.1	0.25	mA
	$I_{LED} = 20$ mA		1	3	mA
Dropout Voltage	$I_{LED(ON)} = 20$ mA @ $V_{LED} = 5V$, $\Delta I_{LED} = 2$ mA			1.5	V
Saturation Voltage	$I_{LED} = 2.0$ mA, $I_{L(REF)} = 0.4$ mA		0.15	0.4	V
Output Leakage, Each Collector	Bar Mode (Note 4)		0.1	10	μA
Output Leakage	Dot Mode (Note 4)				
Pins 10 − 18			0.1	10	μA
Pin 1		60	150	450	μA
Supply Current					
Standby Supply Current (All Outputs Off)	$V^+ = +5V$, $I_{L(REF)} = 0.2$ mA		2.4	4.2	mA
	$V^+ = +20V$, $I_{L(REF)} = 1.0$ mA		6.1	9.2	mA

Notes

Note 1: Unless otherwise stated, all specifications apply with the following conditions:

$3V_{DC} \leq V^+ \leq 20V_{DC}$ $\quad -0.015V \leq V_{RLO} \leq 12V_{DC}$ $\quad T_A = 25°C$, $I_{L(REF)} = 0.2$ mA, pin 9 connected to pin 3 (bar mode).

$3V_{DC} \leq V_{LED} \leq V^+$ $\quad V_{REF}, V_{RHI}, V_{RLO} \leq (V^+ - 1.5V)$ $\quad$ For higher power dissipations, pulse testing is used.

$-0.015V \leq V_{RHI} \leq 12V_{DC}$ $\quad 0V \leq V_{IN} \leq V^+ - 1.5V$

Note 2: Accuracy is measured referred to 0 dB = + 10.000V_{DC} at pin 5, with + 10.000V_{DC} at pin 6, and 0.000V_{DC} at pin 4. At lower full scale voltages, buffer and comparator offset voltage may add significant error. See table for threshold voltages.

Note 3: Pin 5 input current must be limited to ± 3 mA. The addition of a 39k resistor in series with pin 5 allows ± 100V signals without damage.

Note 4: Bar mode results when pin 9 is within 20 mV of V^+. Dot mode results when pin 9 is pulled at least 200 mV below V^+. LED #10 (pin 10 output current) is disabled if pin 9 is pulled 0.9V or more below V_{LED}.

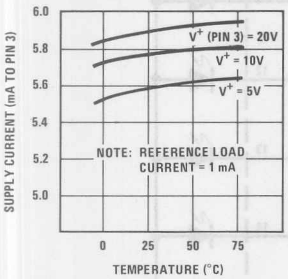
Note 5: The maximum junction temperature of the LM3915 is 100°C. Devices must be derated for operation at elevated temperatures. Junction to ambient thermal resistance is 75°C/W for the ceramic DIP (J package) and 120°C/W for the molded DIP (N package).

THRESHOLD VOLTAGE (Note 2)

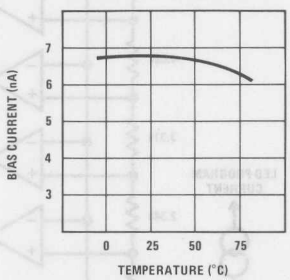
Output	dB	Min	Typ	Max	Output	dB	Min	Typ	Max
1	− 27	0.422	0.447	0.531	6	− 12	2.372	2.512	2.819
2	− 24	0.596	0.631	0.750	7	− 9	3.350	3.548	3.825
3	− 21	0.841	0.891	1.059	8	− 6	4.732	5.012	5.309
4	− 18	1.189	1.259	1.413	9	− 3	6.683	7.079	7.498
5	− 15	1.679	1.778	1.995	10	0	9.985	10	10.015

Typical Performance Characteristics

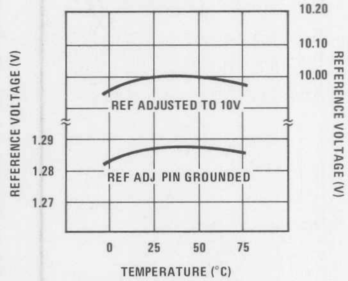
Supply Current vs Temperature



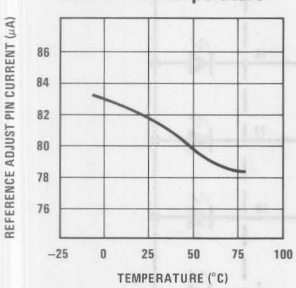
Operating Input Bias Current vs Temperature



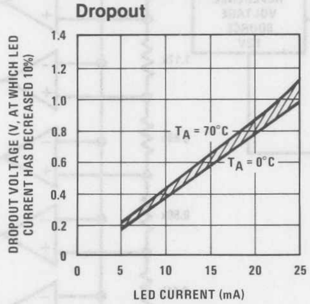
Reference Voltage vs Temperature



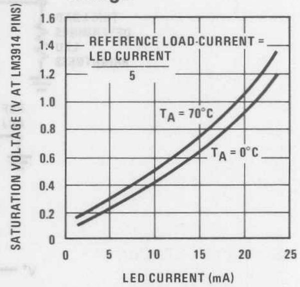
Reference Adjust Pin Current vs Temperature



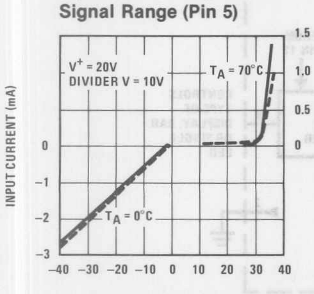
LED Current-Regulation Dropout



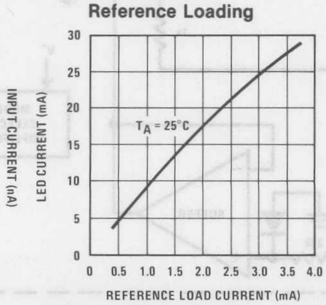
LED Driver Saturation Voltage



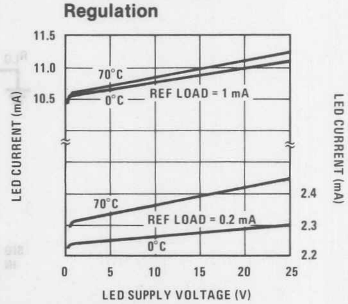
Input Current Beyond Signal Range (Pin 5)



LED Current vs Reference Loading

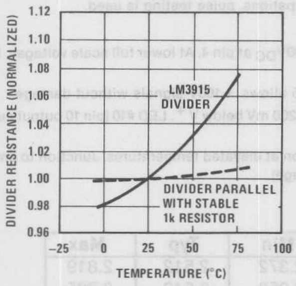


LED Driver Current Regulation

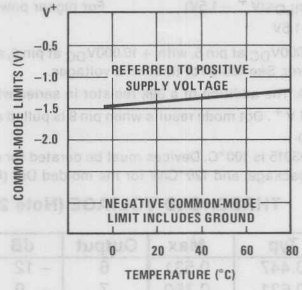


Typical Performance Characteristics (Continued)

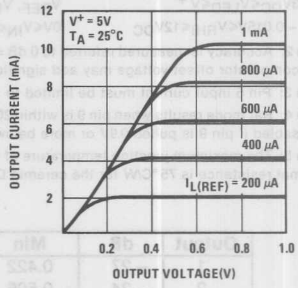
Total Divider Resistance vs Temperature



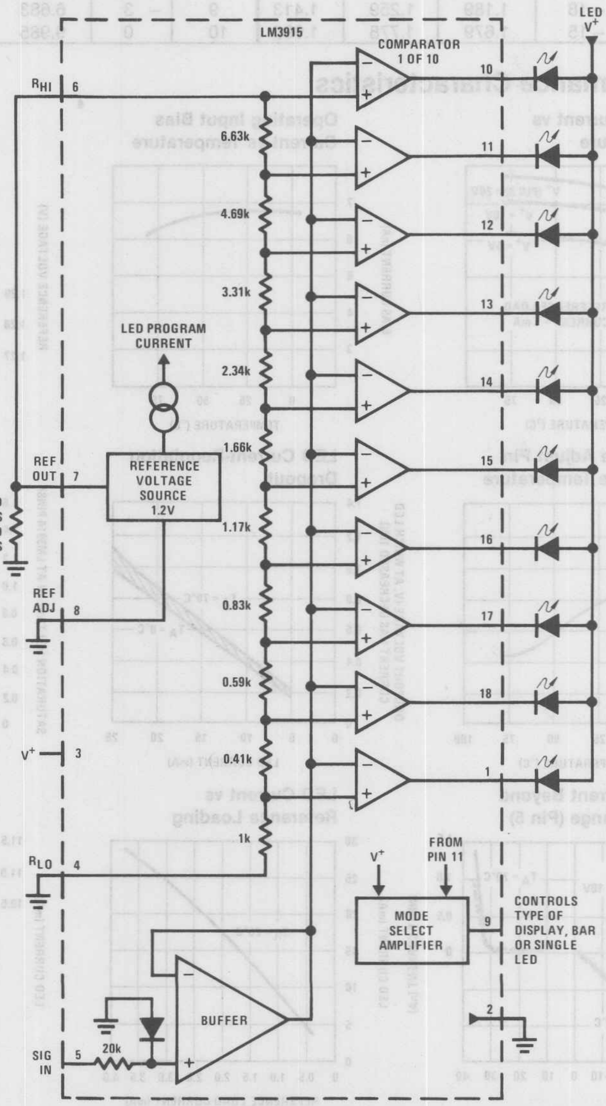
Common-Mode Limits



Output Characteristics



Block Diagram (Showing Simplest Application)



Functional Description

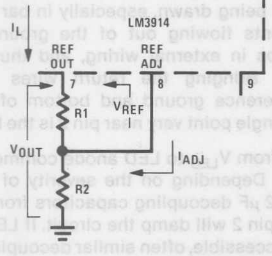
The simplified LM3915 block diagram is included to give the general idea of the circuit's operation. A high input impedance buffer operates with signals from ground to 12V, and is protected against reverse and overvoltage signals. The signal is then applied to a series of 10 comparators; each of which is biased to a different comparison level by the resistor string.

In the example illustrated, the resistor string is connected to the internal 1.25V reference voltage. In this case, for each 3 dB that the input signal increases, a comparator will switch on another indicating LED. This resistor divider can be connected between any 2 voltages, providing that they are at least 1.5V below V^+ and no lower than V^-.

Internal Voltage Reference

The reference is designed to be adjustable and develops a nominal 1.25V between the REF OUT (pin 7) and REF ADJ (pin 8) terminals. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R2 giving an output voltage of:

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}\,R2$$



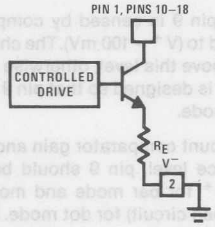
Since the 120 μA current (max) from the adjust terminal represents an error term, the reference was designed to minimize changes of this current with V^+ and load changes. For correct operation, reference load current should be between 80 μA and 5 mA. Load capacitance should be less than 0.05 μF.

Current Programming

A feature not completely illustrated by the block diagram is the LED brightness control. The current drawn out of the reference voltage pin (pin 7) determines LED current. Approximately 10 times this current will be drawn through each lighted LED, and this current will be relatively constant despite supply voltage and temperature changes. Current drawn by the internal 10-resistor divider, as well as by the external current and voltage-setting divider should be included in calculating LED drive current. The ability to modulate LED brightness with time, or in proportion to input voltage and other signals can lead to a number of novel displays or ways of indicating input overvoltages, alarms, etc.

The LM3915 outputs are current-limited NPN transistors as shown below. An internal feedback loop regulates the transistor drive. Output current is held at about 10 times the reference load current, independent of output voltage and processing variables, as long as the transistor is not saturated.

LM3915 Output Circuit



Outputs may be run in saturation with no adverse effects, making it possible to directly drive logic. The effective saturation resistance of the output transistors, equal to R_E plus the transistors' collector resistance, is about 50Ω. It's also possible to drive LEDs from rectified AC with no filtering. To avoid oscillations, the LED supply should be bypassed with a 2.2 μF tantalum or 10 μF aluminum electrolytic capacitor.

Mode Pin Use

Pin 9, the Mode Select input, permits chaining of multiple LM3915s, and controls bar or dot mode operation. The following tabulation shows the basic ways of using this input. Other more complex uses will be illustrated in the applications.

Bar Graph Display: Wire Mode Select (pin 9) *directly* to pin 3 (V^+ pin).

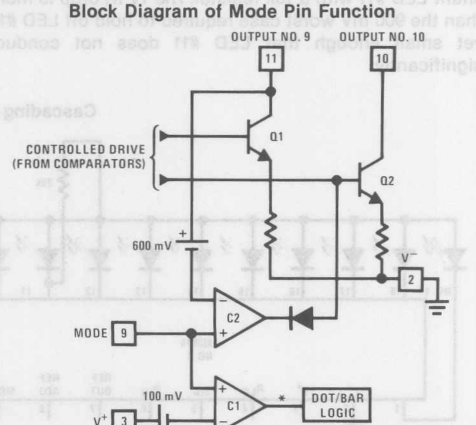
Dot Display, Single LM3915 Driver: Leave the Mode Select pin open circuit.

Dot Display, 20 or More LEDs: Connect pin 9 of the *first* driver in the series (i.e., the one with the lowest input voltage comparison points) to pin 1 of the next higher LM3915 driver. Continue connecting pin 9 of lower input drivers to pin 1 of higher input drivers for 30 or more LED displays. The last LM3915 driver in the chain will have pin 9 left open. All previous drivers should have a 20k resistor in parallel with LED #9 (pin 11 to V_{LED}).

Mode Pin Functional Description

This pin actually performs two functions. Refer to the simplified block diagram below.

Block Diagram of Mode Pin Function



* High for bar

nally referenced to (V^+ − 100 mV). The chip is in bar mode when pin 9 is above this level; otherwise it's in dot mode. The comparator is designed so that pin 9 can be left open circuit for dot mode.

Taking into account comparator gain and variation in the 100 mV reference level, pin 9 should be no more than 20 mV below V^+ for bar mode and more than 200 mV below V^+ (or open circuit) for dot mode. In most applications, pin 9 is either open (dot mode) or tied to V^+ (bar mode). In bar mode, pin 9 should be connected directly to pin 3. Large currents drawn from the power supply (LED current, for example) should not share this path so that large IR drops are avoided.

Dot Mode Carry

In order for the display to make sense when multiple LM3915s are cascaded in dot mode, special circuitry has been included to shut off LED #10 of the first device when LED #1 of the second device comes on. The connection for cascading in dot mode has already been described and is depicted below.

As long as the input signal voltage is below the threshold of the second LM3915, LED #11 is off. Pin 9 of LM3915 #1 thus sees effectively an open circuit so the chip is in dot mode. As soon as the input voltage reaches the threshold of LED #11, pin 9 of LM3915 #1 is pulled an LED drop (1.5V or more) below V_{LED}. This condition is sensed by comparator C2, referenced 600 mV below V_{LED}. This forces the output of C2 low, which shuts off output transistor Q2, extinguishing LED #10.

V_{LED} is sensed via the 20k resistor connected to pin 11. The very small current (less than 100 μA) that is diverted from LED #9 does not noticeably affect its intensity.

An auxiliary current source at pin 1 keeps at least 100 μA flowing through LED #11 even if the input voltage rises high enough to extinguish the LED. This ensures that pin 9 of LM3915 #1 is held low enough to force LED #10 off when *any* higher LED is illuminated. While 100 μA does not normally produce significant LED illumination, it may be noticeable when using high-efficiency LEDs in a dark environment. If this is bothersome, the simple cure is to shunt LED #11 with a 10k resistor. The 1V IR drop is more than the 900 mV worst case required to hold off LED #10 yet small enough that LED #11 does not conduct significantly.

number of LEDs can be powered from about 3V, it is a very efficient display driver. Typical standby supply current (all LEDs OFF) is 1.6 mA. However, any reference loading adds 4 times that current drain to the V^+ (pin 3) supply input. For example, an LM3916 with a 1 mA reference pin load (1.3k) would supply almost 10 mA to every LED while drawing only 10 mA from its V^+ pin supply. At full-scale, the IC is typically drawing less than 10% of the current supplied to the display.

The display driver does not have built-in hysteresis so that the display does not jump instantly from one LED to the next. Under rapidly changing signal conditions, this cuts down high frequency noise and often an annoying flicker. An "overlap" is built in so that at no time are all segments completely off in the dot mode. Generally 1 LED fades in while the other fades out over a mV or more of range. The change may be much more rapid between LED #10 of one device and LED #1 of a *second* device "chained" to the first.

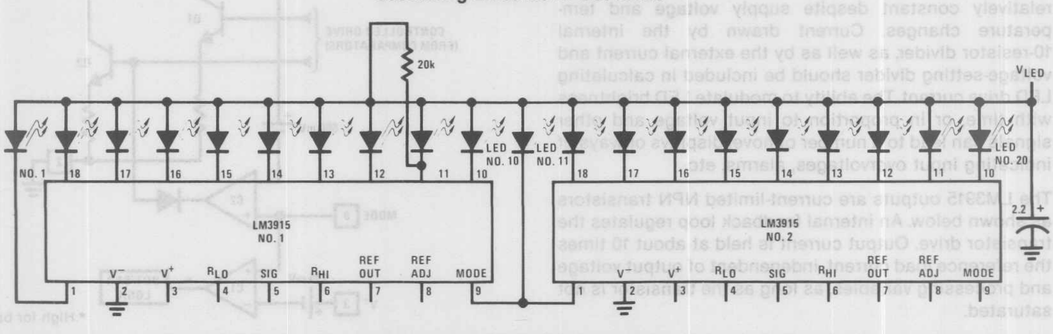
Application Hints

The most difficult problem occurs when large LED currents are being drawn, especially in bar graph mode. These currents flowing out of the ground pin cause voltage drops in external wiring, and thus errors and oscillations. Bringing the return wires from signal sources, reference ground and bottom of the resistor string to a single point very near pin 2 is the best solution.

Long wires from V_{LED} to LED anode common can cause oscillations. Depending on the severity of the problem 0.05 μF to 2.2 μF decoupling capacitors from LED anode common to pin 2 will damp the circuit. If LED anode line wiring is inaccessible, often similar decoupling from pin 1 to pin 2 will be sufficient.

If LED turn ON seems slow (bar mode) or several LEDs light (dot mode), oscillation or excessive noise is usually the problem. In cases where proper wiring and bypassing fail to stop oscillations, V^+ voltage at pin 3 is usually below suggested limits. Expanded scale meter applications may have one or both ends of the internal voltage divider terminated at relatively high value resistors. These high-impedance ends should be bypassed to pin 2 with at lease a 0.001 μF capacitor, or up to 0.1 μF in noisy environments.

Cascading LM3915s in Dot Mode



Application Hints (Continued)

Power dissipation, especially in bar mode should be given consideration. For example, with a 5V supply and all LEDs programmed to 20 mA the driver will dissipate over 600 mW. In this case a 7.5Ω resistor in series with the LED supply will cut device heating in half. The negative end of the resistor should be bypassed with a 2.2 μF solid tantalum capacitor to pin 2.

Tips on Rectifier Circuits

The simplest way to display an AC signal using the LM3915 is to apply it right to pin 5 unrectified. Since the LED illuminated represents the instantaneous value of the AC waveform, one can readily discern both peak and average values of audio signals in this manner. The LM3915 will respond to positive half-cycles only but will not be damaged by signals up to ±35V (or up to ±100V if a 39k resistor is in series with the input). It's recommended to use dot mode and to run the LEDs at 30 mA for high enough average intensity.

True average or peak detection requires rectification. If an LM3915 is set up with 10V full scale across its voltage divider, the turn-on point for the first LED is only 450 mV. A simple silicon diode rectifier won't work well at the low end due to the 600 mV diode threshold. The half-wave peak detector in *Figure 1* uses a PNP emitter-follower in front of the diode. Now, the transistor's base-emitter voltage cancels out the diode offset, within about 100 mV. This approach is usually satisfactory when a single LM3915 is used for a 30 dB display.

Display circuits using two or more LM3915s for a dynamic range of 60 dB or greater require more accurate detection. In the precision half-wave rectifier of *Figure 2* the effective diode offset is reduced by a factor equal to the open-loop gain of the op amp. Filter capacitor C2 charges through R3 and discharges through R2 and R3, so that appropriate selection of these values results in either a peak or an average detector. The circuit has a gain equal to R2/R1.

It's best to capacitively couple the input. Audio sources frequently have a small DC offset that can cause significant error at the low end of the log display. Op amps that slew quickly, such as the LF351, LF353 or LF356, are needed to faithfully respond to sudden transients. It may be necessary to trim out the op amp DC offset voltage to accurately cover a 60 dB range. Best results are obtained if the circuit is adjusted for the correct output when a low-level AC signal (10 to 20 mV) is applied, rather than adjusting for zero output with zero input.

For precision full-wave averaging use the circuit in *Figure 3*. Using 1% resistors for R1 through R4, gain for positive and negative signal differs by only 0.5 dB worst case. Substituting 5% resistors increases this to 2 dB worst case. (A 2 dB gain difference means that the display may have a ±1 dB error when the input is a nonsymmetrical transient). The averaging time constant is R5·C2. A simple modification results in the precision full-wave detector of *Figure 4*. Since the filter capacitor is not buffered, this circuit can drive only high impedance loads such as the input of an LM3915.

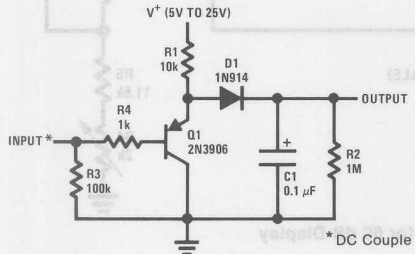
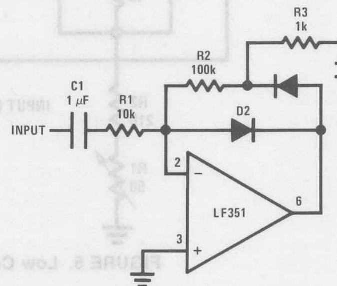


FIGURE 1. Half-Wave Peak Detector



D1, D2: 1N914 or 1N4148

	Average	Peak
R2	1k	100k
R3	100k	1k

$R1 = R2$ for $A_V = 1$

$R1 = R2/10$ for $A_V = 10$

$C1 = 10/R1$

FIGURE 2. Precision Half-Wave Rectifier

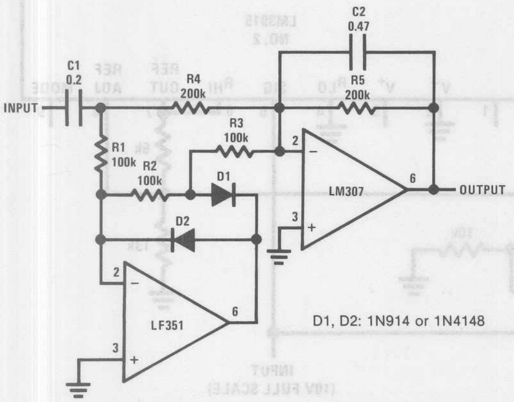


FIGURE 3. Precision Full-Wave Average Detector

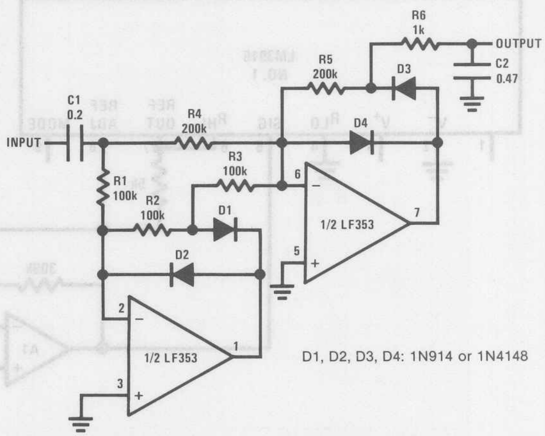


FIGURE 4. Precision Full-Wave Peak Detector

Application Hints (Continued)

Cascading the LM3915

To display signals of 60 or 90 dB dynamic range, multiple LM3915s can be easily cascaded. Alternatively, it is possible to cascade an LM3915 with LM3914s for a log/linear display or with an LM3916 to get an extended range VU meter.

A simple, low cost approach to cascading two LM3915s is to set the reference voltages of the two chips 30 dB apart as in *Figure 5*. Potentiometer R1 is used to adjust the full scale voltage of LM3915 #1 to 316 mV nominally while the second IC's reference is set at 10V by R4. The drawback of this method is that the threshold of LED #1 is only 14 mV and, since the LM3915 can have an offset voltage as high as 10 mV, large errors can occur. This technique is not recommended for 60 dB displays requiring good accuracy at the first few display thresholds.

A better approach shown in *Figure 6* is to keep the reference at 10V for both LM3915s and amplify the input signal to the lower LM3915 by 30 dB. Since two 1% resistors can set the amplifier gain within ±0.2 dB, a gain trim is unnecessary. However, an op amp offset voltage of 5 mV will shift the first LED threshold as much as 4 dB, so that an offset trim may be required. Note that a single adjustment can null out offset in both the precision rectifier and the 30 dB gain stage. Alternatively, instead of amplifying, input signals of sufficient amplitude can be fed directly to the lower LM3915 and *attenuated* by 30 dB to drive the second LM3915.

To extend this approach to get a 90 dB display, another 30 dB of amplification must be placed in the signal path ahead of the lowest LM3915. Extreme care is required as the lowest LM3915 displays input signals down to 0.5 mV! Several offset nulls may be required. High currents should not share the same path as the low level signal. Also power line wiring should be kept away from signal lines.

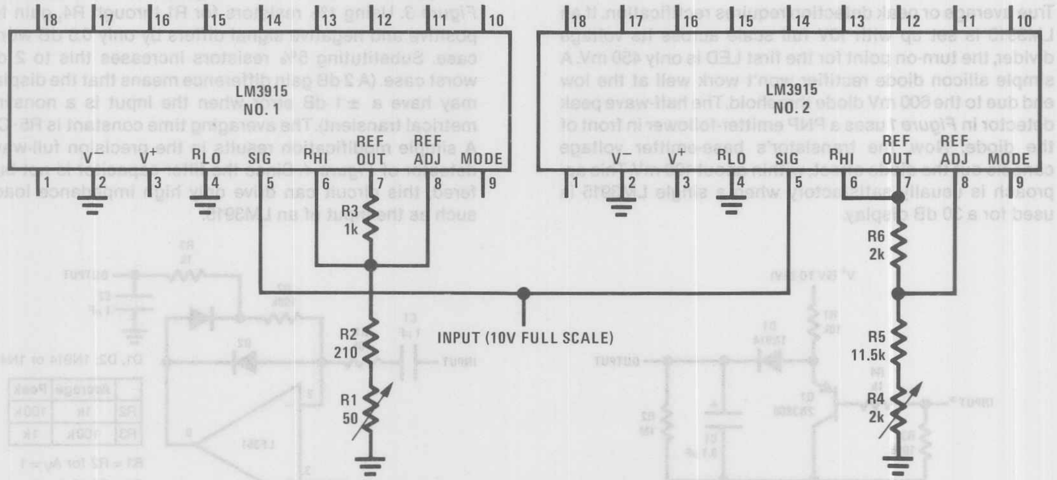


FIGURE 5. Low Cost Circuit for 60 dB Display

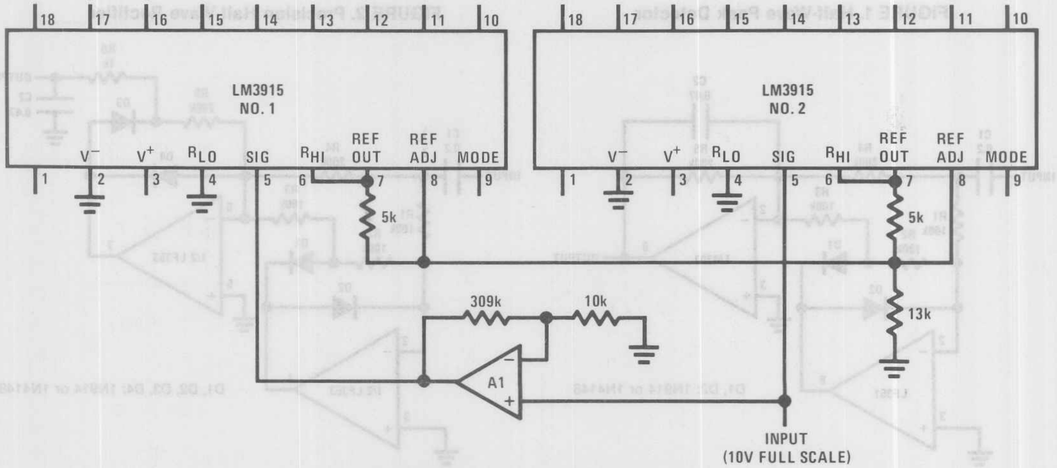


FIGURE 6. Improved Circuit for 60 dB Display

Application Hints (Continued)

TIPS ON REFERENCE VOLTAGE AND LED CURRENT PROGRAMMING

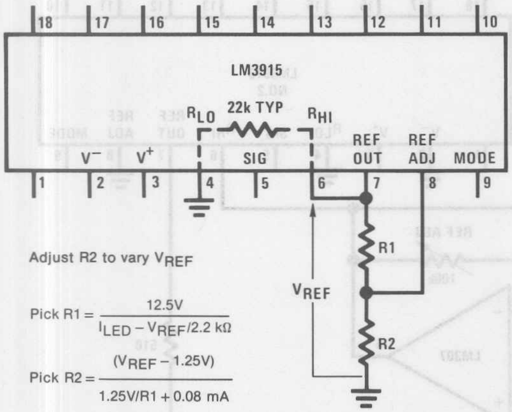
Single LM3915

The equations in *Figure 7* illustrate how to choose resistor values to set reference voltage for the simple case where no LED intensity adjustment is required. A LED current of 10 mA to 20 mA generally produces adequate illumination. Having 10V full-scale across the internal voltage divider gives best accuracy by keeping signal level high relative to the offset voltage of the internal comparators. However, this causes 450 μA to flow from pin 7 into the divider which means that the LED current will be at least 5 mA. R1 will typically be between 1 kΩ and 2 kΩ. To trim the reference voltage, vary R2.

The circuit in *Figure 8* shows how to add a LED intensity control which can vary LED current from 9 mA to 28 mA. The reference adjustment has some effect on LED intensity but the reverse is not true.

Multiple LM3915s

Figure 9 shows how to obtain a common reference trim and intensity control for two LM3915s. The two ICs may be connected in cascade for a 60 dB display or may be handling separate channels for stereo. This technique can be extended for larger numbers of LM3915s by varying the values of R1, R2 and R3 in inverse proportion to the number of devices tied in. The ICs' internal references track within 100 mV so that worst case error from chip to chip is only 0.1 dB for $V_{REF} = 10V$.

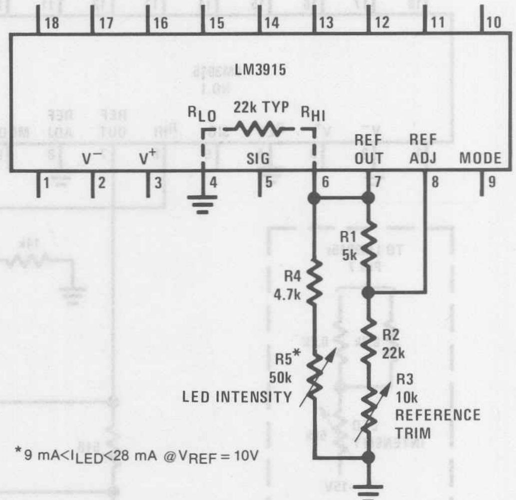


Adjust R2 to vary V_{REF}

$$\text{Pick R1} = \frac{12.5V}{I_{LED} - V_{REF}/2.2\ k\Omega}$$

$$\text{Pick R2} = \frac{(V_{REF} - 1.25V)}{1.25V/R1 + 0.08\ mA}$$

FIGURE 7. Design Equations for Fixed LED Intensity



*9 mA<I_{LED}<28 mA @V_{REF} = 10V

FIGURE 8. Varying LED Intensity

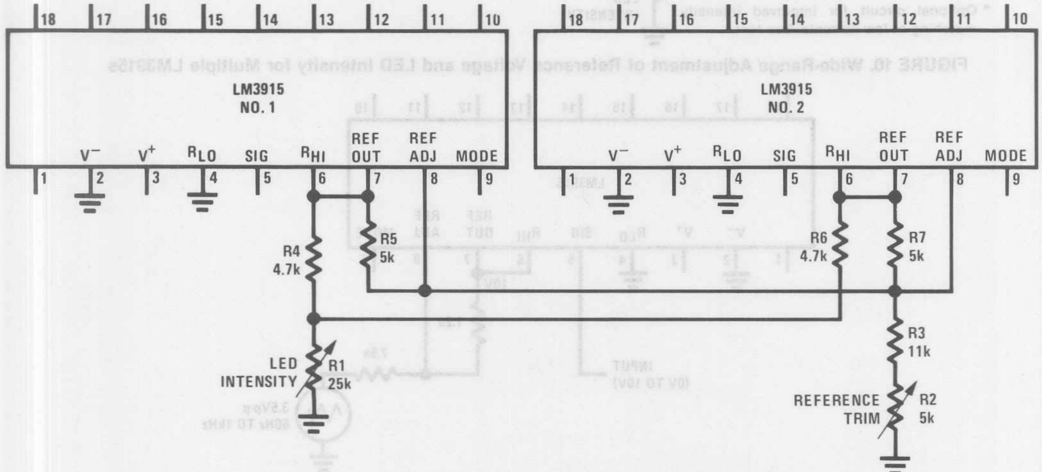


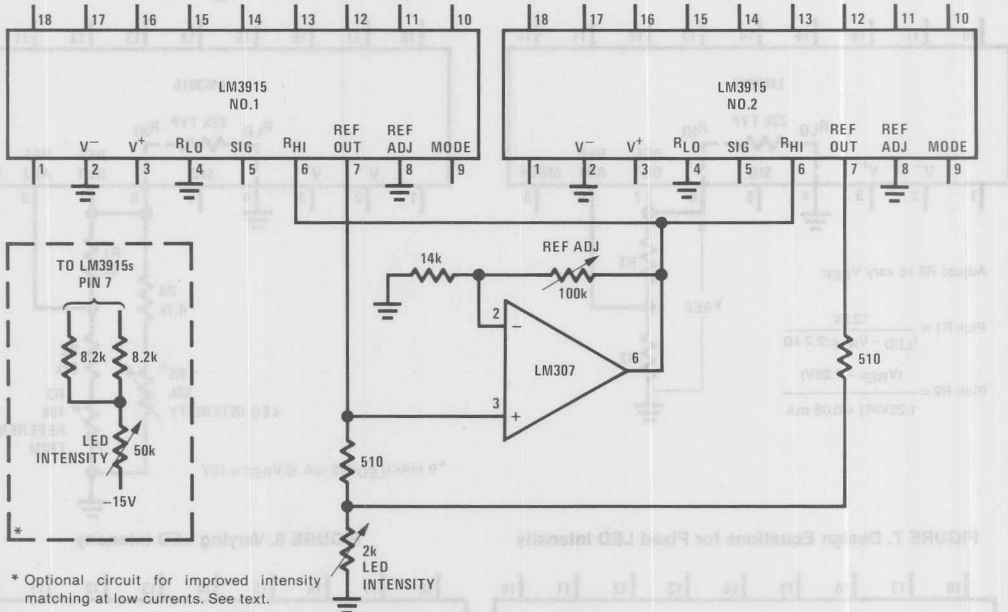
FIGURE 9. Independent Adjustment of Reference Voltage and LED Intensity for Multiple LM3915s

range. The R_{HI} voltage can be adjusted from 1.2V to 10V with no effect on LED current. Since the internal divider here does not load down the reference, minimum LED current is much lower. At the minimum recommended reference load of 80 μA, LED current is about 0.8 mA. The resistor values shown give a LED current range from 1.5 mA to 20 mA.

At the low end of the intensity adjustment, the voltage drop across the 510Ω current-sharing resistors is so small that chip to chip variation in reference voltage may yield a visible variation in LED intensity. The optional approach shown of connecting the bottom end of the intensity control pot to a negative supply overcomes this problem by allowing a larger voltage drop across the (larger) current-sharing resistors.

complished by varying the reference level at pin 6 by 3 dBp-p as shown in *Figure 11.* The signal can be a triangle, sawtooth or sine wave from 60 Hz to 1 kHz. The display can be run in either dot or bar mode.

When an exponentially decaying RC discharge waveform is applied to pin 5, the LM3915's outputs will switch at equal intervals. This makes a simple timer or sequencer. Each time interval is equal to RC/3. The output may be used to drive logic, opto-couplers, relays or PNP transistors, for example.



* Optional circuit for improved intensity matching at low currents. See text.

FIGURE 10. Wide-Range Adjustment of Reference Voltage and LED Intensity for Multiple LM3915s

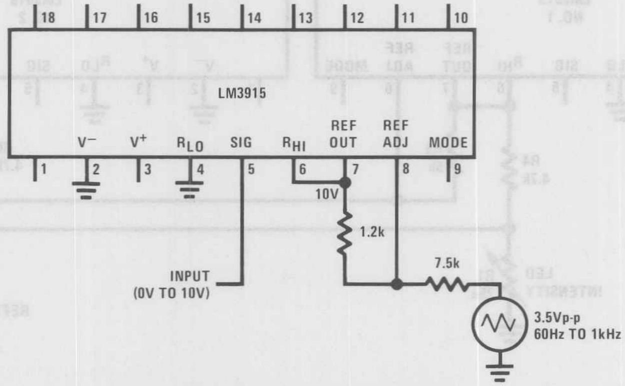
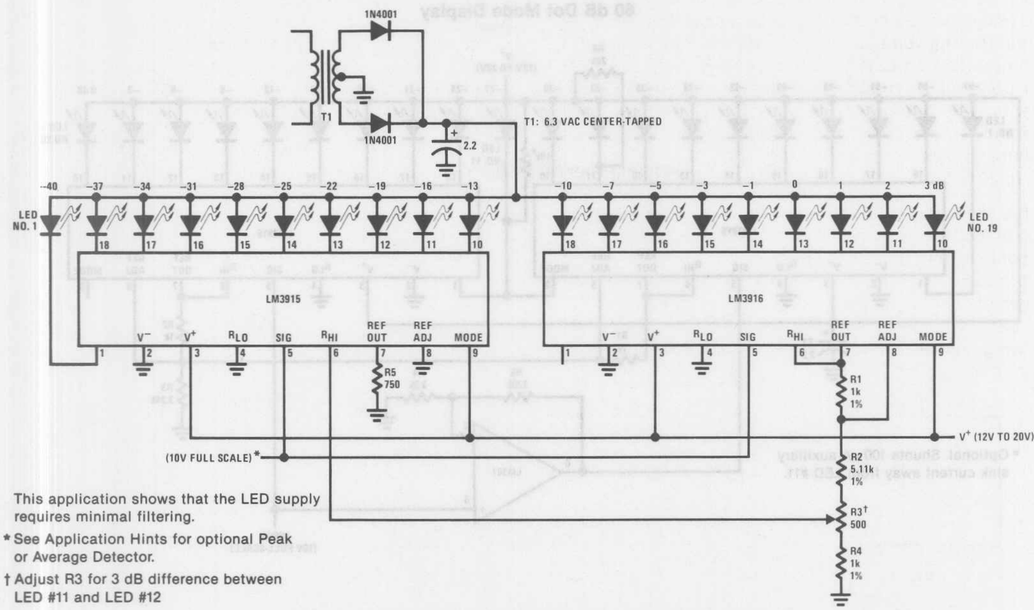


FIGURE 11. 0V to 10V Log Display with Smooth Transitions

Typical Applications (Continued)

Extended Range VU Meter

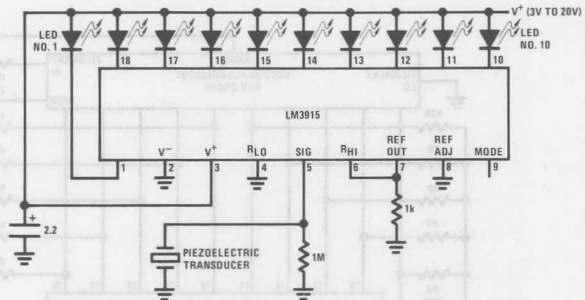


This application shows that the LED supply requires minimal filtering.

*See Application Hints for optional Peak or Average Detector.

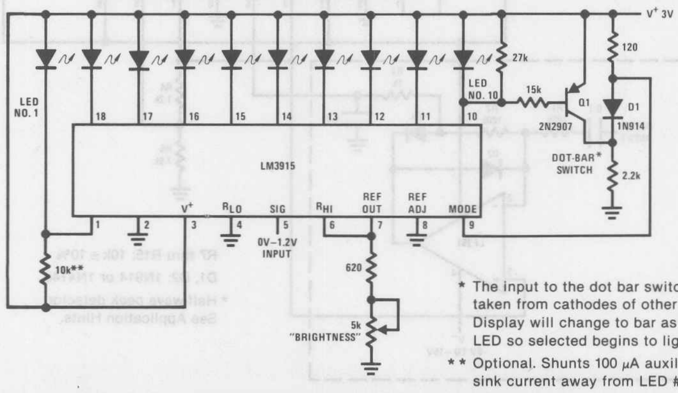
† Adjust R3 for 3 dB difference between LED #11 and LED #12

Vibration Meter



LED	Threshold
1	60 mV
2	80 mV
3	110 mV
4	160 mV
5	220 mV
6	320 mV
7	440 mV
8	630 mV
9	890 mV
10	1.25 V

Indicator and Alarm, Full-Scale Changes Display From Dot to Bar

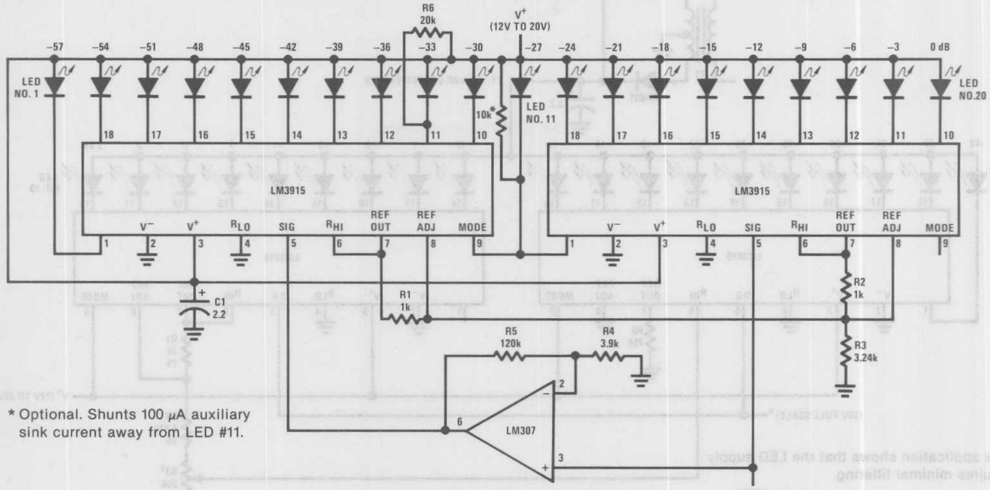


* The input to the dot bar switch may be taken from cathodes of other LEDs. Display will change to bar as soon as the LED so selected begins to light.

** Optional. Shunts 100 μA auxiliary sink current away from LED #1.

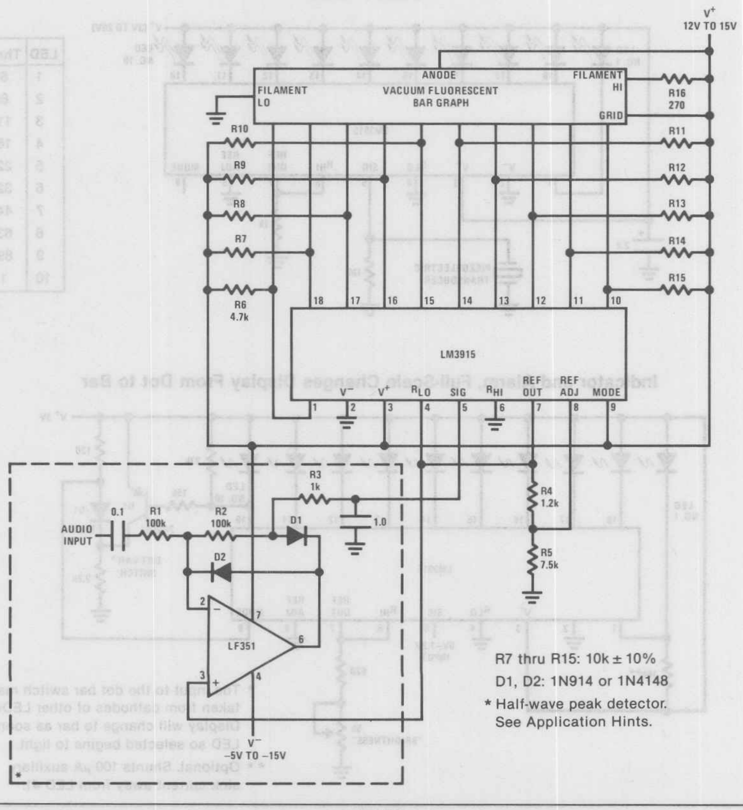
Typical Applications (Continued)

60 dB Dot Mode Display



* Optional. Shunts 100 μA auxiliary sink current away from LED #11.

Driving Vacuum Fluorescent Display



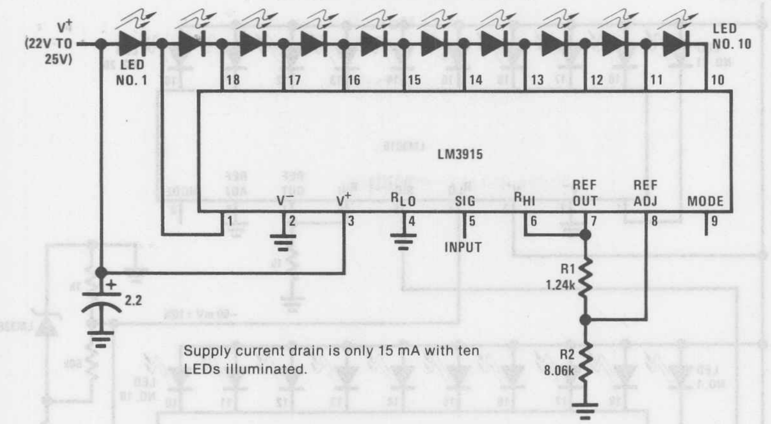
R7 thru R15: 10k ± 10%

D1, D2: 1N914 or 1N4148

* Half-wave peak detector. See Application Hints.

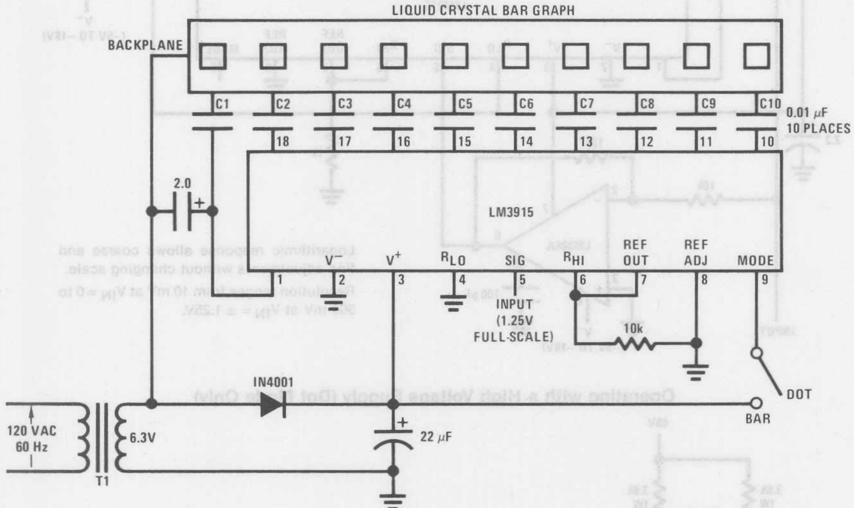
Typical Applications (Continued)

Low Current Bar Mode Display

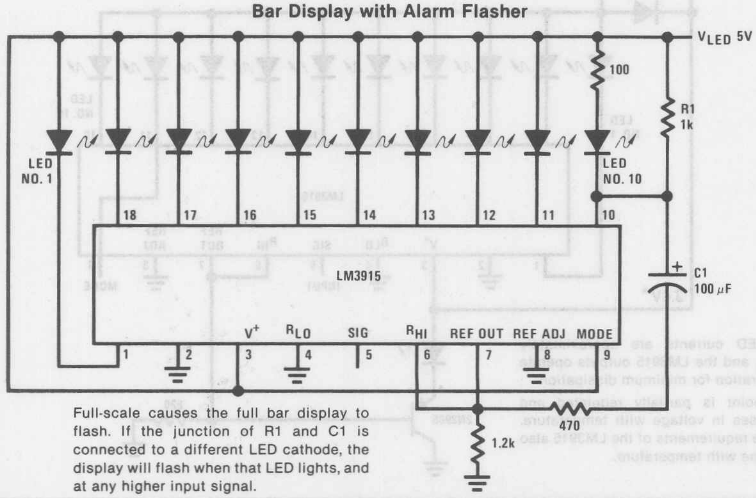


Supply current drain is only 15 mA with ten LEDs illuminated.

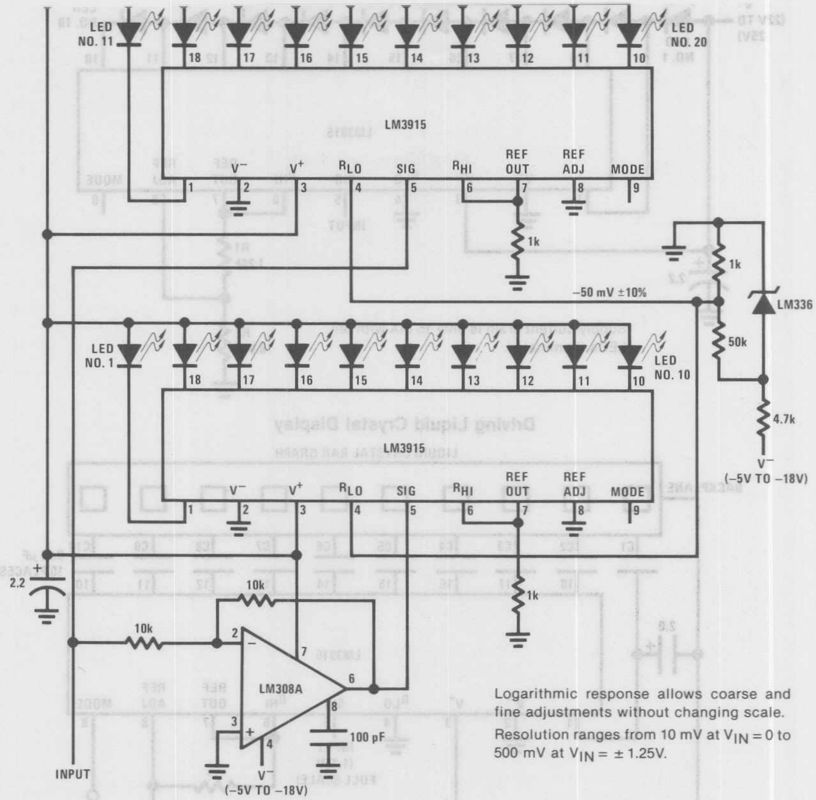
Driving Liquid Crystal Display



Bar Display with Alarm Flasher

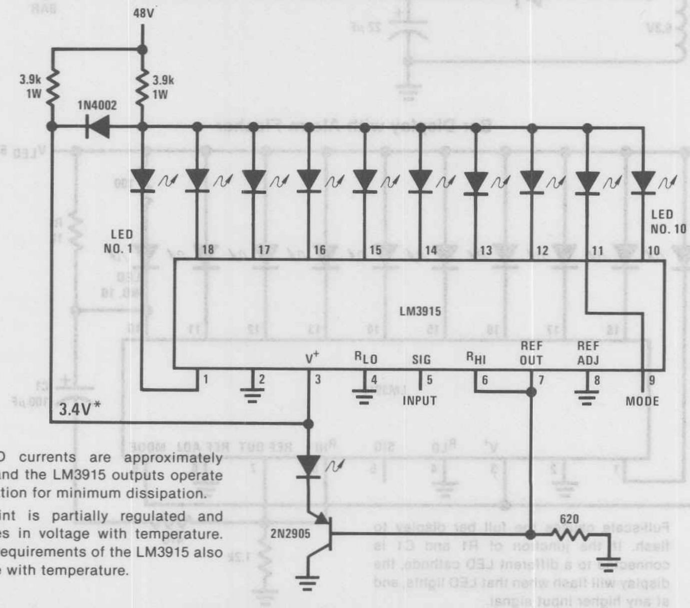


Full-scale causes the full bar display to flash. If the junction of R1 and C1 is connected to a different LED cathode, the display will flash when that LED lights, and at any higher input signal.



Logarithmic response allows coarse and fine adjustments without changing scale. Resolution ranges from 10 mV at $V_{IN} = 0$ to 500 mV at $V_{IN} = \pm 1.25V$.

Operating with a High Voltage Supply (Dot Mode Only)

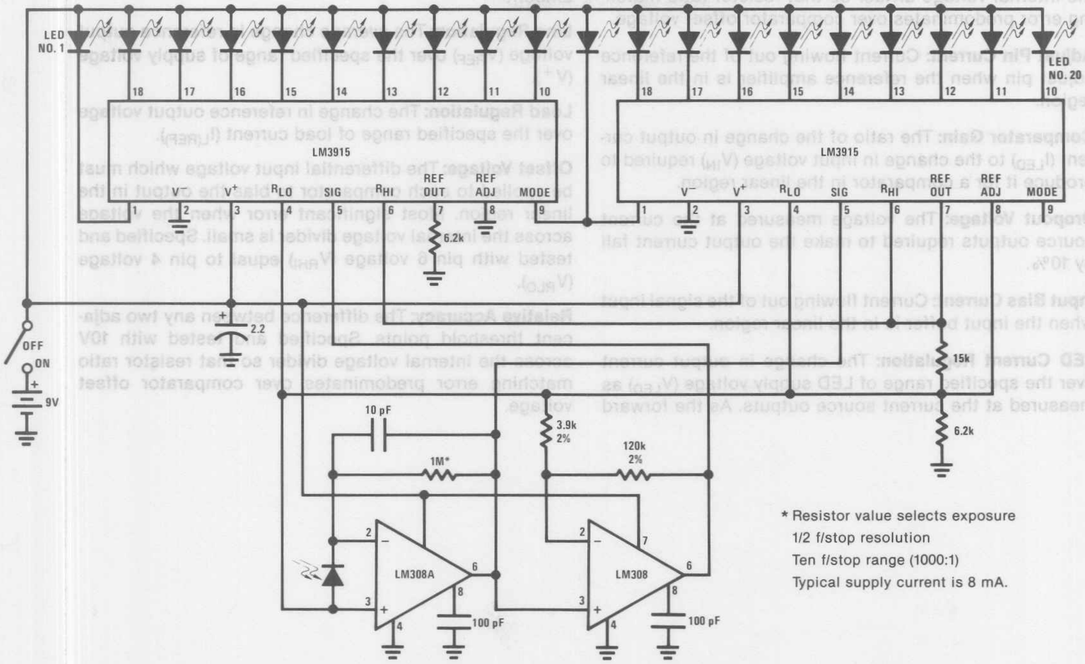


The LED currents are approximately 10 mA, and the LM3915 outputs operate in saturation for minimum dissipation.

*This point is partially regulated and decreases in voltage with temperature. Voltage requirements of the LM3915 also decrease with temperature.

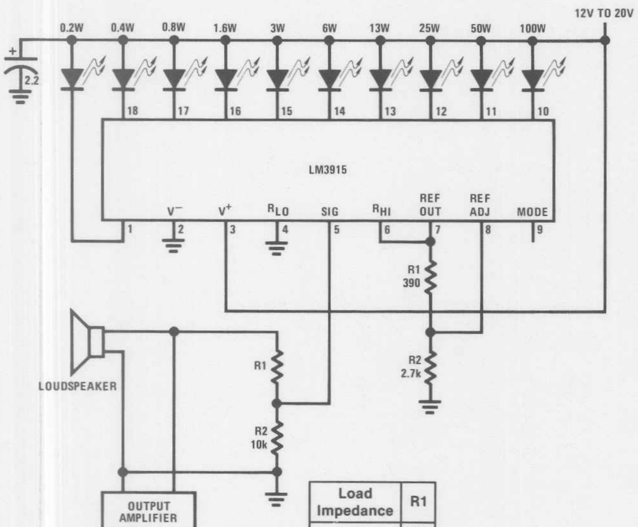
Typical Applications (Continued)

Light Meter



* Resistor value selects exposure
1/2 f/stop resolution
Ten f/stop range (1000:1)
Typical supply current is 8 mA.

Audio Power Meter

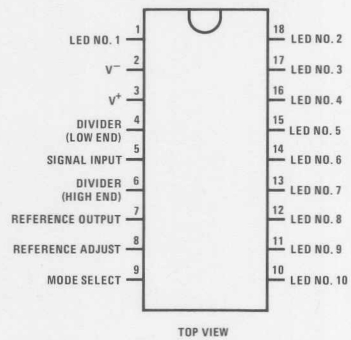


Load Impedance	R1
4Ω	10k
8Ω	18k
16Ω	30k

See Application Hints for optional Peak or Average Detector

Connection Diagram

Dual-In-Line Package



Order Number LM3915J
See NS Package J18A

Order Number LM3915N
See NS Package N18A

Definition of Terms

Absolute Accuracy: The difference between the observed threshold voltage and the ideal threshold voltage for each comparator. Specified and tested with 10V across the internal voltage divider so that resistor ratio matching error predominates over comparator offset voltage.

Adjust Pin Current: Current flowing out of the reference adjust pin when the reference amplifier is in the linear region.

Comparator Gain: The ratio of the change in output current (I_{LED}) to the change in input voltage (V_{IN}) required to produce it for a comparator in the linear region.

Dropout Voltage: The voltage measured at the current source outputs required to make the output current fall by 10%.

Input Bias Current: Current flowing out of the signal input when the input buffer is in the linear region.

LED Current Regulation: The change in output current over the specified range of LED supply voltage (V_{LED}) as measured at the current source outputs. As the forward voltage of an LED does not change significantly with a small change in forward current, this is equivalent to changing the voltage at the LED anodes by the same amount.

Line Regulation: The average change in reference output voltage (V_{REF}) over the specified range of supply voltage (V^+).

Load Regulation: The change in reference output voltage over the specified range of load current ($I_{L(REF)}$).

Offset Voltage: The differential input voltage which must be applied to each comparator to bias the output in the linear region. Most significant error when the voltage across the internal voltage divider is small. Specified and tested with pin 6 voltage (V_{RHI}) equal to pin 4 voltage (V_{RLO}).

Relative Accuracy: The difference between any two adjacent threshold points. Specified and tested with 10V across the internal voltage divider so that resistor ratio matching error predominates over comparator offset voltage.

National Semiconductor

LM3916 Dot/Bar Display Driver

General Description

The LM3916 is a monolithic integrated circuit that senses analog voltage levels and drives ten LEDs, LCDs or vacuum fluorescent displays, providing an electronic version of the popular VU meter. One pin changes the display from a bar graph to a moving dot display. LED current drive is regulated and programmable, eliminating the need for current limiting resistors. The whole display system can operate from a single supply as low as 3V or as high as 25V.

The IC contains an adjustable voltage reference and an accurate ten-step voltage divider. The high-impedance input buffer accepts signals down to ground and up to within 1.5V of the positive supply. Further, it needs no protection against inputs of ±35V. The input buffer drives 10 individual comparators referenced to the precision divider. Accuracy is typically better than 0.2 dB.

Audio applications include average or peak level indicators, and power meters. Replacing conventional meters with an LED bar graph results in a faster responding, more rugged display with high visibility that retains the ease of interpretation of an analog display.

The LM3916 is extremely easy to apply. A 1.2V full-scale meter requires only one resistor in addition to the ten LEDs. One more resistor programs the full-scale anywhere from 1.2V to 12V independent of supply voltage. LED brightness is easily controlled with a single pot.

The LM3916 is very versatile. The outputs can drive LCDs, vacuum fluorescents and incandescent bulbs as well as LEDs of any color. Multiple devices can be cascaded for a dot or bar mode display for increased range and/or resolution. Useful in other applications are the linear LM3914 and the logarithmic LM3915.

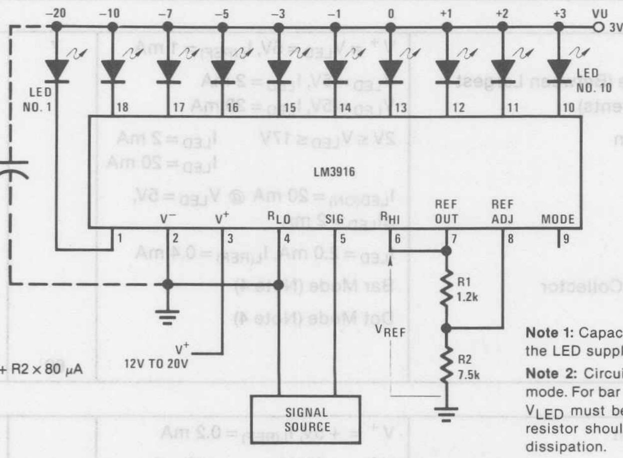
Features

- Fast responding electronic VU meter
- Drives LEDs, LCDs, or vacuum fluorescents
- Bar or dot display mode externally selectable by user
- Expandable to displays of 70 dB
- Internal voltage reference from 1.2V to 12V
- Operates with single supply of 3V to 25V
- Inputs operate down to ground
- Output current programmable from 1 mA to 30 mA
- Input withstands ±35V without damage or false outputs
- Outputs are current regulated, open collectors
- Directly drives TTL or CMOS
- The internal 10-step divider is floating and can be referenced to a wide range of voltages

The LM3916 is rated for operation from 0°C to +70°C. The LM3916N is available in an 18-lead molded DIP package and the LM3916J comes in the 18-lead ceramic DIP.

Typical Applications

0V to 10V VU Meter



$$V_{REF} = 1.25V\left(1 + \frac{R2}{R1}\right) + R2 \times 80\ \mu A$$

$$I_{LED} = \frac{12.5V}{R1} + \frac{V_{REF}}{2.2\ k\Omega}$$

Note 1: Capacitor C1 is required if leads to the LED supply are 6" or longer.

Note 2: Circuit as shown is wired for dot mode. For bar mode, connect pin 9 to pin 3. V_{LED} must be kept below 7V or dropping resistor should be used to limit IC power dissipation.

Ceramic DIP(J)	1W
Molded DIP(N)	625 mW
Supply Voltage	25V
Voltage on Output Drivers	25V
Divider Voltage	-100 mV to V^+
Reference Load Current	10 mA
Storage Temperature Range	$-55°C$ to $+150°C$
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 1)

Parameter	Conditions (Note 1)	Min	Typ	Max	Units
Comparators					
Offset Voltage, Buffer and First Comparator	$0V \le V_{RLO} = V_{RHI} \le 12V$, $I_{LED} = 1$ mA		3	10	mV
Offset Voltage, Buffer and Any Other Comparator	$0V \le V_{RLO} = V_{RHI} \le 12V$, $I_{LED} = 1$ mA		3	15	mV
Gain ($\Delta I_{LED}/\Delta V_{IN}$)	$I_{L(REF)} = 2$ mA, $I_{LED} = 10$ mA	3	8		mA/mV
Input Bias Current (at Pin 5)	$0V \le V_{IN} \le (V^+ - 1.5V)$		10	50	nA
Input Signal Overvoltage	No Change in Display	-35		35	V
Voltage Divider					
Divider Resistance	Total, Pin 6 to 4	6.5	10	15	kΩ
Relative Accuracy (Input Change Between Any Two Threshold Points)	(Note 2)				
	$-1 \text{ dB} \le V_{IN} \le 3 \text{ dB}$	0.75	1.0	1.25	dB
	$-7 \text{ dB} \le V_{IN} \le -1 \text{ dB}$	1.5	2.0	2.5	dB
	$-10 \text{ dB} \le V_{IN} \le -7 \text{ dB}$	2.5	3.0	2.5	dB
Absolute Accuracy	(Note 2)				
	$V_{IN} = 2, 1, 0, -1$ dB	-0.25		$+0.25$	dB
	$V_{IN} = -3, -5$ dB	-0.5		$+0.5$	dB
	$V_{IN} = -7, -10, -20$ dB	-1		$+1$	dB
Voltage Reference					
Output Voltage	$0.1 \text{ mA} \le I_{L(REF)} \le 4$ mA, $V^+ = V_{LED} = 5V$	1.2	1.28	1.34	V
Line Regulation	$3V \le V^+ \le 18V$		0.01	0.03	%/V
Load Regulation	$0.1 \text{ mA} \le I_{L(REF)} \le 4$ mA, $V^+ = V_{LED} = 5V$		0.4	2	%
Output Voltage Change with Temperature	$0°C \le T_A \le +70°C$, $I_{L(REF)} = 1$ mA, $V^+ = V_{LED} = 5V$		1		%
Adjust Pin Current			75	120	μA
Output Drivers					
LED Current	$V^+ = V_{LED} = 5V$, $I_{L(REF)} = 1$ mA	7	10	13	mA
LED Current Difference (Between Largest and Smallest LED Currents)	$V_{LED} = 5V$, $I_{LED} = 2$ mA		0.12	0.4	mA
	$V_{LED} = 5V$, $I_{LED} = 20$ mA		1.2	3	mA
LED Current Regulation	$2V \le V_{LED} \le 17V$, $I_{LED} = 2$ mA		0.1	0.25	mA
	$I_{LED} = 20$ mA		1	3	mA
Dropout Voltage	$I_{LED(ON)} = 20$ mA @ $V_{LED} = 5V$, $\Delta I_{LED} = 2$ mA			1.5	V
Saturation Voltage	$I_{LED} = 2.0$ mA, $I_{L(REF)} = 0.4$ mA		0.15	0.4	V
Output Leakage, Each Collector	Bar Mode (Note 4)		0.1	100	μA
Output Leakage	Dot Mode (Note 4)				
Pins 10–18			0.1	100	μA
Pin 1		60	150	450	μA
Supply Current					
Standby Supply Current (All Outputs Off)	$V^+ = +5V$, $I_{L(REF)} = 0.2$ mA		2.4	4.2	mA
	$V^+ = +20V$, $I_{L(REF)} = 1.0$ mA		6.1	9.2	mA

Notes

Note 1: Unless otherwise stated, all specifications apply with the following conditions:

$3\ V_{DC} \le V^+ \le 20\ V_{DC}$ $\quad -0.015V \le V_{RLO} \le 12\ V_{DC}$ $\quad T_A = 25°C$, $I_{L(REF)} = 0.2$ mA, pin 9 connected to pin 3 (bar mode).

$3\ V_{DC} \le V_{LED} \le V^+$ $\quad V_{REF}, V_{RHI}, V_{RLO} \le (V^+ - 1.5V)$ $\quad$ For higher power dissipations, pulse testing is used.

$-0.015V \le V_{RHI} \le 12\ V_{DC}$ $\quad 0V \le V_{IN} \le V^+ - 1.5V$

Note 2: Accuracy is measured referred to +3 dB = +10.000 V_{DC} at pin 5, with +10.000 V_{DC} at pin 6, and 0.000 V_{DC} at pin 4. At lower full-scale voltages, buffer and comparator offset voltage may add significant error. See table for threshold voltages.

Note 3: Pin 5 input current must be limited to ±3 mA. The addition of a 39k resistor in series with pin 5 allows ±100V signals without damage.

Note 4: Bar mode results when pin 9 is within 20 mV of V^+. Dot mode results when pin 9 is pulled at least 200 mV below V^+. LED #10 (pin 10 output current) is disabled if pin 9 is pulled 0.9V or more below V_{LED}.

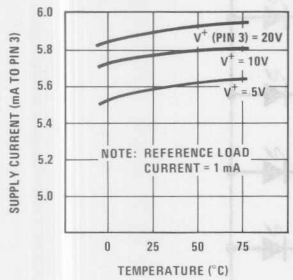
Note 5: The maximum junction temperature of the LM3916 is 100°C. Devices must be derated for operation at elevated temperatures. Junction to ambient thermal resistance is 75°C/W for the ceramic DIP (J package) and 120°C/W for the molded DIP (N package).

LM3916 THRESHOLD VOLTAGE (Note 2)

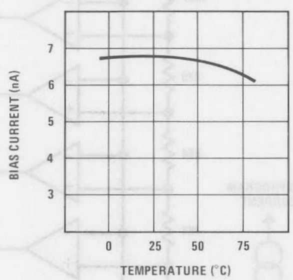
	Volts				Volts		
dB	Min	Typ	Max	dB	Min	Typ	Max
3	9.985	10.000	10.015	−3 ± 1/2	4.732	5.012	5.309
2 ± 1/4	8.660	8.913	9.173	−5 ± 1/2	3.548	3.981	4.467
1 ± 1/4	7.718	7.943	8.175	−7 ± 1	2.818	3.162	3.548
0 ± 1/4	6.879	7.079	7.286	−10 ± 1	1.995	2.239	2.512
−1 ± 1/2	5.957	6.310	6.683	−20 ± 1	0.631	0.708	0.794

Typical Performance Characteristics

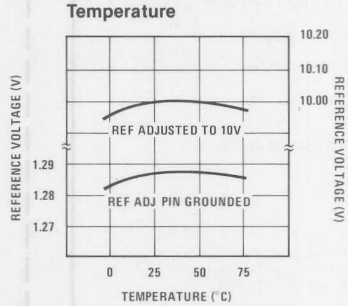
Supply Current vs Temperature



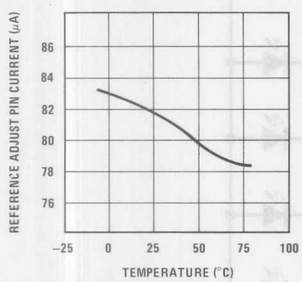
Operating Input Bias Current vs Temperature



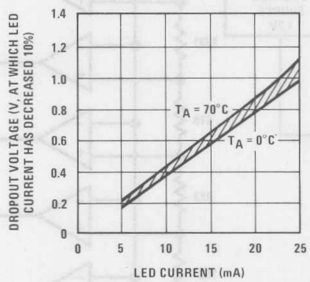
Reference Voltage vs Temperature



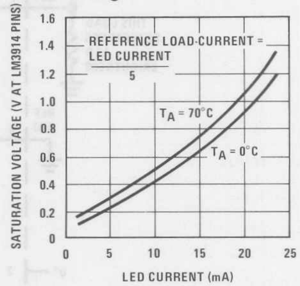
Reference Adjust Pin Current vs Temperature



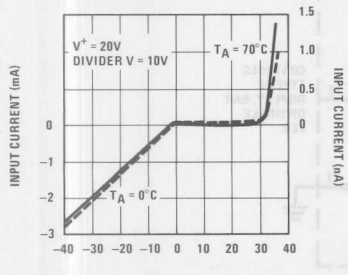
LED Current-Regulation Dropout



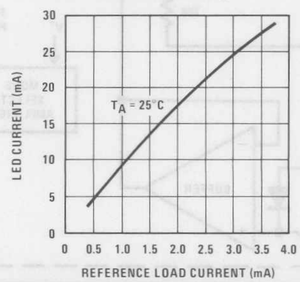
LED Driver Saturation Voltage



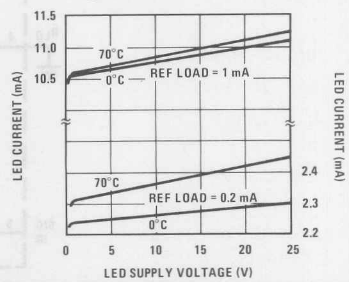
Input Current Beyond Signal Range (Pin 5)



LED Current vs Reference Loading

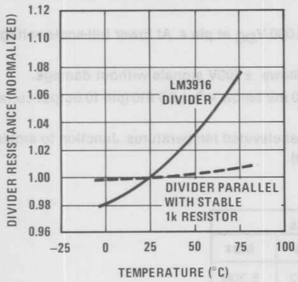


LED Driver Current Regulation

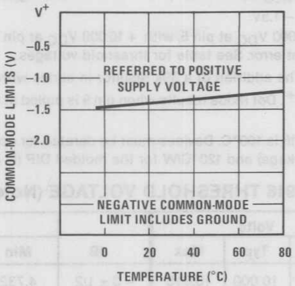


Typical Performance Characteristics (Continued)

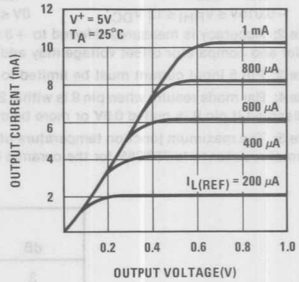
Total Divider Resistance vs Temperature



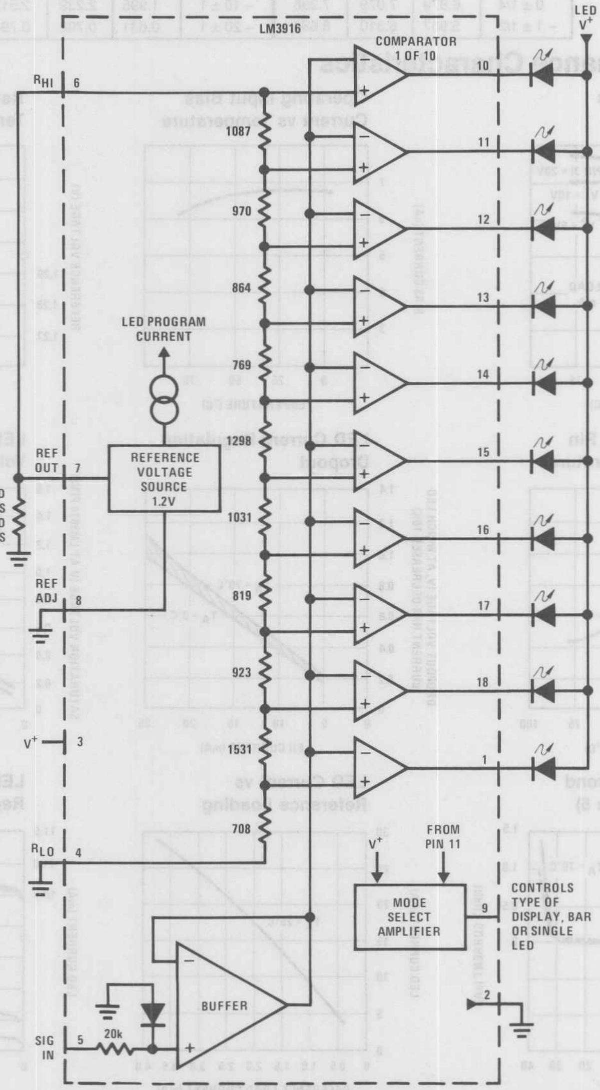
Common-Mode Limits



Output Characteristics



Block Diagram (Showing Simplest Application)



Functional Description

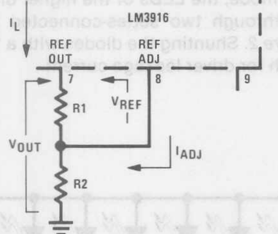
The simplified LM3916 block diagram is included to give the general idea of the circuit's operation. A high input impedance buffer operates with signals from ground to 12V, and is protected against reverse and overvoltage signals. The signal is then applied to a series of 10 comparators; each of which is biased to a different comparison level by the resistor string.

In the example illustrated, the resistor string is connected to the internal 1.25V reference voltage. As the input voltage varies from 0 to 1.25, the comparator outputs are driven low one by one, switching on the LED indicators. The resistor divider can be connected between any 2 voltages, providing that they are at least 1.5V below V^+ and no lower than V^-.

Internal Voltage Reference

The reference is designed to be adjustable and develops a nominal 1.25V between the REF OUT (pin 7) and REF ADJ (pin 8) terminals. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R2 giving an output voltage of:

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}\,R2$$



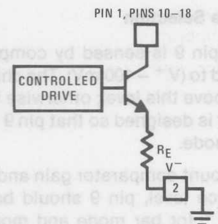
Since the 120 μA current (max) from the adjust terminal represents an error term, the reference was designed to minimize changes of this current with V^+ and load changes. For correct operation, reference load current should be between 80 μA and 5 mA. Load capacitance should be less than 0.05 μF.

Current Programming

A feature not completely illustrated by the block diagram is the LED brightness control. The current drawn out of the reference voltage pin (pin 7) determines LED current. Approximately 10 times this current will be drawn through each lighted LED, and this current will be relatively constant despite supply voltage and temperature changes. Current drawn by the internal 10-resistor divider, as well as by the external current and voltage-setting divider should be included in calculating LED drive current. The ability to modulate LED brightness with time, or in proportion to input voltage and other signals can lead to a number of novel displays or ways of indicating input overvoltages, alarms, etc.

The LM3916 outputs are current-limited NPN transistors as shown below. An internal feedback loop regulates the transistor drive. Output current is held at about 10 times the reference load current, independent of output voltage and processing variables, as long as the transistor is not saturated.

LM3916 Output Circuit



Outputs may be run in saturation with no adverse effects, making it possible to directly drive logic. The effective saturation resistance of the output transistors, equal to R_E plus the transistors' collector resistance, is about 50Ω. It's also possible to drive LEDs from rectified AC with no filtering. To avoid oscillations, the LED supply should be bypassed with a 2.2 μF tantalum or 10 μF aluminum electrolytic capacitor.

Mode Pin Use

Pin 9, the Mode Select input, permits chaining of multiple devices, and controls bar or dot mode operation. The following tabulation shows the basic ways of using this input. Other more complex uses will be illustrated in the applications.

Bar Graph Display: Wire Mode Select (pin 9) *directly* to pin 3 (V^+ pin).

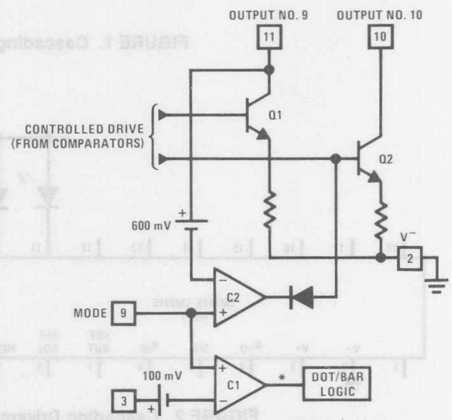
Dot Display, Single LM3916 Driver: Leave the Mode Select pin open circuit.

Dot Display, 20 or More LEDs: Connect pin 9 of the *first* driver in the series (i.e., the one with the lowest input voltage comparison points) to pin 1 of the next higher LM3916 driver. Continue connecting pin 9 of lower input drivers to pin 1 of higher input drivers for 30 or more LED displays. The last LM3916 driver in the chain will have pin 9 left open. All previous drivers should have a 20k resistor in parallel with LED #9 (pin 11 to V_{LED}).

Mode Pin Functional Description

This pin actually performs two functions. Refer to the simplified block diagram below.

Block Diagram of Mode Pin Function



mally referenced to (V^+ − 100 mV). The chip is in bar mode when pin 9 is above this level; otherwise it's in dot mode. The comparator is designed so that pin 9 can be left open circuit for dot mode.

Taking into account comparator gain and variation in the 100 mV reference level, pin 9 should be no more than 20 mV below V^+ for bar mode and more than 200 mV below V^+ (or open circuit) for dot mode. In most applications, pin 9 is either open (dot mode) or tied to V^+ (bar mode). In bar mode, pin 9 should be connected directly to pin 3. Large currents drawn from the power supply (LED current, for example) should not share this path so that large IR drops are avoided.

Dot Mode Carry

In order for the display to make sense when multiple drivers are cascaded in dot mode, special circuitry has been included to shut off LED #10 of the first device when LED #1 of the second device comes on. The connection for cascading in dot mode has already been described and is depicted in *Figure 1*.

As long as the input signal voltage is below the threshold of the second driver, LED #11 is off. Pin 9 of driver #1 thus sees effectively an open circuit so the chip is in dot mode. As soon as the input voltage reaches the threshold of LED #11, pin 9 of driver #1 is pulled an LED drop (1.5V or more) below V_{LED}. This condition is sensed by comparator C2, C2 low, which shuts off output transistor Q2, extinguishing LED #10.

V_{LED} is sensed via the 20k resistor connected to pin 11. The very small current (less than 100 μA) that is diverted from LED #9 does not noticeably affect its intensity.

An auxiliary current source at pin 1 keeps at least 100 μA flowing through LED #11 even if the input voltage rises high enough to extinguish the LED. This ensures that pin 9 of driver #1 is held low enough to force LED #10 off when *any* higher LED is illuminated. While 100 μA does not normally produce significant LED illumination, it may be noticeable when using high-efficiency LEDs in a dark environment. If this is bothersome, the simple cure is to shunt LED #11 (and LED #1) with a 10k resistor. The 1V IR drop is more than the 900 mV worst case required to hold off LED #10 yet small enough that LED #11 does not conduct significantly.

In some circuits a number of outputs on the higher device are not used. Examples include the high resolution VU meter and the expanded range VU meter circuits (see Typical Applications). To provide the proper carry sense voltage in dot mode, the LEDs of the higher driver IC are tied to V_{LED} through two series-connected diodes as shown in *Figure 2*. Shunting the diodes with a 1k resistor provides a path for driver leakage current.

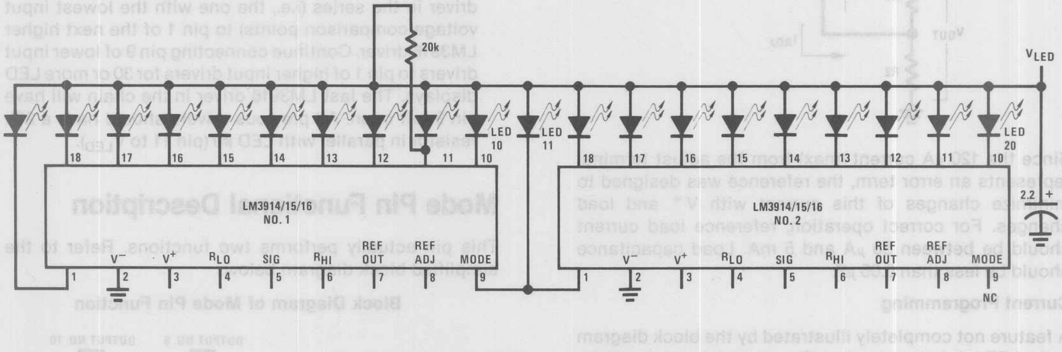


FIGURE 1. Cascading LM3914/15/16 Series in Dot Mode

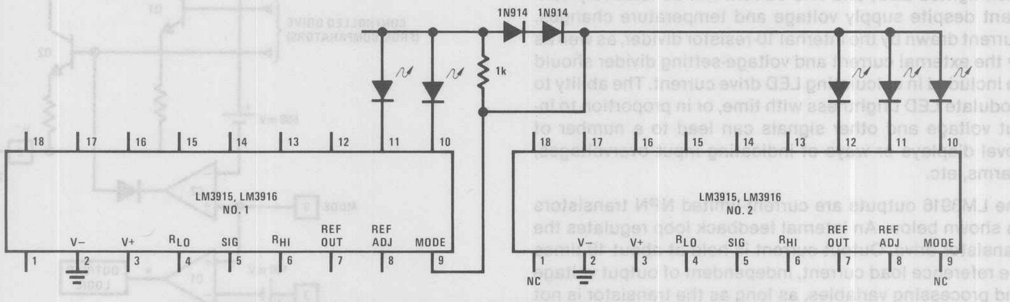


FIGURE 2. Cascading Drivers in Dot Mode with Pin 1 of Driver #2 Unused

Mode Pin Functional Description (Continued)

Other Device Characteristics

The LM3915 is relatively low-powered itself, and since any number of LEDs can be powered from about 3V, it is a very efficient display driver. Typical standby supply current (all LEDs OFF) is 1.6 mA. However, any reference loading adds 4 times that current drain to the V^+ (pin 3) supply input. For example, an LM3915 with a 1 mA reference pin load (1.3k) would supply almost 10 mA to every LED while drawing only 10 mA from its V^+ pin supply. At full-scale, the IC is typically drawing less than 10% of the current supplied to the display.

The display driver does not have built-in hysteresis so that the display does not jump instantly from one LED to the next. Under rapidly changing signal conditions, this cuts down high frequency noise and often an annoying flicker. An "overlap" is built in so that at no time are all segments completely off in the dot mode. Generally one LED fades in while the other fades out over a 1 mV to 3 mV range. The change may be much more rapid between LED #10 of one device and LED #1 of a *second* device cascaded.

Application Hints

The most difficult problem occurs when large LED currents are being drawn, especially in bar graph mode. These currents flowing out of the ground pin cause voltage drops in external wiring, and thus errors and oscillations. Bringing the return wires from signal sources, reference ground and bottom of the resistor string to a single point very near pin 2 is the best solution.

Long wires from V_{LED} to LED anode common can cause oscillations. The usual cure is bypassing the LED anodes with a 2.2 μF tantalum or 10 μF aluminum electrolytic capacitor. If the LED anode line wiring is inaccessible, often a 0.1 μF capacitor from pin 1 to pin 2 will be sufficient.

If there is a large amount of LED overlap in the bar mode, oscillation or excessive noise is usually the problem. In cases where proper wiring and bypassing fail to stop oscillations, V^+ voltage at pin 3 is usually below suggested limits. When several LEDs are lit in dot mode, the problem is usually an AC component of the input signal which should be filtered out. Expanded scale meter applications may have one or both ends of the internal voltage divider terminated at relatively high value resistors. These high-impedance ends should be bypassed to pin 2 with 0.1 μF.

Power dissipation, especially in bar mode should be given consideration. For example, with a 5V supply and all LEDs programmed to 20 mA the driver will dissipate over 600 mW. In this case a 7.5Ω resistor in series with the LED supply will cut device heating in half. The negative end of the resistor should be bypassed with a 2.2 μF solid tantalum or 10 μF aluminum electrolytic capacitor to pin 2.

Tips on Rectifier Circuits

The simplest way to display an AC signal using the LM3916 is to apply it right to pin 5 unrectified. Since the LED illuminated represents the instantaneous value of the AC waveform, one can readily discern both peak and average values of audio signals in this manner. The LM3916 will respond to positive half-cycles only but will not be damaged by signals up to ± 35V (or up to ± 100V if a 39k resistor is in series with the input). A smear or bar type display results even though the LM3916 is connected for dot mode. The LEDs should be run at 20 mA to 30 mA for high enough average intensity.

True average or peak detection requires rectification. If an LM3916 is set up with 10V full scale across its voltage divider, the turn-on point for the first LED is only 450 mV. A simple silicon diode rectifier won't work well at the low end due to the 600 mV diode threshold. The half-wave peak detector in *Figure 3* uses a PNP emitter-follower in front of the diode. Now, the transistor's base-emitter voltage cancels out the diode offset, within about 100 mV. This approach is usually satisfactory when a single LM3916 is used for a 23 dB display.

Display circuits such as the extended range VU meter using two or more drivers for a dynamic range of 40 dB or greater require more accurate detection. In the precision half-wave rectifier of *Figure 4* the effective diode offset is reduced by a factor equal to the open-loop gain of the op amp. Filter capacitor C2 charges through R3 and discharges through R2 and R3, so that appropriate selection of these values results in either a peak or an average detector. The circuit has a gain equal to R2/R1.

It's best to capacitively couple the input. Audio sources frequently have a small DC offset that can cause significant error at the low end of the log display. Op amps that slew quickly, such as the LF351, LF353 or LF356, are needed to faithfully respond to sudden transients. It may be necessary to trim out the op amp DC offset voltage to accurately cover a 60 dB range. Best results are obtained if the circuit is adjusted for the correct output when a low-level AC signal (10 to 20 mV) is applied, rather than adjusting for zero output with zero input.

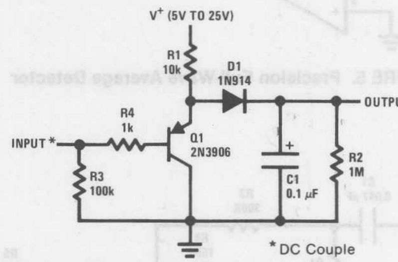
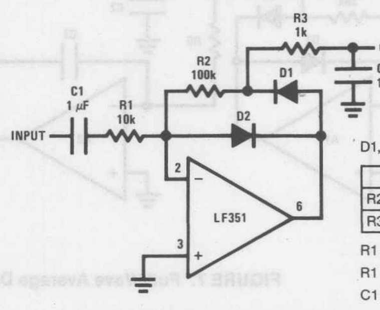


FIGURE 3. Half-Wave Peak Detector



D1, D2: 1N914 or 1N4148

	Average	Peak
R2	1k	100k
R3	100k	1k

R1 = R2 for $A_V = 1$

R1 = R2/10 for $A_V = 10$

C1 = 10/R1

FIGURE 4. Precision Half-Wave Rectifier

Application Hints (Continued)

For precision full-wave averaging use the circuit in *Figure 5*. Using 1% resistors for R1 through R4, gain for positive and negative signal differs by only 0.5 dB worst case. Substituting 5% resistors increases this to 2 dB worst case. (A 2 dB gain difference means that the display may have a ±1 dB error when the input is a nonsymmetrical transient). The averaging time constant is R5•C2. A simple modification results in the precision full-wave detector of *Figure 6*. Since the filter capacitor is not buffered, this circuit can drive only high impedance loads such as the input of an LM3916.

AUDIO METER STANDARDS

VU Meter

The audio level meter most frequently encountered is the VU meter. Its characteristics are defined in the ANSI specification C165. The LM3916's outputs correspond to the meter indications specified with the omission of the −2 VU indication. The VU scale divisions differ slightly from a linear scale in order to obtain whole numbers in dB.

Some of the most important specifications for an AC meter are its dynamic characteristics. These define how the meter responds to transients and how fast the reading decays. The VU meter is a relatively slow full-wave averaging type, specified to reach 99% deflection in 300 ms and overshoot by 1 to 1.5%. In engineering terms this means a slightly underdamped second order response with a resonant frequency of 2.1 Hz and a Q of 0.62. *Figure 7* depicts a simple rectifier/filter circuit that meets these criteria.

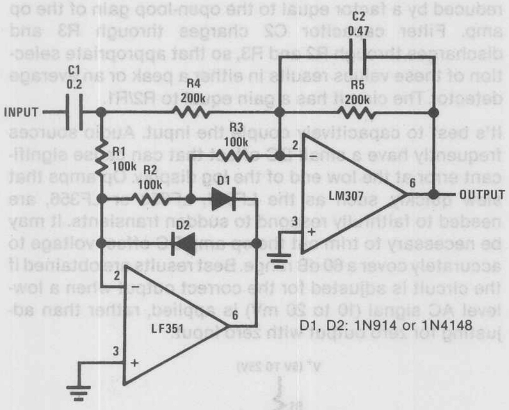


FIGURE 5. Precision Full-Wave Average Detector

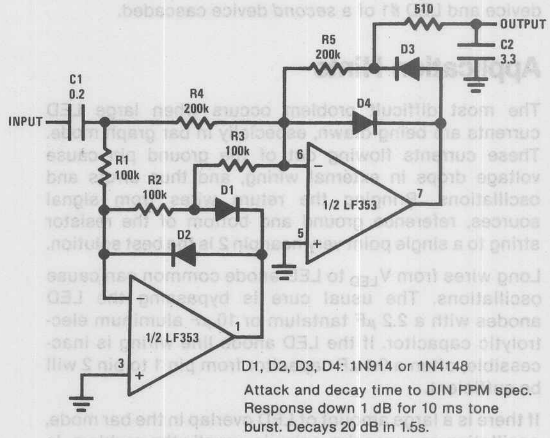
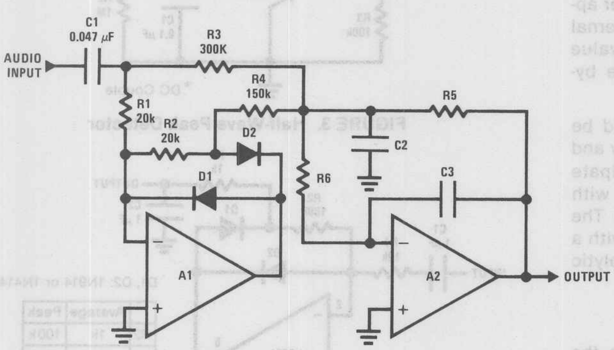


FIGURE 6. Precision Full-Wave Peak Detector



Gain	R5	R6	C2	C3
1	100k	43k	2.0	0.56 μF
10	1M	100k	1.0	0.056 μF

Design Equations

$$\frac{1}{R5 \cdot R6 \cdot C2 \cdot C3} = \omega_0^2 = 177\ \text{sec}^{-2}$$

$$\frac{1}{C2}\left(\frac{1}{R3} + \frac{1}{R4} + \frac{1}{R5} + \frac{1}{R6}\right) = \frac{\omega_0}{Q} = 21.5\ \text{sec}^{-1}$$

$R3 = 2R4$

$R1 = R2 << R4$

A1, A2: 1/2 LF353

D1, D2: 1N914 or 1N4148

* Reaches 99% level at 300 ms after applied tone burst and overshoots 1.2%.

FIGURE 7. Full-Wave Average Detector to VU Meter Specifications*

Application Hints (Continued)

Peak Program Meter

The VU meter, originally intended for signals sent via telephone lines, has shortcomings when used in high fidelity systems. Due to its slow response time, a VU meter will not accurately display transients that can saturate a magnetic tape or drive an amplifier into clipping. The fast-attack peak program meter (PPM) which does not have this problem is becoming increasingly popular.

While several European organizations have specifications for peak program meters, the German DIN specification 45406 is becoming a de facto standard. Rather than respond instantaneously to peak, however, PPM specifications require a finite "integration time" so that only peaks wide enough to be audible are displayed. DIN 45406 calls for a response of 1 dB down from steady-state for a 10 ms tone burst and 4 dB down for a 3 ms tone burst. These requirements are consistent with the other frequently encountered spec of 2 dB down for a 5 ms burst and are met by an attack time constant of 1.7 ms.

The specified return time of 1.5s to −20 dB requires a 650 ms decay time constant. The full-wave peak detector of *Figure 6* satisfies both the attack and decay time criteria.

Cascading the LM3916

The LM3916 by itself covers the 23 dB range of the conventional VU meter. To display signals of 40 dB or 70 dB dynamic range, the LM3916 may be cascaded with the 3 dB/step LM3915s. Alternatively, two LM3916s may be cascaded for increased resolution over a 28 dB range. Refer to the Extended Range VU Meter and High Resolution VU Meter in the Typical Applications section for the complete circuits for both dot and bar mode displays.

To obtain a display that makes sense when an LM3915 and an LM3916 are cascaded, the −20 dB output from the LM3916 is dropped. The full-scale display for the LM3915 is set at 3 dB below the LM3916's −10 dB output and the rest of the thresholds continue the 3 dB/step spacing. A simple, low cost approach is to set the reference voltage of the two chips 16 dB apart as in *Figure 5*. The LM3915, with pin 8 grounded, runs at 1.25V full-scale. R1 and R2 set the LM3916's reference 16 dB higher or 7.89V. Variation in the two on-chip references and resistor tolerance may cause a ±1 dB error in the −10 dB to −13 dB transition. If this is objectionable, R2 can be trimmed.

The drawback of the aforementioned approach is that the threshold of LED #1 on the LM3915 is only 56 mV. Since comparator offset voltage may be as high as 10 mV, large errors can occur at the first few thresholds. A better approach, as shown in *Figure 9*, is to keep the reference the same for both drivers (10V in the example) and *amplify* the input signal by 16 dB ahead of the LM3915. Alternatively,

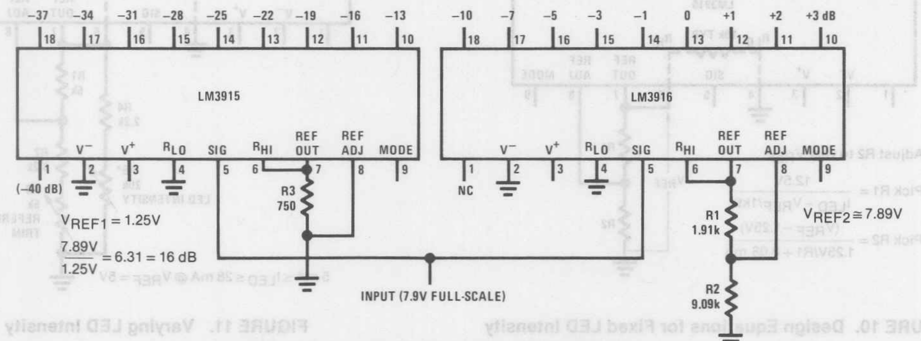


FIGURE 8. Low Cost Circuit for 40 dB Display

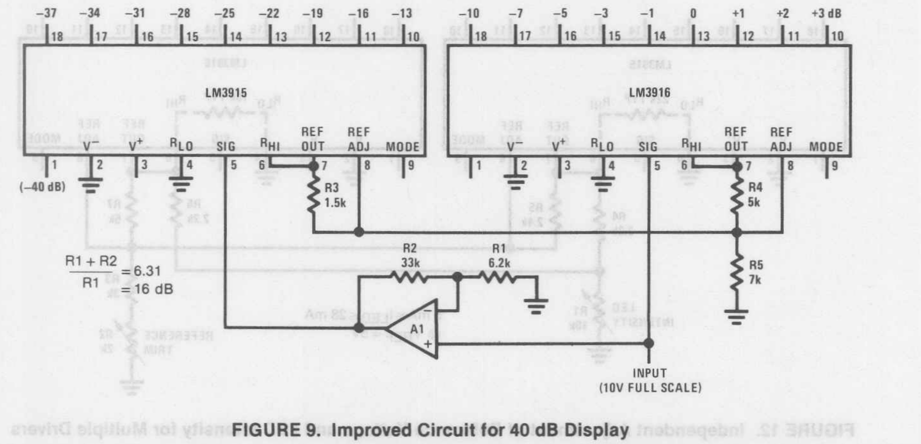


FIGURE 9. Improved Circuit for 40 dB Display

tenuated by 16 dB to drive the LM3915.

To extend this approach to get a 70 dB display, another 30 dB of amplification must be placed in the signal path ahead of the lowest LM3915. Extreme care is required as the lowest LM3915 displays input signals down to 2 mV! Several offset nulls may be required. High currents should not share the same path as the low level signal. Also power line wiring should be kept away from signal lines.

TIPS ON REFERENCE VOLTAGE AND LED CURRENT PROGRAMMING

Single Driver

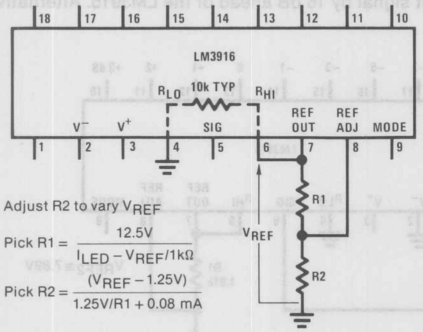
The equations in *Figure 10* illustrate how to choose resistor values to set reference voltage for the simple case where no LED intensity adjustment is required. A LED current of 10 mA to 20 mA generally produces adequate illumination. Having 10V full-scale across the internal voltage divider gives best accuracy by keeping signal level high relative to the offset voltage of the internal com-

least 10 mA. R1 will typically be between 1 kΩ and 5 kΩ. To trim the reference voltage, vary R2.

The circuit in *Figure 11* shows how to add a LED intensity control which can vary LED current from 5 mA to 28 mA. Choosing $V_{REF} = 5V$ lowers the current drawn by the ladder, increasing the intensity adjustment range. The reference adjustment has some effect on LED intensity but the reverse is not true.

Multiple Drivers

Figure 12 shows how to obtain a common reference trim and intensity control for two drivers. The two ICs may be connected in cascade or may be handling separate channels for stereo. This technique can be extended for larger numbers of drivers by varying the values of R1, R2 and R3. Because the LM3915 has a greater ladder resistance, R5 was picked less than R7 in such a way as to provide equal reference load currents. The ICs' internal references track within 100 mV so that worst case error from chip to chip is only 0.2 dB for $V_{REF} = 5V$.



Adjust R2 to vary V_{REF}

$$\text{Pick R1} = \frac{12.5V}{I_{LED} - V_{REF}/1k\Omega}$$

$$\text{Pick R2} = \frac{(V_{REF} - 1.25V)}{1.25V/R1 + 0.08\ mA}$$

FIGURE 10. Design Equations for Fixed LED Intensity

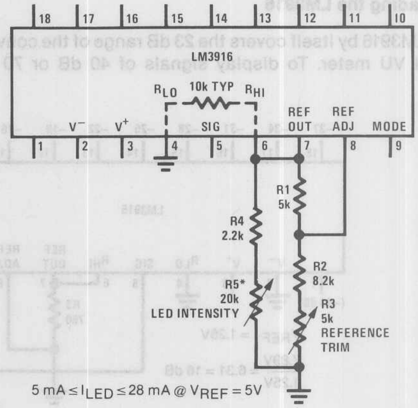


FIGURE 11. Varying LED Intensity

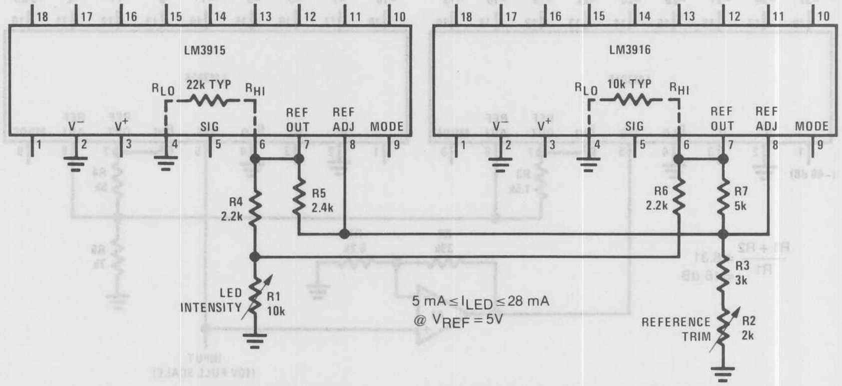


FIGURE 12. Independent Adjustment of Reference Voltage and LED Intensity for Multiple Drivers

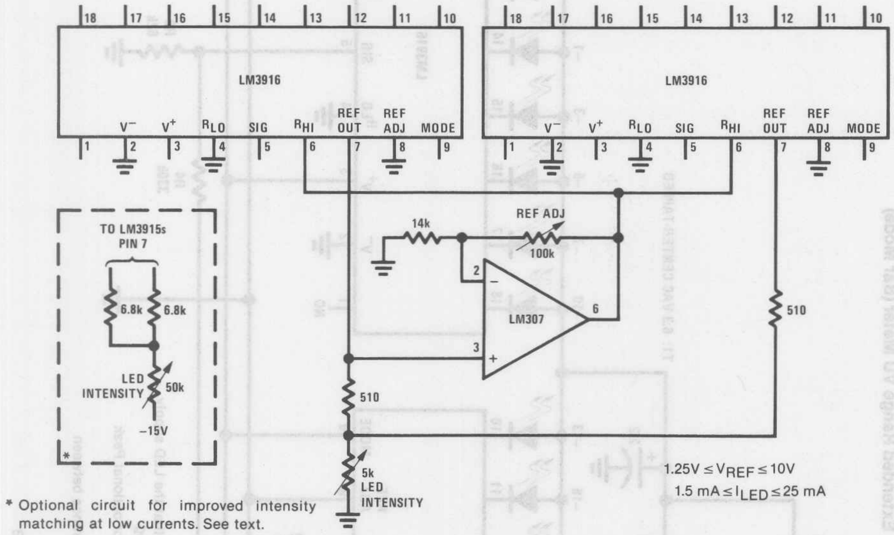
Application Hints (Continued)

The scheme in *Figure 13* is useful when the reference and LED intensity must be adjusted independently over a wide range. The R_{HI} voltage can be adjusted from 1.2V to 10V with no effect on LED current. Since the internal divider here does not load down the reference, minimum LED current is much lower. At the minimum recommended reference load of 80 μA, LED current is about 0.8 mA. The resistor values shown give a LED current range from 1.5 mA to 25 mA.

At the low end of the intensity adjustment, the voltage drop across the 510Ω current-sharing resistors is so small that chip to chip variation in reference voltage may yield a visible variation in LED intensity. The optional approach shown of connecting the bottom end of the intensity control pot to a negative supply overcomes this problem by allowing a larger voltage drop across the (larger) current-sharing resistors.

Other Applications

For increased resolution, it's possible to obtain a display with a smooth transition between LEDs. This is accomplished by superimposing an AC waveform on top of the input level as shown in *Figure 14*. The signal can be a triangle, sawtooth or sine wave from 60 Hz to 1 kHz. The display can be run in either dot or bar mode.



* Optional circuit for improved intensity matching at low currents. See text.

FIGURE 13. Wide-Range Adjustment of Reference Voltage and LED Intensity for Multiple Drivers

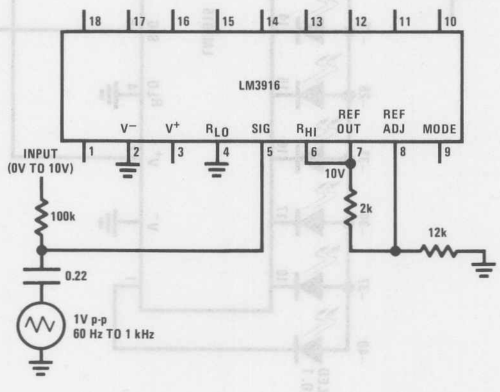
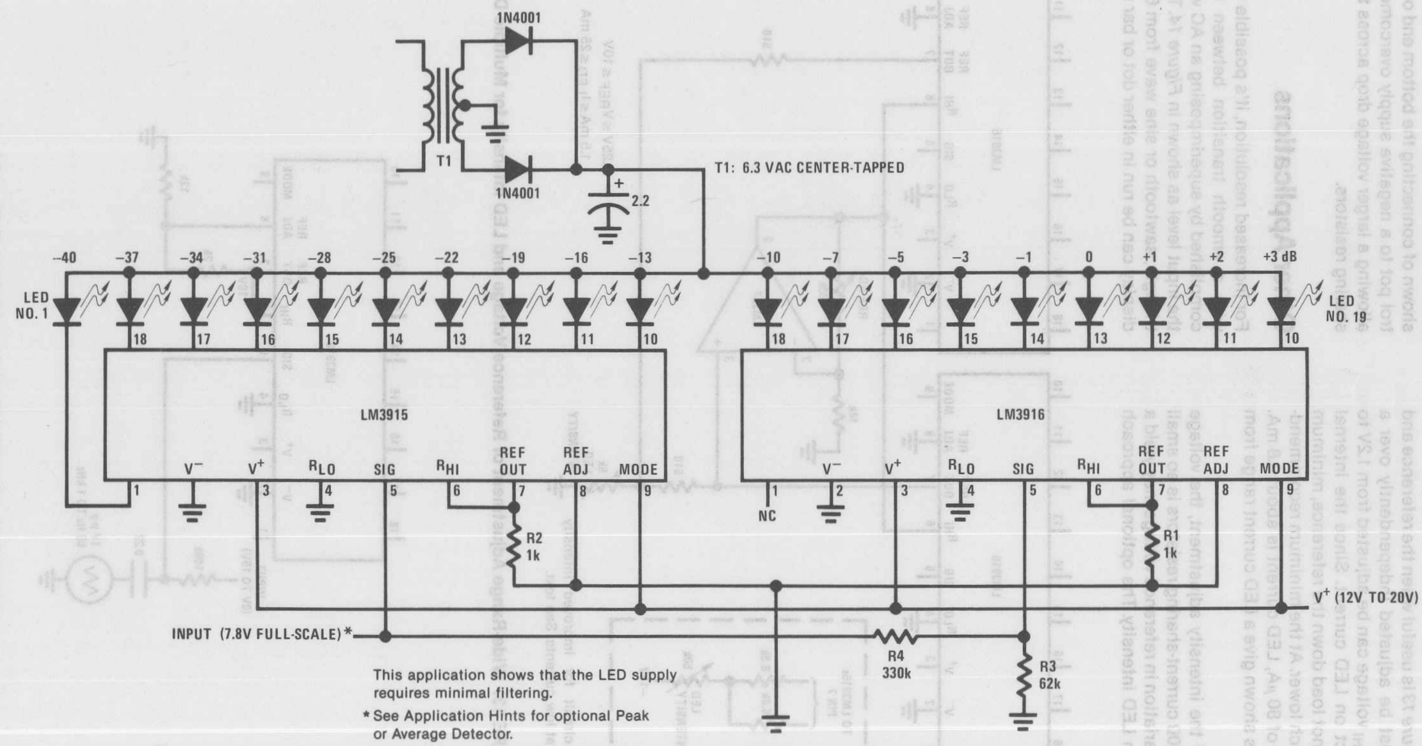


FIGURE 14. 0V to 10V VU Meter with Smooth Transitions

Typical Applications (Continued)

Extended Range VU Meter (Bar Mode)



This application shows that the LED supply requires minimal filtering.

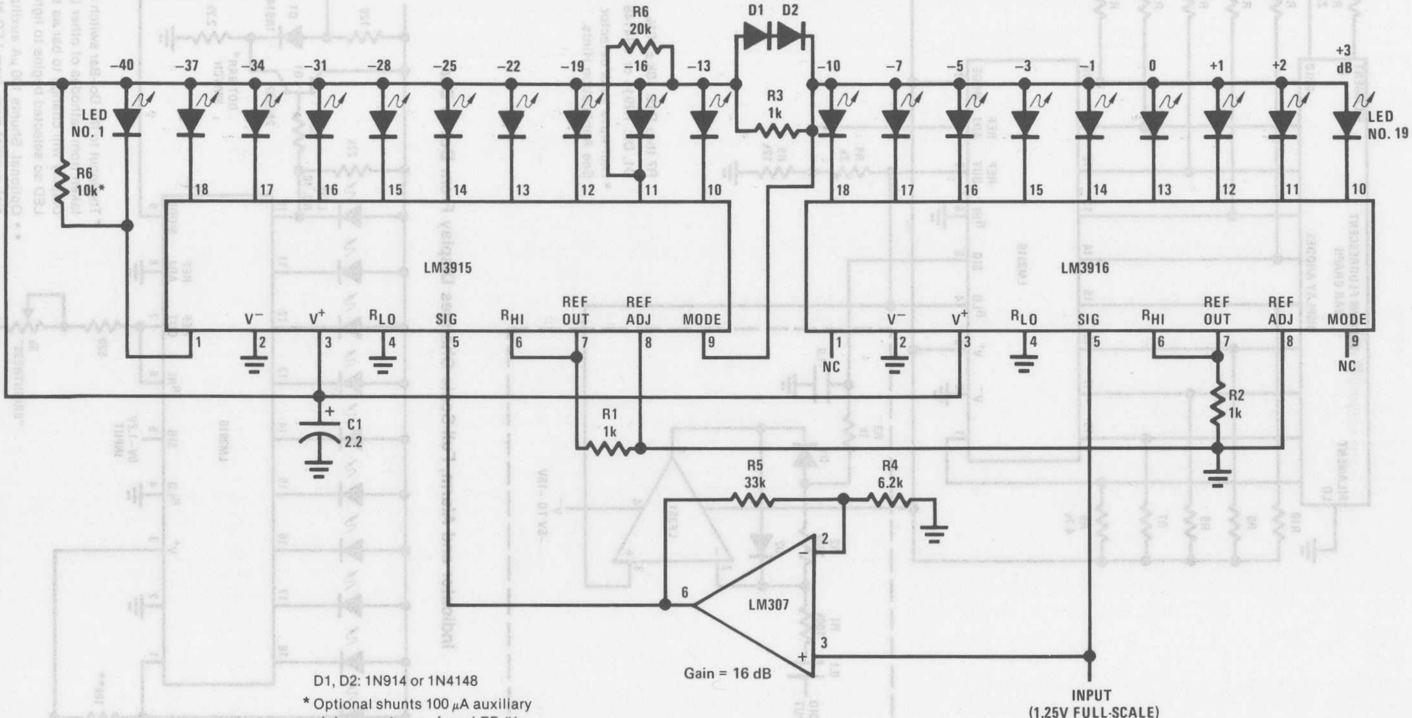
*See Application Hints for optional Peak or Average Detector.

†Adjust R3 for 3 dB difference between LED #11 and LED #12

$$\frac{R3}{R3 + R4} = 0.158 = -16\ dB$$

Typical Applications (Continued)

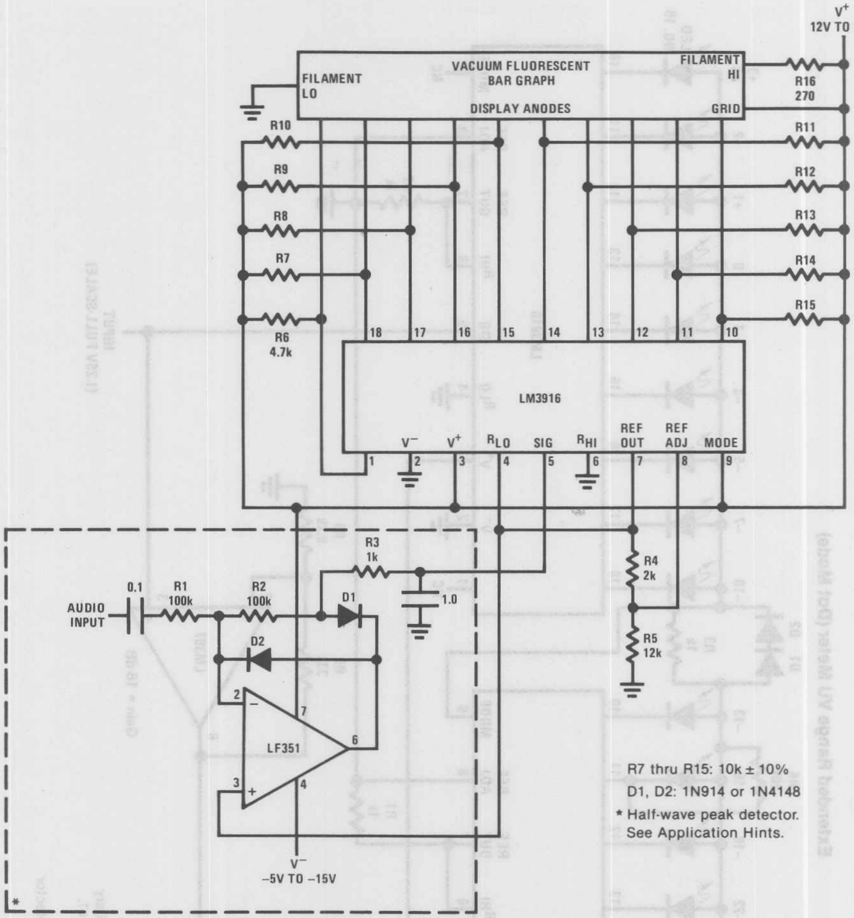
Extended Range VU Meter (Dot Mode)



D1, D2: 1N914 or 1N4148

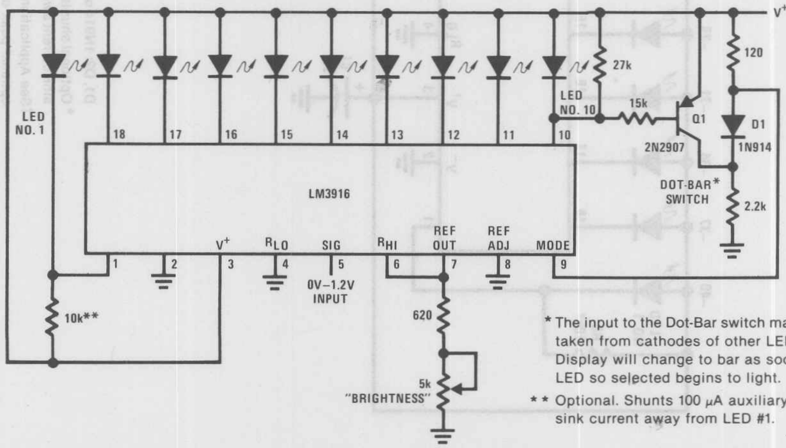
* Optional shunts 100 μA auxiliary sink current away from LED #1.

†See Application Hints for optional peak or average detector



R7 thru R15: 10k ± 10%
D1, D2: 1N914 or 1N4148
* Half-wave peak detector.
See Application Hints.

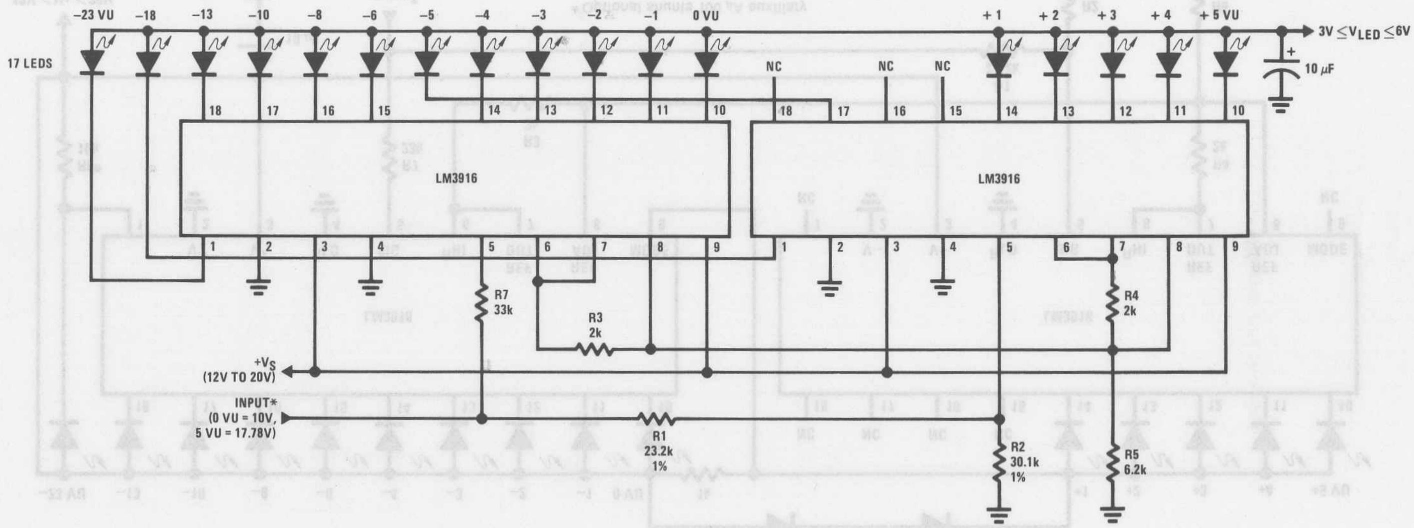
Indicator and Alarm, Full-Scale Changes Display From Dot to Bar



* The input to the Dot-Bar switch may be taken from cathodes of other LEDs. Display will change to bar as soon as the LED so selected begins to light.

** Optional. Shunts 100 μA auxiliary sink current away from LED #1.

High Resolution VU Meter (Bar Mode)

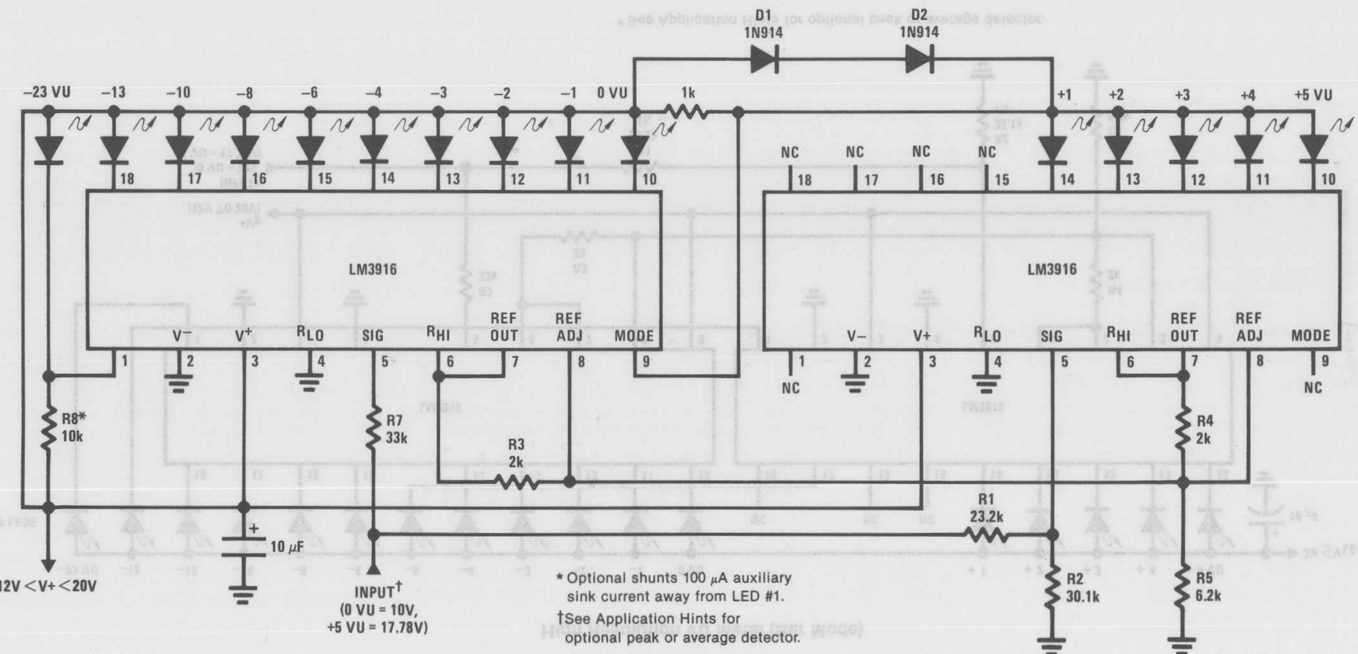


* See Application Hints for optional peak or average detector.

$$\frac{R2}{R1 + R2} \cong 0.562 = -5\ \text{dB}$$

or $R1 \cong 0.788 \cdot R2$

High Resolution VU Meter (Dot Mode)



* Optional shunts 100 µA auxiliary sink current away from LED #1.

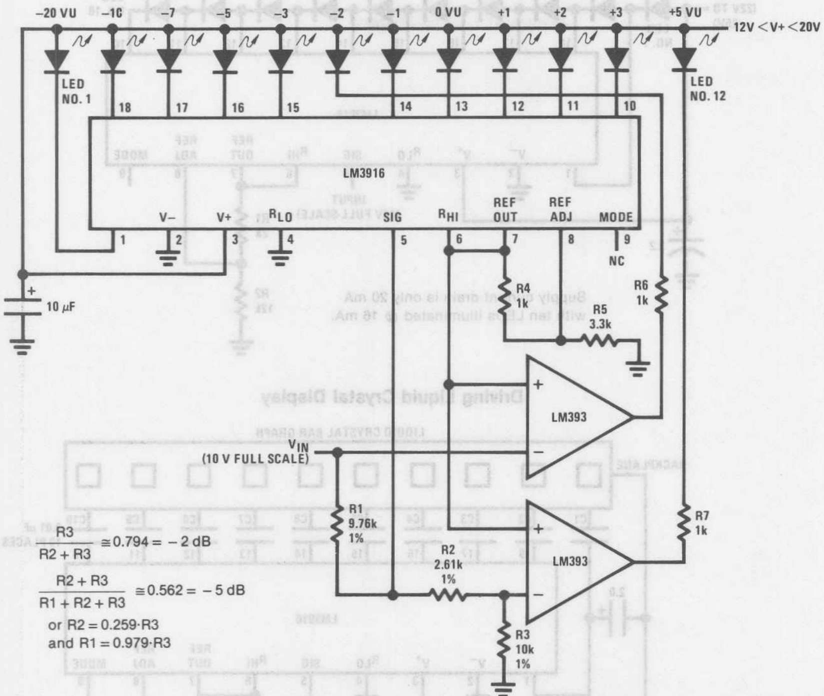
†See Application Hints for optional peak or average detector.

$$\frac{R2}{R1 + R2} \cong 0.562 = -5\ \text{dB}$$

or $R1 \cong 0.788 \cdot R2$

Typical Applications (Continued)

Displaying Additional Levels

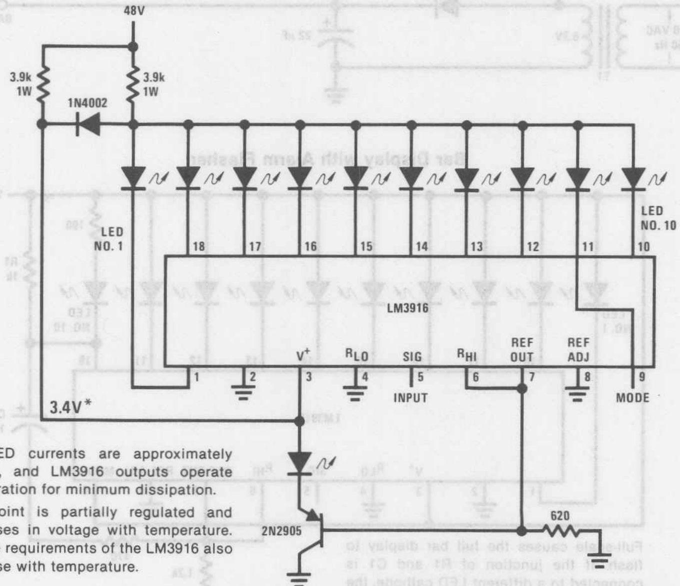


$$\frac{R3}{R2+R3} \cong 0.794 = -2\text{ dB}$$

$$\frac{R2+R3}{R1+R2+R3} \cong 0.562 = -5\text{ dB}$$

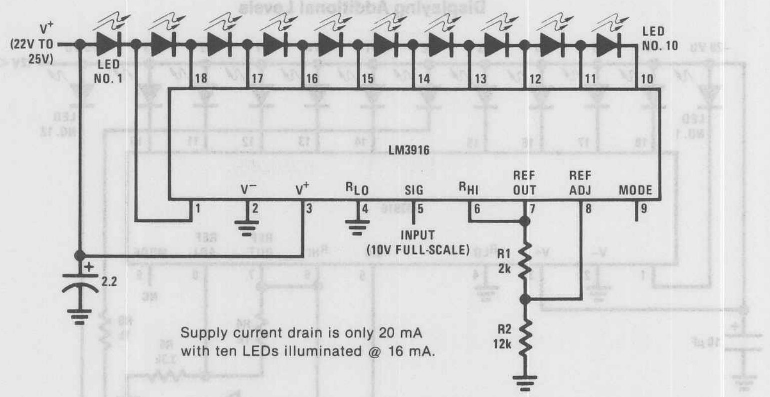
or $R2 = 0.259 \cdot R3$
and $R1 = 0.979 \cdot R3$

Operating with a High Voltage Supply (Dot Mode Only)



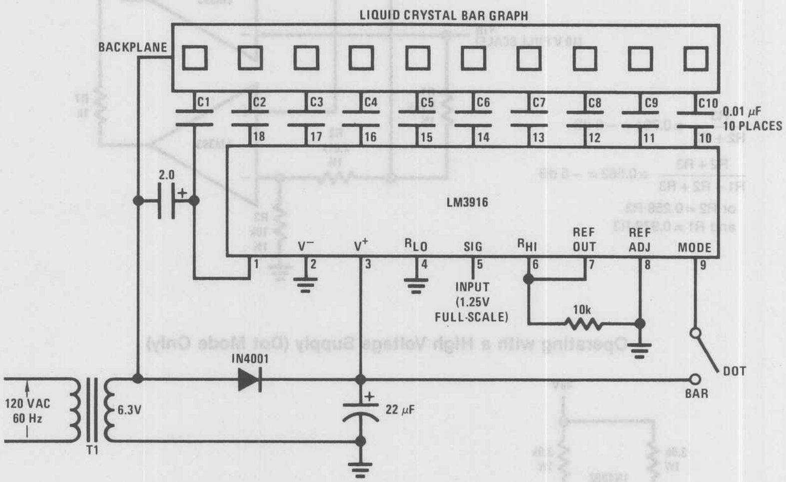
The LED currents are approximately 10 mA, and LM3916 outputs operate in saturation for minimum dissipation.

*This point is partially regulated and decreases in voltage with temperature. Voltage requirements of the LM3916 also decrease with temperature.

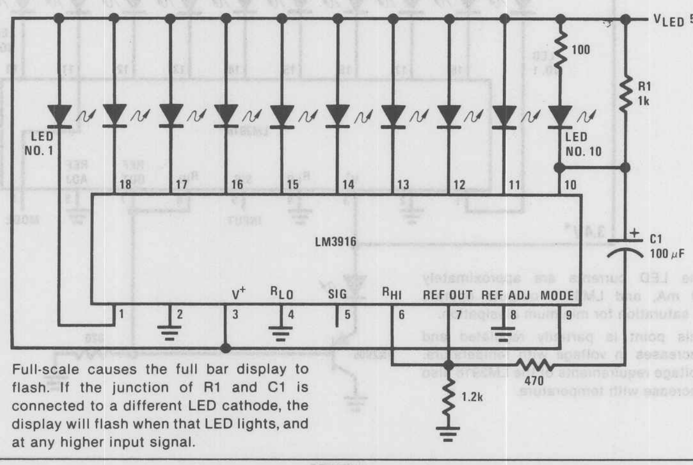


Supply current drain is only 20 mA with ten LEDs illuminated @ 16 mA.

Driving Liquid Crystal Display



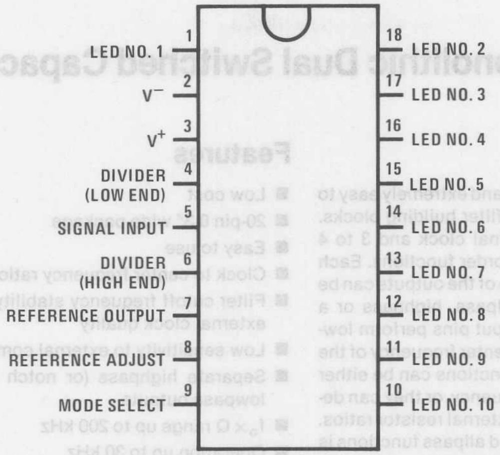
Bar Display with Alarm Flasher



Full-scale causes the full bar display to flash. If the junction of R1 and C1 is connected to a different LED cathode, the display will flash when that LED lights, and at any higher input signal.

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number LM3916J
See NS Package J18A

Order Number LM3916N
See NS Package N18A

Definition of Terms

Absolute Accuracy: The difference between the observed threshold voltage and the ideal threshold voltage for each comparator. Specified and tested with 10V across the internal voltage divider so that resistor ratio matching error predominates over comparator offset voltage.

Adjust Pin Current: Current flowing out of the reference adjust pin when the reference amplifier is in the linear region.

Comparator Gain: The ratio of the change in output current (I_{LED}) to the change in input voltage (V_{IN}) required to produce it for a comparator in the linear region.

Dropout Voltage: The voltage measured at the current source outputs required to make the output current fall by 10%.

Input Bias Current: Current flowing out of the signal input when the input buffer is in the linear region.

LED Current Regulation: The change in output current over the specified range of LED supply voltage (V_{LED}) as measured at the current source outputs. As the forward voltage of an LED does not change significantly with a small change in forward current, this is equivalent to changing the voltage at the LED anodes by the same amount.

Line Regulation: The average change in reference output voltage (V_{REF}) over the specified range of supply voltage (V^+).

Load Regulation: The change in reference output voltage over the specified range of load current ($I_{L(REF)}$).

Offset Voltage: The differential input voltage which must be applied to each comparator to bias the output in the linear region. Most significant error when the voltage across the internal voltage divider is small. Specified and tested with pin 6 voltage (V_{RHI}) equal to pin 4 voltage (V_{RLO}).

Relative Accuracy: The difference between any two adjacent threshold points. Specified and tested with 10V across the internal voltage divider so that resistor ratio matching error predominates over comparator offset voltage.

National Semiconductor

MF10 Universal Monolithic Dual Switched Capacitor Filter

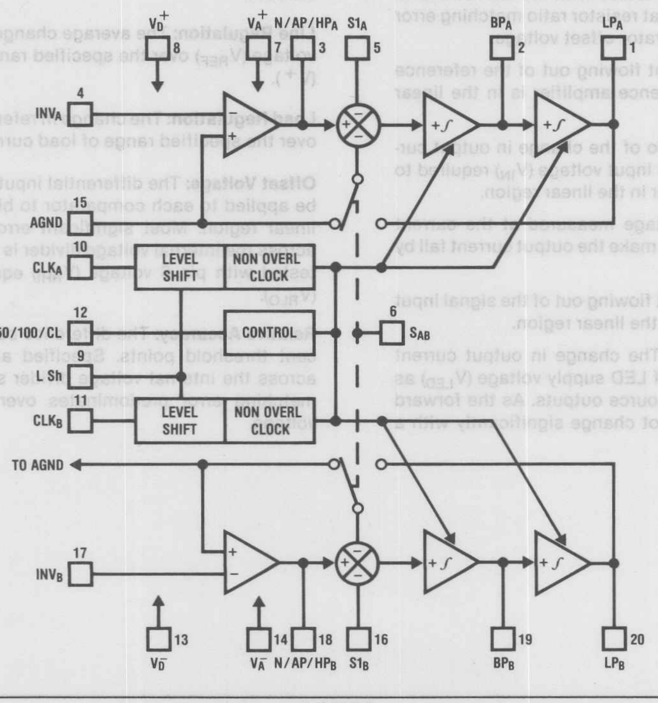
General Description

The MF10 consists of 2 independent and extremely easy to use, general purpose CMOS active filter building blocks. Each block, together with an external clock and 3 to 4 resistors, can produce various 2nd order functions. Each building block has 3 output pins. One of the outputs can be configured to perform either an allpass, highpass or a notch function; the remaining 2 output pins perform lowpass and bandpass functions. The center frequency of the lowpass and bandpass 2nd order functions can be either directly dependent on the clock frequency, or they can depend on both clock frequency and external resistor ratios. The center frequency of the notch and allpass functions is directly dependent on the clock frequency, while the highpass center frequency depends on both resistor ratio and clock. Up to 4th order functions can be performed by cascading the two 2nd order building blocks of the MF10; higher than 4th order functions can be obtained by cascading MF10 packages. Any of the classical filter configurations (such as Butterworth, Bessel, Cauer and Chebyshev) can be formed.

Features

- Low cost
- 20-pin 0.3″ wide package
- Easy to use
- Clock to center frequency ratio accuracy = 0.6%
- Filter cutoff frequency stability directly dependent on external clock quality
- Low sensitivity to external component variation
- Separate highpass (or notch or allpass), bandpass, lowpass outputs
- $f_0 \times Q$ range up to 200 kHz
- Operation up to 30 kHz

System Block Diagram



Absolute Maximum Ratings

Supply Voltage	7V
Power Dissipation	500 mW
Operating Temperature	0°C to 70°C
Storage Temperature	150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Complete Filter) $V_S = \pm 5V$, $T_A = 25°C$

Parameter	Conditions	Min	Typ	Max	Units
Frequency Range	$f_o \times Q < 200$ kHz	20	30		kHz
Clock to Center Frequency Ratio, f_{CLK}/f_o					
MF10BN	Pin 12 High, Q = 10		49.94 ± 0.2%	± 0.6%	
MF10CN	$f_o \times Q < 50$ kHz, Mode 1		49.94 ± 0.2%	± 1.5%	
MF10BN	Pin 12 at Mid Supplies		99.35 ± 0.2%	± 0.6%	
MF10CN	Q = 10, $f_o \times Q < 50$ kHz, Mode 1		99.35 ± 0.2%	± 1.5%	
Q Accuracy (Q Deviation from an Ideal Continuous Filter)					
MF10BN	Pin 12 High, Mode 1		± 2%	± 4%	
MF10CN	$f_o \times Q < 100$ kHz, $f_o < 5$ kHz		± 2%	± 6%	
MF10BN	Pin 12 at Mid Supplies		± 2%	± 3%	
MF10CN	$f_o \times Q < 100$ kHz $f_o < 5$ kHz, Mode 1		± 2%	± 6%	
f_o Temperature Coefficient	Pin 12 High (~50:1)		± 10		ppm/°C
	Pin 12 Mid Supplies (~100:1) $f_o \times Q < 100$ kHz, Mode 1 External Clock Temperature Independent		± 100		ppm/°C
Q Temperature Coefficient	$f_o \times Q < 100$ kHz, Q Setting Resistors Temperature Independent		± 500		ppm/°C
DC Low Pass Gain Accuracy	Mode 1, R1 = R2 = 10k			± 2	%
Crosstalk			50		dB
Clock Feedthrough			10		mV
Maximum Clock Frequency		1	1.5		MHz
Power Supply Current			8	10	mA

Electrical Characteristics (Internal Op Amps) $T_A = 25°C$

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage		± 4	± 5		V
Voltage Swing (Pins 1, 2, 9, 20)	$V_S = \pm 5V$, $R_L = 5k$				
MF10BN		± 3.8	± 4		V
MF10CN		± 3.2	± 3.7		V
Voltage Swing (Pins 3 and 18)	$V_S = \pm 5V$, $R_L = 3.5k$				
MF10BN		± 3.8	± 4		V
MF10CN		± 3.2	± 3.7		V
Output Short Circuit Current	$V_S = \pm 5V$				
Source			3		mA
Sink			1.5		mA
Op Amp Gain BW Product			2.5		MHz
Op Amp Slew Rate			7		V/µs

plex pole pair. f_o is measured at the bandpass output of each 1/2 MF10, and it is the frequency of the bandpass peak occurrence *(Figure 1)*.

Q: quality factor of the 2nd order function complex pole pair. Q is also measured at the bandpass output of each 1/2 MF10 and it is the ratio of f_o over the -3 dB bandwidth of the 2nd order bandpass filter, *Figure 1*. The value of Q is not measured at the lowpass or highpass outputs of the filter, but its value relates to the possible amplitude peaking at the above outputs.

H_{OBP}: the gain in (V/V) of the bandpass output at $f = f_o$.

H_{OLP}: the gain in (V/V) of the lowpass output of each 1/2 MF10 at $f \to 0$ Hz, *Figure 2*.

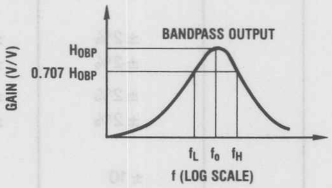
Q_z: the quality factor of the 2nd order function complex zero pair, if any. (Q_z is a parameter used when an allpass output is sought and unlike Q it cannot be directly measured).

f_z: the center frequency of the 2nd order function complex zero pair, if any. If f_z is different from f_o, and if the Q_z is quite high it can be observed as a notch frequency at the allpass output.

f_{notch}: the notch frequency observed at the notch output(s) of the MF10.

H_{ON_1}: the notch output gain as $f \to 0$ Hz.

H_{ON_2}: the notch output gain as $f \to f_{CLK}/2$.

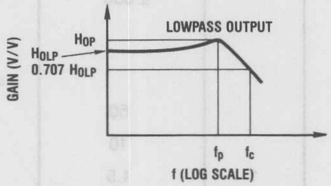


$$Q = \frac{f_o}{f_H - f_L}; \; f_o = \sqrt{f_L f_H}$$

$$f_L = f_o \left(\frac{-1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1} \right)$$

$$f_H = f_o \left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1} \right)$$

FIGURE 1

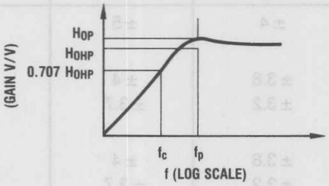


$$f_c = f_o \times \sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}$$

$$f_p = f_o \sqrt{1 - \frac{1}{2Q^2}}$$

$$H_{OP} = H_{OLP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

FIGURE 2



$$f_c = f_o \times \left[\sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}} \right]^{-1}$$

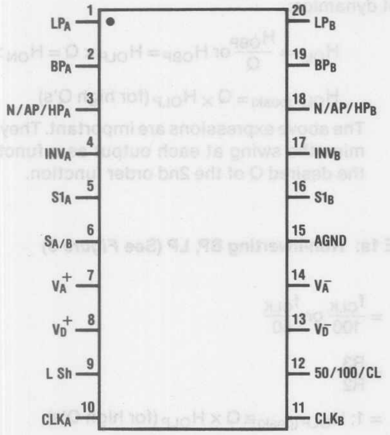
$$f_p = f_o \times \left[\sqrt{1 - \frac{1}{2Q^2}} \right]^{-1}$$

$$H_{OP} = H_{OHP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

FIGURE 3

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number MF10CN or MF10BN

Pin Description

LP, BP, N/AP/HP — These are the lowpass, bandpass, notch or allpass or highpass outputs of each 2nd order section. The LP and BP outputs can sink typically 1 mA and source 3 mA. The N/AP/HP output can typically sink and source 1.5 mA and 3 mA, respectively.

INV — This is the inverting input of the summing op amp of each filter. The pin has static discharge protection.

S1 — S1 is a signal input pin used in the allpass filter configurations (see modes of operation 4 and 5). The pin should be driven with a source impedance of less than 1 kΩ.

$S_{A/B}$ — It activates a switch connecting one of the inputs of the filter's 2nd summer either to analog ground ($S_{A/B}$ low to V_A^-) or to the lowpass output of the circuit ($S_{A/B}$ high to V_A^+). This allows flexibility in the various modes of operation of the IC. $S_{A/B}$ is protected against static discharge.

V_A^+, V_D^+ — Analog positive supply and digital positive supply. These pins are internally connected through the IC substrate and therefore V_A^+ and V_D^+ should be derived from the same power supply source. They have been brought out separately so they can be bypassed by separate capacitors, if desired. They can be externally tied together and bypassed by a single capacitor.

V_A^-, V_D^- — Analog and digital negative supply respectively. The same comments as for V_A^+ and V_D^+ apply here.

L Sh — Level shift pin; it accommodates various clock levels with dual or single supply operation. With dual ±5V supplies, the MF10 can be driven with CMOS clock levels (±5V) and the L Sh pin should be tied either to the system ground or to the negative supply pin. If the same supplies as above are used but T^2L clock levels, derived from 0V to 5V supply, are only available, the L Sh pin should be tied to the system ground. For single supply operation (0V and 10V) the V_D^-, V_A^- pins should be connected to the system ground, the AGND pin should be biased at 5V and the L Sh pin should also be tied to the system ground. This will accommodate both CMOS and T^2L clock levels.

CLK (A or B) — Clock inputs for each switched capacitor filter building block. They should both be of the same level (T^2L or CMOS). The level shift (L Sh) pin description discusses how to accommodate their levels. The duty cycle of the clock should preferably be close to 50% especially when clock frequencies above 200 kHz are used. This allows the maximum time for the op amps to settle which yields optimum filter operation.

50/100/CL — By tying the pin high a 50:1 clock to filter center frequency operation is obtained. Tying the pin at mid supplies (i.e., analog ground with dual supplies) allows the filter to operate at a 100:1 clock to center frequency ratio. When the pin is tied low, a simple current limiting circuitry is triggered to limit the overall supply current down to about 2.5 mA. The filtering action is then aborted.

AGND — Analog ground pin; it should be connected to the system ground for dual supply operation or biased at mid supply for single supply operation. The positive inputs of the filter op amps are connected to the AGND pin so "clean" ground is mandatory. The AGND pin is protected against static discharge.

Modes of Operation

The MF10 is a switched capacitor (sampled data) filter. To fully describe its transfer functions, a time domain approach will be appropriate. Since this may appear cumbersome and, since the MF10 closely approximates continuous filters, the following discussion is based on the well known frequency domain. The following illustrations refer to 1/2 of the MF10; the other 1/2 is identical. Each MF10 can produce a full 2nd order function, so up to 4th order functions can be performed by using cascading techniques.

MODE 1: Notch 1, Bandpass, Lowpass Outputs: $f_{notch} = f_o$ (See *Figure 4*)

f_o = center frequency of the complex pole pair

$$= \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

f_{notch} = center frequency of the imaginary zero pair $= f_o$.

H_{OLP} = Lowpass gain (as $f \to 0$) $= -\frac{R2}{R1}$

H_{OBP} = Bandpass gain (at $f = f_o$) $= -\frac{R3}{R1}$

H_{ON} = Notch output gain as $\left.\begin{matrix} f \to 0 - \frac{R2}{R1} \\ f \to f_{CLK}/2 \end{matrix}\right\}$

$Q = \frac{f_o}{BW} = \frac{R3}{R2}$

= quality factor of the complex pole pair.

BW = the −3 dB bandwidth of the bandpass output.

Circuit dynamics:

$$H_{OLP} = \frac{H_{OBP}}{Q} \text{ or } H_{OBP} = H_{OLP} \times Q = H_{ON} \times Q.$$

$$H_{OLP\,(peak)} \cong Q \times H_{OLP} \text{ (for high Q's)}$$

The above expressions are important. They determine the swing at each output as a function of the desired Q of the 2nd order function.

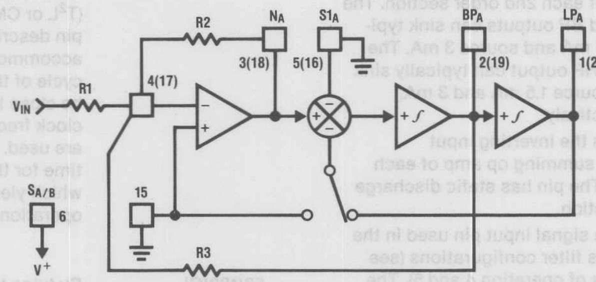


FIGURE 4. MODE 1

MODE 1a: Non-Inverting BP, LP (See *Figure 5*)

$f_o = \frac{f_{CLK}}{100}$ or $\frac{f_{CLK}}{50}$

$Q = \frac{R3}{R2}$

$H_{OLP} = 1$; $H_{OLP\,(peak)} \cong Q \times H_{OLP}$ (for high Q's)

$H_{OBP_1} = -\frac{R3}{R2}$

$H_{OBP_2} = 1$ (non-inverting)

Circuit dynamics: $H_{OBP_1} = Q$

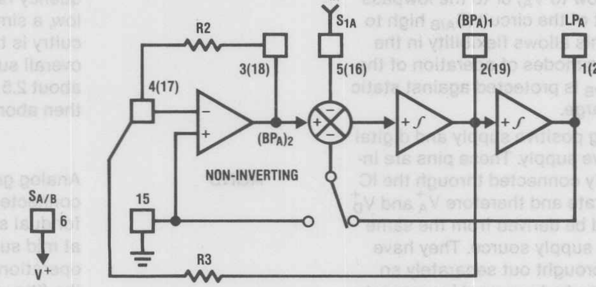


FIGURE 5. MODE 1a

Modes of Operation (Continued)

MODE 2: Notch 2, Bandpass, Lowpass: $f_{notch} < f_o$ (See *Figure 6*)

f_o = center frequency

$$= \frac{f_{CLK}}{100}\sqrt{\frac{R2}{R4}+1} \text{ or } \frac{f_{CLK}}{50}\sqrt{\frac{R2}{R4}+1}$$

$$f_{notch} = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

Q = quality factor of the complex pole pair

$$= \frac{\sqrt{R2/R4+1}}{R2/R3}$$

H_{OLP} = Lowpass output gain (as $f \to 0$)

$$= -\frac{R2/R1}{R2/R4+1}$$

H_{OBP} = Bandpass output gain (at $f = f_o$) = $-R3/R1$

H_{ON_1} = Notch output gain (as $f \to 0$)

$$= -\frac{R2/R1}{R2/R4+1}$$

H_{ON_2} = Notch output gain $\left(\text{as } f \to \frac{f_{CLK}}{2}\right) = -R2/R1$

Filter dynamics: $H_{OBP} = Q\sqrt{H_{OLP}\ H_{ON_2}} = Q\ \sqrt{H_{ON_1}\ H_{ON_2}}$

MODE 3: Highpass, Bandpass, Lowpass Outputs (See *Figure 7*)

$$f_o = \frac{f_{CLK}}{100} \times \sqrt{\frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50} \times \sqrt{\frac{R2}{R4}}$$

Q = quality factor of the complex pole pair

$$= \sqrt{\frac{R2}{R4}} \times \frac{R3}{R2}$$

H_{OHP} = Highpass gain $\left(\text{as } f \to \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1}$

H_{OBP} = Bandpass gain (at $f = f_o$) = $-\frac{R3}{R1}$

H_{OLP} = Lowpass gain (as $f \to 0$) = $-\frac{R4}{R1}$

Circuit dynamics: $\frac{R2}{R4} = \frac{H_{OHP}}{H_{OLP}}$; $H_{OBP} = \sqrt{H_{OHP} \times H_{OLP}} \times Q$

$H_{OLP\,(peak)} \cong Q \times H_{OLP}$ (for high Q's)

$H_{OHP\,(peak)} \cong Q \times H_{OHP}$ (for high Q's)

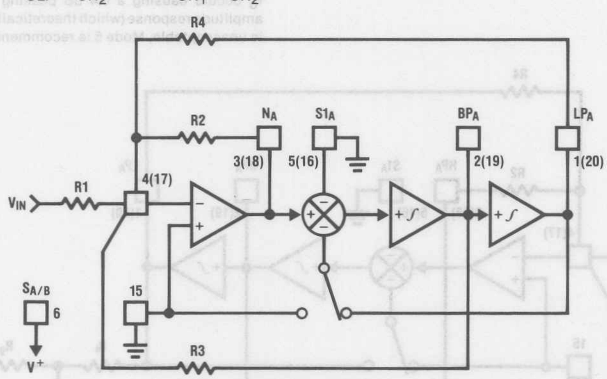
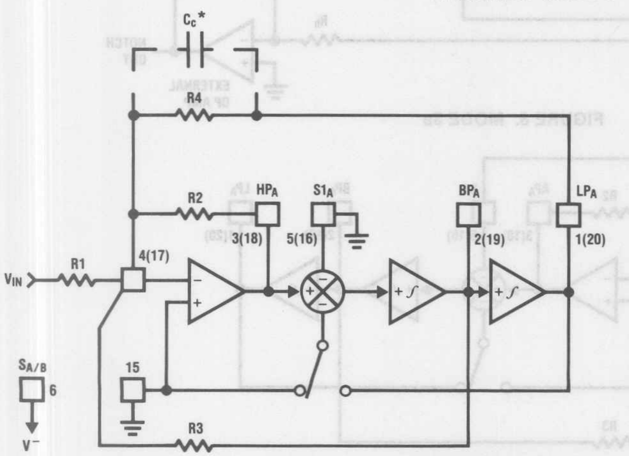


FIGURE 6. MODE 2



*In Mode 3, the feedback loop is closed around the input summing amplifier; the finite GBW product of this op amp causes a slight Q enhancement. If this is a problem, connect a small capacitor (10 pF–100 pF) across R4 to provide some phase lead.

FIGURE 7. MODE 3

$$f_o = \frac{f_{CLK}}{100} \times \sqrt{\frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50} \times \sqrt{\frac{R2}{R4}}$$

$$Q = \sqrt{\frac{R2}{R4}} \times \frac{R3}{R2}$$

$$H_{OHP} = -\frac{R2}{R1}$$

$$H_{OBP} = -\frac{R3}{R1}$$

$$H_{OLP} = -\frac{R4}{R1}$$

$$f_n = \text{notch frequency} = \frac{f_{CLK}}{100}\sqrt{\frac{R_h}{R_l}} \text{ or } \frac{f_{CLK}}{50}\sqrt{\frac{R_h}{R_l}}$$

$$H_{on} = \text{gain of notch at } f = f_o = \left\|Q\left(\frac{R_g}{R_l}H_{OLP} - \frac{R_g}{R_h}H_{OHP}\right)\right\|$$

$$H_{n1} = \text{gain of notch (as } f \to 0) = \frac{R_g}{R_l} \times H_{OLP}$$

$$H_{n2} = \text{gain of notch}\left(\text{as } f \to \frac{f_{CLK}}{2}\right) = -\frac{R_g}{R_h} \times H_{OHP}$$

$$= \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50},$$

f_z^* = center frequency of the complex zero pair $\simeq f_o$

$$Q = \frac{f_o}{BW} = \frac{R3}{R2},$$

Q_z = quality factor of complex zero pair $= \frac{R3}{R1}$

For AP output make R1 = R2

$$H_{OAP} = \text{Allpass gain}\left(\text{at } 0 < f < \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1} = -1$$

$$H_{OLP} = \text{Lowpass gain (as } f \to 0)$$
$$= -\left(\frac{R2}{R1} + 1\right) = -2$$

$$H_{OBP} = \text{Bandpass gain (at } f = f_o)$$
$$= -\frac{R3}{R2}\left(1 + \frac{R2}{R1}\right) = -2\left(\frac{R3}{R2}\right)$$

Circuit dynamics: $H_{OBP} = (H_{OLP}) \times Q = (H_{OAP} + 1)\,Q$

*Due to the sampled data nature of the filter, a slight mismatch of f_z and f_o occurs causing a 0.4 dB peaking around f_o of the allpass filter amplitude response (which theoretically should be a straight line). If this is unacceptable, Mode 5 is recommended.

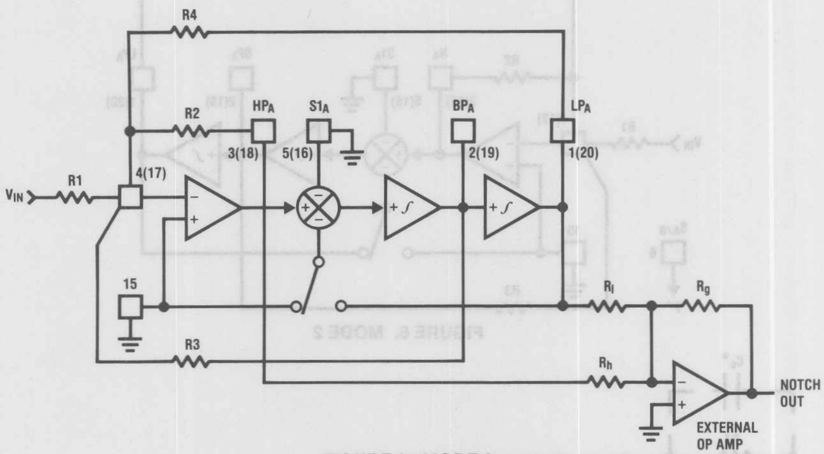


FIGURE 8. MODE 3a

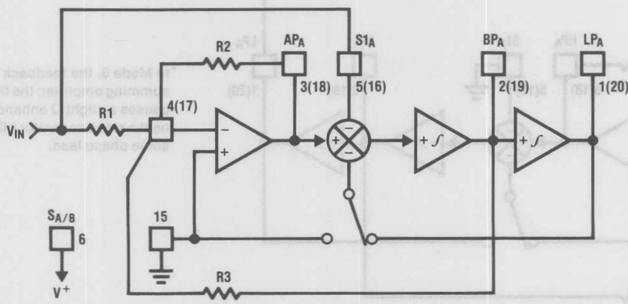


FIGURE 9. MODE 4

Modes of Operation (Continued)

MODE 5: Numerator Complex Zeros, BP, LP (See *Figure 10*)

$$f_o = \sqrt{1+\frac{R2}{R4}} \times \frac{f_{CLK}}{100} \text{ or } \sqrt{1+\frac{R2}{R4}} \times \frac{f_{CLK}}{50}$$

$$f_z = \sqrt{1-\frac{R1}{R4}} \times \frac{f_{CLK}}{100} \text{ or } \sqrt{1-\frac{R1}{R4}} \times \frac{f_{CLK}}{50}$$

$$Q = \sqrt{1+R2/R4} \times \frac{R3}{R2}$$

$$Q_z = \sqrt{1-R1/R4} \times \frac{R3}{R1}$$

$$H_{0_{z1}} = \text{gain at C.z output (as f} \rightarrow 0 \text{ Hz)} = \frac{R2\,(R4-R1)}{R1\,(R2+R4)}$$

$$H_{0_{z2}} = \text{gain at C.z output} \left(\text{as } f \rightarrow \frac{f_{CLK}}{2}\right) = \frac{R2}{R1}$$

$$H_{OBP} = \left(\frac{R2}{R1}+1\right) \times \frac{R3}{R2}$$

$$H_{OLP} = \left(\frac{R2+R1}{R2+R4}\right) \times \frac{R4}{R1}$$

MODE 6a: Single Pole, HP, LP Filter (See *Figure 11*)

f_c = cutoff frequency of LP or HP output

$$= \frac{R2}{R3}\frac{f_{CLK}}{100} \text{ or } \frac{R2}{R3}\frac{f_{CLK}}{50}$$

$$H_{OLP} = -\frac{R3}{R1}$$

$$H_{OHP} = -\frac{R2}{R1}$$

MODE 6b: Single Pole LP Filter (Inverting and Non-Inverting) (See *Figure 12*)

f_c = cutoff frequency of LP outputs

$$\cong \frac{R2}{R3}\frac{f_{CLK}}{100} \text{ or } \frac{R2}{R3}\frac{f_{CLK}}{50}$$

H_{OLP_1} = 1 (non-inverting)

$$H_{OLP_2} = -\frac{R3}{R2}$$

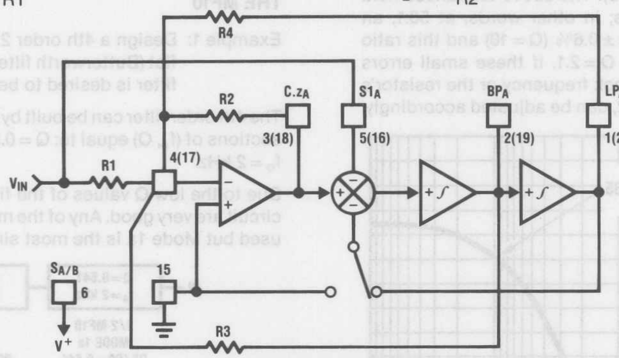


FIGURE 10. MODE 5

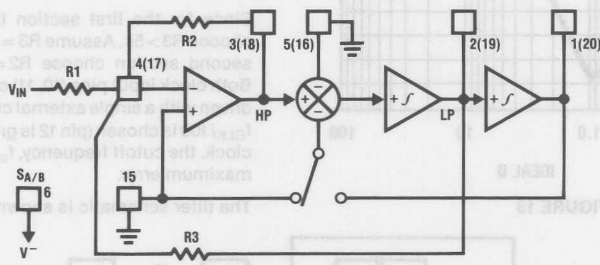


FIGURE 11. MODE 6a

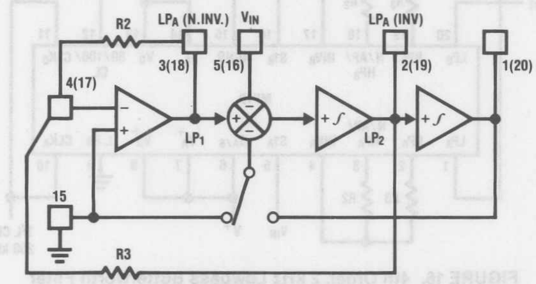


FIGURE 12. MODE 6b

Applications Information

HOW TO USE THE f_{CLK}/f_o RATIO SPECIFICATION

The MF10 is a switched capacitor filter designed to approximate the response of a 2nd order state variable filter. When the sampling frequency is much larger than the frequency band of interest, the sampled data filter is a good approximation to its continuous time equivalent. In the case of the MF10, this ratio is about 50:1 or 100:1. Nevertheless the filter's response must be examined in the z-domain in order to obtain the actual response. It can be shown that the clock frequency to center frequency ratio, f_{CLK}/f_o and the quality factor, Q, deviate from their ideal values determined in the continuous time domain. These deviations are shown graphically in *Figures 13 and 14*. The ratio, f_{CLK}/f_o, is a function of the ideal Q and the largest errors occur for the lowest values of Q.

The curve for the f_{CLK}/f_o ratio versus the ideal Q has been normalized for a Q of 10 which is the Q value used for the f_{CLK}/f_o ratio testing of the MF10. At this point the f_{CLK}/f_o ratio is 49.94 in the 50:1 mode and 99.35 in the 100:1 mode. These values are within a maximum tolerance of $\pm 0.6\%$ (MF10B) and $\pm 1.5\%$ (MF10C). The above tolerances hold for the entire range of Q's; in other words, at 50:1, an MF10B has a ratio of $49.94 \pm 0.6\%$ ($Q = 10$) and this ratio becomes ($49.44 \pm 0.6\%$) at $Q = 2.1$. If these small errors cannot be tolerated, the clock frequency or the resistor's ratio, in Mode 3 and Mode 2, can be adjusted accordingly.

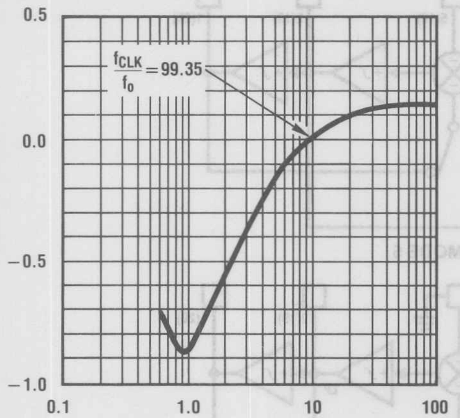


FIGURE 13

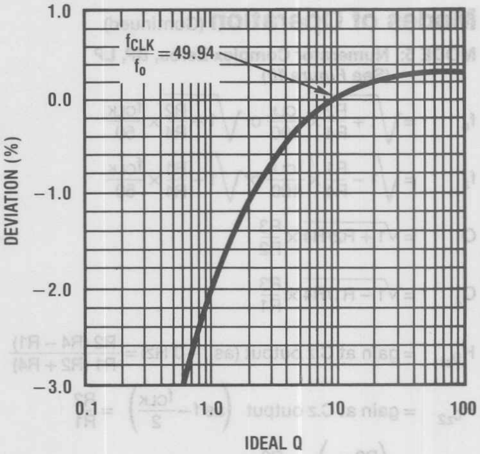


FIGURE 14

A SIMPLE AND INFORMATIVE FILTER DESIGN USING THE MF10

Example 1: Design a 4th order 2 kHz lowpass maximally flat (Butterworth filter). The overall gain of the filter is desired to be equal to 1V/V.

The 4th order filter can be built by cascading two 2nd order sections of (f_o, Q) equal to: $Q = 0.541$, $f_o = 2$ kHz, $Q = 1.306$, $f_o = 2$ kHz.

Due to the low Q values of the filter, the dynamics of the circuit are very good. Any of the modes of operation can be used but Mode 1a is the most simple:

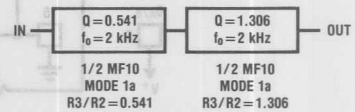


FIGURE 15

Since for the first section the smallest resistor is R3, choose R3 > 5k. Assume R3 = 10k then R2 = 18.48k. For the second section choose R2 = 10k and then R3 = 13.06k. Both clock input pins (10, 11) can be tied together and then driven with a single external clock. If the approximate ratio $f_{CLK}/100$ is chosen (pin 12 is grounded), then with a 200 kHz clock, the cutoff frequency, f_c, will be at 2 kHz with a 1.5% maximum error.

The filter schematic is shown in *Figure 16*.

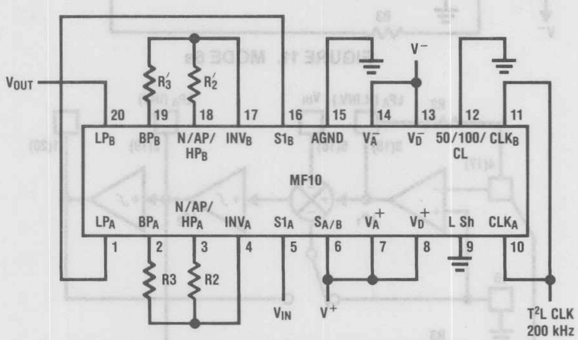


FIGURE 16. 4th Order, 2 kHz Lowpass Butterworth Filter

Applications Information (Continued)

With a ±5V supply, each output node of the IC (pins 1, 2, 3, 18, 19, 20) will swing to ±3.8V (MF10B) or ±3.2V (MF10C). The maximum gain of 1.306 occurs at pin 19 at $f_o \simeq 2$ kHz. The input voltage amplitude should be limited to less than 7.6 Vp-p/1.306 = 5.8 Vp-p. If the Q of 1.306 section of the MF10 precedes the Q of 0.541 section, the maximum gain is at pin 1. This gain can be calculated from the expression for H_{OP} given in Definition of Terms, and equals 1.41.

Getting Optimum Cutoff Frequency, f_c, Accuracy (if needed):

In the previous example, an approximate 100:1 ratio was assumed. The true f_{CLK}/f_o ratio should be read from the curves, *Figures 13 and 14.* At 100:1 the normalized ratio to Q = 10 is: $f_{CLK}/f_o = 99.35$. For Q's of 0.541 and 1.306 this ratio becomes 99.35 − 0.75% = 98.6. For a 2 kHz f_c, the clock frequency should be 2 kHz × 98.6 = 197.2 kHz.

With an MF10B and a 197.2 kHz clock, the maximum error on the 2 kHz cutoff frequency is ±0.6% as indicated in the specs.

If only a 200 kHz is available in Mode 1a, the true value of f_c and its maximum error is: 200 kHz/(98.6 ± 0.6%) = 2028 ∓ 0.6%.

If only a 200 kHz is available and there is need for a tight tolerance cutoff frequency, then Mode 3 should be used instead of Mode 1a. The resistor ratios are:

1st Section, Q = 0.541	2nd Section, Q = 1.306
R2/R4 = 0.972	R2/R4 = 0.972
R3/R2 = 0.548	R3/R2 = 1.324
R4/R1 = 1	R4/R1 = 1

MF10 OFFSETS

The switched capacitor integrators of the MF10 have higher equivalent input offset than the typical R,C integrator of a discrete active filter. These offsets are created by a parasitic charge injection from the switches into the integrating capacitors; they are temperature and clock frequency independent and their sign is shown to be consistent from part to part. The input offsets of the CMOS op amps also add to the overall offset, but their contribution is very small. *Figure 17* shows an equivalent circuit from where output DC offsets can be calculated.

V_{OS1} = 0 mV to ±10 mV

V_{OS2} = charge injected offset plus op amp offset $\simeq$ −120 mV to −170 mV (at 50:1)

V_{OS3} = charge injected offset plus op amp offset $\simeq$ 100 mV to 150 mV (at 50:1)

The V_{OS2} and V_{OS3} numbers approximately double at 100:1.

Output Offsets

The DC offset at the BP output(s) of the MF10 is equal to the input offset of the lowpass switched capacitor integrator, V_{OS3}.

The DC offsets at the remaining outputs are roughly dependent upon the mode of operation and resistor ratios.

Mode 1 and Mode 4

$$V_{OS(N)} = V_{OS1}\left(\frac{1}{Q} + 1 + \left\|H_{OLP}\right\|\right) - \frac{V_{OS3}}{Q}$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N)} - V_{OS2}$$

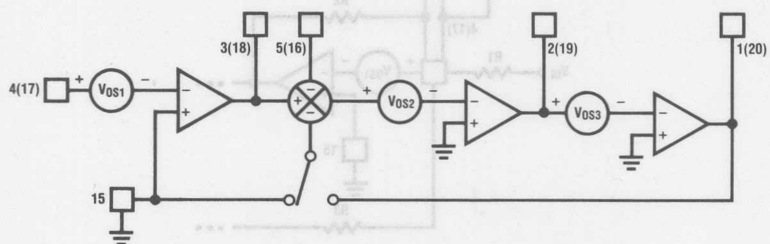


FIGURE 17

$$V_{OS(N)} = \left(\frac{R2}{R_P}+1\right) V_{OS1} \times \frac{1}{1+R2/R4} + V_{OS2}\frac{1}{1+R4/R2} - \frac{V_{OS3}}{Q\sqrt{1+R2/R4}};$$

$$R_P = R1//R2//R4$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N)} - V_{OS2}$$

Mode 3

$$V_{OS(HP)} = V_{OS2}$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = -\frac{R4}{R2}\left(\frac{R2}{R3}V_{OS3}+V_{OS2}\right) + \frac{R4}{R2}\left(1+\frac{R2}{R_P}\right)V_{OS1};\ R_P = R1//R3//R4$$

Mode 1a

$$V_{OS}(N.INV.BP) = \left(1+\frac{1}{Q}\right)V_{OS1} - \frac{V_{OS3}}{Q}$$

$$V_{OS}(INV.BP) = V_{OS3}$$

$$V_{OS}(LP) = V_{OS}(N.INV.BP) - V_{OS2}$$

bothersome unless large input voltage signals are applied to the filter. For instance, if the BP output is used and it is AC coupled, the remaining two outputs should not be allowed to saturate. If so, gain nonlinearities and f_o, Q errors will occur. For Mode 3 of operation a word of caution is necessary: by allowing small R2/R4 ratios and high Q, the LP output will exhibit a couple of volts of DC offset and an offset adjustment should be made.

An extreme example: Design a 1.76 kHz BP filter with a Q of 21 and a gain equal to unity. The MF10 will be driven with a 250 kHz clock, and it will be switched 50:1.

$$\text{Resistor values: } \sqrt{\frac{R2}{R4}} = \frac{f_o}{f_{CLK}} \times 50 = 0.352;\ \frac{R2}{R4} = 0.124$$

$$\frac{R3}{R2} = 21 \times \frac{1}{0.352} = 59.63;\quad \frac{R3}{R1} = 1$$

Since R3/R2 is the highest resistor ratio, start with R2 = 10k, then R3 ≃ 600k, R1 ≅ 600k, R4 = 80k. Assuming $V_{OS1} = 2$ mV, $V_{OS2} = -150$ mV, $V_{OS3} = 150$ mV, the DC offset at the LP output is $V_{OS(LP)} = +1.2$V. The offset adjustment will be done by injecting a small amount of current into the inverting input of the first op amp, *Figure 18*. This will change the effective V_{OS1}, but the output DC offset of the HP and BP will remain unchanged.

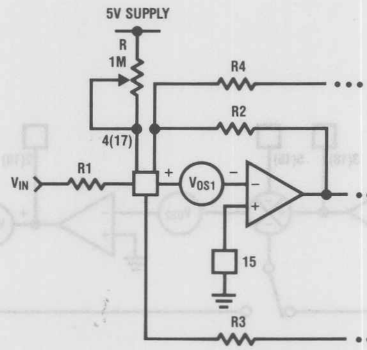


FIGURE 18. V_{OS} Adjust Scheme

National Semiconductor

TP5116A, TP5117A, TP5156A Monolithic CODECs

General Description

The TP5116A, TP5117A and TP5156A are monolithic PCM CODECs implemented with double-poly CMOS technology. The TP5116A and TP5117A are intended for μ-law applications and the TP5156A is for A-law applications. The TP5117A has a D3 compatible format for line card compatibility with the TP5156A.

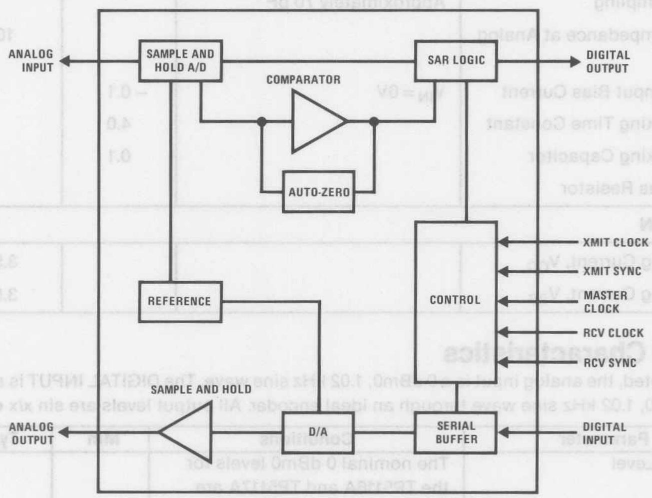
Each device contains separate D/A and A/D circuitry, all necessary sample and hold capacitors, and internal auto-zero circuits. Each device also contains a precision internal voltage reference, eliminating the need for an external reference. There are no internal connections to pins 15 or 16, making them directly interchangeable with CODECs using external reference components.

All devices are intended to be used with the TP3040 monolithic PCM filter which provides the input anti-aliasing function for the encoder and smooths the output of the decoder and corrects for the sin x/x distortion introduced by the decoder sample and hold output.

Features

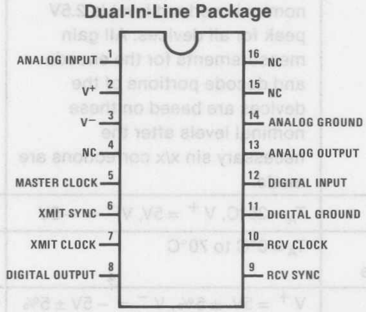
- Low operation power — 50 mW typical
- ± 5V operation
- TTL compatible digital interface
- Internal precision reference on TP5116A, TP5117A and TP5156A
- Internal sample and hold capacitors
- Internal auto-zero circuit
- TP5116A—μ-law coding (sign plus magnitude format)
- TP5117A—μ-law, D3 compatible format
- TP5156A—A-law coding
- Synchronous or asynchronous operation

Simplified Block Diagram



Connection Diagram

Dual-In-Line Package



TOP VIEW

Absolute Maximum Ratings

Operating Temperature	$-25°C$ to $+125°C$
Storage Temperature	$-65°C$ to $+150°C$
V^+ with Respect to DIGITAL GROUND	7V
V^+ with Respect to V^-	14V
V^- with Respect to DIGITAL GROUND	$-7V$
Voltage at Any Input or Output	$V^- -0.3V$ to $V^+ +0.3V$

DC Electrical Characteristics

Unless otherwise noted $T_A = 0°C$ to $70°C$, $V^+ = 5.0V \pm 5\%$, $V^- = -5.0V \pm 5\%$. Typical characteristics are specified at $V^+ = 5.0V$, $V^- = -5.0V$ and $T_A = 25°C$. All digital signals are referenced to DIGITAL GROUND. All analog signals are referenced to ANALOG GROUND.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL INTERFACE						
I_I	Input Current	$0V < V_{IN} < V^+$	-10		10	μA
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		2.2			V
V_{OL}	Output Low Voltage	$I_{OL} = 3.2$ mA			0.4	V
V_{OH}	Output High Voltage	$I_{OH} = 6$ mA	2.4			V
ANALOG INTERFACE						
Z_I	Analog Input Impedance when Sampling	Resistance in Series with Approximately 70 pF	2			kΩ
Z_O	Output Impedance at Analog Output			10	20	Ω
I_{IN}	Analog Input Bias Current	$V_{IN} = 0V$	-0.1		0.1	μA
$R1 \times C1$	DC Blocking Time Constant		4.0			ms
C1	DC Blocking Capacitor		0.1			μF
R1	Input Bias Resistor				50	kΩ
POWER DISSIPATION						
I_{CC1}	Operating Current, V_{CC}			3.5	7.0	mA
I_{BB1}	Operating Current, V_{BB}			3.5	7.0	mA

AC Electrical Characteristics

Unless otherwise noted, the analog input is a 0 dBm0, 1.02 kHz sine wave. The DIGITAL INPUT is a PCM bit stream generated by passing a 0 dBm0, 1.02 kHz sine wave through an ideal encoder. All output levels are sin x/x corrected.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Absolute Level	The nominal 0 dBm0 levels for the TP5116A and TP5117A are 1.227 Vrms and 1.231 Vrms for the TP5156A. The resulting nominal overload level is 2.5V peak for all devices. All gain measurements for the encode and decode portions of the devices are based on these nominal levels after the necessary sin x/x corrections are made.				
G_{RA}	Receive Gain, Absolute	$T_A = 25°C$, $V^+ = 5V$, $V^- = -5V$	-0.1		0.1	dB
G_{RAT}	Absolute Receive Gain Variation with Temperature	$T_A = 0°C$ to $70°C$	-0.05		0.05	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	$V^+ = 5V \pm 5\%$, $V^- = -5V \pm 5\%$	-0.07		0.07	dB

AC Electrical Characteristics (Continued)

Unless otherwise noted, the analog input is a 0 dBm0, 1.02 kHz sine wave. The DIGITAL INPUT is a PCM bit stream generated by passing a 0 dBm0, 1.02 kHz sine wave through an ideal encoder. All output levels are sin x/x corrected.

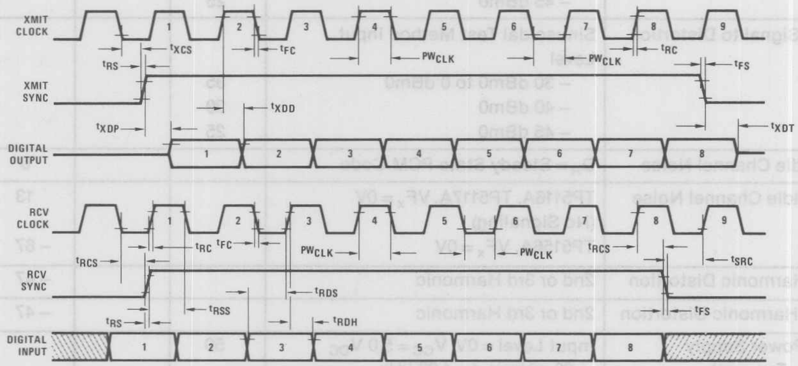
Symbol	Parameter	Conditions	Min	Typ	Max	Units
G_{XA}	Transmit Gain, Absolute	$T_A = 25°C$, $V^+ = 5V$, $V^- = -5V$	−0.1		0.1	dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature	$T_A = 0°C$ to 70°C	−0.05		0.05	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	$V^+ = 5V \pm 5\%$, $V^- = -5V \pm 5\%$	−0.07		0.07	dB
G_{RAL}	Absolute Receive Gain Variation with Level	CCITT Method 2 Relative to −10 dBm0 0 dBm0 to 3 dBm0 −40 dBm0 to 0 dBm0 −50 dBm0 to −40 dBm0 −55 dBm0 to −50 dBm0	 −0.3 −0.2 −0.4 −1.0		 0.3 0.2 0.4 1.0	 dB dB dB dB
G_{XAL}	Absolute Transmit Gain Variation with Level	CCITT Method 2 Relative to −10 dBm0 0 dBm0 to 3 dBm0 −40 dBm0 to 0 dBm0 −50 dBm0 to −40 dBm0 −55 dBm0 to −50 dBm0	 −0.3 −0.2 −0.4 −1.0		 0.3 0.2 0.4 1.0	 dB dB dB dB
S/D_R	Receive Signal to Distortion Ratio	Sinusoidal Test Method Input Level −30 dBm0 to 0 dBm0 −40 dBm0 −45 dBm0	 35 29 25			 dBc dBc dBc
S/D_X	Transmit Signal to Distortion Ratio	Sinusoidal Test Method Input Level −30 dBm0 to 0 dBm0 −40 dBm0 −45 dBm0	 35 29 25			 dBc dBc dBc
N_R	Receive Idle Channel Noise	D_R = Steady State PCM Code			0	dBrnc0
N_X	Transmit Idle Channel Noise	TP5116A, TP5117A, $VF_x = 0V$ (No Signaling) TP5156A, $VF_x = 0V$			13 −67	dBrnc0 dBm0p
HD_R	Receive Harmonic Distortion	2nd or 3rd Harmonic			−47	dB
HD_X	Transmit Harmonic Distortion	2nd or 3rd Harmonic			−47	dB
$PPSR_X$	Positive Power Supply Rejection, Transmit	Input Level = 0V, $V_{CC} = 5.0\ V_{DC}$ + 20 mVrms, f = 1.02 kHz	50			dB
$PPSR_R$	Positive Power Supply Rejection, Receive	D_R = Steady PCM Code, $V_{CC} = 5.0\ V_{DC}$ + 20 mVrms, f = 1.02 kHz	40			dB
$NPSR_X$	Negative Power Supply Rejection, Transmit	Input Level = 0V, $V_{BB} = -5.0\ V_{DC}$ + 20 mVrms, f = 1.02 kHz	50			dB
$NPSR_R$	Negative Power Supply Rejection, Receive	D_R = Steady PCM Code, $V_{BB} = -5.0\ V_{DC}$ + 20 mVrms, f = 1.02 kHz	45			dB
CT_{XR}	Transmit to Receive Crosstalk	D_R = Steady PCM Code			−75	dB
CT_{RX}	Receive to Transmit Crosstalk	Transmit Input Level = 0V			−70	dB

F_M	MASTER CLOCK Frequency		1.5	2.048	2.1	MHz
F_X, F_R	XMIT, RCV CLOCK Frequency		0.064	2.048	2.1	MHz
PW_{CLK}	Clock Pulse Width	MASTER, XMIT, RCV CLOCKS	150			ns
t_{RC}, t_{FC}	Clock Rise and Fall Time	MASTER, XMIT, RCV CLOCKS			50	ns
t_{RS}, t_{FS}	Sync Pulse Rise and Fall Time	RCV, XMIT SYNC			50	ns
t_{RCS}, t_{XCS}	Clock to Sync Delay	RCV, XMIT	0			ns
t_{XSS}	XMIT SYNC Set-Up Time				150	ns
t_{XDD}	XMIT Data Delay	Load = 100 pF + 2 LSTTL Loads			200	ns
t_{XDP}	XMIT Data Present	Load = 100 pF + 2 LSTTL Loads			200	ns
t_{XDT}	XMIT Data TRI-STATE®				150	ns
t_{SRC}	RCV CLOCK to RCV SYNC Delay		0			ns
t_{RDS}	RCV Data Set-Up Time		0			ns
t_{RSS}	RCV SYNC Set-Up Time				150	ns
t_{RDH}	RCV Data Hold Time		100			ns
t_{XSL}	XMIT SYNC Low Time	64 kHz Operation	300			ns
t_{RSL}	RCV SYNC Low Time	64 kHz Operation	17			(Note 1)

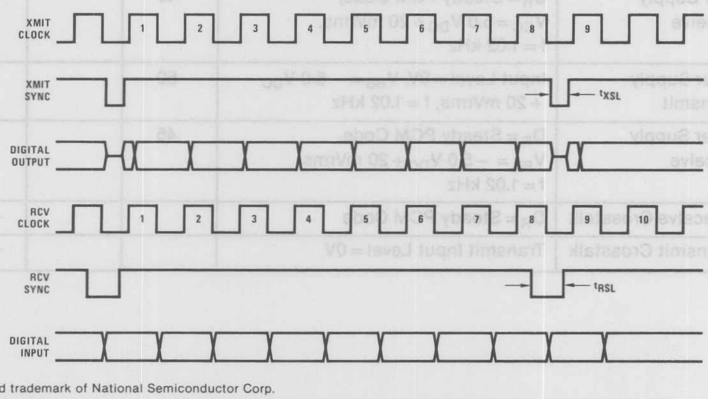
Note 1: RCV SYNC must remain low for 17 cycles of MASTER CLOCK.

Timing Waveforms

72 kHz or Greater Operation



64 kHz Operation



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Description of Pin Functions

Pin No.	Name	Function
1	ANALOG INPUT	ANALOG INPUT to the encoder. This signal will be sampled at the end of the encoder time slot and the resulting PCM code will be shifted out during the subsequent encode time slot.
2	V+	5V (±5%) input.
3	V−	−5V (±5%) input.
4	NC	Unused.
5	MASTER CLOCK	MASTER CLOCK input used to operate the internal encode and decode sequencers. Should be 1.536 MHz, 1.544 MHz or 2.048 MHz.
6	XMIT SYNC	Encoder frame sync pulse. Normally occurring at an 8 kHz rate, this pulse is nominally eight XMIT CLOCK cycles wide.
7	XMIT CLOCK	Transmit bit clock input used to shift out the PCM data on DIGITAL OUTPUT. May operate from 64 kHz to 2.048 MHz. May be asynchronous with RCV CLOCK.
8	DIGITAL OUTPUT	Serial PCM TRI-STATE® output from encoder. During the encoder time slot, the PCM code for the previous sample of ANALOG INPUT is shifted out, most significant bit first, on the rising edge of XMIT CLOCK.

Description of Pin Functions (Continued)

Pin No.	Name	Function
9	RCV SYNC	Decoder frame sync pulse. Normally occurring at an 8 kHz rate, this pulse is nominally eight RCV CLOCK cycles wide.
10	RCV CLOCK	Receive bit clock input used to shift in the PCM data on DIGITAL INPUT. May operate from 64 kHz to 2048 MHz. May be asynchronous with XMIT CLOCK.
11	DIGITAL GROUND	All digital levels referenced to the DIGITAL GROUND pin.
12	DIGITAL INPUT	Serial PCM data input to the decoder. During the decoder time slot, PCM data is shifted into DIGITAL INPUT, most significant bit first, on the rising edge of RCV CLOCK.
13	ANALOG OUTPUT	ANALOG OUTPUT from the decoder. The decoder sample and hold amplifier is updated approximately 15 μs after the end of the decode time slot.
14	ANALOG GROUND	All analog signals are referenced to the ANALOG GROUND pin.
15	NC	Unused.
16	NC	Unused.

Functional Description

Approximately 4 μs after the rising edge of the XMIT SYNC pulse, the voltage present on the ANALOG INPUT is sampled and the process of encoding that sample into a PCM code is begun. Simultaneously, the 8-bit PCM code corresponding to the previous sample is shifted out of the DIGITAL OUTPUT, MSB first, on the rising edge of the next eight cycles of the XMIT CLOCK. When XMIT SYNC (which is normally eight XMIT CLOCK cycles long) goes low, the TRI-STATE® DIGITAL OUTPUT is returned to the high impedance state. On the TP5116A, the PCM code is in a μ-law sign plus magnitude format. The TP5117A PCM output is the standard μ-law format wherein the magnitude bits are inverted. The TP5156A uses the standard A-law coding.

An 8-bit PCM code is shifted into DIGITAL INPUT on the rising edge of the first eight RCV CLOCK pulses after RCV SYNC goes high. RCV SYNC is nominally eight RCV CLOCK cycles wide. Approximately 15 μs after RCV SYNC goes low, the ANALOG OUTPUT is updated to the voltage corresponding to the PCM input code.

All encoding and decoding operations are run off the MASTER CLOCK. MASTER CLOCK should be in the range of 1.536 MHz to 2.048 MHz and should be synchronous with XMIT CLOCK and RCV CLOCK. The XMIT and RCV CLOCK may vary from 64 kHz to 2.048 MHz.

Encoding Delay

The encoding process begins immediately at the beginning of the encode time slot and is concluded no later than 18 time slots later. In normal applications, the PCM data is not shifted out until the next time slot 125 μs later, resulting in an encoding delay of 125 μs. In some applications it is possible to operate the CODEC at a higher frame rate to reduce this delay. With a 2.048 MHz MASTER CLOCK, the FS rate could be increased to 15 kHz, reducing the delay from 125 μs to 67 μs.

Functional Description (Continued)

Decoding Delay

The decoding process begins immediately after the end of the decoder time slot. The output of the decoder sample and hold amplifier is updated 28 MASTER CLOCK cycles later. The decoding delay is therefore approximately 28 clock cycles plus one half of a frame time or, 81 μs for a 1.544 MHz system with an 8 kHz frame rate or, 76 μs for a 2.048 MHz system with an 8 kHz frame rate. Again, for some applications the frame rate could be increased to reduce this delay.

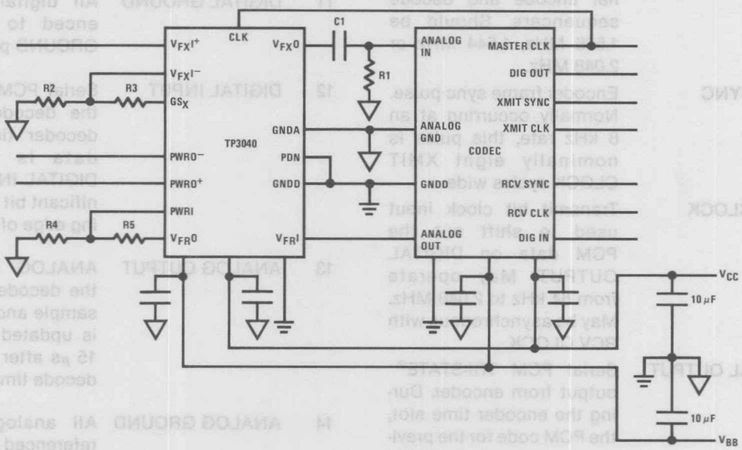
Typical Application

A typical application of these CODECs used in conjunction with the TP3040 PCM filter is shown below. The values of resistor R1 and DC blocking capacitor C1, are noncritical. The capacitor value should exceed 0.1 μF, R1 should be less than 50 kΩ, and the product R1 $\times$ C1 should exceed 4 ms.

$$\text{XMIT GAIN} = 20 \times \log\left(\frac{R3 + R2}{R2}\right) + 3\,\text{dB}$$

$$\text{RCV GAIN} = 20 \times \log\left(\frac{R4}{R4 + R5}\right)$$

The power supply decoupling capacitors should be 0.1 μF. In order to take advantage of the excellent noise performance of these CODECs, care must be taken in board layout to prevent coupling of digital noise into the sensitive analog lines. For card insertion into a hot connector, care should be taken to insure that GNDA and GNDD are contacted prior to V_{CC} and V_{BB}.



National Semiconductor

TP3020/TP3021 Monolithic CODECs

General Description

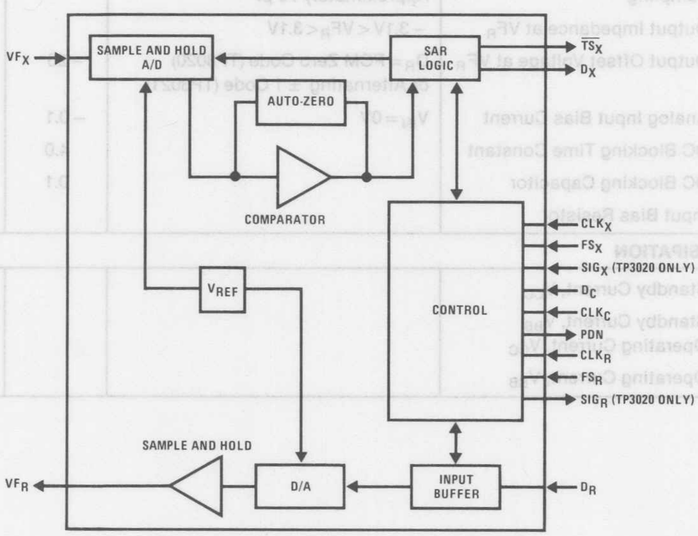
The TP3020 and TP3021 are monolithic PCM CODECs implemented with double-poly CMOS technology. The TP3020 is intended for μ-law applications and contains logic for μ-law signaling insertion and extraction. The TP3021 is intended for A-law applications.

Each device contains separate D/A and A/D circuitry, all necessary sample and hold capacitors, a precision voltage reference and internal auto-zero circuit. A serial control port allows an external controller to individually assign the PCM input and output ports to one of up to 32 time slots or to place the CODEC into a power-down mode. Alternately, the TP3020/TP3021 may be operated in a fixed time slot mode. Both devices are intended to be used with the TP3040 monolithic PCM filter which provides the input anti-aliasing function for the encoder and smoothes the output of the decoder and corrects for the sin x/x distortion introduced by the decoder sample and hold output.

Features

- Low operation power—45 mW typical
- Low standby power—1 mW typical
- ±5V operation
- TTL compatible digital interface
- Time slot assignment or alternate fixed time slot modes
- Internal precision reference
- Internal sample and hold capacitors
- Internal auto-zero circuit
- TP3020—μ-law coding with signaling capabilities
- TP3021—A-law coding
- Synchronous or asynchronous operation

Simplified Block Diagram



V_{CC} with Respect to GNDD	7V
V_{CC} with Respect to V_{BB}	14V
V_{BB} with Respect to GNDD	−7V
Voltage at Any Input or Output	$V_{BB}-0.3V$ to $V_{CC}+0.3V$
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Unless otherwise noted $T_A=0°C$ to $70°C$, $V_{CC}=5.0V \pm 5\%$, $V_{BB}=-5.0V \pm 5\%$. Typical characteristics are specified at $V_{CC}=5.0V$, $V_{BB}=-5.0V$ and $T_A=25°C$. All digital signals are referenced to GNDD. All analog signals are referenced to GNDA.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL INTERFACE						
I_I	Input Current	$0<V_{IN}<V_{CC}$	−10		10	μA
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		2.2			V
V_{OL}	Output Low Voltage	D_X, $I_{OL}=4.0$ mA			0.4	V
		SIG_R, $I_{OL}=0.5$ mA			0.4	V
		$\overline{TS}_X$, $I_{OL}=3.2$ mA, Open Drain			0.4	V
		PDN, $I_{OL}=1.6$ mA			0.4	V
V_{OH}	Output High Voltage	D_X, $I_{OH}=6$ mA	2.4			V
		SIG_R, $I_{OH}=0.6$ mA	2.4			V
ANALOG INTERFACE						
Z_I	VF_X Input Impedance when Sampling	Resistance in Series with Approximately 70 pF	2.0			kΩ
Z_O	Output Impedance at VF_R	$-3.1V<VF_R<3.1V$		10	20	Ω
V_{OS}	Output Offset Voltage at VF_R	$D_R=$ PCM Zero Code (TP3020) or Alternating ±1 Code (TP3021)	−25		25	mV
I_{IN}	Analog Input Bias Current	$V_{IN}=0V$	−0.1		0.1	μA
R1 × C1	DC Blocking Time Constant		4.0			ms
C1	DC Blocking Capacitor		0.1			μF
R1	Input Bias Resistor				50	kΩ
POWER DISSIPATION						
I_{CC0}	Standby Current, V_{CC}			0.1	0.4	mA
I_{BB0}	Standby Current, V_{BB}			0.03	0.1	mA
I_{CC1}	Operating Current, V_{CC}			4.5	8.0	mA
I_{BB1}	Operating Current, V_{BB}			4.5	8.0	mA

AC Electrical Characteristics

Unless otherwise noted, the analog input is a 0 dBm0, 1.02 kHz sine wave. The digital input is a PCM bit stream generated by passing a 0 dBm0, 1.02 kHz sine wave through an ideal encoder. All output levels are sin x/x corrected.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Absolute Level	The nominal 0 dBm0 levels for the TP3020 and TP3021 are 1.520 Vrms and 1.525 Vrms respectively. The resulting nominal overload level is 3.096V peak for both devices. All gain measurements for the encode and decode portions of the TP3020/TP3021 are based on these nominal levels after the necessary sin x/x corrections are made.				
G_{RA}	Receive Gain, Absolute	T = 25°C, V_{CC} = 5V, V_{BB} = −5V	−0.1		0.1	dB
G_{RAT}	Absolute Receive Gain Variation with Temperature	T = 0°C to 70°C	−0.05		0.05	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	V_{CC} = 5V ±5%, V_{BB} = −5V ±5%	−0.07		0.07	dB
G_{XA}	Transmit Gain, Absolute	T = 25°C, V_{CC} = 5V, V_{BB} = −5V	−0.1		0.1	dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature	T = 0°C to 70°C	−0.05		0.05	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	V_{CC} = 5V ±5%, V_{BB} = −5V ±5%	−0.07		0.07	dB
G_{RAL}	Absolute Receive Gain Variation with Level	CCITT Method 2 Relative to −10 dBm0				
		0 dBm0 to 3 dBm0	−0.3		0.3	dB
		−40 dBm0 to 0 dBm0	−0.2		0.2	dB
		−50 dBm0 to −40 dBm0	−0.4		0.4	dB
		−55 dBm0 to −50 dBm0	−1.0		1.0	dB
G_{XAL}	Absolute Transmit Gain Variation with Level	CCITT Method 2 Relative to −10 dBm0				
		0 dBm0 to 3 dBm0	−0.3		0.3	dB
		−40 dBm0 to 0 dBm0	−0.2		0.2	dB
		−50 dBm0 to −40 dBm0	−0.4		0.4	dB
		−55 dBm0 to −50 dBm0	−1.0		1.0	dB
S/D_R	Receive Signal to Distortion Ratio	Sinusoidal Test Method Input Level				
		−30 dBm0 to 0 dBm0	35			dBc
		−40 dBm0	29			dBc
		−45 dBm0	25			dBc
S/D_X	Transmit Signal to Distortion Ratio	Sinusoidal Test Method Input Level				
		−30 dBm0 to 0 dBm0	35			dBc
		−40 dBm0	29			dBc
		−45 dBm0	25			dBc
N_R	Receive Idle Channel Noise	D_R = Steady State PCM Code			0	dBrnc0
N_X	Transmit Idle Channel Noise	TP3020, VF_x = 0V (No Signaling)			13	dBrnc0
		TP3021, VF_x = 0V			−67	dBm0p
HD_R	Receive Harmonic Distortion	2nd or 3rd Harmonic			−47	dB
HD_X	Transmit Harmonic Distortion	2nd or 3rd Harmonic			−47	dB

AC Electrical Characteristics

(Continued) Unless otherwise noted, the analog input is a 0 dBm0, 1.02 kHz sine wave. The digital input is a PCM bit stream generated by passing a 0 dBm0, 1.02 kHz sine wave through an ideal encoder. All output levels are sin x/x corrected.

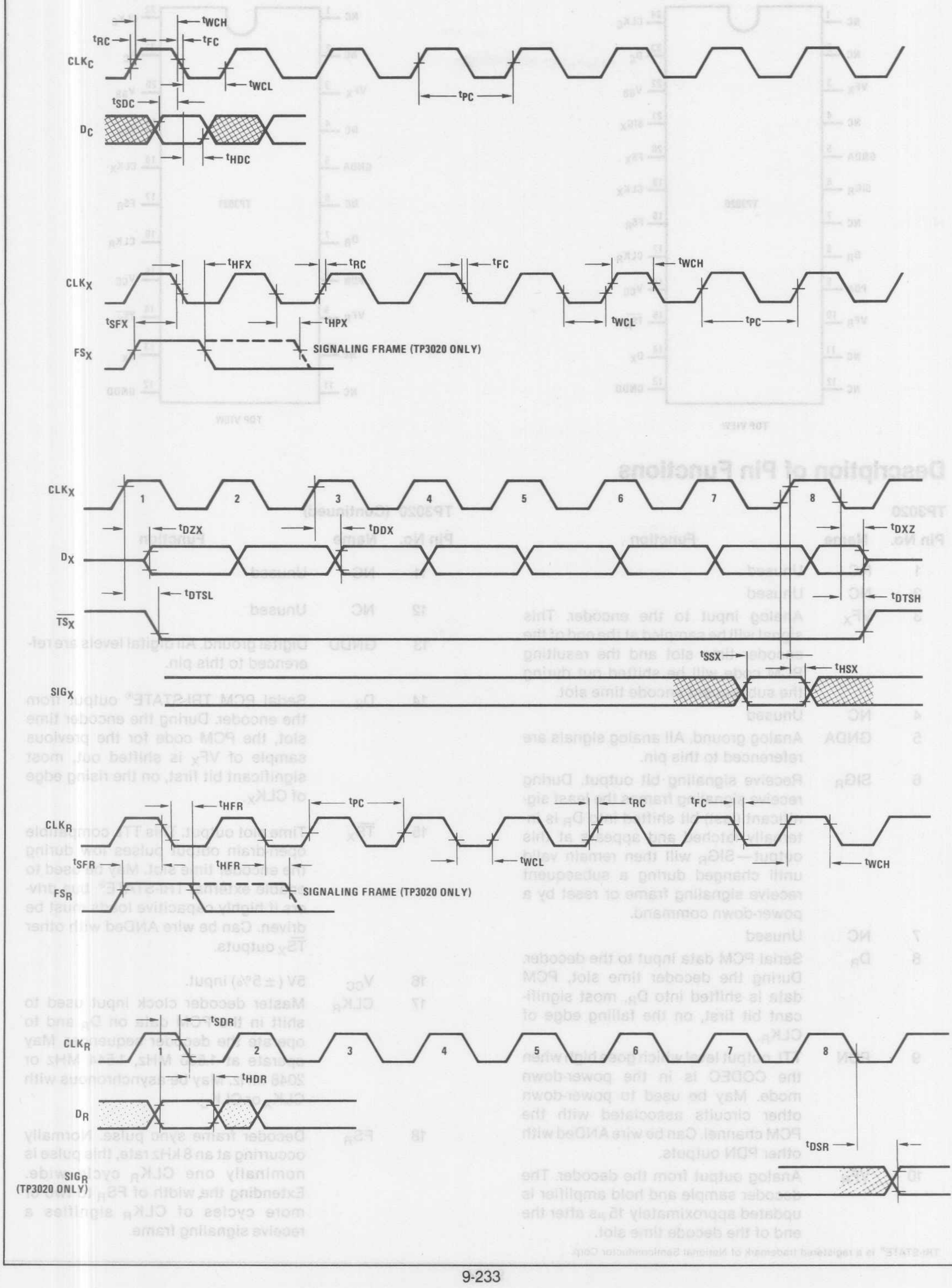
Symbol	Parameter	Conditions	Min	Typ	Max	Units
$PPSR_X$	Positive Power Supply Rejection, Transmit	Input Level = 0V, $V_{CC} = 5.0\ V_{DC}$ + 20 mVrms, f = 1.02 kHz	50			dB
$PPSR_R$	Positive Power Supply Rejection, Receive	D_R = Steady PCM Code, $V_{CC} = 5.0\ V_{DC}$ + 20 mVrms, f = 1.02 kHz	40			dB
$NPSR_X$	Negative Power Supply Rejection, Transmit	Input Level = 0V, $V_{BB} = -5.0\ V_{DC}$ + 20 mVrms, f = 1.02 kHz	50			dB
$NPSR_R$	Negative Power Supply Rejection, Receive	D_R = Steady PCM Code, $V_{BB} = -5.0\ V_{DC}$ + 20 mVrms, f = 1.02 kHz	45			dB
CT_{XR}	Transmit to Receive Crosstalk	D_R = Steady PCM Code			−75	dB
CT_{RX}	Receive to Transmit Crosstalk	Transmit Input Level = 0V			−70	dB

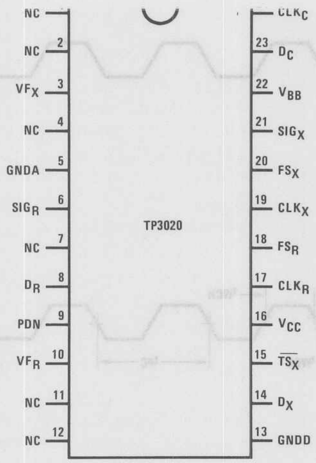
Timing Specifications

Unless otherwise noted, $T_A = 0°C$ to 70°C, $V_{CC} = 5.0 \pm 5\%$, $V_{BB} = -5.0 \pm 5\%$. All digital signals are referenced to GNDD and measured at V_{IL} and V_{IH} levels as indicated in the Timing Waveforms.

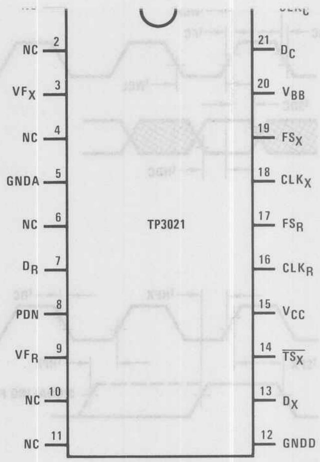
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PC}	Period of Clock	CLK_C, CLK_R, CLK_X	488			ns
t_{RC}, t_{FC}	Rise and Fall Time of Clock	CLK_C, CLK_R, CLK_X			30	ns
t_{WCH}	Width of Clock High	CLK_C, CLK_R, CLK_X	165			ns
t_{WCL}	Width of Clock Low	CLK_C, CLK_R, CLK_X	165			ns
$t_{A/D}$	A/D Conversion Time	From End of Encoder Time Slot to Completion of Conversion			16	Time Slots
$t_{D/A}$	D/A Conversion Time	From End of Decoder Time Slot to Transition of VF_R			2	Time Slots
t_{SDC}	Set-Up Time, D_C to CLK_C		100			ns
t_{HDC}	Hold Time, CLK_C to DC		100			ns
t_{SFC}	Set-Up Time, FS_X or CLK_X		100			ns
t_{HFX}	Hold Time, CLK_X to FS_X		100			ns
t_{DZX}	Delay Time to Enable D_X on TS Entry	$C_L = 150$ pF			125	ns
t_{DDX}	Delay Time, CLK_X to D_X	$C_L = 150$ pF			125	ns
t_{DXZ}	Delay Time, D_X to High Impedance State on TS Exit	$C_L = 0$ pF	50		165	ns
t_{DTSL}	Delay to $\overline{TS}_X$ Low	$0 \le C_L \le 150$ pF	30		185	ns
t_{DTSH}	Delay to $\overline{TS}_X$ Off	$C_L = 0$ pF	30		185	ns
t_{SSX}	Set-Up Time, SIG_X to CLK_X		100			ns
t_{HSX}	Hold Time, CLK_X to SIG_X		100			ns
t_{SFR}	Set-Up Time, FS_R to CLK_R		100			ns
t_{HFR}	Hold Time, CLK_R to FS_R		100			ns
t_{SDR}	Set-Up Time, D_R to CLK_R		40			ns
t_{HDR}	Hold Time, CLK_R to D_R		30			ns
t_{DSR}	Delay Time, CLK_R to SIG_R	$C_L = 100$ pF			300	ns

Timing Waveforms





TOP VIEW



TOP VIEW

Description of Pin Functions

TP3020

Pin No.	Name	Function
1	NC	Unused
2	NC	Unused
3	VF_X	Analog input to the encoder. This signal will be sampled at the end of the encoder time slot and the resulting PCM code will be shifted out during the subsequent encode time slot.
4	NC	Unused
5	GNDA	Analog ground. All analog signals are referenced to this pin.
6	SIG_R	Receive signaling bit output. During receive signaling frames the least significant (last) bit shifted into D_R is internally latched and appears at this output—SIG_R will then remain valid until changed during a subsequent receive signaling frame or reset by a power-down command.
7	NC	Unused
8	D_R	Serial PCM data input to the decoder. During the decoder time slot, PCM data is shifted into D_R, most significant bit first, on the falling edge of CLK_R.
9	PDN	TTL output level which goes high when the CODEC is in the power-down mode. May be used to power-down other circuits associated with the PCM channel. Can be wire ANDed with other PDN outputs.
10	VF_R	Analog output from the decoder. The decoder sample and hold amplifier is updated approximately 15 μs after the end of the decode time slot.

TP3020 (Continued)

Pin No.	Name	Function
11	NC	Unused
12	NC	Unused
13	GNDD	Digital ground. All digital levels are referenced to this pin.
14	D_X	Serial PCM TRI-STATE® output from the encoder. During the encoder time slot, the PCM code for the previous sample of VF_X is shifted out, most significant bit first, on the rising edge of CLK_X.
15	$\overline{TS}_X$	Time slot output. This TTL compatible open-drain output pulses low during the encoder time slot. May be used to enable external TRI-STATE® bus drivers if highly capacitive loads must be driven. Can be wire ANDed with other $\overline{TS}_X$ outputs.
16	V_{CC}	5V (±5%) input.
17	CLK_R	Master decoder clock input used to shift in the PCM data on D_R and to operate the decoder sequencer. May operate at 1.536 MHz, 1.544 MHz or 2048 MHz. May be asynchronous with CLK_X or CLK_C.
18	FS_R	Decoder frame sync pulse. Normally occurring at an 8 kHz rate, this pulse is nominally one CLK_R cycle wide. Extending the width of FS_R to two or more cycles of CLK_R signifies a receive signaling frame.

Description of Pin Functions (Continued)

TP3020 (Continued)

Pin No.	Name	Function
19	CLK_X	Master encoder clock input used to shift out the PCM data on D_X and to operate the encoder sequencer. May operate at 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with CLK_R or CLK_C.
20	FS_X	Encoder frame sync pulse. Normally occurring at an 8 kHz rate, this pulse is nominally one CLK_X cycle wide. Extending the width of FS_X to two or more cycles of CLK_X signifies a transmit signaling frame.
21	SIG_X	Transmit signaling input. During a transmit signaling frame, the signal at SIG_X is shifted out of D_X in place of the least significant (last) bit of PCM data.
22	V_{BB}	−5V (±5%) input.
23	D_C	Serial control data input. Serial data on D_C is shifted into the CODEC on the falling edge of CLK_C. In the fixed time slot mode, D_C doubles as a power-down input.
24	CLK_C	Control clock input used to shift serial control data into D_C. CLK_C must pulse 8 times during a period of time less than or equal to one frame time, although the 8 pulses may overlap a frame boundary. CLK_C need not be synchronous with CLK_X or CLK_R. Connecting CLK_C continuously high places the TP3020/TP3021 into the fixed time slot mode.

TP3021

Pin No.	Name	Function
1	NC	Unused
2	NC	Unused
3	VF_X	Analog input to the encoder. This signal will be sampled at the end of the encoder time slot and the resulting PCM code will be shifted out during the subsequent encode time slot.
4	NC	Unused
5	GNDA	Analog ground. All analog signals are referenced to this pin.
6	NC	Unused
7	D_R	Serial PCM data input to the decoder. During the decoder time slot, PCM data is shifted into D_R, most significant bit first, on the falling edge of CLK_R.
8	PDN	Open drain output which turns off when the CODEC is in the power-down mode. May be used to power-down other circuits associated with the PCM channel. Can be wire ANDed with other PDN outputs.
9	VF_R	Analog output from the decoder. The decoder sample and hold amplifier is updated approximately 15 μs after the end of the decode time slot.
10	NC	Unused
11	NC	Unused
12	GNDD	Digital ground. All digital levels are referenced to this pin.
13	D_X	Serial PCM TRI-STATE® output from the encoder. During the encoder time slot, the PCM code for the previous sample of VF_X is shifted out, most significant bit first, on the rising edge of CLK_X.
14	$\overline{TS}_X$	Time slot output. This TTL compatible open-drain output pulses low during the encoder time slot. May be used to enable external TRI-STATE® bus drivers if highly capacitive loads must be driven. Can be wire ANDed with other $\overline{TS}_X$ outputs.
15	V_{CC}	5V (±5%) input.
16	CLK_R	Master decoder clock input used to shift in the PCM data on D_R and to operate the decoder sequencer. May operate at 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with CLK_X or CLK_C.
17	FS_R	Decoder frame sync pulse. Normally occurring at an 8 kHz rate, this pulse is nominally one CLK_R cycle wide.
18	CLK_X	Master encoder clock input used to shift out the PCM data on D_X and to operate the encoder sequencer. May operate at 1.536 MHz 1.544 MHz, or 2.048 MHz. May be asynchronous with CLK_R or CLK_C.
19	FS_X	Encoder frame sync pulse. Normally occurring at an 8 kHz rate, this pulse is nominally one CLK_X cycle wide.
20	V_{BB}	−5V (±5%) input.
21	D_C	Serial control data input. Serial data on D_C is shifted into the CODEC on the falling edge of CLK_C. In the fixed time slot mode, D_C doubles as a power-down input.
22	CLK_C	Control clock input used to shift serial control data into D_C. CLK_C must pulse 8 times during a period of time less than or equal to one frame time, although the 8 pulses may overlap a frame boundary. CLK_C need not be synchronous with CLK_X or CLK_R. Connecting CLK_C continuously high places the TP3020/TP3021 into the fixed time slot mode.

Functional Description

Power-Up

Upon application of power, internal circuitry initializes the CODEC and places it into the power-down mode. No sequencing of 5V or −5V is required. In the power-down mode, all non-essential circuits are deactivated, the TRI-STATE® PCM data output D_X is placed in the high impedance state and the receive signaling output of the TP3020, SIG_R, is reset to logical zero. Once in the power-down mode, the method of activating the TP3020/TP3021 depends on the chosen mode of operation, time slot assignment or fixed time slot.

Time Slot Assignment Mode

The time slot assignment mode of operation is selected by maintaining CLK_C in a normally low state. The state of the CODEC is updated by pulsing CLK_C eight times within a period of 125 μs or less. The falling edge of each clock pulse shifts the data on the D_C input into the CODEC. The first two control bits determine if the subsequent control bits B3–B8 are to specify the time slot for the encoder (B1 = 0), the decoder (B2 = 0) or both (B1 and B2 = 0) or if the CODEC is to be placed into the power-down mode (B1 and B2 = 1). The desired action will take place upon the occurrence of the second frame sync pulse following the first pulse of CLK_C. Assigning a time slot to either the encoder or decoder will automatically power-up the entire CODEC circuit. The D_X output and D_R input, however, will be inhibited for one additional frame to allow the analog circuitry time to stabilize. If separate time slots are to be assigned to the encoder and the decoder, the encoder time slot should be assigned first. This is necessary because up to four frames are required to assign both time slots separately, but only three frames are necessary to activate the D_X output. If the encode time slot has not been updated the PCM data will be outputted during the previously assigned time slot which may now be assigned to another CODEC.

Fixed Time Slot Mode

There are several ways in which the TP3020/TP3021 may operate in the fixed time slot mode. The first and easiest method is to leave CLK_C disconnected or to connect CLK_C to V_{CC}. In this situation, D_C behaves as a power-down input. When D_C goes low, both encode and decode time slots are set to one on the second subsequent frame sync pulse. Time slot one corresponds to the eight CLK_X or CLK_R cycles starting one cycle from the nominal leading edge of FS_X or FS_R respectively. As in the time slot assignment mode, the D_X output is inhibited for one additional frame after the circuit is powered up. A logical "1" on D_C powers the CODEC down on the second subsequent FS_X pulse.

A second fixed time slot method is to operate CLK_C continuously. Placing a "1" on D_C will then cause the serial control register to fill up with ones. With B1 and B2 equal to "1" the CODEC will power-down. Placing a "0" on D_C will cause the serial control register to fill up with zeroes, assigning time slot one to both the encoder and decoder and powering up the device. One important restriction with this method of operation is that the rising transition of D_C must occur at least 8 cycles of CLK_C prior to FS_X. If this restriction is not followed, it is possible that on the frame prior to power-down, the encoder could be assigned to an incorrect time slot (e.g., 1, 3, 7, 15 or 31), resulting in a possible PCM bus conflict.

Serial Control Port

When the TP3020/TP3021 is operated in the time slot assignment mode or the fixed time slot mode with continuous clock, the data on D_C is shifted into the serial control register, bit 1 first. In the time slot assignment mode, depending on B1 and B2, the data in the RCV or XMT time slot registers is updated at the second FS_R or FS_X pulse after the first CLK_C pulse, or the CODEC is powered down. In the continuous clock fixed time slot mode, the CODEC is powered up or down at every second FS_R or FS_X pulse. The control register data is interpreted as follows:

B1	B2	Action
0	0	Assign time slot to encoder and decoder
0	1	Assign time slot to encoder
1	0	Assign time slot to decoder
1	1	Power-down CODEC

B3	B4	B5	B6	B7	B8	Time Slot
0	0	0	0	0	0	1
0	0	0	0	0	1	2
0	0	0	0	1	0	3
0	0	0	0	1	1	4
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1	1	1	1	1	0	63
1	1	1	1	1	1	64

During the power-down command, bits 3 through 8 are ignored. Note that with 64 possible time slot assignments it is frequently possible to assign a time slot which does not exist. This can be useful to disable an encoder or decoder without powering down the CODEC.

Signaling

The TP3020 μ-law CODEC contains circuitry to insert and extract signaling information for the PCM data. The transmit signaling frame is signified by widening the FS_X pulse from one cycle of CLK_X to two or more cycles.

When this occurs, the data present on the SIG_X input at the eighth clock pulse of the encode time slot is inserted into the last bit of the PCM data stream. A receive signaling frame is indicated in a similar fashion by widening the FS_R pulse to two or more cycles of CLK_R.

During a receive signaling frame, the last PCM bit shifted in is latched into a flip-flop and appears at the SIG_R output. This output will remain unchanged until the next signaling frame, until a power-down is executed or until power is removed from the device. Since the least significant bit of the PCM data is lost during a signaling frame, the decoder interprets the bit as a "1/2" (i.e., half way between a "0" and a "1"). This minimizes the noise and distortion due to the signaling.

Functional Description (Continued)

Encoding Delay

The encoding process begins immediately at the end of the encode time slot and is concluded no later than 17 time slots later. In normal applications, this PCM data is not shifted out until the next time slot 125 μs later, resulting in an encoding delay of 125 μs. In some applications it is possible to operate the CODEC at a higher frame rate to reduce this delay. With a 2.048 MHz clock, the FS rate could be increased to 15 kHz reducing the delay from 125 μs to 67 μs.

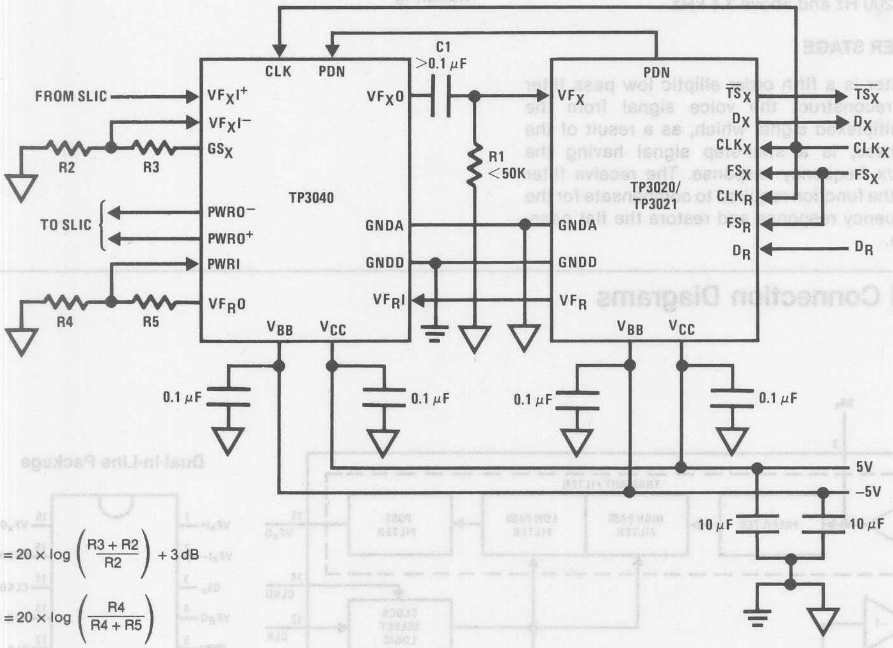
Decoding Delay

The decoding process begins immediately after the end of the decoder time slot. The output of the decoder sample and hold amplifier is updated 28 CLK_R cycles later. The decoding delay is therefore approximately 28 clock cycles plus one half of a frame time or 81 μs for a 1.544 MHz system with an 8 kHz frame rate or 76 μs for a 2.048 MHz system with an 8 kHz frame rate. Again, for some applications the frame rate could be increased to reduce this delay.

Typical Application

A typical application of the TP3020/TP3021 used in conjunction with the TP3040 PCM filter is shown. The values of resistor R1 and DC blocking capacitor C1, are non-critical. The capacitor value should exceed 0.1 μF, R1 should be less than 50 kΩ, and the product R1 $\times$ C1 should exceed 4 ms.

Typical Application



$$\text{XMT gain} = 20 \times \log\left(\frac{R3 + R2}{R2}\right) + 3\,\text{dB}$$

$$\text{RCV gain} = 20 \times \log\left(\frac{R4}{R4 + R5}\right)$$

The power supply decoupling capacitors should be 0.1 μF. In order to take advantage of the excellent noise performance of the TP3020/TP3021/TP3040, care must be taken in board layout to prevent coupling of digital noise into the sensitive analog lines.

TP3040/TP3040A PCM Monolithic Filter

General Description

The TP3040/TP3040A filter is a monolithic circuit containing both transmit and receive filters specifically designed for PCM CODEC filtering applications in 8 kHz sampled systems.

The filter is manufactured using double-poly silicon gate CMOS technology. Switched capacitor integrators are used to simulate classical LC ladder filters which exhibit low component sensitivity.

TRANSMIT FILTER STAGE

The transmit filter is a fifth order elliptic low pass filter in series with a fourth order Chebyshev high pass filter. It provides a flat response in the passband and rejection of signals below 200 Hz and above 3.4 kHz.

RECEIVE FILTER STAGE

The receive filter is a fifth order elliptic low pass filter designed to reconstruct the voice signal from the decoded/demultiplexed signal which, as a result of the sampling process, is a stair-step signal having the inherent sin x/x frequency response. The receive filter approximates the function required to compensate for the degraded frequency response and restore the flat passband response.

Features

- Exceeds all D3/D4 and CCITT specifications
- +5V, −5V power supplies
- Low power consumption:
  45 mW (600Ω 0 dBm load)
  30 mW (power amps disabled)
- Power down mode: 0.5 mW
- 20 dB gain adjust range
- No external anti-aliasing components
- Sin x/x correction in receive filter
- 50/60 Hz rejection in transmit filter
- TTL and CMOS compatible logic
- All inputs protected against static discharge due to handling

Block and Connection Diagrams

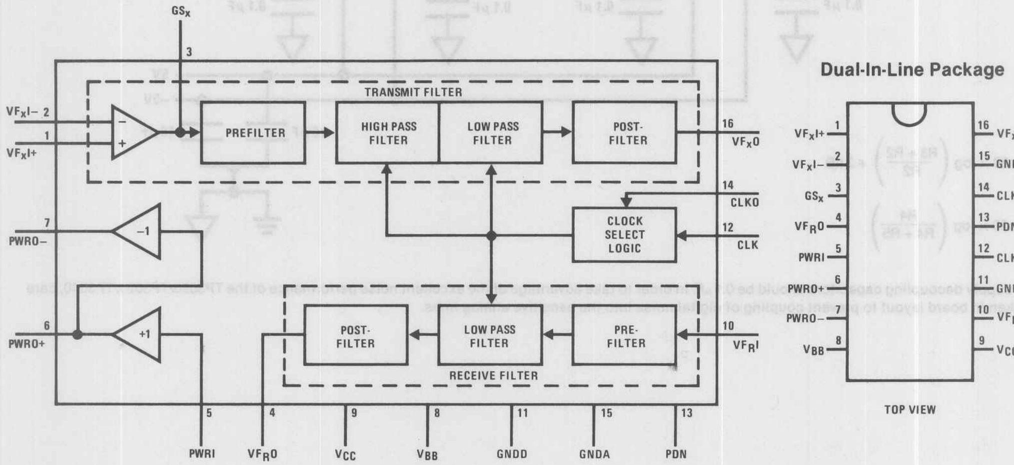


FIGURE 1

Absolute Maximum Ratings

Supply Voltages	±7V
Power Dissipation	1 W/Package
Input Voltage	±7V
Output Short-Circuit Duration	Continuous
Operating Temperature Range	−25°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Unless otherwise noted, $T_A = 0°C$ to $70°C$, $V_{CC} = 5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$, clock frequency is 2.048 MHz. Typical parameters are specified at $T_A = 25°C$, $V_{CC} = 5.0V$, $V_{BB} = -5.0V$. Digital interface voltages measured with respect to digital ground, GNDD. Analog voltages measured with respect to analog ground, GNDA.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER DISSIPATION						
I_{CC0}	V_{CC} Standby Current	PDN = V_{DD}, Power Down Mode		50	100	μA
I_{BB0}	V_{BB} Standby Current	PDN = V_{DD}, Power Down Mode		50	100	μA
I_{CC1}	V_{CC} Operating Current	$\overline{PWRI} = V_{BB}$, Power Amp Inactive		3.0	4.0	mA
I_{BB1}	V_{BB} Operating Current	$\overline{PWRI} = V_{BB}$, Power Amp Inactive		3.0	4.0	mA
I_{CC2}	V_{CC} Operating Current	Note 1		4.6	6.4	mA
I_{BB2}	V_{BB} Operating Current	Note 1		4.6	6.4	mA
DIGITAL INTERFACE						
I_{INC}	Input Current, CLK	$V_{BB} \le V_{IN} \le V_{CC}$	−10		10	μA
I_{INP}	Input Current, PDN	$V_{BB} \le V_{IN} \le V_{CC}$	−100			μA
I_{IN0}	Input Current, CLK0	$V_{BB} \le V_{IN} \le V_{CC} - 2V$	−10		−0.1	μA
V_{IL}	Input Low Voltage, CLK, PDN		0		0.8	V
V_{IH}	Input High Voltage, CLK, PDN		2.2		V_{CC}	V
V_{IL0}	Input Low Voltage, CLK0		V_{BB}		$V_{BB}+0.5$	V
V_{II0}	Input Intermediate Voltage, CLK0		−0.8		0.8	V
V_{IH0}	Input High Voltage, CLK0		$V_{CC}-0.5$		V_{CC}	V
TRANSMIT INPUT OP AMP						
IB_xI	Input Leakage Current, VF_xI	$V_{BB} \le VF_xI \le V_{CC}$	−100		100	nA
RI_xI	Input Resistance, VF_xI	$V_{BB} \le VF_xI \le V_{CC}$	10			MΩ
VOS_xI	Input Offset Voltage, VF_xI	$-2.5V \le V_{IN} \le +2.5V$	−20		20	mV
V_{CM}	Common-Mode Range, VF_xI		−2.5		2.5	V
CMRR	Common-Mode Rejection Ratio	$-2.5V \le V_{IN} \le 2.5V$	60			dB
PSRR	Power Supply Rejection of V_{CC} or V_{BB}		60			dB
R_{OL}	Open Loop Output Resistance, GS_x			1		kΩ
R_L	Minimum Load Resistance, GS_x		10			kΩ
C_L	Maximum Load Capacitance, GS_x				25	pF
VO_xI	Output Voltage Swing, GS_x	$R_L \ge 10k$	±2.5			V
A_{VOL}	Open Loop Voltage Gain, GS_x	$R_L \ge 10k$	5,000			V/V
F_c	Open Loop Unity Gain Bandwidth, GS_x			2		MHz

AC Electrical Characteristics

Unless otherwise specified, $T_A = 25°C$. All parameters are specified for a signal level of 0 dBm0 at 1 kHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TRANSMIT FILTER (Transmit filter input op amp set to the non-inverting unity gain mode, with $VF_xI = 1.1$ Vrms unless otherwise noted.)						
RL_x	Minimum Load Resistance, VF_xO		10			kΩ
CL_x	Load Capacitance, VF_xO				25	pF
RO_x	Output Resistance, VF_xO			1	3	Ω
PSRR1	V_{CC} Power Supply Rejection, VF_xO	f = 1 kHz, $VF_xI+ = 0$ Vrms	30			dB
PSRR2	V_{BB} Power Supply Rejection, VF_xO	Same as Above	35			dB
GA_x	Absolute Gain	f = 1 kHz (TP3040A)	2.9	3.0	3.1	dB
		f = 1 kHz (TP3040)	2.875	3.0	3.125	dB
GR_x	Gain Relative to GA_x	Below 50 Hz			−35	dB
		50 Hz		−41	−35	dB
		60 Hz		−35	−30	dB
		200 Hz (TP3040A)	−1.5		0	dB
		200 Hz (TP3040)	−1.5		0.05	dB
		300 Hz to 3 kHz (TP3040A)	−0.125		0.125	dB
		300 Hz to 3 kHz (TP3040)	−0.15		0.15	dB
		3.3 kHz	−0.35		0.03	dB
		3.4 kHz	−0.70		−0.1	dB
		4.0 kHz		−15	−14	dB
		4.6 kHz and Above			−32	dB
DA_x	Absolute Delay at 1 kHz				230	μs
DD_x	Differential Envelope Delay from 1 kHz to 2.6 kHz				60	μs
DP_x1	Single Frequency Distortion Products				−48	dB
DP_x2	Distortion at Maximum Signal Level	0.16 Vrms, 1 kHz Signal Applied to VF_xI+, Gain = 20 dB, $R_L = 10k$			−45	dB
NC_x1	Total C Message Noise at VF_xO			2	5	dBrnc0
NC_x2	Total C Message Noise at VF_xO	Gain Setting Op Amp at 20 dB, Non-Inverting, Note 3 $T_A = 0°C$ to 70°C		3	6	dBrnc0
GA_xT	Temperature Coefficient of 1 kHz Gain			0.0004		dB/°C
GA_xS	Supply Voltage Coefficient of 1 kHz Gain	$V_{CC} = 5.0V \pm 5\%$ $V_{BB} = -5.0V \pm 5\%$		0.01		dB/V
CT_{RX}	Crosstalk, Receive to Transmit $20 \log \frac{VF_xO}{VF_RO}$	Receive Filter Output = 2.2 Vrms $VF_xI+ = 0$ Vrms, f = 0.2 kHz to 3.4 kHz Measure VF_xO			−70	dB
GR_xL	Gaintracking Relative to GA_x	Output Level = +3 dBm0	−0.1		0.1	dB
		+2 dBm0 to −40 dBm0	−0.05		0.05	dB
		−40 dBm0 to −55 dBm0	−0.1		0.1	dB

AC Electrical Characteristics (Continued)

Unless otherwise specified, $T_A = 25°C$. All parameters are specified for a signal level of 0 dBm0 at 1 kHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVE FILTER (Unless otherwise noted, the receive filter is preceded by a sin x/x filter with an input signal level of 1.6 Vrms.)						
IB_R	Input Leakage Current, VF_RI	$-3.2V \le V_{IN} \le 3.2V$	−100		100	nA
RI_R	Input Resistance, VF_RI		10			MΩ
RO_R	Output Resistance, VF_RO			1	3	Ω
CL_R	Load Capacitance, VF_RO				25	pF
RL_R	Load Resistance, VF_RO		10			kΩ
PSRR3	Power Supply Rejection of V_{CC} or V_{BB}, VF_RO	VF_RI Connected to GNDA f = 1 kHz	35			dB
VOS_RO	Output DC Offset, VF_RO	VF_RI Connected to GNDA	−200		200	mV
GA_R	Absolute Gain	f = 1 kHz (TP3040A) f = 1 kHz (TP3040)	−0.1 −0.125	0 0	0.1 0.125	dB dB
GR_R	Gain Relative to Gain at 1 kHz	Below 300 Hz 300 Hz to 3.0 kHz (TP3040A) 300 Hz to 3.0 kHz (TP3040) 3.3 kHz 3.4 kHz 4.0 kHz 4.6 kHz and Above	 −0.125 −0.15 −0.35 −0.7 		0.125 0.125 0.15 0.03 −0.1 −14 −32	dB dB dB dB dB dB dB
DA_R	Absolute Delay at 1 kHz				100	µs
DD_R	Differential Envelope Delay 1 kHz to 2.6 kHz				100	µs
DP_R1	Single Frequency Distortion Products	f = 1 kHz			−48	dB
DP_R2	Distortion at Maximum Signal Level	2.2 Vrms Input to Sin x/x Filter, f = 1 kHz, R_L = 10k			−45	dB
NC_R	Total C-Message Noise at VF_RO			3	5	dBrnc0
GA_RT	Temperature Coefficient of 1 kHz Gain			0.0004		dB/°C
GA_RS	Supply Voltage Coefficient of 1 kHz Gain			0.01		dB/V
CT_{XR}	Crosstalk, Transmit to Receive $20 \log \frac{VF_RO}{VF_XO}$	Transmit Filter Output = 2.2 Vrms VF_RI = 0 Vrms, f = 0.3 kHz to 3.4 kHz Measure VF_RO			−70	dB
GR_RL	Gaintracking Relative to GA_R	Output Level = +3 dBm0 +2 dBm0 to −40 dBm0 −40 dBm0 to −55 dBm0 Note 5	−0.1 −0.05 −0.1		0.1 0.05 0.1	dB dB dB

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVE OUTPUT POWER AMPLIFIER						
IBP	Input Leakage Current, PWRI	$-3.2V \le V_{IN} \le 3.2V$	0.1		3	μA
RIP	Input Resistance, PWRI		10			MΩ
ROP1	Output Resistance, PWRO+, PWRO−	Amplifiers Active		1		Ω
CLP	Load Capacitance, PWRO+, PWRO−				500	pF
GA_P+	Gain, PWRI to PWRO+	$R_L = 600\Omega$ Connected Between PWRO+ and PWRO−, Input Level = 0 dBm0 (Note 4)		1		V/V
GA_P-	Gain, PWRI to PWRO−			−1		V/V
GR_PL	Gaintracking Relative to 0 dBm0 Output Level	V = 2.05 Vrms, $R_L = 600\Omega$ (Notes 4, 5) V = 1.75 Vrms, $R_L = 300\Omega$	−0.1 −0.1		0.1 0.1	dB dB
S/D_P	Signal/Distortion	V = 2.05 Vrms, $R_L = 600\Omega$ (Notes 4, 5) V = 1.75 Vrms, $R_L = 300\Omega$			−45 −45	dB dB
VOSP	Output DC Offset, PWRO+, PWRO−	PWRI Connected to GNDA	−50		50	mV
PSRR5	Power Supply Rejection of V_{CC} or V_{BB}	PWRI Connected to GNDA	45			dB

Note 1: Maximum power consumption will depend on the load impedance connected to the power amplifier. The specification listed assumes 0 dBm is delivered to 600Ω connected from PWRO+ to PWRO−.

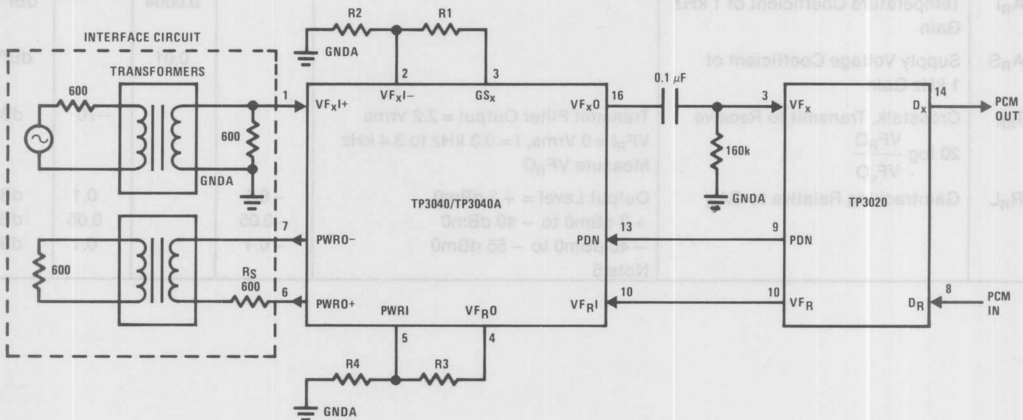
Note 2: Voltage input to receive filter at 0V, VF_RO connected to PWRI, 600Ω from PWRO+ to PWRO−. Output measured from PWRO+ to PWRO−.

Note 3: The 0 dBm0 level for the filter is assumed to be 1.54 Vrms measured at the output of the XMT or RCV filter.

Note 4: The 0 dBm0 level for the power amplifiers is load dependent. For $R_L = 600\Omega$ to GNDA, the 0 dBm0 level is 1.43 Vrms measured at the amplifier output. For $R_L = 300\Omega$ the 0 dBm0 level is 1.22 Vrms.

Note 5: VF_RO connected to PWRI, input signal applied to VF_RI.

Typical Application



Note 1: Transmit voltage gain $= \frac{R1 + R2}{R2} \times \sqrt{2}$ (The filter itself introduces a 3 dB gain), ($R1 + R2 \ge 10k$)

Note 2: Receive gain $= \frac{R4}{R3 + R4}$

($R3 + R4 \ge 10k$)

Note 3: In the configuration shown, the receive filter power amplifiers will drive a 600Ω T to R termination to a maximum signal level of 8.5 dBm. An alternative arrangement, using a transformer winding ratio equivalent to 1.414:1 and 300Ω resistor, R_S, will provide a maximum signal level of 10.1 dBm across a 600Ω termination impedance.

FIGURE 2

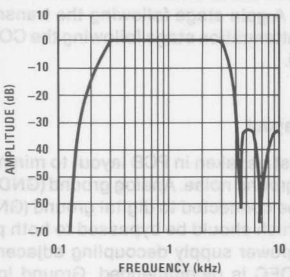
Description of Pin Functions

Pin No.	Name	Function
1	VF_XI+	The non-inverting input to the transmit filter stage.
2	VF_XI-	The inverting input to the transmit filter stage.
3	GS_X	The output used for gain adjustments of the transmit filter.
4	VF_RO	The low power receive filter output. This pin can directly drive the receive port of an electronic hybrid.
5	PWRI	The input to the receive filter differential power amplifier.
6	PWRO +	The non-inverting output of the receive filter power amplifier. This output can directly interface conventional transformer hybrids.
7	PWRO −	The inverting output of the receive filter power amplifier. This output can be used with PWRO + to differentially drive a transformer hybrid.
8	V_{BB}	The negative power supply pin. Recommended input is −5V.
9	V_{CC}	The positive power supply pin. The recommended input is 5V.
10	VF_RI	The input pin for the receive filter stage.

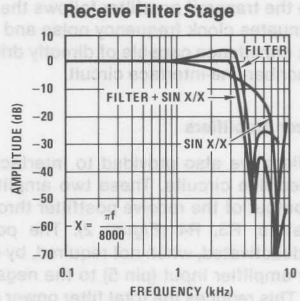
Pin No.	Name	Function
11	GNDD	Digital ground input pin. All digital signals are referenced to this pin.
12	CLK	Master input clock. Input frequency can be selected as 2.048 MHz, 1.544 MHz or 1.536 MHz.
13	PDN	The input pin used to power down the TP3040/TP3040A during idle periods. Logic 1 (V_{CC}) input voltage causes a power down condition. An internal pull-up is provided.
14	CLK0	This input pin selects internal counters in accordance with the CLK input clock frequency: **CLK** — **Connect CLK0 to:** 2048 kHz — V_{CC} 1544 kHz — GNDD 1536 kHz — V_{BB} An internal pull-up is provided.
15	GNDA	Analog ground input pin. All analog signals are referenced to this pin. Not internally connected to GNDD.
16	VF_XO	The output of the transmit filter stage.

Typical Performance Characteristics

Transmit Filter Stage



Receive Filter Stage



Functional Description

The TP3040/TP3040A monolithic filter contains four main sections; Transmit Filter, Receive Filter, Receive Filter Power Amplifier, and Frequency Divider/Select Logic *(Figure 1)*. A brief description of the circuit operation for each section is provided below.

Transmit Filter

The input stage of the transmit filter is a CMOS operational amplifier which provides an input resistance of greater than 10 MΩ, a voltage gain of greater than 10,000, low power consumption (less than 3 mW), high power supply rejection, and is capable of driving a 10 kΩ load in parallel with up to 25 pF. The inputs and output of the amplifier are accessible for added flexibility. Non-inverting mode, inverting mode, or differential amplifier mode operation can be implemented with external resistors. It can also be connected to provide a gain of up to 20 dB without degrading the overall filter performance.

The input stage is followed by a prefilter which is a two-pole RC active low pass filter designed to attenuate high frequency noise before the input signal enters the switched-capacitor high pass and low pass filters.

A high pass filter is provided to reject 200 Hz or lower noise which may exist in the signal path. The low pass portion of the switched-capacitor filter provides stopband attenuation which exceeds the D3 and D4 specifications as well as the CCITT G712 recommendations.

The output stage of the transmit filter, the postfilter, is also a two-pole RC active low pass filter which attenuates clock frequency noise by at least 40 dB. The output of the transmit filter is capable of driving a ±3.2V peak to peak signal into a 10 kΩ load in parallel with up to 25 pF.

Receive Filter

The input stage of the receive filter is a prefilter which is similar to the transmit prefilter. The prefilter attenuates high frequency noise that may be present on the receive input signal. A switched capacitor low pass filter follows the prefilter to provide the necessary passband flatness, stopband rejection and sin x/x gain correction. A postfilter which is similar to the transmit postfilter follows the low pass stage. It attenuates clock frequency noise and provides a low output impedance capable of directly driving an electronic subscriber-line-interface circuit.

Receive Filter Power Amplifiers

Two power amplifiers are also provided to interface to transformer coupled line circuits. These two amplifiers are driven by the output of the receive postfilter through gain setting resistors, R3, R4 *(Figure 2)*. The power amplifiers can be deactivated, when not required, by connecting the power amplifier input (pin 5) to the negative power supply V_{BB}. This reduces the total filter power consumption by approximately 10 mW–20 mW depending on output signal amplitude.

Power Down Control

A power down mode is also provided. A logic 1 power down command applied on the PDN pin (pin 13) will reduce the total filter power consumption to less than 1 mW and clamp the power amplifier outputs to V_{BB}. Connect PDN to GNDD for normal operation.

Frequency Divider and Select Logic Circuit

This circuit divides the external clock frequency down to the switching frequency of the low pass and high pass switched capacitor filters. The divider also contains a TTL – CMOS interface circuit which converts the external TTL clock level to the CMOS logic level required for the divider logic. This interface circuit can also be directly driven by CMOS logic. A frequency select circuit is provided to allow the filter to operate with 2.048 MHz, 1.544 MHz or 1.536 MHz clock frequencies. By connecting the frequency select pin CLK0 (pin 14) to V_{CC}, a 2.048 MHz clock input frequency is selected. Digital ground selects 1.544 MHz and V_{BB} selects 1.536 MHz.

Applications Information

Gain Adjust

Figure 2 shows the signal path interconnections between the TP3040/TP3040A and the TP3020 single-channel CODEC. The transmit RC coupling components have been chosen both for minimum passband droop and to present the correct impedance to the CODEC during sampling.

Optimum noise and distortion performance will be obtained from the TP3040/TP3040A filter when operated with system peak overload voltages of ±2.5V to ±3.2V at VF_xO and VF_RO. When interfacing to a PCM CODEC with a peak overload voltage outside this range, further gain or attenuation may be required.

For example, the TP3040/TP3040A filter can be used with the TP3000 series CODEC which has a 5.5V peak overload voltage. A gain stage following the transmit filter output and an attenuation stage following the CODEC output are required.

Board Layout

Care must be taken in PCB layout to minimize power supply and ground noise. Analog ground (GNDA) of each filter should be connected to digital ground (GNDD) at a single point, which should be bypassed to both power supplies. Further power supply decoupling adjacent to each filter and CODEC is recommended. Ground loops should be avoided, both between GNDA and GNDD and between the GNDA traces of adjacent filters and CODECs.

National Semiconductor

PRELIMINARY

TP3051, TP3056 Monolithic Parallel Interface CODEC/Filter Family

General Description

The TP3051, TP3056 family consists of a μ-law and A-law monolithic PCM CODEC/filter set utilizing a common A/D and D/A conversion architecture, as shown in *Figure 1*, and a unique parallel I/O logic interface.

The encode portion of each device consists of an input gain adjust amplifier, an active RC pre-filter which eliminates very high frequency noise prior to entering a switched-capacitor band-pass filter that rejects signals below 200 Hz or above 3400 Hz. Also included are auto-zero circuitry and a companding coder which samples the filtered signal and encodes it in the companded μ-law or A-law PCM format. The decode portion of each device consists of an expanding decoder, which reconstructs the analog signal from the companded μ-law or A-law code, a low-pass filter which corrects for the sin x/x response of the decoder output and rejects signals above 3400 Hz.

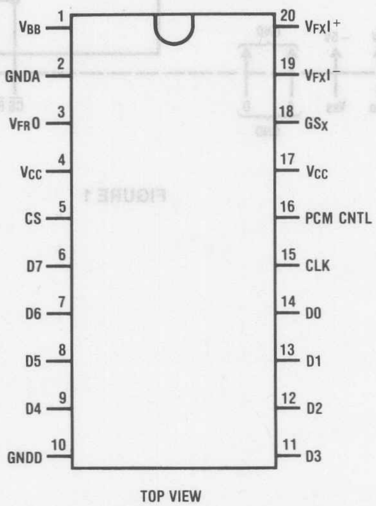
The TP3051 μ-law and TP3056 A-law devices are pin compatible parallel interface CODEC/filters intended to be used in conjunction with the TP3100 family of Digital Line Interface Controllers (DLIC) in switching system applications. All control, clock and signal information is communicated between the DLIC controller and up to 32 TP3051 or TP3056 devices via an eight bit I/O port and three control lines.

Features

- Complete CODEC and filtering system including:
  - Transmit high-pass and low-pass filtering
  - Receive low-pass filter with sin x/x correction
  - Active RC noise filters
  - μ-law or A-law compatible COder and DECoder
  - Internal precision voltage reference
  - Parallel I/O and control interface
- Meets or exceeds all D3/D4 and CCITT specifications
- ±5V operation
- Maximizes line interface card circuit density
- Low operating power—typically 50 mW
- Power-down standby mode—typically 1 mW

Connection Diagram

Dual-In-Line Package



TOP VIEW

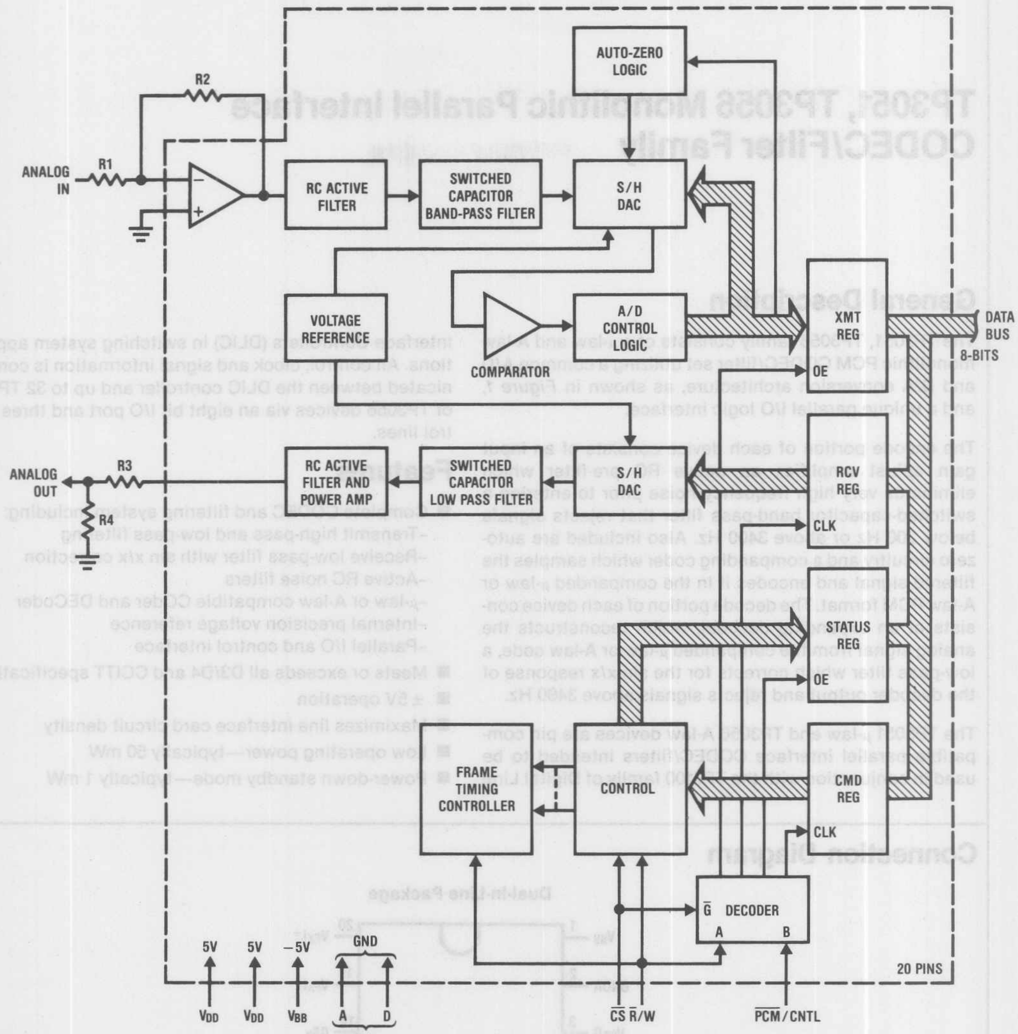

AUTO-ZERO LOGIC
R2
ANALOG IN
R1
RC ACTIVE FILTER
SWITCHED CAPACITOR BAND-PASS FILTER
S/H DAC
VOLTAGE REFERENCE
COMPARATOR
A/D CONTROL LOGIC
XMT REG
OE
DATA BUS 8-BITS
ANALOG OUT
R3
R4
RC ACTIVE FILTER AND POWER AMP
SWITCHED CAPACITOR LOW PASS FILTER
S/H DAC
RCV REG
CLK
STATUS REG
OE
FRAME TIMING CONTROLLER
CONTROL
CMD REG
CLK
G DECODER
A
B
20 PINS
5V
5V
−5V
GND
V_{DD}
V_{DD}
V_{BB}
A
D
GND
CS R/W
PCM/CNTL

FIGURE 1

National Semiconductor

TP3052, TP3053, TP3054, TP3057 Monolithic Serial Interface CODEC/Filter Family

General Description

The TP3052, TP3053, TP3054, TP3057 family consists of μ-law and A-law monolithic PCM CODEC/filters utilizing the A/D and D/A conversion architecture, shown in *Figure 1*, and a serial PCM interface.

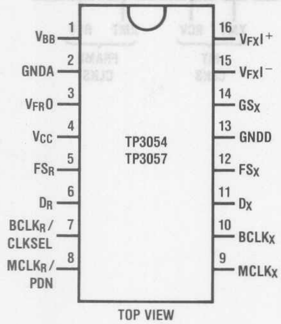
The encode portion of each device consists of an input gain adjust amplifier, an active RC pre-filter which eliminates very high frequency noise prior to entering a switched-capacitor band-pass filter that rejects signals below 200 Hz or above 3400 Hz. Also included are auto-zero circuitry and a companding coder which samples the filtered signal and encodes it in the companded μ-law or A-law PCM format. The decode portion of each device consists of an expanding decoder, which reconstructs the analog signal from the companded μ-law or A-law code, a low-pass filter which corrects for the sin x/x response of the decoder output and rejects signals above 3400 Hz. The devices require two 1.536/1.544 MHz or 2.048 MHz transmit and receive master clocks, which may be asynchronous, transmit and receive bit clocks, which are synchronous with the master clocks but may vary from 64 kHz to 2.048 MHz, and transmit and receive frame sync pulses. The timing of the frame sync pulses and PCM data is compatible with both industry standard formats.

Features

- Complete CODEC and filtering system including:
  - -Transmit high-pass and low-pass filtering
  - -Receive low-pass filter with sin x/x correction
  - -Active RC noise filters
  - -μ-law or A-law compatible COder and DECoder
  - -Internal precision voltage reference
  - -Serial I/O interface
- μ-law with signaling, TP3020 (2910) timing—TP3052
- μ-law with signaling, TP5116A, TP5117A timing—TP3053
- μ-law without signaling, 16-pin—TP3054
- A-law, 16-pin—TP3057
- Meets or exceeds all D3/D4 and CCITT specifications
- ±5V operation
- Maximizes line interface card circuit density
- Low operating power—typically 50 mW
- Power-down standby mode—typically 1 mW

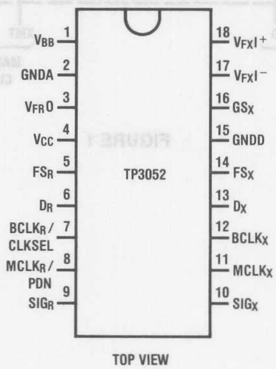
Connection Diagrams

Dual-In-Line Package



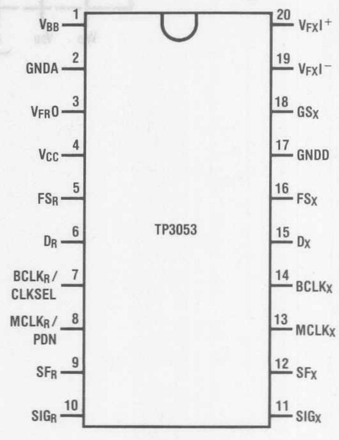
TOP VIEW

Dual-In-Line Package



TOP VIEW

Dual-In-Line Package



TOP VIEW

Block Diagram

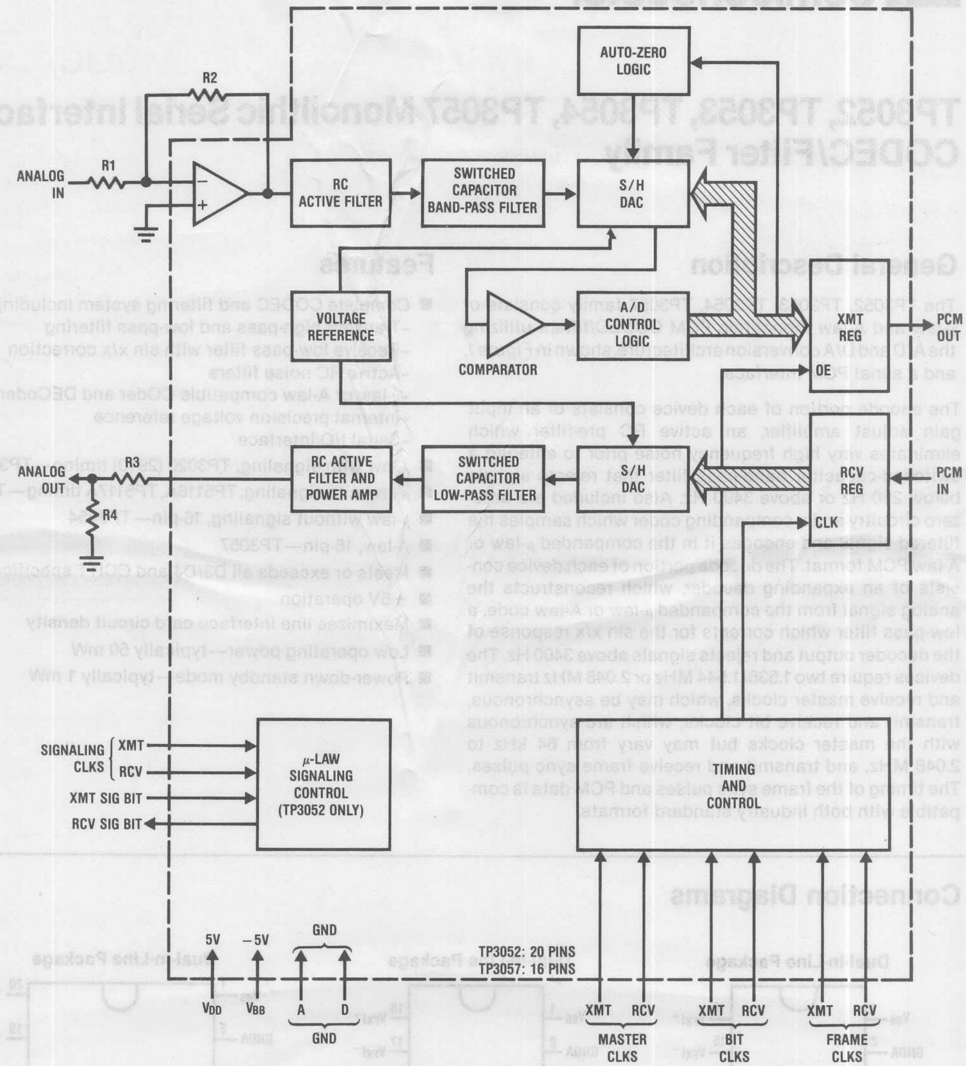


FIGURE 1

National Semiconductor

PRELIMINARY

TP3110, TP3120 Digital Line Interface Controllers (DLIC)

General Description

The TP3110, TP3120 Digital Line Interface Controllers (DLIC) are general purpose switching components primarily intended to serve as controllers of subscriber line, service and trunk circuit cards of a digital switching system. They are also useful as general purpose data controllers for data switching and multiplexing applications.

The DLIC performs a three-way control function when used for digital switching applications. The block diagram (*Figure 1*) displays this tri-port arrangement. First, the DLIC controls the space and time switching function between subscriber line PCM CODECs and filters and the switching system time division multiplex (TDM) highways. Second, the DLIC controls the flow of information between the per line circuit devices and the line card's local processor. Last, it performs all protocol control functions, using the HDLC protocol format, for information passing between the local line card processor and the main switching system processor (or any other system processor).

The DLIC is configured with a parallel interface for the per line and local processor circuits and with full duplex multiple port serial highways for the system interface. All system related communications with the DLIC controlled circuit card are handled via channel assignments on the serial TDM interface. In this way, all system data communications, subscriber PCM, data, signaling and system control information are transported and switched with a single network. This approach improves the overall flexibility and modularity of the total system design.

The DLIC contains a time-slot memory map for up to 128 duplex TDM channels, four high speed serial port transceivers, interface logic to allow the local processor to communicate with the per line circuit devices (combination CODEC/filter circuits and the SLIC), a complete HDLC protocol controller for system control messages, a vectored interrupt controller for the HDLC protocol, signaling and timing control and finally, a buffer memory for per line signaling data.

Features

- A complete interface controller for up to 32 subscribers of a digital switching system
- Performs all time division multiplex (TDM) channel assignments for the circuit card it controls
- Provides two (TP3110) or four (TP3120) full duplex serial TDM highways for the system interface
- Performs the first stage space and time switching function to minimize hardware requirements and switching delay
- Assignable addressing plus a "broadcast" address allows up to 255 controllers per subsystem control group without address field overlap
- System control uses the HDLC protocol with all zero insertion/deletion, checksum and flag control functions performed by the DLIC
- Single 5V power supply operation

Block Diagram

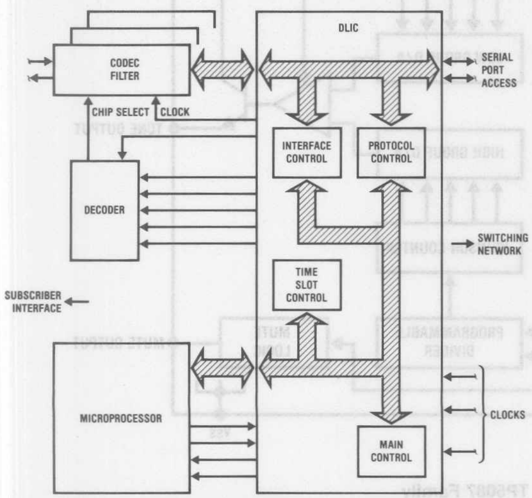
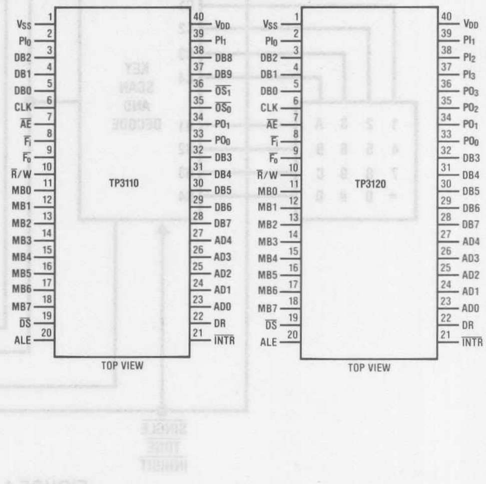


FIGURE 1. DLIC Signal Flows

Connection Diagrams

Dual-In-Line Package　　Dual-In-Line Package



TP5087/TP5087A, TP5092/TP5092A, TP5094/TP5094A DTMF (TOUCH-TONE®) Generators

General Description

The TP5087, TP5092 and TP5094 are low threshold voltage, field-implanted, metal gate CMOS integrated circuits. The devices interface directly to a standard telephone keypad and generate all dual tone multi-frequency pairs required in tone-dialing systems. The tone synthesizers are locked to an on-chip reference oscillator using an inexpensive 3.579545 MHz crystal for high tone accuracy. The crystal and an output load resistor are the only external components required for tone generation. A MUTE OUT logic signal, which changes state when any key is depressed, is also provided.

Features

- 2.5V–15V operation when generating tones (TP5087A, TP5092A, TP5094A)
- 2V operation of keyscan and MUTE logic
- Powered directly from telephone line
- Interfaces with standard single-contact or 2-of-8 telephone keypad
- Static sensing of key closures
- On-chip 3.579545 MHz crystal-controlled oscillator
- On-chip regulation of tone amplitudes
- High group and low group tones generated and mixed internally
- High group pre-emphasis
- Low harmonic distortion
- Open emitter-follower low-impedance output
- SINGLE TONE INHIBIT pin

Block Diagram

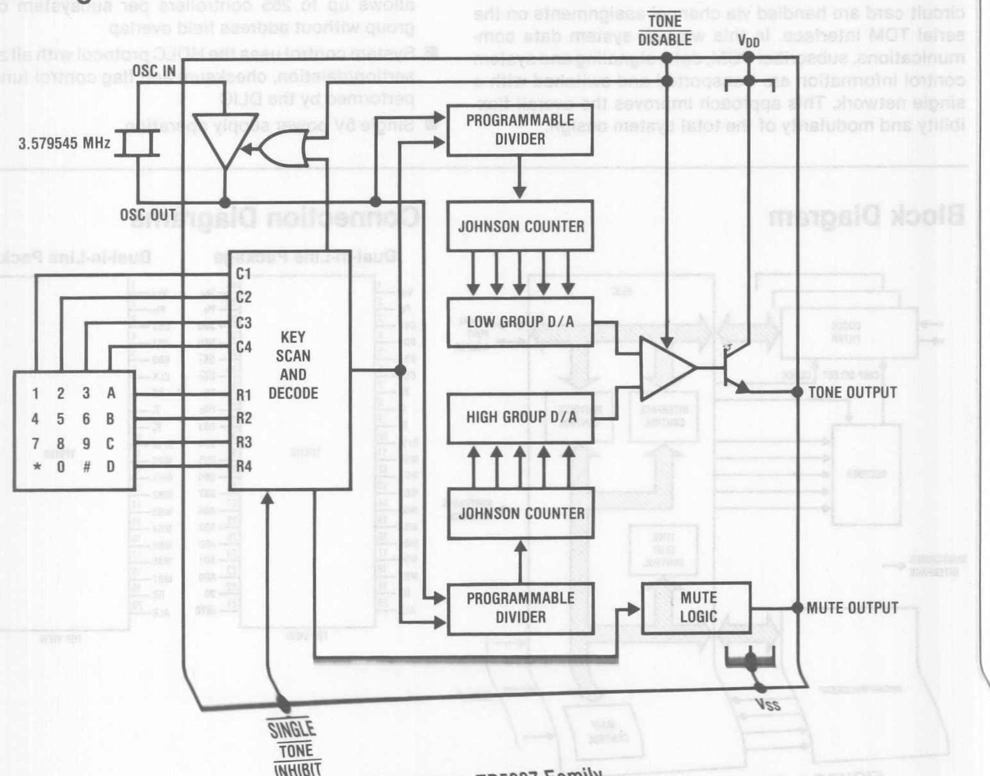


FIGURE 1. TP5087 Family

® is a registered trademark of Bell Telephone.

Absolute Maximum Ratings

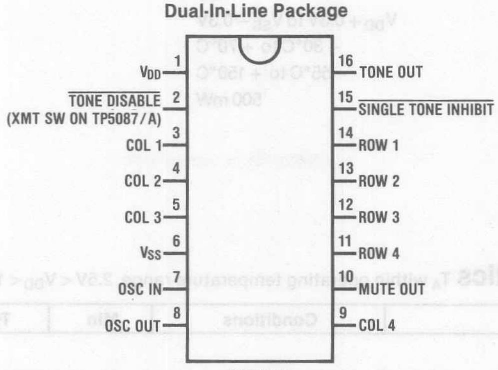
Supply Voltage ($V_{DD} - V_{SS}$)	15V
Maximum Voltage at Any Pin	$V_{DD} + 0.3V$ to $V_{SS} - 0.3V$
Operating Temperature	$-30°C$ to $+70°C$
Storage Temperature	$-55°C$ to $+150°C$
Maximum Power Dissipation	500 mW

Electrical Characteristics T_A within operating temperature range, $2.5V < V_{DD} < 10V$ unless otherwise stated.

Parameter	Conditions	Min	Typ	Max	Units
TP5087, TP5092, TP5094					
Minimum Supply Voltage Swing, $V_{DD\,(min)}$	Generating Tones	3.5			V
Output Amplitudes	$R_L = 240\Omega$				
Low Group	$V_{DD} = 3.8V$		430		mVrms
	$V_{DD} = 10V$		480		mVrms
High Group	$V_{DD} = 3.8V$		580		mVrms
	$V_{DD} = 10V$		650		mVrms
Mean Output DC Offset	$V_D = 3.8V$		2		V
	$V_{DD} = 10V$		4.2		V
TP5087A, TP5092A, TP5094A					
Minimum Supply Voltage Swing, $V_{DD\,(min)}$	Generating Tones	2.5			V
Output Amplitudes	$R_L = 100\Omega$				
Low Group	$V_{DD} = 2.5V$		170		mVrms
	$V_{DD} = 10V$		190		mVrms
High Group	$V_{DD} = 2.5V$		230		mVrms
	$V_{DD} = 10V$		255		mVrms
Mean Output DC Offset	$V_{DD} = 2.5V$		0.7		V
	$V_{DD} = 10V$		2.5		
ALL PARTS					
Minimum Supply Voltage for Keyscan and MUTE Logic Functions		2			V
Operating Current					
Idle	$R_L = 10\ k\Omega$		20		μA
Generating Tones	$V_{DD} = 5V$		2		mA
Input Pull-Up Resistors					
COLUMN and ROW (Pull-Down)			40		kΩ
$\overline{\text{SINGLE TONE INHIBIT}}$			50		kΩ
$\overline{\text{TONE DISABLE}}$			50		kΩ
MUTE OUT Sink Current (COLUMN and ROW Inactive)	$V_{DD} = 3V$, $V_o = 0.5V$	0.5			mA
MUTE OUT Source Current (COLUMN and ROW Active)	$V_{DD} = 3V$, $V_o = 2.5V$	0.5			mA
High Group Pre-Emphasis		2.4	2.7	3.0	dB
Dual Tone/Total Harmonic Distortion Ratio	1 MHz Bandwidth	22			dB
Start-Up Time (to 90% Amplitude)				5	ms

Connection Diagram

Dual-In-Line Package



TOP VIEW

Pin Descriptions

V_{DD} (Pin 1): This is positive voltage supply to the device, referenced to V_{SS}. The collectors of the TONE OUT, and XMT SW transistors are also connected to this pin.

V_{SS} (Pin 6): This is the negative voltage supply.

OSCILLATOR (Pins 7 and 8): All tone generation timing is derived from the on-chip oscillator circuit. A low-cost 3.579545 MHz A-cut crystal (NTSC TV color-burst) is needed between pins 7 and 8. Load capacitors and a feedback resistor are included on-chip for good start-up and stability. The oscillator stops when both COLUMN inputs and ROW inputs are sensed sequentially with no valid input having been detected. The oscillator is also stopped when the $\overline{\text{TONE DISABLE}}$ input is pulled to logic low.

ROW and COLUMN Inputs (Pins 3, 4, 5, 9, 11, 12, 13, 14): When no key is pushed, pull-up resistors are active on COLUMN inputs and pull-down resistors are active on ROW inputs. Column latches are ON and ready to store column key closures. After a key is pushed, the row pull-down resistors cause a negative-true on COLUMN inputs which starts the oscillator and initiates tone generation. Negative-true logic signals simulating key closures can also be used.

$\overline{\text{TONE DISABLE}}$ Input (Pin 2): The $\overline{\text{TONE DISABLE}}$ input has an internal pull-up resistor. When this input is open or at logic high, the normal tone output mode will occur. When $\overline{\text{TONE DISABLE}}$ input is at logic low, the device will be in the inactive mode, tone output will be at an open circuit state. With mask option, $\overline{\text{TONE DISABLE}}$ input can either inhibit or not inhibit the MUTE function.

XMT SW Output (Pin 2 of TP5087/A only): With no key inputs, this output is pulled high by the open emitter of an NPN transistor. Any key entry turns off this transistor by pulling its base to V_{SS}.

MUTE Output (Pin 10): The MUTE output is a conventional CMOS output that sinks current to V_{SS} with no valid input and sources current from V_{DD} when a valid key input is sensed. The MUTE output will switch regardless of the state of the $\overline{\text{SINGLE TONE INHIBIT}}$ input.

$\overline{\text{SINGLE TONE INHIBIT}}$ Input (Pin 15): The $\overline{\text{SINGLE TONE INHIBIT}}$ input is used to inhibit the generation of other than valid tone pairs due to multiple row-column closures. It has a pull-up resistor to V_{DD}, and when left open or tied to V_{DD}, single or dual tones may be generated in accordance with Table II. When forced to V_{SS}, any input situation that would normally result in a single tone will now result in no tone, with all other chip functions operating normally.

TONE OUT (Pin 16): This output is the open emitter of an NPN transistor, the collector of which is connected to V_{DD}. When an external load resistor is connected from TONE OUT to V_{SS}, the output voltage on this pin is the sum of the high and low group sine-waves superimposed on a DC offset. When not generating tones, this output transistor is turned OFF to minimize the device idle current.

Adjustment of the emitter load resistor results in variation of the mean DC current during tone generation, the sine-wave signal current through the output transistor, and the output distortion. Increasing values of load resistance decrease both the signal current and distortion, while increasing the source impedance of the device as seen from its power supply terminals. Note that the DTMF generator is a current source which modulates its own supply terminals in a conventional telephone application.

Functional Description

With no key inputs to the device the oscillator is inhibited, the output transistor is pulled OFF and device current consumption is reduced to a minimum. Key closures are sensed statically to ensure no modulation of the line when tones are not being generated. A valid key closure activates the MUTE output, starts the oscillator and sets the high group and low group programmable counters to the appropriate divide ratio. These counters sequence two ratioed-capacitor D/A converters through a series of 28 equal duration steps per sine-wave cycle. On-chip regulators ensure good stability of tone amplitudes with variations in supply voltage and temperature. The two tones are summed by a mixer amplifier, with pre-emphasis applied to the high group tone. The output is an NPN emitter-follower requiring the addition of an external load resistor to V_{SS}. This resistor facilitates adjustment of the signal current flowing from V_{DD} through the output transistor.

TABLE I. OUTPUT FREQUENCY ACCURACY

Tone Group	Valid Input	Standard DTMF (Hz)	Tone Output Frequency	% Deviation from Standard
Low Group f_L	R1	697	694.8	−0.32
	R2	770	770.1	+0.02
	R3	852	852.4	+0.03
	R4	941	940.0	−0.11
High Group f_H	C1	1209	1206.0	−0.24
	C2	1336	1331.7	−0.32
	C3	1477	1486.5	+0.64
	C4	1633	1639.0	+0.37

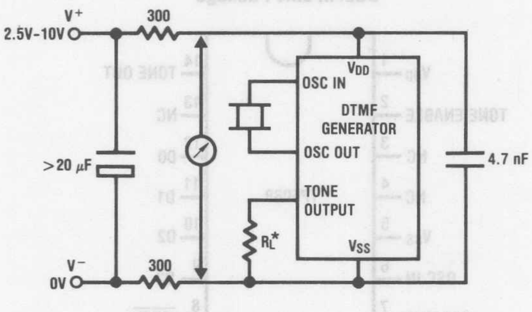
TABLE II. FUNCTIONAL TRUTH TABLE

$\overline{\text{SINGLE TONE INHIBIT}}$	$\overline{\text{TONE DISABLE}}$	ROW	COLUMN	Tones Low	Tones High	$\overline{\text{MUTE}}$
X	0	X	X	0V	0V	0
X	X	O/C	O/C	0V	0V	0
X	1	One	One	f_L	f_H	1
1	1	2 or More	One		f_H	1
1	1	One	2 or More	f_L		1
1	1	2 or More	2 or More	V_{OS}	V_{OS}	1
0	1	2 or More	One	V_{OS}	V_{OS}	1
0	1	One	2 or More	V_{OS}	V_{OS}	1
0	1	2 or More	2 or More	V_{OS}	V_{OS}	1

Note 1: X is don't care state.

Note 2: V_{OS} is the output offset voltage.

Note 3: $\overline{\text{TONE DISABLE}}$ and $\overline{\text{SINGLE TONE INHIBIT}}$ have internal pull-up resistors.



* Adjust R_L for desired tone amplitudes.

FIGURE 2. Amplitude and Distortion Measurements for Conventional Telephone Applications

National Semiconductor

PRELIMINARY

TP5088 DTMF Generator for Binary Input Data

General Description

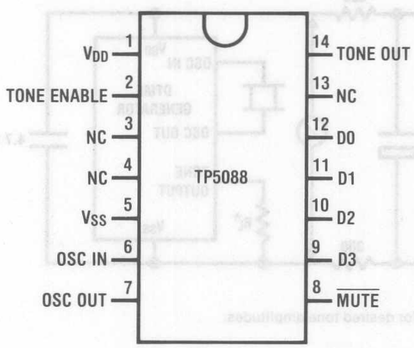
This CMOS device provides low cost tone-dialing capability in microprocessor-controlled telephone applications. Binary data is decoded directly, without the need for conversion to simulated keyboard inputs required by standard DTMF generators. With the TONE ENABLE input low, the oscillator is inhibited and the device is in a low power idle mode. On the low-to-high transition of TONE ENABLE, 4-bit binary data is latched into the device and the selected tone pair is generated. An open-drain N-channel transistor provides a $\overline{\text{MUTE}}$ output during tone generation.

Features

- 2.5V–15V operation
- Direct microprocessor interface
- Binary input data with latches
- Generates 16 standard tone pairs
- On-chip 3.579545 MHz crystal-controlled oscillator
- High-group pre-emphasis
- $\overline{\text{MUTE}}$ output interfaces to speech network
- Low power idle mode

Connection Diagram

Dual-In-Line Package



TOP VIEW

TP9151, TP9152, TP9156, TP9158 Push Button Pulse Dialer Circuits with Redial

General Description

This family of monolithic metal-gate CMOS integrated circuits provides all logic necessary to convert 4×3 matrix keypad inputs into a series of pulses simulating rotary telephone dialing. An on-chip memory capable of storing up to 22 digits allows keypad entries to be made at rates comparable to those of tone-dialing telephones, and provides one-key redial of the last number dialed. For PBX applications, pauses may be inserted in a redialed number sequence to ensure the user waits for dial tone following an access code. Two outputs are provided, requiring simple interface circuits to pulse the telephone line and mute the receiver.

The low voltage and low current requirements of the TP9151 family allow direct telephone-line powered operation.

Features

- 2.3V and 150 μA operation
- < 1 μA on-hook current to store number
- Low power idle mode when not outpulsing
- Stabilized RC oscillator
- < ± 5% frequency stability with voltage and temperature
- 22-digit redial memory
- Single contact or negative-common key interface
- BREAK/MAKE ratio pin selectable (TP9151 and TP9156)
- BREAK/MAKE ratio 60:40 (TP9152)
- BREAK/MAKE ratio 67:33 (TP9158)
- Inter-Digit Pause pin selectable
- Reset delayed for line breaks < 200 ms
- * key inserts pauses
- # key releases redial and pauses
- Scratchpad (new number storage without dialing) option
- Two-phase drive to bistable MUTE relay (TP9152)

Block Diagram

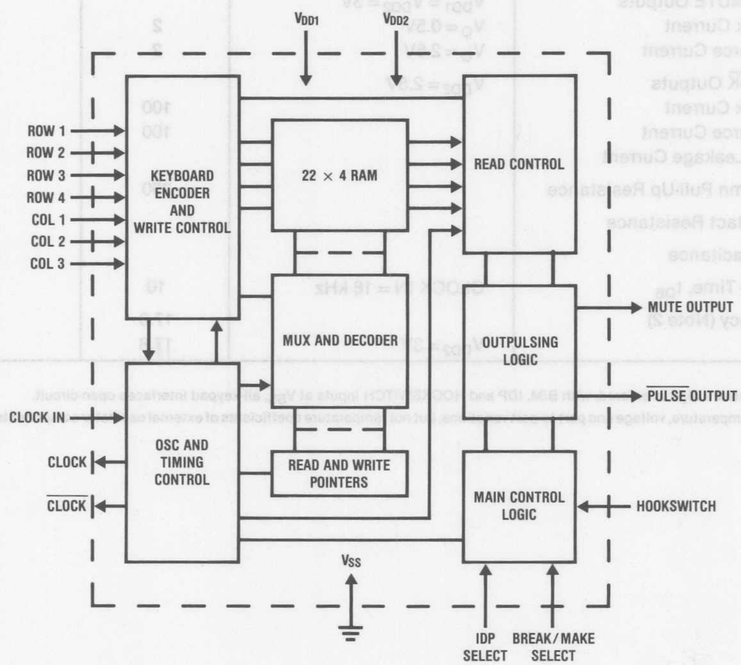


FIGURE 1. TP9151, TP9152, TP9156, TP9158 Pulse Dialer

Voltage on Any Pin	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Operating Temperature Range	−30°C to 70°C
Storage Temperature Range	−50°C to 150°C

Electrical Characteristics

T_A within operating temperature range, $V_{SS} = GND$, $2.3V \le V_{DD1} \le 5V$ except where otherwise stated.

Parameter	Conditions	Min	Typ	Max	Units
Supply Current					
I_{DD1}	$V_{DD1} = V_{DD2} = 5V$			1	μA
I_{DD2} (Note 1)	$V_{DD1} = V_{DD2} = 5V$; Osc On			150	μA
	$V_{DD1} = V_{DD2} = 5V$; Osc Off			2	μA
Inputs					
IDP, B/M, HOOKSWITCH					
Logic 0				0.5	V
Logic 1		$V_{DD2} - 0.5$			V
Outputs					
$\overline{\text{PULSE}}$ Output	$V_{DD1} = V_{DD2} = 3V$				
Logic 0 Sink Current	$V_O = 0.5V$	2			mA
Logic 1 Leakage Current	$V_O = 2.5V$			1	μA
MUTE and $\overline{\text{MUTE}}$ Outputs	$V_{DD1} = V_{DD2} = 3V$				
Logic 0 Sink Current	$V_O = 0.5V$	2			mA
Logic 1 Source Current	$V_O = 2.5V$	2			mA
CLOCK, $\overline{\text{CLOCK}}$ Outputs	$V_{DD2} = 2.5V$				
Logic 0 Sink Current		100			μA
Logic 1 Source Current		100			μA
CLOCK IN Leakage Current				20	nA
Row and Column Pull-Up Resistance		200			kΩ
Keyboard Contact Resistance				1	kΩ
Keyboard Capacitance				30	pF
Key Debounce Time, t_{DB}	CLOCK IN = 18 kHz	10		12	ms
Clock Frequency (Note 2)		17.3		19.1	kHz
	$V_{DD2} = 3V$	17.8		18.9	kHz

Note 1. Measured after a digit is entered, with B/M, IDP and HOOKSWITCH inputs at V_{SS}, all keypad interfaces open-circuit.

Note 2: Including temperature, voltage and part-to-part variations, but not temperature coefficients of external oscillator components. See *Figure 5* for component values.

Connection Diagrams

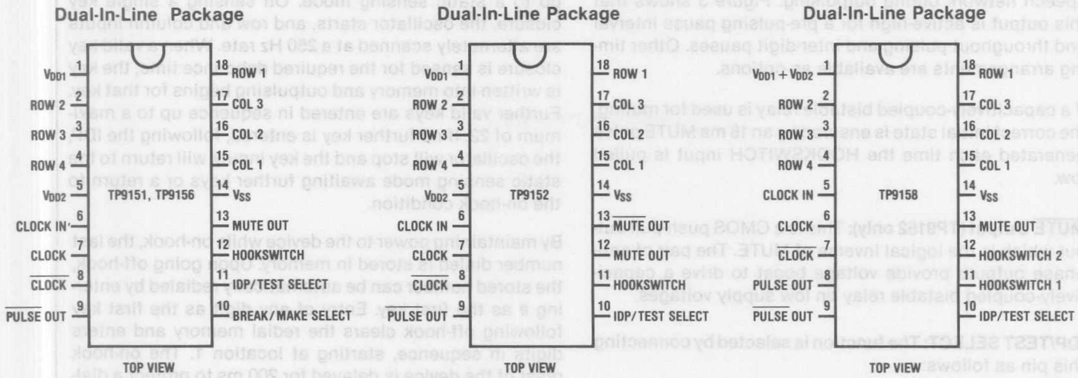


FIGURE 2

Pin Descriptions

V_{SS}: This is the negative supply to the device and the voltages on all other pins are normally referenced to this.

V_{DD1} (common with V_{DD2} on TP9158): This is the positive supply to the redial memory. Maintaining power to this pin while on-hook will store the last number dialed. A low-voltage detect circuit will reset the device and inhibit redial if the voltage on this pin falls too low for the memory cells to retain data.

V_{DD2}: This is the positive supply to all other functions of the device. It may be tied directly to V_{DD1}, or may be disconnected when on-hook in order to reduce on-hook leakage current.

CLOCK IN, CLOCK and $\overline{\text{CLOCK}}$: The clock oscillator consists of two inverters and a comparator requiring two external capacitors and a resistor for oscillation. All timing is referenced to this oscillator running at 18 kHz, typically with $C1 = C2 = 47$ pF and $R = 390$ kΩ. The comparator assures good frequency stability over the operating voltage and temperature ranges.

Keypad Inputs: A valid key entry is defined as either connecting a single row to a single column or connecting V_{SS} simultaneously to a single row and a single column. In the on-hook condition, the keypad interfaces are disabled and pulled low. On entering the off-hook condition, the keypad inputs go to a static sensing mode until a key closure is sensed. The oscillator is then enabled and rows and columns are alternately scanned (pulled high, then low) to verify that the input is valid. The key must then remain valid continuously for the specified debounce time before the circuit will accept and decode it and begin outpulsing.

HOOKSWITCH: This input controls the reset of internal counters and registers. Pulling this pin up to V_{DD1} puts the device in the on-hook condition. The oscillator is stopped, all keypad pins are pulled low and all logic functions inhibited. Taking this pin to V_{SS} resets the device and starts the oscillator to generate an 18 ms MUTE output pulse, then puts the device in standby mode with the oscillator turned off, ready to sense key closures. Returning this input to V_{DD1} at any time starts a 200 ms delayed reset counter. If V_{SS} is restored before 200 ms (as would occur on a short line break) the counter is reset and operation continues. After 200 ms with HOOKSWITCH at V_{DD1} the device returns to the on-hook condition.

A mask option of 300 ms reset delay is available.

The TP9158 bypasses the 200 ms delay reset counter, and provides instead two HOOKSWITCH connections enabling a Schmitt trigger circuit to be made with two external resistors *(Figure 4)*. Reset can then be delayed during a line break by suitable design of the Schmitt trigger threshold.

$\overline{\text{PULSE}}$ Output: This is an open-drain N-channel transistor intended to drive a high-voltage interface circuit to pulse the telephone line with the correct BREAK/MAKE ratio and IDP timing. The output transistor sinks current only during pulse BREAK periods.

PULSE Output (TP9158 only): This is an open-drain P-channel transistor providing the logical inverse of the $\overline{\text{PULSE}}$ output.

Pin Functions (Continued)

MUTE Output: This CMOS push-pull output is intended to drive a simple interface circuit to mute the telephone speech network during outpulsing. *Figure 3* shows that this output is active-high for a pre-pulsing pause interval and throughout pulsing and inter-digit pauses. Other timing arrangements are available as options.

If a capacitively-coupled bistable relay is used for muting, the correct initial state is ensured by an 18 ms MUTE pulse generated each time the HOOKSWITCH input is pulled low.

$\overline{\text{MUTE}}$ Output (TP9152 only): This is a CMOS push-pull output which is the logical inverse of MUTE. The pair of antiphase outputs provide voltage boost to drive a capacitively-coupled bistable relay on low supply voltages.

IDP/TEST SELECT: The function is selected by connecting this pin as follows:

Pin Input	TP9151, TP9152	TP9156	TP9158
V_{DD2}	IDP = 500	900	
V_{SS}	IDP = 800	800	800
CLOCK	IDP = 1000	500	500
$\overline{\text{CLOCK}}$			Fast Test Mode

Note: All IDP times in ms.

The fast test mode bypasses counter stages, increasing the outpulsing speed by a factor of 225, and the keyscan and debounce speed by a factor of 9.

Note that this input is read and latched only during a HOOKSWITCH reset. Also, this input must not be allowed to "float" as no pull-up/pull-down resistor is provided.

BREAK/MAKE SELECT (not on TP9152 or TP9158): The BREAK/MAKE ratio on the TP9151 and TP9156 is selected by connecting this pin as follows:

Pin Input	B/M Ratio
V_{DD2}	67:33 = 2:1
CLOCK	61.5:38.5 = 1.6:1
V_{SS}	60:40 = 1.5:1

On the TP9152 the BREAK/MAKE ratio is internally fixed at 60:40. On the TP9158 the BREAK/MAKE ratio is internally fixed at 67:33. Note that this input is read and latched only during a HOOKSWITCH reset. Also, this input must not be allowed to "float" as no pull-up/pull-down resistor is provided.

Functional Description

The time base for the TP9151 family is derived from an inverter/comparator circuit requiring two external capacitors and one resistor to set the oscillation frequency. The comparator greatly reduces the variation of oscillation frequency with supply voltage and temperature normally associated with CMOS RC oscillators. In the on-hook condition, the oscillator is stopped and the keypad scan disabled.

After going off-hook, the oscillator turns on to generate an 18 ms MUTE reset pulse, then turns off. The keypad inputs go to a static sensing mode. On sensing a single key closure, the oscillator starts, and row and column inputs are alternately scanned at a 250 Hz rate. When a valid key closure is sensed for the required debounce time, the key is written into memory and outpulsing begins for that key. Further valid keys are entered in sequence up to a maximum of 22. If no further key is entered, following the IDP, the oscillator will stop and the key inputs will return to the static sensing mode awaiting further keys or a return to the on-hook condition.

By maintaining power to the device while on-hook, the last number dialed is stored in memory. Upon going off-hook, the stored number can be automatically redialed by entering # as the first key. Entry of any digit as the first key following off-hook clears the redial memory and enters digits in sequence, starting at location 1. The on-hook reset of the device is delayed for 200 ms to protect a dialing sequence against short loop breaks. The device will also reset if V_{DD1} falls to a voltage too low for the memory cells to retain data.

The * key enables the user to enter and store a pause in a manually dialed number sequence. Both manual and automatic dialing will stop on reaching this pause. The # key will release the pause and allow outpulsing to continue. Pauses may be stored in any memory location, but the number of pauses plus digits cannot exceed 22. Each pause requires a # entry to release it.

As a mask option, the * key can be set up to provide entry to the Scratchpad feature, which allows the memory to be overwritten with a new telephone number without that number being outpulsed and without muting. Scratchpad mode can be entered directly after going off-hook or during a conversation by keying ** followed by the next desired number. The new number can only be outpulsed by returning on-hook, then off-hook, followed by the # key, which will redial the stored number as normal. Selecting the Scratchpad option still provides pause storage with a * entry, provided the next key is a digit.

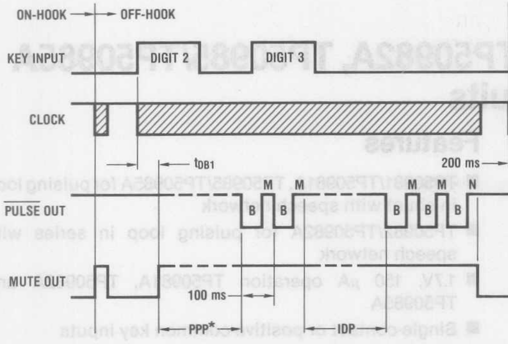
Various timing options are available for $\overline{\text{PULSE}}$ and MUTE outputs. Popular BREAK/MAKE ratios and Inter-Digit Pause periods can be pin-selected.

Application Notes

The TP9151 pulse dialer family may be set up to drive a pulsing loop either in series or in shunt with the speech network. A typical series dialer is shown in *Figure 5*. In this circuit, the dialer is fed from a current-limited source of a minimum of 200 μA to allow a safe margin for the device, plus the zener and HOOKSWITCH resistor currents.

To take maximum advantage of the low current consumption of the TP9151 family, particularly in the on-hook, last-number-stored mode, all other current paths must be minimized. These include leakage of the decoupling capacitor and reverse leakage of current through the current source to ground via the speech network. A zener diode with very low leakage current below the conduction "knee" should be specified. If on-hook current is drawn from the telephone line, reverse leakage of the two back-biased diodes in the rectifier bridge must also be considered.

Application Notes (Continued)



* PPP = pre-pulsing pause, normally the same as the IDP. Other delays available as mask options.

FIGURE 3. Outpulse Timing

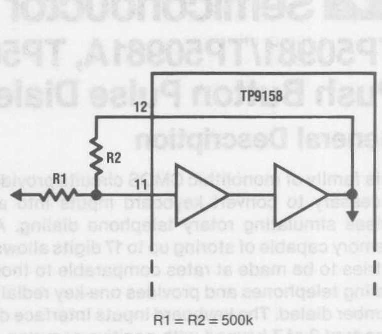
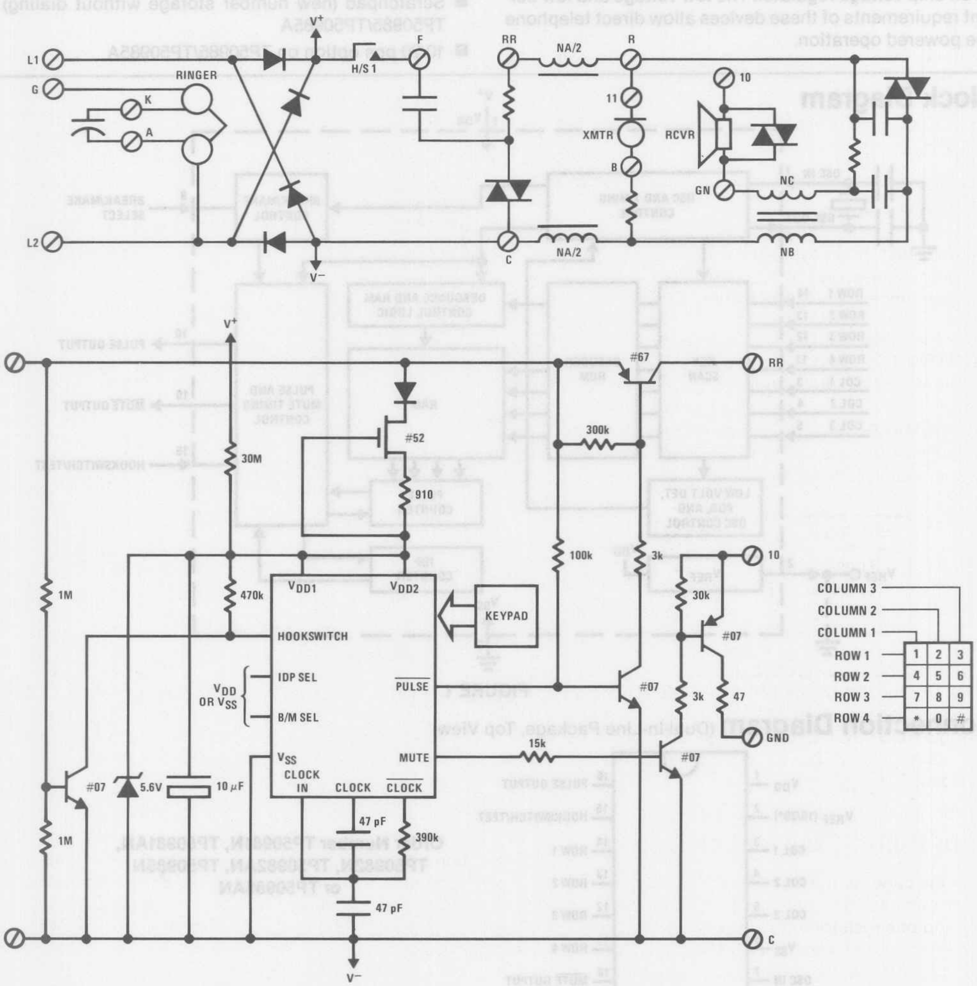


FIGURE 4. TP9158 Schmitt Trigger Reset



# indicates National Semiconductor Discrete Process number.

FIGURE 5. Typical Series Dialer Application

TP50981/TP50981A, TP50982/TP50982A, TP50985/TP50985A Push Button Pulse Dialer Circuits

General Description

This family of monolithic CMOS circuits provides all logic necessary to convert keyboard inputs into a series of pulses simulating rotary telephone dialing. An on-chip memory capable of storing up to 17 digits allows keyboard entries to be made at rates comparable to those of tone-dialing telephones and provides one-key redial of the last number dialed. The keyboard inputs interface directly to a standard 2-of-7 keypad with positive-common or an inexpensive form A-type keyboard. Two outputs, one for pulsing the telephone line and one to mute the receiver, are provided along with pin selectable Break/Make ratios and an on-chip voltage regulator. The low voltage and low current requirements of these devices allow direct telephone line powered operation.

Features

- TP50981/TP50981A, TP50985/TP50985A for pulsing loop in shunt with speech network
- TP50982/TP50982A for pulsing loop in series with speech network
- 1.7V, 150 μA operation TP50981A, TP50982A and TP50985A
- Single-contact or positive-common key inputs
- Break/Make ratio pin selectable
- On-chip voltage regulator
- On-chip oscillator using 480 kHz ceramic resonator
- Scratchpad (new number storage without dialing) on TP50985/TP50985A
- 10/20 pps option on TP50985/TP50985A

Block Diagram

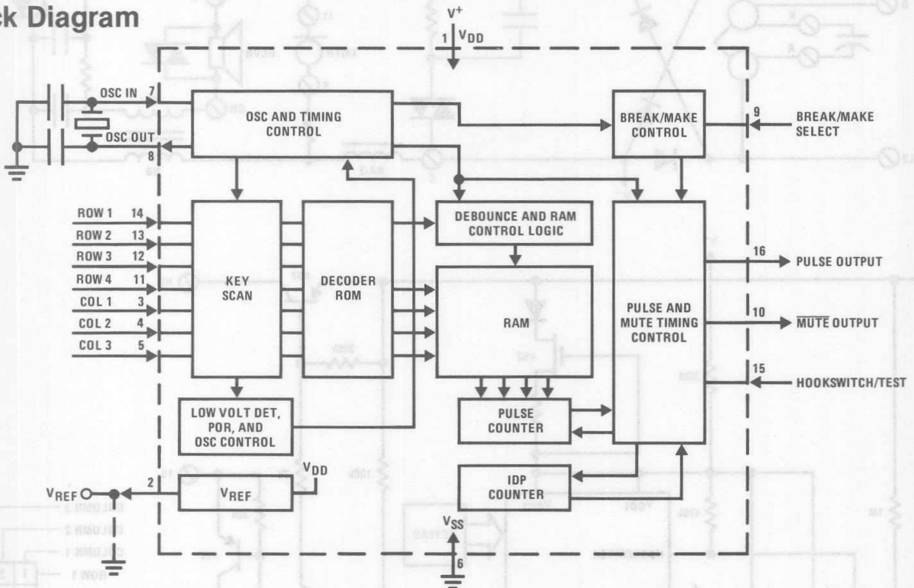
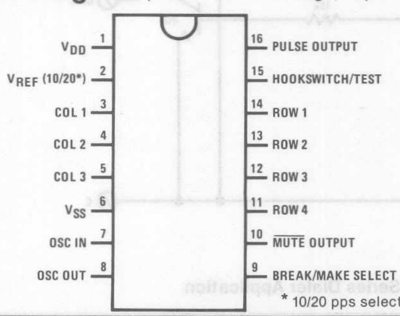


FIGURE 1

Connection Diagram (Dual-In-Line Package, Top View)



* 10/20 pps select input on TP50985/TP50985A

Order Number TP50981N, TP50981AN, TP50982N, TP50982AN, TP50985N or TP50985AN

Absolute Maximum Ratings

DC Supply Voltage (V_{DD}–V_{SS})	6.2V
Voltage on Any Pin	V_{DD} + 0.3V to V_{SS} – 0.3V
Operating Temperature	– 30°C to + 70°C
Storage Temperature	– 55°C to + 150°C
Maximum Power Dissipation (25°C)	500 mW

DC Electrical Characteristics

T_A within operating temperature range, V_{DD} min $\leq V_{DD} \leq$ 6.0V, unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
V_{DD} Min DC Supply Voltage					
TP50981, TP50982, TP50985	Pin 1 Ref. Pin 6	2.5			V
TP50981A; TP50982A, TP50985A		1.7			V
Memory Retention Current					
TP50981, TP50982, TP50985	V_{DD} = 2.5V, Notes 1 and 2		0.7	2.4	μA
TP50981A, TP50982A, TP50985A	V_{DD} = 1.7V, Notes 1 and 2		0.5	1.0	μA
DC Operating Current	Off-Hook, Valid Key, V_{REF} Tied to V_{SS}		100	150	μA
V_{REF} Sink Current	V_{DD} = 5.0V	1.0			mA
$\overline{\text{MUTE}}$ Sink Current	V_{DD} = V_{DD} Min, V_o = 0.5V	0.5	2.0		mA
PULSE Sink Current	V_{DD} = V_{DD} Min, V_o = 0.5V	1.0	4.0		mA
$\overline{\text{MUTE}}$ and PULSE Leakage	V_{DD} = 6.0V, V_o = 6.0V		0.001	1.0	μA
Keyboard Contact Resistance				1.0	kΩ
Keyboard Capacitance				30	pF
Logic '0' Level Input		V_{SS}		0.2 V_{DD}	V
Logic '1' Level Input		0.8 V_{DD}		V_{DD}	V
Keyboard Pull-Up Resistance			4.0		kΩ
Keyboard Pull-Down Resistance			100		kΩ
HOOKSWITCH Pull-Up Resistance			100		kΩ

Note 1: On-hook mode, V_{REF} tied to V_{SS}, all outputs open.

Note 2: Power-on reset and low-voltage-detect circuits inhibit the redial function if the supply voltage falls below V_{DD} Min.

AC Electrical Characteristics

T_A within operating temperature range, V_{DD} min $\leq V_{DD} \leq$ 6.0V, unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Oscillator Frequency	Anti-Resonant Mode		480		kHz
Keyboard Debounce Time	OSC IN = 480 kHz	9		11	ms
Oscillator Start-Up Time	V_{DD} = V_{DD} Min		5.0		ms
Pulse Rate			10.0		pps
Break Time	Pin 9 @ V_{DD}		61.0		ms
	Pin 9 @ V_{SS}		67.0		ms
Interdigit Pause			800		ms

Functional Description

The time base for this family of pulse dialers is derived from a 480 kHz ceramic resonator in anti-resonant mode. In the on-hook condition, the oscillator is stopped and all keyboard row and column inputs are forced to V_{DD} which inhibits any key closures from effecting the circuit. After going off-hook the oscillator remains off and the keyboard inputs go to a static sensing mode. Upon sensing a single key closure, the oscillator starts, and the row and column inputs are alternately scanned at a 500 Hz rate. When the circuit senses a valid key closure for the required debounce time, the key is written into memory and outpulsing begins for that key. Further valid keys are entered in sequence, provided that no more than 17 digits remain to be outpulsed. If no further key is entered, following the IDP the oscillator will stop and the key inputs will return to the static sensing mode awaiting further keys or a return to the on-hook condition. By maintaining power to the device while on-hook, the last number dialed (up to 17 digits) is stored in the memory. On going off-hook (HOOKSWITCH goes to V_{SS}) the stored number can be automatically redialed by entering either * or # as the first key (TP50981/TP50981A and TP50982/TP50982A). Entry of any digit as the first key following off-hook clears the redial memory and enters digits in sequence, starting at location 1.

The * key on the TP50985/TP50985A is redefined to provide entry to the Scratchpad feature. This mode allows the outpulsing memory to be overwritten with a new telephone number without that number being outpulsed. Scratchpad mode can be entered directly after going off-hook or during a conversation by keying * followed by the next desired number. The new number can only be outpulsed by returning on-hook, then off-hook followed by the # key, which will redial the last number as normal.

The TP50985/TP50985A also enables the user to select an output pulse rate of either 10 pps by connecting pin 2 to ground or 20 pps by connecting pin 2 to V_{DD}. On this version V_{REF} is connected to V_{SS} internally.

In the on-hook condition [HOOKSWITCH/TEST (pin 15) connected to V_{DD}] the keyboard inputs are disabled and pulled high. Upon entering the off-hook condition the keyboard inputs go to a static sensing mode until a key closure is sensed. The oscillator is then enabled and the rows and columns are alternately scanned (pulled high, then low) to verify that the input is valid. The key must then remain valid continuously for the specified debounce time before the circuit will accept and decode it and begin outpulsing.

Pin Descriptions

V_{DD} (pin 1): This is the positive supply to the device and is referenced to V_{SS} (pin 6). The voltage on this pin must be limited to less than 6V either externally or by current-limiting the supply to the on-chip voltage regulator. In the last-number-stored mode a minimum of 1 μA of supply current must be available to this pin while on-hook.

V_{REF} (pin 2): In normal applications, this pin is tied to V_{SS} (pin 6) which enables the on-chip voltage regulator circuit. When V_{REF} is tied to V_{SS}, the voltage regulator will provide a current sink from V_{DD} to V_{SS} of a minimum of 1 mA with V_{DD} equal to 5V.

KEYBOARD INPUTS (pins 3, 4, 5, 11, 12, 13, and 14): A valid key entry is defined as either connecting a single row to a single column or connecting V_{DD} simultaneously to a single row and a single column. This allows direct interface to an inexpensive single-contact (form A) keyboard, the standard 2-of-7 keyboard with positive-common, or logic-generated inputs.

V_{SS} (pin 6): This is the negative supply.

OSCILLATOR IN, OUT (pins 7, 8): The device contains an on-chip oscillator circuit designed to work with a 480 kHz ceramic resonator (anti-resonant mode) and 2 external capacitors, normally 100 pF. A 1 MΩ resistor is included on-chip for good oscillator stability. The circuit may also be driven with an external 480 kHz source on OSCILLATOR IN (pin 7).

BREAK/MAKE SELECT (pin 9): The Break/Make ratio is selected by connecting pin 9 to either V_{DD} or V_{SS}. Table I indicates the available ratios.

TABLE I. BREAK/MAKE SELECT

Input to BREAK/MAKE (pin 9)	PULSE OUTPUT Break	Make
V_{DD}	61%	39%
V_{SS}	67%	33%

$\overline{\text{MUTE}}$ (pin 10): This pin is the output of an open-drain N-channel transistor. It drives a simple interface circuit to mute the receiver during outpulsing. See the timing diagram and application notes for further information concerning this output.

HOOKSWITCH/TEST (pin 15): This input has a 100 kΩ internal pull-up resistor to V_{DD}. Allowing this pin to float, or connecting a V_{DD} level puts the circuit in the on-hook idle mode.

With this pin connected to V_{SS} the circuit is in the off-hook mode and will accept keyboard inputs, and outpulse them at the normal 10 pps rate. When the outpulsing is complete, the oscillator stops and waits for further key inputs. If, however, pin 15 is taken to V_{DD} while the circuit is still outpulsing the remaining digits will be outpulsed at 100 times the normal rate (BREAK/MAKE becomes 50%). This allows for rapid testing of the device and also provides a means for resetting the circuit if power to the device is maintained while on-hook. (Note: Taking the worst-case of 17 zeros remaining to be outpulsed, this operation could take 300 ms to complete. Therefore, to ensure that the circuit has been properly reset, pin 15 should remain at V_{DD} for more than 300 ms before entering a new number.)

PULSE OUTPUT (pin 16): The pulse output consists of an open-drain N-channel transistor. It is intended to drive a transistor interface circuit to pulse the telephone line with the correct Break/Make ratio, IDP timing, and pulse rate. On the TP50981/TP50981A, TP50985/TP50985A this output is normally low and pulses high. On the TP50982/TP50982A the output is normally high and pulses low. See *Figure 2* for further details of the timing differences between the parts.

Timing Diagram

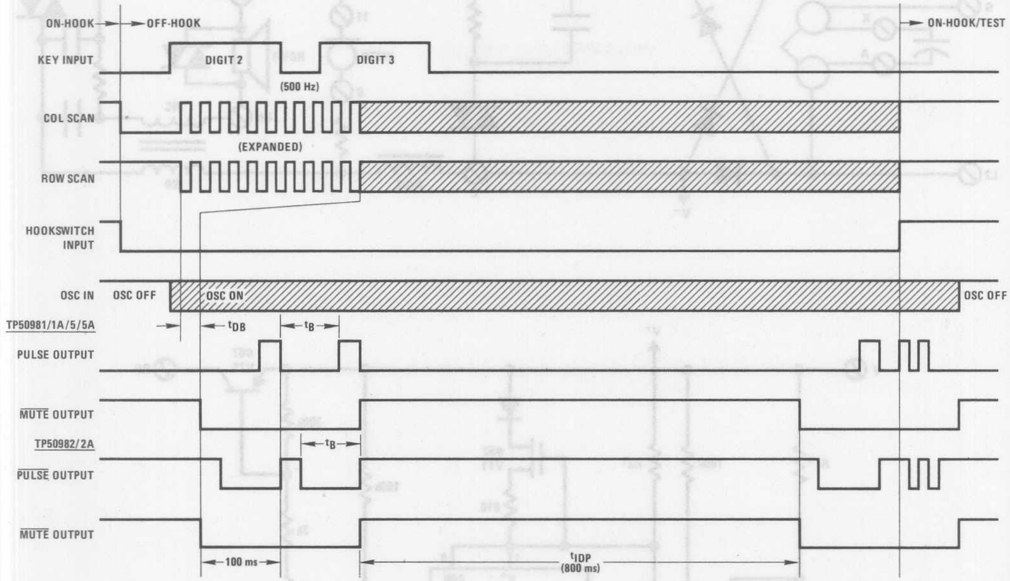


FIGURE 2

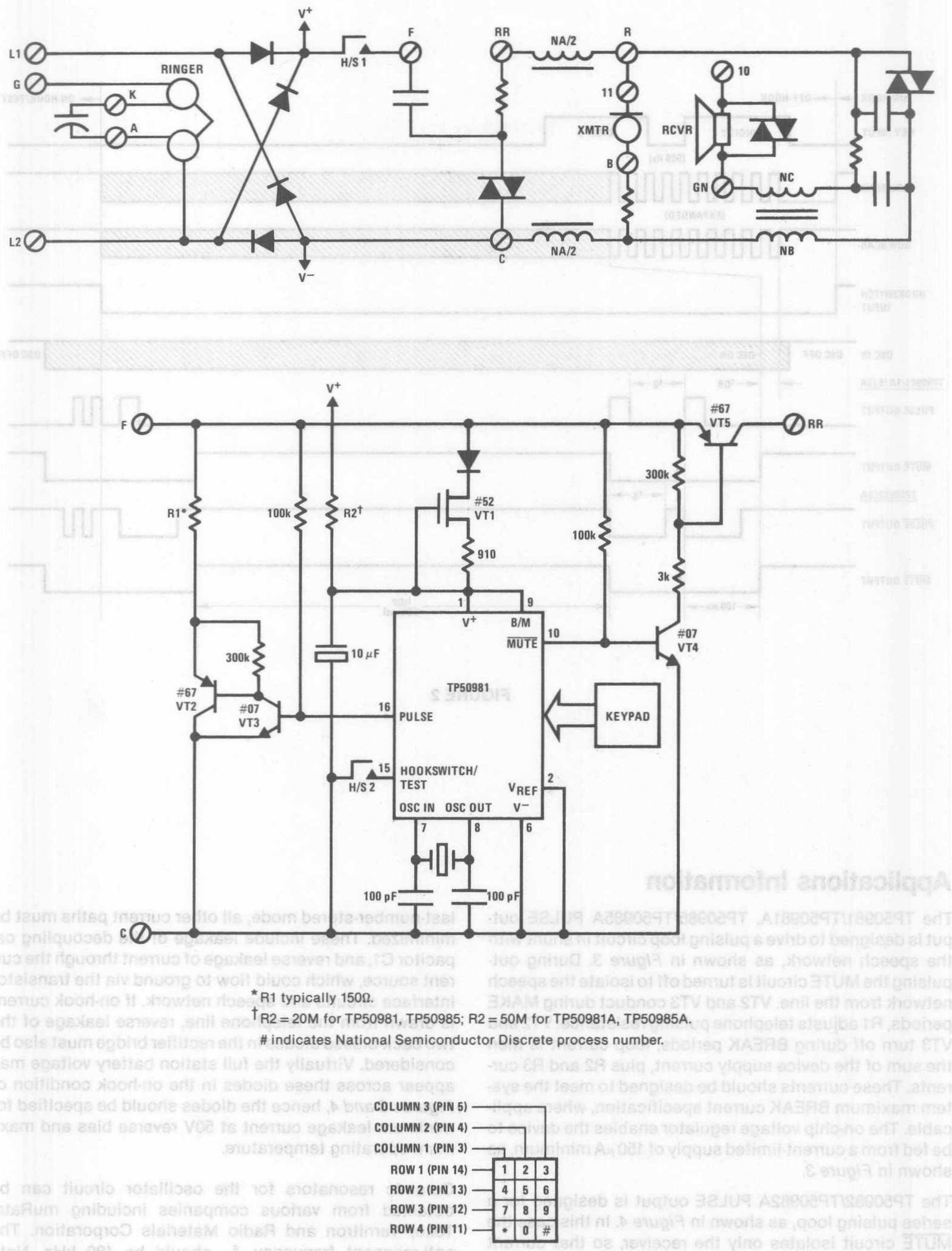
Applications Information

The TP50981/TP50981A, TP50985/TP50985A PULSE output is designed to drive a pulsing loop circuit in shunt with the speech network, as shown in *Figure 3.* During outpulsing the MUTE circuit is turned off to isolate the speech network from the line. VT2 and VT3 conduct during MAKE periods, R1 adjusts telephone pulsing resistance. VT2 and VT3 turn off during BREAK periods, loop current is then the sum of the device supply current, plus R2 and R3 currents. These currents should be designed to meet the system maximum BREAK current specification, where applicable. The on-chip voltage regulator enables the device to be fed from a current-limited supply of 150 μA minimum, as shown in *Figure 3.*

The TP50982/TP50982A PULSE output is designed for a series pulsing loop, as shown in *Figure 4.* In this case the $\overline{\text{MUTE}}$ circuit isolates only the receiver, so that current flows through the speech network while outpulsing MAKE periods. VT3 cuts off this current during BREAK periods.

To take maximum advantage of the low current consumption of the TP50981A, TP50982A, TP50985A in the on-hook, last-number-stored mode, all other current paths must be minimized. These include leakage of the decoupling capacitor C1, and reverse leakage of current through the current source, which could flow to ground via the transistor interface circuits and speech network. If on-hook current is drawn from the telephone line, reverse leakage of the two back-biased diodes in the rectifier bridge must also be considered. Virtually the full station battery voltage may appear across these diodes in the on-hook condition of *Figures 3 and 4,* hence the diodes should be specified for minimum leakage current at 50V reverse bias and maximum operating temperature.

Ceramic resonators for the oscillator circuit can be obtained from various companies including muRata, Toko, Vernitron and Radio Materials Corporation. The anti-resonant frequency, f_a, should be 480 kHz. Note that resonators are often referred to by their resonant frequency, f_r, which is typically 15 kHz–25 kHz lower than f_a. Consult manufacturers' data for specifications and tolerances.



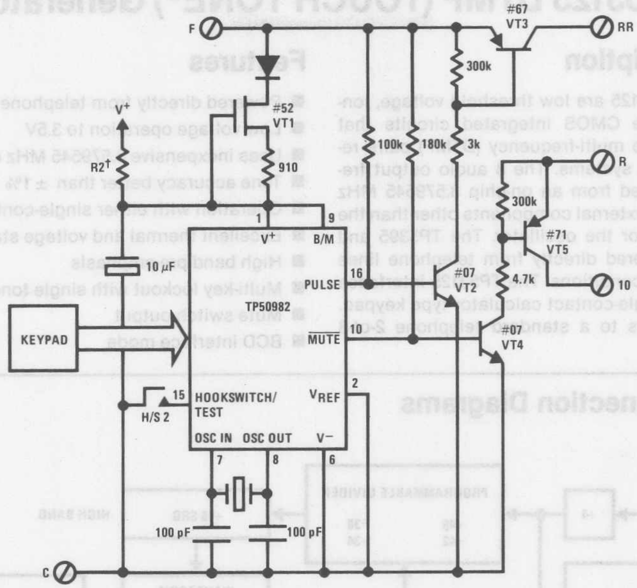
*R1 typically 150Ω.

†R2 = 20M for TP50981, TP50985; R2 = 50M for TP50981A, TP50985A.

# indicates National Semiconductor Discrete process number.

FIGURE 3. TP50981, TP50985 Shunt Dialer Application

Applications Information (Continued)



†R2 = 20M for TP50982, R2 = 50M for TP50982A

FIGURE 4. TP50982 Series Dialer Application

National Semiconductor

TP5395, TP53125 DTMF (TOUCH TONE®) Generators

General Description

The TP5395 and TP53125 are low threshold voltage, ion-implanted, metal-gate CMOS integrated circuits that generate all dual tone multi-frequency (DTMF) pairs required in tone-dialing systems. The 8 audio output frequencies are generated from an on-chip 3.579545 MHz master oscillator. No external components other than the crystal are required for the oscillator. The TP5395 and TP53125 can be powered directly from telephone lines over wide range loop conditions. The TP53125 interfaces to an inexpensive single-contact calculator type keypad. The TP5395 interfaces to a standard telephone 2-of-8 keypad.

Features

- Powered directly from telephone line
- Low voltage operation to 3.5V
- Uses inexpensive 3.579545 MHz crystal
- Tone accuracy better than ±1% without tuning
- Operation with either single-contact or 2-of-8 keypads
- Excellent thermal and voltage stability
- High band pre-emphasis
- Multi-key lockout with single tone capability
- Mute switch output
- BCD interface mode

Block and Connection Diagrams

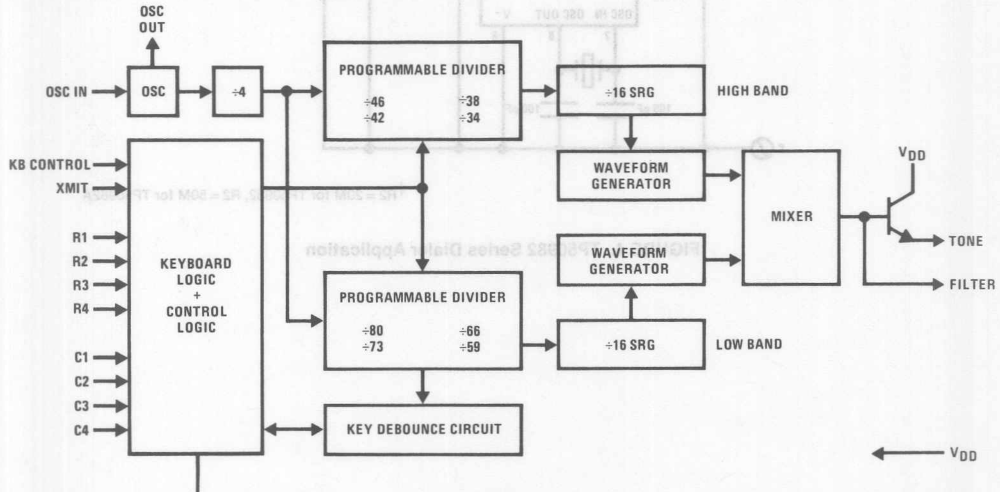


FIGURE 1a

Dual-In-Line Package

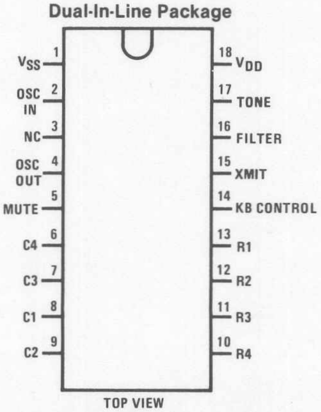


FIGURE 1b

TOUCH TONE® is a registered trademark of Bell Telephone

Absolute Maximum Ratings

Voltage at Any Pin	$V_{SS}-0.3V$ to $V_{DD}+0.3V$
Operating Temperature Range	$-30°C$ to $+70°C$
Storage Temperature Range	$-55°C$ to $+150°C$
$V_{DD}-V_{SS}$	6.5V
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

T_A within operating temperature range, $3.5V \le V_{DD}-V_{SS} \le 6V$, unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Input Pull-Up Resistor at Column Inputs	$V_{IN}=V_{SS}$	100		400	kΩ
Input Pull-Down Resistor at XMIT	$V_{IN}=V_{DD}$	100		400	kΩ
Internal Resistor at Row Inputs					
To V_{DD} (TP5395)	$V_{IN}=V_{SS}$	100		400	kΩ
To V_{SS} (TP53125)	$V_{IN}=V_{DD}$	100		400	kΩ
Keypad Contact Resistance				1	kΩ
Input Voltage Levels					
Logical "1"		$V_{DD}-0.25$		V_{DD}	V
Logical "0"		V_{SS}		$V_{SS}+0.25$	V
Output Voltage Swings at TONE OUTPUT	$V_{DD}-V_{SS}=3.5V$, $R_L \ge 500\Omega$				
Low Band Only			820		mVp-p
High Band Only			1000		mVp-p
High Band Pre-Emphasis			2		dB
Harmonic Distortion	$R_L \ge 500\Omega$				
	No External Filtering		−19		dB
	With 1000 pF at Filter		−27		dB
Tone Frequency Deviation				1.0	%
Operating Frequency			3.579545		MHz
Key Debounce Time			2	4	ms
Power Dissipation	$V_{DD}-V_{SS}=6V$, $R_L=500\Omega$			50	mW
Output Current Level at MUTE	$V_{DD}-V_{SS}=3.5V$				
Logical "1"	$V_{OUT}=V_{DD}-0.2V$	20			μA
Logical "0"	$V_{OUT}=V_{SS}+0.5V$	2.0			mA

Functional Description

A functional block diagram of the TP5395 (or TP53125) is shown in *Figure 1a,* and a connection diagram is shown in *Figure 1b.* The oscillator will start immediately upon power being applied. When a key is pressed, both output tones start from zero on the negative half cycle after a 2 ms to 4 ms key debounce period. If 2 or more keys are pressed together, one or both tones will be switched OFF according to the functional truth table, *Figure 2a.* Output frequencies and accuracies are shown in *Figure 2b.*

The KB CONTROL input is used to change the interface from keyboard to BCD according to *Figure 3.* In the BCD interface mode, tone pairs are generated corresponding to the input BCD code on the row inputs *(Figure 4)* and are enabled during the period XMIT is high. By appropriate use of the column inputs during this mode, individual tones can be generated for test or signaling purposes.

A MUTE output is provided to electronically control common key functions such as switching out the transmitter and switching a muting resistor to the receiver.

The sum of the 2 sine waves is provided at the TONE output. A FILTER connection is available for access to the base of the output emitter follower for efficient filtering of the output waveform. A 500 pF capacitor produces a total harmonic distortion 20 dB below the in-band power without degrading high band pre-emphasis for operation in the North American telephone system. The TONE output signal amplitude varies directly with the V_{DD} supply. Using a zener diode to clamp this supply near the low end of the line variation and the output circuits shown in *Figures 5 and 6* generates a line current signal amplitude that will remain constant with line voltage variations. Typical performance of this circuit is shown in *Figure 7.* In order to

quency components at 10 kHz and above the output, additional external filtering is required as shown in *Figure 8.*

row and column connections for both types of keypads. Timing waveforms are shown in *Figure 10.*

Row	Column	Low Band	High Band
None	None	DC	DC
One	One	f_L	f_H
None	One	DC	f_H
One	None	f_L	DC
Two or more	None	DC	DC
Two or more	One	DC	f_H
None	Two or more	DC	DC
One	Two or more	f_L	DC
Two or more	Two or more	DC	DC

a. Functional Truth Table

Inputs	Desired Frequencies		Actual Frequency (Hz)	Percent Deviation
	f_L (Hz)	f_H (Hz)		
R1	697	—	699.1	0.306
R2	770	—	766.2	−0.497
R3	852	—	847.4	−0.536
R4	941	—	948.0	0.741
C1	—	1209	1215.9	0.569
C2	—	1336	1331.7	−0.324
C3	—	1477	1471.9	−0.35
C4	—	1633	1645.0	0.736

b. Output Frequencies

FIGURE 2. Keypad Interface Mode

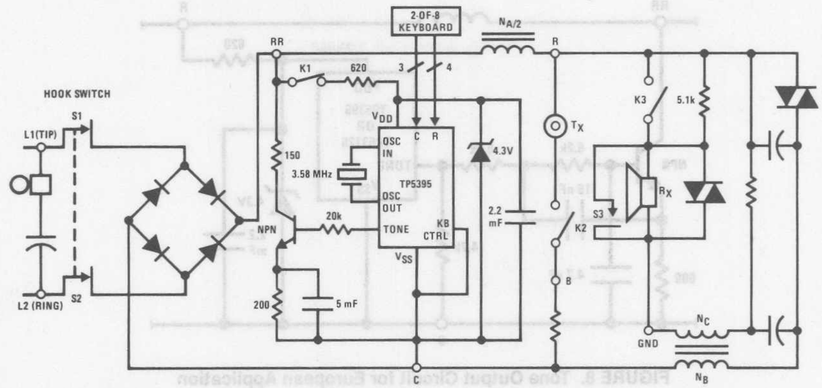
KB CONTROL	XMIT	Interface Mode
0	Open	Keypad
1	0	Idle
1	1	Send tones

FIGURE 3. Interface Mode Control

XMIT	C1	C2	R1	R2	R3	R4	Frequencies Generated	
							f_L (Hz)	f_H (Hz)
0	X	X	X	X	X	X	DC	DC
1	Open	Open	0	0	0	0	941	1336
1	Open	Open	0	0	0	1	697	1209
1	Open	Open	0	0	1	0	697	1336
1	Open	Open	0	0	1	1	697	1447
1	Open	Open	0	1	0	0	770	1209
1	Open	Open	0	1	0	1	770	1336
1	Open	Open	0	1	1	0	770	1477
1	Open	Open	0	1	1	1	852	1209
1	Open	Open	1	0	0	0	852	1336
1	Open	Open	1	0	0	1	852	1477
1	0	Open	Valid BCD Inputs				f_L	DC
1	Open	0	Valid BCD Inputs				DC	f_H
1	0	0	Valid BCD Inputs				DC	DC

FIGURE 4. Functional Truth Table for Signal Interface Mode

Functional Description (Continued)



Note 1: All S switches are common with hookswitch.

Note 2: All K switches are common with KB.

Note 3: Switches shown in OFF hook and KB depressed positions.

FIGURE 5. TP5395 Typical Application

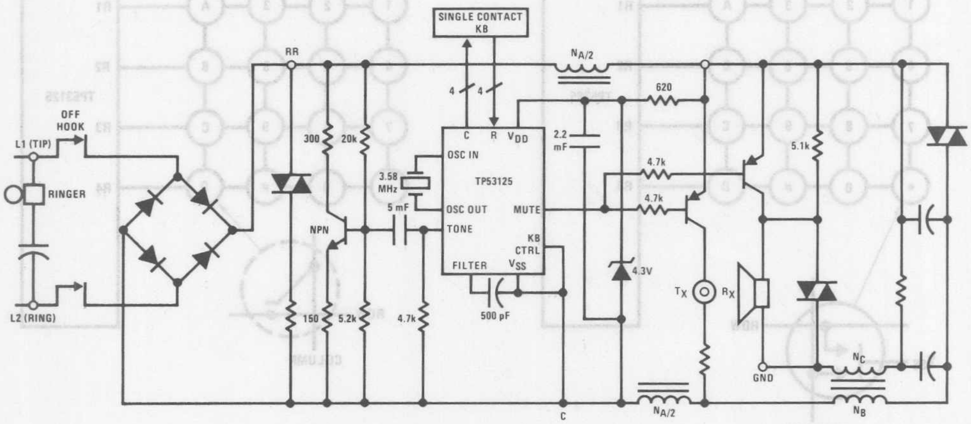


FIGURE 6. TP53125 Typical Application

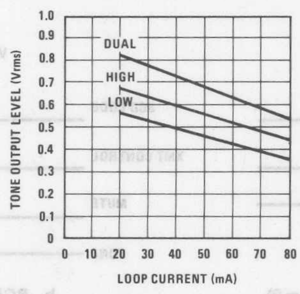


FIGURE 7. Typical Tone Output vs Loop Current

Functional Description (Continued)

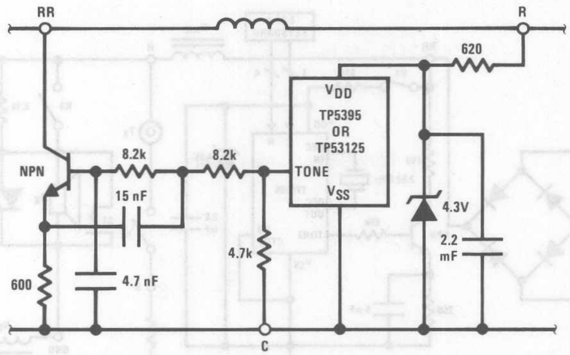
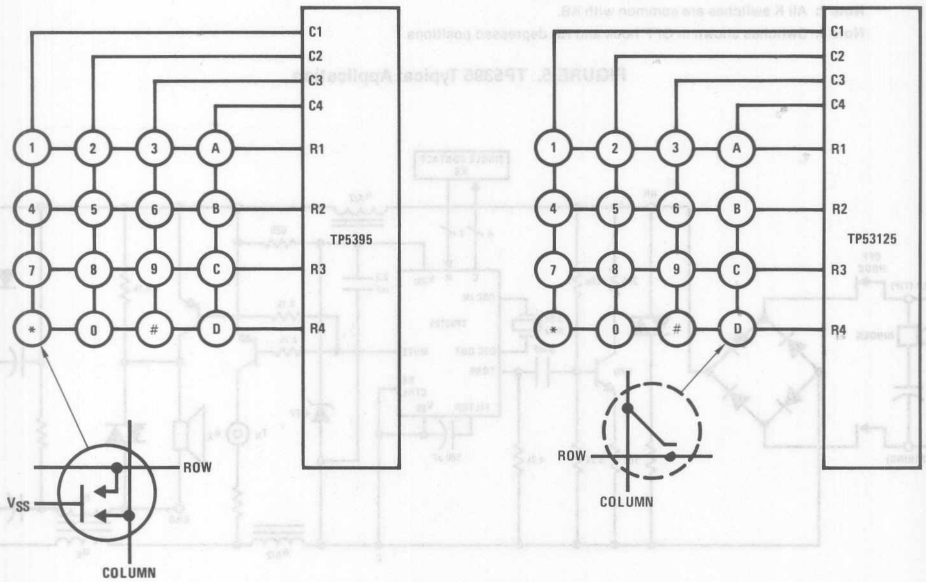


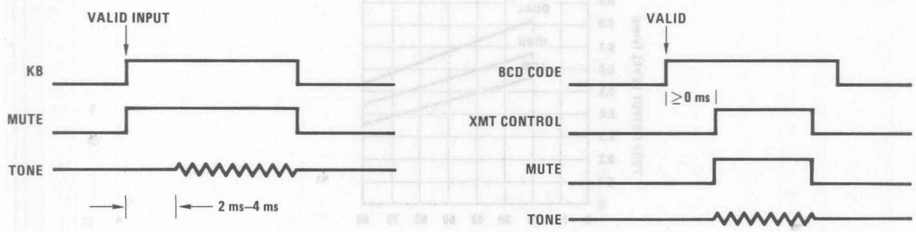
FIGURE 8. Tone Output Circuit for European Application



a. Standard Telephone Keypad

b. Single Contact Keypad

FIGURE 9. Keypad Interconnection Diagrams



a. Keyboard Mode (KB CONTROL = 0)

b. BCD Mode (KB CONTROL = 1)

FIGURE 10

National Semiconductor

TP5393, TP5394, TP53143, TP53144 Pushbutton Pulse Dialer Circuits

General Description

The TP5393, TP5394, TP53143 and TP53144 are low threshold voltage, ion-implanted, metal-gate CMOS integrated circuits that convert pushbutton inputs into a series of pulses to simulate a telephone rotary dial. Pushbutton inputs require the use of a simple, low cost single contact calculator type keypad. An inexpensive RC oscillator network is used as the frequency reference. Storage is provided for 21 digits. A redial feature via use of the # key is included. An interdigit pause can be externally selected as either 420 ms or 840 ms. A mute output is provided to mute receiver noise during outpulsing. No muting occurs during the interdigit pause, thereby allowing the user to hear any busy or error condition arising during the call. The TP5393 and TP53143 provide a pacifier tone of 600 Hz every time a key is depressed. The TP5393 and TP5394 provide a 1.6:1 break/make ratio. The TP53143 and TP53144 provide a 2:1 break/make ratio.

Features

- Direct line powered operation
- Low voltage operation to 2V
- Low cost RC oscillator
- Single contact keypad
- 21-digit storage
- Selectable interdigital pause
- Redial of last number
- 600 Hz tone (available in TP5393 and TP53143)

Block Diagram

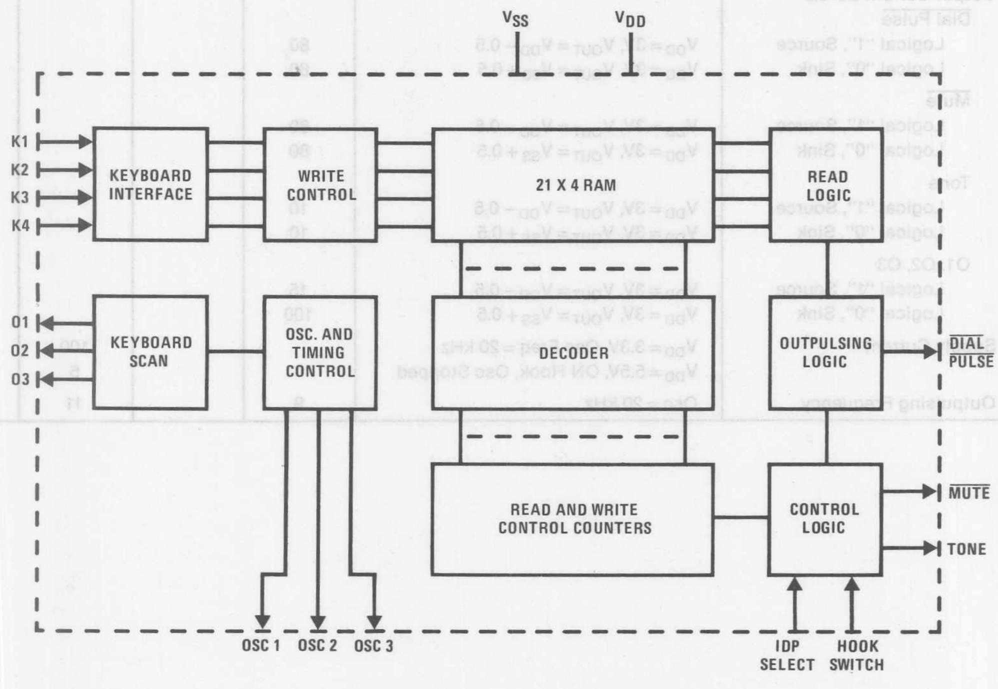


FIGURE 1

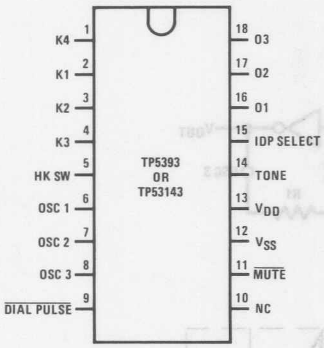
Voltage at Any Pin	$V_{SS}-0.3V$ to $V_{DD}+0.3V$
Operating Temperature Range	$-30°C$ to $+70°C$
Storage Temperature Range	$-55°C$ to $+150°C$
$V_{DD}-V_{SS}$	6.5V Max
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics T_A within operating temperature range, $V_{SS}=GND$, $2V \le V_{DD} \le 5.5V$

Parameter	Conditions	Min	Typ	Max	Units
Input Voltage Levels at IDP Select, HK SW, K1–K4					
Logical "1"		$V_{DD}-0.25$		V_{DD}	V
Logical "0"		V_{SS}		$V_{SS}+0.25$	V
Input Pull-Up Resistor Currents at K1–K4, Source	$V_{DD}=3V$, $V_{IN}=V_{SS}$		1	3	μA
Input Pull-Down Resistor Current at HK SW, Sink	$V_{DD}=3V$, $V_{IN}=3V$		1.5	3	μA
Keypad Contact Resistance				1	kΩ
Output Current Levels					
$\overline{\text{Dial Pulse}}$					
Logical "1", Source	$V_{DD}=3V$, $V_{OUT}=V_{DD}-0.5$	80			μA
Logical "0", Sink	$V_{DD}=3V$, $V_{OUT}=V_{SS}+0.5$	80			μA
$\overline{\text{Mute}}$					
Logical "1", Source	$V_{DD}=3V$, $V_{OUT}=V_{DD}-0.5$	80			μA
Logical "0", Sink	$V_{DD}=3V$, $V_{OUT}=V_{SS}+0.5$	80			μA
Tone					
Logical "1", Source	$V_{DD}=3V$, $V_{OUT}=V_{DD}-0.5$	10			μA
Logical "0", Sink	$V_{DD}=3V$, $V_{OUT}=V_{SS}+0.5$	10			μA
O1, O2, O3					
Logical "1", Source	$V_{DD}=3V$, $V_{OUT}=V_{DD}-0.5$	15			μA
Logical "0", Sink	$V_{DD}=3V$, $V_{OUT}=V_{SS}+0.5$	100			μA
Supply Current	$V_{DD}=3.3V$, Osc Freq = 20 kHz			100	μA
	$V_{DD}=5.5V$, ON Hook, Osc Stopped			5	μA
Outpulsing Frequency	Osc = 20 kHz	9		11	Hz

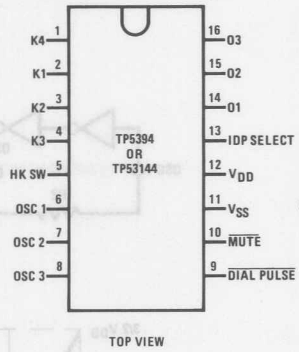
Connection Diagrams

Dual-In-Line Package



Order Number TP5393J or TP53143J See NS Package J18A

Dual-In-Line Package



Order Number TP5394J or TP53144J See NS Package J16A

FIGURE 2

Functional Description

A block diagram of the TP5393, TP5394, TP53143 and TP53144 integrated circuit is shown in *Figure 1* and package connection diagrams for the 2 package options are shown in *Figure 2.*

Oscillator (Pins 6, 7, and 8): The time base for the pulse dialer integrated circuit is an RC-controlled oscillator like that shown in *Figure 3*, typically tuned to 20 kHz by the R1 and C1 combination. Stability of ±10% of typical frequency can be maintained over the voltage range 3.0V–5.5V and temperature range −30°C to +70°C. At fixed voltage and temperature, part to part variation is less than 5%.

This clock is successively divided to derive the necessary timing for outpulsing and interdigit pause.

Keyboard (Pins 1–4 and 16–18 or 14–16): The TP5393, TP5394, TP53143 and TP53144 utilize an inexpensive single contact (Form A, *Figure 7*) keypad. A valid key closure is recorded when a single row (K_x input) is connected to a single column (O_y input). Key closures are protected from contact bounce for 5 ms.

$\overline{\text{Dial Pulse}}$ Output (Pin 9): The $\overline{\text{Dial Pulse}}$ output drives an external bipolar transistor that sequentially opens (breaks) the telephone loop a number of times equal to the input digit selected. For example, key 5 will generate 5 loop current breaks. The break/make ratio of the TP5393 and TP5394 is 1.6:1.0 (i.e., 61.5%:38.5%). The break/make ratio of the TP53143 and TP53144 is 2.0:1.0 (i.e., 67%:33%).

IDP Select (Pin 15 or 13): The IDP select input is used to select an interdigit separation of either 420 ms (logic "0" = V_{SS}) or 840 ms (logic "1" = V_{DD}). An interdigit delay precedes the first digit outpulse sequence.

$\overline{\text{Mute}}$ (Pin 11 or 10): The $\overline{\text{Mute}}$ output is used to drive an external bipolar transistor that is used to mute the receiver during the outpulse period. System timing between key closure, mute and dial pulse is shown by the timing diagram in *Figure 4*.

Tone (Pin 14 TP5393 and TP53143 Only): The TP5393 and TP53143 provide a tone output to provide audio feedback to the user. The output is a 600 Hz tone that requires an external bipolar driver to activate the telephone receiver.

Hook Switch Input (Pin 5): The function of the hook switch input is to properly initialize the circuitry for proper memory and redial operation. In the ON hook, logic "0" or V_{SS} condition, the hook switch input

a. stops the 20 kHz oscillator

b. sets the memory pointer back to digit 1

c. clamps the $\overline{\text{dial pulse}}$ and $\overline{\text{mute}}$ ouputs to logic "1" or V_{DD}

d. resets all control logic

When the telephone is taken OFF hook, this input must be taken to logic "1" or V_{DD} to release the oscillator and enable the memory and various outputs. For a non-redial application it is necessary to provide an RC delay of approximately 10 μs to the hook switch input in order to provide a proper power-on clear sequence.

Schematic diagrams for use of the TP5393, TP5394, TP53143 and TP53144 in typical applications are shown in *Figures 5 and 6.*

REDIAL FEATURE

Pushbutton inputs are accepted at an asynchronous rate. If only 1 key is detected for 5 ms, the decoded key will be loaded into a first-in-first-out memory and outpulsing of the correct number of pulses will immediately begin. After the first digit has been completed, outpulsing will cease unless another key has been entered. This allows use in a PBX system to insure receipt of a dial tone after an access code has been entered and before entering the remainder of the number. If the call was not successful, it can be redialed at a later time by pressing the redial (#) key. If an access code is required, as in a PBX system, it can be manually entered, the dial tone established, and then the redial key pushed to automatically dial the remainder of the number. Only 1 key can be entered before pushing the redial key.

An example of this operation is shown here:

	Key Inputs	Outpulses	Memory
First Try	9 P 4087375000	94087375000	94087375000
Second Try	9 P #	94087375000	94087375000
Third Try	9 P #	94087375000	94087375000

where P implies a user pause.

Functional Description (Continued)

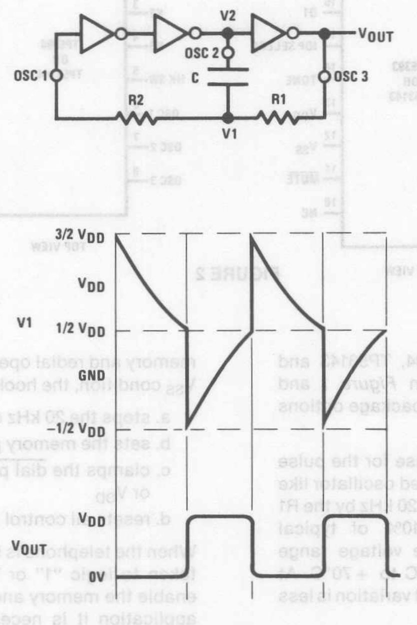


FIGURE 3. Three Gate Oscillator and Waveforms

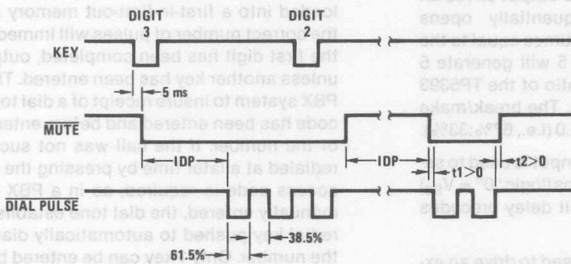
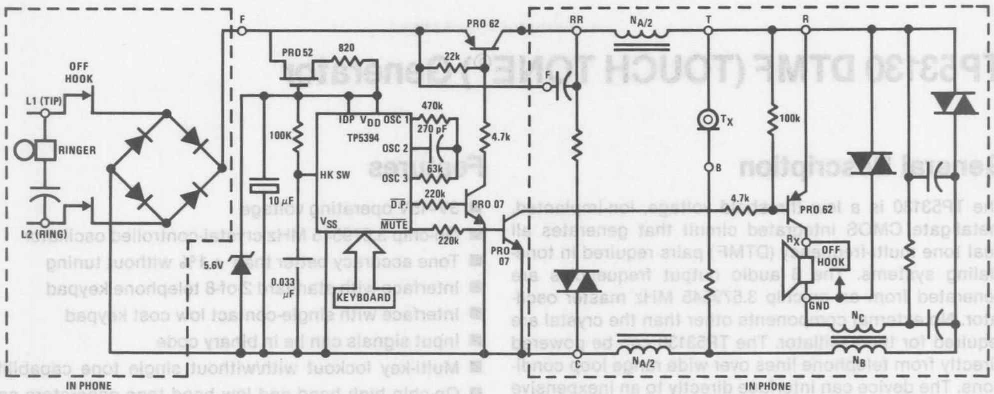


FIGURE 4. Output Timing Waveforms

Functional Description (Continued)

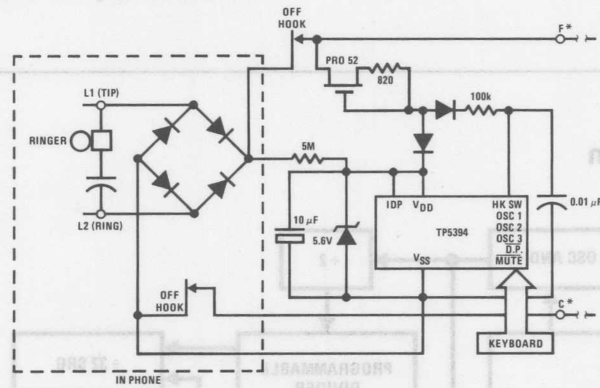


Note 1: No redial.

Note 2: Non-valued parts included in instrument.

Note 3: Letters refer to instrument terminals.

FIGURE 5. Typical Application of TP5394 in Type 500D Telephone



* Remainder of system is same as *Figure 5.*

FIGURE 6. Typical Application of TP5394 Using Redial Feature

FIGURE 7. Keypad Matrix

9

TP53130 DTMF (TOUCH TONE®) Generator

General Description

The TP53130 is a low threshold voltage, ion-implanted, metal-gate CMOS integrated circuit that generates all dual tone multi-frequency (DTMF) pairs required in tone-dialing systems. The 8 audio output frequencies are generated from an on-chip 3.579545 MHz master oscillator. No external components other than the crystal are required for the oscillator. The TP53130 can be powered directly from telephone lines over wide range loop conditions. The device can interface directly to an inexpensive single-contact calculator type keyboard or a standard telephone 2-of-8 keypad *(Figure 4)*. The TP53130 is also capable of accepting binary code inputs for microprocessor-controlled systems applications.

Features

- 3V–15V operating voltage
- On-chip 3.579545 MHz crystal-controlled oscillator
- Tone accuracy better than ±1% without tuning
- Interface with standard 2-of-8 telephone keypad
- Interface with single-contact low cost keypad
- Input signals can be in binary code
- Multi-key lockout with/without single tone capability
- On-chip high band and low band tone generators and mixer
- High band pre-emphasis
- Low harmonic distortion
- Open emitter-follower low impedance output
- Separate receiver mute and transmitter mute switch outputs
- Powered directly from the telephone line

Block Diagram

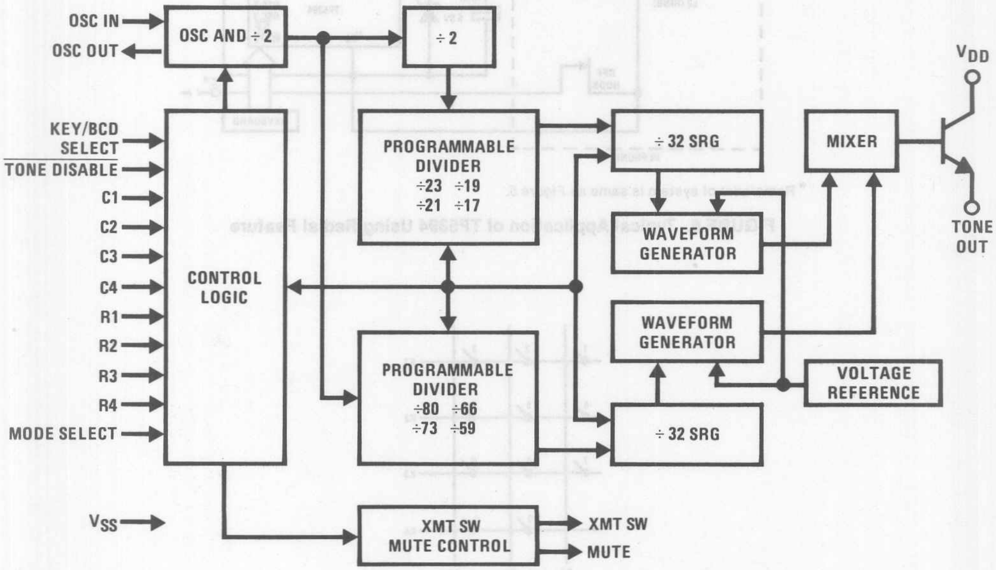


FIGURE 1

TOUCH TONE® is a registered trademark of Bell Telephone

Absolute Maximum Ratings

Voltage at Any Pin Except XMT SW and MUTE	$V_{SS}-0.3V$ to $V_{DD}+0.3V$
Voltage at XMT SW and MUTE Pins	$V_{SS}-0.3V$ to 15V
Operating Temperature Range	$-40°C$ to $+70°C$
Storage Temperature Range	$-65°C$ to $+150°C$
V_{DD}-V_{SS}	15V
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

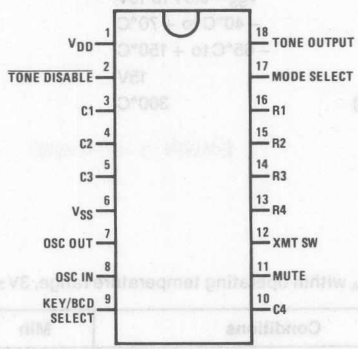
T_A within operating temperature range, $3V \le V_{DD} \le 8V$, unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Input Pull-Up Resistor					
Column and Row Inputs		25	50	90	kΩ
Key/BCD Select		200	650	1000	kΩ
$\overline{\text{Mode Select}}$		200	650	1000	kΩ
Tone Disable		200	650	1000	kΩ
Input Pull-Down Resistor					
Column and Row Inputs	$V_{DD}=3V$	650			Ω
	$V_{DD}=8V$	200			Ω
Input Voltage Levels					
Logical "1"		80% of V_{DD}		V_{DD}	V
Logical "0"		V_{SS}		20% of V_{DD}	V
Operating Frequency			3.579545		MHz
Output Voltage Swing at Tone Output					
Low Band Alone	$R_L > 150\Omega$		820		mVp-p
High Band Alone	$R_L > 150\Omega$		1000		mVp-p
Harmonic Distortion	$R_L > 150\Omega$			-20	dB
Tone Frequency Deviation				1.0	%
Typical Application Output Level V_L (See *Figure 5*)	$20 < I_L < 100$ mA				
Low Band Tone	$R_L = 150\Omega$		-7		dBV
High Band Tone	$R_L = 150\Omega$		-6		dBV
THD	$f \le 20$ kHz		4		%
Output Currents XMT SW/MUTE	$V_{DD}=3V$, $V_{OUT}=2V$	3			mA
Idle Current	$R_L=\infty$, $V_{DD}=8.0V$ (No Key Depressed)			1	mA
Operating Current	$R_L=\infty$, $V_{DD}=3.5V$			2	mA
Key Down to Tone Outputting Time (Debounce)			3	4	ms
DC Output	Tone Disable = 0		TRI-STATE®		

TRI-STATE® is a registered trademark of National Semiconductor Corp.

Connection Diagram

Dual-In-Line Package



TOP VIEW

FIGURE 2

Order Number TP53130N
See NS Package N18A

Functional Description

A functional block diagram of the TP53130 is shown in *Figure 1*, and connection diagram is shown in *Figure 2*. The TP53130 can be operated in the Keyboard Interface Mode and can also be operated in the Binary Interface Mode depending on the logic level at the Key/BCD Select input. In either mode, the device will digitally synthesize the high and low band sine waves of DTMF signaling, when valid signals are applied to row and/or column inputs. The sum of the two sine waves is then provided at the Tone output.

Tone Disable: This input has an internal pull-up resistor. When this input is open or at logical high (V_{DD}), the XMT SW and MUTE outputs will deliver valid output signals in response to the proper input signals. When Tone Disable is at logical low (V_{SS}), the device will be in the inactive mode. Tone output will go to an open circuit state, XMT SW and MUTE outputs will sink current through on-chip N-channel devices and the crystal oscillator will be disabled.

Key/Binary Select: When this input is open or at logical high (V_{DD}), the device will interface a keyboard. (See Table I.) When Key/Binary Select is low (V_{SS}), the device will accept binary inputs on the row signal input lines. (See Table II.)

Oscillator: Tone generation and internal timing are dependent on the accurate operation of the crystal oscillator. The oscillator inverter/amplifier and all necessary bias networks are included on-chip. The only external component is a 3.579545 MHz crystal. It should be connected to the device as shown in the typical application diagram *(Figure 5)*. The oscillator is not running unless a valid input signal is applied to the device. The oscillator is also disabled when Tone Disable is tied to logic low (V_{SS}). This feature will prevent RF modulation on the telephone line.

Single Tone Capability: This is a desirable feature for initial testing. With the device operating in the Keypad Interface Mode, operation of multiple keys in different rows and columns will not generate output tones. However, operation of two or more keys in the same row or column will generate the proper tone for that row or column. During multiple key operation, the XMT SW and MUTE outputs will not change state more than once. With the device operating in the Binary Interface Mode, a logical low at the column 1 input will inhibit the high band tone output while a logical low at the column 2 input will inhibit the low band tone output. (See Table I.) Logical low inputs on both column inputs 1 and 2 will disable the device the same way as the Tone Disable input will when set to logical low.

Mode Select: This input has an internal pull-up resistor. When open or at logical high, single tone outputs are allowed. When this input is at logical low, single tone outputs are prohibited. XMT SW and MUTE outputs will stay high during a multiple key depression input.

Tone Output: Dual-tone output frequencies are generated in response to valid input signals to the device. (See Table III.) Each frequency is synthesized with 32 steps of approximation for low harmonic distortion. The amplitudes of the low and high frequency tones are constant and independent of operating voltages. When tone outputs are present, the Tone output will be the composite of the AC signal superimposed on a DC offset. The DC offset is approximately 1/2 V_{DD}. When no tones are present at the Tone output pin, the pin will be open circuit.

XMT SW (Transmitter Switch) and MUTE Outputs: In the idle state (no key depressed, no signal interface inputs and Tone Disable at a logical low) both the XMT SW and MUTE outputs will sink current to V_{SS} through on-chip transistors. In the active state, these outputs will source current from V_{DD} whenever valid output tones are generated. The MUTE output activates before the XMT SW output as shown in *Figure 3*.

Signal Inputs (Row and Column Inputs): These inputs do not have a fixed pull-up or pull-down internal resistor, or a fixed logical level. Logic levels at the inputs are determined by internal states of the device. An input scan technique is used so that the device can directly interface either 2-of-8 keypads with common switch arrangements or the single contact X-Y keypads. (See *Figure 4*.)

Functional Description (Continued)

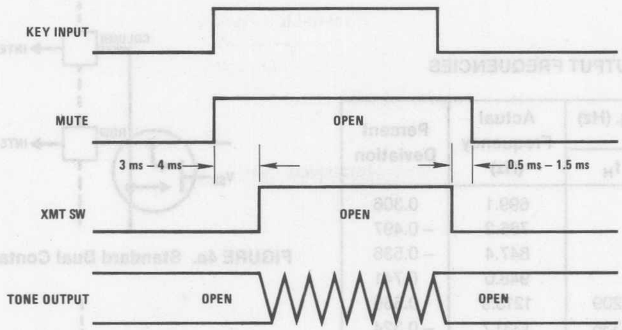


FIGURE 3. Timing Diagram of MUTE and XMT SW in Relation to Key Input and Tone Output

TABLE I. FUNCTIONAL TRUTH TABLE (WITH "MODE SELECT" OPEN)

Key/Binary Select	Tone Disable	Row	Column	Tone Output Low Band	Tone Output High Band	XMT SW	MUTE
X	0	X	X	0	0	0	0
1	1	One	One	f_L	f_H	1	1
1	1	One	Two or More	f_L	0	1	1
1	1	Two or More	One	0	f_H	1	1
1	1	Two or More	Two or More	0	0	0	0
0	1	Binary	Open	f_L	f_H	1	1
0	1	Binary	C1 = 0	f_L	0	1	1
0	1	Binary	C2 = 0	0	f_H	1	1
0	1	X	C1 and C2 = 0	0	0	0	0

TABLE II. FUNCTIONAL TRUTH TABLE FOR BINARY INTERFACE

Keyboard Inputs	Binary Inputs C1	C2	R1	R2	R3	R4	Frequencies Generated f_L (Hz)	f_H (Hz)
1	Open	Open	0	0	0	1	697	1209
2	Open	Open	0	0	1	0	697	1336
3	Open	Open	0	0	1	1	697	1477
4	Open	Open	0	1	0	0	770	1209
5	Open	Open	0	1	0	1	770	1336
6	Open	Open	0	1	1	0	770	1477
7	Open	Open	0	1	1	1	852	1209
8	Open	Open	1	0	0	0	852	1336
9	Open	Open	1	0	0	1	852	1477
0	Open	Open	1	0	1	0	941	1336
*	Open	Open	1	0	1	1	941	1209
#	Open	Open	1	1	0	0	941	1477
A	Open	Open	1	1	0	1	697	1633
B	Open	Open	1	1	1	0	770	1633
C	Open	Open	1	1	1	1	852	1633
D	Open	Open	0	0	0	0	941	1633
	0	Open	Valid				f_L	—
	Open	0	Binary				—	f_H
	0	0	Inputs				1/2 V_{DD}	1/2 V_{DD}

TABLE III. OUTPUT FREQUENCIES

Inputs	Desired Freq. (Hz) f_L	Desired Freq. (Hz) f_H	Actual Frequency (Hz)	Percent Deviation
R1	697		699.1	0.306
R2	770		766.2	– 0.497
R3	852		847.4	– 0.536
R4	941		948.0	0.741
C1		1209	1215.9	0.569
C2		1336	1331.7	– 0.324
C3		1477	1471.9	– 0.35
C4		1633	1645.0	0.736

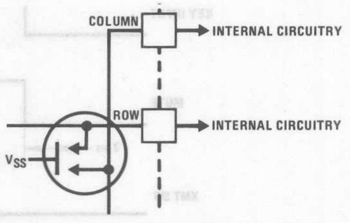


FIGURE 4a. Standard Dual Contact Telephone Key

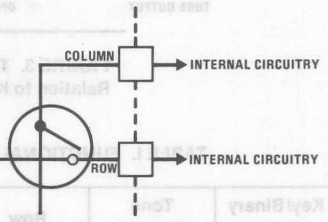
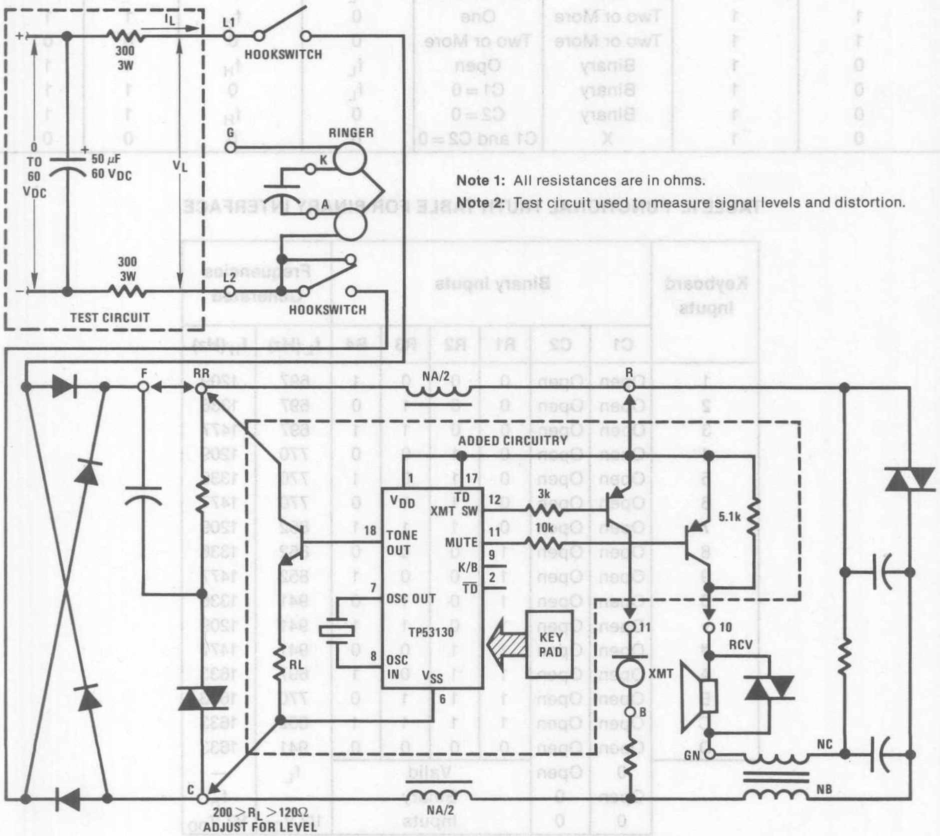


FIGURE 4b. Single Contact Key

Typical Application



Note 1: All resistances are in ohms.

Note 2: Test circuit used to measure signal levels and distortion.

FIGURE 5

National Semiconductor

PRELIMINARY

TP5600, TP5605, TP5610, TP5615 Ten-Number Repertory Pulse Dialers

General Description

The TP5600, TP5605, TP5610, TP5615 are monolithic integrated circuits built using National's advanced P^2CMOS process (double poly-silicon gate CMOS). They provide all logic necessary to convert keypad inputs into a series of pulses simulating rotary telephone dialing. An on-chip memory provides storage for nine telephone numbers plus the last number dialed, each up to 16 digits in length. The simple control scheme needs only 2 key entries to store a number or initiate automatic dialing of a stored number. This control scheme is the same as that used on the TP5650 repertory DTMF generator so that no user re-education is necessary when converting from pulse to tone dialing. For PBX applications, the first 1 or 2 digits may be overwritten to obtain a second dial tone prior to automatic dialing. Two outputs are provided to control pulsing of the telephone line and muting of the receiver. The low voltage and low current requirements of this device allow direct telephone line powered operation for dialing. A small battery is recommended for on-hook memory retention.

Features

- 2V, 150 μA telephone-line powered operation
- 1 μA memory retention current
- Stores and auto-dials ten 16-digit numbers
- Last-number-redial included
- Scratchpad (number storage without dialing)
- Control key scheme—same as TP5650 DTMF repertory dialer
- 2-digit overwrite for PBX access codes
- Voltage regulator on-chip
- RC oscillator with ±3% frequency stability
- Single-contact or negative-common key inputs
- TP5600, TP5605 for pulsing loop in shunt with speech network
- TP5610, TP5615 for pulsing loop in series with speech network
- TP5605, TP5615 have IDP select and 10/20 pps select

Block Diagram

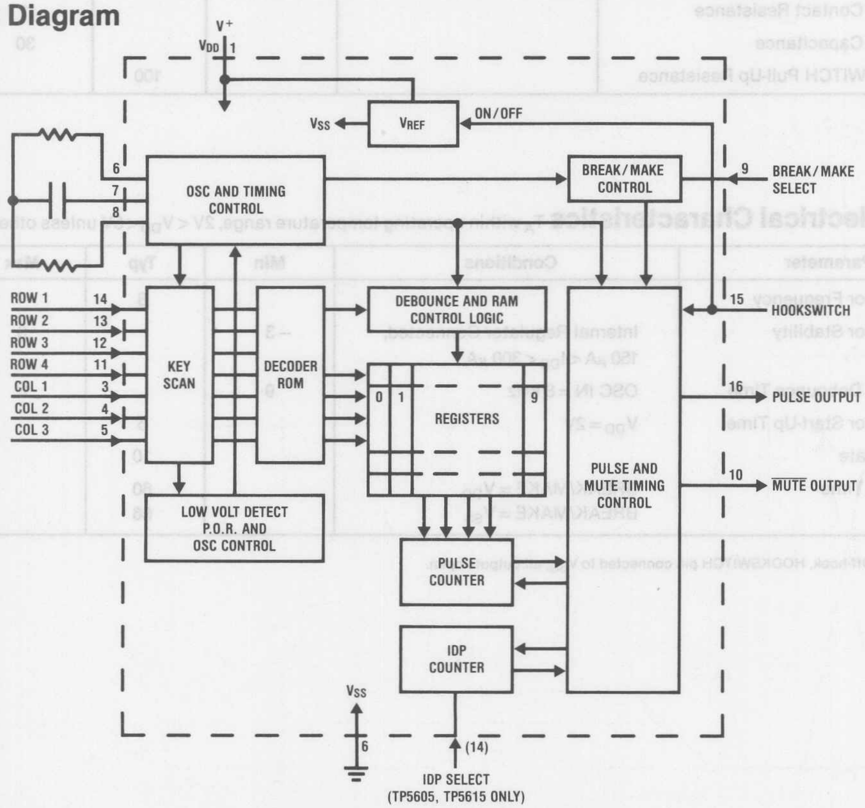


FIGURE 1

TP5600, TP5605, TP5610, TP5615

9

Absolute Maximum Ratings

DC Supply Voltage (V_{DD}–V_{SS})	6V
Voltage on Any Pin	V_{DD} + 0.3V to V_{SS} − 0.3V
Operating Temperature (T_A)	−30°C to +70°C
Storage Temperature	−55°C to +150°C
Maximum Power Dissipation (25°C)	500 mW

DC Electrical Characteristics T_A within operating temperature range, $2V < V_{DD} < 5V$ unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
DC Operating Current	$V_{DD} = 2V$ (Note 1)			150	µA
	$V_{DD} = 5V$ (Note 1)	1			mA
Memory Retention Current	On-Hook, $V_{DD} = 2V$			1	µA
PULSE Sink Current	$V_{DD} = 2V$, $V_{OUT} = 0.5V$	50			µA
PULSE Source Current	$V_{DD} = 2V$, $V_{OUT} = 1.5V$	150			µA
MUTE Sink Current	$V_{DD} = 2V$, $V_{OUT} = 0.5V$	50			µA
MUTE Source Current	$V_{DD} = 2V$, $V_{OUT} = 1.5V$	150			µA
Logic '0' Level Input		V_{SS}		$0.2\ V_{DD}$	
Logic '1' Level Input		$0.8\ V_{DD}$		V_{DD}	
Keyscan Pull-Up Resistance			100		kΩ
Keyscan Pull-Down Resistance			4		kΩ
Keypad Contact Resistance				1	kΩ
Keypad Capacitance				30	pF
HOOKSWITCH Pull-Up Resistance			100		kΩ

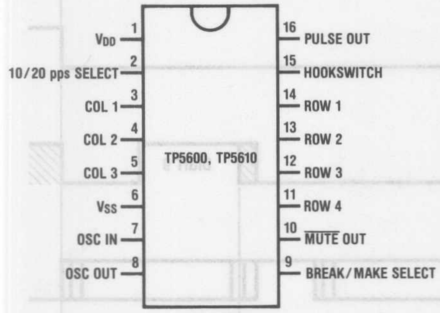
AC Electrical Characteristics T_A within operating temperature range, $2V < V_{DD} < 5V$ unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Oscillator Frequency			8		kHz
Oscillator Stability	Internal Regulator Connected, 150 µA < I_{DD} < 300 µA	−3		3	%
Keypad Debounce Time	OSC IN = 8 kHz	9		11	ms
Oscillator Start-Up Time	$V_{DD} = 2V$		5		ms
Pulse Rate			10		pps
BREAK Time	BREAK/MAKE = V_{DD}		60		ms
	BREAK/MAKE = V_{SS}		66		ms

Note 1: Off-hook, HOOKSWITCH pin connected to V_{SS}, all outputs open.

Connection Diagrams

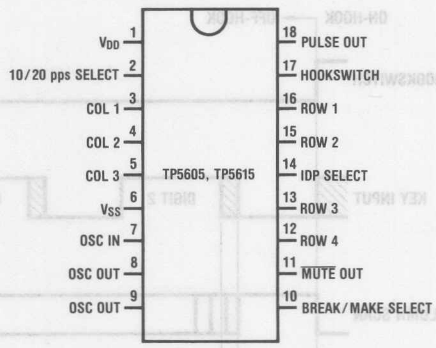
Dual-In-Line Package



TOP VIEW

Order Number TP5600N or TP5610N

Dual-In-Line Package



TOP VIEW

Order Number TP5605N or TP5615N

Pin Descriptions (Pin numbers refer to TP5600, TP5610)

V_{DD} (pin 1): This is the positive supply to the device and is referenced to V_{SS} (pin 5). An active zener regulator is connected on-chip between V_{DD} and V_{SS} (see pin 5), and the device is intended to be powered from a current-limited source. This regulator is turned off and effectively disconnected when the device is in the on-hook state in order to minimize current consumption. Power-on reset and low-voltage detect circuits ensure correct operation following power-up or reduction of the on-hook supply voltage below that required to retain stored data.

Keypad Inputs (pins 3, 4, 5, 11, 12, 13 and 14): A valid key entry is defined as either connecting a single row to a single column or connecting V_{SS} simultaneously to a single row and a single column. This allows direct interface to an inexpensive single-contact (form A) keypad, the standard 2-of-7 keypad with negative-common, or logic-generated inputs.

V_{SS} (pin 6): This is the negative supply.

OSC IN, OSC OUT (pins 7, 8 on TP5600, TP5610 only): The device contains an on-chip oscillator circuit designed to work with a ceramic resonator at 480 kHz in anti-resonant mode. 2 external capacitors are required, typically 100 pF each. The circuit may also be driven with an external 480 kHz source on OSC IN.

OSC IN, OSC OUT, $\overline{\text{OSC}}$ OUT (pins 7, 8 and 9 on TP5605, TP5615 only): The device includes a stable on-chip oscillator circuit designed to work with the component values shown in *Figure 3*. The circuit may also be driven with an external 8 kHz source on OSC IN (pin 6).

On all devices, the oscillator runs only while the device is scanning the keypad and/or timing storage or outpulsing functions.

BREAK/MAKE SELECT (pin 9): The BREAK/MAKE ratio is selected by connecting this pin as follows:

Input to BREAK/MAKE Pin	PULSE Output	
	BREAK	MAKE
V_{DD}	60%	40%
V_{SS}	66%	34%

$\overline{\text{MUTE}}$ OUT (pin 10): This is a CMOS output designed to drive a simple interface circuit to mute the receiver during outpulsing. See the timing diagram for further details.

HOOKSWITCH (pin 15): This input has a 100 kΩ internal pull-up resistor to V_{DD}. Allowing this pin to float, or connecting a V_{DD} level puts the circuit in the on-hook, low power idle mode. It also turns off the active zener regulator.

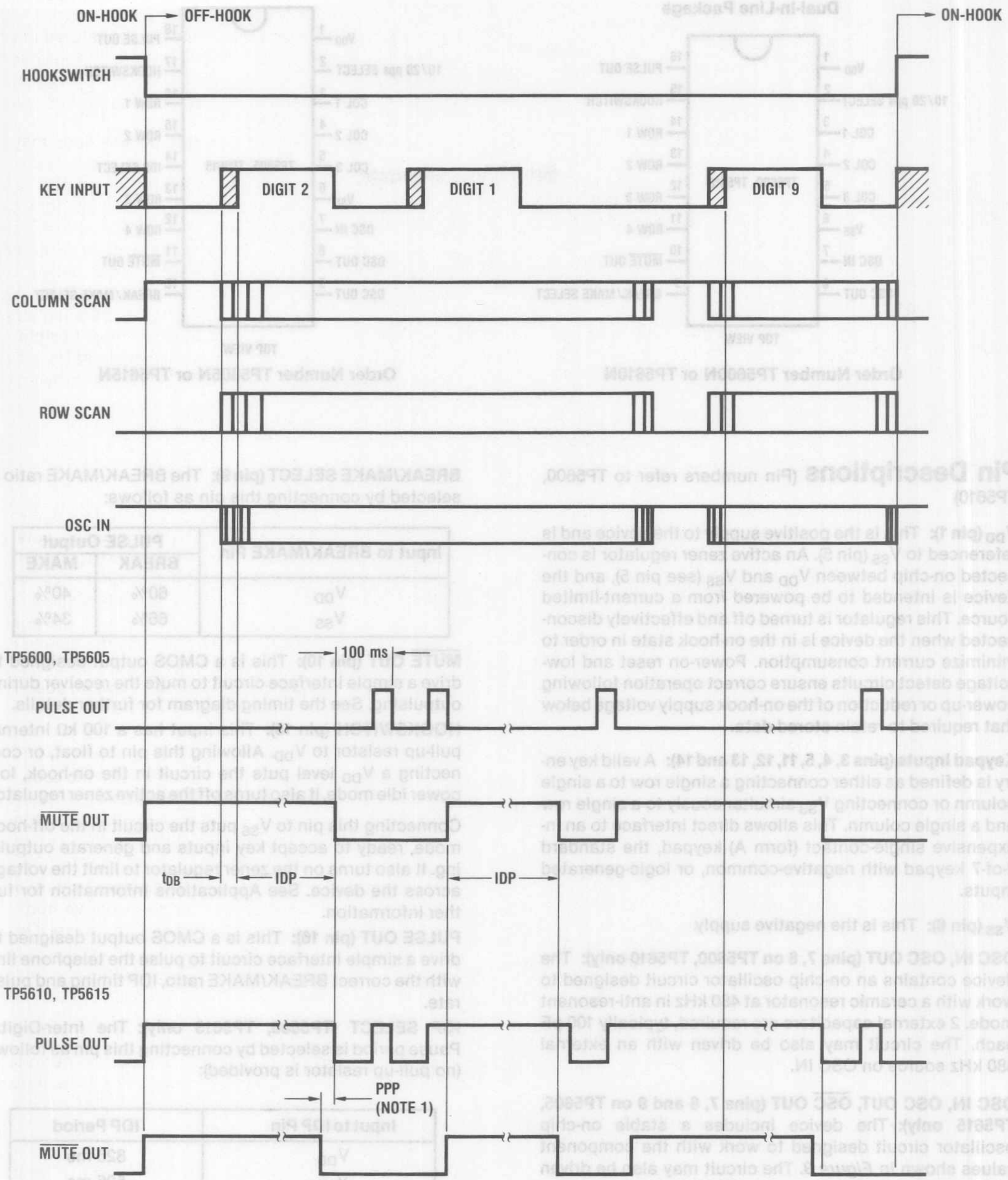
Connecting this pin to V_{SS} puts the circuit in the off-hook mode, ready to accept key inputs and generate outpulsing. It also turns on the zener regulator to limit the voltage across the device. See Applications Information for further information.

PULSE OUT (pin 16): This is a CMOS output designed to drive a simple interface circuit to pulse the telephone line with the correct BREAK/MAKE ratio, IDP timing and pulse rate.

IDP SELECT (TP5605, TP5615 only): The Inter-Digital Pause period is selected by connecting this pin as follows (no pull-up resistor is provided):

Input to IDP Pin	IDP Period
V_{DD}	825 ms
V_{SS}	525 ms

10/20 pps SELECT (pin 2): For normal 10 pps dialing, connect this pin to V_{SS}. Connecting this pin to V_{DD} doubles the rate of all PULSE OUT and $\overline{\text{MUTE}}$ OUT timing.



Note 1: PPP is a pre-pulsing pause equal to 1 MAKE period.

Note 2: A mask option of $\overline{\text{MUTE}}$ continuously active low during the IDP is available as a mask option.

FIGURE 2

Functional Description

The timebase for this family of repertory dialers is derived from a stable RC oscillator connected as shown in *Figure 3*. In the on-hook condition, the oscillator is stopped and all keypad inputs inhibited. After going off-hook, the oscillator remains off and the keypad inputs go to a static sensing mode. Upon sensing a single key closure, the oscillator starts, and the row and column inputs are alternately scanned at a 500 Hz rate. When a key closure remains valid for the required debounce time, the key is interpreted in accordance with Table I. During manual dialing, valid digit keys are entered into the last-number-dialed register (register 0) in sequence and outpulsed at the nominal 10 pps rate. A manually dialed number may be entered rapidly and may exceed 16 digits without limit, provided no more than 15 digits remain to be outpulsed. Automatic dialing is inhibited, however, if an attempt is made to store more than 16 digits in any register. When no further digits remain to be outpulsed, the oscillator stops and key inputs return to the static sensing mode awaiting further keys or a return to the on-hook condition.

TABLE I. CONTROL SCHEME

Function	Control Sequence
Dial and store in register 0	$\uparrow D_1 \ldots D_x$
No dial, store in register N only	$\uparrow * N D_1 \ldots D_x$
Scratchpad	$\ldots D_x * N D_1 \ldots D_y$
Copy last number to register N	$\ldots D_x (\downarrow \uparrow) * N \downarrow$
Auto-dial register N	$\uparrow$ # N
Last number redial	$\uparrow$ # 0
PBX access	$\uparrow (D_1) (D_2)$ # 0 or N

Note 1: N is a long-term storage register numbered from 1–9.

Note 2: $\uparrow$ indicates on-hook to off-hook, $\downarrow$ indicates off-hook to on-hook.

Note 3: Entries in brackets may be omitted.

NUMBER STORAGE

Telephone numbers are stored in 10 registers, numbered 0–9. Register contents can only be modified while off-hook. Register 0 always stores the last number which was manually dialed, and remains unchanged during automatic dialing. Numbers for long-term storage in registers 1–9 are entered by *, then N and then the telephone number, where N is the register number. Other registers can be successively modified by entering a new *, N followed by the telephone number. Once a * key is entered, no further outpulsing is possible until after an on-hook reset on the HOOKSWITCH pin. This facilitates the Scratchpad feature, whereby a number can be stored in a register without outpulsing during a conversation. The last number dialed manually is copied from register 0 to any of the long-term storage registers by entering *, N.

An attempt to store more than 16 digits in a register will set an overflow flag to inhibit automatic dialing from that register. The flag is reset following the next *, N entry to re-program that register.

DIALING

Automatic dialing of the telephone number stored in any register is initiated by entering #, then N. The keypad is then locked out until completion of outpulsing, after which further manual or automatic dialing is permitted.

For PBX applications, a 1 or 2-digit access code may be entered prior to a #, N code. These access digits overwrite the previously stored digits at the start of register 0, the last-number-dialed register. The user then waits for a second dial-tone before automatically dialing the required number. Note that if a 2-digit access code is entered followed by #, 0, register 0 is automatically dialed from location 3 onwards. Either a 1 or 2-digit access code followed by #, 0, however, automatically dials register N from location 1 onwards. This allows the most flexible use of registers 1–9. Thus, it is not necessary to store access codes in registers 1–9, either manually or by copying the last number dialed.

Applications Information

The TP5600 and TP5605 PULSE output is designed to drive a pulsing loop circuit in shunt with the speech network, as shown in *Figure 3*. During outpulsing, the MUTE circuit is turned off to isolate the speech network from the line. Q2 and Q3 conduct during MAKE periods, R1 adjusts telephone pulsing resistance. Q2 and Q3 turn off during BREAK periods, loop current is then only the supply current to the device. Q1 provides a current source of 200 μA minimum to ensure that the device will have an adequate supply voltage.

The TP5610 and TP5615 PULSE output is designed for a series pulsing loop, as shown in *Figure 4*. In this case, the MUTE circuit isolates only the receiver, so that current flows through the speech network while outpulsing MAKE periods. Q3 cuts off this current during BREAK periods.

The on-hook current required for the device to retain data is low enough to allow this current to be drawn from the telephone line in certain applications. In this case, it is advisable to add an external protection zener diode, specified for very low leakage, as the internal regulator is turned off when the HOOKSWITCH pin goes high. A low leakage decoupling capacitor should also be specified.

To protect stored data in the event of reduced line voltage (caused by an off-hook extension telephone, for example), a small back-up battery is recommended, as shown in *Figures 3 and 4*.

The off-hook current source formed by JFET Q1 and its source resistor must provide sufficient current to supply the repertory dialer plus the PULSE and $\overline{\text{MUTE}}$ loads when in their active states.

Applications Information (Continued)

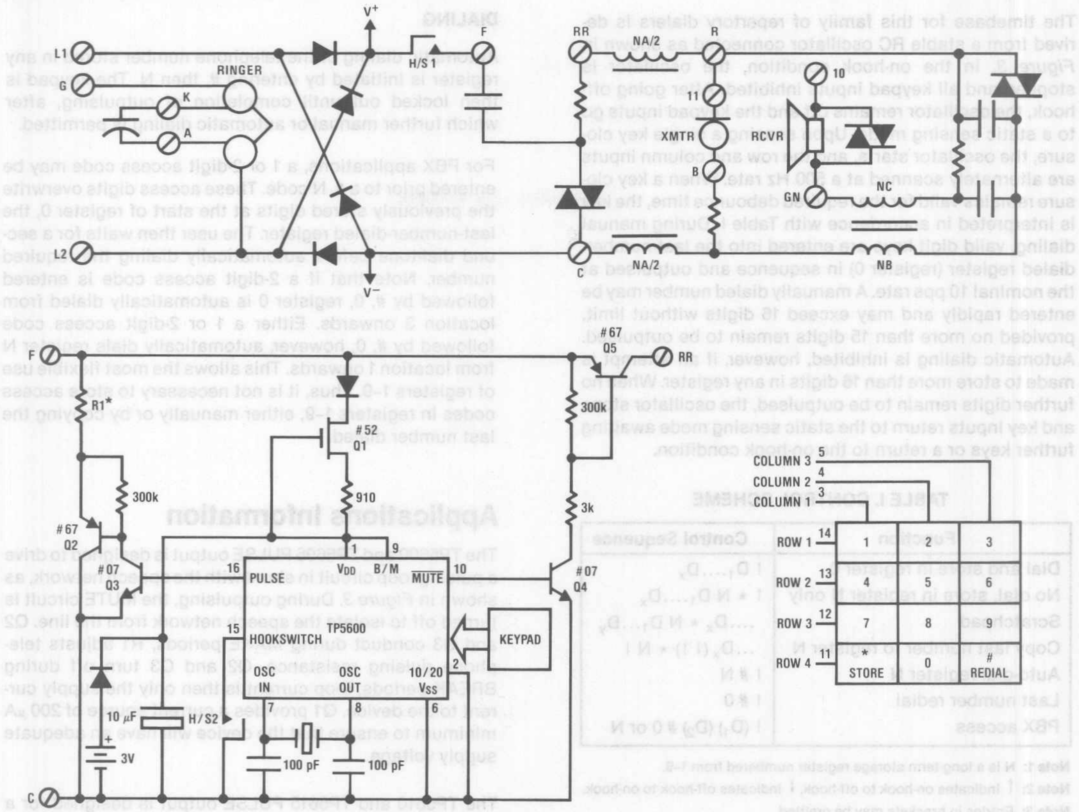


FIGURE 3. TP5600 Shunt Dialer Application

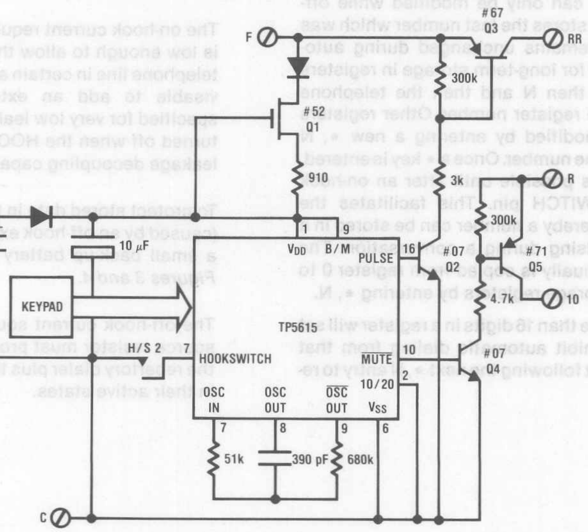


FIGURE 4. TP5615 Series Dialer Application

National Semiconductor

PRELIMINARY

TP5650, TP5660 Ten-Number Repertory DTMF Generators

General Description

The TP5650 and TP5660 are monolithic integrated circuits built using National's advanced P^2CMOS process (double poly-silicon gate CMOS). They interface directly to a telephone keypad and generate all 16 standard dual-tone multi-frequency pairs required in tone dialing systems. An on-chip memory provides storage for nine telephone numbers plus the last number dialed, each up to 16 digits in length. The simple control scheme needs only 2 key entries to store a number or initiate automatic dialing of a stored number. This control scheme is the same as that used on the TP5600 family of repertory pulse dialers so that no user re-education is necessary when converting from pulse to tone dialing. The tone synthesizers are locked to an inexpensive 3.579545 MHz crystal for high accuracy. A MUTE OUT logic signal, which changes state when any key is depressed, is also provided. The low voltage and low current requirements of this device allow direct telephone line powered operation. A small battery is recommended for on-hook memory retention.

Features

- 2.5V–12V operation when generating tones
- 2V operation of keyscan and MUTE logic
- 1 μA memory retention current
- Stores and auto-dials ten 16-digit numbers
- Last-number-redial included
- Scratchpad (number storage without dialing)
- TP5650 control key scheme same as TP5600 repertory pulse dialer
- TP5660 has 14 keys—separate Store and Redial
- 2-digit overwrite for PBX access codes
- 3.579545 MHz crystal-controlled oscillator
- Low harmonic distortion
- Single-contact or negative-common (2-of-8) key inputs

Block Diagram

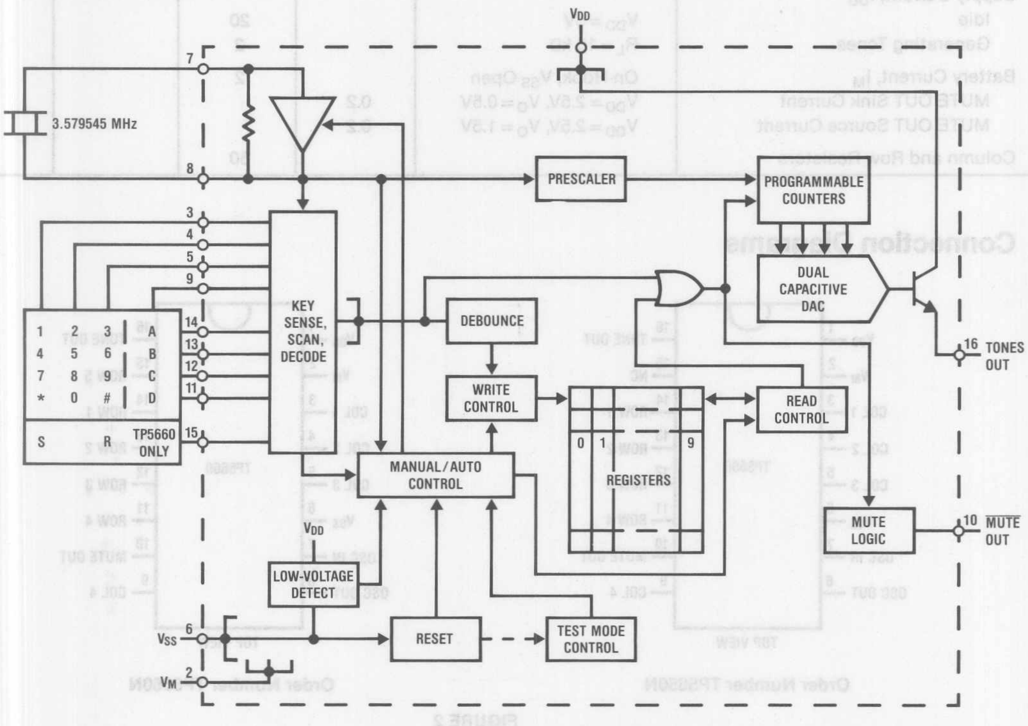


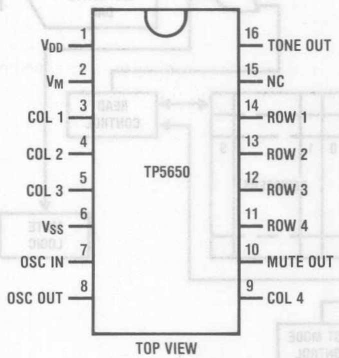
FIGURE 1

Operating Temperature (T_A)	−30°C to +60°C
Storage Temperature	−55°C to +150°C
Maximum Power Dissipation	500 mW

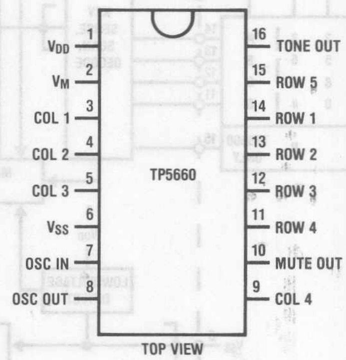
Electrical Characteristics $2V < V_{DD} < 10V$, unless otherwise specified, T_A within operating temperature range

Parameter	Conditions	Min	Typ	Max	Units
Minimum Supply Voltage Swing	Generating Tones	2.5			V
TONE OUT Amplitudes	$R_L = 100\Omega$				
Low Group	$V_{DD} = 2.5V$		175		mVrms
	$V_D = 10V$		190		mVrms
High Group	$V_{DD} = 2.5V$		225		mVrms
	$V_{DD} = 10V$		240		mVrms
High Group Pre-Emphasis			2		dB
Mean DC Offset	Generating Tones				
	$V_{DD} = 2.5V$		0.7		V
	$V_{DD} = 10V$		2.8		V
Dual Tone/Total Harmonic Distortion Ratio	1 MHz Bandwidth	20			dB
Start-Up Time (to 90% Amplitude)				5	ms
Tones-On Duration	Automatic Dialing		72.3		ms
Tones-Off Duration	Automatic Dialing		72.3		ms
Supply Current, I_{DD}					
Idle	$V_{DD} = 5V$		20		μA
Generating Tones	$R_L = 10\ k\Omega$		2		mA
Battery Current, I_M	On-Hook, V_{SS} Open		2		μA
MUTE OUT Sink Current	$V_{DD} = 2.5V$, $V_O = 0.5V$	0.2			mA
MUTE OUT Source Current	$V_{DD} = 2.5V$, $V_O = 1.5V$	0.2			mA
Column and Row Resistors			50		kΩ

Connection Diagrams



Order Number TP5650N



Order Number TP5660N

FIGURE 2

Pin Descriptions

V_{DD} (pin 1): The positive supply to the device, referenced to V_{SS}. A power-on reset circuit ensures correct operation following initial power-up.

V_M (pin 2): The negative terminal of the back-up battery for on-hook memory retention. A low-voltage detect circuit prevents misoperation of the circuit in the event of a reduction in the on-hook supply voltage below that required to retain stored data.

COLUMN and ROW Scans (pins 3, 4, 5, 9, 11, 12, 13, 14 plus pin 15 on TP5650 only): When no key is closed, pull-up resistors are active on COLUMN inputs and pull-down resistors are active on ROW inputs. After a key is closed the ROW pull-down resistors cause a negative-true on COLUMN inputs, which starts the oscillator and initiates tone generation.

V_{SS} (pin 6): The negative supply to the device in the off-hook state. An open-circuit on this pin while back-up power is maintained on V_M will reset the circuit.

OSC IN, OSC OUT (pins 7 and 8): All logic and tone generator timing is derived from the on-chip oscillator circuit. A low cost 3.579545 MHz A-cut crystal (NTSC TV color-burst) must be connected between pins 7 and 8. Load capacitors and a feedback resistor are included on-chip for good start-up and stability. The oscillator stops when automatic tone generation is completed or there are no key closures.

MUTE OUT (pin 10): This is a CMOS output which sinks current to V_{SS} when no tones are being generated and sources current from V_{DD} when tones are being generated.

TONE OUT (pin 10): This output is the open emitter of an NPN transistor, the collector of which is connected to V_{DD}. When an external load resistor is connected from TONE OUT to V_{SS}, the output voltage on this pin is the sum of the high and low group sine-waves superimposed on a DC offset. When not generating tones, this output transistor is turned off to minimize the device idle current.

Functional Description

In the on-hook state, with power maintained for memory retention, the oscillator is stopped, the output transistor is pulled off and all keypad inputs are inhibited. After going off-hook, the oscillator remains off and the key inputs go to a static sensing mode. A single key closure activates the MUTE OUTPUT and starts the oscillator and keyscan. A valid digit key sets the high group and low group programmable counters to the appropriate divide ratio. These counters sequence two sine-weighted-capacitor D/A converters through a series of 28 equal-duration steps per sine-wave cycle. An on-chip voltage reference ensures good stability of tone amplitudes with variations in supply voltage and temperature. The two tones are summed by a mixer amplifier, with pre-emphasis applied to the high group tone. The output is an NPN emitter-follower requiring the addition of an external load resistor to V_{SS}. This resistor facilitates adjustment of the signal current flowing from V_{DD} through the output transistor.

Key inputs which are digits for manual dialing are not debounced prior to tone generation. Keys are debounced prior to being accepted as digits to be stored or as control keys (Table II). Upon completion of a manually or automatically dialed number, the oscillator stops and key inputs return to the static sensing mode awaiting further keys or a return to the on-hook state.

TABLE I. OUTPUT FREQUENCY ACCURACY

Tone Group	Valid Input	Standard DTMF (Hz)	Tone Out Frequency	% Deviation from Standard
LOW	ROW 1	697	694.8	−0.32
GROUP	ROW 2	770	770.1	+0.02
f_L	ROW 3	852	852.4	+0.03
	ROW 4	941	940.0	−0.11
HIGH	COL 1	1209	1206.0	−0.24
GROUP	COL 2	1336	1331.7	−0.32
f_H	COL 3	1477	1486.5	+0.64
	COL 4	1633	1639.0	+0.37

TABLE II. CONTROL SCHEME

Function	Control Sequence
Dial and Store in Register 0	↑ $D_1 \ldots D_x$
No Dial, Store in Register N Only	↑ S N $D_1 \ldots D_x$
Scratchpad	↑ $D_1 \ldots D_x$ S N $D_1 \ldots D_y$
Copy Last Number to Register N	… D_x (↓ ↑) S N ↓
Auto-Dial Register N	↑ R N
Last Number Redial	↑ R 0
PBX Access	↑ (D_1) (D_2) R 0 or N
* Tones	* (TP5660) ** (TP5650) Note 1
# Tones	# (TP5660) ## (TP5650) Note 2

Note 1: * key is also STORE key S on TP5650

Note 2: # key is also REDIAL key R on TP5650

Note 3: N is a long-term storage register numbered from 1–9

Note 4: ↑ indicates on-hook to off-hook, ↓ indicates off-hook to on-hook

Note 5: Entries in brackets may be omitted

NUMBER STORAGE

S (for store) and R (for redial) entries refer to TP5660 only. * is shown in brackets to replace S and # is shown in brackets to replace R on the TP5650 only.

Telephone numbers are stored in 10 registers, numbered 0–9. Register 0 always stores the last number which was manually dialed, and remains unchanged during automatic dialing. Register contents can only be modified while off-hook.

Numbers are stored in long-term registers 1–9 by entering S (*), then N and then the telephone number, where N is the register number. Other registers can be successively modified by entering a new S (*), N, followed by the telephone number. Once an S (*) key is entered, no further digit tone outputs are possible until after an on-hook reset. This facilitates the Scratchpad feature, whereby a number can be stored in a register without tone outputs during a conversation. The last number dialed manually can be copied from register 0 to any of the long-term storage registers by entering S (*), N, then going on-hook.

An attempt to store more than 16 digits in a register will set an overflow flag to inhibit automatic dialing from that register. The flag is reset following the next S (*), N entry to re-program that register.

DIALING

In the manual dialing mode (i.e., direct dialing from the keypad), tone pairs are generated for the duration of a valid key closure.

Automatic dialing of the number stored in register N is initiated by entering R (#) followed by N. The correct tone

Functional Description (Continued)

pairs are generated in alternate bursts of tones-on, tones-off until the end of the stored number. During this time, the keypad is locked out until completion of dialing, following which further manual or automatic dialing is permitted.

For PBX applications a 1 or 2-digit access code may be entered prior to the R (#), N code. These access digits overwrite the previously-stored digits at the start of register 0, the last-number-dialed register. The user then waits for a second dial tone before entering R (#), N to automatically dial the stored number.

Note that if a 2-digit access code is entered followed by R (#), 0, register 0 is automatically dialed from location 3 onwards. Entering either a 1 or 2-digit access code followed by R (#), N, automatically dials register N from location 1 onwards. This allows the most flexible use of registers 1-9. Note that access codes should not be entered into registers 1-9, either manually or by copying the last number dialed.

Applications Information

Adjustment of the emitter load resistor results in variation of the mean DC current during tone generation, the sine-wave signal current through the output transistor, and the output distortion. Increasing values of load resistance decrease both the signal current and distortion, while increasing the source impedance of the device as seen from its power supply terminal. Note that the DTMF generator is a current source which modulates its own supply terminals in a conventional telephone application.

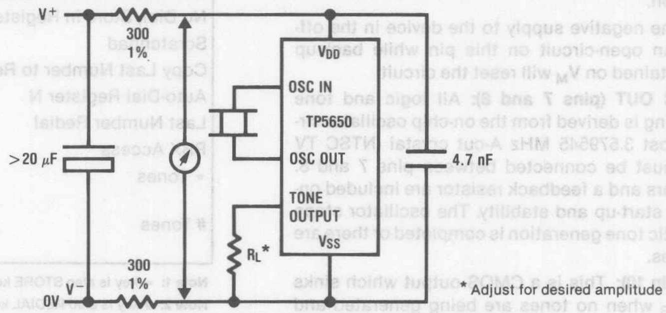


FIGURE 3. Amplitude and Distortion Measurement Circuit

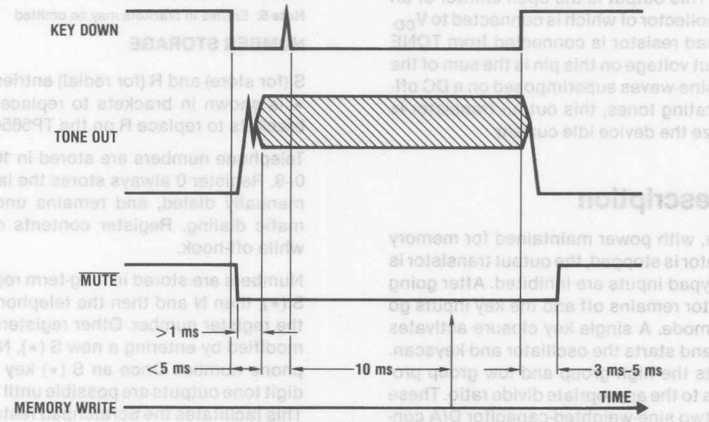


FIGURE 4a. Manual Timing

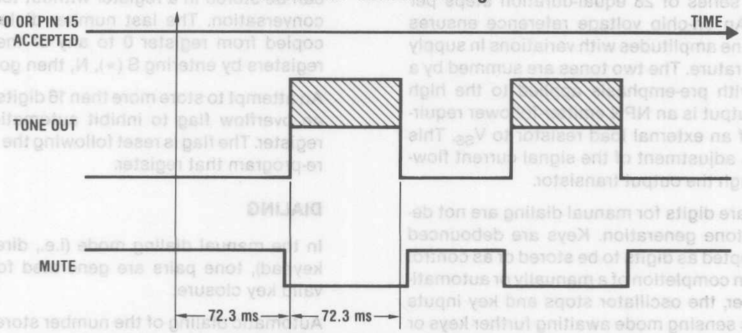


FIGURE 4b. Auto-Redial Timing

LH0091 True RMS to DC Converter

General Description

The LH0091, rms to dc converter, generates a dc output equal to the rms value of any input per the transfer function:

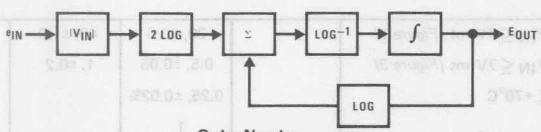
$$E_{OUT(DC)} = \sqrt{\frac{1}{T}\int_0^T E_{IN}^2\,(t)\,dt}$$

The device provides rms conversion to an accuracy of 0.1% of reading using the external trim procedure. It is possible to trim for maximum accuracy (0.5 mV ±0.05% typ) for decade ranges i.e., 10 mV → 100 mV, 0.7V → 7V, etc.

Features

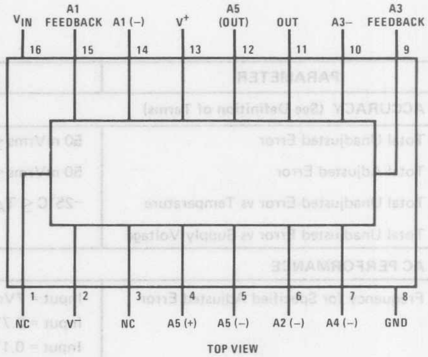
- Low cost
- True rms conversion
- 0.5% of reading accuracy untrimmed
- 0.05% of reading accuracy with external trim
- Minimum component count
- Input voltage to ±15V peak for V_S = ±15V
- Uncommitted amplifier for filtering, gain, or high crest factor configuration
- Military or commercial temperature range.

Block and Connection Diagrams



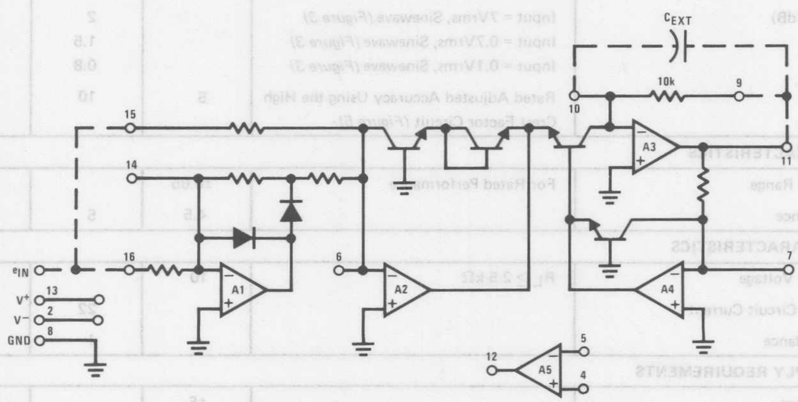
Order Number
LH0091D
LH0091CD
See Package D16D

Dual-In-Line Package



TOP VIEW

Simplified Schematic



Note: Dotted lines denote external connections.

Supply Voltage	±22V	
Input Voltage	±15V peak	
Output Short Circuit Duration	Continuous	
Operating Temperature Range	T_{MIN}	T_{MAX}
LH0091	−55°C	125°C
LH0091C	−25°C	85°C
Storage Temperature Range		
LH0091	−65°C to +150°C	
LH0091C	−25°C to +85°C	
Lead Temperature (Soldering, 10 seconds)	300°C	

Electrical Characteristics $V_S = \pm 15V$, $T_A = 25°C$ unless otherwise notes

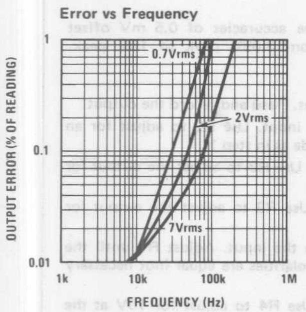
Transfer Function $= E_{O(DC)} = \sqrt{\frac{1}{T}\int_0^T E_{IN}^2(t)\,dt}$

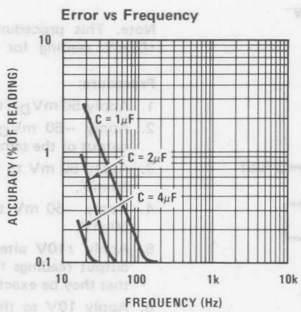
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY (See Definition of Terms)					
Total Unadjusted Error	50 mVrms $\leq V_{IN} \leq$ 7Vrms *(Figure 1)*		20, ±0.5	40, ±1.0	mV, %
Total Adjusted Error	50 mVrms $\leq V_{IN} \leq$ 7Vrms *(Figure 3)*		0.5, ±0.05	1, ±0.2	mV, %
Total Unadjusted Error vs Temperature	−25°C $\leq T_A \leq$ +70°C		0.25, ±0.02%		mV, %/°C
Total Unadjusted Error vs Supply Voltage			1		mV/V
AC PERFORMANCE					
Frequency for Specified Adjusted Error	Input = 7Vrms, Sinewave *(Figure 3)*	30	70		kHz
	Input = 0.7Vrms, Sinewave *(Figure 3)*		40		kHz
	Input = 0.1Vrms, Sinewave *(Figure 3)*		20		kHz
Frequency for 1% Additional Error	Input = 7Vrms, Sinewave *(Figure 3)*	100	200		kHz
	Input = 0.7Vrms, Sinewave *(Figure 3)*		75		kHz
	Input = 0.1Vrms, Sinewave *(Figure 3)*		50		kHz
Bandwidth (3 dB)	Input = 7Vrms, Sinewave *(Figure 3)*		2		MHz
	Input = 0.7Vrms, Sinewave *(Figure 3)*		1.5		MHz
	Input = 0.1Vrms, Sinewave *(Figure 3)*		0.8		MHz
Crest Factor	Rated Adjusted Accuracy Using the High Crest Factor Circuit *(Figure 5)*	5	10		
INPUT CHARACTERISTICS					
Input Voltage Range	For Rated Performance	±0.05		±11	Vpeak
Input Impedance		4.5	5		kΩ
OUTPUT CHARACTERISTICS					
Rated Output Voltage	$R_L \geq 2.5\ k\Omega$	10			V
Output Short Circuit Current			22		mA
Output Impedance			1		Ω
POWER SUPPLY REQUIREMENTS					
Operating Range		±5		±20	V
Quiescent Current	$V_S = \pm 15V$		14	18	mA

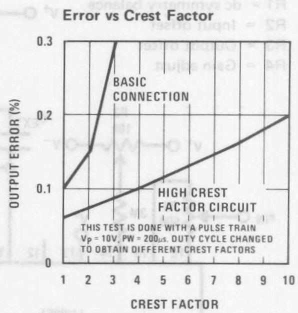
Op Amp Electrical Characteristics $V_S = \pm 15V$, $T_A = 25°C$ unless otherwise notes

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$R_S \leq 10\ k\Omega$		1.0	10	mV
I_{OS}	Input Offset Current			4.0	200	nA
I_B	Input Bias Current			30	500	nA
R_{IN}	Input Resistance			2.5		MΩ
A_{OL}	Large Signal Voltage Gain	$V_{OUT} = \pm 10V$, $R_L \geq 2\ k\Omega$	15	160		V/mV
V_O	Output Voltage Swing	$R_L = 10\ k\Omega$	±10	±13		V
V_I	Input Voltage Range		±10			V
CMRR	Common-Mode Rejection Ratio	$R_S \leq 10\ k\Omega$		90		dB
PSRR	Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$		96		dB
I_{SC}	Output Short-Circuit Current			25		mA
S_r	Slew Rate (Unity Gain)			0.5		V/µs
BW	Small Signal Bandwidth			1.0		MHz

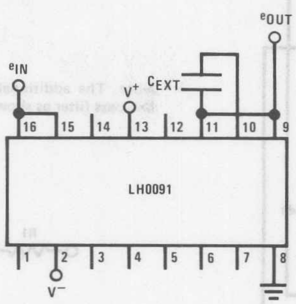
Typical Performance Characteristics







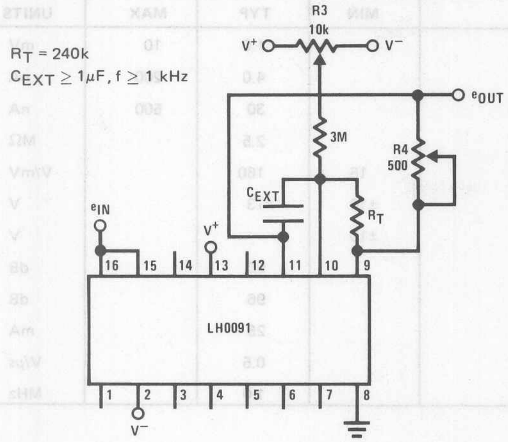
Typical Applications (All applications require power supply by-pass capacitors.)



$C_{EXT} \geq 1\mu F$; frequency ≥ 1 kHz

FIGURE 1. LH0091 Basic Connection (No Trim)

Typical Applications (Cont'd)

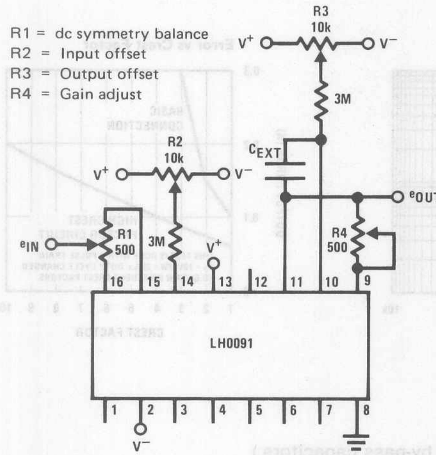


Note. The easy trim procedure is used for ac coupled input signals. It involves two trims and can achieve accuracies of 2 mV offset ±0.1% reading.

Procedure:

1. Apply 100 mV rms (sine wave) to input, adjust R3 until the output reads 100 mV_{DC}.
2. Apply 5 V_{rms} (sine wave) to input, adjust R4 until the output reads 5 V_{DC}.
3. Repeat steps 1 and 2 until the desired initial accuracy is achieved.

FIGURE 2. LH0091 "Easy Trim" (For ac Inputs Only)

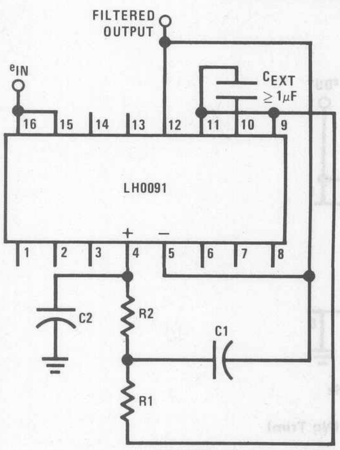


Note. This procedure will give accuracies of 0.5 mV offset ±0.05% reading for inputs from 0.05V peak to 10V peak.

Procedure:

1. Apply 50 mV_{DC} to the input. Read and record the output.
2. Apply −50 mV_{DC} to the input. Use R2 to adjust for an output of the same magnitude as in step 1.
3. Apply 50 mV to the input. Use R3 to adjust the output for 50 mV.
4. Apply −50 mV to input. Use R2 to adjust the output for 50 mV.
5. Apply ±10V alternately to the input. Adjust R1 until the output readings for both polarities are equal (not necessary that they be exactly 10V).
6. Apply 10V to the input. Use R4 to adjust for 10V at the output.
7. Repeat this procedure to obtain the desired accuracy.

FIGURE 3. LH0091 Standard dc Trim Procedure



Note. The additional op amp in the LH0091 may be used as a low pass filter as shown in *Figure 4*.

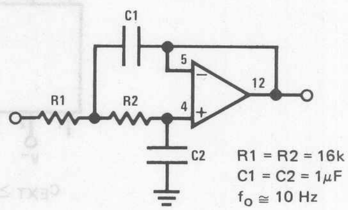
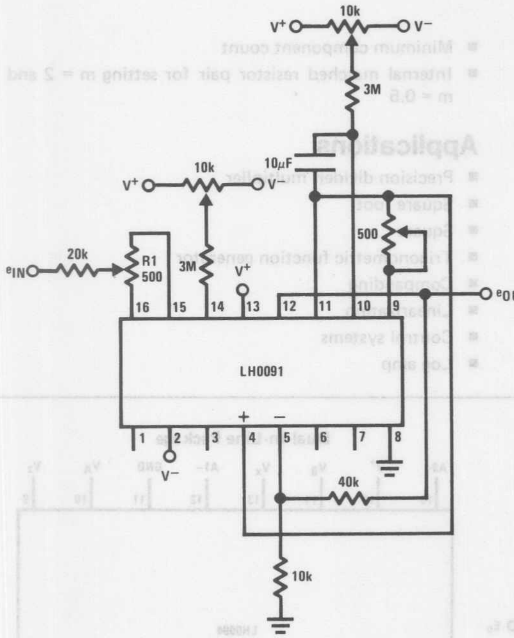


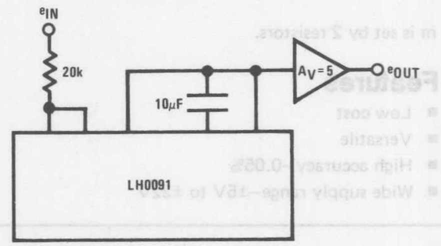
FIGURE 4. Output Filter Connection Using the Internal Op Amp

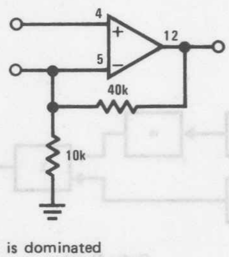
Typical Applications (Cont'd)



Note. When converting signals with a crest factor ≥ 2, the LH0091 should be connected as shown. Note that this circuit utilizes a 20k resistor to drop the input current by a factor of five. The frequency response will correspond to a voltage which is 1/5 e_{IN}.

Note that the extra op amp in the LH0091 may be used to build a gain of 5 amplifier to restore the output voltage.





Note. Response time of the dc output voltage is dominated by the RC time constant consisting of the total resistance between pins 9 and 10 and the external capacitor, C_{EX}.

FIGURE 5. High Crest Factor Circuit

Definition of Terms

True rms to dc Converter: A device which converts any signal (ac, dc, ac + dc) to the dc equivalent of the rms value.

Error: is the amount by which the actual output differs from the theoretical value. Error is defined as a sum of a fixed term and a percent of reading term. The fixed term remains constant, regardless of input while the percent of reading term varies with the input.

Total Unadjusted Error: The total error of the device without any external adjustments.

Bandwidth: The frequency at which the output dc voltage drops to 0.707 of the dc value at low frequency.

Frequency for Specified Error: The error at low frequency is governed by the size of the external averaging capacitor. At high frequencies, error is dependent on the frequency response of the internal circuitry. The frequency for specified error is the maximum input frequency for which the output will be within the specified error band (i.e., frequency for 1% error means the input frequency must be less than 200 kHz to maintain an output with an error of less than 1% of the initial reading.

Crest Factor: is the peak value of a waveform divided by the rms value of the same waveform. For high crest factor signals, the performance of the LH0091 can be improved by using the high crest factor connection.

LH0094 Multifunction Converter

General Description

The LH0094 multifunction converter generates an output voltage per the transfer function:

$$E_O = V_Y \left(\frac{V_Z}{V_X}\right)^m, \; 0.1 \leq m \leq 10, \text{ m continuously adjustable}$$

m is set by 2 resistors.

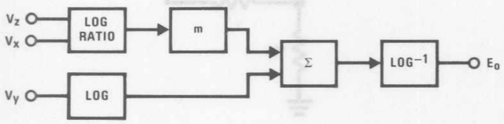
Features

- Low cost
- Versatile
- High accuracy—0.05%
- Wide supply range—±5V to ±22V
- Minimum component count
- Internal matched resistor pair for setting m = 2 and m = 0.5

Applications

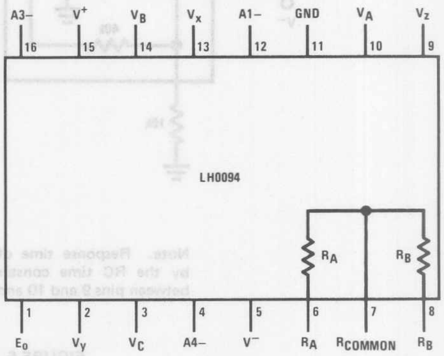
- Precision divider, multiplier
- Square root
- Square
- Trigonometric function generator
- Companding
- Linearization
- Control systems
- Log amp

Block and Connection Diagrams



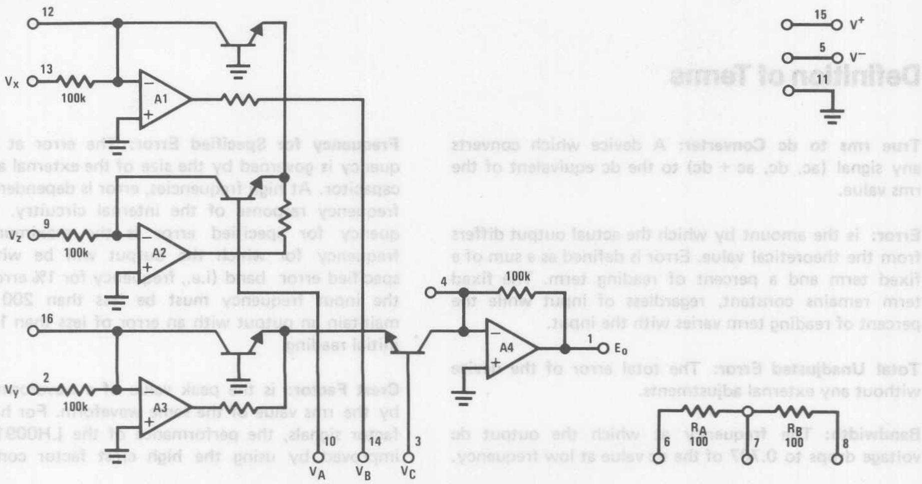
Order Number
LH0094D
LH0094CD
See Package D16D

Dual-In-Line Package



TOP VIEW

Simplified Schematic



Absolute Maximum Ratings

Supply Voltage	±22V
Input Voltage	±22V
Output Short-Circuit Duration	Continuous
Operating Temperature Range	
LH0094CD	−25°C to +85°C
LH0094D	−55°C to +125°C
Storage Temperature Range	
LH0094D	−65°C to +150°C
LH0094CD	−55°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

$V_S = \pm 15V$, $T_A = 25°C$ unless otherwise specified. Transfer function: $E_O = V_y \left(\frac{V_z}{V_x}\right)^m$; $0.1 \leqslant m \leqslant 10$; $0V \leqslant V_x, V_y, V_z \leqslant 10V$

Parameter	Conditions	LH0094 Min.	LH0094 Typ.	LH0094 Max.	LH0094C Min.	LH0094C Typ.	LH0094C Max.	Units
Accuracy								
Multiply	$E_O = \frac{V_z V_y}{10}$ $(0.03 \leqslant V_y \leqslant 10V; 0.01 \leqslant V_z \leqslant 10V)$							% F.S.
Untrimmed	(Figure 2)		0.25	0.45		0.45	0.9	(10V)
External Trim	(Figure 3)		0.10			0.1		% F.S.
	vs. Temperature		0.2			0.2		mV/°C
Divide	$E_O = 10 V_z/V_x$							
Untrimmed	(Figure 4) $0.5 \leqslant V_x \leqslant 10; 0.01 \leqslant V_z \leqslant 10)$		0.25	0.45		0.45	0.9	% F.S.
External Trim	(Figure 5), $(0.1 \leqslant V_x \leqslant 10; 0.01 \leqslant V_z \leqslant 10)$		0.10			0.1		% F.S.
	vs. Temperature		0.2			0.2		mV/°C
Square Root	$E_O = 10\sqrt{V_z/10}$							
Untrimmed	(Figure 8), $(0.03 \leqslant V_z \leqslant 10$		0.25	0.45		0.45	0.9	% F.S.
External Trim	(Figure 9), $(0.01 \leqslant V_z \leqslant 10$		0.15			0.15		% F.S.
Square	$E_O = 10 (V_z/10)^2$ $(0.1 \leqslant V_z \leqslant 10)$							
Untrimmed	(Figure 6)	0.5	1.0		1.0	2.0	% F.S.	
External Trim	(Figure 7)	0.15			0.15		% F.S.	
Low Level Square Root	$E_O = \sqrt{10V_z}$; $5.0 mV \leqslant V_z \leqslant 10V$ (Figure 10)		0.05			0.05		% F.S.
Exponential Circuits	$m = 0.2$, $E_O = 10 (V_z/10)^2$ (Figure 11), $(0.1 \leqslant V_z \leqslant 10)$		0.05			0.08		% F.S.
	$m = 5.0$, $E_O = 10 (V_z/10)^5$ (Figure 11), $(1.0 \leqslant V_z \leqslant 10)$		0.05			0.08		% F.S.
Output Offset								
	V_x 10V, $V_y = V_z = 0$		2.0	5.0		5.0	10	mV
AC Characteristics								
3dB Bandwidth	$m = 1.0$, $V_x = 10V$, $V_y = 0.1V_{rms}$		10			10		kHz
Noise	10 Hz to 1.0 kHz, $m = 1.0$, $V_y = V_z = 0V$							
	$V_x = 10V$		100			100		μV/rms
	$V_x = 0.1V$		300			300		μV/rms
Exponents								
m		0.2 to 5.0	0.1 to 10		0.2 to 5.0	0.1 to 10		
Input Characteristics								
Input Voltage	(For Rated Performance)	0		10	0		10	V
Input Impedance	(All Inputs)	98	100		98	100		kΩ
Output Characteristics								
Output Swing	$(R_L \leqslant 10k)$	10	12		10	12		V
Output Impedance			1.0			1.0		Ω
Supply Current	$(V_S = \pm 15V)$, Note 1		3.0	5.0		3.0	5.0	mA

LH0094

9

Applications Information

GENERAL INFORMATION

Power supply bypass capacitors (0.1 μF) are recommended for all applications.

The LH0094 series is designed for positive input signals only. However, negative input up to the supply voltage will not damage the device.

A clamp diode *(Figure 1)* is recommended for those applications in which the inputs may be subjected to open circuit or negative input signals.

For basic applications (multiply, divide, square, square root) it is possible to use the device without any external adjustments or components. Two matched resistors are provided internally to set m for square or square root.

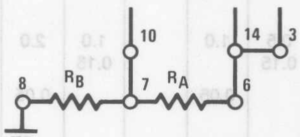
When using external resistors to set m, such resistors should be as close to the device as possible.

SELECTION OF RESISTORS TO SET m

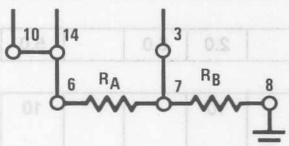
Internal Matched Resistors

R_A and R_B are matched internal resistors. They are 100Ω ±10%, but matched to 0.1%.

(a) m = 2*



(b) m = 0.5*



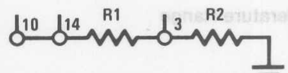
*No external resistors required, strap as indicated

External Resistors

The exponent is set by 2 external resistors or it may be continuously varied by a single trim pot. (R1 + R2 ≤ 500Ω.

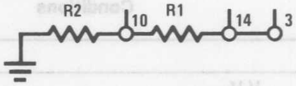
(a) m = 1

(b) m < 1



$$m = \frac{R2}{R1 + R2} \qquad R1 + R2 \approx 200\Omega$$

(c) m > 1



$$m = \frac{R1 + R2}{R2}$$

ACCURACY (ERROR)

The accuracy of the LH0094 is specified for both externally adjusted and unadjusted cases.

Although it is customary to specify the errors in percent of full-scale (10V), it is seen from the typical performance curves that the actual errors are in percent of reading. Thus, the specified errors are overly conservative for small input voltages. An example of this is the LH0094 used in the multiplication mode. The specified typical error is 0.25% of full-scale (25 mV). As seen from the curve, the unadjusted error is ≈ 25 mV at 10V input, but the error is less than 10 mV for inputs up to 1V. Note also that if either the multiplicand or the multiplier is at less than 10V, (5V for example) the unadjusted error is less. Thus, the errors specified are at full-scale—the worst case.

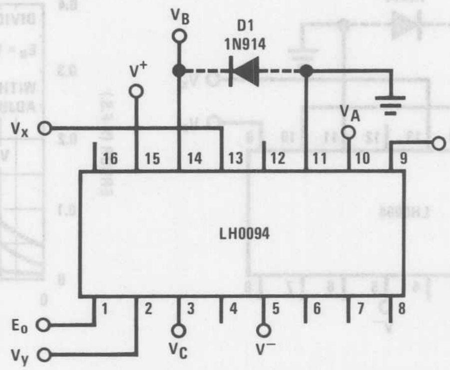
The LH0094 is designed such that the user is able to externally adjust the gain and offset of the device—thus trim out all of the errors of conversion. In most applications, the gain adjustment is the only external trim needed for super accuracy—except in division mode, where a denominator offset adjust is needed for small denominator voltages.

EXPONENTS

The LH0094 is capable of performing roots to 0.1 and powers up to 10. However, care should be taken when applying these exponents—otherwise, results may be misinterpreted. For example, consider the 1/10th power of a number: i.e., 0.001 raised to 0.1 power is 0.5011; 0.1 raised to the 0.1 power is 0.7943; and 10 raised to the 0.1 power is 1.2589. Thus, it is seen that while the input has changed 4 decades, the output has only changed a little more than a factor of 2. It is also seen that with as little as 1 mV of offset, the output will also be greater than zero with zero input.

Applications Information (Continued)

1. CLAMP DIODE CONNECTION



$$E_o = V_y \left(\frac{V_z}{V_x}\right)^m$$

$0.1 \leq m \leq 10$

Note. This clamp diode connection is recommended for those applications in which the inputs may be subject to open circuit or negative signals.

FIGURE 1. Clamp Diode Connection

2. MULTIPLY

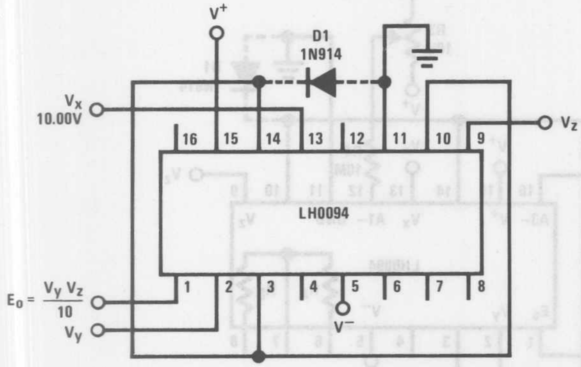


FIGURE 2a. LH0094 Used to Multiply (No External Adjustment)

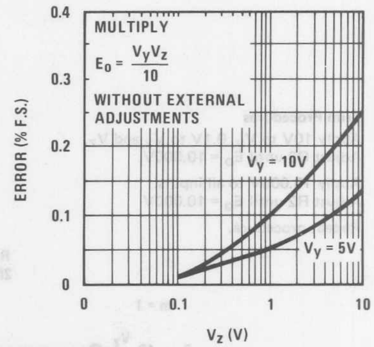
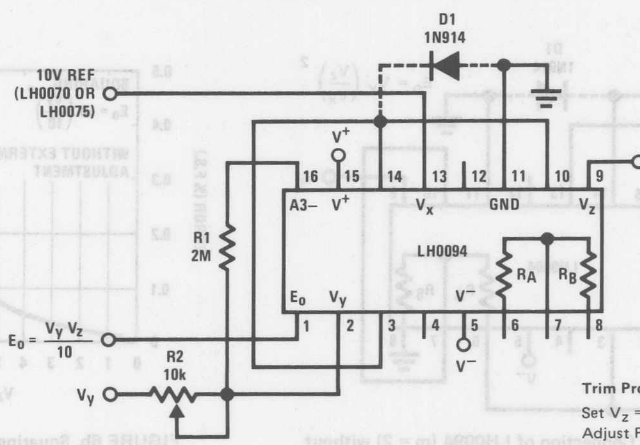


FIGURE 2b. Typical Performance of LH0094 in Multiply Mode Without External Adjustment



$$E_o = \frac{V_y\,V_z}{10} \qquad m = 1$$

Trim Procedure

Set $V_z = V_y = 10V$

Adjust R2 until output = 10.000V

FIGURE 3. Precision Multiplier (0.02% Typ) with 1 External Adjustment

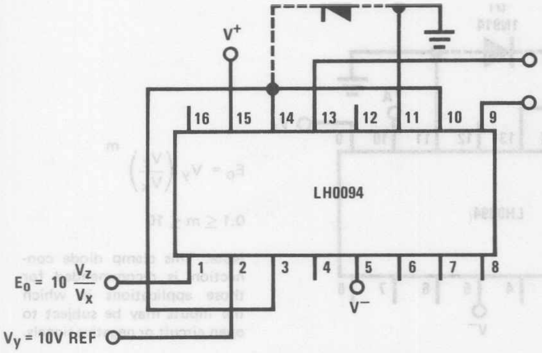


FIGURE 4a. LH0094 Used to Divide (No External Adjustment)

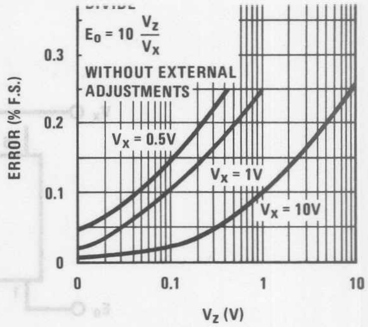


FIGURE 4b. Typical Performance, Divide Mode, Without External Adjustments

Trim Procedures

Apply 10V to V_Y, 0.1V to V_X and V_Z.
Adjust R3 until E_0 = 10.000V.

Apply 10.000V to all inputs.
Adjust R2 until E_0 = 10.000V

Repeat procedure.

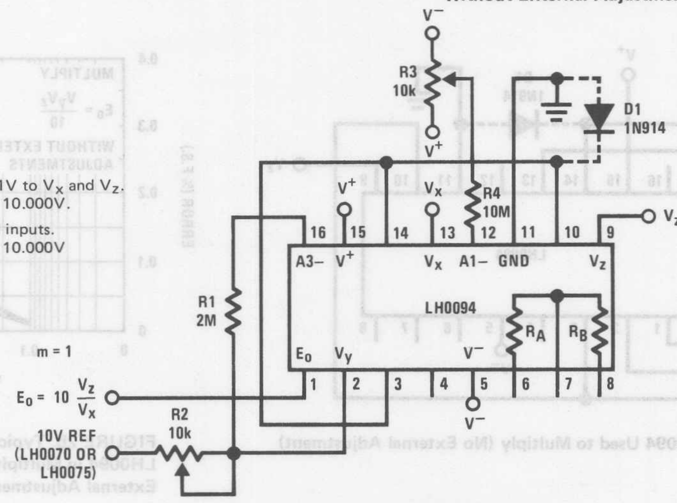


FIGURE 5. Precision Divider (0.05% Typ)

4. SQUARE

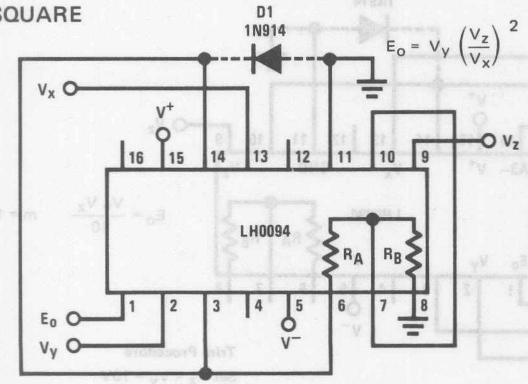


FIGURE 6a. Basic Connection of LH0094 (m = 2) without External Adjustment Using Internal Resistors to Set m

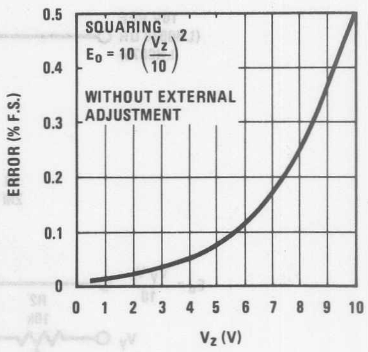
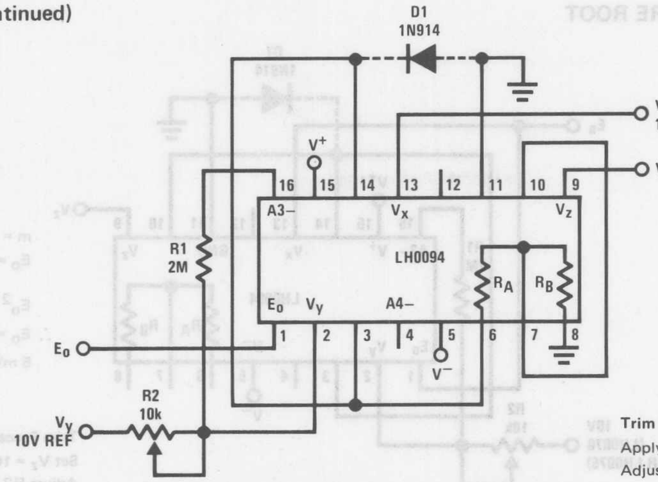


FIGURE 6b. Squaring Mode without External Adjustment

Applications Information (Continued)

4. SQUARE (Continued)



$$E_O = 10\left(\frac{V_Z}{10}\right)^2$$

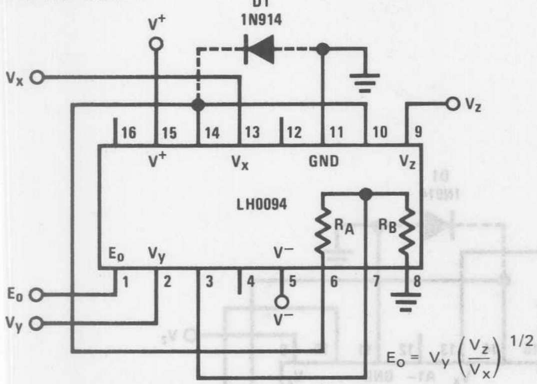
Trim Procedure

Apply 10V to V_Z

Adjust R2 for 10.000V at output

FIGURE 7. Precision Squaring Circuit (0.15% Typ)

5. SQUARE ROOT



$$E_O = V_Y\left(\frac{V_Z}{V_X}\right)^{1/2}$$

FIGURE 8a. Basic Connection of LH0094 (m = 0.5) without External Adjustment Using Internal Resistors to Set m

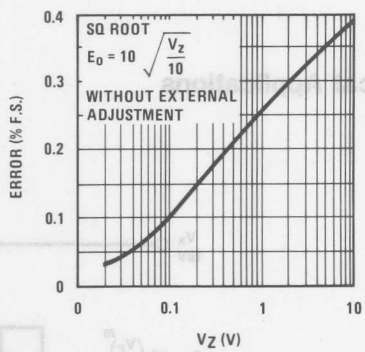
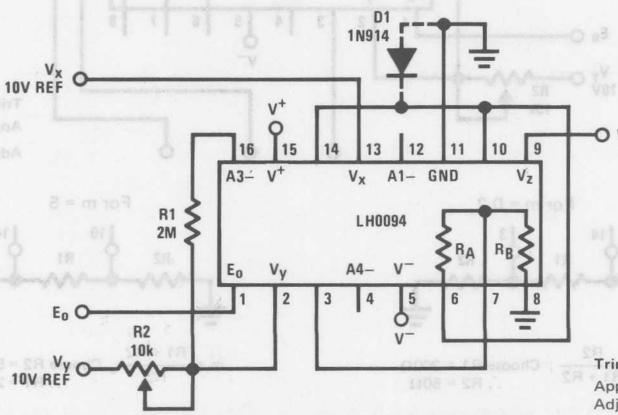


FIGURE 8b. Typical Performance Curve Square Root, No External Adjustment



$$E_O = 10\sqrt{\frac{V_Z}{10}}$$

Trim Procedure

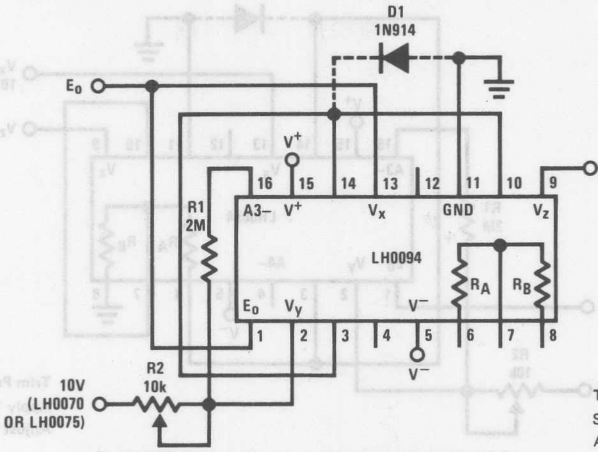
Apply 10V to all inputs.

Adjust R2 until E_O = 10.000V

FIGURE 9. Precision Square Rooter (0.15% Typ)

Applications Information (Continued)

6. LOW LEVEL SQUARE ROOT



$m = 1$

$E_o = 10\ \frac{V_z}{E_o}$

$E_o^2 = 10\ V_z$

$\therefore\ E_o = \sqrt{10\ V_z}$

$5\ mV \le V_z \le 10V$

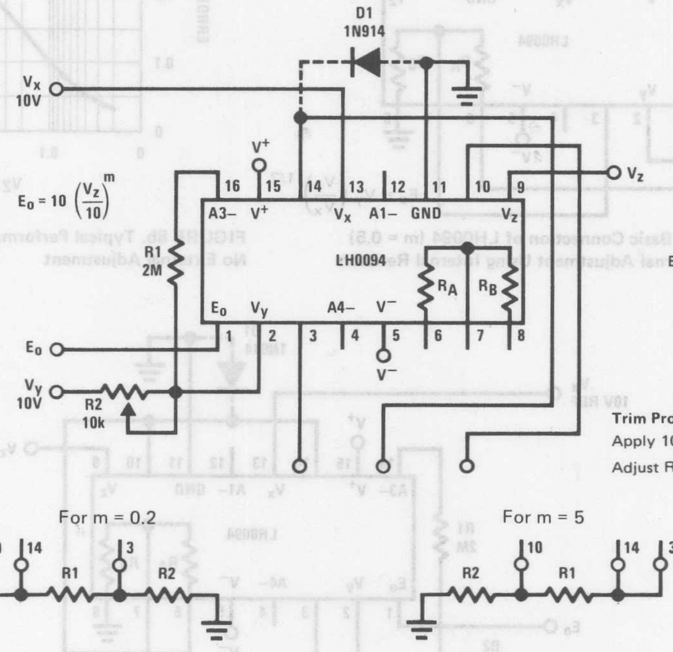
Trim Procedure

Set V_z = 10V

Adjust R2 until output = 10.000V

FIGURE 10. 3-Decade Precision Square Root Circuit Using the LH0094 with m = 1

Typical Applications



Trim Procedure

Apply 10V to all inputs

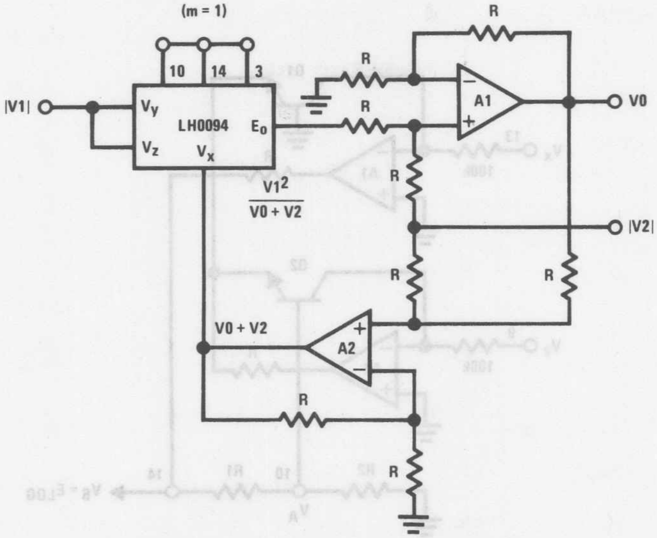
Adjust R2 for output of 10.000V

$m = \frac{R2}{R1 + R2}$; Choose R1 = 200Ω $\therefore$ R2 = 50Ω

$m = \frac{R1 + R2}{R2}$; Choose R2 = 50Ω $\therefore$ R1 = 200Ω

FIGURE 11. Precision Exponentiator (m = 0.2 to 5)

Typical Applications (Continued)



Note. The LH0094 may be used to generate a voltage equivalent to:

$$V0 = \sqrt{V1^2 + V2^2}$$

$$V0 = V2 + \frac{V1^2}{V0 + V2}$$

$$V0^2 + V0\,V2 = V2\;V0 + V2^2 + V1^2$$

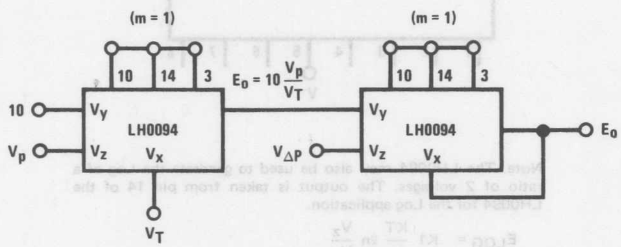
$$V0^2 = V1^2 + V2^2$$

$$\therefore\; V0 = \sqrt{V1^2 + V2^2} \qquad V1, V2\; 0 \rightarrow 10V$$

$R \approx 10k$

National Semiconductor resistor array RA08–10k is recommended

FIGURE 12. Vector Magnitude Function



Note. The LH0094 may be used in direct measurement of gas flow.

$$\text{Flow} = k\sqrt{\frac{P\Delta P}{T}}$$

$$E_o = 10\,\frac{V_P}{V_T} \times \frac{V_{\Delta P}}{E_o}$$

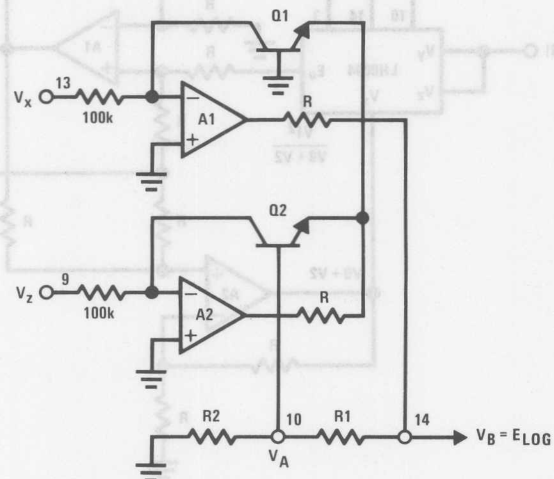
$$E_o^2 = 10\,\frac{V_P\,V_{\Delta P}}{V_T}$$

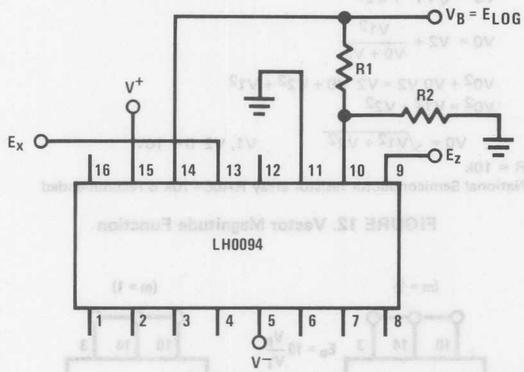
$$E_o = \sqrt{10\,\frac{V_P\;V_{\Delta P}}{V_T}}$$

P = Absolute pressure
T = Absolute temperature
ΔP = Pressure drop

FIGURE 13. Mass Gas Flow Circuit

Typical Applications (Continued)





Note. The LH0094 may also be used to generate the Log of a ratio of 2 voltages. The output is taken from pin 14 of the LH0094 for the Log application.

$$E_{LOG} = K1 \frac{KT}{q} \ln \frac{V_z}{V_x}$$

where $K1 = \dfrac{R1 + R2}{R2}$

If $K1 = \dfrac{1}{KT/q \ln 10}$

then $E_{LOG} = \text{Log}_{10} \dfrac{V_z}{V_x}$

$R1 = 15.9\ R2$
$R2 \approx 400\Omega$

R2 must be a thermistor with a tempco of $\approx$ 0.33%/°C to be compensated over temperature.

FIGURE 14. Log Amp Application

Section 10

Audio/Radio Circuits

10

Section Contents

Section Contents (Continued)

10

AM RF/IF/DETECTOR

	Application			Package	Voltage Range	Input Sensitivity	Overall AM THD	Signal to Noise	Notes
	Portable	Home	Auto						
LM1866	●	●	●	N20	3V–15V	9 μV	0.3%	50 dB	Also FM
LM1868	●	●		N20	4.5V–15V	12 μV	1.1%	50 dB	Also FM, audio
LM3820	●	●	●	N14	4.5V–16V	35 μV			External detector

AM STEREO DECODER

	Application			Package	Voltage Range	Separation	THD	Signal to Noise	Notes
	Portable	Home	Auto						
LM1981		●	●	N20	8V–18V	30 dB	1.0%	55 dB	Decodes all systems

Note: Availability of the LM1981 in production quantities is dependent upon FCC system selection.

FM IF/DETECTOR

	Application			Package	Voltage Range	Input Sensitivity	Signal to Noise	THD	Mute Control	AGC Outputs	AFC	Meter Drive
	Portable	Home	Auto									
LM1865		●	●	N20	7V–16V	6 μV	84 dB	0.15%	●	●	●	●
LM1866	●	●	●	N20	3V–15V	12 μV	76 dB	0.5%	●		●	●
LM1868	●	●		N20	4.5V–15V	15 μV	64 dB	1.1%				
LM3011	●	●		H10	6V–15V	300 μV						
LM3075	●	●	●	N14	8.5V–12.5V	250 μV		1.5%				
LM3089		●	●	N16	8V–16V	12 μV	70 dB	0.5%	●	●	●	●
LM3189		●	●	N16	8V–16V	12 μV	80 dB	0.5%	●	●	●	●
TBA120	●	●	●	N14	6V–18V	30 μV		0.5%				

FM STEREO DECODER

	Application			Package	Voltage Range	THD	Channel Separation	Blend	High Cut	Lamp Driver	Output Buffer	ARI Interface Rejection
	Portable	Home	Auto									
LM1310		●		N14	10V–18V	0.3%	45 dB			●		
LM1800		●		N16	10V–18V	0.1%	45 dB			●	●	
LM1870	●	●	●	N20	7V–15V	0.25%	45 dB	●	●	●	●	
LM4500A	●	●	●	N16	8V–16V	0.1%	40 dB	●		●	●	●

PREAMPLIFIERS

	Application			Package	Voltage Range	Equivalent Input Noise	THD	PSR	Input Coupling	Notes
	Portable	Home	Auto							
LM381	●	●		N14	9V–40V	0.5 μV	0.1%	120 dB	AC	Stereo
LM382	●	●	●	N14	9V–40V	0.8 μV	0.1%	120 dB	AC	Stereo
LM387	●	●	●	N08	9V–30V	0.65 μV	0.1%	110 dB	AC	Stereo
LM1303		●		N14	10V–30V	0.8 μV			AC	Stereo
LM1818	●	●	●	N20	3.5V–18V	0.85 μV	0.05%	85 dB	AC	Tape system
LM1837	●	●	●	N18	4V–18V	0.6 μV†	0.03%	105 dB	DC	Autoreverse
LM1897	●	●	●	N16	4V–18V	0.6 μV†	0.03%	105 dB	DC	Few externals

†CCIR/ARM in DIN circuit referred to gain at 1 kHz.

*Note that all values shown are typical. Please refer to data sheets for test conditions.

AUDIO CONTROLS

	Application			Package	Voltage Range	Volume Control Range	Signal to Noise	THD	Separation	Notes
	Portable	Home	Auto							
LM1035	•	•	•	N20	8V–18V	80 dB	80 dB	0.05%	70 dB	Dual DC tone/volume/balance
LM1037	•	•	•	N18	5V–30V		100 dB	0.04%	100 dB	DC audio switch
LM1038	•	•	•	N18	5V–30V		100 dB	0.04%	100 dB	BCD input
LM13600 LM13700	•	•	•	N16	±2V–±18V			0.5%	100 dB	Transconductance amplifiers

NOISE REDUCTION

	Application			Package	Voltage Range	NR Type	NR Effect	Encoding Required	Single/ Dual	Decode S/N	Notes
	Portable	Home	Auto								
LM1111	•	•	•	N16	6V–18V	Dolby	10 dB	Yes	Single	83 dB	Tightened spec
LM1121	•	•	•	N16	6V–18V	Dolby	10 dB	Yes	Single	82 dB	DC switched
LM1131	•	•	•	N18	6V–18V	Dolby	10 dB	Yes	Dual	87 dB	DC switched
LM1894	•	•	•	N14	4.5V–18V	DNR	12 dB	No	Dual	76 dB	NSC system
LM13700		•		N16	±15V	C-X	20 dB	Yes	**		Phono
LF347		•		N14	±15V	C-X	20 dB	Yes	**		Phono
LF353		•		N08	±15V	C-X	20 dB	Yes	**		Phono

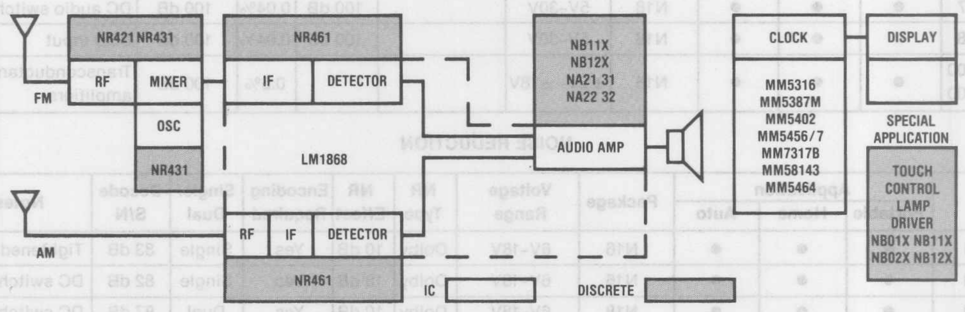
**The C-X system requires one LM13700 and 8–10 op amps for stereo phono noise reduction.

AUDIO POWER AMPLIFIERS

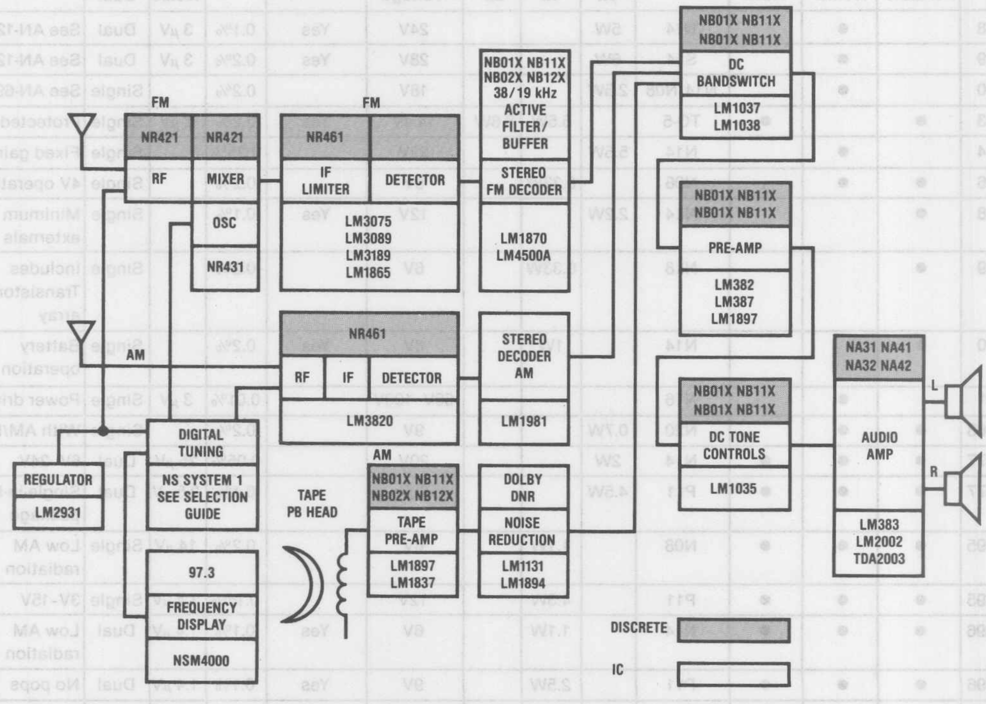
	Application			Package	Power			@ Voltage	Bridgeable	THD	Input Noise	Single/ Dual	Notes
	Portable	Home	Auto		8Ω	4Ω	2Ω						
LM378		•		N14	5W			24V	Yes	0.1%	3 μV	Dual	See AN-125
LM379		•		S14	6W			28V	Yes	0.2%	3 μV	Dual	See AN-125
LM380		•		N14/N08	2.5W			18V		0.2%		Single	See AN-69
LM383	•		•	TO-5		5.5W	8.6W	14.4V	Yes	0.2%	2 μV	Single	Protected
LM384		•		N14	5.5W			22V		0.25%		Single	Fixed gain
LM386	•	•		N08		0.33W		6V		0.2%		Single	4V operation
LM388	•			N14	2.2W			12V	Yes	0.1%		Single	Minimum externals
LM389	•			N18		0.33W		6V		0.2%		Single	Includes Transistor array
LM390	•			N14		1W		6V	Yes	0.2%		Single	Battery operation
LM391		•		N16				60V–100V		0.01%	3 μV	Single	Power driver
LM1868	•	•		N20	0.7W			9V		0.2%		Single	With AM/FM
LM1877	•	•	•	N14	2W			20V		0.05%	25 μV	Dual	6V–24V
LM2877	•	•	•	P11	4.5W			20V		0.1%	2.5 μV	Dual	Single-in-line package
LM1895	•	•	•	N08		1.1W		6V		0.2%	14 μV	Single	Low AM radiation
LM2895	•	•	•	P11		4.3W		12V		0.15%	1.4 μV	Single	3V–15V
LM1896	•	•	•	N14		1.1W		6V	Yes	0.1%	1.4 μV	Dual	Low AM radiation
LM2896	•	•	•	P11		2.5W		9V	Yes	0.1%	1.4 μV	Dual	No pops
LM2002	•		•	TO-5		5.2W	8W	14.4V	Yes	0.1%	2 μV	Single	Protected
LM2878		•		P11	5.5W			22V		0.15%	2.5 μV	Dual	6V–32V

*Note that all values shown are typical. Please refer to data sheets for test conditions.

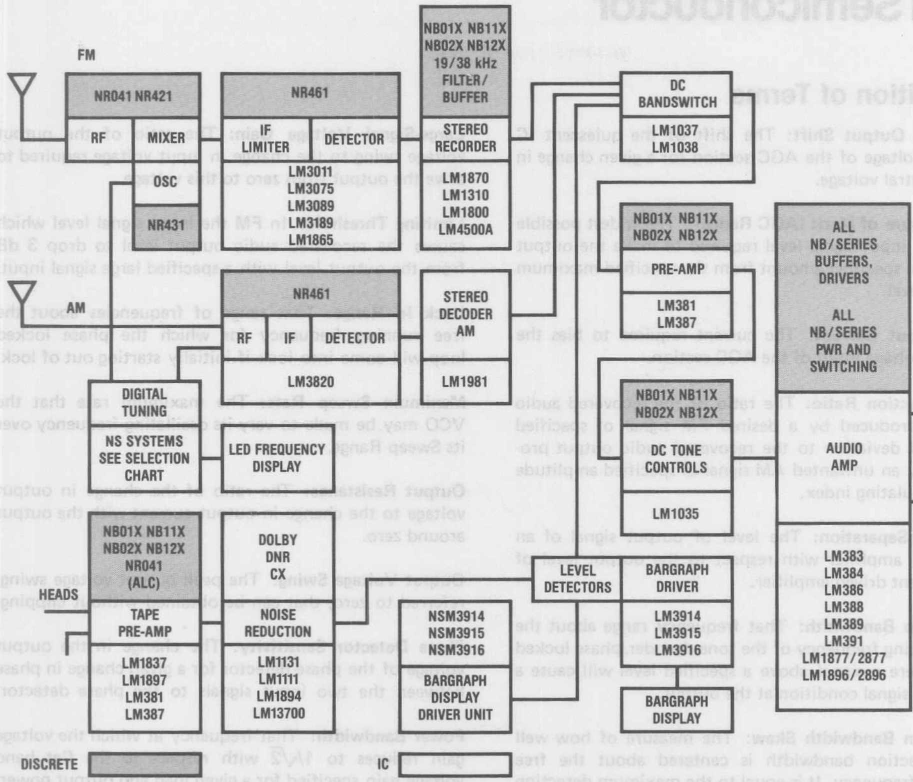
Clock Radio



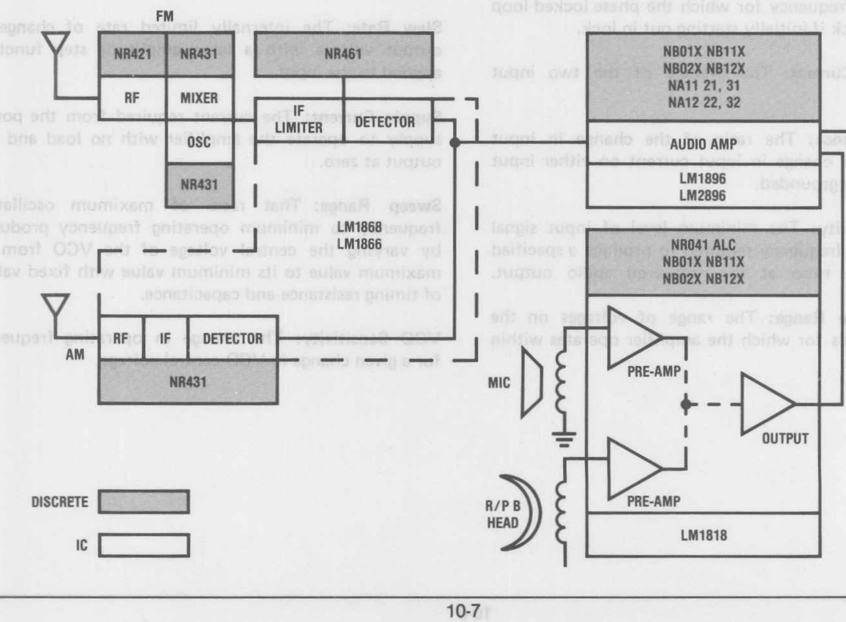
Car Stereo



Home Music System



Portable Mono Cassette Radio



Definition of Terms

AGC dc Output Shift: The shift of the quiescent IC output voltage of the AGC section for a given change in AGC central voltage.

AGC Figure of Merit (AGC Range): The widest possible range of input signal level required to make the output drop by a specified amount from the specified maximum output level.

AGC Input Current: The current required to bias the central voltage input of the AGC section.

AM Rejection Ratio: The ratio of the recovered audio output produced by a desired FM signal of specified level and deviation to the recovered audio output produced by an unwanted AM signal of specified amplitude and modulating index.

Channel Separation: The level of output signal of an undriven amplifier with respect to the output level of an adjacent driven amplifier.

Detection Bandwidth: That frequency range about the free running frequency of the tone decoder/phase locked loop where a signal above a specified level will cause a detected signal condition at the output.

Detection Bandwidth Skew: The measure of how well the detection bandwidth is centered about the free running frequency. It is equal to the maximum detection bandwidth frequency plus the minimum detection bandwidth frequency minus twice the free running frequency.

Hold In Range: That range of frequencies about the free running frequency for which the phase locked loop will stay in lock if initially starting out in lock.

Input Bias Current: The average of the two input currents.

Input Resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Input Sensitivity: The minimum level of input signal at a specified frequency required to produce a specified signal-to-noise ratio at the recovered audio output.

Input Voltage Range: The range of voltages on the input terminals for which the amplifier operates within specifications.

Large-Signal Voltage Gain: The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

Limiting Threshold: In FM the input signal level which causes the recovered audio output level to drop 3 dB from the output level with a specified large signal input.

Lock In Range: That range of frequencies about the free running frequency for which the phase locked loop will come into lock if initially starting out of lock.

Maximum Sweep Rate: The maximum rate that the VCO may be made to vary its oscillating frequency over its Sweep Range.

Output Resistance: The ratio of the change in output voltage to the change in output current with the output around zero.

Output Voltage Swing: The peak output voltage swing, referred to zero, that can be obtained without clipping.

Phase Detector Sensitivity: The change in the output voltage of the phase detector for a given change in phase between the two input signals to the phase detector.

Power Bandwidth: That frequency at which the voltage gain reduces to $1/\sqrt{2}$ with respect to the flat band voltage gain specified for a given load and output power.

Power Supply Rejection: The ratio of the change in input offset voltage to the change in power supply voltages producing it.

Slew Rate: The internally limited rate of change in output voltage with a large amplitude step function applied to the input.

Supply Current: The current required from the power supply to operate the amplifier with no load and the output at zero.

Sweep Range: That ratio of maximum oscillating frequency to minimum operating frequency produced by varying the central voltage of the VCO from its maximum value to its minimum value with fixed values of timing resistance and capacitance.

VCO Sensitivity: The change in operating frequency for a given change in VCO central voltage.

National Semiconductor

LM377 Dual 2 Watt Audio Amplifier

General Description

The LM377 is a monolithic dual power amplifier which offers high quality performance for stereo phonographs, tape players, recorders, and AM-FM stereo receivers, etc.

The LM377 will deliver 2W/channel into 8 or 16Ω loads. The amplifier is designed to operate with a minimum of external components and contains an internal bias regulator to bias each amplifier. Device overload protection consists of both internal current limit and thermal shutdown. For more information, see AN-125. The LM377 is not recommended for new designs; see the LM1877 data sheet for an improved pin-for-pin replacement to the LM377 in audio applications.

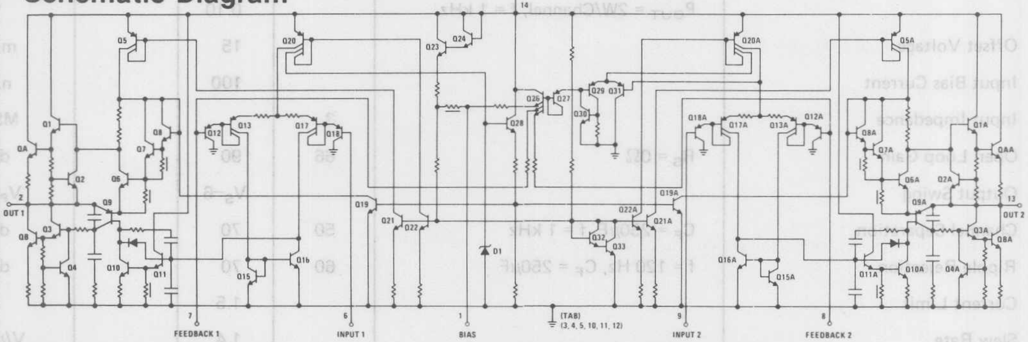
Features

- A_{VO} typical 90 dB
- 2W per channel
- 70 dB ripple rejection
- 75 dB channel separation
- Internal stabilization
- Self centered biasing
- 3 MΩ input impedance
- 10–26V operation
- Internal current limiting
- Internal thermal protection

Applications

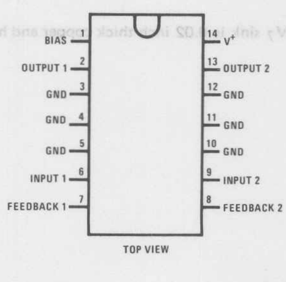
- Multi-channel audio systems
- Tape recorders and players
- Movie projectors
- Automotive systems
- Stereo phonographs
- Bridge output stages
- AM-FM radio receivers
- Intercoms
- Servo amplifiers
- Instrument systems

Schematic Diagram



Connection Diagram

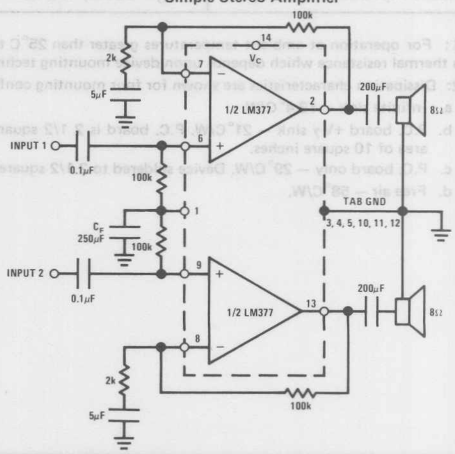
Dual-In-Line Package



Order Number LM377N
See NS Package N14A

Typical Applications

Simple Stereo Amplifier



Absolute Maximum Ratings

Supply Voltage	26V
Input Voltage	0V – V_{SUPPLY}
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

V_S = 20V, T_{TAB} = 25°C, R_L = 8Ω, A_V = 50 (34 dB), unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Total Supply Current	P_{OUT} = 0W		15	50	mA
	P_{OUT} = 1.5W/Channel		430	500	mA
DC Output Level			10		V
Supply Voltage		10		26	V
Output Power	T.H.D. = < 5%	2	2.5		W
T.H.D.	P_{OUT} = 0.05W/Channel, f = 1 kHz		0.25		%
	P_{OUT} = 1W/Channel, f = 1 kHz		0.07	1	%
	P_{OUT} = 2W/Channel, f = 1 kHz		0.10		%
Offset Voltage			15		mV
Input Bias Current			100		nA
Input Impedance		3			MΩ
Open Loop Gain	R_S = 0Ω	66	90		dB
Output Swing			V_S–6		V_{P-P}
Channel Separation	C_F = 250μF, f = 1 kHz	50	70		dB
Ripple Rejection	f = 120 Hz, C_F = 250μF	60	70		dB
Current Limit			1.5		A
Slew Rate			1.4		V/μs
Equivalent Input Noise Voltage	R_S = 600Ω, 100 Hz – 10 kHz		3		μVrms

Note 1: For operation at ambient temperatures greater than 25°C the LM377 must be derated based on a maximum 150°C junction temperature using a thermal resistance which depends upon device mounting techniques.

Note 2: Dissipation characteristics are shown for four mounting configurations.

a. Infinite sink – 13.4°C/W

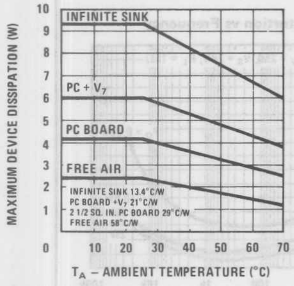
b. P.C. board +V_7 sink – 21°C/W. P.C. board is 2 1/2 square inches. Staver V_7 sink is 0.02 inch thick copper and has a radiating surface area of 10 square inches.

c. P.C. board only – 29°C/W. Device soldered to 2 1/2 square inch P.C. board.

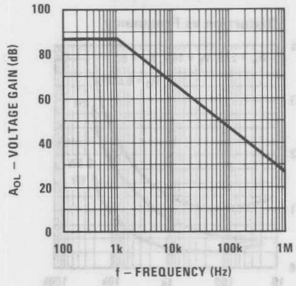
d. Free air – 58°C/W.

Typical Performance Characteristics

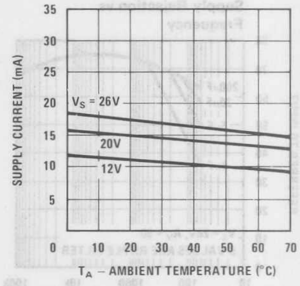
Maximum Dissipation vs Ambient Temperature



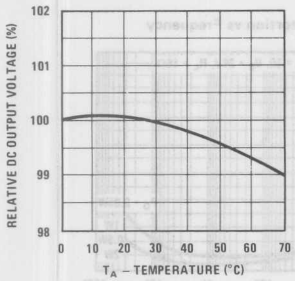
Open Loop Gain



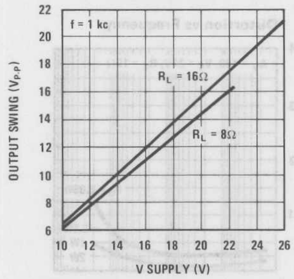
Supply Current vs Temperature



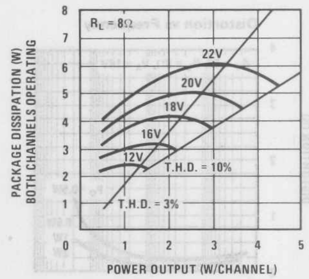
DC Output Level vs Temperature



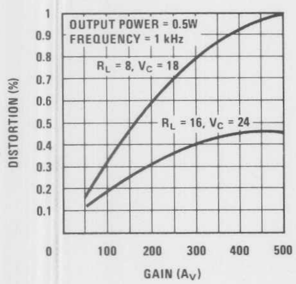
Output Swing vs V_S



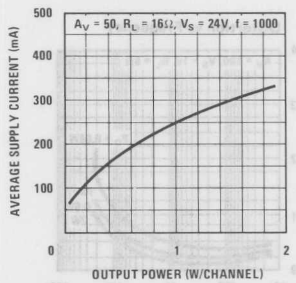
Power Dissipation vs Power Output



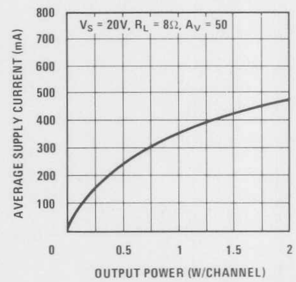
Distortion vs Gain



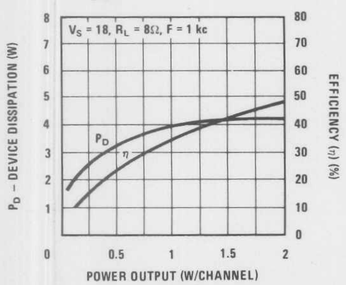
Supply Current vs Output Power



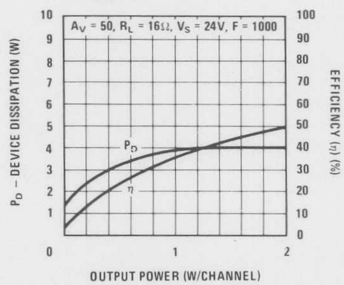
Supply Current vs P_{OUT}



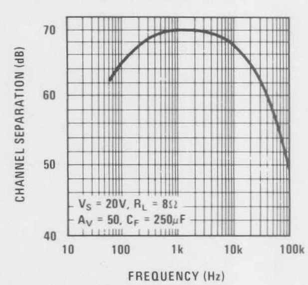
Dissipation and Efficiency vs P_{OUT}



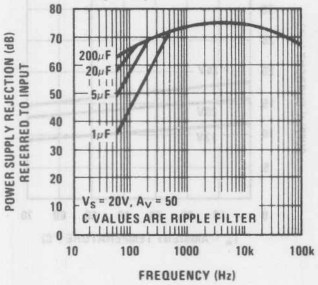
Dissipation and Efficiency vs P_{OUT}



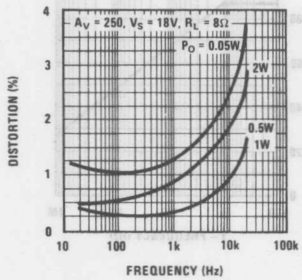
Channel Separation



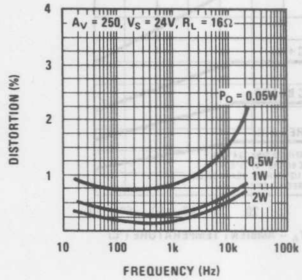
Frequency



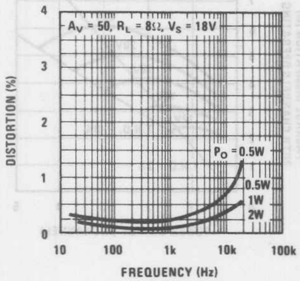
Distortion vs Frequency



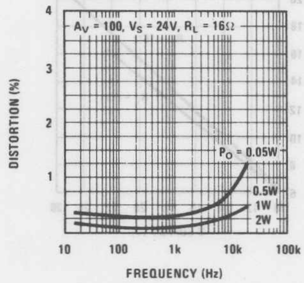
Distortion vs Frequency



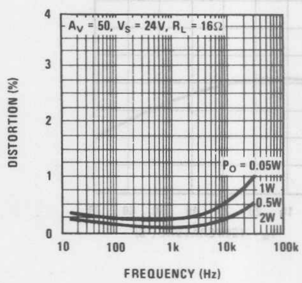
Distortion vs Frequency



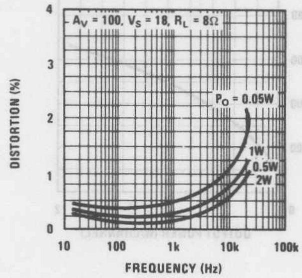
Distortion vs Frequency



Distortion vs Frequency

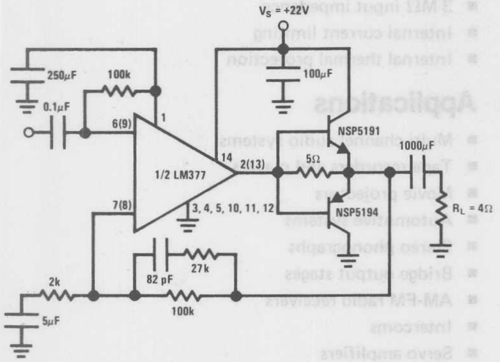


Distortion vs Frequency

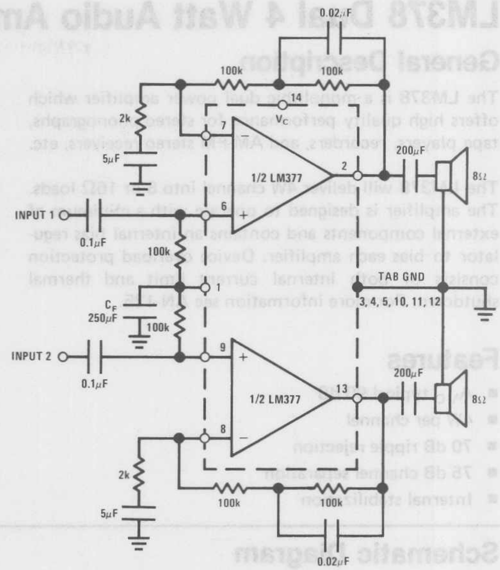


Typical Applications (Continued)

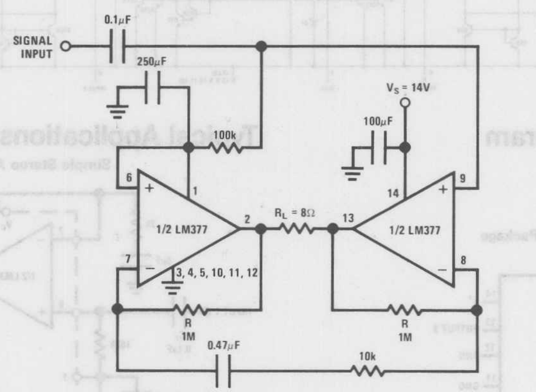
10W Per Channel Audio Amplifier



Simple Stereo Amplifier with Bass Boost



4W Bridge Amplifier



National Semiconductor

LM378 Dual 4 Watt Audio Amplifier

General Description

The LM378 is a monolithic dual power amplifier which offers high quality performance for stereo phonographs, tape players, recorders, and AM-FM stereo receivers, etc.

The LM378 will deliver 4W channel into 8 or 16Ω loads. The amplifier is designed to operate with a minimum of external components and contains an internal bias regulator to bias each amplifier. Device overload protection consists of both internal current limit and thermal shutdown. For more information see AN-125.

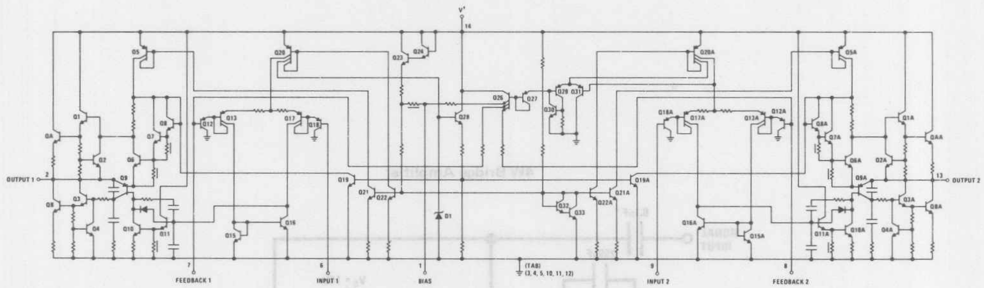
Features

- A_{VO} typical 90 dB
- 4W per channel
- 70 dB ripple rejection
- 75 dB channel separation
- Internal stabilization
- Self centered biasing
- 3 MΩ input impedance
- Internal current limiting
- Internal thermal protection

Applications

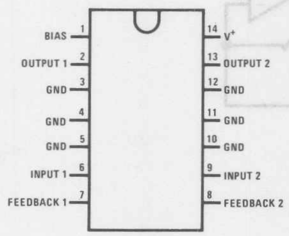
- Multi-channel audio systems
- Tape recorders and players
- Movie projectors
- Automotive systems
- Stereo phonographs
- Bridge output stages
- AM-FM radio receivers
- Intercoms
- Servo amplifiers
- Instrument systems

Schematic Diagram



Connection Diagram

Dual-In-Line Package

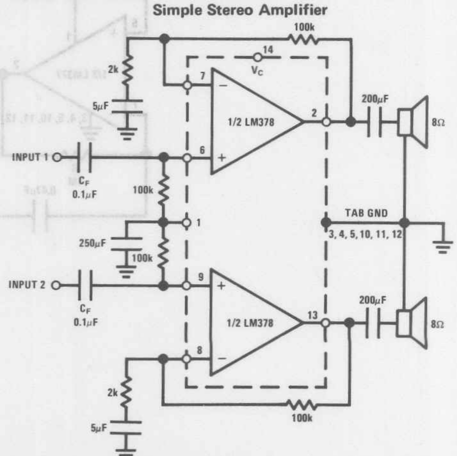


TOP VIEW

Order Number LM378N
See NS Package N14A

Typical Applications

Simple Stereo Amplifier



Absolute Maximum Ratings

Supply Voltage	35V
Input Voltage	0V – V_{SUPPLY}
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

$V_S = 24V$, $T_{TAB} = 25°C$, $R_L = 8\Omega$, $A_V = 50$ (34 dB), unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Total Supply Current	P_{OUT} = 0W		15	50	mA
	P_{OUT} = 1.5W/Channel		430	500	mA
DC Output Level			12		V
Supply Voltage		10			V
Output Power	T.H.D. = < 5%, $R_L = 8\Omega$	4	5		W
	T.H.D. = < 5%, $R_L = 16\Omega$	4	5		W*
T.H.D.	P_{OUT} = 0.05W/Channel, f = 1 kHz		0.25		%
	P_{OUT} = 1W/Channel, f = 1 kHz		0.07	1	%
	P_{OUT} 2W/Channel, f = 1 kHz		0.10		%
Offset Voltage			15		mV
Input Bias Current			100		nA
Input Impedance		3			MΩ
Open Loop Gain	$R_S = 0\Omega$	66	90		dB
Channel Separation	$C_F = 250\mu F$, f = 1 kHz	50	70		dB
Ripple Rejection	f = 120 Hz, $C_F = 250\mu F$	60	70		dB
Current Limit			1.5		A
Slew Rate			1.4		V/µs
Equivalent Input Noise Voltage	$R_S = 600\Omega$, 100 Hz – 10 kHz		3		µVrms

Note 1: For operation at ambient temperatures greater than 25°C the LM378 must be derated based on a maximum 150°C junction temperature using a thermal resistance which depends upon device mounting techniques.

Note 2: Dissipation characteristics are shown for four mounting configurations.

a. Infinite sink – 13.4°C/W

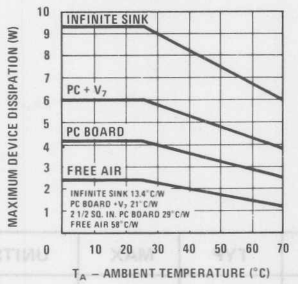
b. P.C. board $+V_7$ sink – 21°C/W. P.C. board is 2 1/2 square inches. Staver V_7 sink is 0.02 inch thick copper and has a radiating surface area of 10 square inches.

c. P.C. board only – 29°C/W. Device soldered to 2 1/2 square inch P.C. board.

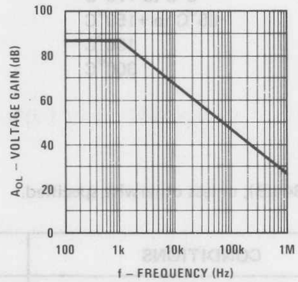
d. Free air – 58°C/W.

*Tested at V_S = 30V.

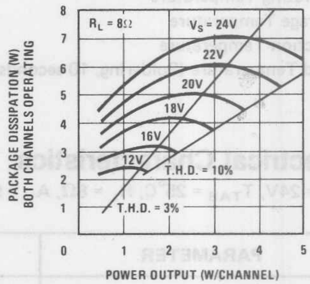
Ambient Temperature



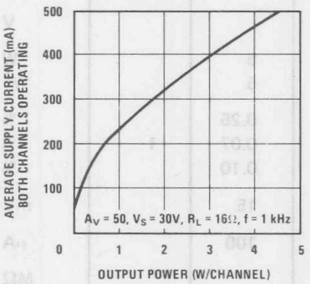
Open Loop Gain



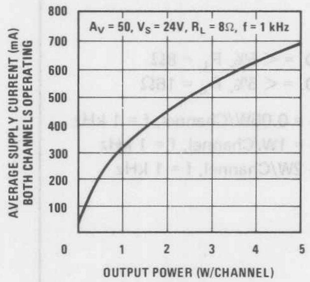
Power Dissipation vs Power Output



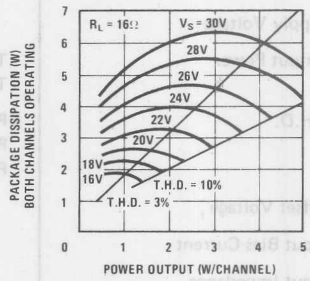
Supply Current vs Output Power



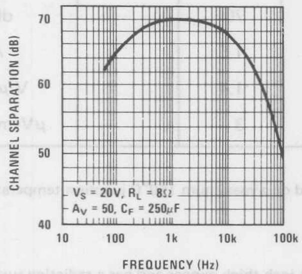
Supply Current vs Output Power



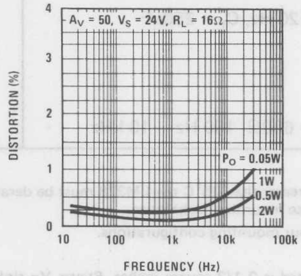
Power Dissipation vs Power Output



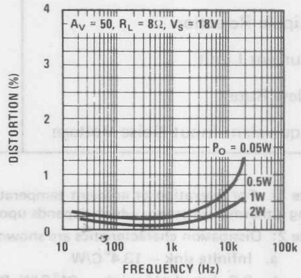
Channel Separation



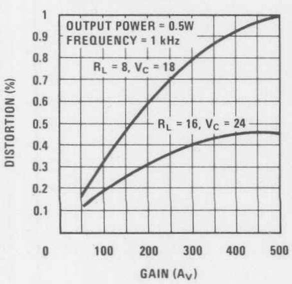
Distortion vs Frequency



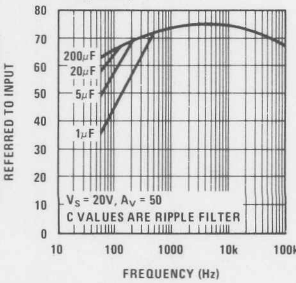
Distortion vs Frequency



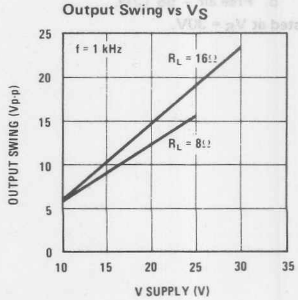
Distortion vs Gain



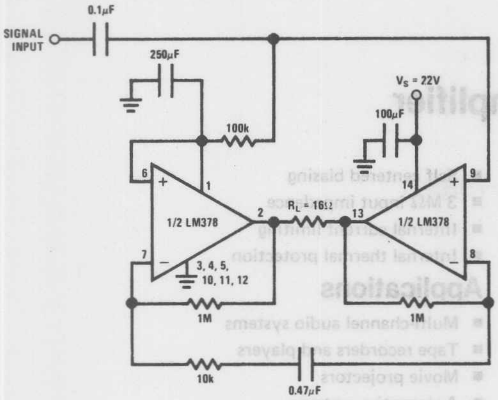
Supply Rejection vs Frequency



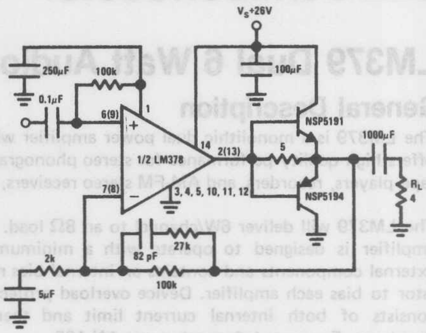
Output Swing vs V_S



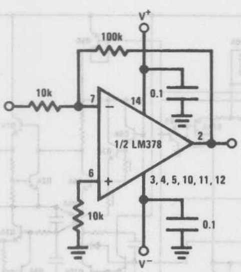
Typical Applications (Continued)



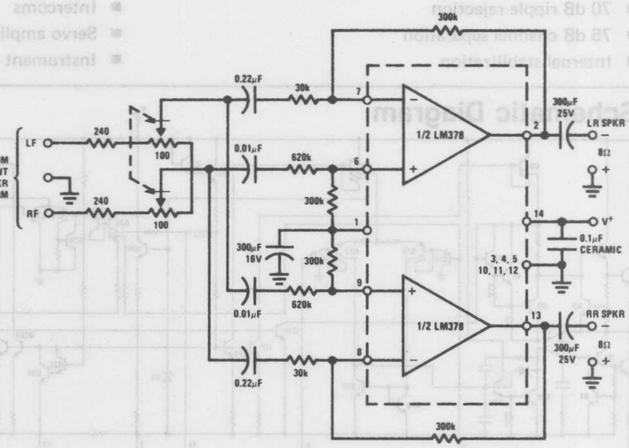
8W Bridge Amplifier



15W Per Channel Audio Amplifier



Power Op Amp
(Using Split Supplies)



Rear Speaker Ambience (4-Channel) Amplifier

National Semiconductor

LM379 Dual 6 Watt Audio Amplifier

General Description

The LM379 is a monolithic dual power amplifier which offers high quality performance for stereo phonographs, tape players, recorders, and AM-FM stereo receivers, etc.

The LM379 will deliver 6W/channel to an 8Ω load. The amplifier is designed to operate with a minimum of external components and contains an internal bias regulator to bias each amplifier. Device overload protection consists of both internal current limit and thermal shutdown. For more information, see AN-125.

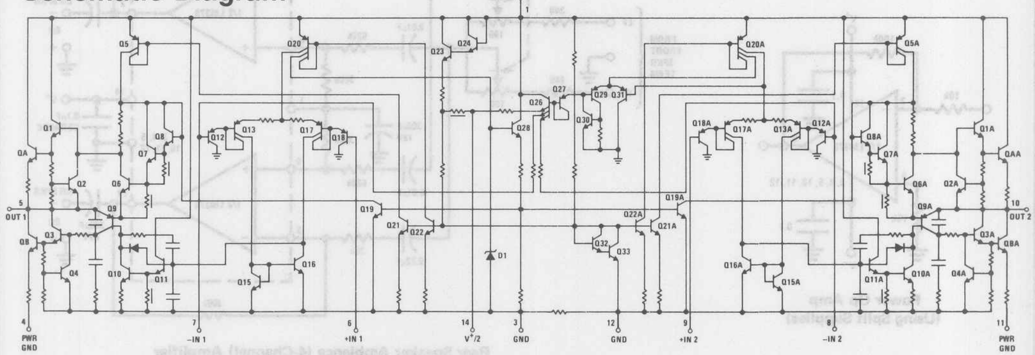
Features

- A_{VO} typical 90 dB
- 6W per channel
- 70 dB ripple rejection
- 75 dB channel separation
- Internal stabilization
- Self centered biasing
- 3 MΩ input impedance
- Internal current limiting
- Internal thermal protection

Applications

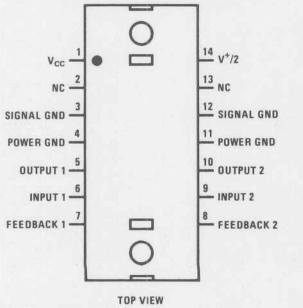
- Multi-channel audio systems
- Tape recorders and players
- Movie projectors
- Automotive systems
- Stereo phonographs
- Bridge output stages
- AM-FM radio receivers
- Intercoms
- Servo amplifiers
- Instrument systems

Schematic Diagram



Connection Diagram

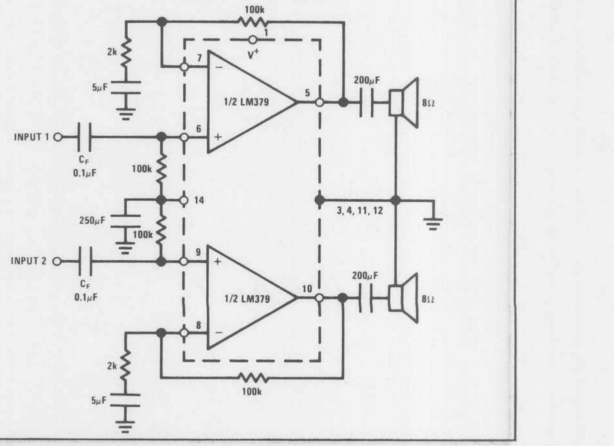
Dual-In-Line Power Package



Order Number LM379S
See NS Package S14A

Typical Applications

Simple Stereo Amplifier



Absolute Maximum Ratings

Supply Voltage	35V
Input Voltage	0V – V_{SUPPLY}
Operating Temperature	0°C to +70°C
Storage Temperature	–65°C to +150°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

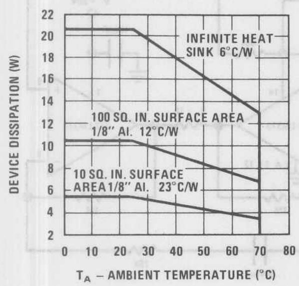
V_S = 28V, T_{TAB} = 25°C, R_L = 8Ω, A_V = 50 (34 dB), unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Total Supply Current	P_{OUT} = 0W		15	65	mA
	P_{OUT} = 1.5W/Channel		430		mA
DC Output Level			14		V
Supply Voltage		10			V
Output Power	T.H.D. = 5%		6		W
	T.H.D. = 10%	6	7		W
T.H.D.	P_{OUT} = 1W/Channel, f = 1 kHz		0.07	1	%
	P_{OUT} = 4W/Channel, f = 1 kHz		0.2		%
Offset Voltage			15		mV
Input Bias Current			100		nA
Input Impedance		3			MΩ
Open Loop Gain	R_S = 0Ω	66	90		dB
Channel Separation	C_F = 250μF, f = 1 kHz	50	70		dB
Ripple Rejection	f = 120 Hz, C_F = 250μF		70		dB
Current Limit			1.5		A
Slew Rate			1.4		V/μs
Equivalent Input Noise Voltage	R_S = 600Ω, 100 Hz – 10 kHz		3		μVrms

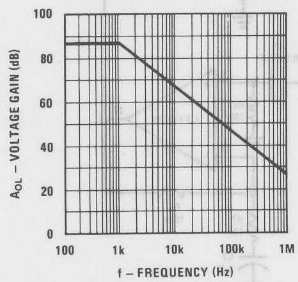
Note 1: For operation at ambient temperatures greater than 25°C the LM379 must be derated based on a maximum 150°C junction temperature using a thermal resistance which depends upon device mounting techniques. In most applications it is advisable to heat sink to the chassis. See curves.

Typical Performance Characteristics

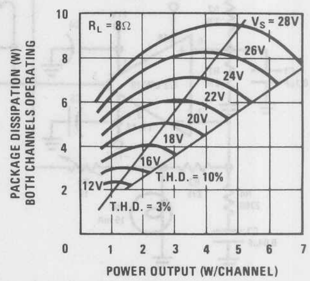
Maximum Dissipation vs Ambient Temperature



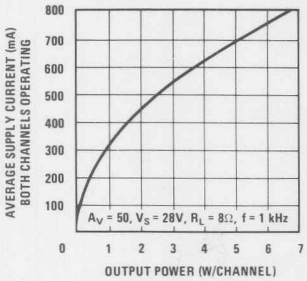
Open Loop Gain



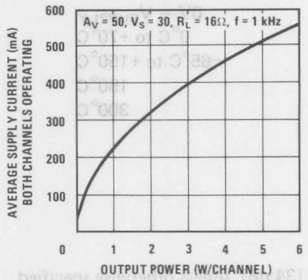
Power Dissipation vs Power Output



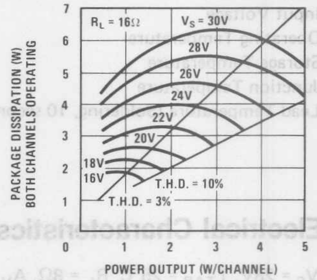
Supply Current vs Output Power



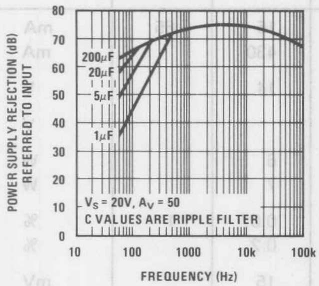
Supply Current vs P_{OUT}



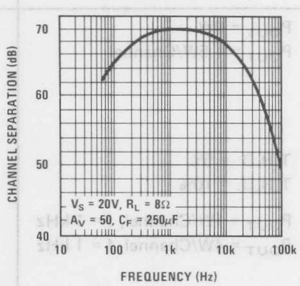
Power Dissipation vs Power Output



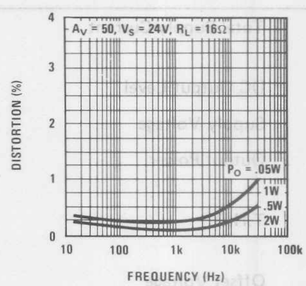
Supply Rejection vs Frequency



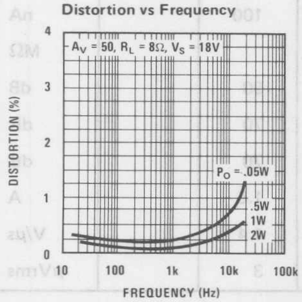
Channel Separation



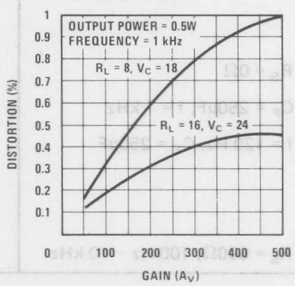
Distortion vs Frequency



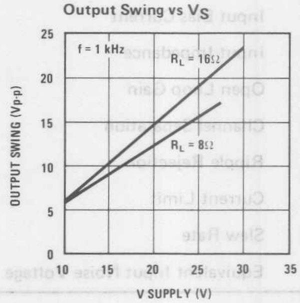
Distortion vs Frequency



Distortion vs Gain

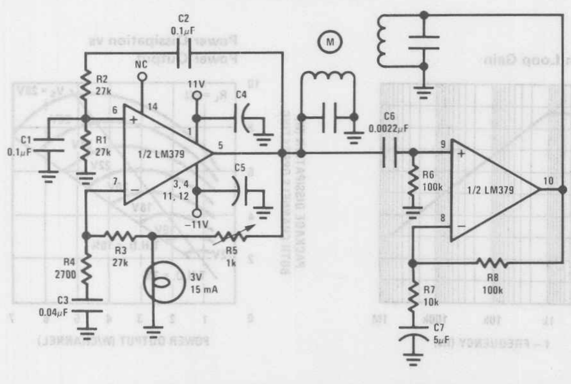


Output Swing vs V_S

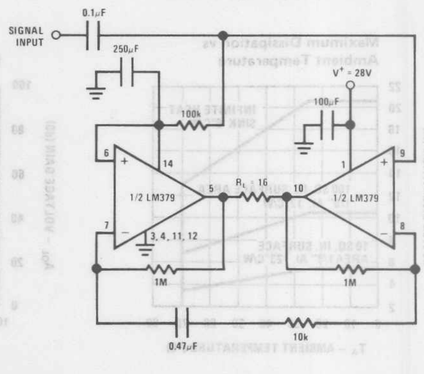


Typical Applications (Continued)

Two-Phase Motor Drive

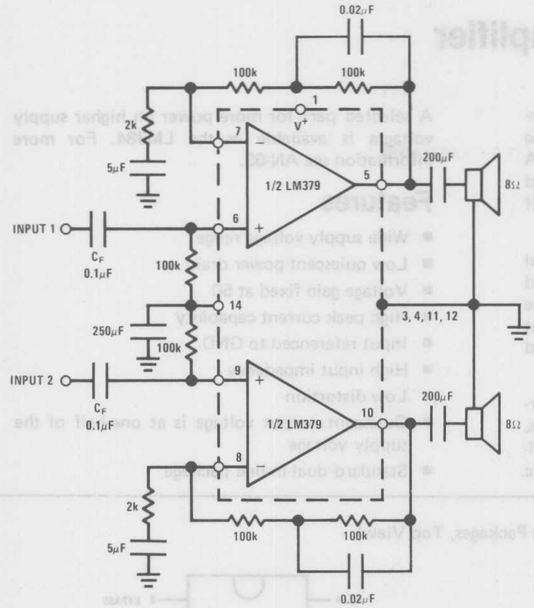


12W Bridge Amplifier

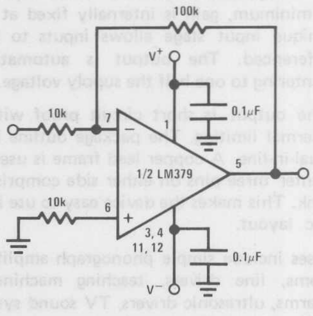


Typical Applications (Continued)

Simple Stereo Amplifier with Bass Boost



Power Op Amp (Using Split Supplies)



National Semiconductor

Audio/Radio Circuits

LM380 Audio Power Amplifier

General Description

The LM380 is a power audio amplifier for consumer application. In order to hold system cost to a minimum, gain is internally fixed at 34 dB. A unique input stage allows inputs to be ground referenced. The output is automatically self centering to one half the supply voltage.

The output is short circuit proof with internal thermal limiting. The package outline is standard dual-in-line. A copper lead frame is used with the center three pins on either side comprising a heat sink. This makes the device easy to use in standard p-c layout.

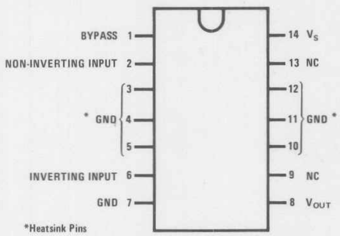
Uses include simple phonograph amplifiers, intercoms, line drivers, teaching machine outputs, alarms, ultrasonic drivers, TV sound systems, AM-FM radio, small servo drivers, power converters,etc.

A selected part for more power on higher supply voltages is available as the LM384. For more information see AN-69.

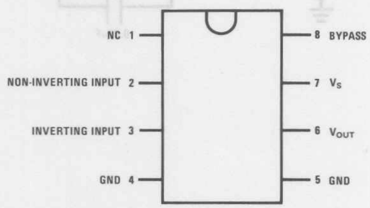
Features

- Wide supply voltage range
- Low quiescent power drain
- Voltage gain fixed at 50
- High peak current capability
- Input referenced to GND
- High input impedance
- Low distortion
- Quiescent output voltage is at one-half of the supply voltage
- Standard dual-in-line package

Connection Diagrams (Dual-In-Line Packages, Top View)



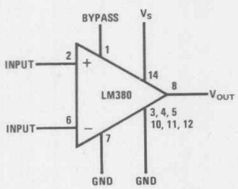
Order Number LM380N
See NS Package N14A



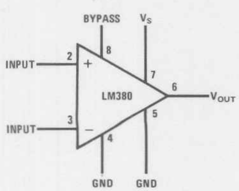
Order Number LM380N-8
See NS Package N08B

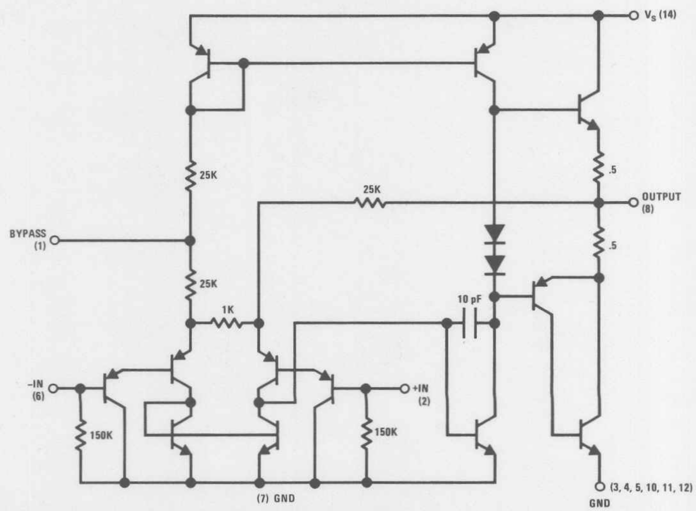
Block and Schematic Diagrams

LM380N



LM380N-8





Absolute Maximum Ratings

Supply Voltage	22V
Peak Current	1.3A
Package Dissipation 14-Pin DIP (Notes 6 and 7)	10W
Input Voltage	±0.5V
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Junction Temperature	+150°C
Lead Temperature (Soldering, 10 sec)	+300°C

Electrical Characteristics (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Power	$P_{OUT(RMS)}$	(Notes 3, 4) $R_L = 8\Omega$, THD = 3%	2.5			W
Gain	A_V		40	50	60	V/V
Output Voltage Swing	V_{OUT}	$R_L = 8\Omega$		14		$V_{p\text{-}p}$
Input Resistance	Z_{IN}			150k		Ω
Total Harmonic Distortion	THD	(Note 4, 5)		0.2		%
Power Supply Rejection Ratio	PSRR	(Note 2)		38		dB
Supply Voltage	V_S	(Note 8)	10		22	V
Bandwidth	BW	$P_{OUT} = 2W$, $R_L = 8\Omega$		100k		Hz
Quiescent Supply Current	I_Q			7	25	mA
Quiescent Output Voltage	V_{OUTQ}		8	9.0	10	V
Bias Current	I_{BIAS}	Inputs Floating		100		nA
Short Circuit Current	I_{SC}			1.3		A

Note 1: $V_S = 18V$ and $T_A = 25°C$ unless otherwise specified.

Note 2: Rejection ratio referred to the output with $C_{BYPASS} = 5\ \mu F$.

Note 3: With device Pins 3, 4, 5, 10, 11, 12 soldered into a 1/16" epoxy glass board with 2 ounce copper foil with a minimum surface of 6 square inches.

Note 4: If oscillation exists under some load conditions, add 2.7Ω and 0.1 μfd series network from Pin 8 to Gnd.

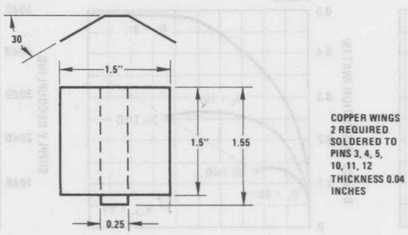
Note 5: $C_{BYPASS} = 0.47\ \mu fd$ on Pin 1.

Note 6: The maximum junction temperature of the LM380 is 150°C.

Note 7: The package is to be derated at 12°C/W junction to heat sink pins.

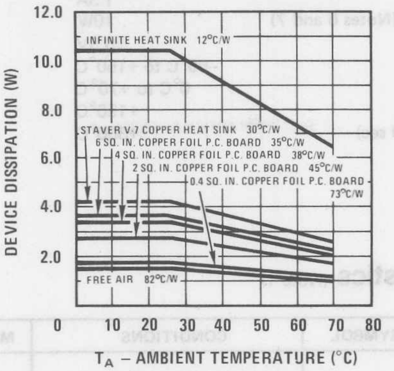
Note 8: Can select for 8V operation.

Heat Sink Dimensions

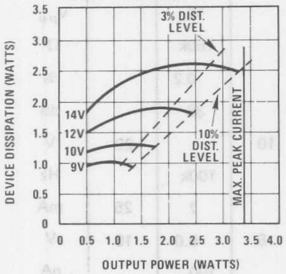


Typical Performance Characteristics

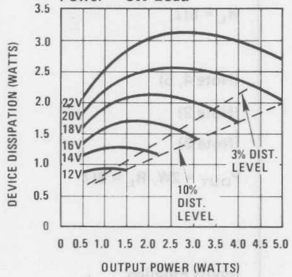
Device Dissipation vs Ambient Temperature



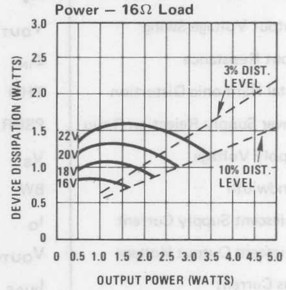
Device Dissipation vs Output Power — 4Ω Load



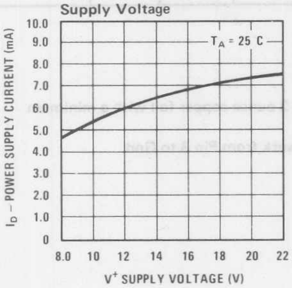
Device Dissipation vs Output Power — 8Ω Load



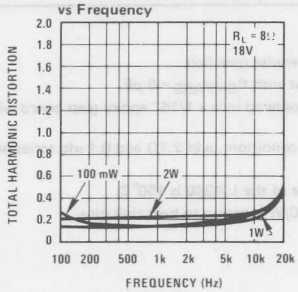
Device Dissipation vs Output Power — 16Ω Load



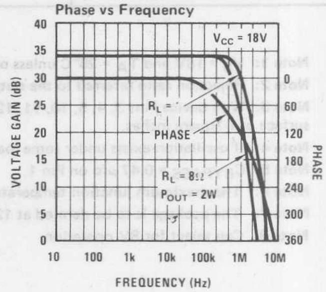
Power Supply Current vs Supply Voltage



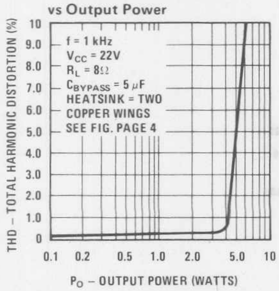
Total Harmonic Distortion vs Frequency



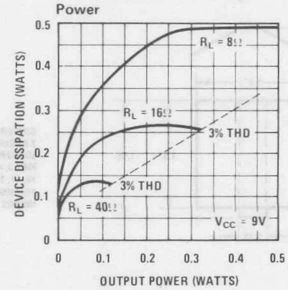
Output Voltage Gain and Phase vs Frequency



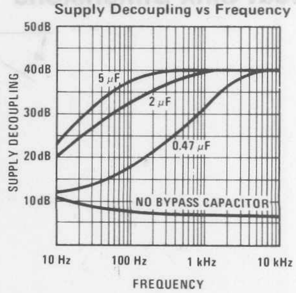
Total Harmonic Distortion vs Output Power



Device Dissipation vs Output Power

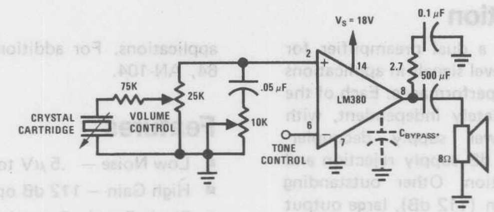


Supply Decoupling vs Frequency

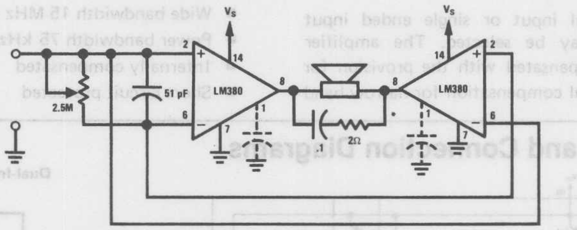


Typical Applications

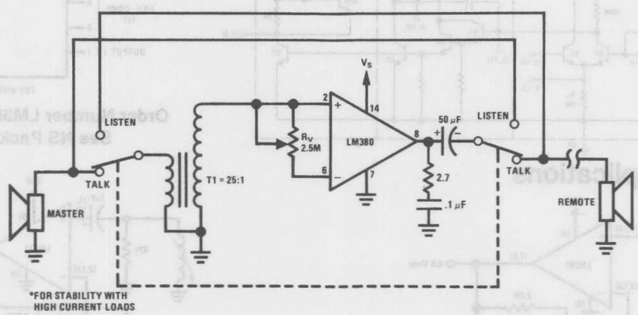
Phono Amplifier



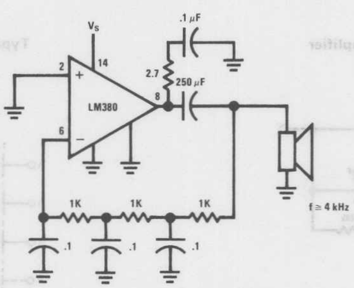
Bridge Amplifier



Intercom



Phase Shift Oscillator



LM381/LM381A Low Noise Dual Preamplifier

General Description

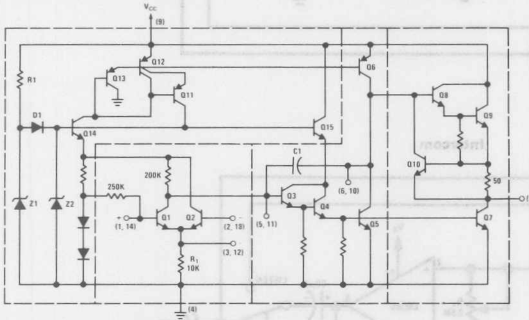
The LM381/LM381A is a dual preamplifier for the amplication of low level signals in applications requiring optimum noise performance. Each of the two amplifiers is completely independent, with individual internal power supply decoupler-regulator, providing 120 dB supply rejection and 60 dB channel separation. Other outstanding features include high gain (112 dB), large output voltage swing (V_{CC} −2V) p-p, and wide power bandwidth (75 kHz, $20V_{P-P}$). The LM381/LM381A operates from a single supply across the wide range of 9 to 40V.

Either differential input or single ended input configurations may be selected. The amplifier is internally compensated with the provision for additional external compensation for narrow band applications. For additional information see AN-64, AN-104.

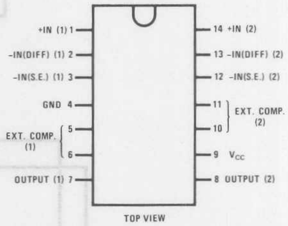
Features

- Low Noise — .5 μV total input noise
- High Gain — 112 dB open loop
- Single Supply Operation
- Wide supply range 9–40V
- Power supply rejection 120 dB
- Large output voltage swing (V_{CC} −2V)$_{p-p}$
- Wide bandwidth 15 MHz unity gain
- Power bandwidth 75 kHz, 20 V_{p-p}
- Internally compensated
- Short circuit protected

Schematic and Connection Diagrams

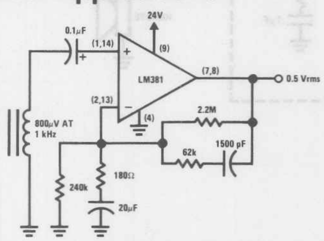


Dual-In-Line Package

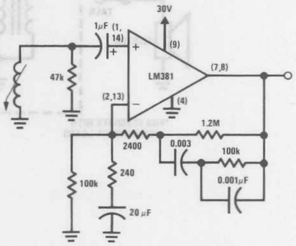


Order Number LM381N or LM381AN
See NS Package N14A

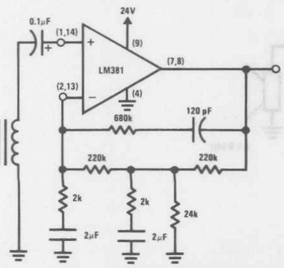
Typical Applications



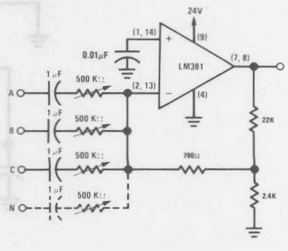
Typical Tape Playback Amplifier



Typical Magnetic Phono Preamp



Two-Pole Fast Turn-On NAB Tape Preamp



Audio Mixer

Absolute Maximum Ratings

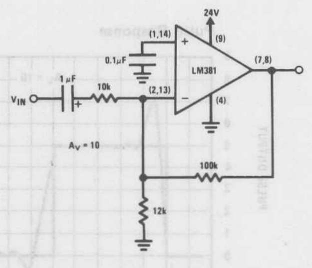
Supply Voltage	+40V
Power Dissipation (Note 1)	715 mW
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics $T_A = 25°C$, $V_{CC} = 14V$, unless otherwise stated.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Gain	Open Loop (Differential Input), f = 100 Hz		160,000		V/V
	Open Loop (Single Ended), f = 100 Hz		320,000		V/V
Supply Current	V_{CC} 9 to 40V, $R_L = \infty$		10		mA
Input Resistance					
(Positive Input)			100		kΩ
(Negative Input)			200		kΩ
Input Current					
(Negative Input)			0.5		μA
Output Resistance	Open Loop		150		Ω
Output Current	Source		8		mA
	Sink		2		mA
Output Voltage Swing	Peak-to-Peak		$V_{CC} - 2$		V
Unity Gain Bandwidth			15		MHz
Power Bandwidth	20 V_{p-p} (V_{CC} = 24V)		75		kHz
Maximum Input Voltage	Linear Operation			300	mVrms
Supply Rejection Ratio	f = 1 kHz		120		dB
Channel Separation	f = 1 kHz		60		dB
Total Harmonic Distortion	60 dB Gain, f = 1 kHz		0.1		%
Total Equivalent Input Noise	$R_S = 600\Omega$, 10 – 10,000 Hz (Single Ended Input, Flat Gain Circuit, A_V = 1000)				
LM381A			0.5	0.7	μVrms
LM381			0.5	1.0	μVrms

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 175°C/W junction to ambient.

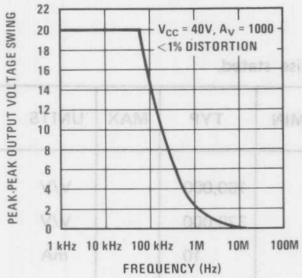
Typical Applications (Continued)



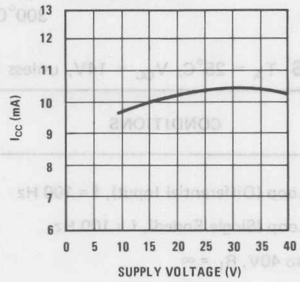
Ultra-Low Distortion Amplifier
(A_V = 10, THD < 0.05%, V_{OUT} = 3 V_{RMS})

Typical Performance Characteristics

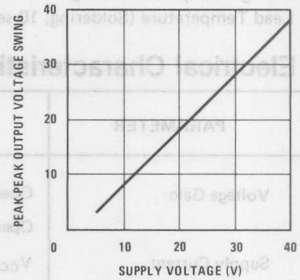
Large Signal Frequency Response



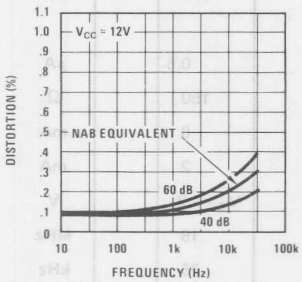
Vcc vs Icc



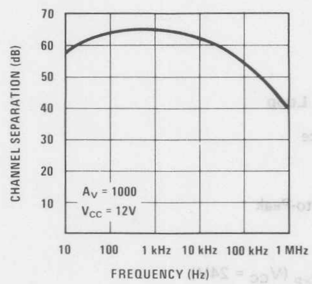
P–P Output Voltage Swing vs V_{CC}



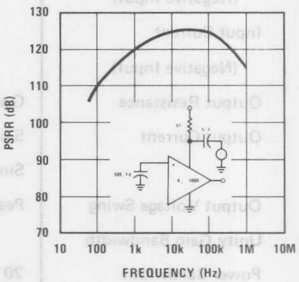
% Distortion



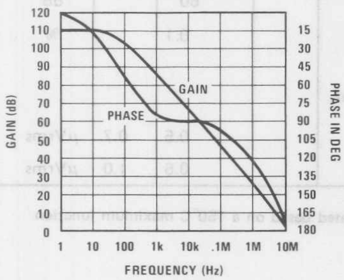
Channel Separation



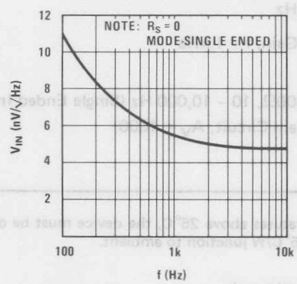
PSRR vs Frequency



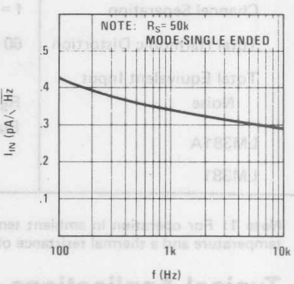
Gain and Phase Response



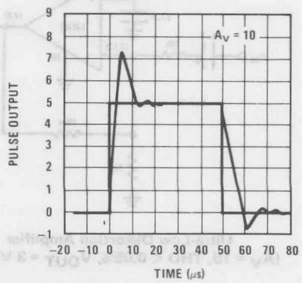
Noise Voltage vs Frequency



Noise Current vs Frequency



Pulse Response



National Semiconductor

LM382 Low Noise Dual Preamplifier

General Description

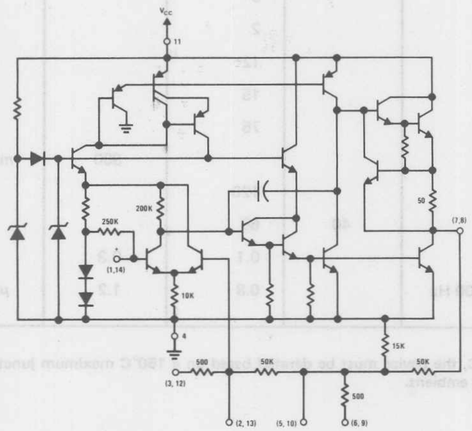
The LM382 is a dual preamplifier for the application of low level signals in applications requiring optimum noise performance. Each of the two amplifiers is completely independent, with individual internal power supply decoupler-regulator, providing 120 dB supply rejection and 60 dB channel separation. Other outstanding features include high gain (100 dB), and wide power bandwidth (75 kHz, 20 Vp-p). The LM382 operates from a single supply across the wide range of 9 to 40V.

A resistor matrix is provided on the chip to allow the user to select a variety of closed loop gain options and frequency response characteristics such as flat-band, NAB or RIAA equalization. The circuit is supplied in the 14 lead dual-in-line package.

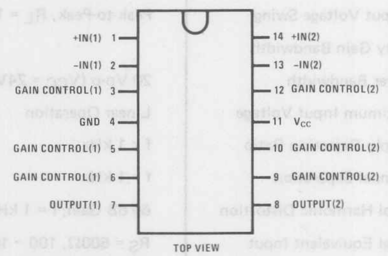
Features

- Low noise – 0.8 μV total equivalent input noise
- High gain – 100 dB open loop
- Single supply operation
- Wide supply range 9 to 40V
- Power supply rejection – 120 dB
- Large output voltage swing
- Wide bandwidth – 15 MHz unity gain
- Power bandwidth – 75 kHz, 20 $V_{p\text{-}p}$
- Internally compensated
- Short circuit protected.

Schematic and Connection Diagrams

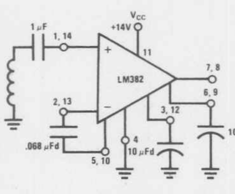


Dual-In-Line Package

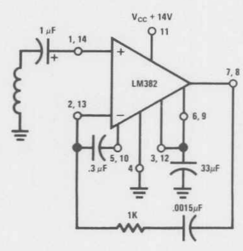


Order Number LM382N
See NS Package N14A

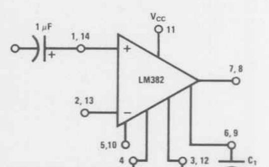
Typical Applications



Tape Preamp (NAB Equalization)



Phono Preamp (RIAA Equalization)



CAPACITOR	GAIN
C1 Only	40 dB
C2 Only	55 dB
C1 & C2	80 dB

Flat Response – Fixed Gain Configuration

Absolute Maximum Ratings

Supply Voltage	+40V
Power Dissipation (Note 1)	715 mW
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics

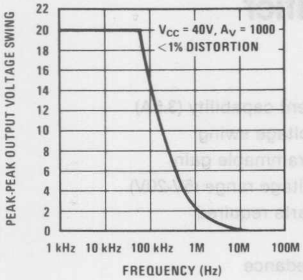
$T_A = 25°C$, $V_{CC} = 14V$, unless otherwise stated.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Gain	Open Loop, f = 100 Hz		100,000		V/V
Supply Current	V_{CC} 9 to 40V, $R_L = \infty$		10	16	mA
Output DC Voltage			6		V
Input Resistance					
(Positive Input)			100		kΩ
(Negative Input)			200		kΩ
Input Current					
(Negative Input)			0.5		μA
Output Resistance	Open Loop		150		Ω
Output Current	Source		8		mA
	Sink		2		mA
Output Voltage Swing	Peak-to-Peak, R_L = 10k		12		V
Unity Gain Bandwidth			15		MHz
Power Bandwidth	20 Vp-p (V_{CC} = 24V)		75		kHz
Maximum Input Voltage	Linear Operation			300	mVrms
Supply Rejection Ratio	f = 1 kHz		120		dB
Channel Separation	f = 1 kHz	40	60		dB
Total Harmonic Distortion	60 dB Gain, f = 1 kHz		0.1	0.3	%
Total Equivalent Input Noise	R_S = 600Ω, 100 − 10,000 Hz (Flat Response Circuit)		0.8	1.2	μVrms

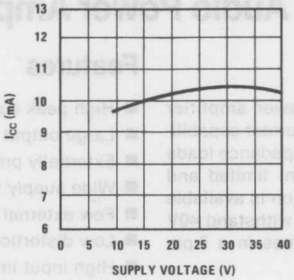
Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 175°C/W junction to ambient.

Typical Performance Characteristics

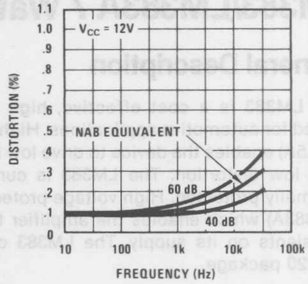
Large Signal Frequency Response



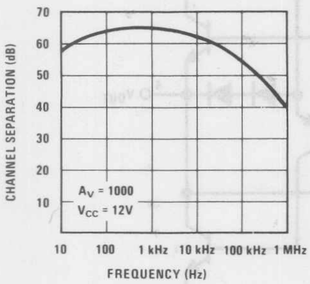
V_{CC} vs I_{CC}



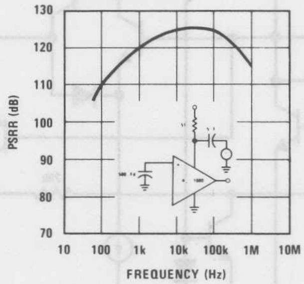
% Distortion



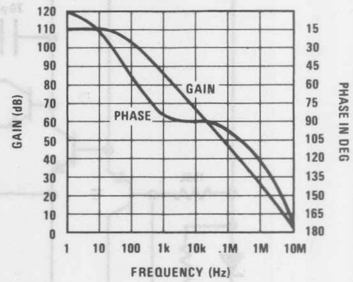
Channel Separation



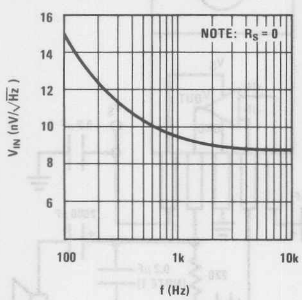
PSRR vs Frequency



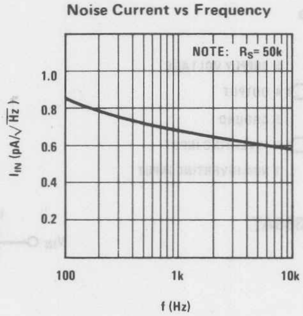
Gain and Phase Response



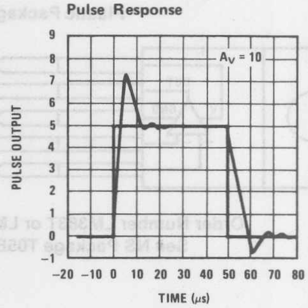
Noise Voltage vs Frequency



Noise Current vs Frequency



Pulse Response



National Semiconductor

LM383/LM383A 7 Watt Audio Power Amplifier

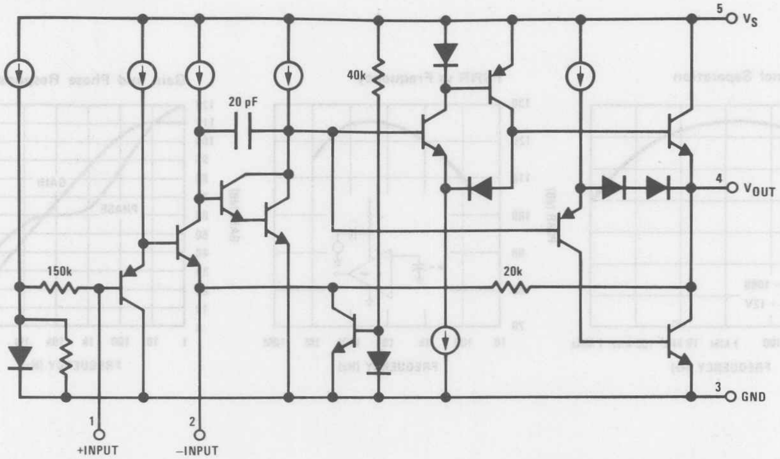
General Description

The LM383 is a cost effective, high power amplifier suited for automotive applications. High current capability (3.5A) enables the device to drive low impedance loads with low distortion. The LM383 is current limited and thermally protected. High voltage protection is available (LM383A) which enables the amplifier to withstand 40V transients on its supply. The LM383 comes in a 5-pin TO-220 package.

Features

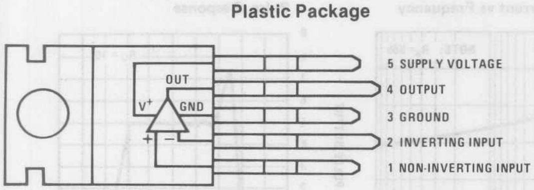
- High peak current capability (3.5A)
- Large output voltage swing
- Externally programmable gain
- Wide supply voltage range (5V-20V)
- Few external parts required
- Low distortion
- High input impedance
- No turn-on transients
- High voltage protection available (LM383A)
- Low noise
- AC short circuit protected

Equivalent Schematic



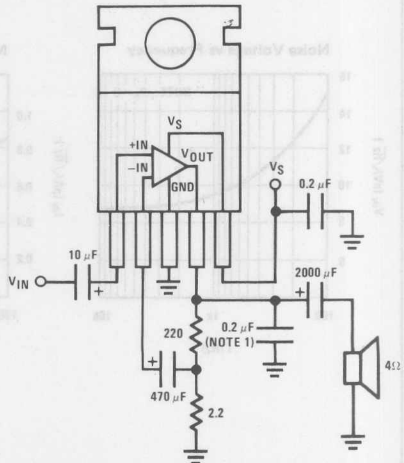
Connection Diagram

Plastic Package



Order Number LM383T or LM383AT
See NS Package T05B

Typical Applications



Absolute Maximum Ratings

Peak Supply Voltage (50 ms)	
LM383A (Note 2)	40V
LM383	25V
Operating Supply Voltage	20V
Output Current	
Repetitive	3.5A
Non-repetitive	4.5A
Input Voltage	±0.5V
Power Dissipation (Note 3)	15W
Operating Temperature	0°C to +70°C
Storage Temperature	−60°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics $V_S = 14.4V$, $T_{TAB} = 25°C$, $A_V = 100$ (40 dB), $R_L = 4\Omega$, unless otherwise specified

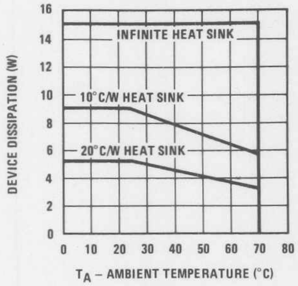
Parameter	Conditions	Min	Typ	Max	Units
DC Output Level		6.4	7.2	8	V
Quiescent Supply Current	Excludes Current in Feedback Resistors		45	80	mA
Supply Voltage Range		5		20	V
Input Resistance			150		kΩ
Bandwidth	Gain = 40 dB		30		kHz
Output Power	$V_S = 13.2V$, f = 1 kHz				
	$R_L = 4\Omega$, THD = 10%		4.7		W
	$R_L = 2\Omega$, THD = 10%		7.2		W
	$V_S = 13.8V$, f = 1 kHz				
	$R_L = 4\Omega$, THD = 10%		5.1		W
	$R_L = 2\Omega$, THD = 10%		7.8		W
	$V_S = 14.4V$, f = 1 kHz				
	$R_L = 4\Omega$, THD = 10%	4.8	5.5		W
	$R_L = 2\Omega$, THD = 10%	7	8.6		W
	$R_L = 1.6\Omega$, THD = 10%		9.3		W
	$V_S = 16V$, f = 1 kHz				
	$R_L = 4\Omega$, THD = 10%		7		W
	$R_L = 2\Omega$, THD = 10%		10.5		W
	$R_L = 1.6\Omega$, THD = 10%		11		W
THD	$P_o = 2W$, $R_L = 4\Omega$, f = 1 kHz		0.2		%
	$P_o = 4W$, $R_L = 2\Omega$, f = 1 kHz		0.2		%
Ripple Rejection	$R_S = 50\Omega$, f = 100 Hz	30	40		dB
	$R_S = 50\Omega$, f = 1 kHz		44		dB
Input Noise Voltage	$R_S = 0$, 15 kHz Bandwidth		2		μV
Input Noise Current	$R_S = 100\ k\Omega$, 15 kHz Bandwidth		40		pA

Note 1: A 0.2 μF capacitor should be placed as close as possible to pins 3 and 4 for stability.

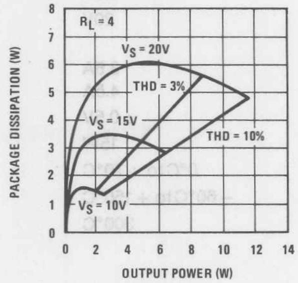
Note 2: The LM383 shuts down above 25V.

Note 3: For operating at elevated temperatures, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 4°C/W junction to case.

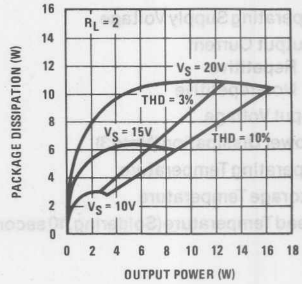
Ambient Temperature



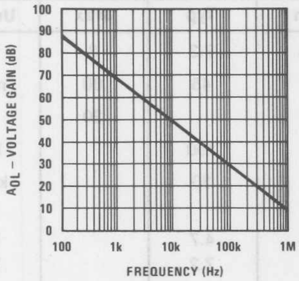
Output Power



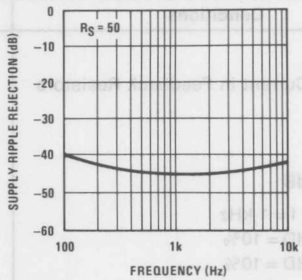
Output Power



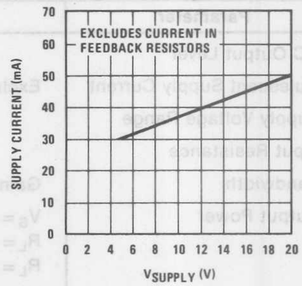
Open Loop Gain vs Frequency



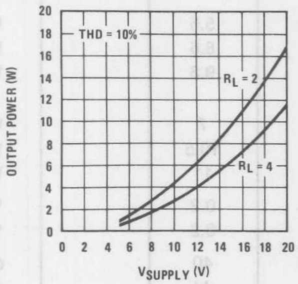
Supply Ripple Rejection vs Frequency



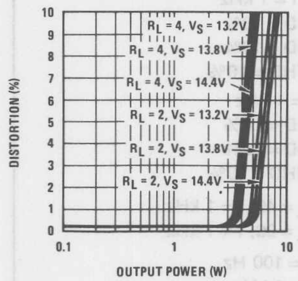
Supply Current vs Supply Voltage



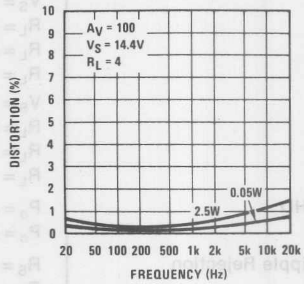
Output Power vs Supply Voltage



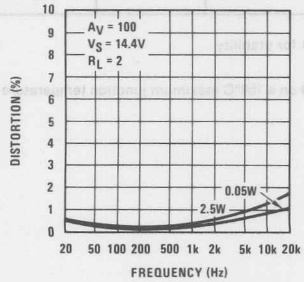
Distortion vs Output Power



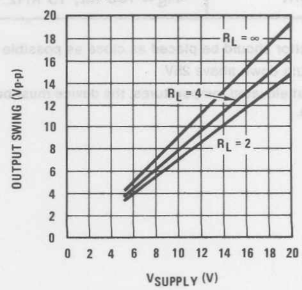
Distortion vs Frequency



Distortion vs Frequency

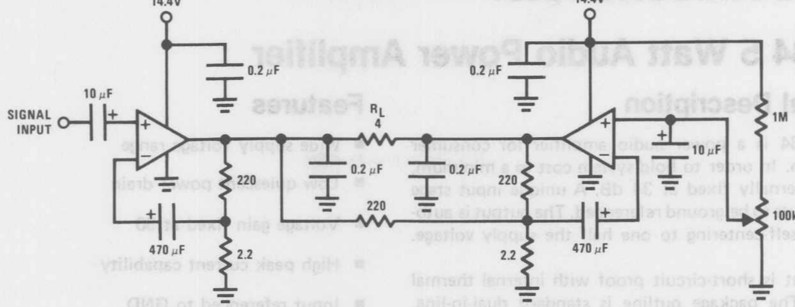


Output Swing vs Supply Voltage

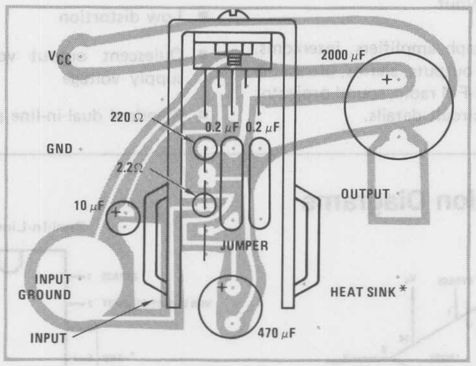


Typical Applications (Continued)

16W Bridge Amplifier



Component Layout



* Staver V-5

National Semiconductor

Audio/Radio Circuits

LM384 5 Watt Audio Power Amplifier

General Description

The LM384 is a power audio amplifier for consumer application. In order to hold system cost to a minimum, gain is internally fixed at 34 dB. A unique input stage allows inputs to be ground referenced. The output is automatically self-centering to one half the supply voltage.

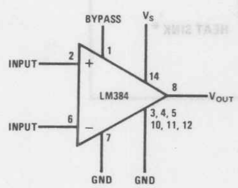
The output is short-circuit proof with internal thermal limiting. The package outline is standard dual-in-line. A copper lead frame is used with the center three pins on either side comprising a heat sink. This makes the device easy to use in standard p-c layout.

Uses include simple phonograph amplifiers, intercoms, line drivers, teaching machine outputs, alarms, ultrasonic drivers, TV sound systems, AM-FM radio, sound projector systems, etc. See AN-69 for circuit details.

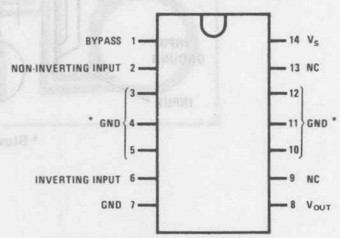
Features

- Wide supply voltage range
- Low quiescent power drain
- Voltage gain fixed at 50
- High peak current capability
- Input referenced to GND
- High input impedance
- Low distortion
- Quiescent output voltage is at one half of the supply voltage
- Standard dual-in-line package

Block and Connection Diagrams



Dual-In-Line Package

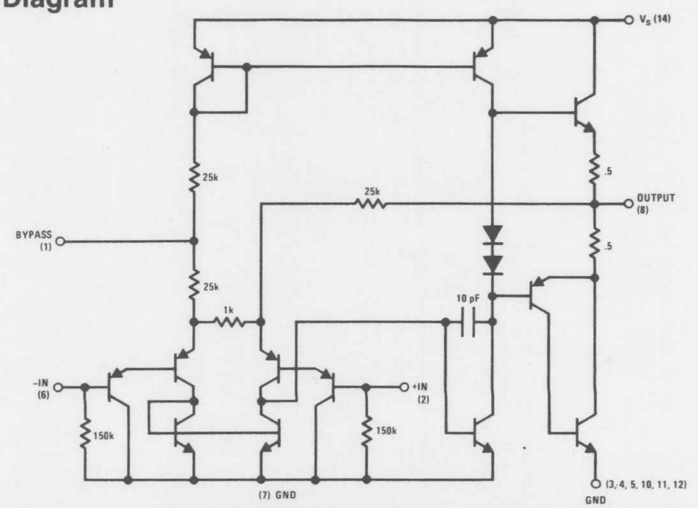


*Heatsink Pins

TOP VIEW

Order Number LM384N
See NS Package N14A

Schematic Diagram



Absolute Maximum Ratings

Supply Voltage	28V
Peak Current	1.3A
Power Dissipation	(See Notes 3 and 4)
Input Voltage	±0.5V
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Resistance (Z_{IN})			150		kΩ
Bias Current (I_{BIAS})	Inputs Floating		100		nA
Gain (A_V)		40	50	60	V/V
Output Power (P_{OUT})	THD = 10%, R_L = 8Ω	5	5.5		W
Quiescent Supply Current (I_Q)			8.5	25	mA
Quiescent Output Voltage ($V_{OUT\ Q}$)			11		V
Bandwidth (BW)	P_{OUT} = 2W, R_L = 8Ω		450		kHz
Supply Voltage (V^+)		12		26	V
Short Circuit Current (I_{SC})			1.3		A
Power Supply Rejection Ratio ($PSRR_{RTO}$) (Note 2)			31		dB
Total Harmonic Distortion (THD)	P_{OUT} = 4W, R_L = 8Ω		0.25	1.0	%

Note 1: V^+ = 22V and T_A = 25°C operating with a Staver V7 heat sink for 30 seconds.

Note 2: Rejection ratio referred to the output with C_{BYPASS} = 5µF, freq = 120 Hz.

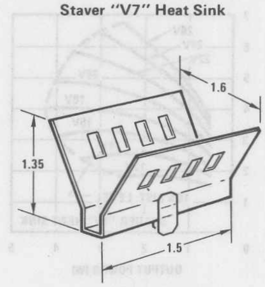
Note 3: The maximum junction temperature of the LM384 is 150°C.

Note 4: The package is to be derated at 12°C/W junction to heat sink pins.

Note 5: Output is fully protected against a shorted speaker condition at all voltages up to 22V.

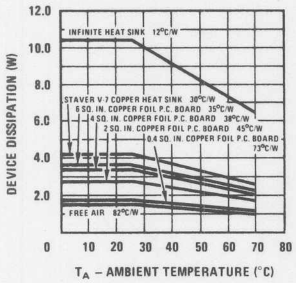
Heat Sink Dimensions

Staver "V7" Heat Sink

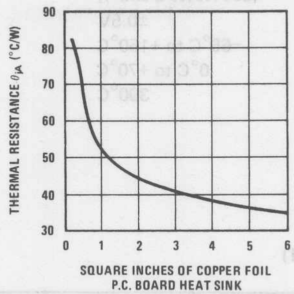


Typical Performance Characteristics

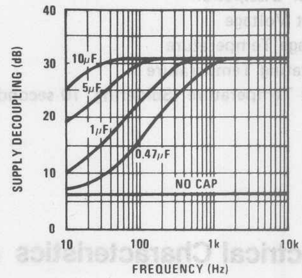
Device Dissipation vs Ambient Temperature



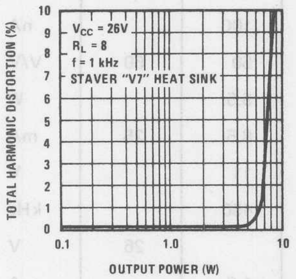
Thermal Resistance vs Square Inches



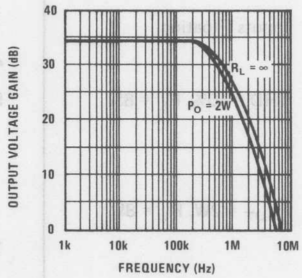
Supply Decoupling vs Frequency



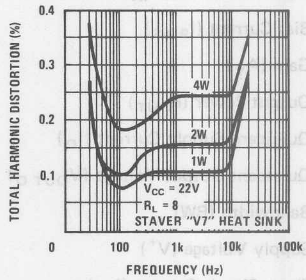
Total Harmonic Distortion vs Output Power



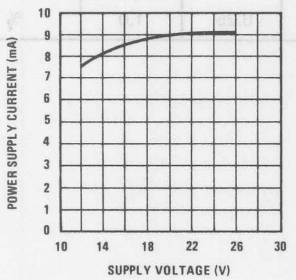
Output Voltage Gain vs Frequency



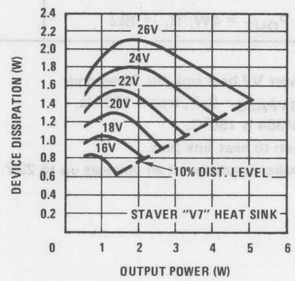
Total Harmonic Distortion vs Frequency



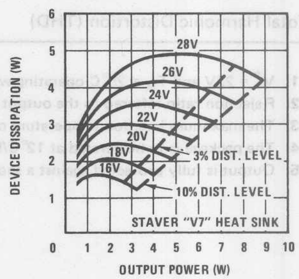
Power Supply Current vs Supply Voltage



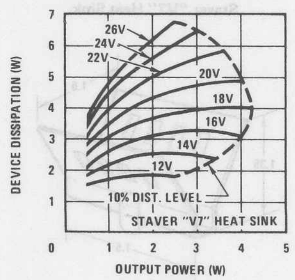
Device Dissipation vs Output Power—16Ω Load



Device Dissipation vs Output Power—8Ω Load

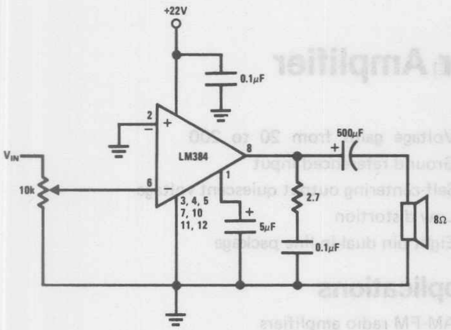


Device Dissipation vs Output Power—4Ω Load

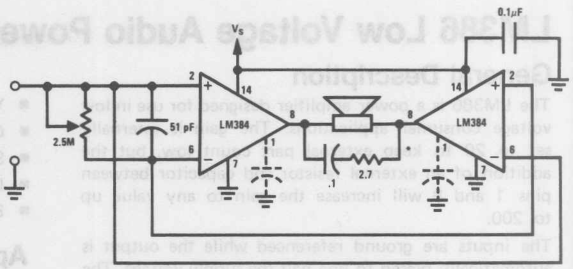


Typical Applications

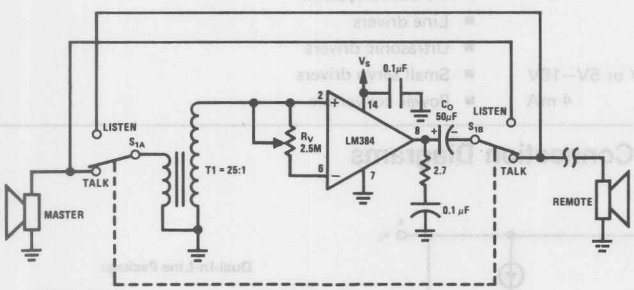
Typical 5W Amplifier



Bridge Amplifier

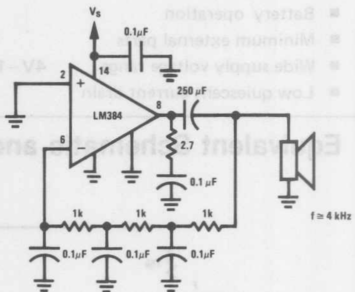


Intercom



*For stability with high current loads

Phase Shift Oscillator



LM386 Low Voltage Audio Power Amplifier

General Description

The LM386 is a power amplifier designed for use in low voltage consumer applications. The gain is internally set to 20 to keep external part count low, but the addition of an external resistor and capacitor between pins 1 and 8 will increase the gain to any value up to 200.

The inputs are ground referenced while the output is automatically biased to one half the supply voltage. The quiescent power drain is only 24 milliwatts when operating from a 6 volt supply, making the LM386 ideal for battery operation.

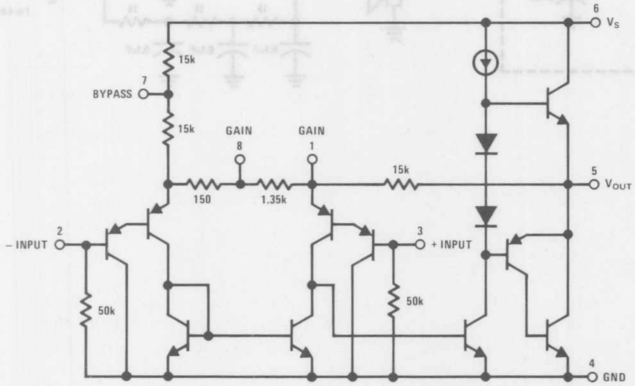
Features

- Battery operation
- Minimum external parts
- Wide supply voltage range 4V–12V or 5V–18V
- Low quiescent current drain 4 mA
- Voltage gains from 20 to 200
- Ground referenced input
- Self-centering output quiescent voltage
- Low distortion
- Eight pin dual-in-line package

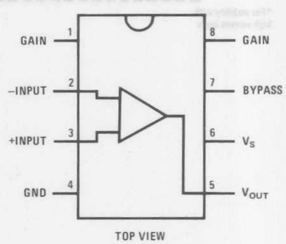
Applications

- AM-FM radio amplifiers
- Portable tape player amplifiers
- Intercoms
- TV sound systems
- Line drivers
- Ultrasonic drivers
- Small servo drivers
- Power converters

Equivalent Schematic and Connection Diagrams



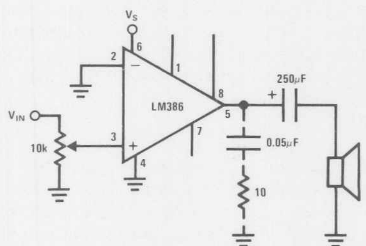
Dual-In-Line Package



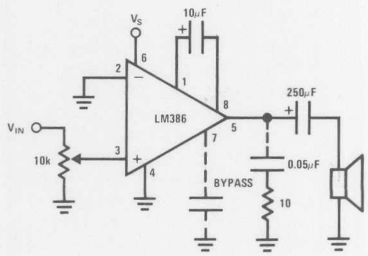
Order Number LM386N-1, LM386N-3 or LM386N-4
See NS Package N08B

Typical Applications

Amplifier with Gain = 20
Minimum Parts



Amplifier with Gain = 200



Absolute Maximum Ratings

Supply Voltage (LM386N)	15V
Supply Voltage (LM386N-4)	22V
Package Dissipation (Note 1) (LM386N-4)	1.25W
Package Dissipation (Note 2) (LM386)	660 mW
Input Voltage	±0.4V
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Junction Temperature	+150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Electrical Characteristics $T_A = 25°C$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage (V_S)					
LM386		4		12	V
LM386N-4		5		18	V
Quiescent Current (I_Q)	$V_S = 6V$, $V_{IN} = 0$		4	8	mA
Output Power (P_{OUT})					
LM386N-1	$V_S = 6V$, $R_L = 8\Omega$, THD = 10%	250	325		mW
LM386N-3	$V_S = 9V$, $R_L = 8\Omega$, THD = 10%	500	700		mW
LM386N-4	$V_S = 16V$, $R_L = 32\Omega$, THD = 10%	700	1000		mW
Voltage Gain (A_V)	$V_S = 6V$, f = 1 kHz		26		dB
	10μF from Pin 1 to 8		46		dB
Bandwidth (BW)	$V_S = 6V$, Pins 1 and 8 Open		300		kHz
Total Harmonic Distortion (THD)	$V_S = 6V$, $R_L = 8\Omega$, $P_{OUT} = 125\,mW$ f = 1 kHz, Pins 1 and 8 Open		0.2		%
Power Supply Rejection Ratio (PSRR)	$V_S = 6V$, f = 1 kHz, $C_{BYPASS} = 10\mu F$ Pins 1 and 8 Open, Referred to Output		50		dB
Input Resistance (R_{IN})			50		kΩ
Input Bias Current (I_{BIAS})	$V_S = 6V$, Pins 2 and 3 Open		250		nA

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 100°C/W junction to ambient.

Note 2: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 187°C junction to ambient.

Application Hints

GAIN CONTROL

To make the LM386 a more versatile amplifier, two pins (1 and 8) are provided for gain control. With pins 1 and 8 open the 1.35 kΩ resistor sets the gain at 20 (26 dB). If a capacitor is put from pin 1 to 8, bypassing the 1.35 kΩ resistor, the gain will go up to 200 (46 dB). If a resistor is placed in series with the capacitor, the gain can be set to any value from 20 to 200. Gain control can also be done by capacitively coupling a resistor (or FET) from pin 1 to ground.

Additional external components can be placed in parallel with the internal feedback resistors to tailor the gain and frequency response for individual applications. For example, we can compensate poor speaker bass response by frequency shaping the feedback path. This is done with a series RC from pin 1 to 5 (paralleling the internal 15kΩ resistor). For 6 dB effective bass boost: R ≅ 15kΩ, the lowest value for good stable operation is R = 10 kΩ if pin 8 is open. If pins 1 and 8 are bypassed then R as low as 2 kΩ can be used. This restriction is because the amplifier is only compensated for closed-loop gains greater than 9.

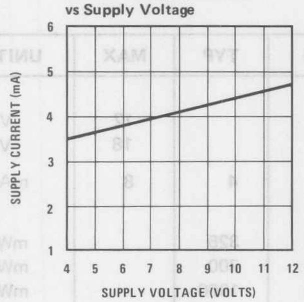
INPUT BIASING

The schematic shows that both inputs are biased to ground with a 50 kΩ resistor. The base current of the input transistors is about 250 nA, so the inputs are at about 12.5 mV when left open. If the dc source resistance driving the LM386 is higher than 250 kΩ it will contribute very little additional offset (about 2.5 mV at the input, 50 mV at the output). If the dc source resistance is less than 10 kΩ, then shorting the unused input to ground will keep the offset low (about 2.5 mV at the input, 50 mV at the output). For dc source resistances between these values we can eliminate excess offset by putting a resistor from the unused input to ground, equal in value to the dc source resistance. Of course all offset problems are eliminated if the input is capacitively coupled.

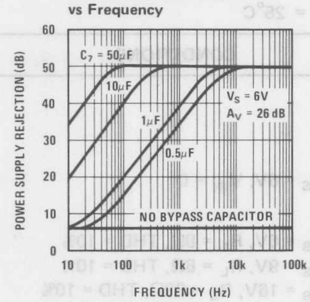
When using the LM386 with higher gains (bypassing the 1.35 kΩ resistor between pins 1 and 8) it is necessary to bypass the unused input, preventing degradation of gain and possible instabilities. This is done with a 0.1μF capacitor or a short to ground depending on the dc source resistance on the driven input.

Typical Performance Characteristics

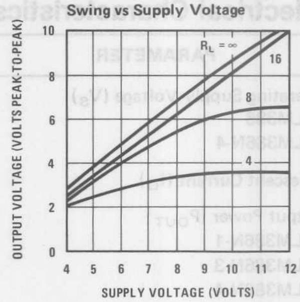
Quiescent Supply Current vs Supply Voltage



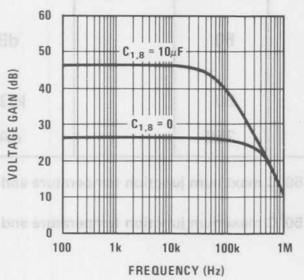
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



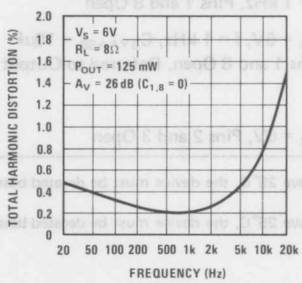
Peak-to-Peak Output Voltage Swing vs Supply Voltage



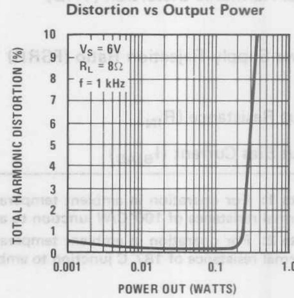
Voltage Gain vs Frequency



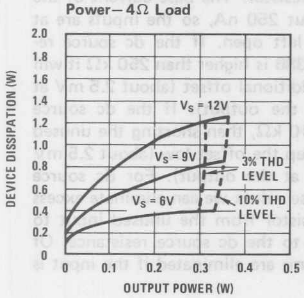
Distortion vs Frequency



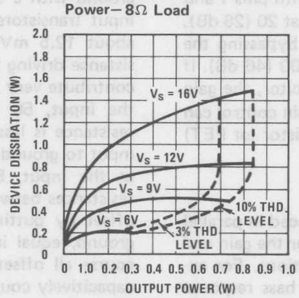
Distortion vs Output Power



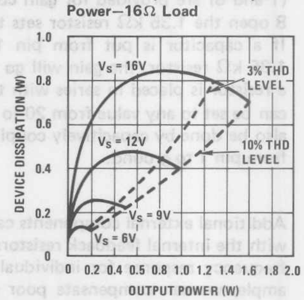
Device Dissipation vs Output Power—4Ω Load



Device Dissipation vs Output Power—8Ω Load

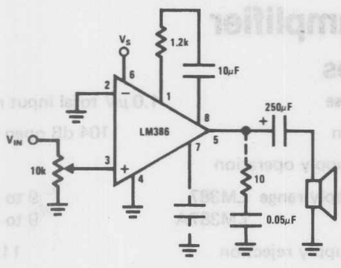


Device Dissipation vs Output Power—16Ω Load

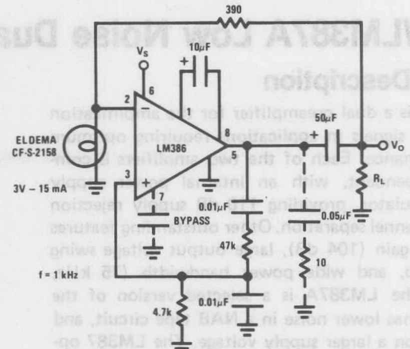


Typical Applications (Continued)

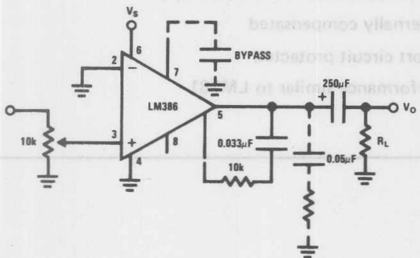
Amplifier with Gain = 50



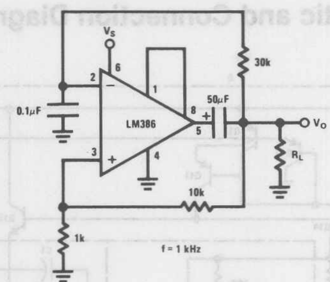
Low Distortion Power Wienbridge Oscillator



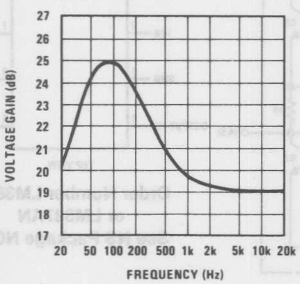
Amplifier with Bass Boost



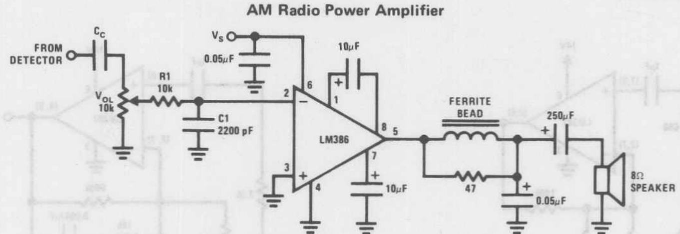
Square Wave Oscillator



Frequency Response with Bass Boost



AM Radio Power Amplifier



Note 1: Twist supply lead and supply ground very tightly.

Note 2: Twist speaker lead and ground very tightly.

Note 3: Ferrite bead is Ferroxcube K5-001-001/3B with 3 turns of wire.

Note 4: R1C1 band limits input signals.

Note 5: All components must be spaced very close to IC.

LM387/LM387A Low Noise Dual Preamplifier

General Description

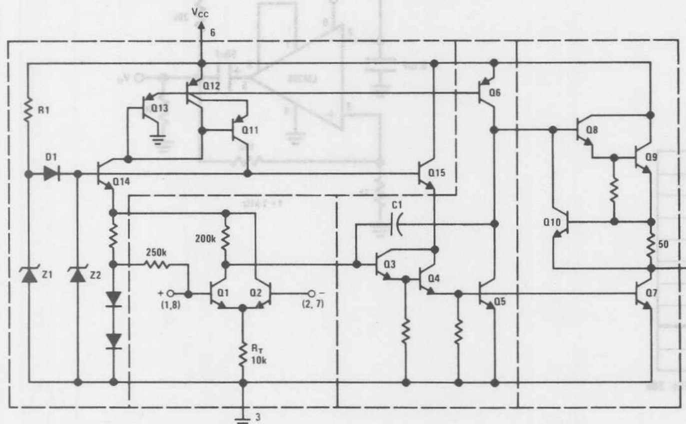
The LM387 is a dual preamplifier for the amplification of low level signals in applications requiring optimum noise performance. Each of the two amplifiers is completely independent, with an internal power supply decoupler-regulator, providing 110 dB supply rejection and 60 dB channel separation. Other outstanding features include high gain (104 dB), large output voltage swing ($V_{CC}-2V$)p-p, and wide power bandwidth (75 kHz, 20 Vp-p). The LM387A is a selected version of the LM387 that has lower noise in a NAB tape circuit, and can operate on a larger supply voltage. The LM387 operates from a single supply across the wide range of 9V to 30V, the LM387A operates on a supply of 9V to 40V.

The amplifiers are internally compensated for gains greater than 10. The LM387, LM387A is available in an 8-lead dual-in-line package. The LM387, LM387A is biased like the LM381. See AN-64 and AN-104.

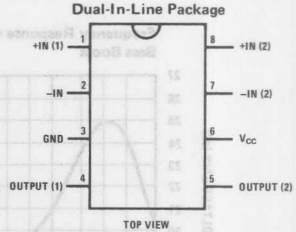
Features

- Low noise — 1.0 μV total input noise
- High gain — 104 dB open loop
- Single supply operation
- Wide supply range — LM387: 9 to 30V; LM387A: 9 to 40V
- Power supply rejection — 110 dB
- Large output voltage swing (V_{CC} − 2V)p-p
- Wide bandwidth 15 MHz unity gain
- Power bandwidth 75 kHz, 20 Vp-p
- Internally compensated
- Short circuit protected
- Performance similar to LM381

Schematic and Connection Diagrams



Dual-In-Line Package



Order Number LM387N or LM387AN
See NS Package N08B

Typical Applications

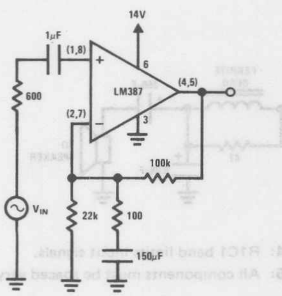


FIGURE 1. Flat Gain Circuit (A_V = 1000)

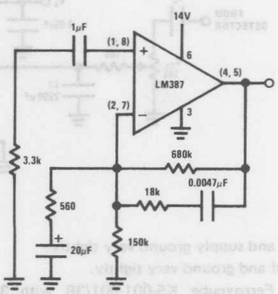


FIGURE 2. NAB Tape Circuit

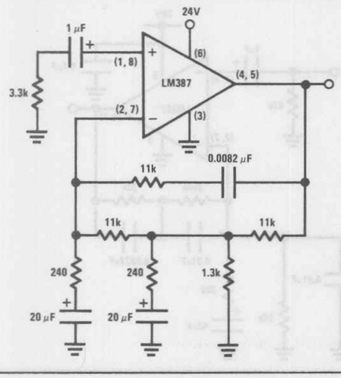
Electrical Characteristics $T_A = 25°C$, $V_{CC} = 14V$, unless otherwise stated.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Gain	Open Loop, f = 100 Hz		160,000		V/V
Supply Current	LM387, V_{CC} 9–30V, $R_L = \infty$		10		mA
	LM387A, V_{CC} 9–40V, $R_L = \infty$		10		mA
Input Resistance					
Positive Input		50	100		kΩ
Negative Input			200		kΩ
Input Current					
Negative Input			0.5	3.1	μA
Output Resistance	Open Loop		150		Ω
Output Current	Source		8		mA
	Sink		2		mA
Output Voltage Swing	Peak-to-Peak		$V_{CC}-2$		V
Unity Gain Bandwidth			15		MHz
Large Signal Frequency Response	20 Vp-p ($V_{CC} > 24V$), THD $\leq$ 1%		75		kHz
Maximum Input Voltage	Linear Operation			300	mVrms
Supply Rejection Ratio Input Referred	f = 1 kHz		110		dB
Channel Separation	f = 1 kHz	40	60		dB
Total Harmonic Distortion	60 dB Gain, f = 1 kHz		0.1	0.5	%
Total Equivalent Input Noise (Flat Gain Circuit)	10–10,000 Hz LM387 *Figure 1*		1.0	1.2	μVrms
Output Noise NAB Tape Playback Circuit Gain of 37 dB	Unweighted LM387A *Figure 2*		400	700	μVrms

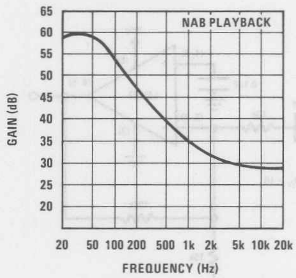
Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 187°C/W junction to ambient.

Typical Applications (Continued)

Two-Pole Fast Turn-ON NAB Tape Preamplifier

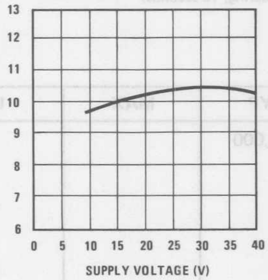


Frequency Response of NAB Circuit of Figure 2

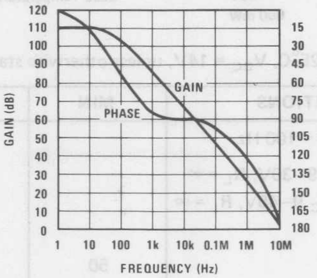


Typical Performance Characteristics

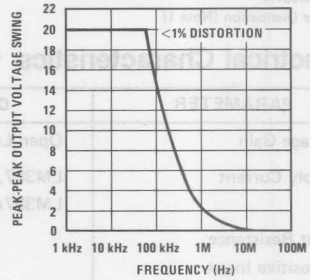
V_{CC} vs I_{CC}



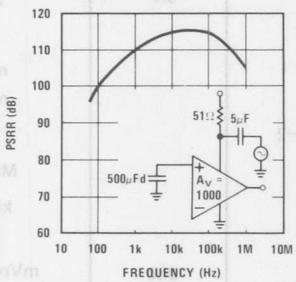
Gain and Phase Response



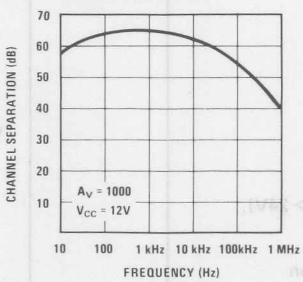
Large Signal Frequency Response



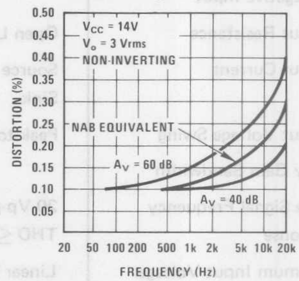
PSRR vs Frequency (Input Referred)



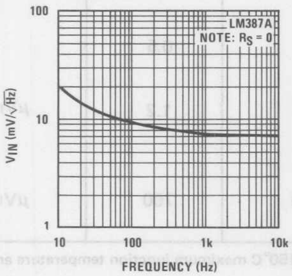
Channel Separation



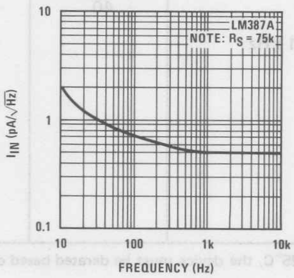
Distortion vs Frequency Non-Inverting Amplifier



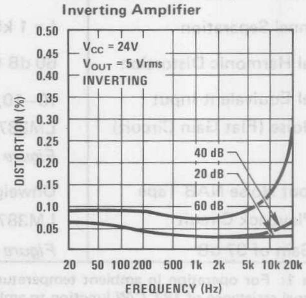
Noise Voltage vs Frequency



Noise Current vs Frequency

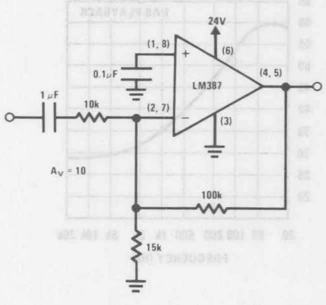


Distortion vs Frequency Inverting Amplifier

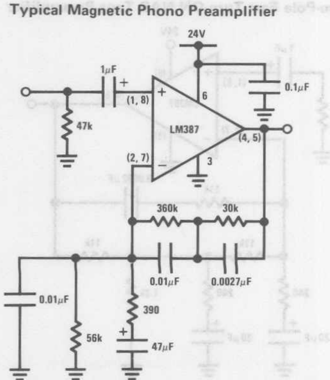


Typical Applications (Continued)

Inverting Amplifier Ultra-Low Distortion



Typical Magnetic Phono Preamplifier



National Semiconductor

Audio/Radio Circuits

LM388 1.5 Watt Audio Power Amplifier

General Description

The LM388 is an audio amplifier designed for use in medium power consumer applications. The gain is internally set to 20 to keep external part count low, but the addition of an external resistor and capacitor between pins 2 and 6 will increase the gain to any value up to 200.

The inputs are ground referenced while the output is automatically biased to one half the supply voltage.

- Variable voltage gain
- Low distortion
- Fourteen pin dual-in-line package
- Low voltage operation, 4V

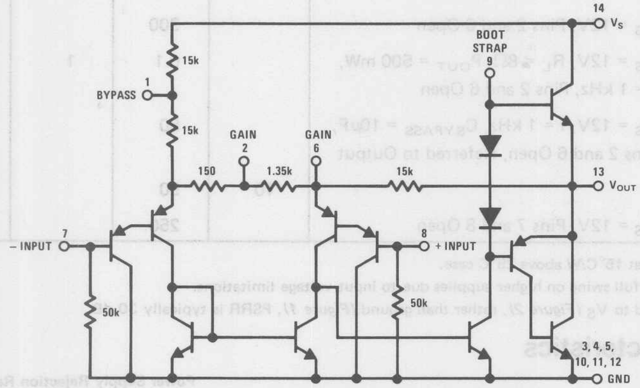
Features

- Minimum external parts
- Wide supply voltage range
- Excellent supply rejection
- Ground referenced input
- Self-centering output quiescent voltage

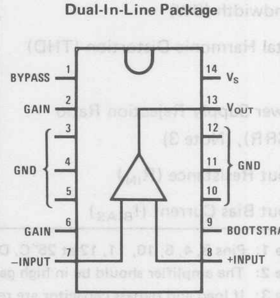
Applications

- AM-FM radio amplifiers
- Portable tape player amplifiers
- Intercoms
- TV sound systems
- Lamp drivers
- Line drivers
- Ultrasonic drivers
- Small servo drivers
- Power converters

Equivalent Schematic and Connection Diagram



Dual-In-Line Package



TOP VIEW

Order Number LM388N-1, LM388N-2 or LM388N-3
See NS Package N14A

Typical Applications

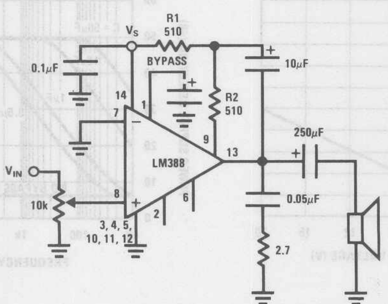


FIGURE 1. Load Returned to Ground (Amplifier with Gain = 20)

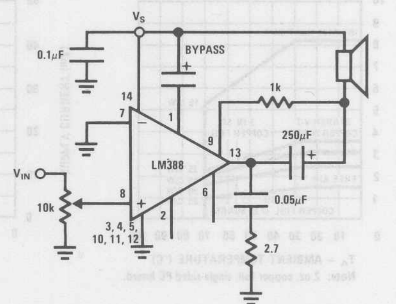


FIGURE 2. Load Returned to V_S (Amplifier with Gain = 20)

Absolute Maximum Ratings

Supply Voltage	15V
Supply Voltage (LM388N-3 Only)	22V
Package Dissipation 14-Pin DIP (Note 1)	8.3W
Input Voltage	±0.4V
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics $T_A = 25°C$, *(Figure 1)*

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage (V_S)					
LM388		4		12	V
LM388N-3		5		18	V
Quiescent Current (I_Q)	$V_{IN} = 0$				
LM388	$V_S = 12V$		16	23	mA
LM388N-3	$V_S = 16V$		20	35	mA
Output Power (P_{OUT}), (Note 2)	R1 = R2 = 180Ω, THD = 10%				
LM388N-1	$V_S = 12V$, $R_L = 8\Omega$	1.5	2.2		W
	$V_S = 6V$, $R_L = 4\Omega$ } R1 = R2 = 180Ω	0.6	0.8		W
LM388N-2	$V_S = 6V$, $R_L = 4\Omega$ } R1 = R2 = 180Ω	0.8	0.9		W
LM388N-3	$V_S = 16V$, $R_L = 8\Omega$	2.5	3.8		W
Voltage Gain (A_V)	$V_S = 12V$, f = 1 kHz	23	26	30	dB
	10μF From Pin 2 to 6		46		dB
Bandwidth (BW)	$V_S = 12V$, Pins 2 and 6 Open		300		kHz
Total Harmonic Distortion (THD)	$V_S = 12V$, $R_L = 8\Omega$, $P_{OUT} = 500$ mW, f = 1 kHz, Pins 2 and 6 Open		0.1	1	%
Power Supply Rejection Ratio (PSRR), (Note 3)	$V_S = 12V$, f = 1 kHz, $C_{BYPASS} = 10\mu F$, Pins 2 and 6 Open, Referred to Output		50		dB
Input Resistance (R_{IN})		10	50		kΩ
Input Bias Current (I_{BIAS})	$V_S = 12V$, Pins 7 and 8 Open		250		nA

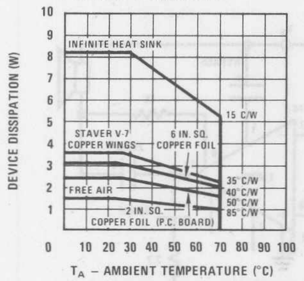
Note 1: Pins 3, 4, 5, 10, 11, 12 at 25°C. Derate at 15°C/W above 25°C case.

Note 2: The amplifier should be in high gain for full swing on higher supplies due to input voltage limitations.

Note 3: If load and bypass capacitor are returned to V_S *(Figure 2)*, rather than ground *(Figure 1)*, PSRR is typically 30 dB.

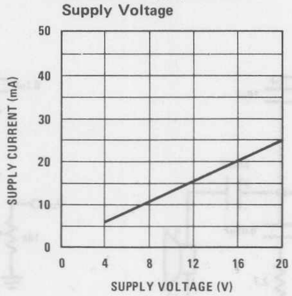
Typical Performance Characteristics

Maximum Device Dissipation vs Ambient Temperature

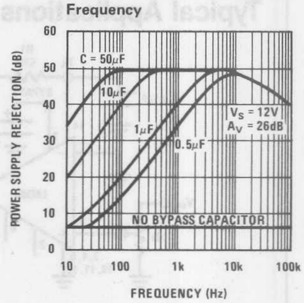


Note: 2 oz. copper foil, single-sided PC board.

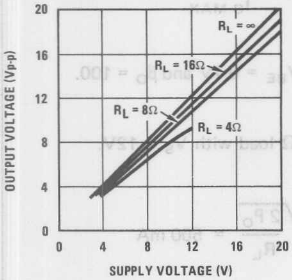
Quiescent Supply Current vs Supply Voltage



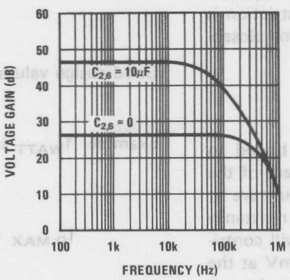
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



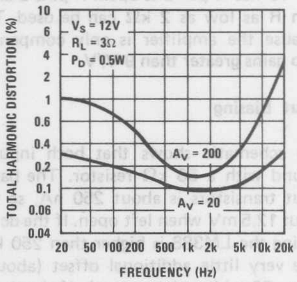
Peak-to-Peak Output Voltage Swing vs Supply Voltage



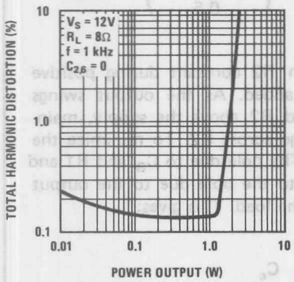
Voltage Gain vs Frequency



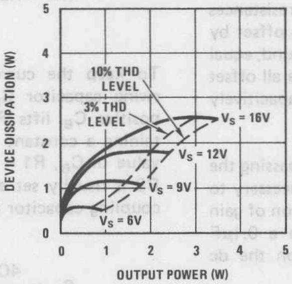
Distortion vs Frequency



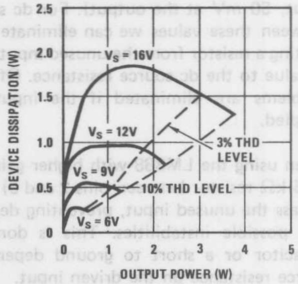
Distortion vs Output Power



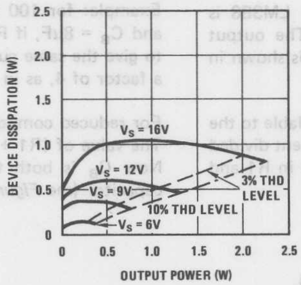
Device Dissipation vs Output Power—4Ω Load



Device Dissipation vs Output Power—8Ω Load



Device Dissipation vs Output Power—16Ω Load



Application Hints

Gain Control

To make the LM388 a more versatile amplifier, two pins (2 and 6) are provided for gain control. With pins 2 and 6 open, the 1.35 kΩ resistor sets the gain at 20 (26 dB). If a capacitor is put from pin 2 to 6, bypassing the 1.35 kΩ resistor, the gain will go up to 200 (46 dB). If a resistor is placed in series with the capacitor, the gain can be set to any value from 20 to 200. A low frequency pole in the gain response is caused by the capacitor working against the external resistor in series with the 150Ω internal resistor. If the capacitor is eliminated and a resistor connects pin 2 to 6 then the output dc level may shift due to the additional dc gain. Gain control can also be done by capacitively coupling a resistor (or FET) from pin 6 to ground, as in *Figure 7*.

Additional external components can be placed in parallel with the internal feedback resistors to tailor the gain and frequency response for individual applications. For example, we can compensate poor speaker bass response by frequency shaping the feedback path. This is done with a series RC from pin 6 to 13 (paralleling the internal 15 kΩ resistor). For 6 dB effective bass boost: R ≅

Application Hints (Continued)

15 kΩ, the lowest value for good stable operation is R = 10 kΩ if pin 2 is open. If pins 2 and 6 are bypassed then R as low as 2 kΩ can be used. This restriction is because the amplifier is only compensated for closed-loop gains greater than 9 V/V.

Input Biasing

The schematic shows that both inputs are biased to ground with a 50 kΩ resistor. The base current of the input transistors is about 250 nA, so the inputs are at about 12.5 mV when left open. If the dc source resistance driving the LM388 is higher than 250 kΩ it will contribute very little additional offset (about 2.5 mV at the input, 50 mV at the output). If the dc source resistance is less than 10 kΩ, then shorting the unused input to ground will keep the offset low (about 2.5 mV at the input, 50 mV at the output). For dc source resistances between these values we can eliminate excess offset by putting a resistor from the unused input to ground, equal in value to the dc source resistance. Of course all offset problems are eliminated if the input is capacitively coupled.

When using the LM388 with higher gains (bypassing the 1.35 kΩ resistor between pins 2 and 6) it is necessary to bypass the unused input, preventing degradation of gain and possible instabilities. This is done with a 0.1μF capacitor or a short to ground depending on the dc source resistance on the driven input.

Bootstrapping

The base of the output transistor of the LM388 is brought out to pin 9 for Bootstrapping. The output stage of the amplifier during positive swing is shown in *Figure 3* with its external circuitry.

R1 + R2 set the amount of base current available to the output transistor. The maximum output current divided by Beta is the value required for the current in R1 and R2:

$$(R1 + R2) = \beta_O \frac{(V_S/2) - V_{BE}}{I_{O\,MAX}}$$

Good design values are V_{BE} = 0.7V and β_O = 100.

Example: 1_{WATT} into 8Ω load with V_S = 12V.

$$I_{O\,MAX} = \sqrt{\frac{2\,P_O}{R_L}} = 500\text{ mA}$$

$$(R1 + R2) = 100\left(\frac{(12/2) - 0.7}{0.5}\right) = 1060\Omega$$

To keep the current in R2 constant during positive swing capacitor C_B is added. As the output swings positive C_B lifts R1 and R2 above the supply, maintaining a constant voltage across R2. To minimize the value of C_B, R1 = R2. The pole due to C_B and R1 and R2 is usually set equal to the pole due to the output coupling capacitor and the load. This gives:

$$C_B \simeq \frac{4C_c}{\beta_O} \simeq \frac{C_c}{25}$$

Example: for 100 Hz pole and R_L = 8Ω; C_c = 200μF and C_B = 8μF, if R1 is made a diode and R2 increased to give the same current, C_B can be decreased by about a factor of 4, as in *Figure 4*.

For reduced component count the load can replace R1. The value of (R1 + R2) is the same, so R2 is increased. Now C_B is both the coupling and the bootstrapping capacitor (see *Figure 2)*.

Typical Applications (Continued)

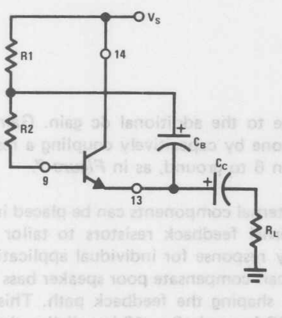


FIGURE 3.

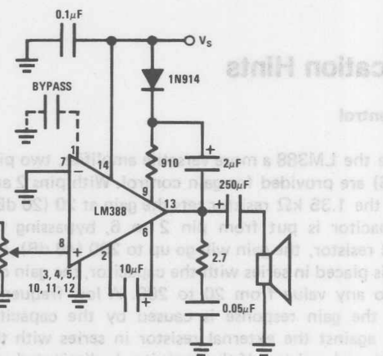


FIGURE 4. Amplifier with Gain = 200 and Minimum C_B

Typical Applications (Continued)

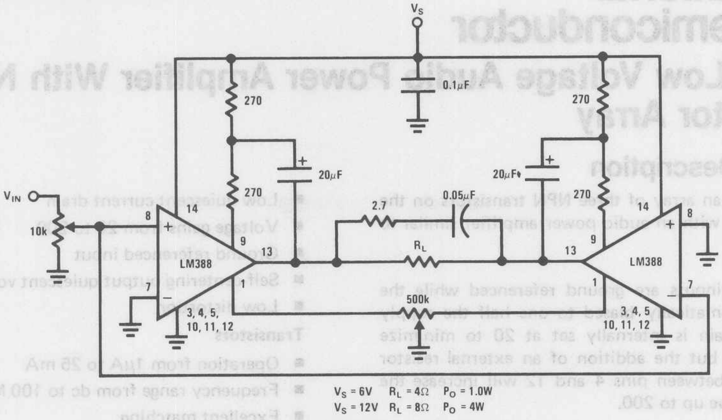


FIGURE 5. Bridge Amp

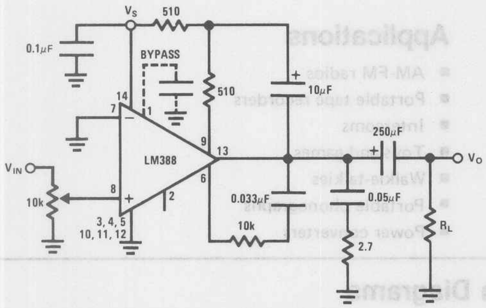


FIGURE 6a. Amplifier with Bass Boost

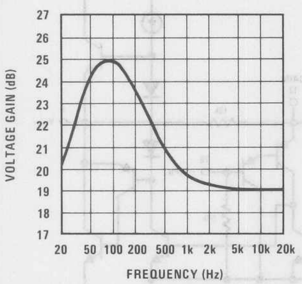


FIGURE 6b. Frequency Response with Bass Boost

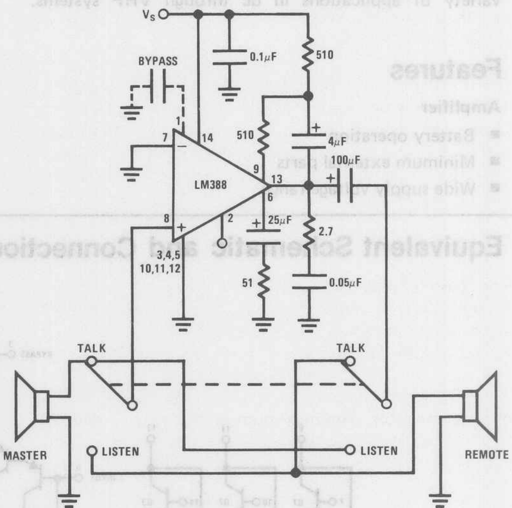


FIGURE 7. Intercom

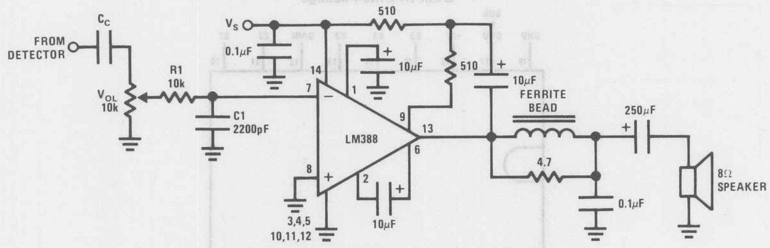


FIGURE 8. AM Radio Power Amplifier

Note 1: Twist supply lead and supply ground very tightly.

Note 2: Twist speaker lead and ground very tightly.

Note 3: Ferrite bead is Ferroxcube K5-001-001/3B with 3 turns of wire.

Note 4: R1C1 band limits input signals.

Note 5: All components must be spaced very close to IC.

LM389 Low Voltage Audio Power Amplifier With NPN Transistor Array

General Description

The LM389 is an array of three NPN transistors on the same substrate with an audio power amplifier similar to the LM386.

The amplifier inputs are ground referenced while the output is automatically biased to one half the supply voltage. The gain is internally set at 20 to minimize external parts, but the addition of an external resistor and capacitor between pins 4 and 12 will increase the gain to any value up to 200.

The three transistors have high gain and excellent matching characteristics. They are well suited to a wide variety of applications in dc through VHF systems.

Features

Amplifier

- Battery operation
- Minimum external parts
- Wide supply voltage range
- Low quiescent current drain
- Voltage gains from 20 to 200
- Ground referenced input
- Self-centering output quiescent voltage
- Low distortion

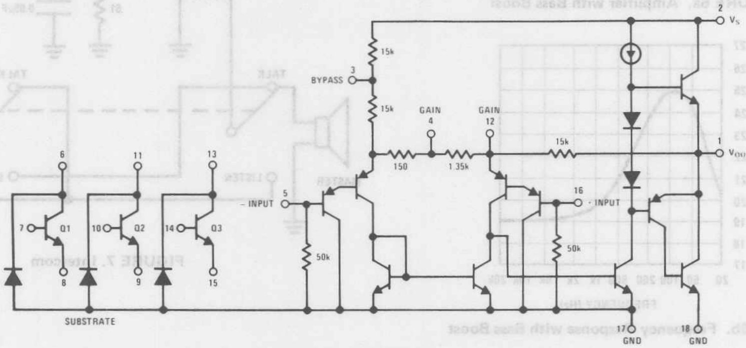
Transistors

- Operation from 1μA to 25 mA
- Frequency range from dc to 100 MHz
- Excellent matching

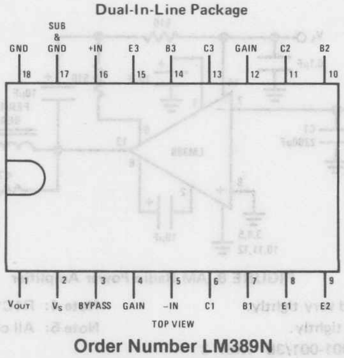
Applications

- AM-FM radios
- Portable tape recorders
- Intercoms
- Toys and games
- Walkie-talkies
- Portable phonographs
- Power converters

Equivalent Schematic and Connection Diagrams



Dual-In-Line Package



Order Number LM389N
See NS Package N18A

Input Voltage	±0.4V	Collector to Substrate Voltage, V_{CIO} (Note 2)	15V
Storage Temperature	−65°C to +150°C	Collector Current, I_C	25 mA
Operating Temperature	0°C to +70°C	Emitter Current, I_E	25 mA
Junction Temperature	150°C	Base Current, I_B	5 mA
Lead Temperature (Soldering, 10 seconds)	300°C	Power Dissipation (Each Transistor) $T_A \leq +70°C$	150 mW

Electrical Characteristics $T_A = 25°C$

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
AMPLIFIER						
V_S	Operating Supply Voltage		4		12	V
I_Q	Quiescent Current	$V_S = 6V$, $V_{IN} = 0V$		6	12	mA
P_{OUT}	Output Power (Note 3)	THD = 10% $V_S = 6V$, $R_L = 8\Omega$	250	325		mW
		THD = 10% $V_S = 9V$, $R_L = 16\Omega$		500		mW
A_V	Voltage Gain	$V_S = 6V$, f = 1 kHz	23	26	30	dB
		10μF From Pins 4 to 12		46		dB
BW	Bandwidth	$V_S = 6V$, Pins 4 and 12 Open		250		kHz
THD	Total Harmonic Distortion	$V_S = 6V$, $R_L = 8\Omega$, $P_{OUT} = 125$ mW, f = 1 kHz, Pins 4 and 12 Open		0.2	3.0	%
PSRR	Power Supply Rejection Ratio	$V_S = 6V$, f = 1 kHz, $C_{BYPASS} = 10\mu F$, Pins 4 and 12 Open, Referred to Output	30	50		dB
R_{IN}	Input Resistance		10	50		kΩ
I_{BIAS}	Input Bias Current	$V_S = 6V$, Pins 5 and 16 Open		250		nA
TRANSISTORS						
V_{CEO}	Collector to Emitter Breakdown Voltage	$I_C = 1$ mA, $I_B = 0$	12	20		V
V_{CBO}	Collector to Base Breakdown Voltage	$I_C = 10\mu A$, $I_E = 0$	15	40		V
V_{CIO}	Collector to Substrate Breakdown Voltage	$I_C = 10\mu A$, $I_E = I_B = 0$	15	40		V
V_{EBO}	Emitter to Base Breakdown Voltage	$I_E = 10\mu A$, $I_C = 0$	6.4	7.1	7.8	V
H_{FE}	Static Forward Current Transfer Ratio (Static Beta)	$I_C = 10\mu A$		100		
		$I_C = 1$ mA	100	275		
		$I_C = 10$ mA		275		
h_{oe}	Open-Circuit Output Admittance	$I_C = 1$ mA, $V_{CE} = 5V$, f = 1.0 kHz		20		μmho
V_{BE}	Base to Emitter Voltage	$I_E = 1$ mA		0.7	0.85	V
$\lvert V_{BE1} - V_{BE2} \rvert$	Base to Emitter Voltage Offset	$I_E = 1$ mA		1	5	mV
V_{CESAT}	Collector to Emitter Saturation Voltage	$I_C = 10$ mA, $I_B = 1$ mA		0.15	0.5	V
C_{EB}	Emitter to Base Capacitance	$V_{EB} = 3V$		1.5		pF
C_{CB}	Collector to Base Capacitance	$V_{CB} = 3V$		2		pF
C_{CI}	Collector to Substrate Capacitance	$V_{CI} = 3V$		3.5		pF
h_{fe}	High Frequency Current Gain	$I_C = 10$ mA, $V_{CE} = 5V$, f = 100 MHz	1.5	5.5		

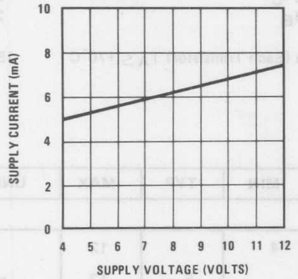
Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 175°C/W junction to ambient.

Note 2: The collector of each transistor is isolated from the substrate by an integral diode. Therefore, the collector voltage should remain positive with respect to pin 17 at all times.

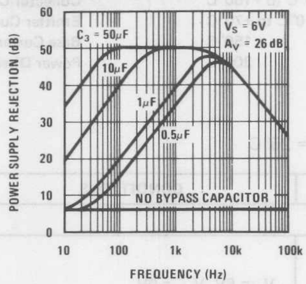
Note 3: If oscillation exists under some load conditions, add 2.7Ω and 0.05μF series network from pin 1 to ground.

Typical Amplifier Performance Characteristics

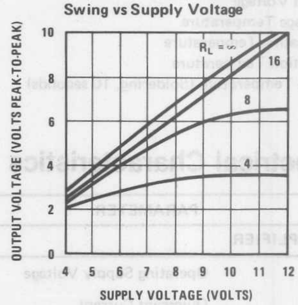
Quiescent Supply Current vs Supply Voltage



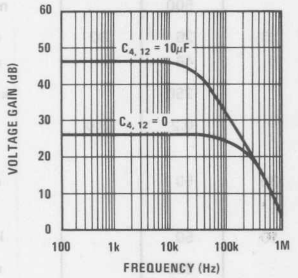
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



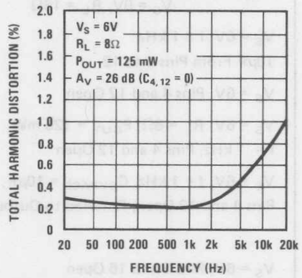
Peak-to-Peak Output Voltage Swing vs Supply Voltage



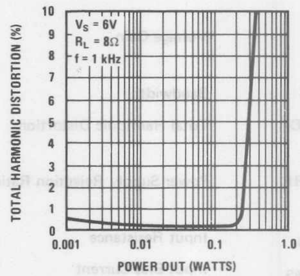
Voltage Gain vs Frequency



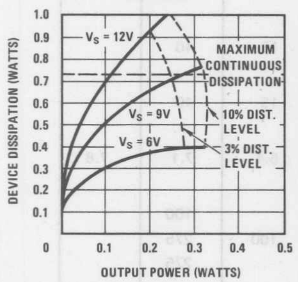
Distortion vs Frequency



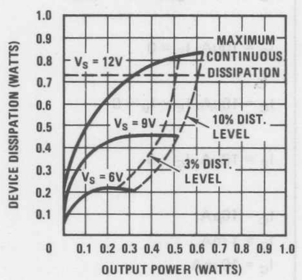
Distortion vs Output Power



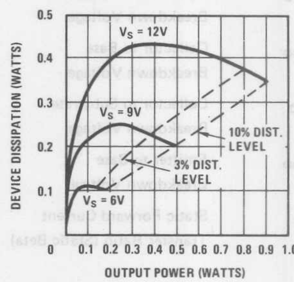
Device Dissipation vs Output Power — 4Ω Load



Device Dissipation vs Output Power — 8Ω Load

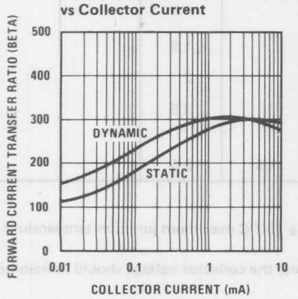


Device Dissipation vs Output Power — 16Ω Load

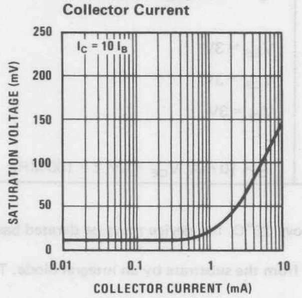


Typical Transistor Performance Characteristics

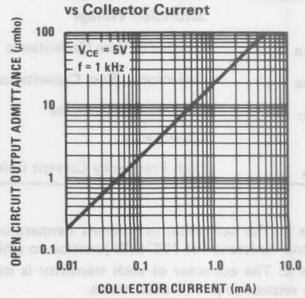
Forward Current Transfer Ratio vs Collector Current



Saturation Voltage vs Collector Current

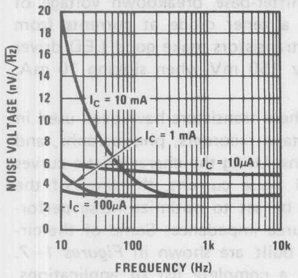


Open Circuit Output Admittance vs Collector Current

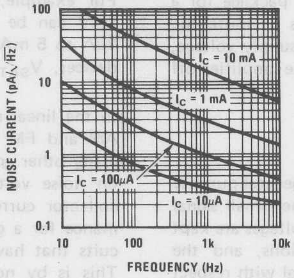


Typical Transistor Performance Characteristics (Continued)

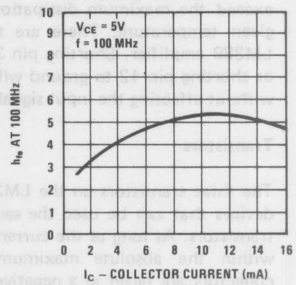
Noise Voltage vs Frequency



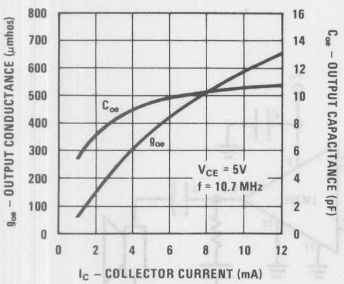
Noise Current vs Frequency



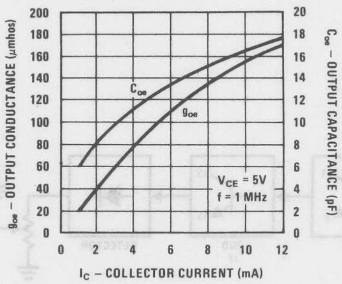
High Frequency Current Gain vs Collector Current



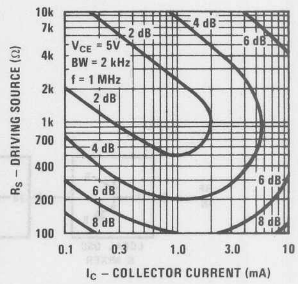
g_{oe} and C_{oe} vs Collector Current



g_{oe} and C_{oe} vs Collector Current



Contours of Constant Noise Figure



Application Hints

Gain Control

To make the LM389 a more versatile amplifier, two pins (4 and 12) are provided for gain control. With pins 4 and 12 open, the 1.35 kΩ resistor sets the gain at 20 (26 dB). If a capacitor is put from pin 4 to 12, bypassing the 1.35 kΩ resistor, the gain will go up to 200 (46 dB). If a resistor is placed in series with the capacitor, the gain can be set to any value from 20 to 200. A low frequency pole in the gain response is caused by the capacitor working against the external resistor in series with the 150Ω internal resistor. If the capacitor is eliminated and a resistor connects pin 4 to 12, then the output dc level may shift due to the additional dc gain. Gain control can also be done by capacitively coupling a resistor (or FET) from pin 12 to ground.

Additional external components can be placed in parallel with the internal feedback resistors to tailor the gain and frequency response for individual applications. For example, we can compensate poor speaker bass response by frequency shaping the feedback path. This is done with a series RC from pin 1 to 12 (paralleling the internal 15 kΩ resistor). For 6 dB effective bass boost: R ≅ 15 kΩ, the lowest value for good stable operation is R = 10 kΩ if pin 4 is open. If pins 4 and 12 are bypassed then R as low as 2 kΩ can be used. This restriction is because the amplifier is only compensated for closed-loop gains greater than 9V/V.

Input Biasing

The schematic shows that both inputs are biased to ground with a 50 kΩ resistor. The base current of the input transistors is about 250 nA, so the inputs are at about 12.5 mV when left open. If the dc source resistance driving the LM389 is higher than 250 kΩ it will contribute very little additional offset (about 2.5 mV at the input, 50 mV at the output). If the dc source resistance is less than 10 kΩ, then shorting the unused input to ground will keep the offset low (about 2.5 mV at the input, 50 mV at the output). For dc source resistances between these values we can eliminate excess offset by putting a resistor from the unused input to ground, equal in value to the dc source resistance. Of course all offset problems are eliminated if the input is capacitively coupled.

When using the LM389 with higher gains (bypassing the 1.35 kΩ resistor between pins 4 and 12) it is necessary to bypass the unused input, preventing degradation of gain and possible instabilities. This is done with a 0.1μF capacitor or a short to ground depending on the dc source resistance of the driven input.

Supplies and Grounds

The LM389 has excellent supply rejection and does not require a well regulated supply. However, to eliminate possible high frequency stability problems, the supply should be decoupled to ground with a 0.1μF capacitor. The high current ground of the output transistor, pin 18, is brought out separately from small signal ground, pin 17. If the two ground leads are returned separately to supply then the parasitic resistance in the power ground lead will not cause stability problems. The parasitic resistance in the signal ground can cause stability problems and it should be minimized. Care should also be taken to insure that the power dissipation does not

exceed the maximum dissipation of the package for a given temperature. There are two ways to mute the LM389 amplifier. Shorting pin 3 to the supply voltage, or shorting pin 12 to ground will turn the amplifier off without affecting the input signal.

Transistors

The three transistors on the LM389 are general purpose devices that can be used the same as other small signal transistors. As long as the currents and voltages are kept within the absolute maximum limitations, and the collectors are never at a negative potential with respect to pin 17, there is no limit on the way they can be used. For example, the emitter-base breakdown voltage of 7.1V can be used as a zener diode at currents from 1μA to 5 mA. These transistors make good LED driver devices, V_{SAT} is only 150 mV when sinking 10 mA.

In the linear region, these transistors have been used in AM and FM radios, tape recorders, phonographs, and many other applications. Using the characteristic curves on noise voltage and noise current, the level of the collector current can be set to optimize noise performance for a given source impedance. Some of the circuits that have been built are shown in *Figures 1–7*. This is by no means a complete list of applications, since that is limited only by the designers imagination.

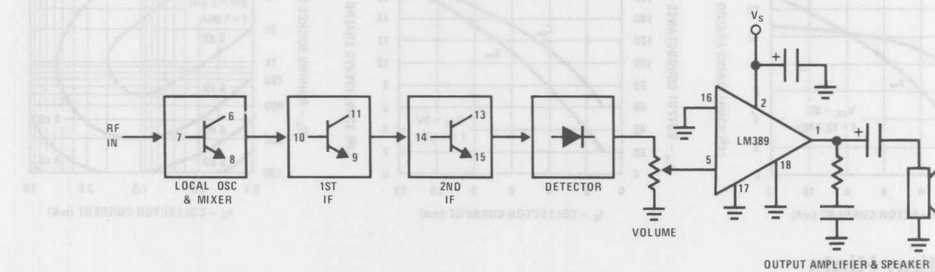


FIGURE 1. AM Radio

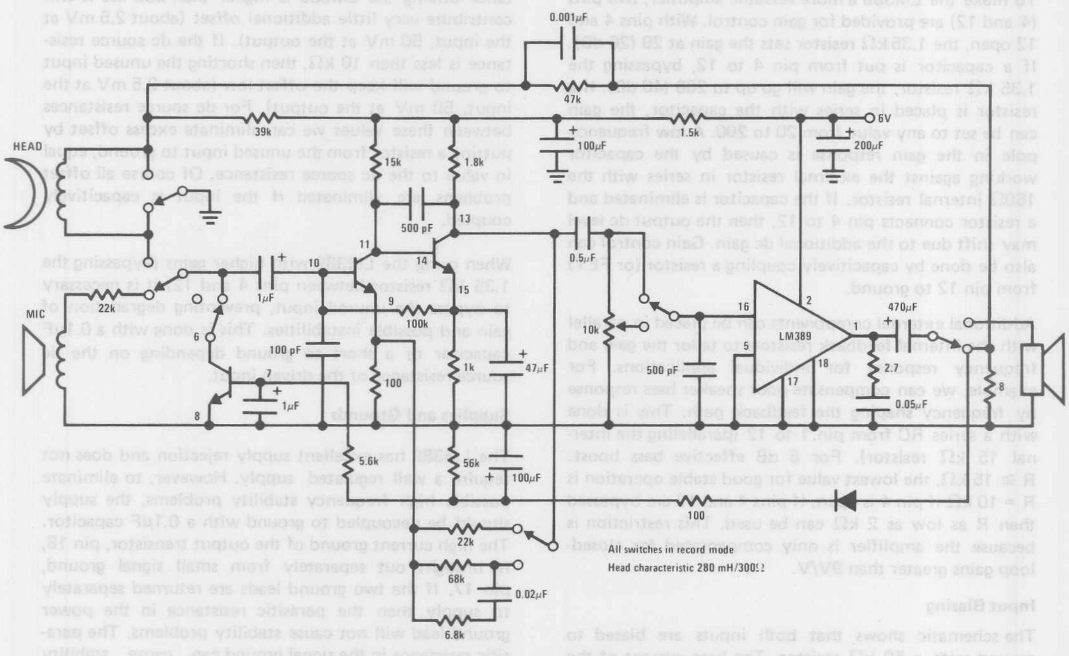


FIGURE 2. Tape Recorder

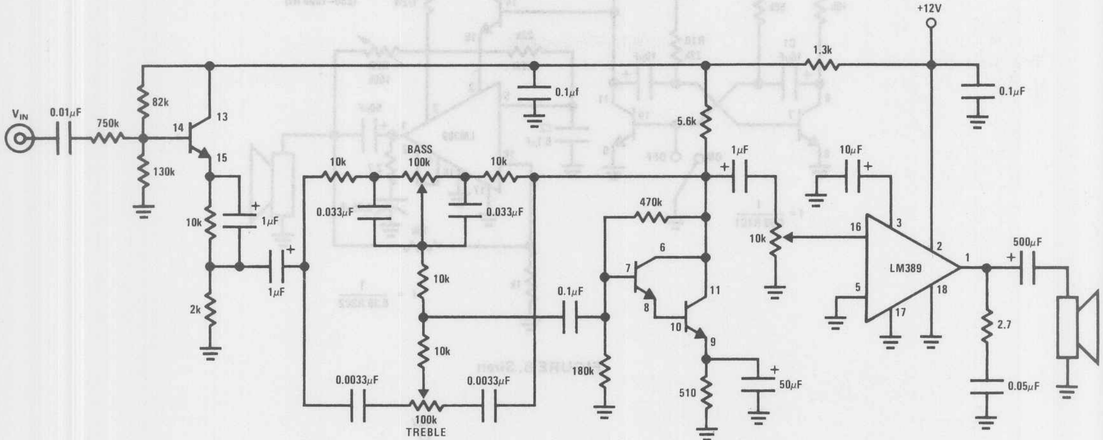


FIGURE 3. Ceramic Phono Amplifier with Tone Controls

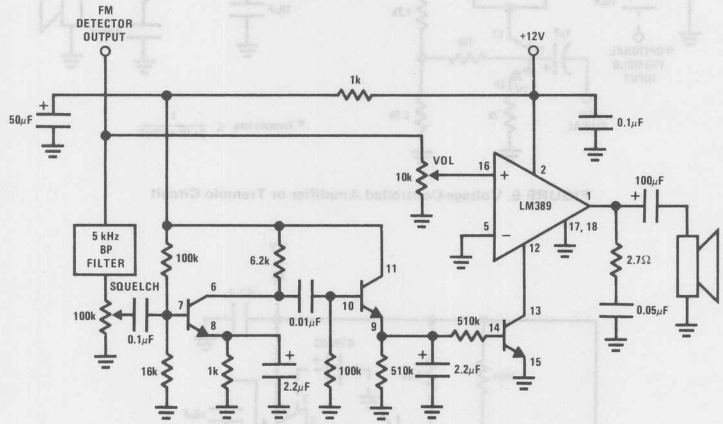


FIGURE 4. FM Scanner Noise Squelch Circuit

10

Application Hints (Continued)

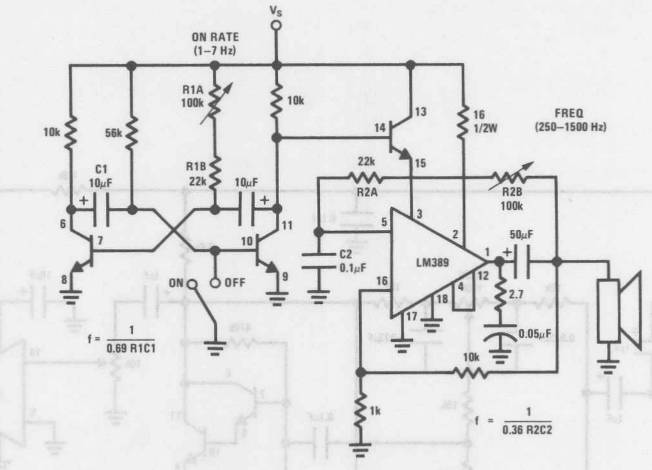


FIGURE 5. Siren

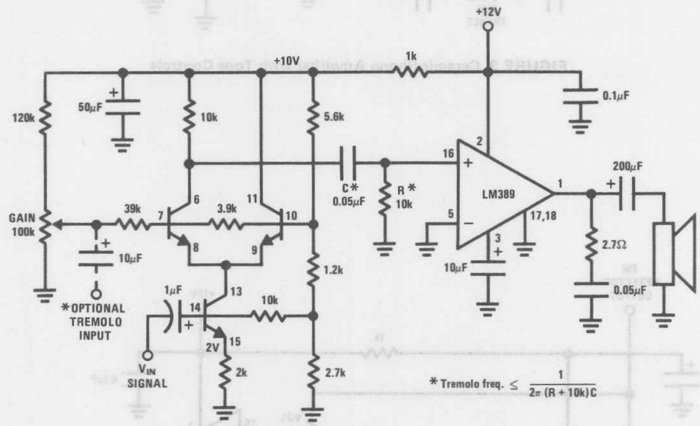


FIGURE 6. Voltage-Controlled Amplifier or Tremolo Circuit

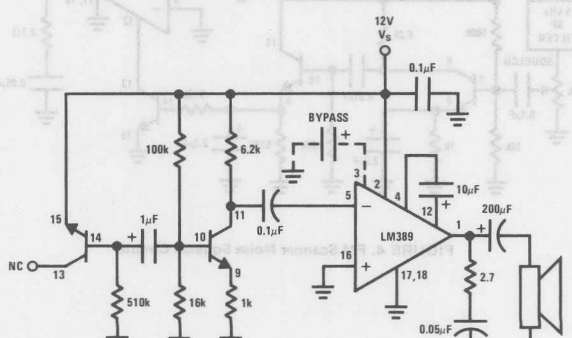


FIGURE 7. Noise Generator Using Zener Diode

National Semiconductor

LM390 1 Watt Battery Operated Audio Power Amplifier

General Description

The LM390 Power Audio Amplifier is optimized for 6V, 7.5V, 9V operation into low impedance loads. The gain is internally set at 20 to keep the external part count low, but the addition of an external resistor and capacitor between pins 2 and 6 will increase the gain to any value up to 200. The inputs are ground referenced while the output is automatically biased to one half the supply voltage.

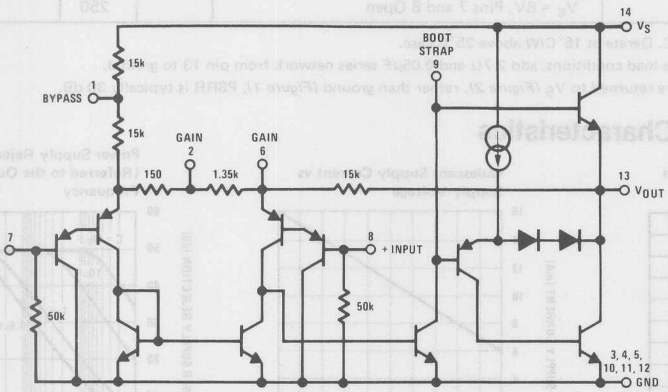
Features

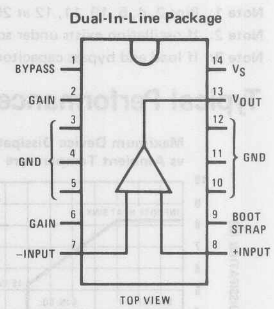
- Battery operation
- 1W output power
- Minimum external parts
- Excellent supply rejection
- Ground referenced input
- Self-centering output quiescent voltage
- Variable voltage gain
- Low distortion
- Fourteen pin dual-in-line package

Applications

- AM-FM radio amplifiers
- Portable tape player amplifiers
- Intercoms
- TV sound systems
- Lamp drivers
- Line drivers
- Ultrasonic drivers
- Small servo drivers
- Power converters

Equivalent Schematic and Connection Diagrams





Order Number LM390N
See NS Package N14A

Typical Applications

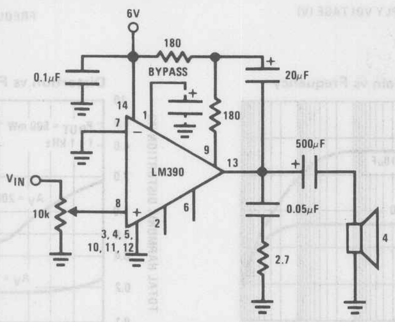


FIGURE 1. Load Returned to Ground (Amplifier with Gain = 20)

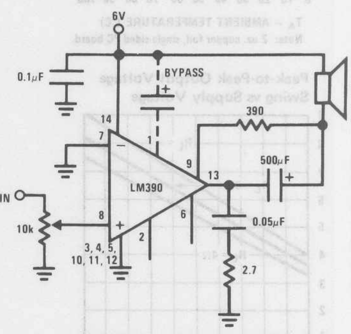


FIGURE 2. Load Returned to Supply (Amplifier with Gain = 20)

Input Voltage	±0.4V
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics $T_A = 25°C$, *(Figure 1)*

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_S	Operating Supply Voltage		4		9	V
I_Q	Quiescent Current	$V_S = 6V$, $V_{IN} = 0$		10	20	mA
P_{OUT}	Output Power	$V_S = 6V$, $R_L = 4\Omega$, THD = 10%, (Note 2)	0.8	1.0		W
A_V	Voltage Gain	$V_S = 6V$, f = 1 kHz	23	26	30	dB
		10μF from Pin 2 to 6		46		dB
BW	Bandwidth	$V_S = 6V$, Pins 2 and 6 Open		300		kHz
THD	Total Harmonic Distortion	$V_S = 6V$, $R_L = 4\Omega$, $P_{OUT} = 500$ mW f = 1 kHz, Pins 2 and 6 Open		0.2	1	%
PSRR	Power Supply Rejection Ratio	$V_S = 6V$, f = 1 kHz, $C_{BYPASS} = 10\mu F$, Pins 2 and 6 Open, Referred to Output (Note 3)		50		dB
R_{IN}	Input Resistance		10	50		kΩ
I_{BIAS}	Input Bias Current	$V_S = 6V$, Pins 7 and 8 Open		250		nA

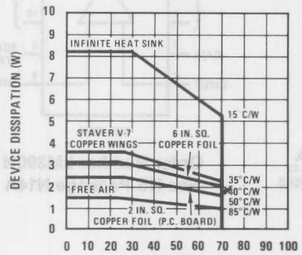
Note 1: Pins 3, 4, 5, 10, 11, 12 at 25°C. Derate at 15°C/W above 25°C case.

Note 2: If oscillation exists under some load conditions, add 2.7Ω and 0.05μF series network from pin 13 to ground.

Note 3: If load and bypass capacitor are returned to V_S *(Figure 2)*, rather than ground *(Figure 1)*, PSRR is typically 30 dB.

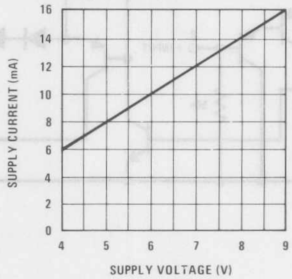
Typical Performance Characteristics

Maximum Device Dissipation vs Ambient Temperature

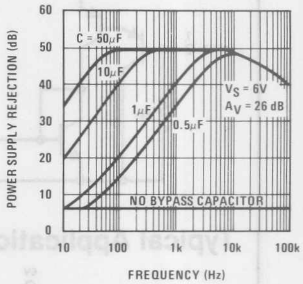


Note: 2 oz. copper foil, single-sided PC board.

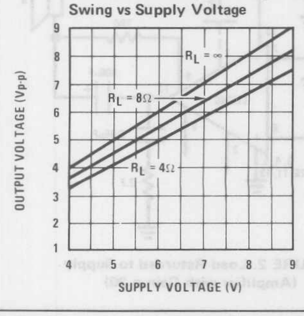
Quiescent Supply Current vs Supply Voltage



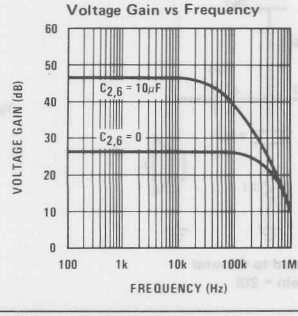
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



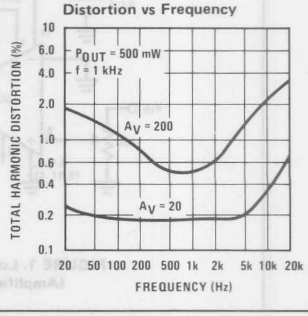
Peak-to-Peak Output Voltage Swing vs Supply Voltage



Voltage Gain vs Frequency

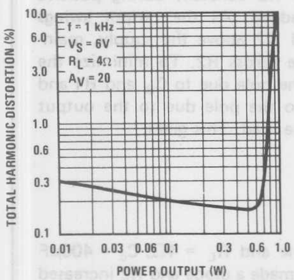


Distortion vs Frequency

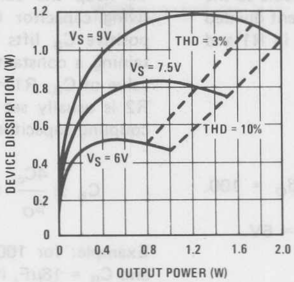


Typical Performance Characteristics (Continued)

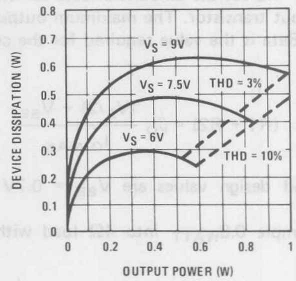
Distortion vs Output Power



Device Dissipation vs Output Power 4Ω Load



Device Dissipation vs Output Power 8Ω Load



Application Hints

Gain Control

To make the LM390 a more versatile amplifier, two pins (2 and 6) are provided for gain control. With pins 2 and 6 open, the 1.35 kΩ resistor sets the gain at 20 (26 dB). If a capacitor is put from pin 2 to 6, bypassing the 1.35 kΩ resistor, the gain will go up to 200 (46 dB). If a resistor is placed in series with the capacitor, the gain can be set to any value from 20 to 200. A low frequency pole in the gain response is caused by the capacitor working against the external resistor in series with the 150Ω internal resistor. If the capacitor is eliminated and a resistor connects pin 2 to 6 then the output dc level may shift due to the additional dc gain. Gain control can also be done by capacitively coupling a resistor (or FET) from pin 6 to ground, as in *Figure 7*.

Additional external components can be placed in parallel with the internal feedback resistors to tailor the gain and frequency response for individual applications. For example, we can compensate poor speaker bass response by frequency shaping the feedback path. This is done with a series RC from pin 6 to 13 (paralleling the internal 15 kΩ resistor). For 6 dB effective bass boost: R ≅ 15 kΩ, the lowest value for good stable operation is R = 10 kΩ if pin 2 is open. If pins 2 and 6 are bypassed then R as low as 2 kΩ can be used. This restriction is because the amplifier is only compensated for closed-loop gains greater than 9 V/V.

Input Biasing

The schematic shows that both inputs are biased to ground with a 50 kΩ resistor. The base current of the input transistors is about 250 nA, so the inputs are at about 12.5 mV when left open. If the dc source resistance driving the LM390 is higher than 250 kΩ it will contribute very little additional offset (about 2.5 mV at the input, 50 mV at the output). If the dc source resistance is less than 10 kΩ, then shorting the unused input to ground will keep the offset low (about 2.5 mV at the input, 50 mV at the output). For dc source resistances between these values we can eliminate excess offset by putting a resistor from the unused input to ground, equal in value to the dc source resistance. Of course all offset problems are eliminated if the input is capacitively coupled.

When using the LM390 with higher gains (bypassing the 1.35 kΩ resistor between pins 2 and 6) it is necessary to bypass the unused input, preventing degradation of gain and possible instabilities. This is done with a 0.1μF capacitor or a short to ground depending on the dc source resistance on the driven input.

Bootstrapping

The base of the output transistor of the LM390 is brought out to pin 9 for Bootstrapping. The output stage of the amplifier during positive swing is shown in *Figure 3* with its external circuitry.

Typical Applications (Continued)

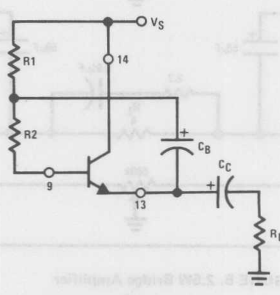


FIGURE 3.

Application Hints (Continued)

R1 + R2 set the amount of base current available to the output transistor. The maximum output current divided by Beta is the value required for the current in R1 and R2:

$$(R1 + R2) = \beta_O \frac{(V_S/2) - V_{BE}}{I_{O\ MAX}}$$

Good design values are V_{BE} = 0.7V and β_O = 100.

Example 0.8_{WATT} into 4Ω load with V_S = 6V.

$$I_{O\ MAX} = \sqrt{\frac{2\ P_O}{R_L}} = 632\ \text{mA}$$

$$(R1 + R2) = 100 \left(\frac{(6/2) - 0.7}{0.632}\right) = 364\Omega$$

To keep the current in R2 constant during positive swing capacitor C_B is added. As the output swings positive C_B lifts R1 and R2 above the supply, maintaining a constant voltage across R2. To minimize the value of C_B, R1 = R2. The pole due to C_B and R1 and R2 is usually set equal to the pole due to the output coupling capacitor and the load. This gives:

$$C_B \simeq \frac{4C_c}{\beta_O} \simeq \frac{C_c}{25}$$

Example: for 100 Hz pole and R_L = 4Ω; C_c = 400μF and C_B = 16μF, if R1 is made a diode and R2 increased to give the same current, C_B can be decreased by about a factor of 4, as in *Figure 4*.

For reduced component count the load can replace R1. The value of (R1 + R2) is the same, so R2 is increased. Now C_B is both the coupling and the bootstrapping capacitor (see *Figure 2*).

Typical Applications (Continued)

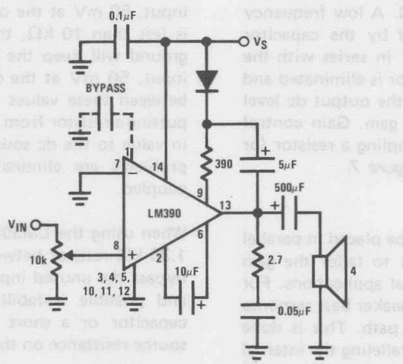


FIGURE 4. Amplifier with Gain = 200 and Minimum C_B

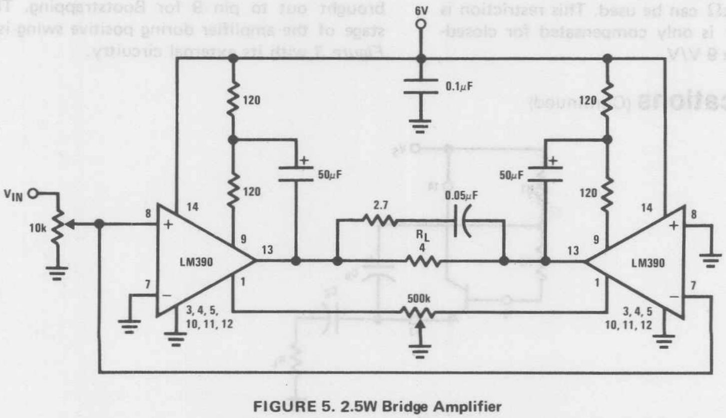


FIGURE 5. 2.5W Bridge Amplifier

Typical Applications (Continued)

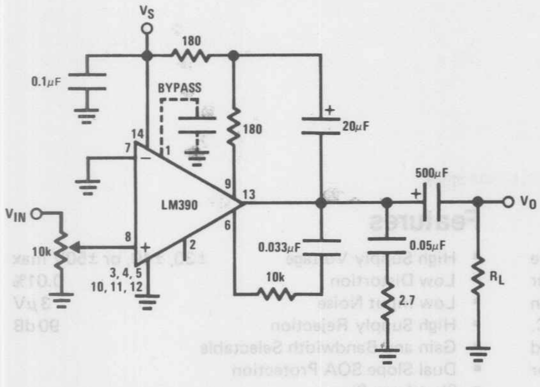


FIGURE 6(a). Amplifier with Bass Boost

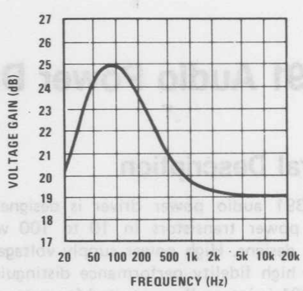


FIGURE 6(b). Frequency Response with Bass Boost

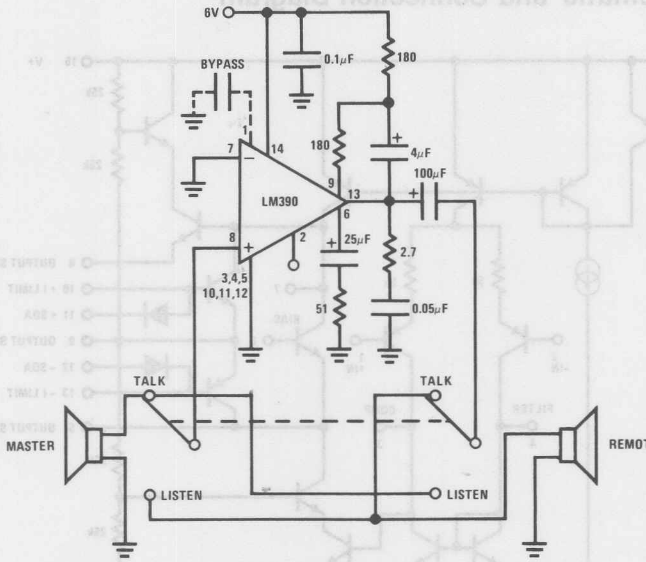


FIGURE 7. Intercom

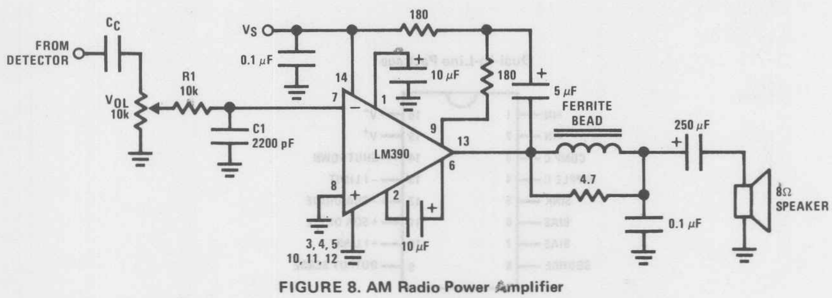


FIGURE 8. AM Radio Power Amplifier

Note 1: Twist supply lead and supply ground very tightly.

Note 2: Twist speaker lead and ground very tightly.

Note 3: Ferrite bead is Ferroxcube K5-001-001/3B with 3 turns of wire.

Note 4: R1C1 band limits input signals.

Note 5: All components must be spaced very close to IC.

LM391 Audio Power Driver

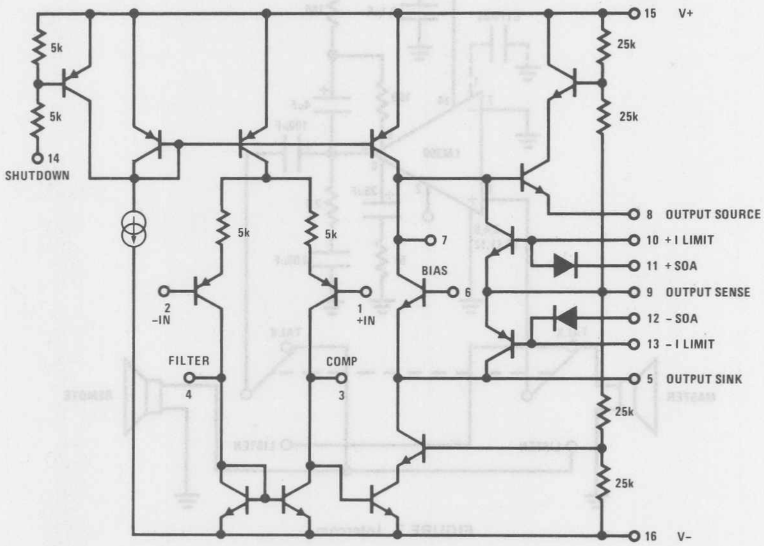
General Description

The LM391 audio power driver is designed to drive external power transistors in 10 to 100 watt power amplifier designs. High power supply voltage operation and true high fidelity performance distinguish this IC. The LM391 is internally protected for output faults and thermal overloads; circuitry providing output transistor protection is user programmable.

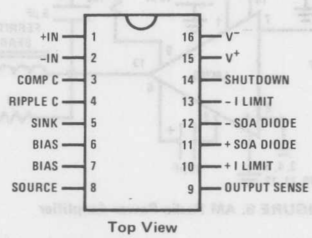
Features

- High Supply Voltage ±30, ±40, or ±50V max
- Low Distortion 0.01%
- Low Input Noise 3 μV
- High Supply Rejection 90 dB
- Gain and Bandwidth Selectable
- Dual Slope SOA Protection
- Shutdown Pin

Equivalent Schematic and Connection Diagram



Dual-In-Line Package



Top View

Order Number LM391N-60, LM391N-80, or LM391N-100
See NS Package N16A

Absolute Maximum Ratings

Supply Voltage	
LM391N – 60	±30 V or +60 V
LM391N – 80	±40 V or +80 V
LM391N – 100	±50 V or +100 V
Input Voltage	Supply Voltage less 5 V
Shutdown Current (Pin 14)	1 mA
Package Dissipation (Note 1)	1.39 W
Storage Temperature	$-65^\circ C$ to $+150^\circ C$
Operating Temperature	$0^\circ C$ to $+70^\circ C$
Lead Temperature (Soldering, 10 seconds)	$+300^\circ C$

Electrical Characteristics

$T_A = 25^\circ C$ (The following are for $V^+ = 90\%\ V^+_{MAX}$ and $V^- = 90\%\ V^-_{MAX}$.)

Parameter	Conditions	Min	Typ	Max	Units
Quiescent Current	current in pin 15				
LM391N – 60	$V_{IN} = 0$		3	10	mA
LM391N – 80			4	8	mA
LM391N – 100			5	6	mA
Output Swing	positive	$V^+ - 7$	$V^+ - 5$		V
	negative	$V^- + 7$	$V^- + 5$		V
Drive Current	source (pin 8)	5			mA
	sink (pin 5)	5			mA
Noise (20 – 20 kHz)	input referred		3		μV
Supply Rejection	input referred	70	90		dB
Total Harmonic Distortion	f = 1 kHz		0.01		%
	f = 20 kHz		0.10	0.25	%
Intermodulation Distortion	60 Hz, 7 kHz, 4:1		0.01		%
Open Loop Gain	f = 1 kHz	1000	5500		V/V
Input Bias Current			0.1	1.0	μA
Input Offset Voltage			5	20	mV
Positive Current Limit V_{BE}	pin 10 - 9		650		mV
Negative Current Limit V_{BE}	pin 9 - 13		650		mV
Positive Current Limit Bias Current	pin 10		10	100	μA
Negative Current Limit Bias Current	pin 13		10	100	μA

Pin 14 Current Comments

Minimum pin 14 current required for shutdown is 0.5 mA, and must not exceed 1 mA.

Maximum pin 14 current for amplifier not shut down is 0.05 mA.

The typical shutdown switch point current is 0.2 mA.

Note 1: For operation in ambient temperatures above $25^\circ C$, the device must be derated based on a $150^\circ C$ maximum junction temperature and a thermal resistance of $90^\circ C/W$ junction to ambient.

Typical Applications

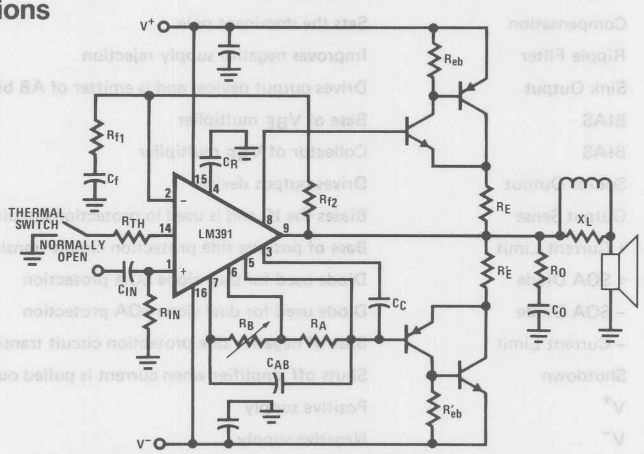
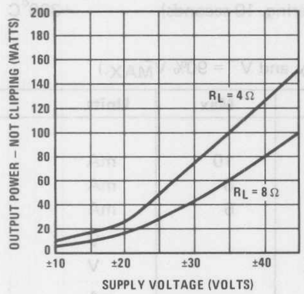


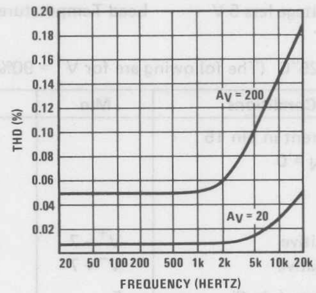
Figure 1. LM391 with External Components — Protection Circuitry Not Shown

Typical Performance Characteristics

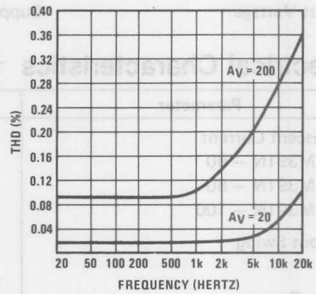
Output Power vs Supply Voltage



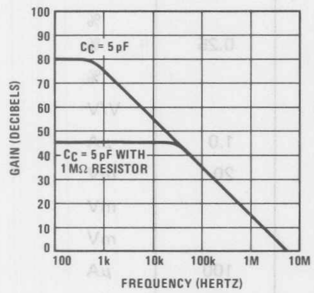
Total Harmonic Distortion vs Frequency ($R_L = 8\Omega$)



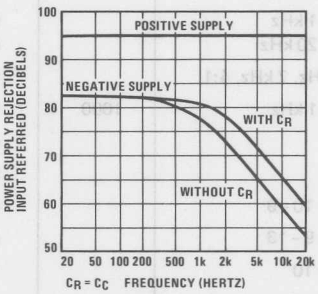
Total Harmonic Distortion vs Frequency ($R_L = 4\Omega$)



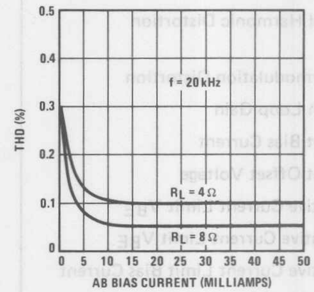
Open Loop Gain vs Frequency



Input Referred Power Supply Rejection vs Frequency



Total Harmonic Distortion vs AB Bias Current



Pin Descriptions

Pin No.	Pin Name	Comments
1	+ Input	Audio input
2	– Input	Feedback input
3	Compensation	Sets the dominant pole
4	Ripple Filter	Improves negative supply rejection
5	Sink Output	Drives output devices and is emitter of AB bias V_{BE} multiplier
6	BIAS	Base of V_{BE} multiplier
7	BIAS	Collector of V_{BE} multiplier
8	Source Output	Drives output devices
9	Output Sense	Biases the IC and is used in protection circuits
10	+ Current Limit	Base of positive side protection circuit transistor
11	+ SOA Diode	Diode used for dual slope SOA protection
12	– SOA Diode	Diode used for dual slope SOA protection
13	– Current Limit	Base of negative side protection circuit transistor
14	Shutdown	Shuts off amplifier when current is pulled out of pin
15	V^+	Positive supply
16	V^-	Negative supply

External Components (figure 1)

Component	Typical Value	Comments
C_{IN}	1 μF	Input coupling capacitor sets a low frequency pole with R_{IN}. $f_L = \frac{1}{2\pi R_{IN} C_{IN}}$
R_{IN}	100k	Sets input impedance and DC bias to input.
R_{f2}	100k	Feedback resistor; for minimum offset voltage at the output this should be equal to R_{IN}.
R_{f1}	5.1k	Feedback resistor that works with R_{f2} to set the voltage gain. $A_V = 1 + \frac{R_{f2}}{R_{f1}}$
C_f	10 μF	Feedback capacitor. This reduces the gain to unity at DC for minimum offset voltage at the output. Also sets a low frequency pole with R_{f1}. $f_L = \frac{1}{2\pi R_{f1} C_f}$
C_C	5 pF	Compensation capacitor. Sets gain bandwidth product and a high frequency pole. $GBW = \frac{1}{2\pi 5000 C_C}$, $f_h = \frac{GBW}{A_V}$ Max f_h for stable design $\approx$ 500 kHz.
R_A	3.9k	AB bias resistor.
R_B	10k	AB bias potentiometer. Adjust to set bias current in the output stage.
C_{AB}	0.1 μF	Bypass capacitor for bias. This improves high frequency distortion and transient response.
C_R	5 pF	Ripple capacitor. This improves negative supply rejection at midband and high frequencies. C_R, if used, must equal C_C.
R_{eb}	100 Ω	Bleed resistor. This removes stored charge in output transistors.
R_O	2.7 Ω	Output compensation resistor. This resistor and C_O compensate the output stage. This value will vary slightly for different output devices.
C_O	0.1 μF	Output compensation capacitor. This works with R_O to form a zero that cancels f_β of the output power transistors.
R_E	0.3 Ω	Emitter degeneration resistor. This resistor gives thermal stability to the output stage quiescent current. IRC PW5 type.
R_{TH}	39k	Shutdown resistor. Sets the amount of current pulled out of pin 14 during shutdown.
C_2, C_2'	1000 pF	Compensation capacitors for protection circuitry.
X_L	10 Ω || 5 μH	Used to isolate capacitive loads, usually 20 turns of wire wrapped around a 10 Ω, 2 W resistor.

Givens: Power Output
Load Impedance
Input Sensitivity
Input Impedance
Bandwidth

The power output and load impedance determine the power supply requirements. Output signal swing and current are found from:

$$V_{Opeak} = \sqrt{2 R_L P_O} \quad (1)$$

$$I_{Opeak} = \sqrt{\frac{2 P_O}{R_L}} \quad (2)$$

Add 5 volts to the peak output swing (V_{OP}) for transistor voltage to get the supplies, i.e., $\pm(V_{OP} + 5\,V)$ at a current of I_{peak}. The regulation of the supply determines the unloaded voltage, usually about 15% higher. Supply voltage will also rise 10% during high line conditions.

$$\text{max supplies} \approx \pm(V_{Opeak} + 5)(1 + \text{regulation})(1.1) \quad (3)$$

The input sensitivity and output power specs determine the required gain.

$$A_V \geqslant \frac{\sqrt{P_O R_L}}{V_{IN}} = \frac{V_{ORMS}}{V_{INRMS}} \quad (4)$$

Normally the gain is set between 20 and 200; for a 25 watt, 8 ohm amplifier this results in a sensitivity of 710 mV and 71 mV, respectively. The higher the gain, the higher the THD, as can be seen from the characteristics curves. Higher gain also results in more hum and noise at the output.

The desired input impedance is set by R_{IN}. Very high values can cause board layout problems and DC offsets at the output. The bandwidth requirements determine the size of C_f and C_C as indicated in the external component listing.

The output transistors and drivers must have a breakdown voltage greater than the voltage determined by equation (3). The current gain of the driver and output device must be high enough to supply I_{Opeak} with 5 mA of drive from the LM391. The power transistors must be able to dissipate approximately 40% of the maximum output power; the drivers must dissipate this amount divided by the current gain of the outputs. See the output transistor selection guide, table A.

To prevent thermal runaway of the AB bias current the following equation must be valid:

$$\theta_{JA} \leqslant \frac{R_E(\beta_{MIN} + 1)}{V_{CEQMAX}(K)} \quad (5)$$

where:

θ_{JA} is the thermal resistance of the driver transistor, junction to ambient, in °C/W.

R_E is the emitter degeneration resistance in ohms.

β_{min} is that of the output transistor.

V_{CEQMAX} is the highest possible value of one supply from equation (3).

K is the temperature coefficient of the driver base-emitter voltage, typically 2 mV/°C.

Often the value of R_E is to be determined and equation (5) is rearranged to be:

$$R_E \geqslant \frac{\theta_{JA}(V_{CEQMAX})K}{\beta_{MIN} + 1} \quad (6)$$

The maximum average power dissipation in each output transistor is:

$$P_{DMAX} = 0.4\,P_{OMAX} \quad (7)$$

The power dissipation in the driver transistor is:

$$P_{DRIVER(MAX)} = \frac{P_{DMAX}}{\beta_{MIN}} \quad (8)$$

Heat sink requirements are found using the following formulas:

$$\theta_{JA} \leqslant \frac{T_{JMAX} - T_{AMAX}}{P_D} \quad (9)$$

$$\theta_{SA} \leqslant \theta_{JA} - \theta_{JC} - \theta_{CS} \quad (10)$$

where:

T_{jMAX} is maximum transistor junction temperature.

T_{AMAX} is maximum ambient temperature.

θ_{JA} is thermal resistance junction to ambient.

θ_{SA} is thermal resistance sink to ambient.

θ_{JC} is thermal resistance junction to case.

θ_{CS} is thermal resistance case to sink, typically 1°C/W for most mountings.

Application Hints (Continued)

PROTECTION CIRCUITRY

The protection circuits of the LM391 are very flexible and should be tailored to the output transistor's safe operating area. The protection V-I characteristics, circuitry, and resistor formulas are described below. The diodes from the output to each supply prevent the output voltage from exceeding the supplies and harming the output transistors. The output will do this if the protection circuitry is activated while driving an inductive load.

TURN-ON DELAY

It is often desirable to delay the turn-ON of the power amplifier so turn-ON pops in the preamplifier do not go to the speakers.

This is easily implemented by putting a resistor in series with a capacitor from pin 14 to ground. The value of the resistor is set to limit the current to less than 1 mA (the absolute maximum). This resistor with the capacitor gives a time constant of RC. The turn-ON delay is approximately 2 time constants.

Example:

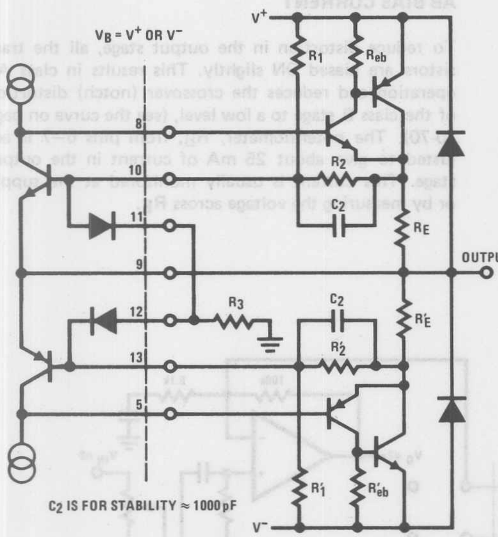
Amplifier with maximum supply of 30V, like the 20 W, 8Ω example in the data sheet, requiring a delay of 1 second.

Time delay = 2 RC

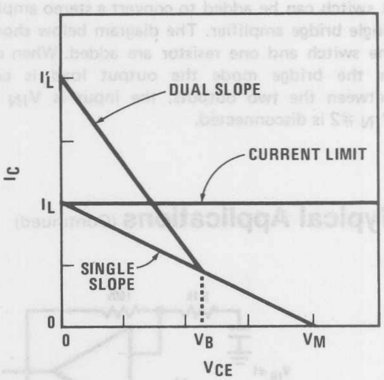
$$R = \frac{\text{Max } V^+}{1 \text{ mA}}$$

So:

R = 30k. Solving for C gives 16.7 μF. Use C = 20 μF with a 30V rating.



Protection Circuitry with External Components



Protection Characteristics

Protection Circuit Resistor Formulas ($V_B = V^+$)

Type of Protection	R_E, R_E'	R_1, R_1'	R_2, R_2'	R_3, R_3'
Current Limit	$R_E = \frac{\phi}{I_L}$	Not Required	Short	Not Required
Single Slope SOA Protection	$R_E = \frac{\phi}{I_L}$	$R_1 = R_2\left(\frac{V_M - \phi}{\phi}\right)$	1 kΩ	Not Required
Dual Slope SOA Protection ($V_B = V^+$)	$R_E = \frac{\phi}{I_L}$	$R_1 = R_2\left(\frac{V_M - \phi}{\phi}\right)$	1 kΩ	$R_3 = R_2\left[\frac{V^+}{I_L R_E - \phi} - 1\right]$

Note: ϕ is the current limit V_{BE} voltage, 650 mV. Assumptions: $V^+ >> \phi$, $V_M >> \phi$. V^+ is the load supply voltage. V_M is the maximum rated V_{CE} of the output transistors.

Application Hints (Continued)

TRANSIENT INTERMODULATION DISTORTION

There has been a lot of interest in recent years about transient intermodulation distortion. Matti Otala of University of Oulu, Oulu, Finland has published several papers on the subject. The results of these investigations show that the open loop pole of the power amplifier should be above 20 kHz.

To do this with the LM391 is easy. Put a 1 MΩ resistor from pin 3 to the output and the open loop gain is reduced to about 46 dB. Now the open loop pole is at 30 kHz. The current in this resistor causes an offset in the input stage that can be cancelled with a resistor from pin 4 to ground. The resistor from pin 4 to ground should be 910 kΩ rather than 1 MΩ to insure that the shutdown circuitry will operate correctly. The slight difference in resistors results in about 15 mV of offset. The 40 W, 8 Ω amplifier schematic shows the hookup of these two resistors.

BRIDGE AMPLIFIER

A switch can be added to convert a stereo amplifier to a single bridge amplifier. The diagram below shows where the switch and one resistor are added. When operating in the bridge mode the output load is connected between the two outputs, the input is V_{IN} #1, and V_{IN} #2 is disconnected.

OSCILLATIONS & GROUNDING

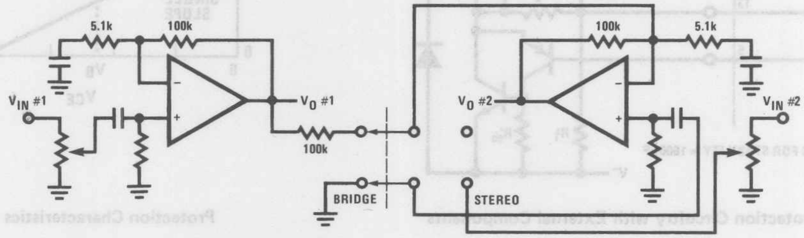
Most power amplifiers work the first time they are turned on. They also tend to oscillate and have excess THD. Most oscillation problems are due to inadequate supply bypassing and/or ground loops. A 10 μF, 50 V electrolytic on each power supply will stop supply-related oscillations. However, if the signal ground is used for these bypass caps the THD is usually excessive. The signal ground must return to the power supply alone, as must the output load ground. All other grounds — bypass, output R-C, protection, etc., can tie together and then return to supply. This ground is called high frequency ground. On the 40 W amplifier schematic all the grounds are labeled.

Capacitive loads can cause instabilities, so they are isolated from the amplifier with an inductor and resistor in the output lead.

AB BIAS CURRENT

To reduce distortion in the output stage, all the transistors are biased ON slightly. This results in class AB operation and reduces the crossover (notch) distortion of the class B stage to a low level, (see the curve on page 10-70). The potentiometer, R_B, from pins 6–7 is adjusted to give about 25 mA of current in the output stage. This current is usually monitored at the supply or by measuring the voltage across R_E.

Typical Applications (Continued)



Bridge Circuit Diagram

Output Transistors Selection Guide

Table A.

Output Power	Driver Transistor		Output Transistor	
	PNP	NPN	PNP	NPN
20 W @ 8 Ω 30 W @ 4 Ω	BD344	BD345	BD346	BD347
40 W @ 8 Ω 60 W @ 4 Ω	BD348	BD349	BD350	BD351

Application Hints (Continued)

A 20 W, 8 Ω; 30 W, 4 Ω AMPLIFIER

Givens:

Power output	20 W into 8 Ω 30 W into 4 Ω
Input Sensitivity	1 V max
Input Impedance	100k
Bandwidth	20 Hz - 20 kHz ± 0.25 dB

Equations (1) and (2) give:

20 W/8 Ω	$V_{OP} = 17.9\,V$	$I_{OP} = 2.24\,A$
30 W/4 Ω	$V_{OP} = 15.5\,V$	$I_{OP} = 3.87\,A$

Therefore the supply required is:

±23 V @ 2.24 A, reducing to . . .

±21 V @ 3.87 A

With 15% regulation and high line we get ±29 V from equation (3).

Sensitivity and equation (4) set minimum gain:

$$A_V \geqslant \frac{\sqrt{20 \times 8}}{1} = 12.65$$

We will use a gain of 20 with resulting sensitivity of 632 mV.

Letting R_{IN} equal 100k gives the required input impedance. For low DC offsets at the output we let R_{f2} = 100k. Solving for R_{f1} gives:

$$R_{f2} = 100k$$

$$R_{f1} = \frac{100k}{20 - 1} = 5.26k\text{; use } 5.1k$$

The bandwidth requirement must be stated as a pole, i.e., the 3 dB frequency. Five times away from a pole gives 0.17 dB down, which is better than the required 0.25 dB. Therefore:

$$f_L = \frac{20}{5} = 4\,\text{Hz}$$

$$f_h = 20k \times 5 = 100\,\text{kHz}$$

Solving for C_f:

$$C_f \geqslant \frac{1}{2\pi R_{f1} f_L} = 7.8\,\mu F\text{; use } 10\,\mu F$$

The recommended value for C_C is 5 pF for gains of 20 or larger. This gives a gain-bandwidth product of 6.4 MHz and a resulting bandwidth of 320 kHz, better than required.

The breakdown voltage requirement is set by the maximum supply; we need a minimum of 58 V and will use 60 V. We must now select a 60 V power transistor with reasonable beta at I_{Opeak}, 3.87 A. The National BD346, BD347 complementary pair are 60 V, 60 W transistors with a minimum beta of 30 at 4 A. The driver transistor must supply the base drive given 5 mA drive from the LM391. The National BD344, BD345 complementary driver transistors are 60 V devices with a minimum beta of 40 at 200 mA. The driver transistors should be much faster (higher f_T) than the output transistors to insure that the R-C on the output will prevent instability.

To find the heat sink required for each output transistor we use equations (7), (9), and (10):

$$\overline{P_D} = 0.4\,(30) = 12\,W \qquad (7)$$

$$\theta_{JA} \leqslant \frac{150^\circ C - 55^\circ C}{12} = 7.9^\circ C/W \text{ for } T_{AMAX} = 55^\circ C \qquad (9)$$

$$\theta_{SA} \leqslant 7.9 - 2.1 - 1.0 = 4.8^\circ C/W \qquad (10)$$

If both transistors are mounted on one heat sink the thermal resistance should be halved to 2.4°C/W.

The maximum average power dissipation in each driver is found using equation (8):

$$\overline{P_{DRIVER(MAX)}} = \frac{12}{30} = 400\,mW$$

Using equation (9):

$$\theta_{JA} \leqslant \frac{155 - 55}{0.4} = 237^\circ C/W$$

..., no heat sink is required.

Using this information and equation (6) we can find the minimum value of R_E required to prevent thermal runaway.

$$R_E \geqslant \frac{100\,(30)\,(0.002)}{30 + 1} = 0.19\,\Omega \qquad (6)$$

We must now use the SOA data on the National BD346, BD347 transistors to set up the protection circuit. Below is the SOA curve with the 4 Ω and 8 Ω load lines. Also shown are the desired protection lines. Note the value of V_B is equal to the supply voltage, so we use the formulas in the table.

D.C. SOA of BD346, BD347 Transistors

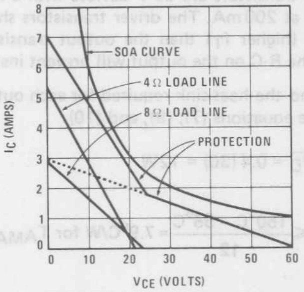


Figure Y.

$V_M = 60\text{ V}, V_B = 23\text{ V}, I_L = 3\text{ A}, I'_L = 7\text{ A}$

Using the dual slope protection formulas:

$$R_E = \frac{0.65}{3} = 0.22\,\Omega$$

$$R_2 = 1\text{k}$$

$$R_1 = 1\text{k}\left(\frac{60 - 0.65}{0.65}\right) \approx 91\text{k}$$

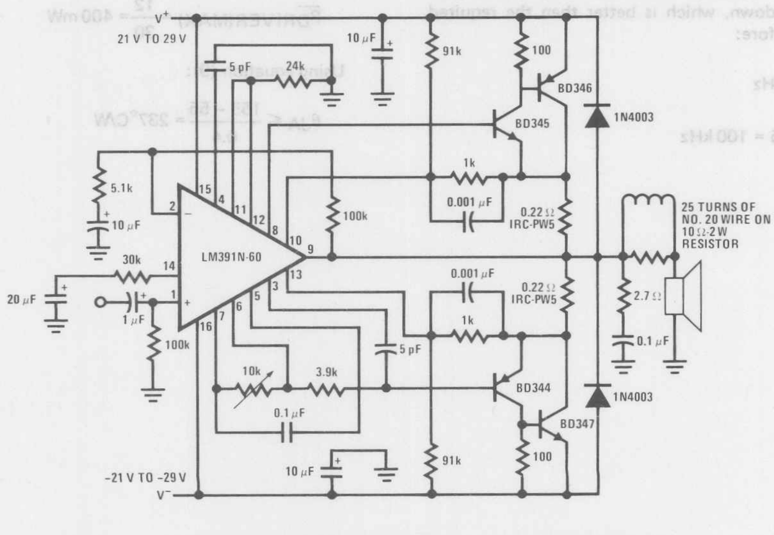
$$R_3 = 1\text{k}\left(\frac{23}{7\,(0.22) - 0.65} - 1\right) \approx 24\text{k}$$

Note that an R_E of 0.22 Ω satisfies equation (6). The final schematic of this amplifier is below. If the output is shorted the current will be 1.8 A and V_{CE} is 23 V. Since the input is AC, the average power is:

$$\text{short } \overline{P_D} = \tfrac{1}{2}\,(1.8)\,(23) \approx 21\text{ W}$$

This power is greater than was used in the heat sink calculations, so the transistors will overheat for long-duration shorts unless a larger heat sink is used.

Typical Applications (Continued)



20 W-8 Ω, 30W-4 Ω Amplifier with 1 Second Turn-ON Delay

Application Hints (Continued)

A 40 W/8 Ω, 60 W/4 Ω AMPLIFIER

Given:

Power Output	40 W/8 Ω
	60 W/4 Ω
Input Sensitivity	1 V max
Input Impedance	100k
Bandwidth	20 Hz - 20 kHz ± 0.25 dB

Equations (1) and (2) give:

40 W/8 Ω $V_{Opeak} = 25.3\ V$ $I_{Opeak} = 3.16\ A$

60 W/4 Ω $V_{Opeak} = 21.9\ V$ $I_{Opeak} = 5.48\ A$

Therefore the supply required is:

±30.3 V @ 3.16 A, reducing to . . .

±26.9 V @ 5.48 A

With 15% regulation and high line we get ±38.3 V using equation (3).

The minimum gain from equation (4) is:

$A_V \geqslant 18$

We select a gain of 20; resulting sensitivity is 900 mV.

The input impedance and bandwidth are the same as the 20 watt amplifier so the components are the same.

$R_{f1} = 5.1k$ $R_{IN} = 100k$ $C_C = 5\ pF$

$R_{f2} = 100k$ $C_f = 10\ \mu F$

The maximum supplies dictate using 80 V devices. The National BD350, BD351 pair are 80 V, 160 W transistors with a minimum beta of 40 at 2 A and 20 at 6 A. This corresponds to a minimum beta of 22.5 at 5.5 A (I_{Opeak}). The National BD348, BD349 driver pair are 80 V transistors with a minimum beta of 50 at 250 mA. This output combination guarantees I_{Opeak} with 5 mA from the LM391.

Output transistor heat sink requirements are found using equations (7), (9), and (10):

$$\overline{P_D} = 0.4\,(60) = 24\ W \qquad (7)$$

$$\theta_{JA} \leqslant \frac{200-55}{24} = 6.0°C/W \text{ for } T_{AMAX} = 55°C \qquad (9)$$

$$\theta_{SA} \leqslant 6.0 - 1.1 - 1.0 = 3.9°C/W \qquad (10)$$

For both output transistors on one heat sink the thermal resistance should be 1.9°C/W.

Now using equation (8) we find the power dissipation in the driver:

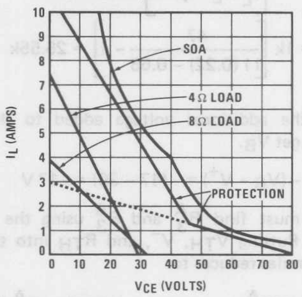
$$\overline{P_{DRIVER}} = \frac{24}{20} = 1.2\ W \qquad (8)$$

$$\theta_{JA} \leqslant \frac{150-55}{1.2} = 79°C/W \qquad (9)$$

Since a heat sink is required on the driver, we should investigate the output stage thermal stability at the same time to optimize the design. If we find a value of R_E that is good for the protection circuitry, we can then use equation (5) to find the heat sink required for the drivers.

The SOA characteristics of the National BD350, BD351 transistors are shown in the following curve along with a desired protection line.

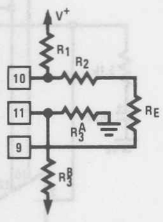
SOA BD350, BD351



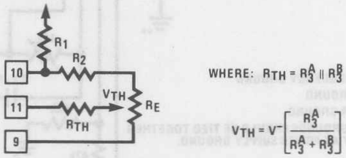
The desired data points are:

$V_M = 80\ V$ $V_B = 47\ V$ $I_L = 3\ A$ $I'_L = 11\ A$

Since the break voltage is not equal to the supply, we will use two resistors to replace R_3 and move V_B.



Circuit Used



Thevenin Equivalent

Application Hints (Continued)

The formulas for R_E, R_1, and R_2 do not change:

$$R_E = \frac{0.65}{3\,A} = 0.22\,\Omega$$

$$R_2 = 1k \qquad R_1 = 1k\,\frac{80 - 0.65}{0.65} = 120k$$

The formula for R_3 now gives R_{TH} when the V^+ in the formula becomes V_B.

$$R_{TH} = R_2\left[\frac{V_B}{I'_L R_E - \phi} - 1\right]$$

$$= 1k\left[\frac{47}{11\,(0.22) - 0.65} - 1\right] = 25.55k$$

V_{TH} is the additional voltage added to the supply voltage to get V_B.

$$V_{TH} = -(V_B - V^+) = -(47 - 30) = -17\,V$$

Now we must find R_3^A and R_3^B using the Thevinen formulas. Putting V_{TH}, V^-, and R_{TH} into the appropriate formulas reduces to:

$$R_3^B = 0.76\,R_3^A \quad \text{and} \quad 25.55k = R_3^A \parallel R_3^B$$

The easiest way to solve these equations is to iterate with standard values. If we guess $R_3^A = 62k$, then $R_3^B = 47.12k$; use 47k. The Thevin impedance comes out 26.7k, which is close enough to 25.55k.

Now we will use equation (5) to determine the heat sinking requirements of the drivers to insure thermal stability:

$$\theta_{JA} \leqslant \frac{0.22\,(20 + 1)}{40\,(0.002)} \approx 57^\circ C/W \tag{5}$$

This value is lower than we got with equation (9), so we will use it in equation (10):

$$\theta_{SA} \leqslant 57 - 6 - 1 = 50^\circ C/W \tag{10}$$

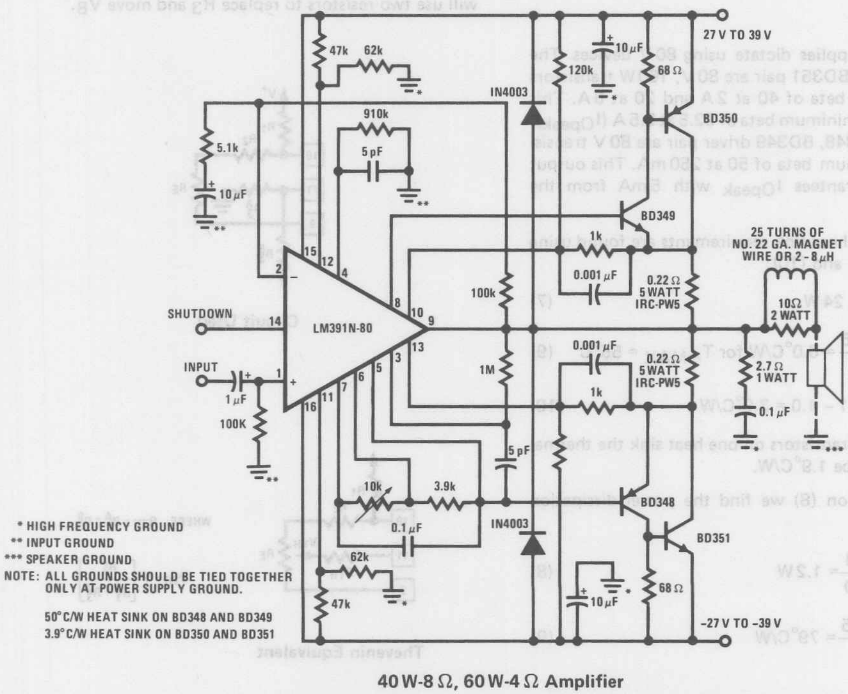
This is the required heat sink for each driver. For low TIM we add the 1 MΩ resistor from pin 3 to the output and a 910k resistor from pin 4 to ground. The complete schematic is on page 11.

If the output is shorted, the transistor voltage is about 28 V and the current is 5 A. Therefore the average power is:

$$\text{short } \overline{P_D} = \tfrac{1}{2}\,(28)\,5 = 70\,W$$

This is much larger than the power used to calculate the heat sinks and the output transistors will overheat if the output is shorted too long.

Typical Applications (Continued)



40 W-8 Ω, 60 W-4 Ω Amplifier

National Semiconductor

LM1035 Dual DC Operated Tone/Volume/Balance Circuit

General Description

The LM1035 is a DC controlled tone (bass/treble), volume and balance circuit for stereo applications in car radio, TV and audio systems. An additional control input allows loudness compensation to be simply effected.

Four control inputs provide control of the bass, treble, balance and volume functions through application of DC voltages from a remote control system or, alternatively, from four potentiometers which may be biased from a zener regulated supply provided on the circuit.

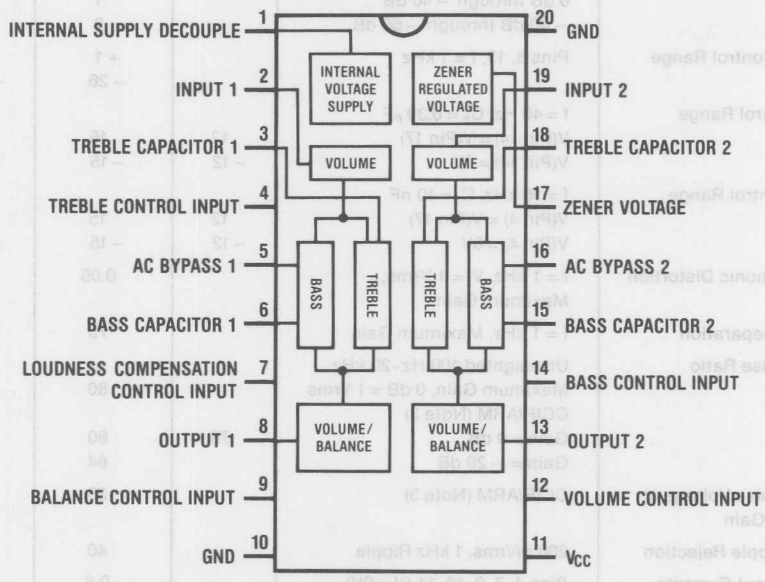
Each tone response is defined by a single capacitor chosen to give the desired characteristic.

Features

- Wide supply voltage range, 8V to 18V
- Large volume control range, 80 dB typical
- Tone control, ± 15 dB typical
- Channel separation, 75 dB typical
- Low distortion, 0.05% typical for an input level of 1 Vrms
- High signal to noise, 80 dB typical for an input level of 1 Vrms
- Few external components required

Block and Connection Diagram

Dual-In-Line Package



TOP VIEW

Storage Temperature Range −65°C to +150°C

Lead Temperature (Soldering, 10 seconds) 300°C

Electrical Characteristics $V_{CC} = 12V$, $T_A = 25°C$ (unless otherwise stated)

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage Range	Pin 11	8		18	V
Supply Current			35	45	mA
Zener Regulated Output	Pin 17				
Voltage			5.4		V
Current				5	mA
Maximum Output Voltage	Pins 8, 13; f = 1 kHz				
	$V_{CC} = 8V$		1.3		Vrms
	$V_{CC} = 12V$	2	2.5		Vrms
	$V_{CC} = 18V$		3.5		Vrms
Maximum Input Voltage (Note 1)	Pins 2, 19; f = 1 kHz Flat Response	2	2.5		Vrms
Input Resistance	Pins 2, 19; f = 1 kHz	20	30		kΩ
Output Resistance	Pins 8, 13; f = 1 kHz		20		Ω
Maximum Gain	V(Pin 12) = V(Pin 17); f = 1 kHz	−2	0	2	dB
Volume Control Range	f = 1 kHz	70	80		dB
Gain Tracking	f = 1 kHz				
	0 dB through −40 dB		1	3	dB
	−40 dB through −60 dB		2		dB
Balance Control Range	Pins 8, 13; f = 1 kHz		+1		dB
			−26	−20	dB
Bass Control Range (Note 2)	f = 40 Hz, $C_b = 0.39\ \mu F$				
	V(Pin 14) = V(Pin 17)	12	15	18	dB
	V(Pin 14) = 0V	−12	−15	−18	dB
Treble Control Range (Note 2)	f = 16 kHz, $C_t = 10$ nF				
	V(Pin 4) = V(Pin 17)	12	15	18	dB
	V(Pin 4) = 0V	−12	−15	−18	dB
Total Harmonic Distortion	f = 1 kHz, $V_i = 1$ Vrms, Maximum Gain		0.05	0.2	%
Channel Separation	f = 1 kHz, Maximum Gain		75		dB
Signal/Noise Ratio	Unweighted 100 Hz–20 kHz				
	Maximum Gain, 0 dB = 1 Vrms		80		dB
	CCIR/ARM (Note 3)				
	Gain = 0 dB	76	80		dB
	Gain = −20 dB		64		dB
Output Noise Voltage at Minimum Gain	CCIR/ARM (Note 3)		25	35	μV
Supply Ripple Rejection	200 mVrms, 1 kHz Ripple		40		dB
Control Input Currents	Pins 4, 7, 9, 12, 14 (V = 0V)		−0.6	−2.5	μA
Frequency Response	−1 dB (Flat Response 20 Hz–16 kHz)		250		kHz

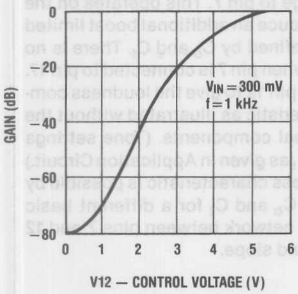
Note 1: The maximum permissible input level is dependent on tone and volume settings. See Application Notes.

Note 2: The tone control range is defined by capacitors C_b and C_t. See Application Notes.

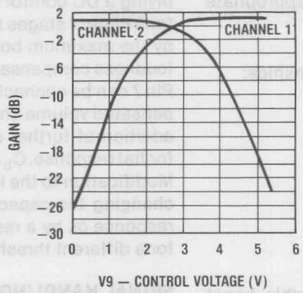
Note 3: Measured with a CCIR filter with a 0 dB level at 2 kHz and an average responding meter.

Typical Performance Characteristics

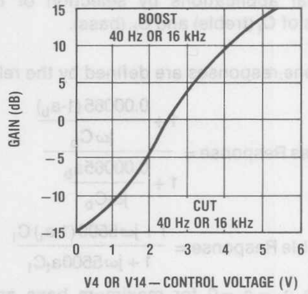
Volume Control Characteristic



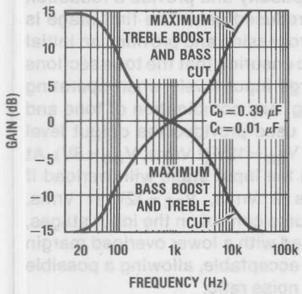
Balance Control Characteristic



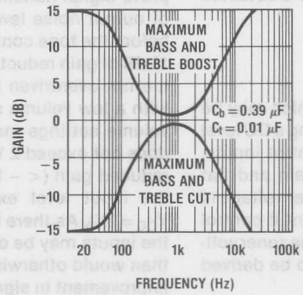
Tone Control Characteristic



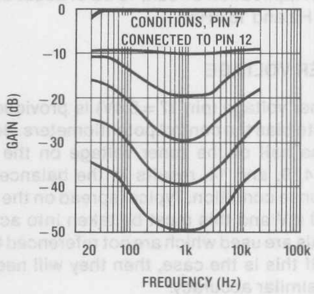
Tone Characteristic (Gain vs Frequency)



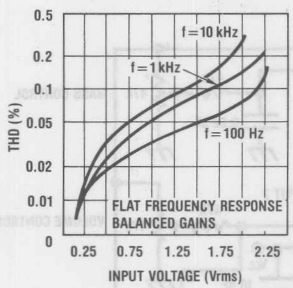
Tone Characteristic (Gain vs Frequency)



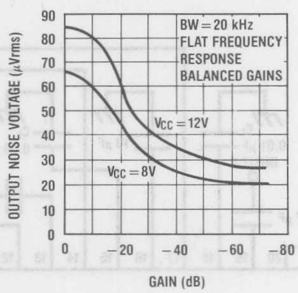
Loudness Compensated Volume Characteristic



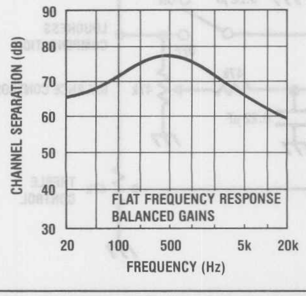
THD vs Input Voltage



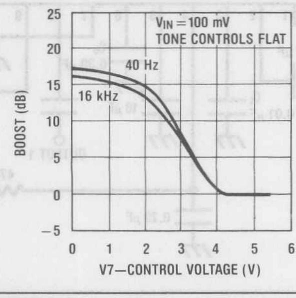
Output Noise Voltage vs Gain



Channel Separation vs Frequency



Loudness Control Characteristic



Application Notes

TONE RESPONSE

The maximum boost and cut can be optimized for individual applications by selection of the appropriate values of C_t (treble) and C_b (bass).

The tone responses are defined by the relationships:

$$\text{Bass Response} = \frac{1 + \dfrac{0.00065\,(1-a_b)}{j\omega C_b}}{1 + \dfrac{0.00065a_b}{j\omega C_b}}$$

$$\text{Treble Response} = \frac{1 + j\omega 5500\,(1-a_t)\,C_t}{1 + j\omega 5500 a_t C_t}$$

Where $a_b = a_t = 0$ for maximum bass and treble boost respectively and $a_b = a_t = 1$ for maximum cut.

For the values of C_b and C_t of 0.39 μF and 0.01 μF as shown in the Application Circuit, 15 dB of boost or cut is obtained at 40 Hz and 16 kHz.

ZENER VOLTAGE

A zener voltage (pin 17 = 5.4V) is provided which may be used to bias the control potentiometers. Setting a DC level of one half of the zener voltage on the control inputs, pins 4, 9, and 14, results in the balanced gain and flat response condition. Typical spread on the zener voltage is ± 100 mV and this must be taken into account if control signals are used which are not referenced to the zener voltage. If this is the case, then they will need to be derived with similar accuracy.

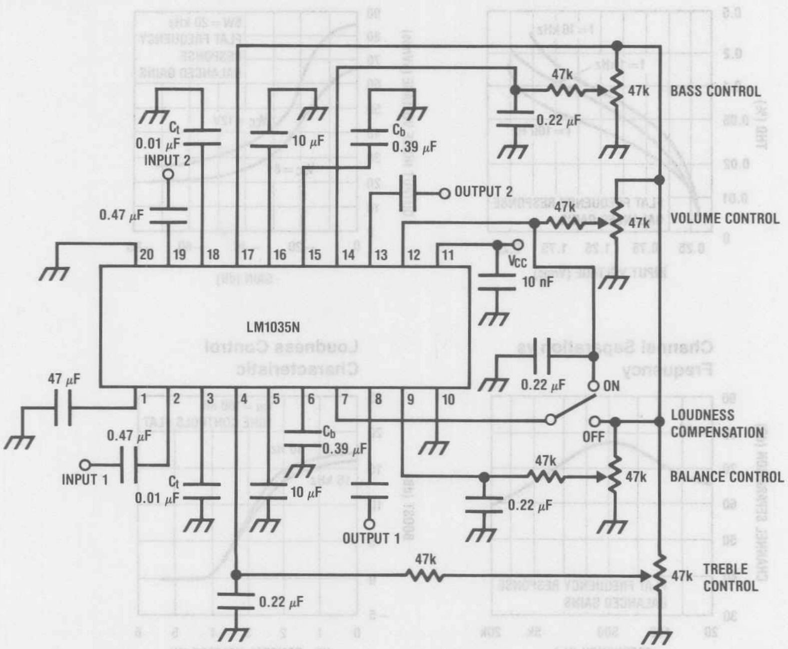
LOUDNESS COMPENSATION

A simple loudness compensation may be effected by applying a DC control voltage to pin 7. This operates on the tone control stages to produce an additional boost limited by the maximum boost defined by C_b and C_t. There is no loudness compensation when pin 7 is connected to pin 17. Pin 7 can be connected to pin 12 to give the loudness compensated volume characteristic as illustrated without the addition of further external components. (Tone settings for flat response. C_b and C_t as given in Application Circuit.) Modification to the loudness characteristic is possible by changing the capacitors C_b and C_t for a different basic response or, by a resistor network between pins 7 and 12 for a different threshold and slope.

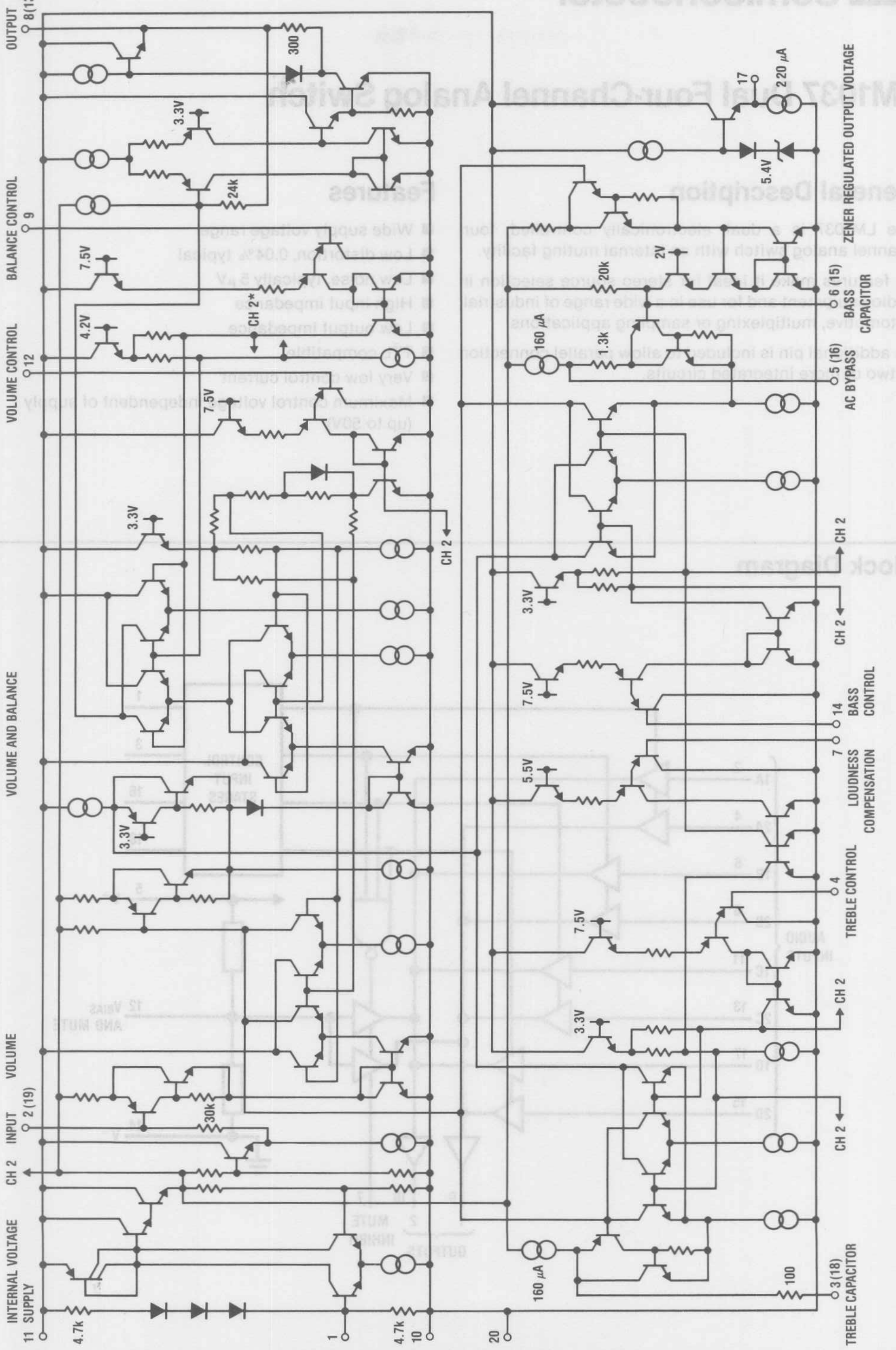
SIGNAL HANDLING

The volume control function of the LM1035 is carried out in two stages, controlled by the DC voltage on pin 12, to improve signal handling capability and provide a reduction of output noise level at reduced gain. The first stage is before the tone control processing and provides an initial 15 dB of gain reduction so ensuring that the tone sections are not overdriven by large input levels when operating with a low volume setting. Any combination of tone and volume settings may be used provided the output level does not exceed 2 Vrms, V_{CC} = 12V (1 Vrms, V_{CC} = 8V). At reduced gain (< − 15 dB) the input stage will overload if the input level exceeds 2 Vrms, V_{CC} = 12V (1 Vrms, V_{CC} = 8V). As there is volume control on the input stages, the inputs may be operated with a lower overload margin than would otherwise be acceptable, allowing a possible improvement in signal to noise ratio.

Application Circuit



Simplified Schematic Diagram (One Channel)



*Connections reversed

LM1037 Dual Four-Channel Analog Switch

General Description

The LM1037 is a dual, electronically controlled, four-channel analog switch with an internal muting facility.

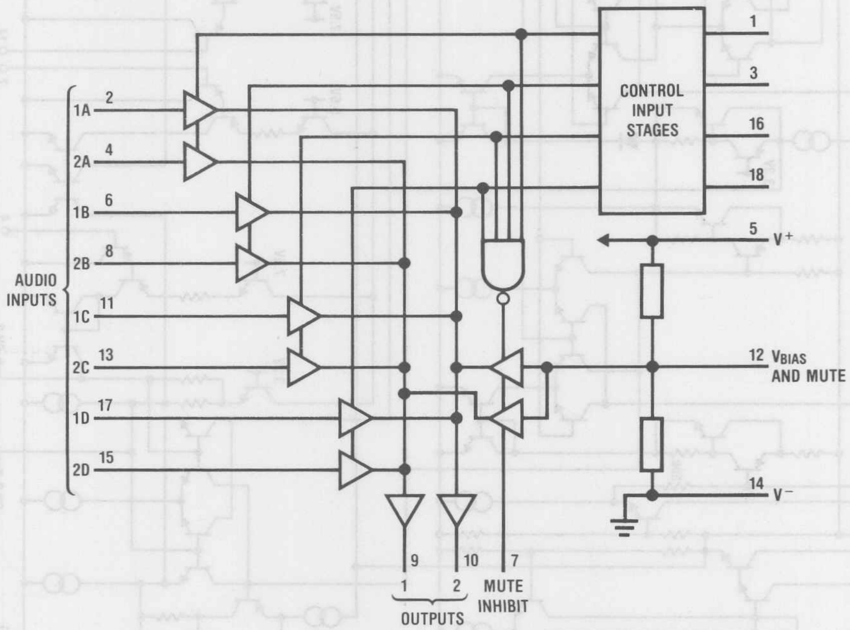
Its features make it ideal for stereo source selection in audio equipment and for use in a wide range of industrial, automotive, multiplexing or sampling applications.

An additional pin is included to allow parallel connection of two or more integrated circuits.

Features

- Wide supply voltage range
- Low distortion, 0.04% typical
- Low noise, typically 5 μV
- High input impedance
- Low output impedance
- TTL compatible
- Very low control current
- Maximum control voltage independent of supply (up to 50V)

Block Diagram



Absolute Maximum Ratings

Supply Voltage	32V
Operating Temperature Range	− 20°C to + 70°C
Storage Temperature Range	− 65°C to + 150°C
Lead Temperature (Soldering, 10 seconds)	300°C

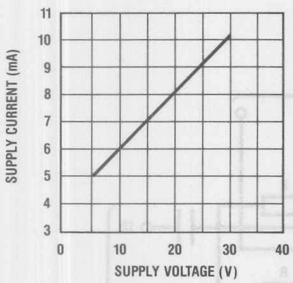
Electrical Characteristics $V_S = 12V$, $T_A = 25°C$

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage Range		5		28	V
Supply Current	$V_{SUPPLY} = 12V$		6.4	8.5	mA
	$V_{SUPPLY} = 30V$		10	12	mA
Voltage Gain		− 0.5	0	0.5	dB
Signal Handling (Note 1)	$V_{SUPPLY} = 12V$	2.8	2.9	3.0	Vrms
Distortion THD	$V_{SIGNAL} = 1$ Vrms @ 1 kHz		0.04	0.1	%
Noise Voltage at Output	CCIR/ARM $R_S = 2k$		5	15	μV
Channel Separation (Note 2)	$V_{SIGNAL} = 1$ Vrms @ 1 kHz		− 95		dB
Relative Output in Muted State	$V_{SIGNAL} = 1$ Vrms @ 1 kHz		− 90		dB

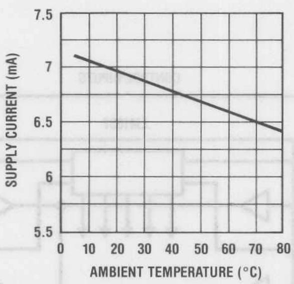
Note 1: The instantaneous maximum voltage difference between any two input pins of one channel is 9.6V. Voltages in excess of this level may cause increased distortion and degraded channel separation.

Typical Performance Characteristics

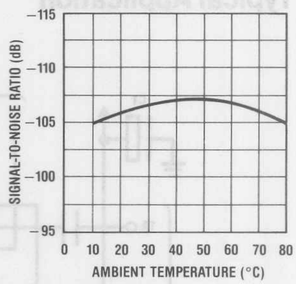
Supply Current vs Supply Voltage



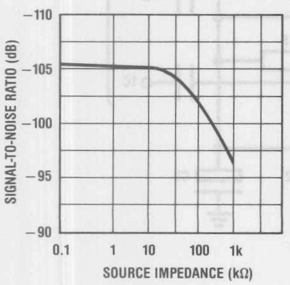
Supply Current vs Temperature



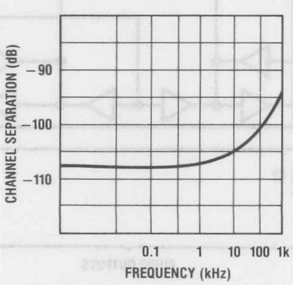
Signal-to-Noise vs Temperature (Note 2)



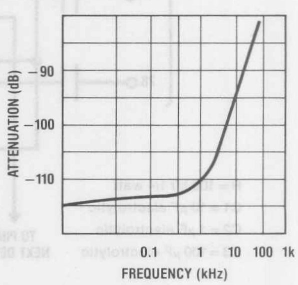
Signal-to-Noise vs Source Impedance (Note 2)



Channel Separation vs Frequency (Note 3)

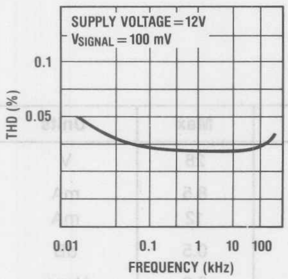


Attenuation of Unselected Inputs vs Frequency

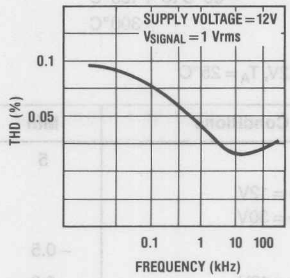


Typical Performance Characteristics (Continued)

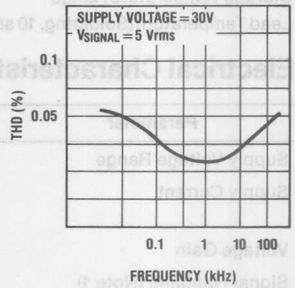
Total Harmonic Distortion vs Frequency



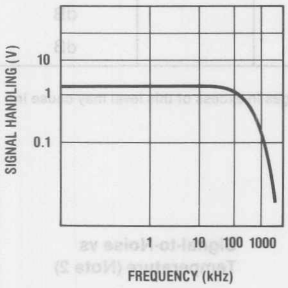
Total Harmonic Distortion vs Frequency



Total Harmonic Distortion vs Frequency



Signal Handling vs Frequency (Note 5)



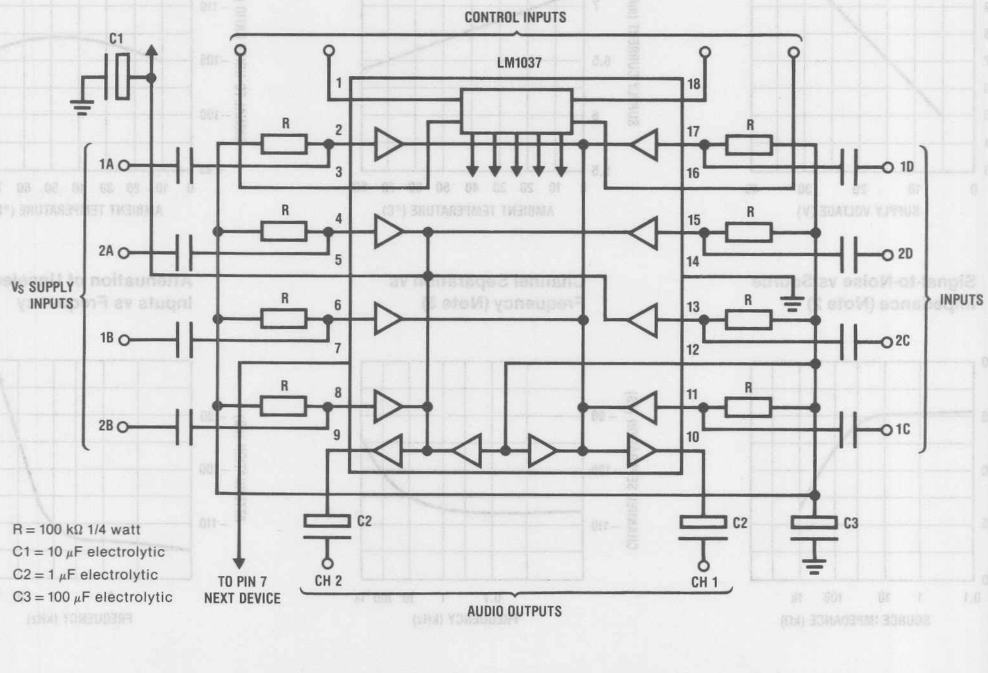
Note 2: Signal-to-noise measurement referred to a 1 Vrms input signal bandwidth to CCIR/ARM specifications.

Note 3: The level of output signal of a selected undriven amplifier with respect to the output level of a selected driven amplifier. For test purposes, signal is applied to only one input and all other inputs are decoupled to eliminate stray pick-up through external components. Channel separation is then defined as the ratio of signal levels of the two output pins.

Note 4: For test purposes, signals are connected to three unselected input pins of one channel group and all other inputs are decoupled to eliminate stray pick-up through external components.

Note 5: Supply voltage 12V; signal handling defined at 1% distortion.

Typical Application



Truth Tables

LM1037

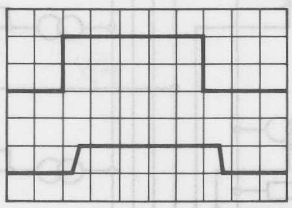
Channel selection is achieved by the application of DC voltages to the control pins.

		Inputs Switched to Output Pins								
I/P Channel		**1A**	**2A**	**1B**	**2B**	**1C**	**2C**	**1D**	**2D**	**Mute Control**
Pin No.		**2**	**4**	**6**	**8**	**11**	**13**	**17**	**15**	**12**
DC Control Conditions (Pins)	1	V_L	V_L	V_L	V_L	V_H	V_H	V_L	V_L	V_L
	3	V_L	V_L	V_L	V_L	V_L	V_L	V_H	V_H	V_L
	16	V_H	V_H	V_L	V_L	V_L	V_L	V_L	V_L	V_L
	18	V_L	V_L	V_H	V_H	V_L	V_L	V_L	V_L	V_L
Output Pin		10	9	10	9	10	9	10	9	9 and 10
Output		O/P1	O/P2	O/P1	O/P2	O/P1	O/P2	O/P1	O/P2	

Low switching level (V_L) < 0.8V

High switching level (V_H) > 2.0V and up to 50V

SWITCHING SPEED
VERTICAL 2V/DIV
HORIZONTAL 2 μs/DIV



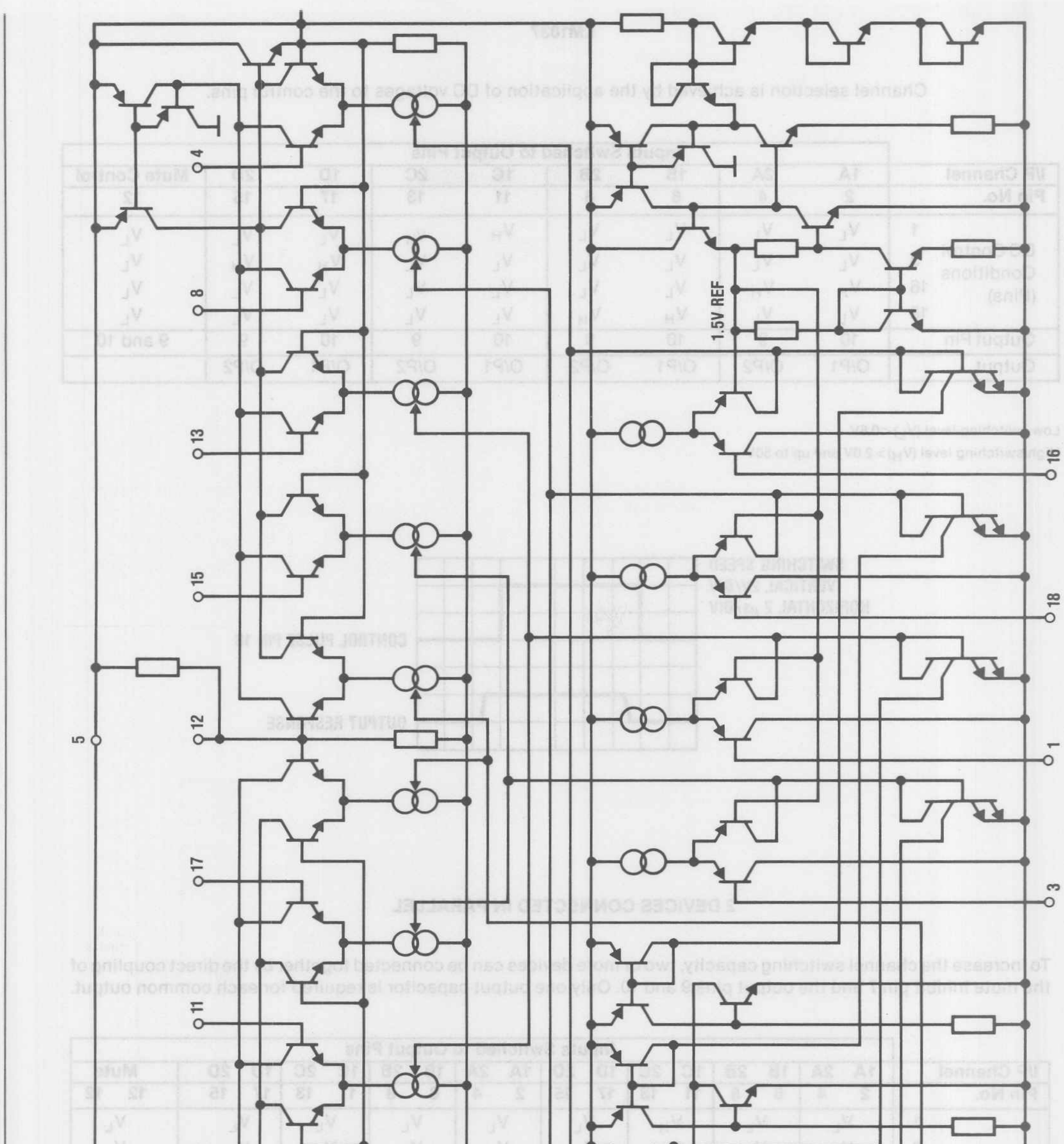
CONTROL PULSE PIN 18

OUTPUT RESPONSE

2 DEVICES CONNECTED IN PARALLEL

To increase the channel switching capacity, two or more devices can be connected together by the direct coupling of the mute inhibit pin 7 and the output pins 9 and 10. Only one output capacitor is required for each common output.

		Inputs Switched to Output Pins								
I/P Channel		**1A 2A**	**1B 2B**	**1C 2C**	**1D 2D**	**1A 2A**	**1B 2B**	**1C 2C**	**1D 2D**	**Mute**
Pin No.		**2 4**	**6 8**	**11 13**	**17 15**	**2 4**	**6 8**	**11 13**	**17 15**	**12 12**
DC Control Conditions (Pins)	1	V_L	V_L	V_H	V_L	V_L	V_L	V_L	V_L	V_L
	3	V_L	V_L	V_L	V_H	V_L	V_L	V_L	V_L	V_L
	16	V_H	V_L	V_L	V_L	V_L	V_L	V_L	V_L	V_L
	18	V_L	V_H	V_L	V_L	V_L	V_L	V_L	V_L	V_L
	1	V_L	V_L	V_L	V_L	V_L	V_L	V_H	V_L	V_L
	3	V_L	V_L	V_L	V_L	V_L	V_L	V_L	V_H	V_L
	16	V_L	V_L	V_L	V_L	V_H	V_L	V_L	V_L	V_L
	18	V_L	V_L	V_L	V_L	V_L	V_H	V_L	V_L	V_L
Output Pins		10 9	10 9	10 9	10 9	10 9	10 9	10 9	10 9	10 9



1.5V REF
4
8
13
15
12
17
11
6
2
10
5
16
18
1
3
7
14

National Semiconductor

Audio/Radio Circuits
PRELIMINARY

LM1038 Dual Four-Channel Analog Switch

General Description

The LM1038 is a dual, electronically controlled, four-channel analog switch with an internal muting facility.

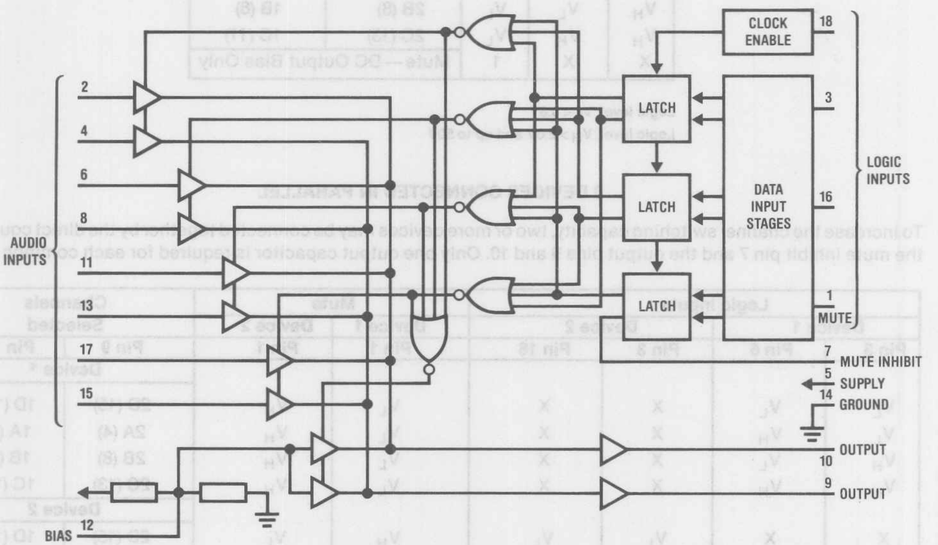
Its features make it ideal for stereo source selection in audio equipment and for use in a wide range of industrial, automotive, multiplexing or sampling applications.

An additional pin is included to allow parallel connection of two or more integrated circuits. Channel selection is achieved via two logic data pins with clock enabled latches.

Features

- Wide supply voltage range
- Low distortion, 0.04% typical
- High input impedance
- Low output impedance
- TTL compatible
- Very low control current
- Maximum control voltage independent of supply (up to 50V)
- 2 control pins accept BCD input pulses
- Clock enable input may be strobed from a bus

Block Diagram



Absolute Maximum Ratings

Supply Voltage	32V
Operating Temperature Range	− 20°C to + 70°C
Storage Temperature Range	− 65°C to + 150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics $V_S = 12V, T_A = 25°C$

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage Range		5		28	V
Supply Current	$V_{SUPPLY} = 12V$		14		mA
	$V_{SUPPLY} = 30V$		20		mA
Voltage Gain		− 0.5	0	0.5	dB
Signal Handling (Note 1)	$V_{SUPPLY} = 12V$	2.8	2.9	3.0	Vrms
Distortion THD	$V_{SIGNAL} = 1$ Vrms @ 1 kHz		0.04	0.1	%
Noise Voltage	CCIR Filter, $R_S = 2k$		5	15	μV
Channel Separation	$V_{SIGNAL} = 1$ Vrms @ 1 kHz		− 95		dB
Relative Output in Muted State	$V_{SIGNAL} = 1$ Vrms @ 1 kHz		− 90		dB

Note 1: The instantaneous maximum voltage difference between any two input pins of one channel is 9.6V. Voltages in excess of this level may cause increased distortion and degraded channel separation.

Truth Tables

LM1038

Logic Inputs		Mute	Stereo Channel Selected	
Pin 3	Pin 16	Pin 1	9 (Pin)	10 (Pin)
V_L	V_L	V_L	2D (15)	1D (17)
V_L	V_H	V_L	2A (4)	1A (2)
V_H	V_L	V_L	2B (8)	1B (6)
V_H	V_H	V_L	2C (13)	1C (11)
X	X	1	Mute — DC Output Bias Only	

Logic level, $V_L < 0.8V$

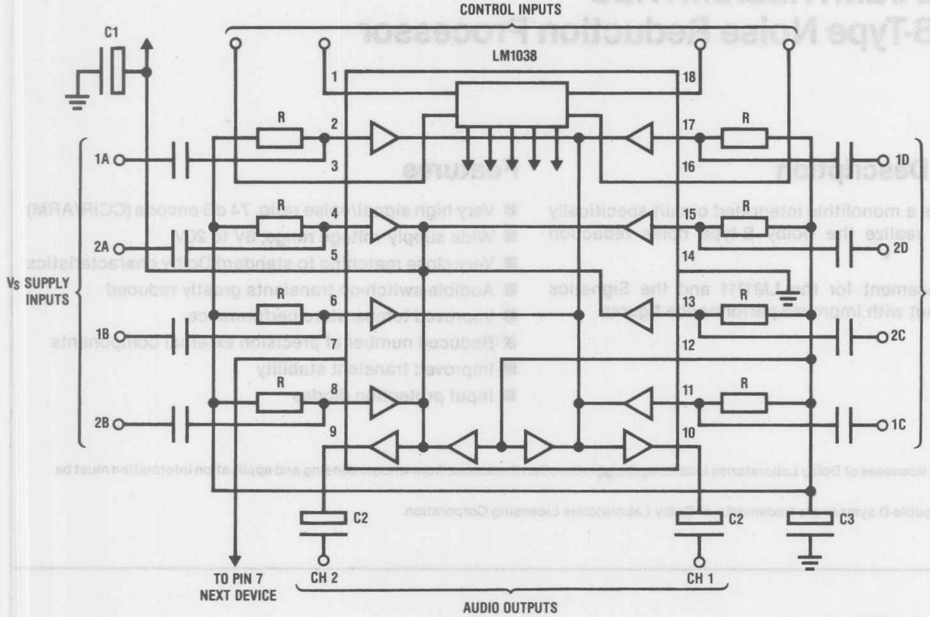
Logic level, $V_H > 2.0V$ and up to 50V

2 DEVICES CONNECTED IN PARALLEL

To increase the channel switching capacity, two or more devices may be connected together by the direct coupling of the mute inhibit pin 7 and the output pins 9 and 10. Only one output capacitor is required for each common output.

Logic Inputs				Mute		Channels Selected	
Device 1		Device 2		Device 1	Device 2		
Pin 3	Pin 6	Pin 3	Pin 16	Pin 1	Pin 1	Pin 9	Pin 10
						Device 1	
V_L	V_L	X	X	V_L	V_H	2D (15)	1D (17)
V_L	V_H	X	X	V_L	V_H	2A (4)	1A (2)
V_H	V_L	X	X	V_L	V_H	2B (8)	1B (6)
V_H	V_H	X	X	V_L	V_H	2C (13)	1C (11)
						Device 2	
X	X	V_L	V_L	V_H	V_L	2D (15)	1D (17)
X	X	V_L	V_H	V_H	V_L	2A (4)	1A (2)
X	X	V_H	V_L	V_H	V_L	2B (8)	1B (6)
X	X	V_H	V_H	V_H	V_L	2C (13)	1C (11)
X	X	X	X	V_H	V_H	Mute — DC Output Bias Only	

Typical Application



R = 100 kΩ 1/4 watt
C1 = 10 μF electrolytic
C2 = 1 μF electrolytic
C3 = 100 μF electrolytic

National Semiconductor

Audio/Radio Circuits

LM1112A/LM1112B/LM1112C Dolby B-Type Noise Reduction Processor

General Description

The LM1112 is a monolithic integrated circuit specifically designed to realize the Dolby B-type noise reduction system.

It is a replacement for the LM1111 and the Signetics NE-645/648 but with improved performance figures.

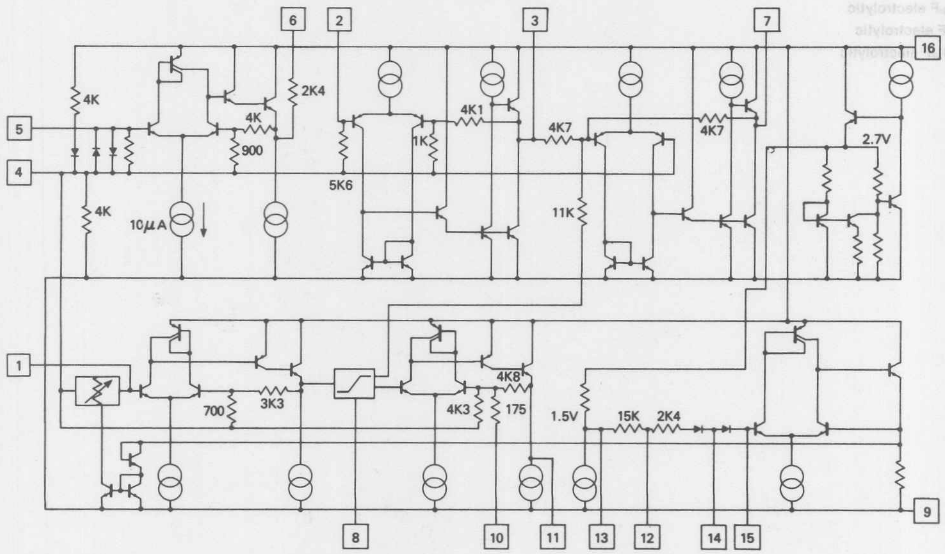
Features

- Very high signal/noise ratio, 74 dB encode (CCIR/ARM)
- Wide supply voltage range, 6V to 20V
- Very close matching to standard Dolby characteristics
- Audible switch-on transients greatly reduced
- Improved temperature performance
- Reduced number of precision external components
- Improved transient stability
- Input protection diodes

Available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, from whom licensing and application information must be obtained.

Dolby and the double-D symbol are trademarks of Dolby Laboratories Licensing Corporation.

Schematic Diagram



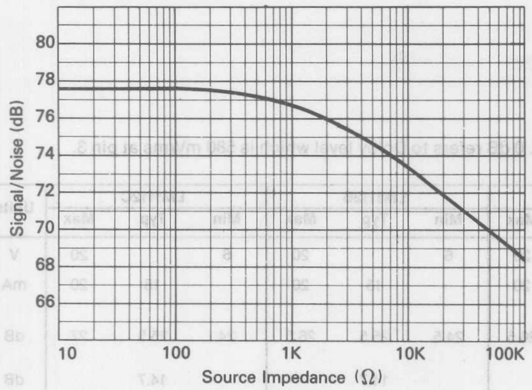
Storage Temperature Range	− 65°C to + 150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics $V_S = 12V$, $T_A = 25°C$. N.B. 0 dB refers to Dolby level which is 580 mVrms at pin 3.

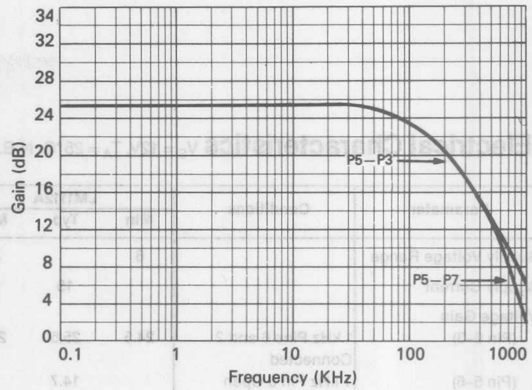
Parameter	Conditions	LM1112A			LM1112B			LM1112C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supply Voltage Range		6		20	6		20	6		20	V
Supply Current			15	20		15	20		15	20	mA
Voltage Gain											
(Pin 5-3)	1 kHz Pins 6 and 2 Connected	24.5	25.5	26.5	24.5	25.5	26.5	24	25.5	27	dB
(Pin 5-6)	1 kHz Pin 6 Open		14.7			14.7			14.7		dB
(Pin 3-7)	1 kHz (Noise Reduction Out)	− 0.5	0	0.5	− 0.5	0	0.5	− 1	0	1	dB
Distortion	1 kHz, 0 dB		0.03	0.1		0.03	0.1		0.03	0.1	%
	10 kHz, + 10 dB		0.2	0.3		0.2	0.3		0.2	0.3	%
Signal Handling	1 kHz, 0.3% Distortion										
	$V_S = 6V$		8.5			8.5			8.5		dB
	$V_S = 12V$	13	15.5		13	15.5		13	15.5		dB
	$V_S = 18V$		19			19			19		dB
Signal/Noise Ratio at Pin 7	Pins 6 and 2 Connected										
Encode Mode (CCIR/ARM)											
NR In	$R_S = 10k$	71.5	74		71	74		70	74		dB
	$R_S = 1k$		77			77			77		dB
NR Out	$R_S = 10k$		83			83			83		dB
Decode Mode (CCIR/ARM)	$R_S = 10k$		83			83			83		dB
Encode Characteristics	Input to Pin 5										
	10 kHz, 0 dB	0	0.5	1.0	− 0.2	0.5	1.2	− 0.5	0.5	1.5	dB
	1.3 kHz, − 20 dB	− 16.2	− 15.7	− 15.2	− 16.7	− 15.7	− 14.7	− 17.2	− 15.7	− 14.2	dB
	5 kHz, − 20 dB	− 17.3	− 16.8	− 16.3	− 17.8	− 16.8	− 15.8	− 18.3	− 16.8	− 15.3	dB
	3 kHz, − 30 dB	− 21.7	− 21.2	− 20.7	− 22.2	− 21.2	− 20.2	− 22.7	− 21.2	− 19.7	dB
	5 kHz, − 30 dB	− 22.3	− 21.8	− 21.3	− 22.8	− 21.8	− 20.8	− 23.3	− 21.8	− 20.3	dB
	10 kHz, − 30 dB	− 24.0	− 23.5	− 23.0	− 24.5	− 23.5	− 22.5	− 25.0	− 23.5	− 22.0	dB
	10 kHz, − 40 dB	− 30.1	− 29.6	− 29.1	− 30.3	− 29.6	− 28.9	− 30.6	− 29.6	− 28.6	dB
Input Resistance	Pin 5	50	65	80	50	65	80	50	65	80	kΩ
	Pin 2	4.3	5.6	6.9	4.3	5.6	6.9	4.3	5.6	6.9	kΩ
Output Resistance	Pin 6	1.8	2.4	3.0	1.8	2.4	3.0	1.8	2.4	3.0	kΩ
	Pin 3		30	45		30	45		30	45	Ω
	Pin 7		30	45		30	45		30	45	Ω
PSRR	f = 120 Hz		40			40			40		dB
Load Impedance											
Pin 3		5			5			5			kΩ
Pin 7		5			5			5			kΩ

Typical Performance Characteristics

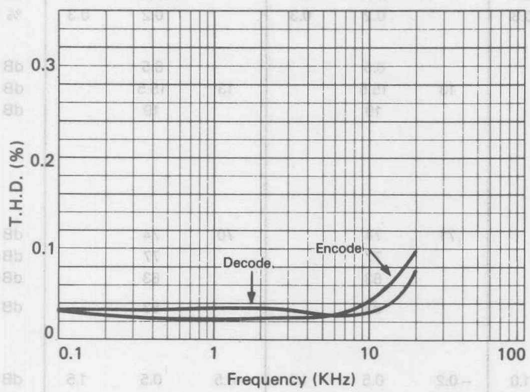
Signal/Noise Ratio vs Source Impedance Encode Mode (CCIR/ARM)



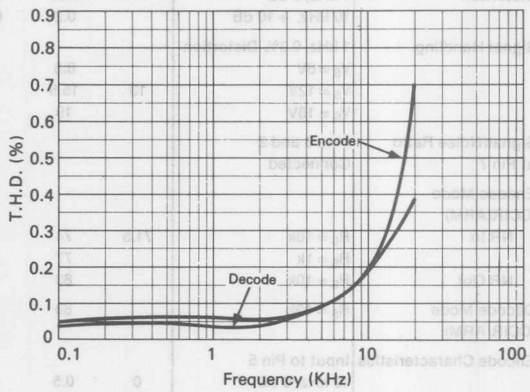
Gain vs Frequency (NR OFF)



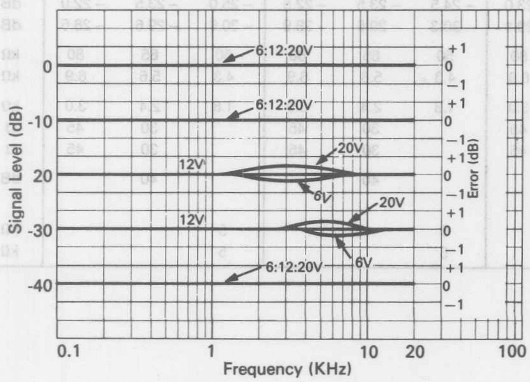
Total Harmonic Distortion—0 dB Level



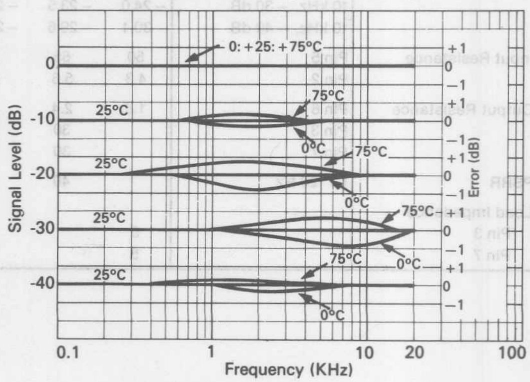
Total Harmonic Distortion— +10 dB Level



Back to Back Response Error vs Frequency and Supply Voltage (Standard Dolby Encoder)

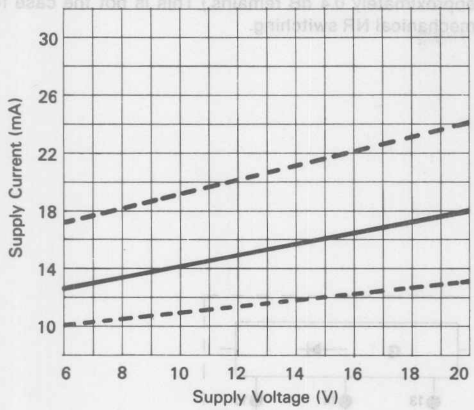


Back to Back Response vs Frequency and Temperature (Encoder Temperature 25°C)

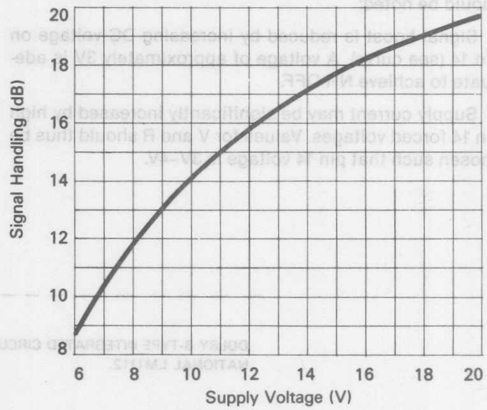


Typical Performance Characteristics (Continued)

Supply Current vs Supply Voltage

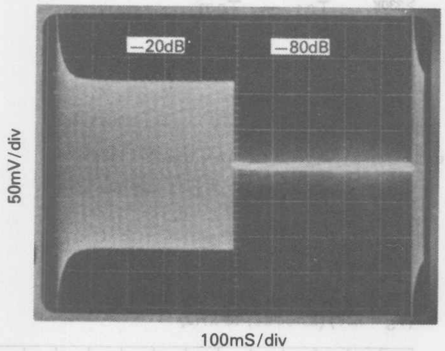


Signal Handling vs Supply Voltage

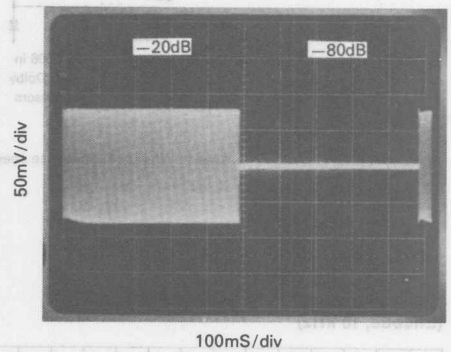


TRANSIENT RESPONSE TO ABRUPT LEVEL CHANGE (Measured at P7)

(a) Encode (f = 5 kHz)

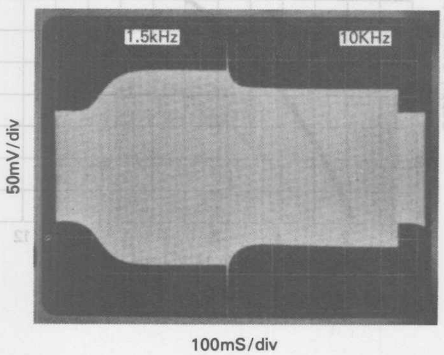


(b) Encoded and Decoded (f = 5 kHz)

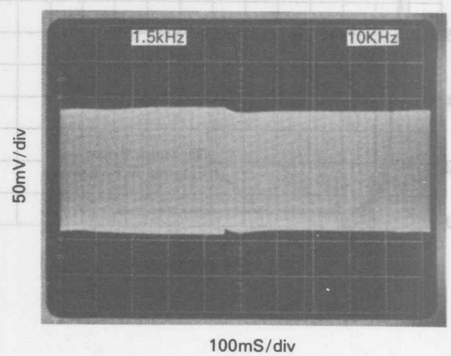


TRANSIENT RESPONSE TO ABRUPT FREQUENCY CHANGE (Measured at P7)

(a) Encode (− 20 dB)



(b) Encoded and Decoded (− 20 dB)

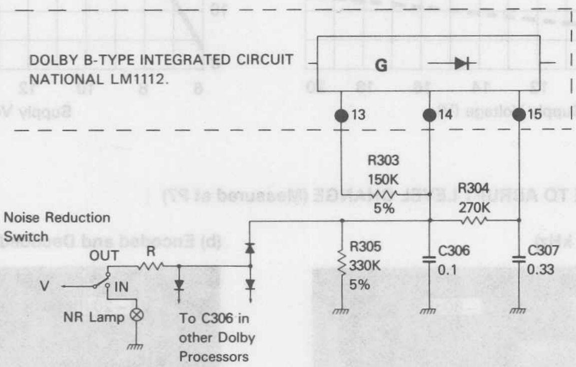


should be noted:

1. Signal boost is reduced by increasing DC voltage on Pin 14 (see curve). A voltage of approximately 3V is adequate to achieve NR OFF.

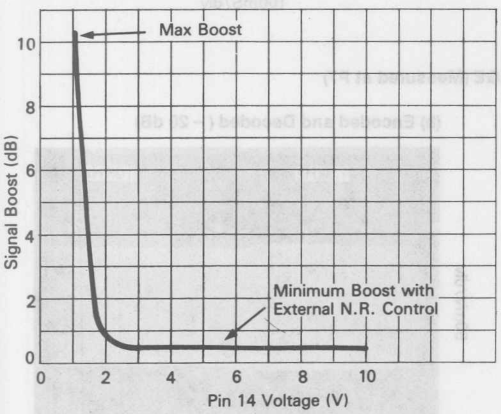
2. Supply current may be significantly increased by high pin 14 forced voltages. Values for V and R should thus be chosen such that pin 14 voltage is 3V–4V.

approximately 0.4 dB remains.) This is not the case for mechanical NR switching.

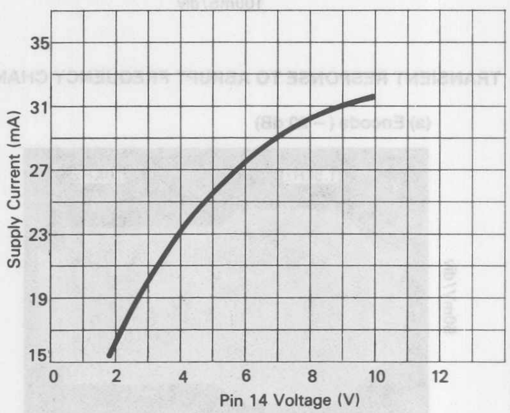


Note 1: Where not otherwise specified, component tolerances are ±10%.

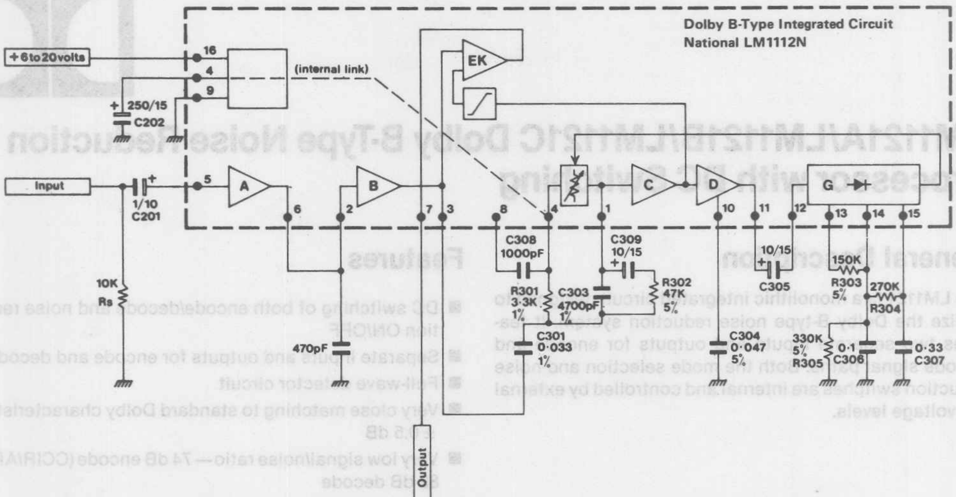
Signal Boost vs Pin 14 Control Voltage (Encode, 10 kHz)



Supply Current vs Pin 14 Control Voltage ($V_S = 12V$) (Encode, 10 kHz)



Test Circuit (Encode)



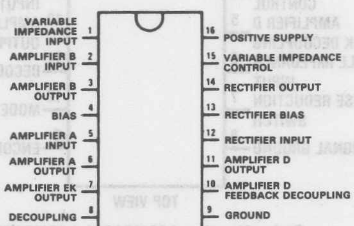
Note 1: 1 nF capacitors from pin 3 and pin 7 to ground may be required on older devices.

Note 2: Where not otherwise specified, component tolerances are ± 10%.

Note 3: For LM1112AN use 2% components for C304, R303, R305. (5% components may cause errors up to ± 0.3 dB.)

Connection Diagram

Dual-In-Line Package



Order Number LM1112AN, LM1112BN or LM1112CN
See NS Package N16E

National Semiconductor

Audio/Radio Circuits
PRELIMINARY

LM1121A/LM1121B/LM1121C Dolby B-Type Noise Reduction Processor with DC Switching

General Description

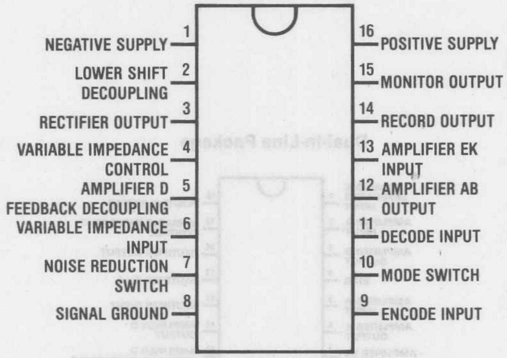
The LM1121 is a monolithic integrated circuit designed to realize the Dolby B-type noise reduction system. It features two separate inputs and outputs for encode and decode signal paths. Both the mode selection and noise reduction switches are internal and controlled by external DC voltage levels.

Features

- DC switching of both encode/decode and noise reduction ON/OFF
- Separate inputs and outputs for encode and decode
- Full-wave detector circuit
- Very close matching to standard Dolby characteristics, ±0.5 dB
- Very low signal/noise ratio—74 dB encode (CCIR/ARM), 82 dB decode
- Very high signal handling capability, >20 dB (V_S = 20V) for operation with metal tape

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number LM1121AN, LM1121BN, or LM1121CN
See NS Package N16E

Switching Truth Tables

Pin 10	Mode
High	Encode
Open	Decode
Low	Decode

Pin 7	Noise Reduction
High	Off
Open	On
Low	On

Switching level = 1.6V (wrt negative supply)

Available to licensees of Dolby Laboratories Licensing Corporation, San Francisco, CA, from whom licensing and applications information must be obtained.

Dolby and the double-D symbol are trademarks of Dolby Laboratories Inc.

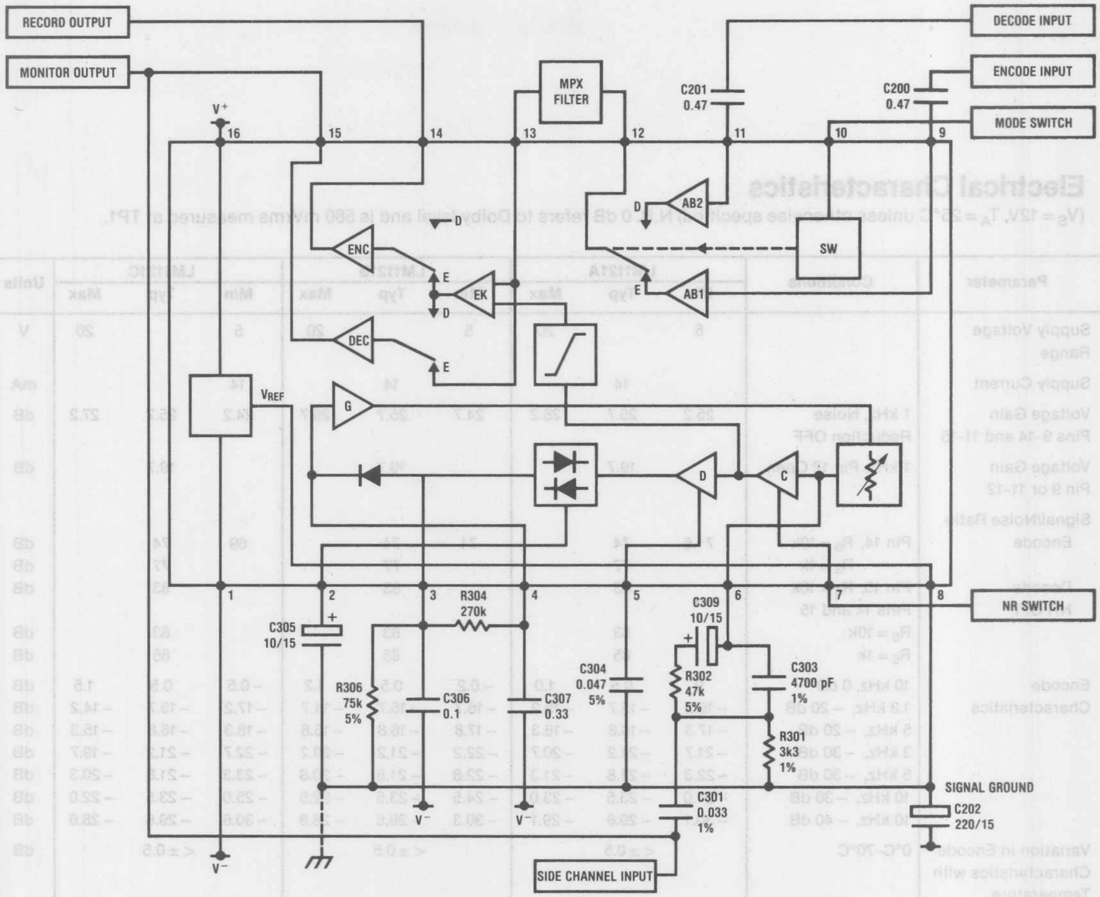
Absolute Maximum Ratings

Supply Voltage	24V
Operating Temperature Range	−20°C to +70°C
Storage Temperature Range	−60°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

($V_S = 12V$, $T_A = 25°C$ unless otherwise specified) N.B. 0 dB refers to Dolby level and is 580 mVrms measured at TP1.

Parameter	Conditions	LM1121A			LM1121B			LM1121C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supply Voltage Range		5		20	5		20	5		20	V
Supply Current			14			14		14			mA
Voltage Gain Pins 9–14 and 11–15	1 kHz, Noise Reduction OFF	25.2	25.7	26.2	24.7	25.7	26.7	24.2	25.7	27.2	dB
Voltage Gain Pin 9 or 11–12	1 kHz, Pin 12 Open		19.7			19.7			19.7		dB
Signal/Noise Ratio											
Encode	Pin 14, $R_S = 10k$	71.5	74		71	74		69	74		dB
	$R_S = 1k$		77			77			77		dB
Decode	Pin 15, $R_S = 10k$		83			83			83		dB
NR OFF	Pins 14 and 15										
	$R_S = 10k$		83			83			83		dB
	$R_S = 1k$		85			85			85		dB
Encode Characteristics	10 kHz, 0 dB	0	0.5	1.0	−0.2	0.5	1.2	−0.5	0.5	1.5	dB
	1.3 kHz, −20 dB	−16.2	−15.7	−15.2	−16.7	−15.7	−14.7	−17.2	−15.7	−14.2	dB
	5 kHz, −20 dB	−17.3	−16.8	−16.3	−17.8	−16.8	−15.8	−18.3	−16.8	−15.3	dB
	3 kHz, −30 dB	−21.7	−21.2	−20.7	−22.2	−21.2	−20.2	−22.7	−21.2	−19.7	dB
	5 kHz, −30 dB	−22.3	−21.8	−21.3	−22.8	−21.8	−20.8	−23.3	−21.8	−20.3	dB
	10 kHz, −30 dB	−24.0	−23.5	−23.0	−24.5	−23.5	−22.5	−25.0	−23.5	−22.0	dB
	10 kHz, −40 dB	−30.1	−29.6	−29.1	−30.3	−29.6	−28.9	−30.6	−29.6	−28.6	dB
Variation in Encode Characteristics with Temperature	0°C–70°C		< ±0.5			< ±0.5			< ±0.5		dB
Distortion	1 kHz, 0 dB		0.03	0.1		0.03	0.1		0.03	0.2	%
	10 kHz, 10 dB		0.2	0.3		0.2	0.5		0.2	0.7	%
Signal Handling	1 kHz, Dist = 0.3%										
	$V_S = 5V$		6.5			6.5			6.5		
	$V_S = 7V$		10.5			10.5			10.5		dB
	$V_S = 12V$	14.0	16.0		14.0	16.0		14.0	16.0		dB
	$V_S = 20V$		21.0			21.0			21.0		dB
Switching Transients Measured at Pin 14 or 15											
Encode/Decode/Encode			20			20			20		mV
NR OFF/ON/OFF			20			20			20		mV
Input Resistance	Pins 9 and 11	50	65	80	50	65	80	50	65	80	kΩ
	Pin 13	4.3	5.6	6.9	4.3	5.6	6.9	4.3	5.6	6.9	kΩ
Output Resistance	Pin 12	1.8	2.4	3.0	1.8	2.4	3.0	1.8	2.4	3.0	kΩ
	Pins 14 and 15		30	55		30	55		30	55	Ω


RECORD OUTPUT
MONITOR OUTPUT
DECODE INPUT
ENCODE INPUT
MODE SWITCH
NR SWITCH
SIGNAL GROUND
SIDE CHANNEL INPUT
MPX FILTER
C201 0.47
C200 0.47
V+
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
ENC
DEC
EK
G
AB2
AB1
SW
D
E
C
VREF
C305 10/15
R306 75k 5%
C306 0.1
R304 270k
C307 0.33
C304 0.047 5%
C309 10/15
R302 47k 5%
C303 4700 pF 1%
R301 3k3 1%
C301 0.033 1%
C202 220/15
V−

National Semiconductor

Audio/Radio Circuits
PRELIMINARY

LM1131A/LM1131B/LM1131C Dual Dolby B-Type Noise Reduction Processor

General Description

The LM1131 is a monolithic integrated circuit specifically designed to realize the Dolby B-type noise reduction system.

The circuit includes two completely separate noise reduction processors and will operate in both encode and decode modes. It is ideal for stereo applications in compact equipment or for mono applications in 3-head equipment where two processors with very closely matched internal gains are required.

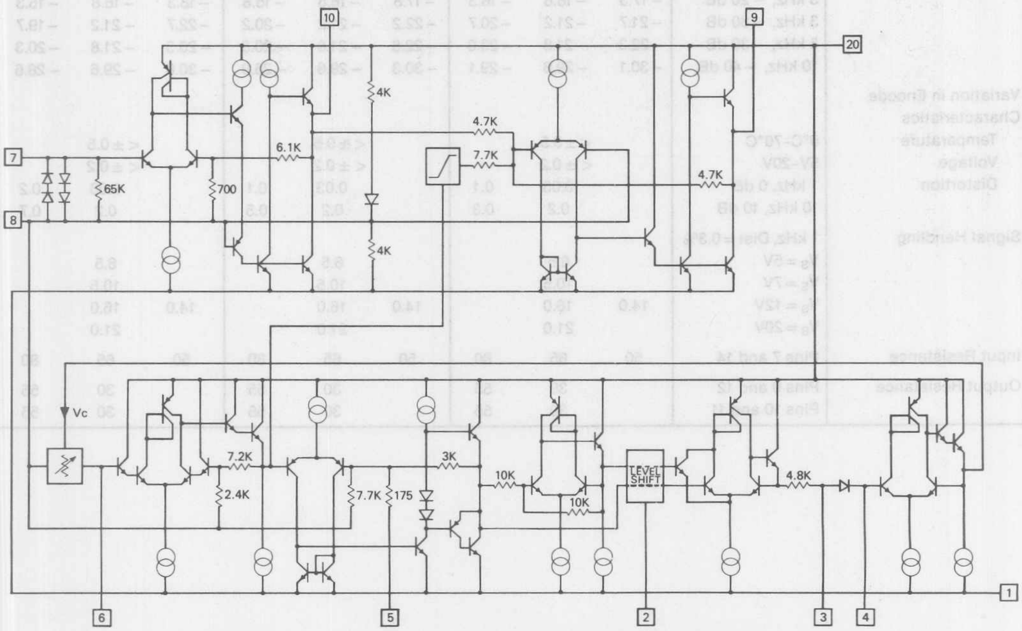
Features

- Stereo Dolby noise reduction with one IC
- Wide supply voltage range, 5V–20V
- Very high signal/noise ratio, 79 dB encode, 90 dB decode (CCIR/ARM)
- Very close gain matching for 3-head recorders
- Close matching to standard Dolby characteristics
- Very low temperature drift of Dolby characteristics
- High signal handling capability, > +20 dB (V_S = 20V)
- Full-wave rectifier in both channels
- Operates with both single and split supply voltages
- Excellent transient response characteristics
- Minimal input switch-on transients
- Reduced number of external components per channel
- Improved input protection

Available to licensees of Dolby Laboratories Licensing Corporation, San Francisco, from whom licensing and application information must be obtained.

Dolby and the double-D symbol are trademarks of Dolby Laboratories Licensing Corporation.

Schematic Diagram (1 channel shown only)



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Absolute Maximum Ratings

Supply Voltage	24V
Operating Temperature Range	−20°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	to 300°C

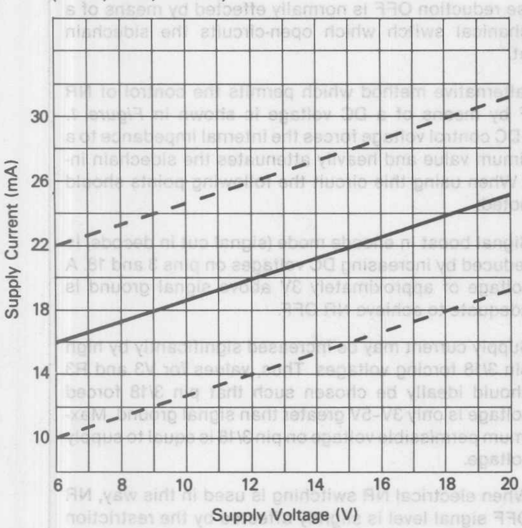
Electrical Characteristics

$V_S = 12V$, $T_A = 25°C$ unless otherwise specified. N.B. 0 dB refers to Dolby level and is 580 mV, measured at TP1 and TP2.

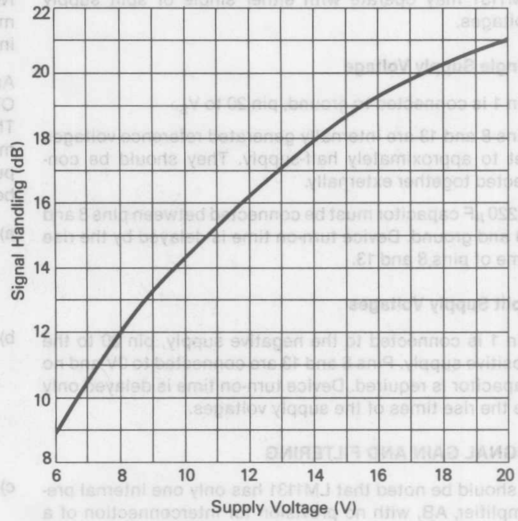
Parameter	Conditions	LM1131A			LM1131B			LM1131C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supply Voltage Range		5		20	5		20	5		20	V
Supply Current			20			20		20			mA
Voltage Gain											
(Pins 7-10 and 14-11)	1 kHz Decode	19.2	19.7	20.2	18.7	19.7	20.7	18.2	19.7	21.2	dB
(Pins 10-9 and 11-12)	1 kHz Decode	−0.5	0	0.5	−0.5	0	0.5	−1.0	0	1.0	dB
Difference in Voltage Gain Between Channels	1 kHz Noise Reduction OFF	−0.2	0	0.2	−0.5	0	0.5	−1.0	0	1.0	dB
Crosstalk Between Channels	1 kHz, 0 dB	−60	−90		−60	−90		−60	−90		dB
Signal/Noise Ratio at Pins 9 and 12											
Encode	$R_S = 10k\Omega$	77	79		75.5	79		74	79		dB
	$R_S = 1k\Omega$		82			82			82		dB
Decode	$R_S = 10k$		90			90			90		dB
	$R_S = 1k$		92			92			92		dB
Encode Characteristics	10 kHz, 0 dB	0	0.5	1.0	0.2	0.5	1.2	−0.5	0.5	1.5	dB
	1.3 kHz, −20 dB	−16.2	−15.7	−15.2	−16.7	−15.7	−14.7	−17.2	−15.7	−14.2	dB
	5 kHz, −20 dB	−17.3	−16.8	−16.3	−17.8	−16.8	−15.8	−18.3	−16.8	−15.3	dB
	3 kHz, −30 dB	−21.7	−21.2	−20.7	−22.2	−21.2	−20.2	−22.7	−21.2	−19.7	dB
	5 kHz, −30 dB	−22.3	−21.8	−23.0	−22.8	−21.8	−20.8	−23.3	−21.8	−20.3	dB
	10 kHz, −40 dB	−30.1	−29.6	−29.1	−30.3	−29.6	−28.9	−30.6	−29.6	−28.6	dB
Variation in Encode Characteristics											
Temperature	0°C–70°C		< ±0.5			< ±0.5			< ±0.5		dB
Voltage	5V–20V		< ±0.2			< ±0.2			< ±0.2		dB
Distortion	1 kHz, 0 dB		0.03	0.1		0.03	0.1		0.03	0.2	%
	10 kHz, 10 dB		0.2	0.3		0.2	0.5		0.2	0.7	%
Signal Handling	1 kHz, Dist = 0.3%										
	$V_S = 5V$		6.5			6.5			6.5		dB
	$V_S = 7V$		10.5			10.5			10.5		dB
	$V_S = 12V$	14.0	16.0		14.0	16.0		14.0	16.0		dB
	$V_S = 20V$		21.0			21.0			21.0		dB
Input Resistance	Pins 7 and 14	50	65	80	50	65	80	50	65	80	kΩ
Output Resistance	Pins 9 and 12		30	55		30	55		30	55	Ω
	Pins 10 and 11		30	55		30	55		30	55	Ω

Typical Performance Characteristics

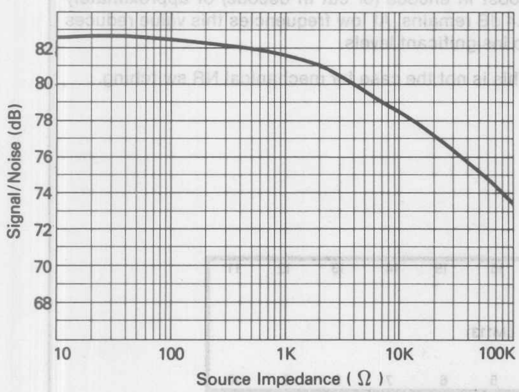
Supply Current vs Supply Voltage (1 kHz, 0 dB; NR ON)



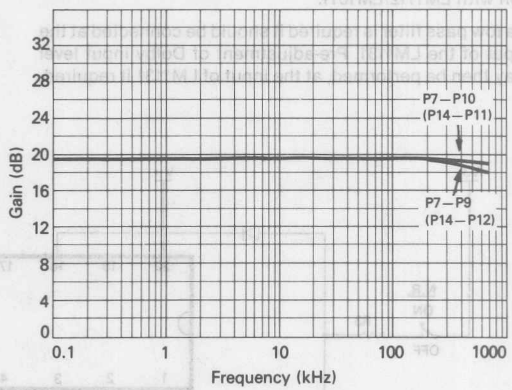
Signal Handling vs Supply Voltage



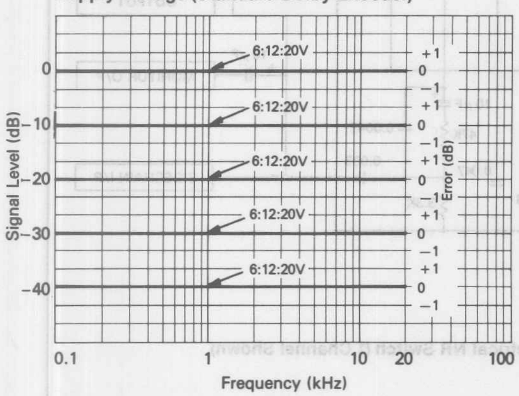
Signal to Noise Ratio vs Source Impedance Encode Mode (CCIR/ARM)



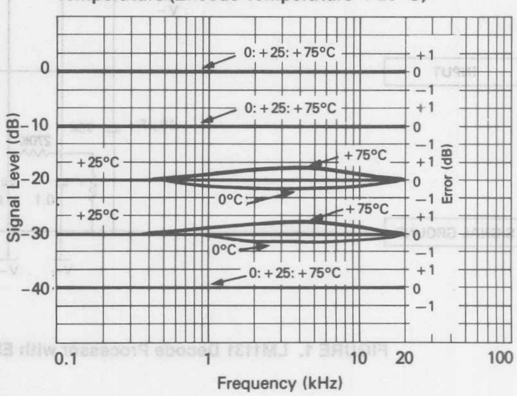
Gain vs Frequency (NR OFF)



Back to Back Response Error vs Frequency and Supply Voltage (Standard Dolby Encoder)



Back to Back Response Error vs Frequency and Temperature (Encode Temperature +25°C)



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Application Notes

SUPPLY VOLTAGE

LM1131 may operate with either single or split supply voltages.

Single Supply Voltage

Pin 1 is connected to ground, pin 20 to V_S.

Pins 8 and 13 are internally generated reference voltages set to approximately half-supply. They should be connected together externally.

A 220 μF capacitor must be connected between pins 8 and 13 and ground. Device turn-on time is delayed by the rise time of pins 8 and 13.

Split Supply Voltages

Pin 1 is connected to the negative supply, pin 20 to the positive supply. Pins 8 and 13 are connected to 0V and no capacitor is required. Device turn-on time is delayed only be the rise times of the supply voltages.

SIGNAL GAIN AND FILTERING

It should be noted that LM1131 has only one internal preamplifier, AB, with no provision for interconnection of a low pass filter to remove bias or multiplex tones. In addition, main chain gain has been reduced by 6 dB in comparison with LM1112/LM1011.

If a low pass filter is required it should be connected at the input of the LM1131. Pre-adjustment of Dolby input level may then be performed, at the input of LM1131 if required.

NOISE REDUCTION SWITCH

Noise reduction OFF is normally effected by means of a mechanical switch which open-circuits the sidechain input.

An alternative method which permits the control of NR OFF by means of a DC voltage is shown in *Figure 1.* The DC control voltage forces the internal impedance to a minimum value and heavily attenuates the sidechain input. When using this circuit the following points should be noted:

a) Signal boost in encode mode (signal cut in decode) is reduced by increasing DC voltages on pins 3 and 18. A voltage of approximately 3V above signal ground is adequate to achieve NR OFF.

b) Supply current may be increased significantly by high pin 3/18 forcing voltages. Thus, values for V3 and R3 should ideally be chosen such that pin 3/18 forced voltage is only 3V–5V greater than signal ground. Maximum permissible voltage on pin 3/18 is equal to supply voltage.

c) When electrical NR switching is used in this way, NR OFF signal level is slightly affected by the restriction that the internal variable impedance cannot achieve zero impedance. Thus, at 10 kHz – 10 dB, a residual boost in encode (or cut in decode) of approximately 0.4 dB remains. At low frequencies this value reduces to insignificant levels.

   This is not the case for mechanical NR switching.

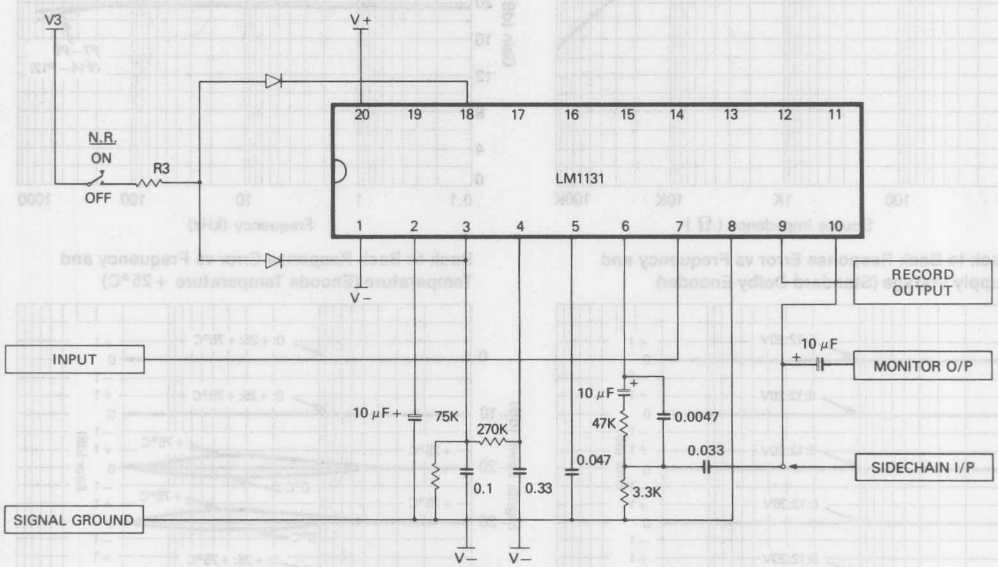
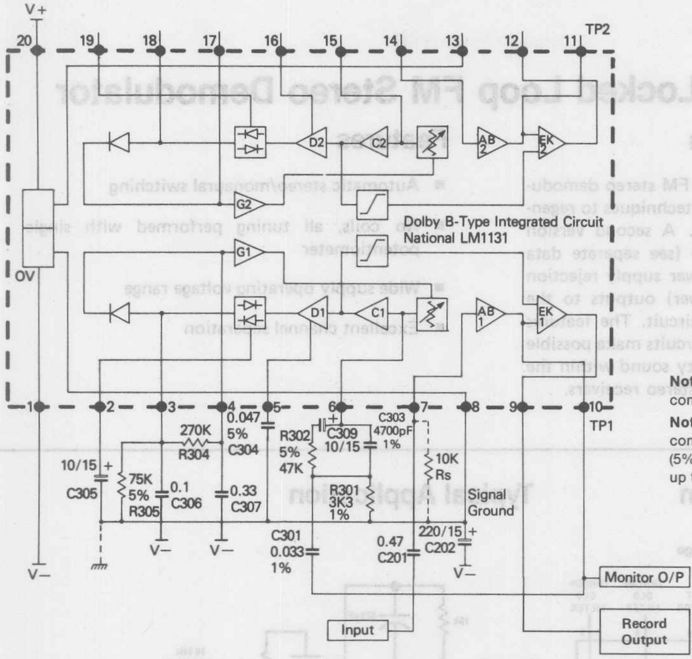


FIGURE 1. LM1131 Decode Processor with Electrical NR Switch (1 Channel Shown)

Test Circuit Encode Mode (components shown for channel 1 only)

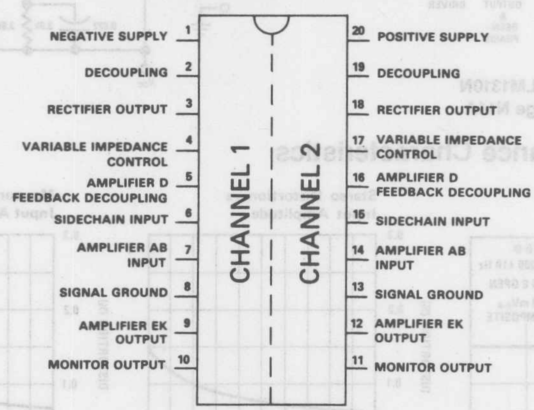


Note 1: Where not otherwise specified component tolerances are ±10%.

Note 2: For LM1131AN use 2% components for C304, R303, R305. (5% components may cause errors up to ±0.3 dB).

Connection Diagram

Dual-In-Line Package



Order Number LM1131AN, LM1131BN or LM1131CN
See NS Package N20A

LM1310 Phase-Locked Loop FM Stereo Demodulator

General Description

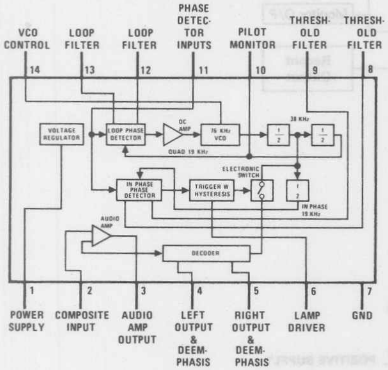
The LM1310 is an integrated FM stereo demodulator using phase locked loop techniques to regenerate the 38 kHz subcarrier. A second version also available is the LM1800 (see separate data sheet) which adds superb power supply rejection and buffered (emitter follower) outputs to the basic phase locked decoder circuit. The features available in these integrated circuits make possible a system delivering high fidelity sound within the cost restraints of inexpensive stereo receivers.

Features

- Automatic stereo/monaural switching
- No coils, all tuning performed with single potentiometer
- Wide supply operating voltage range
- Excellent channel separation

Connection Diagram

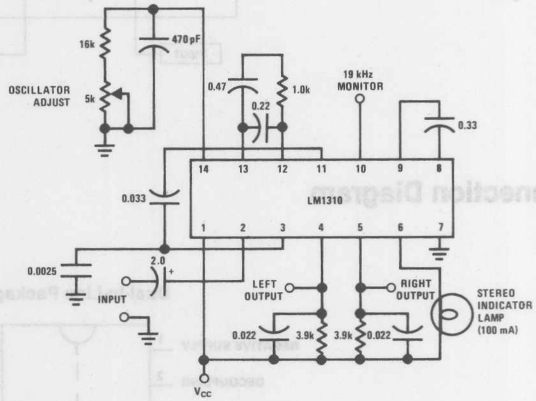
Dual-In-Line Package



TOP VIEW

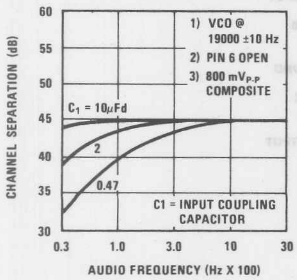
Order Number LM1310N
See NS Package N14A

Typical Application

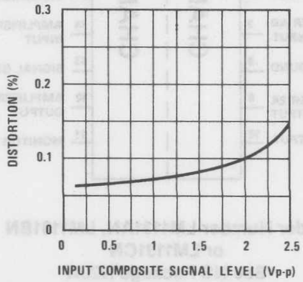


Typical Performance Characteristics

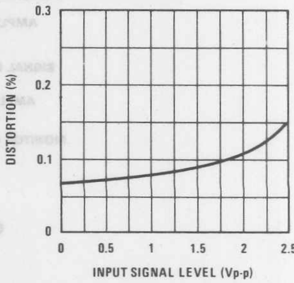
Channel Separation



Stereo Distortion vs Input Amplitude



Monaural Distortion vs Input Amplitude



Absolute Maximum Ratings

Supply Voltage	18V
Power Dissipation (Note 2)	715 mW
Operating Temperature Range	0°C to +70°C
Operating Supply Voltage Range	10V to 18V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 1)

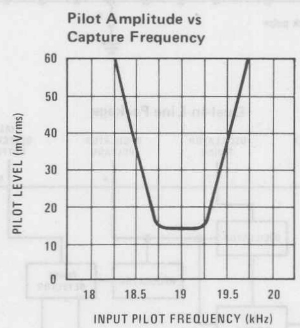
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	Lamp "OFF"		18		mA
Lamp Driver Saturation	100 mA Lamp Current		1.3		V
Lamp Driver Leakage			1.0		nA
Pilot Level for Lamp "ON"	Pin 11 Adjusted to 19.00 kHz		15	20	mVrms
Pilot Level for Lamp "OFF"	Pin 11 Adjusted to 19.00 kHz	3.0	7.0		mVrms
Composite Input	Maximum for THD < 0.5%	2.8			Vp-p
Monaural Input	Maximum for THD < 1.0%	2.8			Vp-p
Stereo Channel Separation		30	40		dB
	2.0Vp-p Composite with 10% Pilot		45		dB
Monaural Channel Unbalance	Pilot "OFF"		0.3	1.5	dB
Recovered Audio			485		mVrms
Total Harmonic Distortion			0.3		%
Total Harmonic Distortion	2.0 Vp-p Composite with 10% Pilot		0.15		%
Capture Range	50 mVrms of Pilot		±3.5		% of f_o
Ultrasonic Frequency Rejection	19 kHz		35		dB
	38 kHz		45		dB
Dynamic Input Resistance		20	50		kΩ
SCA Rejection	f = 67 kHz; Measure 9 kHz Beat Note with 1 kHz Modulation "OFF"		75		dB

Note 1: Unless otherwise noted: V_{CC} = +12 V_{DC} and T_A = +25°C. The input signal is a 2.8 Vp-p standard multiplex composite signal using 10% Pilot and with L or R-channel only modulated at 1.0 kHz.

Note 2: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a themal resistance of 175°C/W junction to ambient.

Note 3: The VCO can be defeated (sometimes desirable when using an AM-FM receiver in the AM mode) by returning pin 14 to ground through a 2.2 kΩ resistor.

Typical Performance Characteristics (Continued)



National Semiconductor

LM1391 Phase-Locked Loop Block

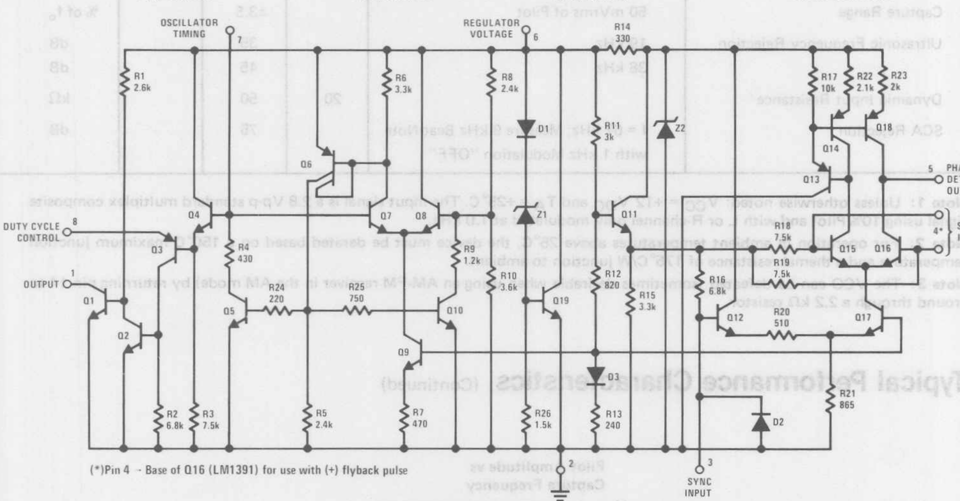
General Description

The LM1391 integrated circuit has been designed primarily for use in the horizontal section of TV receivers, but may find use in other low frequency signal processing applications. It includes a stable VCO, linear pulse phase detector, and variable duty cycle output driver.

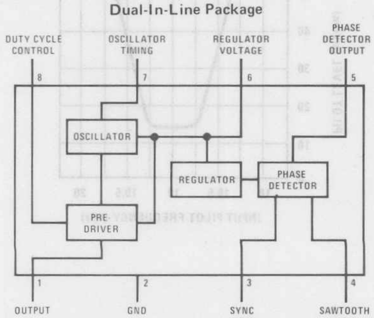
Features

- Internal active regulator for improved supply rejection
- Uncommitted collector of output transistor
- Output transistor with low saturation and high voltage swing
- APC of the oscillator with a synchronizing signal
- DC controlled output duty cycle
- ±300 Hz typical pull-in
- Linear balanced phase detector
- Low thermal frequency drift
- Small static phase error
- Adjustable dc loop gain

Schematic and Connection Diagrams



(*)Pin 4 – Base of Q16 (LM1391) for use with (+) flyback pulse



TOP VIEW

Order Number LM1391N
See NS Package N08B

Absolute Maximum Ratings

Supply Current	40 mA_{DC}
Output Voltage	40 V_{DC}
Output Current	30 mA_{DC}
Sync Input Voltage (Pin 3)	5.0 Vp-p
Flyback Input Voltage (Pin 4)	5.0 Vp-p
Power Dissipation (Package Limitation)	
Plastic Package (Note 1)	1250 mW
Operating Temperature Range (Ambient)	0°C to +75°C
Storage Temperature Range	−65°C to +150°C

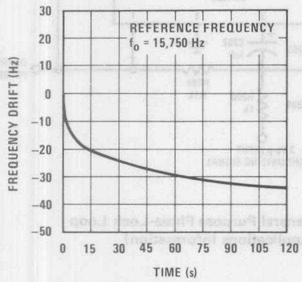
Electrical Characteristics $T_A = 25°C$ (see test circuit, all switches in position 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Regulated Voltage (Pin 6)	$I_6 = 22\ mA_{DC}$	8.0	8.6	9.2	V_{DC}
Supply Current (Pin 6)			20		mA_{DC}
Collector-Emitter Saturation Voltage of Output Transistor (Pin 1)	$I_{C1} = 20\ mA$		0.30	0.40	V_{DC}
Pin 4 Voltage			2.0		V_{DC}
Oscillator Pull-in Range	Adjust R_H		±300		Hz
Oscillator Hold-in Range	Adjust R_H		±900		Hz
Static Phase Error	$\Delta f = 300$ Hz		0.5		μs
Free-running Frequency Supply Dependance	S1 in position 2		±3.0		Hz/V_{DC}
Phase Detector Leakage (Pin 5)	All switches in position 2			±1.0	μA
Sync Input Voltage (Pin 3)		2.0		5.0	Vp-p
Sawtooth Input Voltage (Pin 4)		1.0		3.0	Vp-p
Maximum Oscillator Frequency			500		kHz

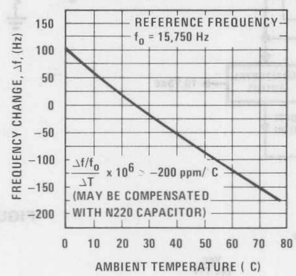
Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 100°C/W junction to ambient.

Typical Performance Characteristics

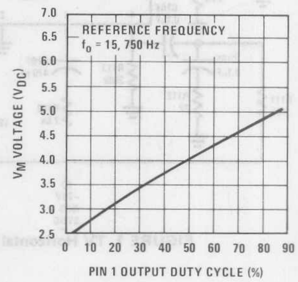
Frequency Drift vs Warm-Up Time



Frequency vs Temperature



Output Duty Cycle vs V_M Voltage



Application Information

The following equations may be considered when using the LM1391 in a particular application.

$$R201 = R301 = \frac{V_{CC} - 8.6}{0.02}\ \Omega$$

$$f_o \cong \frac{1}{0.6\ R_oC_o}\ \text{Hz} \quad 1.5k \le R_o < 51k$$

$$R204 \cong 10\ R_o$$

$$C203 = C204 \cong \frac{1}{600\ f_o(\text{Hz})}\ \text{F}$$

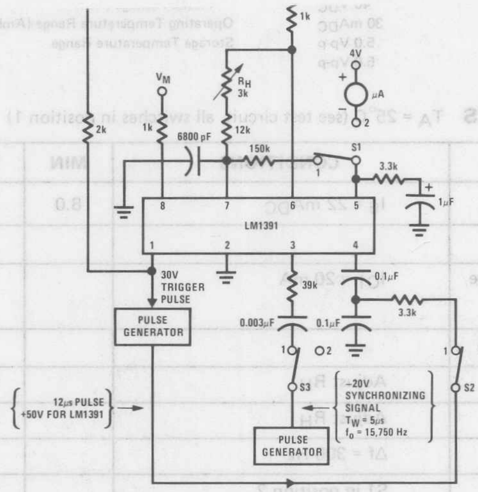
DC Loop Gain $\mu\beta \cong 3.2 \times 10^{-5}\ R_of_o$ Hz/rad

Noise Bandwidth

$$f_{nn} \cong \frac{1 + 2\pi \frac{R_X^2}{R_Y} C_c\,\mu\beta}{4R_XC_c}\ \text{Hz}$$

Damping Factor

$$K \cong \frac{\pi}{2}\,\frac{R_X^2}{R_Y}\,C_c\,\mu\beta$$



Typical Applications

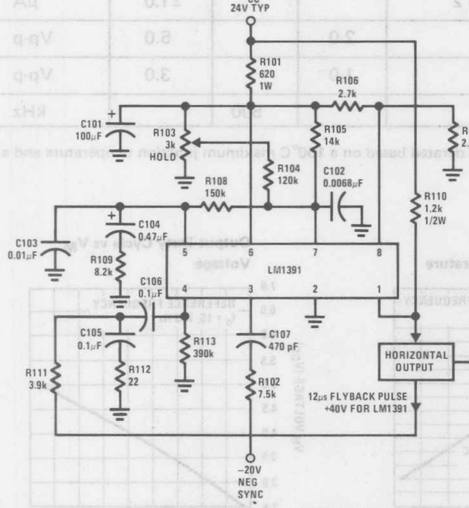


FIGURE 1. TV Horizontal Processor

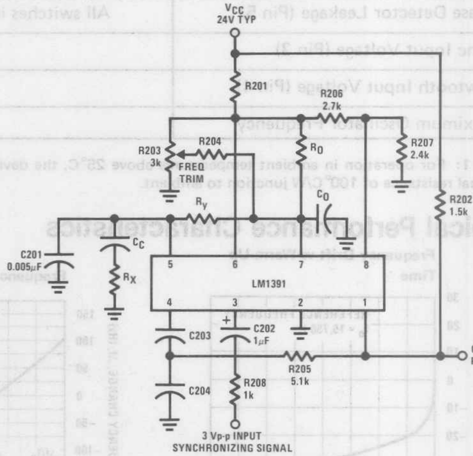


FIGURE 2. General Purpose Phase-Lock Loop
(See Applications Information)

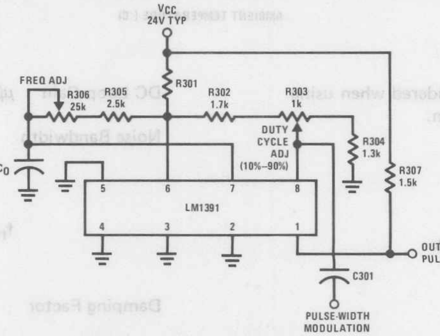


FIGURE 3. Variable Duty Cycle Oscillator
(See Applications Information)

National Semiconductor

Audio/Radio Circuits

LM1596/LM1496 Balanced Modulator-Demodulator

General Description

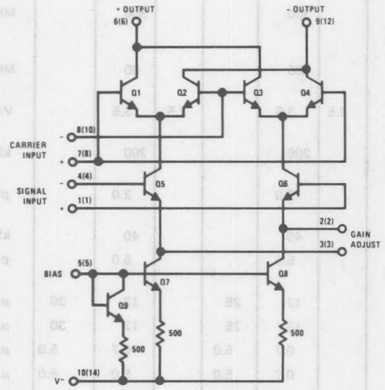
The LM1596/LM1496 are double balanced modulator-demodulators which produce an output voltage proportional to the product of an input (signal) voltage and a switching (carrier) signal. Typical applications include suppressed carrier modulation, amplitude modulation, synchronous detection, FM or PM detection, broadband frequency doubling and chopping.

The LM1596 is specified for operation over the −55°C to +125°C military temperature range. The LM1496 is specified for operation over the 0°C to +70°C temperature range.

Features

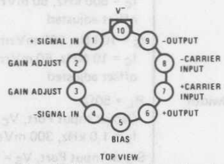
- Excellent carrier suppression
  65 dB typical at 0.5 MHz
  50 dB typical at 10 MHz
- Adjustable gain and signal handling
- Fully balanced inputs and outputs
- Low offset and drift
- Wide frequency response up to 100 MHz

Schematic and Connection Diagrams



Numbers in parentheses show DIP connections.

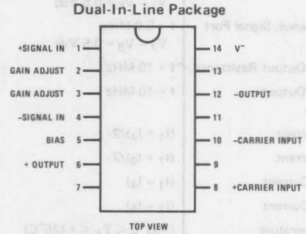
Metal Can Package



Note: Pin 10 is connected electrically to the case through the device substrate.

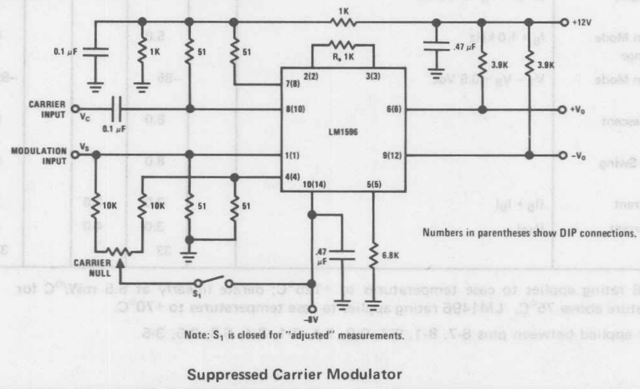
Order Number LM1496H or LM1596H
See NS Package H08C

Dual-In-Line Package



Order Number LM1496N
See NS Package N14A

Typical Application and Test Circuit



Numbers in parentheses show DIP connections.

Note: S_1 is closed for "adjusted" measurements.

Suppressed Carrier Modulator

Absolute Maximum Ratings

Internal Power Dissipation (Note 1)	500 mW
Applied Voltage (Note 2)	30V
Differential Input Signal ($V_7 - V_8$)	±5.0V
Differential Input Signal ($V_4 - V_1$)	$\pm(5+I_5R_e)$ V
Input Signal ($V_2 - V_1$, $V_3 - V_4$)	5.0V
Bias Current (I_5)	12 mA
Operating Temperature Range LM1596	−55°C to +125°C
LM1496	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics (T_A = 25°C, unless otherwise specified, see test circuit)

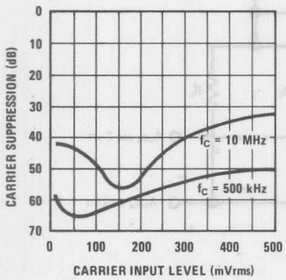
PARAMETER	CONDITIONS	LM1596 MIN	LM1596 TYP	LM1596 MAX	LM1496 MIN	LM1496 TYP	LM1496 MAX	UNITS
Carrier Feedthrough	V_C = 60 mVrms sine wave f_C = 1.0 kHz, offset adjusted		40			40		μVrms
	V_C = 60 mVrms sine wave f_C = 10 MHz, offset adjusted		140			140		μVrms
	V_C = 300 mV_{pp} square wave f_C = 1.0 kHz, offset adjusted		0.04	0.2		0.04	0.2	mVrms
	V_C = 300 mV_{pp} square wave f_C = 1.0 kHz, offset not adjusted		20	100		20	150	mVrms
Carrier Suppression	f_S = 10 kHz, 300 mVrms f_C = 500 kHz, 60 mVrms sine wave offset adjusted	50	65		50	65		dB
	f_S = 10 kHz, 300 mVrms f_C = 10 MHz, 60 mVrms sine wave offset adjusted		50			50		dB
Transadmittance Bandwidth	R_L = 50Ω Carrier Input Port, V_C = 60 mVrms sine wave f_S = 1.0 kHz, 300 mVrms sine wave		300			300		MHz
	Signal Input Port, V_S = 300 mVrms sine wave $V_7 - V_8$ = 0.5Vdc		80			80		MHz
Voltage Gain, Signal Channel	V_S = 100 mVrms, f = 1.0 kHz $V_7 - V_8$ = 0.5Vdc	2.5	3.5		2.5	3.5		V/V
Input Resistance, Signal Port	f = 5.0 MHz $V_7 - V_8$ = 0.5 Vdc		200			200		kΩ
Input Capacitance, Signal Port	f = 5.0 MHz $V_7 - V_8$ = 0.5 Vdc		2.0			2.0		pF
Single Ended Output Resistance	f = 10 MHz		40			40		kΩ
Single Ended Output Capacitance	f = 10 MHz		5.0			5.0		pF
Input Bias Current	$(I_1 + I_4)/2$		12	25		12	30	μA
Input Bias Current	$(I_7 + I_8)/2$		12	25		12	30	μA
Input Offset Current	$(I_1 - I_4)$		0.7	5.0		0.7	5.0	μA
Input Offset Current	$(I_7 - I_8)$		0.7	5.0		5.0	5.0	μA
Average Temperature Coefficient of Input Offset Current	$(-55°C < T_A < +125°C)$ $(0°C < T_A < +70°C$		2.0			2.0		nA/°C nA/°C
Output Offset Current	$(I_6 - I_9)$		14	50		14	60	μA
Average Temperature Coefficient of Output Offset Current	$(-55°C < T_A < +125°C)$ $(0°C < T_A < +70°C)$		90			90		nA/°C nA/°C
Signal Port Common Mode Input Voltage Range	f_S = 1.0 kHz		5.0			5.0		$V_{p\text{-}p}$
Signal Port Common Mode Rejection Ratio	$V_7 - V_8$ = 0.5 Vdc		−85			−85		dB
Common Mode Quiescent Output Voltage			8.0			8.0		Vdc
Differential Output Swing Capability			8.0			8.0		$V_{p\text{-}p}$
Positive Supply Current	$(I_6 + I_9)$		2.0	3.0		2.0	3.0	mA
Negative Supply Current	(I_{10})		3.0	4.0		3.0	4.0	mA
Power Dissipation			33			33		mW

Note 1: LM1596 rating applies to case temperatures to +125°C; derate linearly at 6.5 mW/°C for ambient temperature above 75°C. LM1496 rating applies to case temperatures to +70°C.

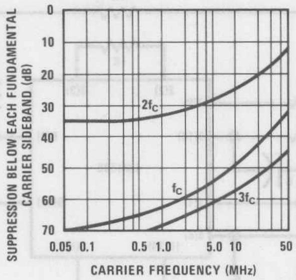
Note 2: Voltage applied between pins 6-7, 8-1, 9-7, 9-8, 7-4, 7-1, 8-4, 6-8, 2-5, 3-5.

Typical Performance Characteristics

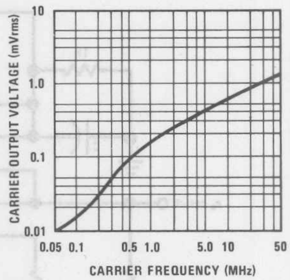
Carrier Suppression vs Carrier Input Level



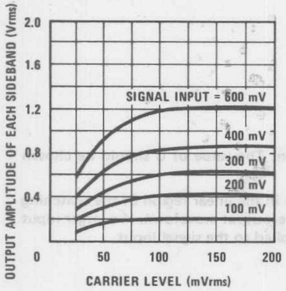
Carrier Suppression vs Frequency



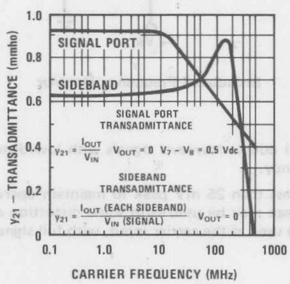
Carrier Feedthrough vs Frequency



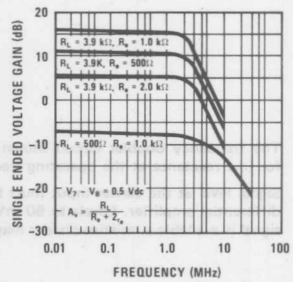
Sideband Output vs Carrier Levels



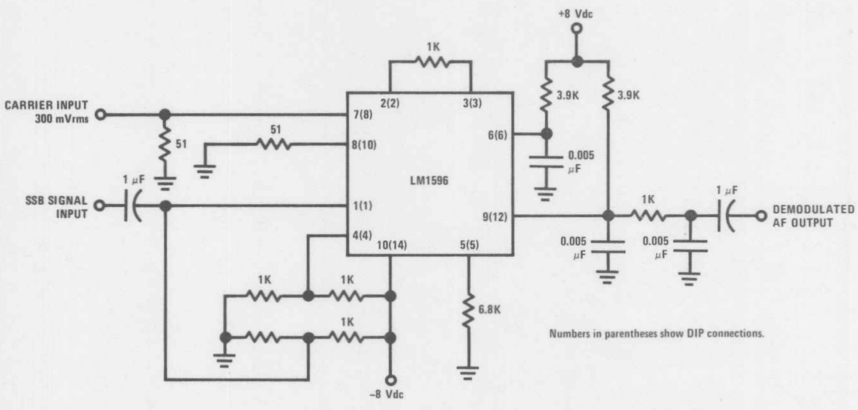
Sideband and Signal Port Transadmittances vs Frequency



Signal-Port Frequency Response

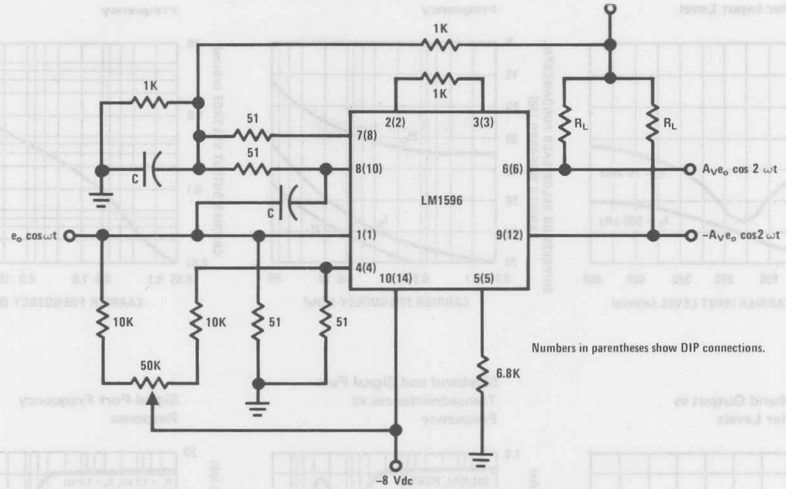


Typical Applications (Continued)



SSB Product Detector

This figure shows the LM1596 used as a single sideband (SSB) suppressed carrier demodulator (product detector). The carrier signal is applied to the carrier input port with sufficient amplitude for switching operation. A carrier input level of 300 mVrms is optimum. The composite SSB signal is applied to the signal input port with an amplitude of 5.0 to 500 mVrms. All output signal components except the desired demodulated audio are filtered out, so that an offset adjustment is not required. This circuit may also be used as an AM detector by applying composite and carrier signals in the same manner as described for product detector operation.



Broadband Frequency Doubler

The frequency doubler circuit shown will double low-level signals with low distortion. The value of C should be chosen for low reactance at the operating frequency.

Signal level at the carrier input must be less than 25 mV peak to maintain operation in the linear region of the switching differential amplifier. Levels to 50 mV peak may be used with some distortion of the output waveform. If a larger input signal is available a resistive divider may be used at the carrier input, with full signal applied to the signal input.

National Semiconductor

LM1800 Phase-Locked Loop FM Stereo Demodulator

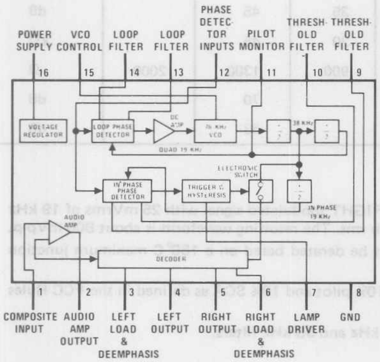
General Description

The LM1800 is a second generation integrated FM stereo demodulator using phase locked loop techniques to regenerate the 38 kHz subcarrier. The numerous features integrated on the die make possible a system delivering high fidelity sound while still meeting the cost requirements of inexpensive stereo receivers. More information available in AN-81.

Features

- Automatic stereo/monaural switching
- 45 dB power supply rejection
- No coils, all tuning performed with single potentiometer
- Wide operating supply voltage range
- Excellent channel separation
- Emitter follower output buffers

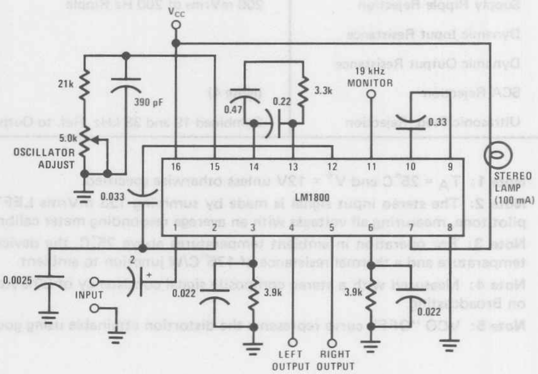
Connection Diagram



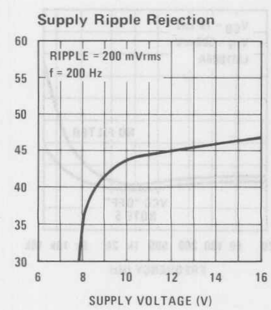
TOP VIEW

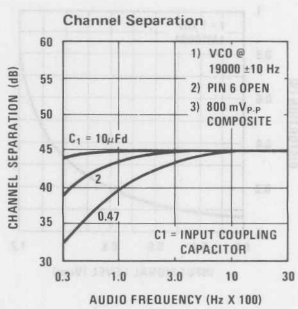
Order Number LM1800N
See NS Package N16A

Typical Application



Typical Performance Characteristics





Absolute Maximum Ratings

Supply Voltage	18V
Power Dissipation (Note 3)	715 mW
Operating Temperature Range	0°C to +70°C
Operating Supply Voltage Range	+10V to +18V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	Lamp "off"		21	30	mA
Lamp Driver Saturation	100 mA Lamp Current		1.3	1.8	V
Lamp Driver Leakage			1.0		nA
Pilot Level for Lamp "ON"	Pin 11 Adjusted to 19.00 kHz		15	20	mVrms
Pilot Level for Lamp "OFF"	Pin 11 Adjusted to 19.00 kHz	3.0	7.0		mVrms
Stereo Lamp Hysteresis		3.0	6.0		dB
Stereo Channel Separation	100 Hz (Note 2)		40		dB
	1000 Hz (Note 2)	30	45		dB
	10000 Hz (Note 2)		45		dB
Monaural Channel Unbalance	200 mVrms, 1000 Hz Input		0.3	1.5	dB
Monaural Voltage Gain	200 mVrms, 400 Hz Input	140	200	260	mVrms
Total Harmonic Distortion	500 mVrms, 1000 Hz Input		0.4	1.0	%
Total Harmonic Distortion	500 mVrms, 1000 Hz Input, 1800A Only		0.1	0.3	%
Capture Range	25 mVrms of Pilot	±2.0		±6.0	% of f_O
Supply Ripple Rejection	200 mVrms of 200 Hz Ripple	35	45		dB
Dynamic Input Resistance		20	45		kΩ
Dynamic Output Resistance		900	1300	2000	Ω
SCA Rejection	(Note 4)		70		dB
Ultrasonic Freq. Rejection	Combined 19 and 38 kHz, Ref. to Output		33		dB

Note 1: $T_A = 25°C$ and $V^+ = 12V$ unless otherwise specified.

Note 2: The stereo input signal is made by summing 123 mVrms LEFT or RIGHT modulated signal with 25 mVrms of 19 kHz pilot tone, measuring all voltages with an average responding meter calibrated in rms. The resulting waveform is about 800 mVp-p.

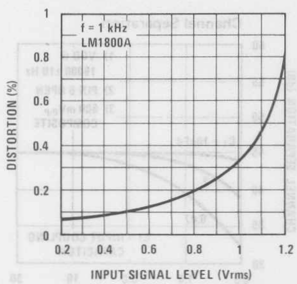
Note 3: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 175°C/W junction to ambient.

Note 4: Measured with a stereo composite signal consistency of 80% stereo, 10% pilot and 10% SCA as defined in the FCC Rules on Broadcasting.

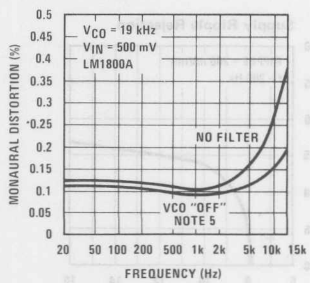
Note 5: VCO "OFF" curve represents the distortion attainable using good 19 kHz and 38 kHz filters.

Typical Performance Characteristics (Continued)

Monaural Distortion vs Input Amplitude



Monaural Distortion vs Frequency



National Semiconductor

Audio/Radio Circuits

LM1818 Electronically Switched Audio Tape System

General Description

The LM1818 is a linear integrated circuit containing all of the active electronics necessary for building a tape recorder deck (excluding the bias oscillator). The electronic functions on the chip include: a microphone and playback preamplifier, record and playback amplifiers, a meter driving circuit, and an automatic input level control circuit. The IC features complete internal electronic switching between the record and playback modes of operation. The multipole switch used in previous systems to switch between record and playback modes is replaced by a single pole switch, thereby allowing for more flexibility and reliability in the recorder design.*

*Monaural operation, *Figure 9*.

Features

- Electronic record/play switching
- 85 dB power supply rejection
- Motional peak level meter circuitry
- Low noise preamplifier circuitry
- 3.5V to 18V supply operation
- Provision for external low noise input transistor

Order Number LM1818N
See NS Package N20A

Typical Applications

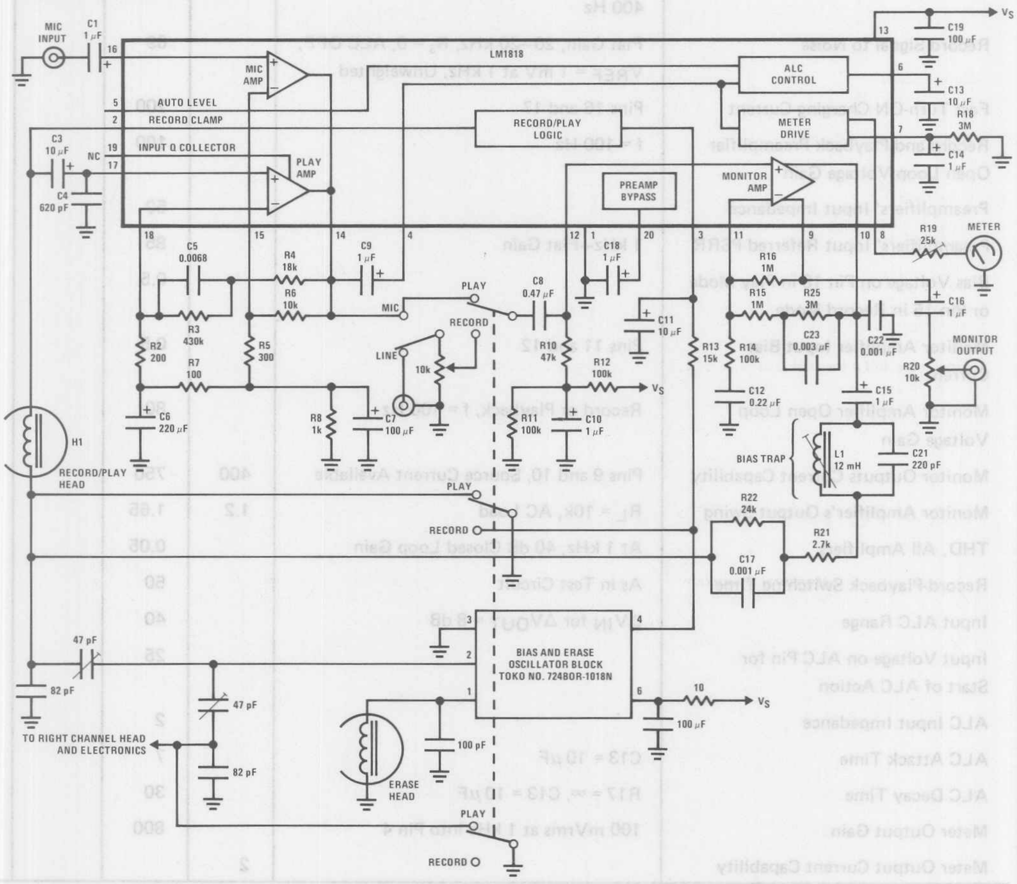


FIGURE 1. Stereo Application Circuit (Left Channel Shown), V_S = 15V

Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Junction Temperature	150°C
Minimum Voltage on Any Pin	−0.1 V_{DC}
Maximum Voltage on Pins 2 and 5	0.1 V_{DC}
Maximum Current Out of Pin 14	5 mA_{DC}
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics V_{CC} = 6V, T_A = 25°C, See Test Circuits *(Figures 2 and 3)*

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage Range		3.5		18	V_{DC}
Supply Current	Test Circuit *(Figure 2)*		5	12	mA
Turn-ON Time	Externally Programmable	50	400		ms
Playback Signal to Noise	DIN Eq. (3180 and 120 μs), 20–20 kHz, R_s = 0, Unweighted, V_{REF} = 1 mV at 400 Hz		74		dB
Record Signal to Noise	Flat Gain, 20–20 kHz, R_s = 0, ALC OFF, V_{REF} = 1 mV at 1 kHz, Unweighted		69		dB
Fast Turn-ON Charging Current	Pins 16 and 17		200		μA
Record and Playback Preamplifier Open Loop Voltage Gain	f = 100 Hz		100		dB
Preamplifiers' Input Impedance			50		kΩ
Preamplifiers' Input Referred PSRR	1 kHz–Flat Gain		85		dB
Bias Voltage on Pin 18 in Play Mode or Pin 15 in Record Mode			0.5		V
Monitor Amplifier Input Bias Current	Pins 11 and 12		0.5		μA
Monitor Amplifier Open Loop Voltage Gain	Record or Playback, f = 100 Hz		80		dB
Monitor Outputs Current Capability	Pins 9 and 10, Source Current Available	400	750		μA
Monitor Amplifier's Output Swing	R_L = 10k, AC Load	1.2	1.65		Vrms
THD, All Amplifiers	At 1 kHz, 40 dB Closed Loop Gain		0.05		%
Record-Playback Switching Time	As in Test Circuit		50		ms
Input ALC Range	ΔV_{IN} for ΔV_{OUT} = 8 dB		40		dB
Input Voltage on ALC Pin for Start of ALC Action			25		mVrms
ALC Input Impedance			2		kΩ
ALC Attack Time	C13 = 10 μF		7		ms
ALC Decay Time	R17 = ∞, C13 = 10 μF		30		sec
Meter Output Gain	100 mVrms at 1 kHz into Pin 4		800		mV_{DC}
Meter Output Current Capability		2			mA_{DC}

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 175°C/W junction to ambient.

Test Circuits

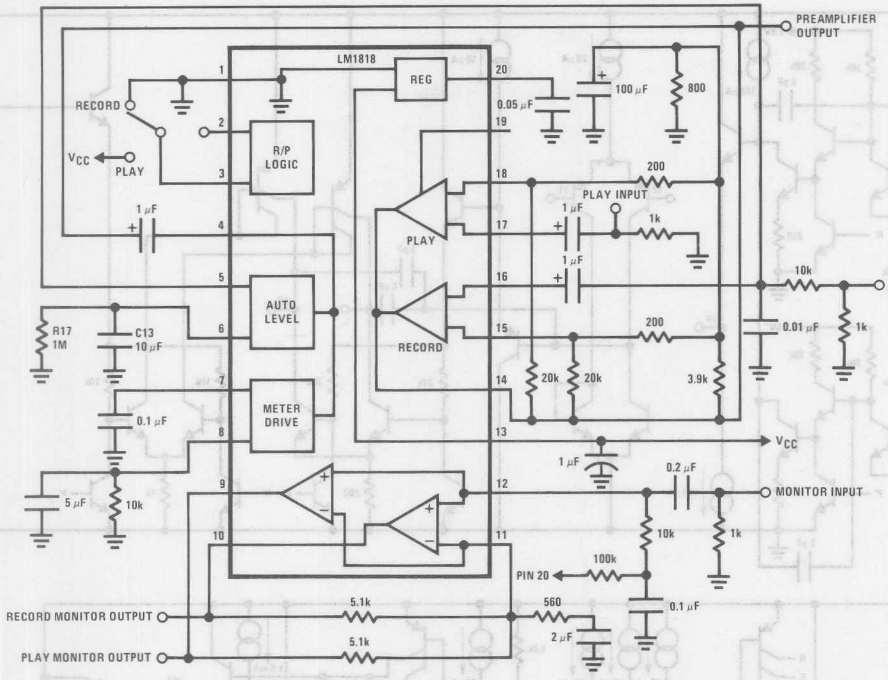


FIGURE 2. General Test Circuit

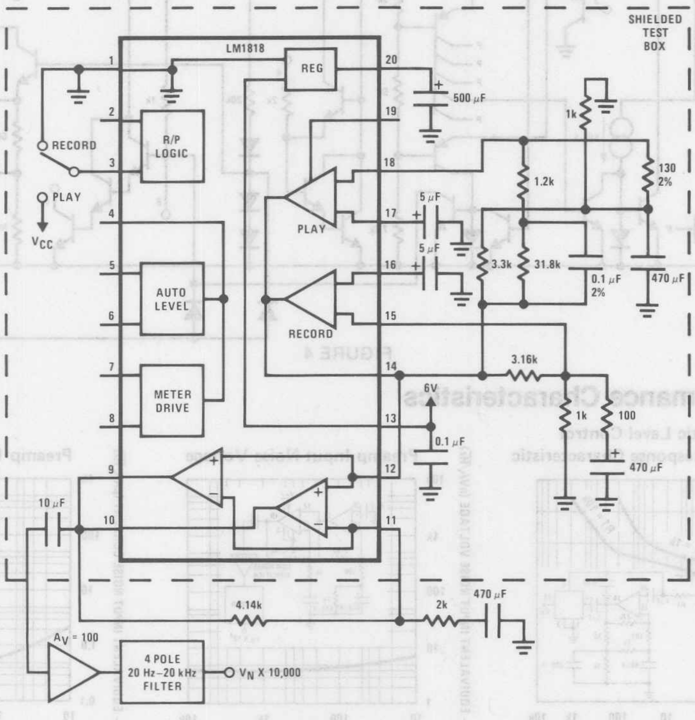


FIGURE 3. Noise Test Circuit

Equivalent Schematic Diagram

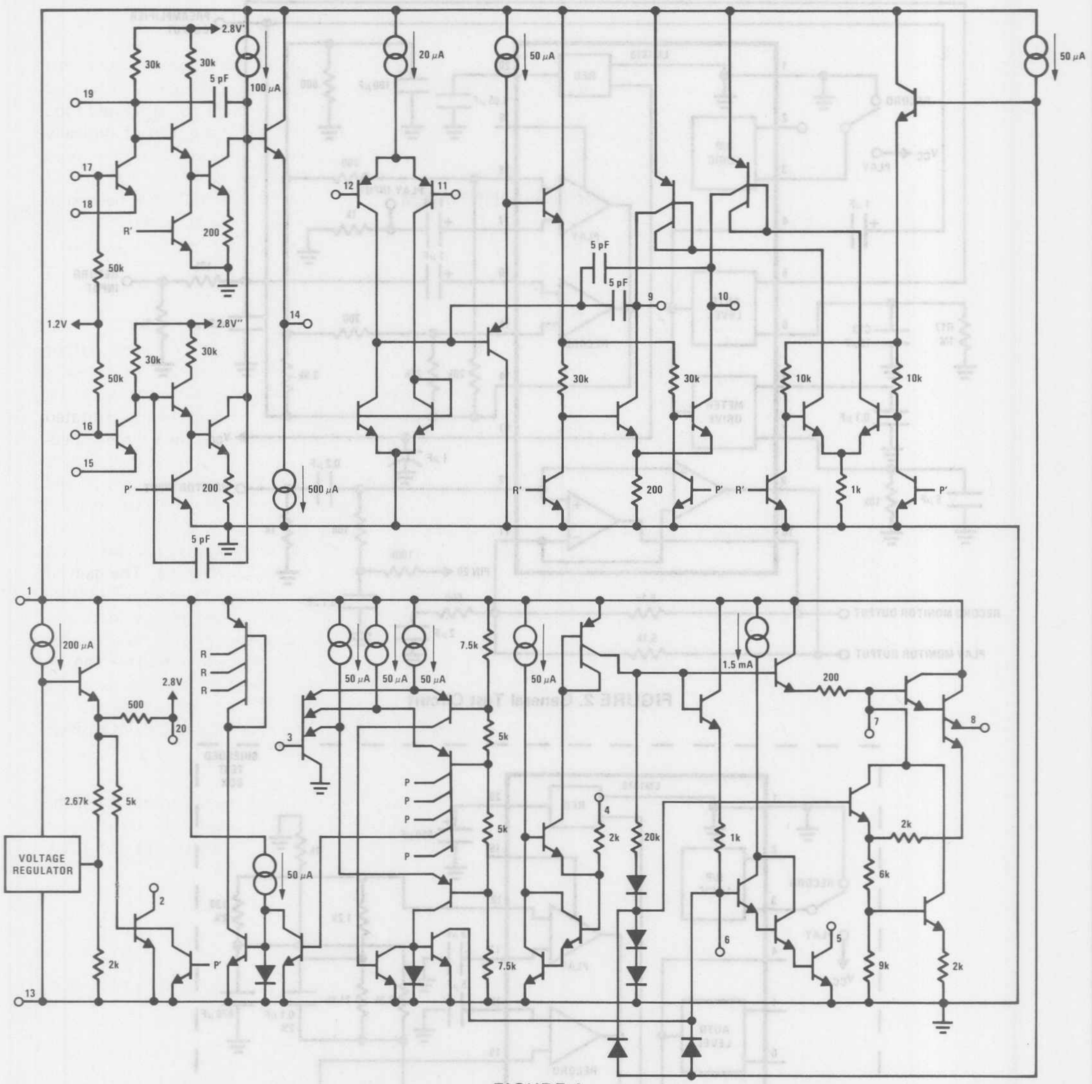
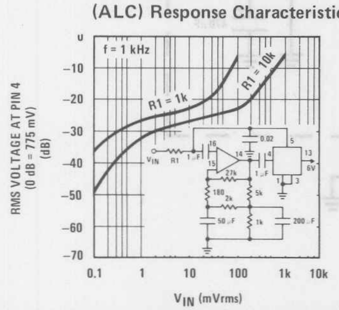


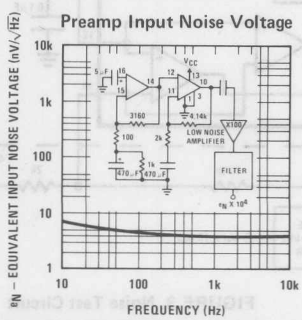
FIGURE 4

Typical Performance Characteristics

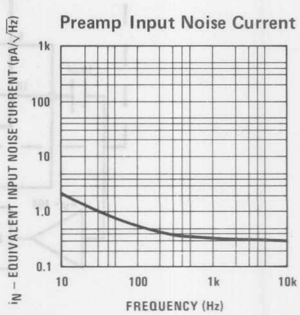
Automatic Level Control (ALC) Response Characteristic



Preamp Input Noise Voltage



Preamp Input Noise Current



Application Hints

Preamplifiers *(Figure 5)*

There are 2 identical preamplifiers with 1 common output pin on the IC. One amplifies low level inputs such as a microphone in the record mode and another amplifies the signal from the playback head in the playback mode. The amplifiers use a common capacitor, C6, to set the low frequency pole of the closed loop responses. On the playback amplifier, the collector of the input device is made available so that an external low noise device can be connected in critical applications. When using an external low noise transistor, pins 17 and 18 of the IC are shorted together to ensure that the internal input transistor is turned OFF and the external transistor's collector is tied to pin 19. The input and feedback connections are now made to the external input transistor. The amplifiers are stable for all gains above 5 and have a typical open loop gain of 100 dB. R8 and R9 enable C6 to be quickly charged and set the DC gain. Internal biasing provides a DC voltage independent of temperature at pin 17 so that the preamplifier DC output will remain relatively constant with temperature. Supply decoupling is provided by an internal regulator. Additional decoupling can be added for the input stages by increasing the size of the capacitor on pin 20 of the IC. A fast charging circuit is connected to the preamplifiers' input capacitors (pins 16 and 17) to decrease the turn-ON time. Larger input capacitors decrease the noise by reducing the source impedance at lower frequencies where 1/f noise current produces an input noise voltage. The input resistance of the preamplifiers is typically 50 kΩ.

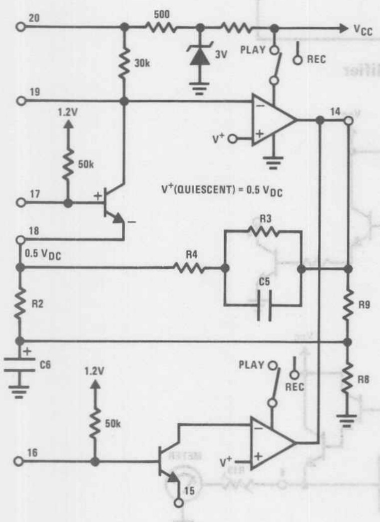
Monitor and Record Amplifiers *(Figure 6)*

The monitor and record amplifiers share common input and feedback connections but have separate outputs. During playback, the input signal is amplified and appears only at the playback monitor output. Because the outputs are separate, different feedback components can be used and, as a result, totally different responses can be set. The amplifiers are stable for all closed loop gains above 3 and have an open loop gain of typically 80 dB. The outputs are capable of supplying a minimum of 400 μA into a load and swing within 500 mV of either V_{CC} or ground. If more than 400 μA is needed to drive a load, an external pull-up resistor on the output of these amplifiers can increase the load driving capability.

Automatic Level Control – ALC *(Figure 7)*

The automatic level control provides a constant output level for a wide range of record source input levels. The ALC works on the varying impedance characteristic of a saturated transistor. The impedance of the saturated transistor forms a voltage divider with the source impedance of a series resistor (R1 in *Figure 9*). The input signal is decreased as the ALC transistor is increasingly forward biased. The ALC transistor will be forward biased when the preamplifier's AC output (pin 14), coupled to the combination ALC-meter drive input (pin 4) reaches 40 mV peak (25 mVrms). The gain of the ALC loop is such that a preamp input signal increase of 10 dB will result in a 2 dB increase on the AC output of the preamplifier. If greater than 25 mVrms is desired at the output of the preamp, a series resistor can be added between the preamp output coupling capacitor and the ALC input (pin 4). The input impedance of the ALC circuit is 2 kΩ; therefore, if a 2 kΩ series resistor is added, ALC action will begin at 50 mVrms.

The ALC memory capacitor connected to pin 6 has the additional function of amplifier anti-pop control; for this reason, it is necessary that a capacitor be connected to pin 6 even if ALC is not used.



Quiescent DC Output Voltage

$$V_{DC} = \left(1 + \frac{R9}{R8}\right)(0.5 - 50 \times 10^{-6} R2)\text{V if } R2 + R3 > 10\,R_E$$

$$\text{where } R_E = \frac{R8R9}{R8 + R9}$$

AC Voltage Gain

$$A_{AC} = \frac{R4 + \dfrac{R3}{1 + SC5R3}}{R2} + 1$$

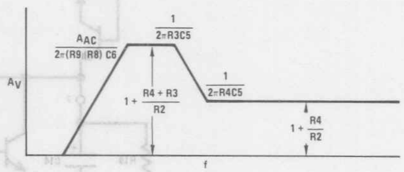


FIGURE 5. Preamplifier

The meter drive output (pin 8) is capable of supplying 1–2 mA at a filtered DC voltage that is typically equal to 10 times the RMS value of the signal applied to the ALC-meter drive input pin (pin 4). The RC network connected to pin 7 of the IC determines the memory constant of the meter circuit. It is therefore possible to store the peak input signal by giving this RC network a long time constant, or read the instantaneous signal level by giving this RC network a very short time constant (i.e., no capacitor). This memory capacitor is discharged within the integrated circuit at a discharge rate related to the DC level on the meter output pin. When the meter output pin is between 0 V_{DC} and 0.7 V_{DC} there is a 50 μA discharge current; when the pin is between 0.7V and 1.1V there is no internal discharge current; and when the voltage on pin 8 is greater than 1.1V there is a discharge equivalent to a 3.3k resistor across the memory capacitor. These different discharge rates allow the meter circuit to display fast, accurate responses on the lower portion of the meter display, slow responses in the higher portion of the meter display, and rapid discharge when the voltage is above the maximum reading the meter can display. The resistor in series with the meter can be adjusted such that the previously mentioned responses coincide with the proper points (0 VU and +3 VU) on the meter scale.

$$\text{Record gain} = 1 + \frac{R15}{R14}$$

$$\text{Playback gain} = 1 + \frac{R16}{R14}$$

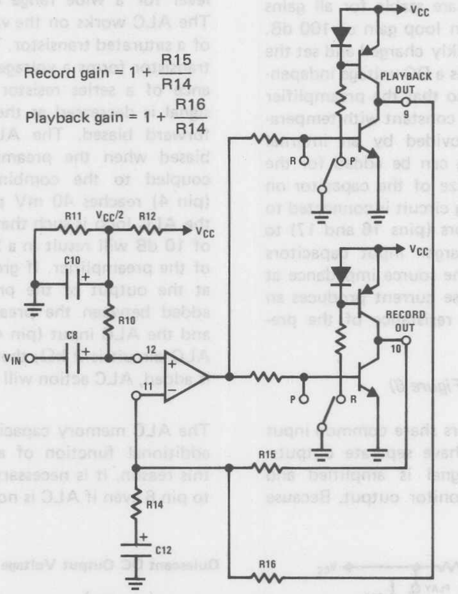


FIGURE 6. Monitor Amplifier

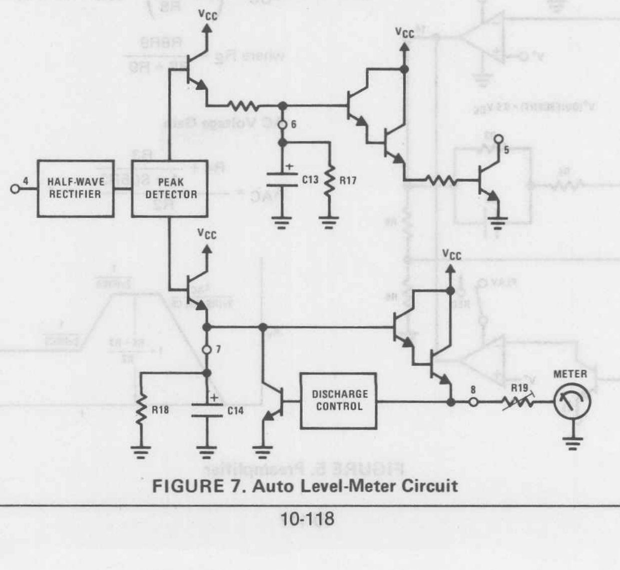


FIGURE 7. Auto Level-Meter Circuit

Application Hints (Continued)

Anti-Pop Circuitry *(Figure 8)*

The capacitor on pin 3 is used in a time delay system in conjunction with C13, the ALC capacitor, to suppress pops when switching between record and playback. *Figure 8* illustrates how this is done. The output amplifier, either record or playback, is shut off prior to switching and carefully rebiased after switching takes place. It is therefore required that a proper ratio is selected between the ALC capacitor and the logic input RC time constant. The ALC capacitor must be discharged to 0.7V within the time it takes the logic input capacitor to: 1) charge from $V_{CC}/2$ to 0.7 V_{CC} when switching from record to playback, or 2) discharge from $V_{CC}/2$ to 0.3 V_{CC} when switching from playback to record. These times would normally be similar; however, the ALC capacitor can be charged to a different initial value depending upon the input to the ALC circuit. The maximum value to which the ALC memory capacitor will normally charge is 3.2V, therefore, the maximum time allowed for discharging C13 is given by:

$$t1 = \frac{(C13 \times \Delta V)}{I_1} \quad C13 \frac{(3.2V - 0.7V)}{350\,\mu A}$$

$$= C13 \times 7.2 \times 10^4$$

If C13 = 10 μF, t1 = 72 ms

It it now necessary to determine the minimum value for the R/P logic capacitor. This is done by computing the time between the 2 voltage switching points using the exponential equations for a single RC network.

$$t2 = R13\,C11 \ln\left[\frac{V_{CC}}{0.3\,V_{CC}}\right] - R13\,C11 \ln\left[\frac{V_{CC}}{0.5\,V_{CC}}\right] = 0.51\ R13\,C11$$

To be sure that C13 is completely discharged, let t2 > t1.

$$R13\,C11 > \frac{t1}{0.51} = \frac{(72\text{ ms})}{0.15} = 141\text{ ms}$$

If C11 = 10 μF, R13 = 15 kΩ

R13 should be kept to a value less than 50 kΩ to insure that bias current existing from pin 3 does not cause an offset voltage above 200 mV. Typically this bias current is less than 3 μA.

Record Playback Switch

When the voltage on pin 3 of the IC is greater than 0.5 V_{CC}, the internal record-playback switch switches into the playback mode. During playback the record preamplifier remains partially biased but the input signal to this preamp does not appear at the preamplifier output. In addition, during the playback mode, the record monitor output (pin 9) is disabled and the ALC circuit operates to minimize the signal into the record preamp input. The meter circuit is operational in the playback as well as the record mode. Similarly, during the record mode, the playback preamp input is ignored and the playback monitor output is disabled. In addition, a pin is available to hold one side of the record head at ground potential while sinking up to 500 μA of AC bias and record current.

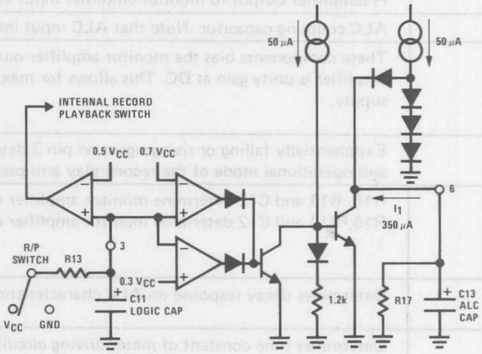


FIGURE 8A. Anti-Pop Circuit

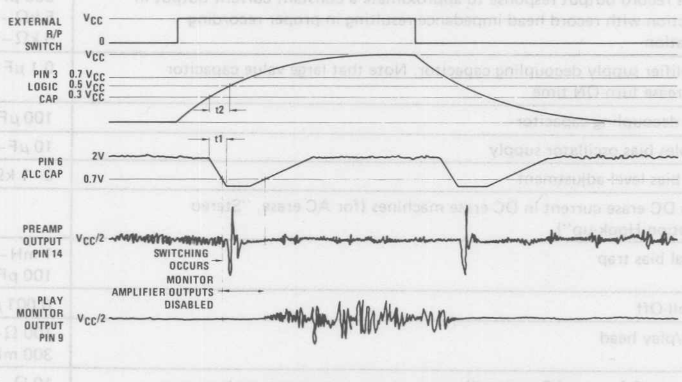


FIGURE 8B. Waveform for Anti-Pop Circuit

External Components

(Refer to *Figure 9,* Monaural Application Circuit)

COMPONENT	EXTERNAL COMPONENT FUNCTION	NORMAL RANGE OF VALUE
R1	Used in conjunction with varying impedance of pin 5, forming a resistor divider network to reduce input level in automatic level control circuit	500 Ω–20 kΩ
C2	Forms a noise reduction system by varying bandwidth as a function of the changing impedance on pin 5. With a small input signal, the bandwidth is reduced by R1 and C2. As the input level increases, so does the bandwidth.	0.01 μF–0.5 μF
C1, C3	Coupling capacitors. Because these are part of the source impedance, it is important to use the larger values to keep low frequency source impedance at a minimum.	0.5 μF–10 μF
C4	Radio frequency interference roll-off capacitor	100 pF–300 pF
R2 R3 R4 C5	Playback response equalization. C5 and R3 form a pole in the amplifier response at 50 Hz. C5 and R4 form a zero in the response at 1.3 kHz for 120 μs equalization and 2.3 kHz for 70 μs equalization.	50 Ω–200 Ω 47 kΩ–3.3 MΩ 2 kΩ–200 kΩ
R5 R6	Microphone preamplifier gain equalization	50 Ω–200 Ω 5 kΩ–200 kΩ
R7 R8 R9 C6 C7	DC feedback path. Provides a low impedance path to the negative input in order to sink the 50 μA negative input amplifier current. C6, R9, R7 and C7 provide isolation from the output so that adequate gain can be obtained at 20 Hz. This 2-pole technique also provides fast turn-ON settling time.	0–2 kΩ 200Ω–5 kΩ 1 kΩ–30 kΩ 200 μF–1000 μF 0–100 μF
C8	Preamplifier output to monitor amplifier input coupling	0.05 μF–1 μF
C9	ALC coupling capacitor. Note that ALC input impedance is 2 kΩ	0.1 μF–5 μF
R10 R11 R12 C10	These components bias the monitor amplifier output to half supply since the amplifier is unity gain at DC. This allows for maximum output swing on a varying supply.	10 kΩ–100 kΩ 10 kΩ–100 kΩ 10 kΩ–100 kΩ 1 μF–100 μF
C11 R13	Exponentially falling or rising signal on pin 3 determines sequencing, time delay, and operational mode of the record/play anti-pop circuitry. See anti-pop diagram.	0–10 μF 0–50 kΩ
R14 R15 R16 C12	R16, R14 and C12 determine monitor amplifier response in the play mode. R15, R14 and C12 determine monitor amplifier response in the record mode.	1k–100k 30 kΩ–3 MΩ 30 kΩ–3 MΩ 0.1 μF–20 μF
C13 R17	Determines decay response on ALC characteristic and reduces amplifier pop	5 μF–20 μF 100k–∞
C14 R18	Determines time constant of meter driving circuitry	0.1 μF–10 μF 100k–∞
R19	Meter sensitivity adjust	10 kΩ–100 kΩ
C15	Record output DC blocking capacitor	1 μF–10 μF
C16	Play output DC blocking capacitor	0.1 μF–10 μF
C17 R21 R22	Changes record output response to approximate a constant current output in conjunction with record head impedance resulting in proper recording equalization	500 pF–0.1 μF 5 kΩ–100 kΩ 5 kΩ–100 kΩ
C18	Preamplifier supply decoupling capacitor. Note that large value capacitor will increase turn-ON time	0.1 μF–500 μF
C19	Supply decoupling capacitor	100 μF–1000 μF
C20	Decouples bias oscillator supply	10 μF–500 μF
R23	Allows bias level adjustment	0–1 kΩ
R24	Adjusts DC erase current in DC erase machines (for AC erase, "Stereo Application Hook-up")	
L1 C21	Optional bias trap	1 mH–30 mH 100 pF–2000 pF
C22	Bias Roll-Off	0.001 μF–0.01 μF
H1	Record/play head	100 Ω–500 Ω; 70 mH–300 mH
H2	Erase head (DC type, AC optional)	10 Ω–300 Ω

Typical Applications (Continued)

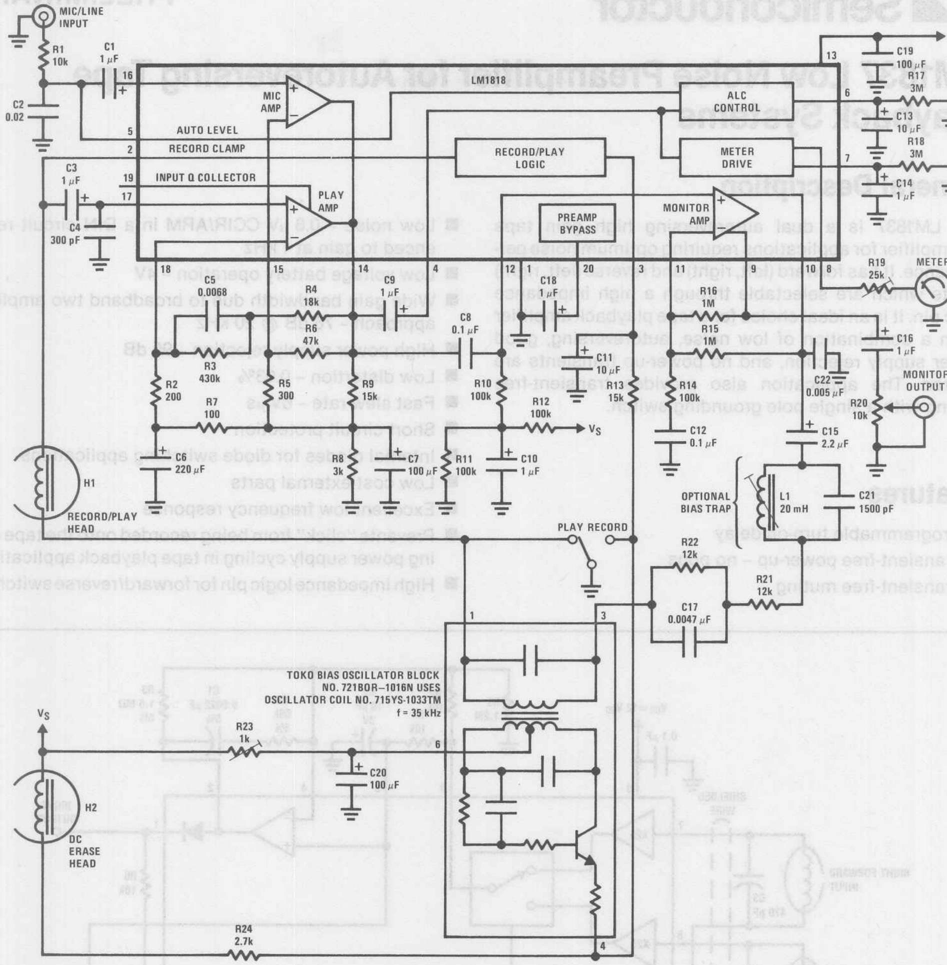


FIGURE 9A. Monaural Application Circuit

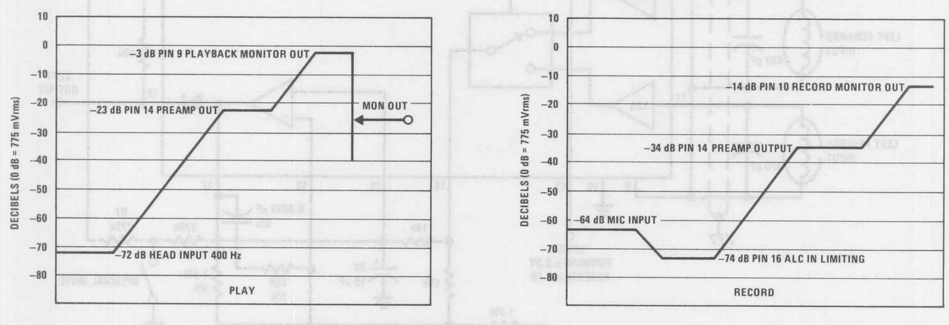


FIGURE 9B. Level Diagram for Monaural Application Circuit

LM1837 Low Noise Preamplifier for Autoreversing Tape Playback Systems

General Description

The LM1837 is a dual autoreversing high gain tape preamplifier for applications requiring optimum noise performance. It has forward (left, right) and reverse (left, right) inputs which are selectable through a high impedance logic pin. It is an ideal choice for a tape playback amplifier when a combination of low noise, autoreversing, good power supply rejection, and no power-up transients are desired. The application also provides transient-free muting with a single pole grounding switch.

Features

- Programmable turn-on delay
- Transient-free power-up – no pops
- Transient-free muting
- Low noise – 0.6 μV CCIR/ARM in a DIN circuit referenced to gain at 1 kHz
- Low voltage battery operation – 4V
- Wide gain bandwidth due to broadband two amplifier approach – 76 dB @ 20 kHz
- High power supply rejection – 95 dB
- Low distortion – 0.03%
- Fast slew rate – 6V/μs
- Short circuit protection
- Internal diodes for diode switching applications
- Low cost external parts
- Excellent low frequency response
- Prevents "click" from being recorded onto the tape during power supply cycling in tape playback applications
- High impedance logic pin for forward/reverse switching

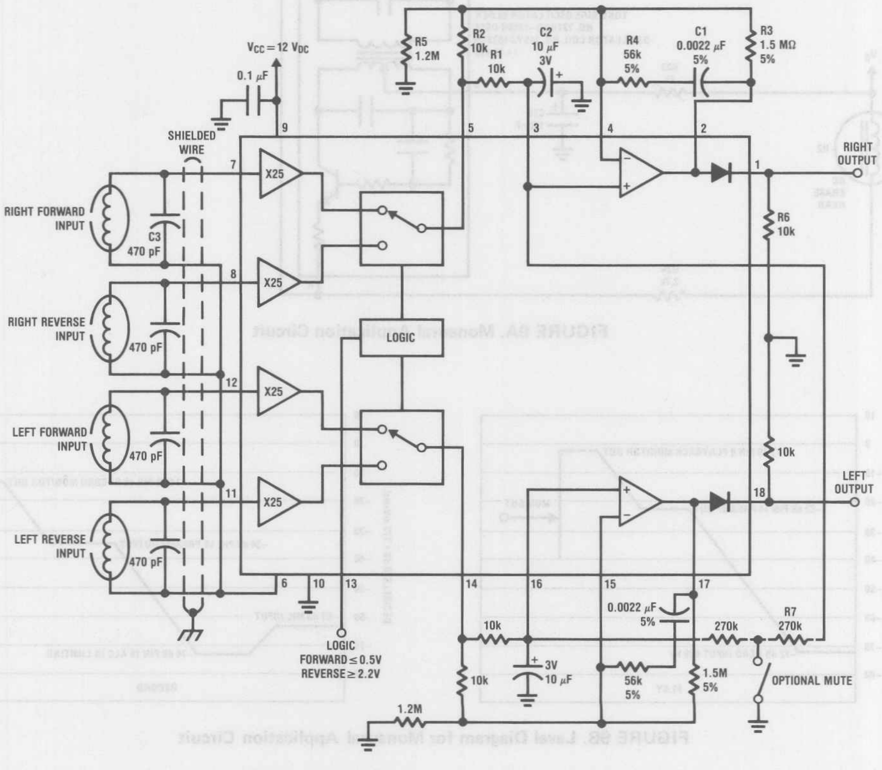


FIGURE 1. Autoreversing Tape Playback Application

Absolute Maximum Ratings

Supply Voltage	18V	Operating Temperature	0°C to +70°C
Voltage on Pins 1 and 18	18V	Minimum Voltage on Any Pin	$-0.1\ V_{DC}$
Package Dissipation (Note 1)	1390 mW	Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature	−65°C to +150°C		

Electrical Characteristics ($T_A = 25°C$, $V_{CC} = 12V$, see Test Circuit, *Figure 2*)

Parameter	Conditions	Min	Typ	Max	Units
Operating Supply Voltage Range	R5 Removed from Circuit for Low Voltage Operation	4		18	V
Supply Current	$V_{CC} = 12V$		9	15	mA
Total Harmonic Distortion	f = 1 kHz, $V_{IN} = 0.3$ mV, Pins 2 and 17, *Figure 2*		0.03		%
THD + Noise (Note 2)	f = 1 kHz, $V_{OUT} = 1V$, Pins 2 and 17, *Figure 2*		0.10	0.25	%
Power Supply Rejection	Input Ref. f = 1 kHz, 1 Vrms	80	95		dB
Channel Separation (Note 3)	f = 1 kHz, Output = 1 Vrms, Output to Output				dB
Left to Right		40	60		dB
Forward to Reverse		40	60		dB
Signal-to-Noise (Note 4)	Unweighted 32 Hz–12.74 kHz (Note 2)		58		dB
	CCIR/ARM (Note 5)		62		dB
	A Weighted		64		dB
	CCIR, Peak (Note 6)		52		dB
Noise	Output Voltage CCIR/ARM (Note 5)		120	200	μV
Input Amplifiers					
Input Bias Current			0.5	2.0	μA
Input Impedance	f = 1 kHz	150			kΩ
AC Gain		27	28	29	dB
AC Gain Imbalance			±0.15	±0.5	dB
DC Output Voltage		2.1	2.5	2.9	V
DC Output Voltage Mismatch	Pins 5 and 14	−200	±30	200	mV
Output Source Current	Pins 5 and 14	2	10		mA
Output Sink Current	Pins 5 and 14	300	600		μA
Logic Level					
Forward				0.5	V
Reverse		2.2			V
Logic Pin Current			2	6	μA
DC Voltage Change at Pins 5 and 14	Change Logic State	−100	±20	100	mV
Output Amplifiers					
Closed Loop Gain	Stable Operation	5			V/V
Open Loop Voltage Gain	DC		100		dB
Gain Bandwidth Product			5		MHz
Slew Rate			6		V/μs
Input Offset Voltage			2	5	mV
Input Offset Current			20	100	nA
Input Bias Current			250	500	nA
Output Source Current	Pin 2 or 17	2	10		mA
Output Sink Current	Pin 2 or 17	400	900		μA
Output Voltage Swing	Pin 2 or 17		11		Vp-p
Output Diode Leakage	Voltage on Pins 1 and 18 = 18V		0	10	μA

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 90°C/W junction to ambient.

Note 2: Measured with an average responding voltmeter using the filter circuit in *Figure 4*. This simple filter is approximately equivalent to a "brick wall" filter with a passband of 20 Hz to 20 kHz (see Application Hints). For 1 kHz THD the 400 Hz high pass filter on the distortion analyzer is used.

Note 3: Channel separation can be measured by applying the input signal through transformers to simulate a floating source (see Application Hints). Care must be taken to shield the coils from extraneous signals. Actual production test techniques at National simulate this floating source with a more complex op amp circuit.

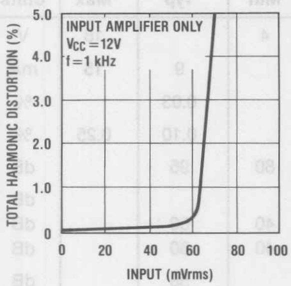
Note 4: The numbers are referred to an output level of 160 mV at pins 2 and 17 using the circuit of *Figure 2*. This corresponds to an input level of 0.3 mVrms at 333 Hz.

Note 5: Measured with an average responding voltmeter using the Dolby lab's standard CCIR filter having a unity gain reference at 2 kHz.

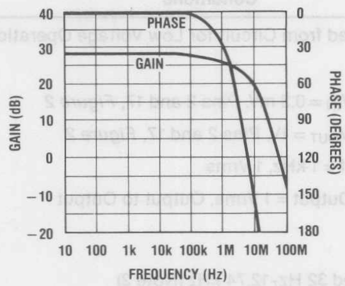
Note 6: Measured using the Rhode-Schwarz psophometer, model UPGR.

Typical Performance Characteristics

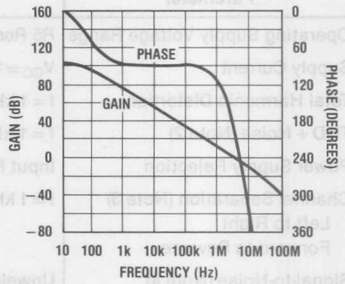
Input Amplifier THD vs Input Level



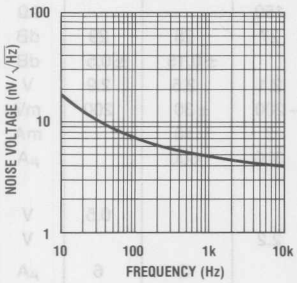
Input Amplifier Gain and Phase vs Frequency



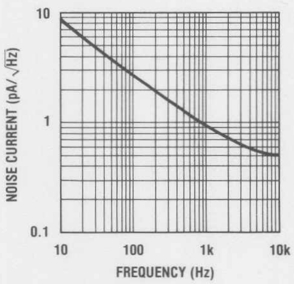
Output Amplifier Open Loop Gain and Phase vs Frequency



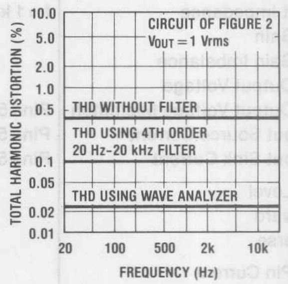
Spot Noise Voltage vs Frequency



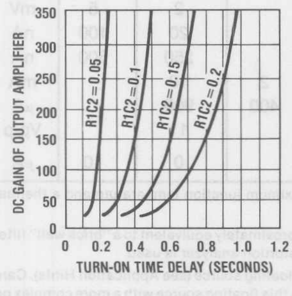
Spot Noise Current vs Frequency



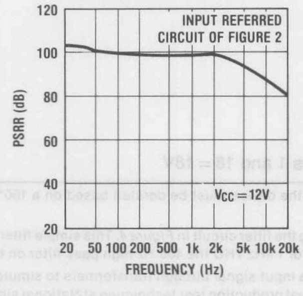
Total Harmonic Distortion vs Frequency



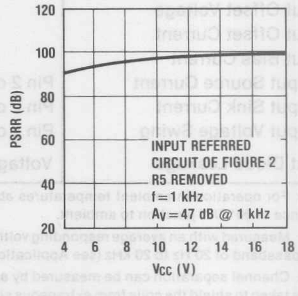
Turn-On Delay vs Component Values and Gain



PSRR vs Frequency

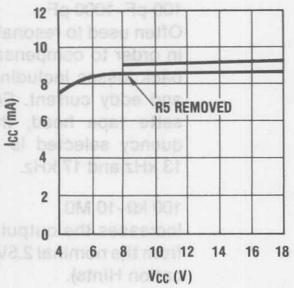


PSRR vs V_{CC}

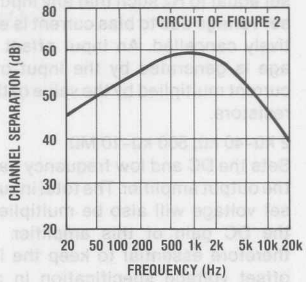


Typical Performance Characteristics (Continued)

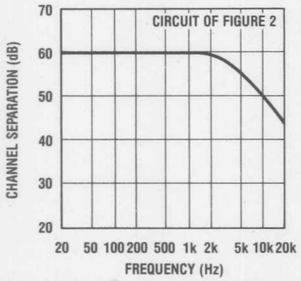
I_{CC} vs V_{CC}



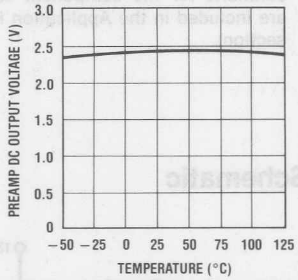
Right to Left Channel Separation vs Frequency



Forward to Reverse Channel Separation vs Frequency

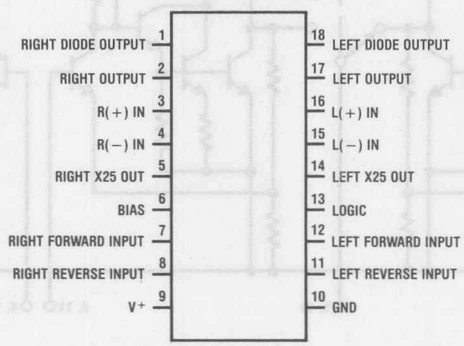


Input Amplifier DC Output Voltage vs Temperature (Pins 5, 14)



Connection Diagram

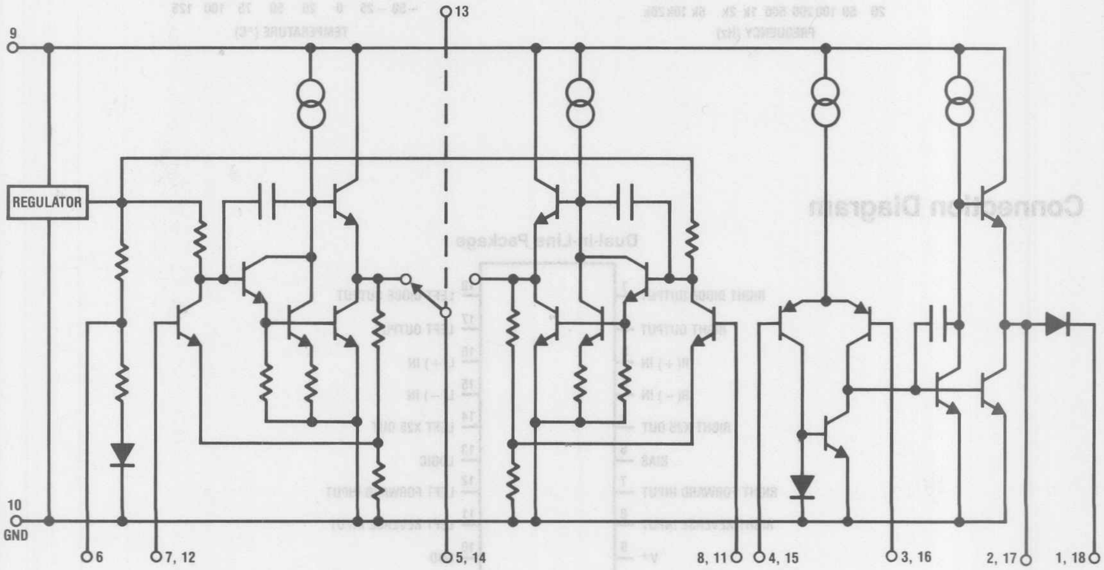
Dual-In-Line Package



TOP VIEW

	Set turn-on delay and second amplifier's low frequency pole. Leakage current in C2 results in DC offset between the amplifier's inputs and therefore this current should be kept low. R1 is set equal to R2 such that any input offset voltage due to bias current is effectively cancelled. An input offset voltage is generated by the input offset current multiplied by the value of these resistors.		Biases the output diode when it is used in DC switching applications. This resistor can be excluded if diode switching is not desired.
R2, R3	2 kΩ–40 kΩ, 500 kΩ–10 MΩ Sets the DC and low frequency gain of the output amplifier. The total input offset voltage will also be multiplied by the DC gain of this amplifier. It is therefore essential to keep the input offset voltage specification in mind when employing high DC gain in the output amplifier; i.e., 5 mV × 400 = 2V offset at the output.	C3	100 pF–1000 pF Often used to resonate with tape head in order to compensate for tape playback losses including tape head gap and eddy current. For a typical cassette tape head, the resonant frequency selected is usually between 13 kHz and 17 kHz.
R4, C1	10 kΩ–200 kΩ, 0.00047 μF–0.01 μF Set tape playback equalization characteristics in conjunction with R3 (calculations for the component values are included in the Application Hints section).	R5	100 kΩ–10 MΩ Increases the output DC bias voltage from the nominal 2.5V value (see Application Hints).
		R7	Optionally used for tape muting. The use of this resistor can also provide "no-pop" turn-off if desired (see Application Hints).

Simplified Schematic



Application Hints

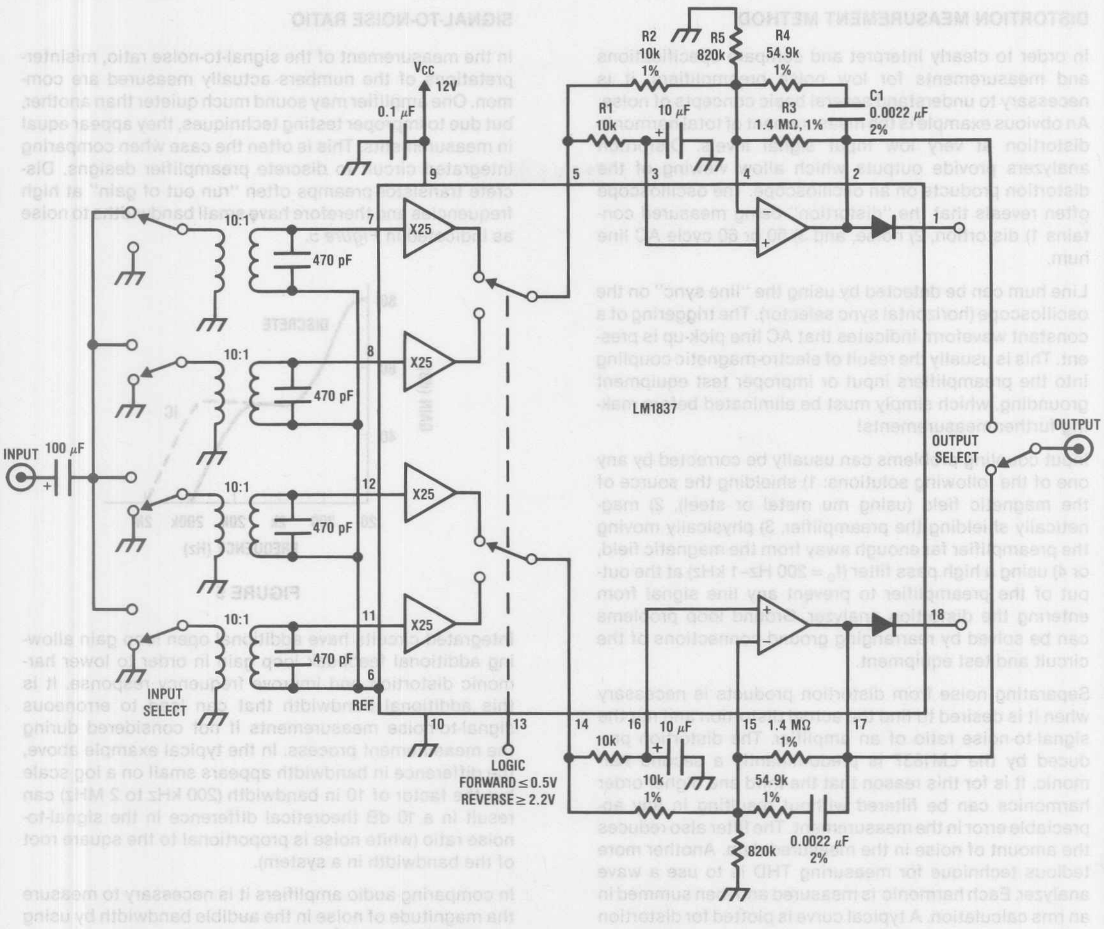


FIGURE 2. General Test Circuit

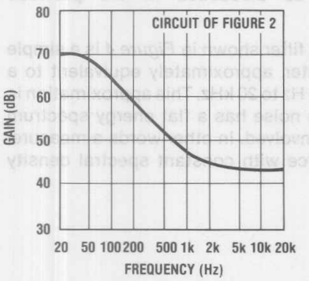


FIGURE 3. Frequency Response of Test Circuit

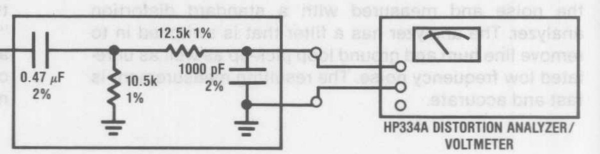


FIGURE 4. Simple 32 Hz–12740 Hz Filter and Meter

Application Hints (Continued)

DISTORTION MEASUREMENT METHOD

In order to clearly interpret and compare specifications and measurements for low noise preamplifiers, it is necessary to understand several basic concepts of noise. An obvious example is the measurement of total harmonic distortion at very low input signal levels. Distortion analyzers provide outputs which allow viewing of the distortion products on an oscilloscope. The oscilloscope often reveals that the "distortion" being measured contains 1) distortion, 2) noise, and 3) 50 or 60 cycle AC line hum.

Line hum can be detected by using the "line sync" on the oscilloscope (horizontal sync selector). The triggering of a constant waveform indicates that AC line pick-up is present. This is usually the result of electro-magnetic coupling into the preamplifiers input or improper test equipment grounding, which simply must be eliminated before making further measurements!

Input coupling problems can usually be corrected by any one of the following solutions: 1) shielding the source of the magnetic field (using mu metal or steel), 2) magnetically shielding the preamplifier, 3) physically moving the preamplifier far enough away from the magnetic field, or 4) using a high pass filter (f_o = 200 Hz–1 kHz) at the output of the preamplifier to prevent any line signal from entering the distortion analyzer. Ground loop problems can be solved by rearranging ground connections of the circuit and test equipment.

Separating noise from distortion products is necessary when it is desired to find the actual distortion and not the signal-to-noise ratio of an amplifier. The distortion produced by the LM1837 is predominantly a second harmonic. It is for this reason that the third and higher order harmonics can be filtered without resulting in any appreciable error in the measurement. The filter also reduces the amount of noise in the measured data. Another more tedious technique for measuring THD is to use a wave analyzer. Each harmonic is measured and then summed in an rms calculation. A typical curve is plotted for distortion vs frequency using this method. A typical curve is also included using a 20 Hz to 20 kHz 4th order filter.

To specify the distortion of the LM1837 accurately and also not require unusual or tedious measurements the following method is used. The output level is set to 1 Vrms at 1 kHz (approximately 5 mV at the input). The output is filtered with the circuit of *Figure 4* to limit the bandwidth of the noise and measured with a standard distortion analyzer. The analyzer has a filter that is switched in to remove line hum and ground loop pick-up as well as unrelated low frequency noise. The resulting measurement is fast and accurate.

SIGNAL-TO-NOISE RATIO

In the measurement of the signal-to-noise ratio, misinterpretations of the numbers actually measured are common. One amplifier may sound much quieter than another, but due to improper testing techniques, they appear equal in measurements. This is often the case when comparing integrated circuit to discrete preamplifier designs. Discrete transistor preamps often "run out of gain" at high frequencies and therefore have small bandwidths to noise as indicated in *Figure 5*.

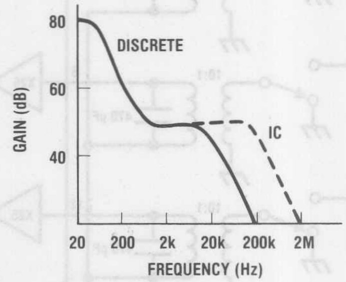


FIGURE 5

Integrated circuits have additional open loop gain allowing additional feedback loop gain in order to lower harmonic distortion and improve frequency response. It is this additional bandwidth that can lead to erroneous signal-to-noise measurements if not considered during the measurement process. In the typical example above, the difference in bandwidth appears small on a log scale but the factor of 10 in bandwidth (200 kHz to 2 MHz) can result in a 10 dB theoretical difference in the signal-to-noise ratio (white noise is proportional to the square root of the bandwidth in a system).

In comparing audio amplifiers it is necessary to measure tha magnitude of noise in the audible bandwidth by using a "weighting" filter.[1] A "weighting" filter alters the frequency response in order to compensate for the average human ear's sensitivity to certain undesirable frequency spectra. The weighting filters at the same time provide the bandwidth limiting as discussed in the previous paragraph.

The 32 Hz to 12740 Hz filter shown in *Figure 4* is a simple two pole, one zero filter, approximately equivalent to a "brick wall" filter of 20 Hz to 20 kHz. This approximation is absolutely valid if the noise has a flat energy spectrum over the frequencies involved. In other words a measurement of a noise source with constant spectral density

Application Hints (Continued)

through either of the two filters would result in the same reading. The output frequency response of the two filters is shown in *Figure 6*.

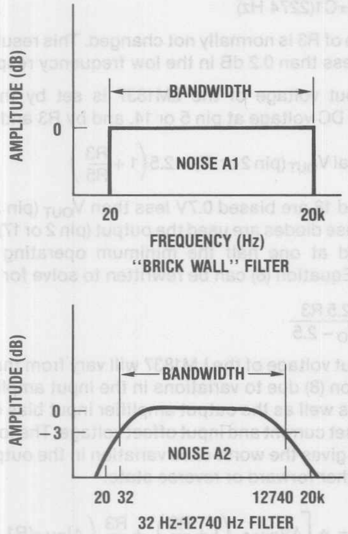


FIGURE 6

Typical signal-to-noise figures are listed for several weighting filters which are commonly used in the measurement of noise. The shape of all weighting filters is similar with the peak of the curve usually occurring in the 3 kHz–7 kHz region as shown in *Figure 7*.

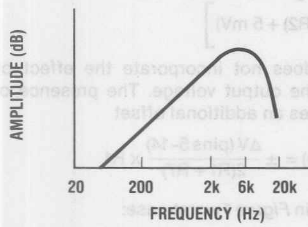


FIGURE 7

In addition to noise filtering, differing meter types give different noise readings. Meter responses include: 1) rms reading, 2) average responding, 3) peak reading, and 4) quasi peak reading. Although theoretical noise analysis is derived using true rms (root mean square) based calculations, most actual measurement is taken with ARM (Average Responding Meter) test equipment.

Unless otherwise noted an average responding meter is used for all AC measurements in this data sheet.

BASIC CIRCUIT APPROACH

The LM1837 IC incorporates a two stage broadband design which minimizes noise, attains overall DC stability and prevents audible transients during turn-on.

The first stage consists of four direct coupled preamplifiers with internal gain of 25V/V (28 dB). Direct coupling to the tape head reduces input source impedance and external component cost by removing the input coupling capacitor. A typical input coupling capacitor of 1 μF has a reactance of 1.5 kΩ at 100 Hz. The resulting noise due to the amplifier's input noise current can dominate the noise voltage at the output of the playback system. The inputs of the amplifiers are biased from a common reference voltage that is temperature compensated to produce a quiescent DC voltage of 2.5V at the output of the first stage. The input stage bias current that flows through the tape head is kept below 2 μA in order to prevent any erasure of tape moving past the head. An added advantage of DC biasing is the prevention of large current transients during the charging of coupling capacitors at turn-on and turn-off. The outputs of the forward and reverse preamplifier are fed to the common output op amp through a logic controlled switch.

The second stage provides additional gain and proper equalization while preventing audible turn-on transients or "pops". The output (pin 2) is kept low until C2 charges through R1. When the voltage on C2 gets close to the DC voltage on pin 5, the output rises exponentially to its final DC value. The result is a transient-free turn-on characteristic.

Internal diodes are provided to facilitate electronic diode switching popular in automotive applications.

The General Test Circuit illustrates the topography of the system. The components determining the overall frequency response are external due to the extreme sensitivity when matching a DIN equalization curve.

MUTE CIRCUIT AND LOGIC

The LM1837 can be muted with the addition of two resistors and a grounding switch, as shown in *Figure 1*. When the circuit is not muted the additional resistors have no effect on the AC performance. They *do* have an effect on the DC Q point however.

The difference in the DC output voltages of the input amplifiers is applied across the mute resistors (R7) and the positive input resistors (R1). This results in an additional offset at the input of the output amplifiers. To keep this offset to a minimum R7 should be as large as possible to achieve effective muting. Unmute voltage is the peak signal the preamplifier can swing without turning on the output amplifier under mute conditions:

Unmute voltage =

$$V_{PIN\ 5,\ 14}\left[\frac{R5//R3}{R2 + R5//R3} - \frac{R7}{R1 + R7}\right]$$

For example: The circuit in *Figure 1* has 2.5V DC at pins 5 and 14, so:

Unmute voltage =

$$2.5\text{V}\left[\frac{1.2\text{M}//1.5\text{M}}{10\text{k}+1.2\text{M}//1.5\text{M}}-\frac{270\text{k}}{10\text{k}+270\text{k}}\right]=52.3\text{ mV}$$

It may be necessary to slow the transition of the logic pin if the mute circuit is not used. The forward and reverse preamplifier output DC voltages can differ by ±100 mV. This rapid DC charge is gained up by the output amplifier and appears as a pop. The circuit of *Figure 8* will slow the DC transition.

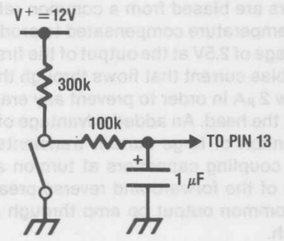


FIGURE 8. Circuit to Slow Logic

DESIGN EQUATIONS

The overall gain of the circuit is given by:

$$A_v = 25\left[\frac{-\text{R4R3}}{\text{R2(R3+R4)}}\right]\frac{\left(s+\dfrac{1}{\text{R4C1}}\right)}{\left(s+\dfrac{1}{\text{(R3+R4)C1}}\right)} \quad (1)$$

Standard cassette tapes require equalization of 3180 μs (50 Hz) and 120 μs (1.3 kHz). These time constants result in an AC gain at 1 kHz given by:

$$A_v(1\text{ kHz}) = 25\left(\frac{-\text{R4R3}}{\text{R2(R3+R4)}}\right)1.663\left\{\begin{matrix}3180\ \mu\text{s or } 50\text{ Hz}\\ \text{and}\\ 120\ \mu\text{s or } 1326\text{ Hz}\end{matrix}\right\} \quad (2)$$

Using the pole and zero locations of the transfer function, the two other equations needed to solve for the component values are:

$$\text{R4} = \frac{1}{2\pi\text{C1(1326 Hz)}} \quad (3)$$

$$\text{R3} = \frac{1}{2\pi\text{C1(50 Hz)}} - \frac{1}{2\pi\text{C1(1326 Hz)}} = \frac{1}{2\pi\text{C1(51.96)}} \quad (4)$$

We can now solve for C1 as a function of R2, or:

$$A_v(1\text{ kHz}) = -25\left\{\frac{\left[\dfrac{1}{2\pi\text{C1(1326)}}\right]\left[\dfrac{1}{2\pi\text{C1(51.96)}}\right]}{\left[\text{R2}\dfrac{1}{2\pi\text{C1(50)}}\right]}\right\}(1.663) \quad (5)$$

$$\text{C1} = \frac{-4.80\times10^{-3}}{\text{R2}[A_v\text{ (1 kHz)}]} \quad (6)$$

When chromium dioxide tape is used, the defined time constants are 3180 μs and 70 μs. This changes equation (3) to:

$$\text{R4} = \frac{1}{2\pi\text{C1(2274 Hz)}} \quad (7)$$

The value of R3 is normally not changed. This results in an error of less than 0.2 dB in the low frequency response.

The output voltage of the LM1837 is set by the input amplifier DC voltage at pin 5 or 14, and by R3 and R5.

$$\text{Nominal } V_{OUT}\text{(pin 2 or 17)} = 2.5\left(1+\frac{\text{R3}}{\text{R5}}\right) \quad (8)$$

Pins 1 and 18 are biased 0.7V less than V_{OUT} (pin 2 or 17). When these diodes are used the output (pin 2 or 17) should be biased at one half the minimum operating supply voltage. Equation (8) can be rewritten to solve for R5.

$$\text{R5} = \frac{2.5\text{ R3}}{V_O - 2.5} \quad (9)$$

The output voltage of the LM1837 will vary from that given in equation (8) due to variations in the input amplifier DC voltage as well as the output amplifier input bias current, input offset current and input offset voltage. The following equation gives the worst-case variation in the output voltage in either forward or reverse state.

$$\Delta V_{OUT} = \pm\left[\Delta V_{PIN\ 3}\left(1+\frac{\text{R3}}{\text{R5}}\right)+\frac{\text{R3}}{\text{R2}}\left(\Delta I_{BIAS}\text{(R1}-\text{R2)}+\frac{I_{OS}}{2}\text{(R1+R2)}+V_{OS}\right)\right] \quad (10)$$

Using the worst-case values in the electrical characteristics reduces this to

$$\Delta V_{OUT} = \pm\left[0.4\left(1+\frac{\text{R3}}{\text{R5}}\right)+\frac{\text{R3}}{\text{R2}}\ \text{(200 nA (R1}-\text{R2)}+\text{50 nA (R1+R2)}+5\text{ mV)}\right] \quad (11)$$

Equation 10 does not incorporate the effect of mute resistors on the output voltage. The presence of mute resistors causes an additional offset

$$\Delta V_{OUT}\text{(mute)} = \pm\frac{\Delta V\text{(pins 5–14)}}{2\text{(R1+R7)}}\times\text{R1} \quad (12)$$

For the circuit in *Figure 1* worst-case:

$$\Delta V_{OUT}\text{ (mute)} = \frac{400\text{ mV}}{2\text{(20k+270k)}}\times1.5\text{M} = 1\text{V}$$

This means that the output pins 2 and 17 would differ by 1V. The trade off here is the amount of unmute voltage versus the DC accuracy of pins 2 and 17.

The turn-on delay is set by R1 and C2; delay can be approximated by:

$$\text{Delay time t} = \text{R1C2}\,\ell n\left(\frac{2.5}{V_{ODC}}\right)\left(\frac{\text{R3}}{\text{R2}}\right) \quad (13)$$

Application Hints (Continued)

EXAMPLE

If we desire a tape preamp with 100 mV output signal from a tape head with a nominal output of 0.5 mV at 1 kHz for standard ferric cassette tape, the external components are determined as follows. The value of R2 is arbitrarily set to 10 kΩ.

$$R1 = R2 = 10k$$

This minimizes errors due to the output amplifier bias currents.

$$C1 = \frac{-4.80 \times 10^{-3}}{10\ k\Omega \left[\frac{-100\ mV}{0.5\ mV}\right]} = 2400\ pF - 0.0022\ \mu F$$

Use 0.0022 μF and determine:

$$R4 = \frac{1}{2\pi C1(1326)} = 54.6\ k\Omega - 54.9\ k\Omega\ 1\%$$

$$R3 = \frac{1}{2\pi C1(51.96)} = 1.39\ M\Omega - 1.4\ M\Omega\ 1\%$$

To bias the output amplifier output voltage at 6V (half supply):

$$R5 = \frac{2.5(1.4\ M\Omega)}{6 - 2.5} = 1\ M\Omega$$

The maximum variation in the output voltage is found using equation (11):

$$\Delta V_{OUT} = \pm 1.9V$$

The low frequency response and turn-on delay determine the value of C2. For R1 = 10k and C2 = 10 μF the low frequency 3 dB point is 1.6 Hz and the turn-on delay is 0.4 seconds, from equation (12).

The complete circuit is shown in *Figure 2*. A circuit with 5% components and biased for a minimum supply of 10V is shown in *Figure 1*. If additional gain is needed R1 and R2 can be reduced without changing the frequency response of the circuit.

DIODE SWITCHING

The LM1837 has a diode in series with each output for source switching applications. The outputs of several functional blocks can be diode OR-connected as shown in *Figure 9*.

By removing the power supply from the FM demodulator, its output diode will be cut off by the LM1837 output DC voltage. R6 is used to bias ON the diode of the LM1837 when power is applied to it. When the output is taken from pin 1 or pin 18, the THD will be higher because of the current modulation in the diode.

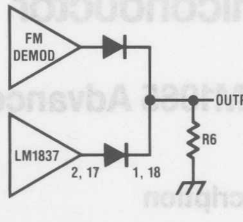


FIGURE 9

CROSSTALK AND CHANNEL SEPARATION

When two signal sources share a common reference point which is separated from ground by a resistance, there will always be some amount of interchannel crosstalk (the reciprocal of channel separation) induced. The coupling method of *Figure 1* is examined to determine whether the induced crosstalk is acceptably low.

Figure 10 is the equivalent AC circuit for the connection scheme of *Figure 1*. R_B is the Thevenin resistance of the common bias point, R_{IN} is the preamplifier input resistance, Z_S is the impedance of the playback head, and V_{S7}, V_{S8}, V_{S11}, and V_{S12} are the open-circuit output voltages of the sources. If we set V_{S8}, V_{S11}, and V_{S12} equal to zero, we can define crosstalk for this circuit as V12/V7, where V7 and V12 are the AC signal voltages appearing at the two preamplifier inputs, assuming $R_B << R_{IN}/3$.

The crosstalk can be shown to be:

$$\frac{V12}{V7} = \frac{R_B}{R_B + Z_S + R_{IN}/3}$$

Since Z_S is dependent on the measurement frequency and the particular head used, we choose the worst-case condition and set $Z_S = 0$. The minimum value of R_{IN} is 150 kΩ, and $R_B \cong 100\Omega$. This yields a crosstalk figure of:

$$\frac{V12}{V7} = \frac{100}{50100} = -54\ dB$$

This is 14 dB better than the minimum guaranteed channel separation, so the connection method of *Figure 1* will provide acceptable crosstalk levels.

Reference 1: CCIR/ARM: *A Practical Noise Measurement Method;* by Ray Dolby, David Robinson and Kenneth Gundry, AES Preprint No. 1353 (F-3).

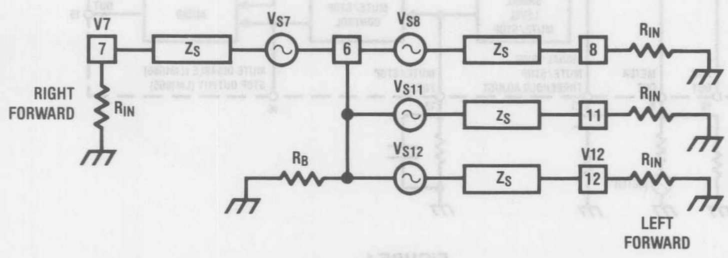


FIGURE 10. AC Equivalent of *Figure 1*

National Semiconductor

Audio/Radio Circuits
PRELIMINARY

LM1865/LM1965 Advanced FM IF System

General Description

Reduced external component cost, improved performance, and additional functions are key features to the LM1865/LM1965 FM IF system. The LM1865 is designed for use in electronically tuned radio applications. This version contains both deviation and signal level stop circuitry in addition to an open-collector stop output. The LM1965 is designed for use in manually tuned radios and provides a deviation and signal level mute function in addition to a pin that disables the mute function when grounded.

Features

- On-chip buffer to provide gain and terminate two ceramic filters
- Low distortion 0.1% typical with a single tuned quadrature coil
- Broad off frequency distortion characteristic
- Low THD at minimum AFT offset
- Meter output proportional to signal level
- Mute function with mute disable and soft deviation mute for LM1965
- Stop detector with open-collector output for LM1865
- Adjustable signal level mute/stop threshold, controlled either by ultrasonic noise in the recovered audio or by the meter output
- Adjustable deviation mute/stop threshold
- Separate time constants for signal level and deviation mute/stop
- Dual threshold AGC eliminates need for local/distance switch and offers improved immunity from third order intermodulation products due to tuner overload
- User control of both AGC thresholds
- Excellent signal to noise ratio, AM rejection and system limiting sensitivity

Block Diagram

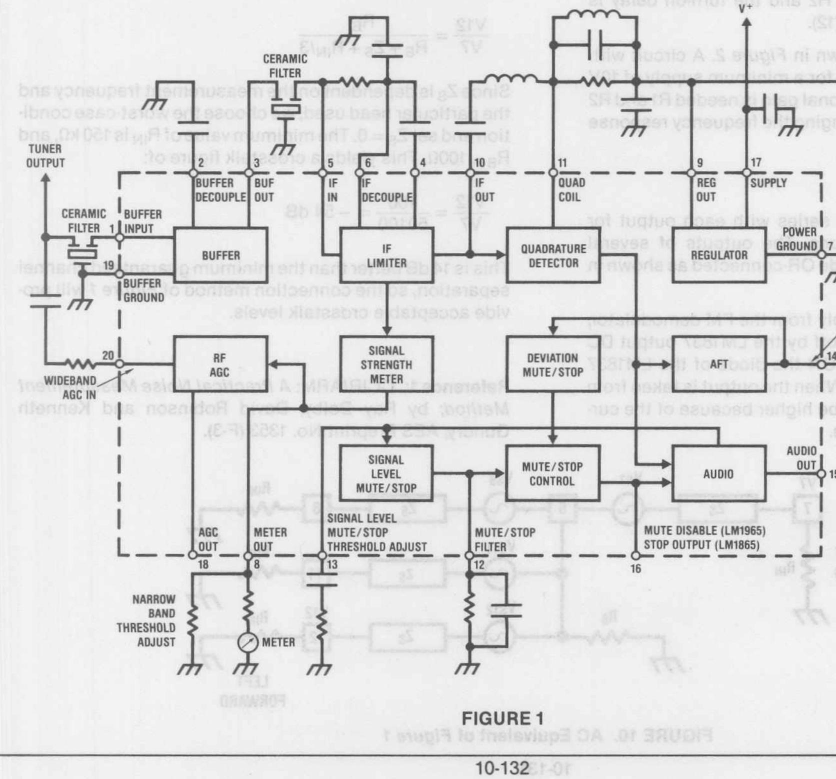


FIGURE 1

Package Dissipation (Note 1)	1.7W
Storage Temperature Range	−55°C to +150°C
Operating Temperature Range	0°C to +70°C
Max Voltage on Pin 16 (Stop Output) for LM1865	16V
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

Test Circuit, $T_A = 25°C$, $V^+ = 12V$; S1 in position 2; S2 in position 1; and S3 in position 2 unless indicated otherwise

Parameter	Conditions	Min	Typ	Max	Units
STATIC CHARACTERISTICS					
Supply Current			43		mA
Pin 9, Regulator Voltage			5.7		V
Operating Voltage Range	(See Note 2)	7.3		16	V
Pin 18, Output Leakage Current	Pin 20 Open, $V_{IF} = 0$, S3 in Position 1		0.1		μA
Pin 16, Stop Low Output Voltage (LM1865 Only)	S1 in Position 1, S2 in Position 3		0.3		V
Pin 16, Stop High Output Leakage Current (LM1865 Only)	S2 in Position 2, V14 = V9		0.1		μA
Pin 15, Audio Output Resistance			4.7		kΩ
Pin 1, Buffer Input Resistance	Measured at DC		350		Ω
Pin 3, Buffer Output Resistance	Measured at DC		350		Ω
Pin 20, Wide Band Input Resistance	Measured at DC		2		kΩ
Pin 8, Meter Output Resistance			760		Ω
DYNAMIC CHARACTERISTICS $f_{MOD} = 400$ Hz, $f_o = 10.7$ MHz, DEVIATION = ±75 kHz					
−3 dB Limiting Sensitivity	IF Only (See Note 3)		60		μVrms
Buffer Voltage Gain	V_{IN} Pin 1 = 10 mVrms at 10.7 MHz		26		dB
Recovered Audio	$V_{IF} = 10$ mVrms, V14 = V9		390		mVrms
Signal-to-Noise	$V_{IF} = 10$ mVrms, V14 = V9 (See Note 4)		84		dB
AM Rejection	V14 = V9 $V_{IF} = 1$ mV, 30% AM Mod $V_{IF} = 10$ mV, 30% AM Mod		 60 60		 dB dB
Minimum Total Harmonic Distortion	$V_{IF} = 10$ mV		0.1		%
THD at Frequency where V14 = V9 (Zero AFT Offset)	$V_{IF} = 10$ mV, Tune until V14 = V9		0.1		%
THD ±10 kHz from Frequency where V14 = V9	$V_{IF} = 10$ mV		0.15		%
AFT Offset Frequency for Deviation Mute (LM1965 Only)	$V_{IF} = 10$ mV, Audio = −3 dB, S2 in Position 4 Offset = (Frequency for −3 dB Audio) − (Frequency where V14 = V9)		±45		kHz
AFT Offset Frequency for Low Stop Output at Pin 16 (LM1865 Only)	$V_{IF} = 10$ mV, S2 in Position 3, $f_{MOD} = 0$ Offset = (Frequency for Pin 16 Low) − (Frequency where V14 = V9)		±40		kHz
Ultrasonic Mute/Stop Level Threshold	V14 = V9, S1 in Position 3 (See Note 5) $V_{IF} = 10$ mV $f_{MOD} = 80$ kHz S2 in Position 4 (LM1965) S2 in Position 3 (LM1865) Amount of Deviation where Audio Mutes (LM1965) Amount of Deviation where V16→12V (LM1865)		75		kHz

Electrical Characteristics (Continued) Test Circuit, $T_A = 25°C$, $V^+ = 12V$; S1 in position 2; S2 in position 1; and S3 in position 2 unless indicated otherwise

Parameter	Conditions	Min	Typ	Max	Units
DYNAMIC CHARACTERISTICS (Continued)	**$f_{MOD} = 400$ Hz, $f_o = 10.7$ MHz, DEVIATION = ± 75 kHz**				
Pin 13 Mute/Stop Threshold Voltage	V14 = V9, S1 in Position 4 S2 in Position 4 (LM1965) S2 in Position 3 (LM1865) V13 where Audio Mutes (LM1965) V13 where V16 → 12V (LM1865)		220		mV
Amount of Muting (LM1965 Only)	S2 in Position 4, S1 in Position 1, $V_{IF} = 10$ mV		66		dB
Amount of Muting with Pin 13 and Pin 16 Grounded	S1 in Position 1 V14 = V9, $V_{IF} = 10$ mV		0	0	dB
Narrow Band AGC Threshold	Increase IF Input until $I_{AGC} = 0.1$ mA Pin 20 = 30 mVrms		200		μVrms
Wide Band AGC Threshold	$V_{IF} = 100$ mVrms Increase Signal to Pin 20 until $I_{AGC} = 0.1$ mA		9		mVrms
Pin 18, Low Output Voltage	V_{IN} Pin 20 = 100 mV, $V_{IF} = 100$ mVrms		0.3		V
Pin 8, Meter Output Voltage	$V_{IF} = 10\ \mu V$ $V_{IF} = 300\ \mu V$ $V_{IF} = 3$ mV		0.1 1.1 2.6		V V V

Note 1: Above $T_A = 25°C$ derate based on $T_{J(max)} = 150°C$ and $\theta_{JA} = 75°C/W$.

Note 2: All data sheet specifications are for $V^+ = 12V$ and may change slightly with supply.

Note 3: When the IF is preceded by 26 dB gain in the buffer, excellent system sensitivity is achieved.

Note 4: Measured with a notch at 60 Hz and 20 Hz to 100 kHz bandwidth.

Note 5: FM modulate RF source with an 80 kHz audio signal and find what modulation level, expressed as kHz deviation, results in audio mute for the LM1965 or V16 → 12V for the LM1865.

Test Circuit

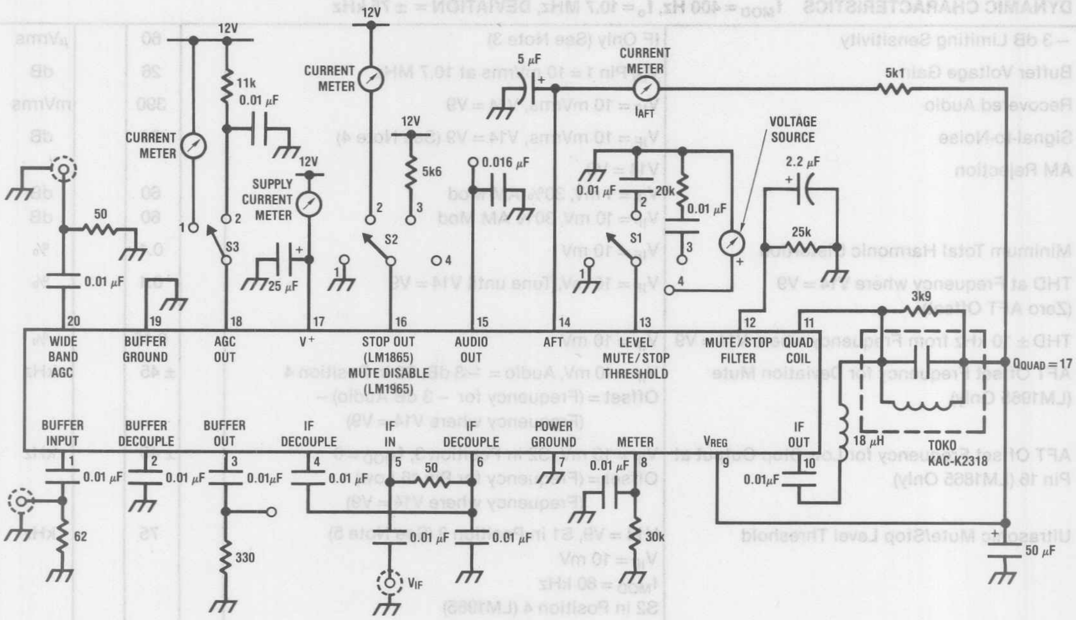
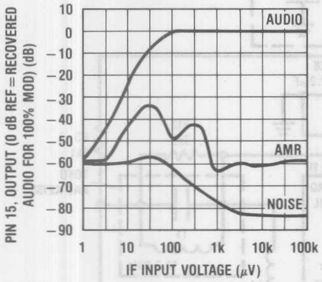


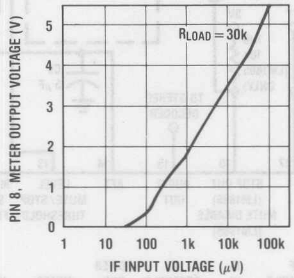
FIGURE 2

Typical Performance Characteristics (from Test Circuit)

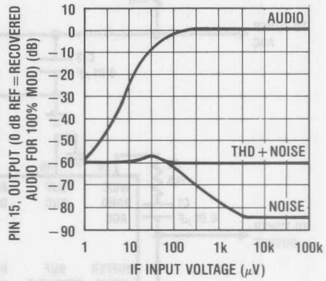
FM Limiting Characteristics and AM Rejection



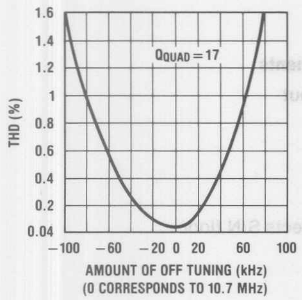
Pin 8, Meter Output Voltage vs IF Input Level



FM Limiting Characteristics + THD

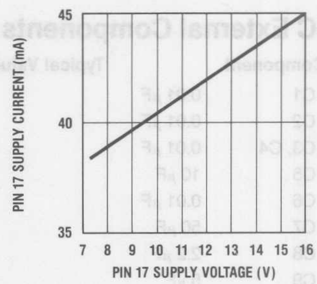


% THD vs OFF Tuning (Single Tuned Quadrature Coil)

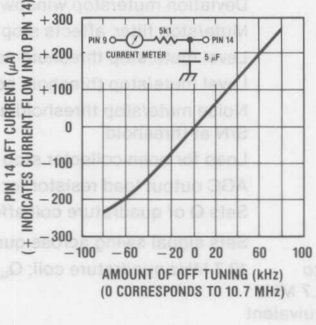


Deviation Mute/Stop Threshold as a Function of AFT Load Resistor

Supply Current vs Supply Voltage



Pin 14, AFT Current vs Tuning



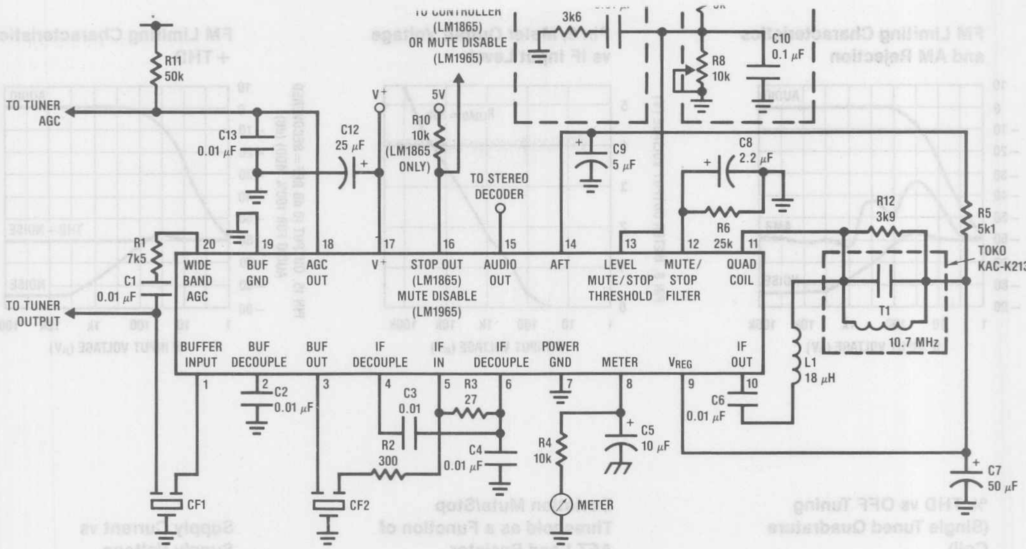
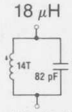


FIGURE 3

IC External Components (see Application Circuit)

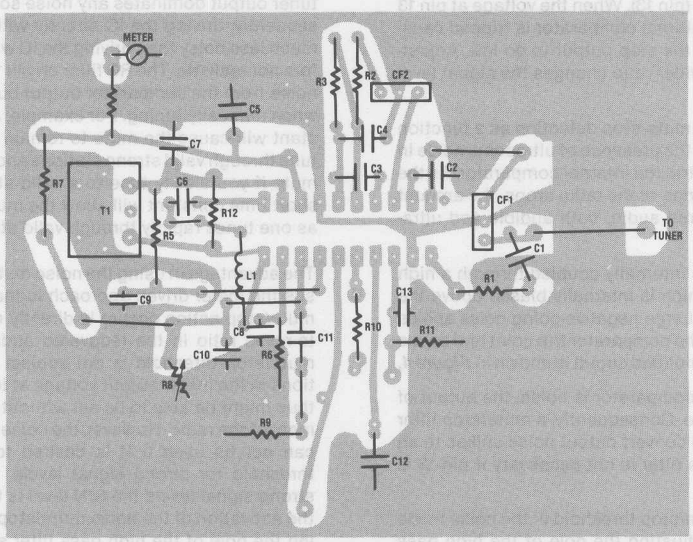
Component	Typical Value	Comments
C1	0.01 μF	AC coupling for wide band AGC input
C2	0.01 μF	Buffer and AGC supply decoupling
C3, C4	0.01 μF	IF decoupling capacitors
C5	10 μF	Meter decoupling capacitor
C6	0.01 μF	AC coupling for IF output
C7	50 μF	Regulator decoupling capacitor, affects S/N floor
C8	2.2 μF	Level mute/stop time constant
C9	5 μF	AFT decoupling, affects stop time
C10	0.1 μF	Disables noise mute/stop
C11	0.01 μF	AC coupling for noise mute/stop threshold adjust
C12	25 μF	Supply decoupling
C13	0.01 μF	AGC output decoupling capacitor
R1	Tuner Dependent	Wide band AGC threshold adjust
R2, R3	Tuner Dependent	Gain set and bias for IF; R2 + R3 = 330Ω to terminate ceramic filter
R4	Meter Dependent	Sets full-scale on meter
R5	5k1	Deviation mute/stop window adjustment
R6	25k	Mute/stop filter, affects stop time
R7	5k	Level mute/stop threshold adjustment
R8	10k Pot	Level mute/stop threshold adjustment
R9	3k6	Noise mute/stop threshold adjustment, decrease resistor for lower S/N at threshold
R10	10k	Load for open-collector stop output
R11	50k	AGC output load resistor for open-collector output
R12	3k9	Sets Q of quadrature coil affecting THD, S/N and recovered audio
L1	18 μH	Sets signal swing across quadrature coil
T1	 $Q_U > 70$ @ 10.7 MHz, L to resonate w/82 pF @ 10.7 MHz TOKO KAC-K2318 or equivalent	10.7 MHz quadrature coil; $Q_{UL} > 70$
CF1, CF2	MuRata SFE10.7ML or equivalent	10.7 MHz ceramic resonators provide selectivity; good group delay characteristics important for low THD of system

Typical Application

LAYOUT CONSIDERATIONS

Although the pinout of the LM1865/LM1965 has been chosen to minimize layout problems, some care is required to insure stability. The ground terminal on CF1 should return to both the input signal ground and the buffer ground, pin 19. The ground terminal on CF2 should return to the ground side of C4. The quadrature coil T1 and inductor L1 should be separated from the input circuitry as far as possible.

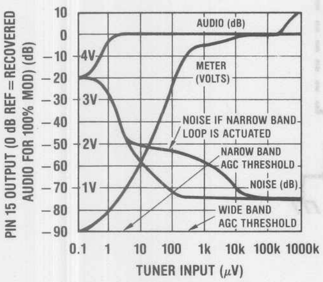
PC Layout (Component Side)



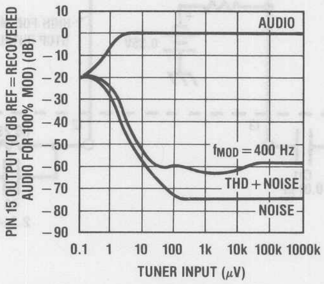
PERFORMANCE CHARACTERISTICS OF TYPICAL APPLICATION WITH TUNER

The following data was taken using the typical application circuit in conjunction with an FM tuner with 43 dB of gain, a 5.5 dB noise figure, and 30 dB of AGC range. The tuner was driven from a 50Ω source. 75 μs of de-emphasis was used on the audio output, pin 15. The 0 dB reference is for ±75 kHz deviation at 400 Hz modulation.

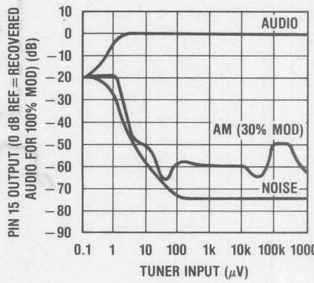
Meter Output and Signal-to-Noise vs Tuner Input



Total Harmonic Distortion vs Tuner Input



AM Rejection vs Tuner Input



−3 dB limiting = 0.9 μV

30 dB quieting = 1.4 μV

Level stop/mute threshold = 1.4 μV

Deviation mute window (−3 dB) = ±45 kHz

Application Notes

ADJUSTABLE MUTE/STOP THRESHOLD

The threshold adjustments for the mute and stop functions are controlled by the same pins. Thus, the term mute/stop will be used to designate either function.

The adjustable mute/stop threshold in the LM1865/LM1965 allows for user programming of the signal level at which muting or stop indication takes place. The adjustment can be made in two mutually exclusive ways. The first way is to take a voltage divider from the meter output (pin 8) to the off channel mute input (pin 13). When the voltage at pin 13 falls below 0.22V, an internal comparator is tripped causing muting or causing the stop output to go low. Adjustment of the voltage divider ratio changes the signal level at which this happens.

The second method of mute/stop detection as a function of signal level is to use the presence of ultrasonic noise in the recovered audio to trip the internal comparator. As the signal level at the antenna of the radio drops, the amount of noise in the recovered audio, both audible and ultrasonic, increases.

The recovered audio is internally coupled through a high pass filter to pin 13 which is internally biased above the comparator trip point. Large negative-going noise spikes will drive pin 13 below the comparator trip point and cause mute/stop action. A simplified circuit is shown in *Figure 4*.

Since the input to the comparator is noise, the output of the comparator is noise. Consequently, a mute/stop filter on pin 12 is required to convert output noise spikes to an average DC value. This filter is not necessary if pin 13 is driven from the meter.

Adjustment of the mute/stop threshold in the noise mode is accomplished by adjusting the pole of the high pass filter coupled to the comparator input. This is done with a series capacitor/resistor combination, R9 C11, from pin 13 to ground. As the pole is moved higher in frequency (i.e., R9 gets smaller) more ultrasonic noise is required in the recovered audio in order to initiate mute/stop action. This corresponds to a weaker signal at the antenna of the radio. In choosing the correct value for R9 it is important to make sure that recovered audio below 75 kHz is not sufficient to cause mute/stop action. This is because stereo and SCA information are contained in the audio signal up to 75 kHz. Also note that the ultrasonic mute/stop circuit will not operate properly unless a tuner is connected to the IF. This is because, at low signal levels, the noise at the tuner output dominates any noise sources in the IC. Consequently, driving the IC directly with a 50Ω generator is much less noisy than driving the IC with a tuner and therefore not realistic. The RC filter on pin 12 not only filters out noise from the comparator output but controls the "feel" when manually tuning. For example, a very long time constant will cause the mute to remain active if you rapidly tune through valid strong stations and will only release the mute if you slowly tune to a valid station. Conversely, a short time constant will allow the mute to kick in and out as one tunes rapidly through valid stations.

The advantage in using the noise mute/stop approach versus the meter driven approach is that the point at which mute/stop action occurs is directly related to the signal-to-noise ratio in the recovered audio. Furthermore, the mute/stop threshold is not subject to production variations in the meter output voltage at low signal levels, and thus might be able to be set without a production adjustment of the radio. However, the noise mute/stop approach can not be used if it is desired to set the mute/stop threshold for strong signal levels. This is because for strong signal levels the S/N level is too large to allow for the activation of the noise mute/stop circuit without moving the pole of the high pass filter so low that the noise mute/stop circuit becomes sensitive to recovered audio below 75 kHz. Thus, for setting the mute/stop threshold for strong signal levels, the meter driven approach is best.

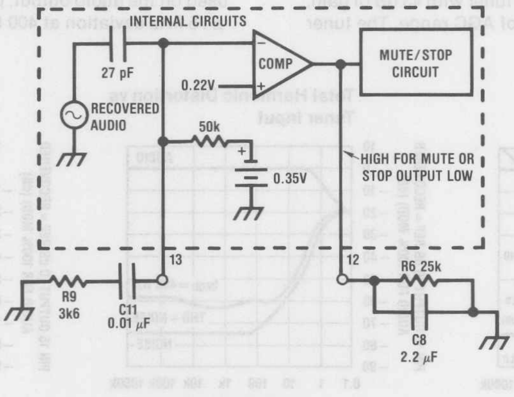


FIGURE 4. Simplified Level Mute/Stop Circuit

Application Notes (Continued)

DEVIATION MUTE/STOP

As with the LM3189, the resistor connected between V_{REG} (pin 9) and the AFT (pin 14) sets the deviation mute/stop window (see Typical Performance Characteristics). The LM1965 was designed with a soft deviation mute. This means that the audio is gradually muted as you off tune from center frequency. Gradually muting avoids the problem of an audio pop which would otherwise occur due to the unavoidable DC voltage shift at the audio output that accompanies the muting action. Capacitor C9 on the AFT pin sets the time constant for the deviation mute/stop independent of the level mute/stop time constant. C9 should be large enough to remove the audio from the AFT. The AFT pulls high at low signal levels if the IF is driven directly from a 50Ω generator and not a tuner. This is a result of a loss of signal across the quad coil and a resulting phase shift in the quadrature detector. This phase shift offsets the AFT. With a tuner and sufficient IF gain, at low signal levels there will be enough noise across the quad coil to prevent much of this AFT shift. Thus, care should be taken when adjusting the IF gain (which is done by adjusting the ratio of R3 to R2) to minimize the AFT shift. Grounding pin 16 on the LM1965 will disable the mute function.

STOP TIME

An electronically tuned radio (ETR) pauses at fixed intervals across the FM band and awaits the stop indication from the LM1865. If, within a predetermined period of time, no stop indication is forthcoming, the controller circuit concludes that there is no valid station at that frequency and will tune to the next interval. There are several time constants that can affect the amount of time it takes the LM1865 to output a valid stop indication on pin 16. In this section each time constant will be discussed.

Deviation Stop Time Constant

An offset voltage is generated by the AFT if the LM1865 is tuned to either side of a station. Since deviation stop detection in the LM1865 is detected by the voltage at pin 14, it is important that this voltage move fast enough to make the deviation stop decision within the time allowed by the controller. The speed at which the voltage at pin 14 moves is governed by the RC time constant, R5 C9. This time constant must be chosen long enough to remove recovered audio from pin 14 and short enough to allow for reasonable stop detection time.

Signal Level Stop Using Ultrasonic Noise Detection

As previously mentioned, the R6 C8 time constant on pin 12 is necessary to filter the noise spikes on the output of the internal comparator in the LM1865/LM1965. This time constant also determines the level stop time. When the voltage at pin 12 is above a threshold voltage of about 0.6V, the stop output is low. The maximum voltage at pin 12 is about 0.8V. The level stop time is dominated by the amount of time it takes the voltage at pin 12 to fall from 0.8V to 0.6V. The voltage at pin 12 follows an exponential decay with RC time constant given by R6 C8. For example if R6 = 25k and C8 = 2.2 μF the stop time is given by

$$t = -(24k)\,(2.2\ \mu F)\ \ell n\left(\frac{0.6}{0.8}\right)$$

which yields t = 15 ms. It should be noted that the 0.6V threshold at pin 12 has a high temperature dependence and can move as much as 100 mV in either direction.

Signal Level Stop Using the Meter Output, Pin 8

As mentioned previously, R6 C8 is not necessary when the meter output is used to drive pin 13. Consequently, this time constant is not a factor in determining the stop time. However, the speed at which the meter voltage can move may become important in this regard. This speed is a function of the resistive load on pin 8 and filter capacitance, C5.

AGC Time Constant

In tuning from a strong station to a weaker station above the level stop threshold, the AGC voltage will move in order to try to maintain a constant tuner output. The AGC voltage must move sufficiently fast so that the tuner is gain increased to the point that the level stop indicates a valid station. This time constant is controlled by R11 and C13.

DISTORTION COMPENSATION CIRCUIT

The quadrature detector of the LM1865/LM1965 has been designed with a special circuit that compensates for distortion generated by the non-linear phase characteristic of the quadrature coil. This circuit not only has the effect of reducing distortion, but also desensitizes the distortion as a function of tuning characteristic. As a result, low distortion is achieved with a single tuned quad coil without the need for a double tuned coil which is costly and difficult to adjust on a production basis. The lower distortion has been achieved without any degradation of the noise floor of the audio output. Furthermore, the compensation circuit first-order cancels the effect of quadrature coil Q on distortion.

When measuring the total harmonic distortion (THD) of the LM1865/LM1965, it is imperative that a low distortion RF generator be used. In the past it has been possible to cancel out distortion in the generator by adjustment of the quadrature coil. This is because centering the quadrature coil at other than the point of inflection on the S-curve introduces 2nd harmonic distortion which can cancel 2nd harmonic distortion in the generator. Thus low THD numbers may have been obtained wrongly. Large AFT offsets, asymmetrical off tuning characteristic, and less than minimum THD will be observed if alignment of the quadrature coil is done with a high distortion RF generator.

Care must also be taken in choosing ceramic filters for the LM1865/LM1965. It is important to use filters with good group delay characteristics and wide enough bandwidth to pass enough FM sidebands to achieve low distortion.

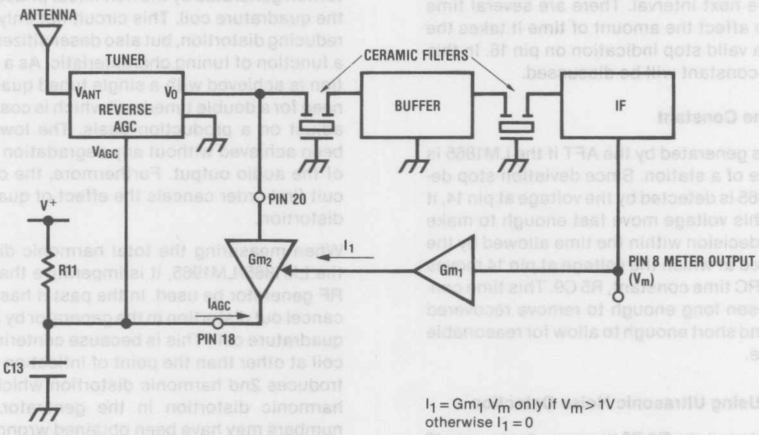
low AFT offset current at the point of minimum THD. AFT offset currrent will cause a non-symmetric deviation mute/stop window about the point of minimum THD. No external AFT offset adjustment should be necessary with the LM1865/LM1965.

DUAL THRESHOLD AGC (AUTOMATIC LOCAL/DISTANCE SWITCH)

There is a well recognized need in the field for gain reducing (AGCing) the front end (tuner) of an FM receiver. This gain reduction is important in preventing overload of the front end which might occur for large signal inputs. Overloading the front end with two out-of-band signals, one channel spacing apart and one channel spacing from center frequency, or, two channel spacings apart and two channel spacings from center frequency, will produce a third order intermodulation product (IM_3) which falls in-band. This IM_3 product can completely block out a weaker desired station. The AGC in the LM1865/LM1965 has been specially designed to deal with the problem of IM_3.

With the LM1865/LM1965 system, a low AGC threshold is achieved whenever there are strong out-of-band signals that might generate an interfering IM_3 product, and a high AGC threshold is achieved if there are no strong out-of-band signals. The high AGC threshold allows the receiver to obtain its best signal-to-noise performance when there is no possibility of an IM_3 product. The low AGC threshold allows for weaker desired stations to be received without gain-reducing the tuner. It should be noted that when the AGC threshold is set low, there will be a signal-to-noise compromise, but is assumed that it is more desirable to listen to a slightly noisy station than to listen to an undesired IM_3 product. The simplified circuit diagram *(Figure 5)* of the AGC system shows how the dual AGC thresholds are achieved.

$V_m = 1V$ corresponds to a fixed in-band signal level (defined as V_{NB}) at the tuner output. V_{NB} will be referred to as the "narrow band threshold". V_{WB} also corresponds to a fixed tuner output which can either be an in-band or out-of-band signal. This fixed tuner output will be called the "wide band threshold". Always $V_{WB} > V_{NB}$. R11 and C13 define the AGC time constant. A reverse AGC system is shown. This means that V_{AGC} decreases to gain-reduce the tuner. The LM1865/LM1965 AGC output is an open-collector current source capable of sinking at least 1 mA. The AGC voltage can move over the full range of the V^+ supply.



$I_1 = Gm_1 V_m$ only if $V_m > 1V$
otherwise $I_1 = 0$

Gm_1, V_{WB} = constants

$I_{AGC} = Gm_2 V_o$ where $Gm_2 = I_1/26$ mV *and*
$V_o > V_{WB}$ otherwise $I_{AGC} = 0$

FIGURE 5. Dual Threshold AGC

Applications Information (Continued)

First examine what happens with a single in-band signal as we vary the strength of this signal. *Figures 6 and 7* illustrate what happens at the tuner and AGC outputs.

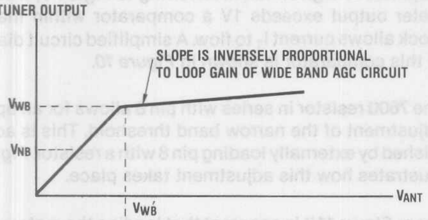


FIGURE 6

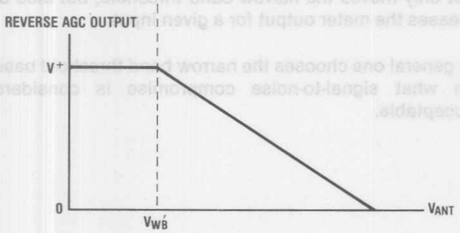


FIGURE 7

In *Figure 7* there is no AGC output until the tuner output equals the wide band threshold. At this point the AGC holds the tuner output in *Figure 6* relatively constant.

Another simple case to examine is that of the single out-of-band signal. Here there is no AGC output even if the signal exceeds V_{WB}. There is no output because the ceramic filters prevent the out-of-band signal from getting to the input of the IF. With no signal at the IF input there is no meter output and thus $I_1=0$, which means $I_{AGC}=0$.

Figures 8 and 9 illustrate what happens at the tuner and AGC outputs when the strength of an in-band signal is varied in the presence of a strong out-of-band signal (i.e., greater than V_{WB}) which is held constant at the tuner input. For this example, the in-band signal at the tuner output will be referred to as V_D (desired signal), and the out-of-band signal as V_{UD} (undesired signal).

In *Figure 9*, we see that there is no AGC output until the tuner output exceeds the narrow band threshold, V_{NB}. At this point $V_m > 1V$ and current $I_1 > 0$. Further increase of the desired signal at the tuner input results in an AGC current that tries to hold the desired signal at the tuner output constant. This gain reduction of the tuner forces the undesired signal at the tuner output to fall. At the point that V_{UD} reaches the wide band threshold, no further gain reduction can occur as V_o would fall below V_{WB} (refer to *Figure 5*). At this point, control of the AGC shifts from the meter output (narrow band loop) to the out-of-band signal (wide band loop). Here V_{UD} is held constant along with the

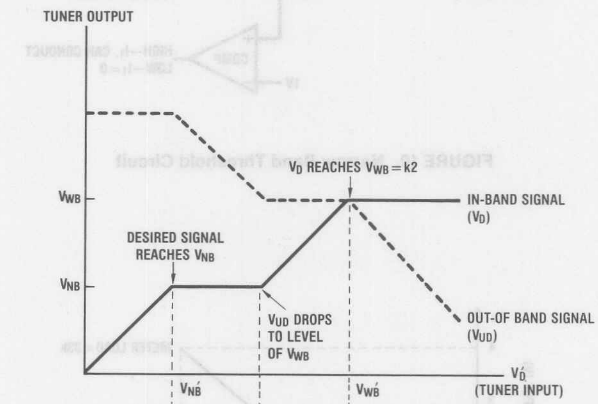
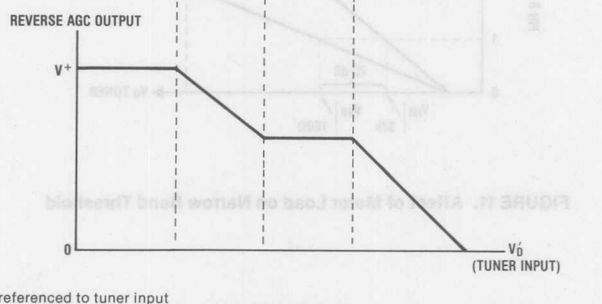


FIGURE 8



Prime indicates referenced to tuner input

FIGURE 9

Applications Information (Continued)

AGC voltage, while V_D is allowed to increase. V_D will increase until it reaches the level of the wide band threshold at the tuner output. When this occurs V_{UD} is no longer needed to keep $V_o > V_{WB}$ as V_D takes over the job. Thus V_{UD} will drop as the amount of AGC increases, while V_D is held constant by the AGC.

When compared to the simple case of a single in-band signal, we see that because of the presence of a strong out-of-band signal, AGC action has occurred earlier. For the simple case, AGC started when $V_D \geq V_{WB}$. For the two signal case above, AGC started when $V_D \geq V_{NB}$. Thus, the LM1865/LM1965 achieves an early AGC when there are strong adjacent channels that might cause IM_3, and a later AGC when these signals aren't present.

For the range of signal levels that the tuner was gain-reduced and $V_D < V_{WB}$ there was loss in signal-to-noise in the recovered audio as compared to the case where there was no gain reduction in this interval. *Note, however, that the tuner is not desensitized by the AGC to weak desired stations below the narrow band threshold.*

NARROW BAND AGC THRESHOLD ADJUSTMENT

Both the narrow band and wide band AGC thresholds are user adjustable. This allows the user to optimize the AGC response to a given tuner. Referring to *Figure 5*, when the meter output exceeds 1V a comparator within the Gm_1 block allows current I_1 to flow. A simplified circuit diagram of this comparator is shown in *Figure 10*.

The 760Ω resistor in series with pin 8 allows for an upward adjustment of the narrow band threshold. This is accomplished by externally loading pin 8 with a resistor. *Figure 11* illustrates how this adjustment takes place.

From *Figure 11* it is apparent that loading the meter output not only moves the narrow band threshold, but also decreases the meter output for a given input.

In general one chooses the narrow band threshold based on what signal-to-noise compromise is considered acceptable.

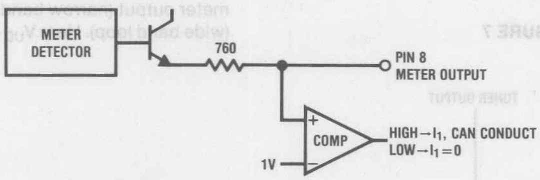


FIGURE 10. Narrow Band Threshold Circuit

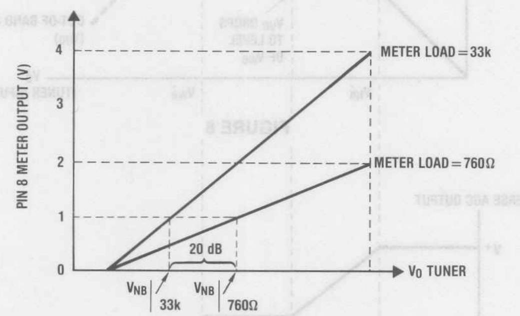


FIGURE 11. Affect of Meter Load on Narrow Band Threshold

Applications Information (Continued)

WIDE BAND AGC THRESHOLD ADJUSTMENT

There are a number of criteria that determine where the wide band threshold should be set. If the threshold is set too high, protection against IM_3 will be lost. If the threshold is set too low, the front end, under certain input conditions, may be needlessly gain-reduced, sacrificing signal-to-noise performance. Ideally, the wide band threshold should be set to a level that will insure AGC operation whenever there are out-of-band signals strong enough to generate an IM_3 product of sufficient magnitude to exceed the narrow band threshold. Ideally, this level should be high enough to allow for a single in-band desired station to AGC the tuner, only after the maximum signal-to-noise has been achieved.

In order to insure that the wide band loop is activated whenever the IM_3 exceeds the narrow band threshold, V_{NB}, determine the minimum signal levels for two out-of-band signals necessary to produce an IM_3 equal to V_{NB}. Then, arrange for the wide band loop to be activated whenever the tuner output exceeds the rms sum of these signals. There are many combinations of two out-of-band signals that will produce an IM_3 of a given level. However, there is only one combination whose rms sum is a minimum at the tuner output. IM_3 at the tuner output is given according to the equation:

$$IM_3 = aV_{UD1}^2\ V_{UD2} \quad \text{(assuming no gain reduction)} \qquad (1)$$

where a = constant dependent on the tuner;

V_{UD1} = out-of-band signal 400 kHz from center frequency, applied to tuner input;

V_{UD2} = out-of-band signal 800 kHz from center frequency and 400 kHz away from V_{UD1}, applied to tuner input.

In general, due to tuned circuits within the tuner, the tuner gain is not constant with frequency. Thus, if the tuner is kept fixed at one frequency while the input frequency is changed, the output level will not remain constant. *Figure 12* illustrates this.

It can be shown that for a given IM_3, the combination of V_{UD1} and V_{UD2} that produces the smallest rms sum at the tuner output is given by the equations:

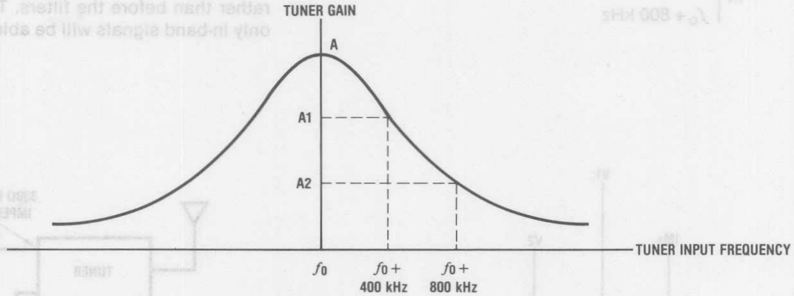
$$V_{UD1} = 1.12\left(\frac{A2}{A1}\,\frac{IM_3}{a}\right)^{1/3} \qquad (2)$$

$$V_{UD2} = 0.794\left(\frac{A1^2}{A2^2}\,\frac{IM_3}{a}\right)^{1/3} \qquad (3)$$

Therefore, in order to guarantee that the AGC will be keyed for an $IM_3 = V_{NB}$ we need only satisfy the condition:

$$V_{WB} \leq \sqrt{V_{NB}^2 + \left[(A1)(1.12)\left(\frac{A2}{A1}\,\frac{V_{NB}}{a}\right)^{1/3}\right]^2 + \left[A2\,(0.794)\left(\frac{A1^2}{A2^2}\,\frac{V_{NB}}{a}\right)^{1/3}\right]^2} \qquad (4)$$

The right hand term of equation (4) defines an upper limit for V_{WB} called V_{WBUL}. V_{WBUL} is the rms sum of all the signals at the tuner output for two out-of-band signals, V_{UD1} and V_{UD2} [as expressed in equations (2) and (3)], applied to the tuner input.



Define A = tuner gain at center frequency

A1 = tuner gain at f_O + 400 kHz

A2 = tuner gain at f_O + 800 kHz

FIGURE 12

In order to make the calculation in equation (4), the constants a, A1, A2 must first be determined. This is done by the following procedure:

1. Connect together two RF generators and apply them to the tuner input. Since the generators will terminate each other, remove the 50Ω termination at the tuner input.
2. Connect a spectrum analyzer to the tuner output. Most spectrum analyzers have 50Ω input impedances. To make sure that this impedance does not load the tuner output use a FET probe connected to the spectrum analyzer. The tuner output should be terminated with a ceramic filter.
3. Disconnect the AGC line to the tuner. Make sure that the tuner is not gain-reduced.
4. Adjust the two RF generators for about 1 mV input and to frequencies 400 kHz and 800 kHz away from center frequency *(Figure 13)*.
5. Note the three output levels in volts.
6. Knowing the tuner input levels for V_{UD1} and V_{UD2} and the resulting IM_3 just measured, "a" is calculated from the formula:

$$a = \frac{IM_3}{V_{UD1}{}^2 V_{UD2}} \tag{5}$$

where all levels are in volts rms. A typical value for "a" might be 2×10^6.

7. A1 and A2 are calculated according to the following formulas:

$$A1 = \frac{V1}{V_{IN}\Big|_{f_o + 400\ kHz}} \tag{6}$$

$$A2 = \frac{V2}{V_{IN}\Big|_{f_o + 800\ kHz}} \tag{7}$$

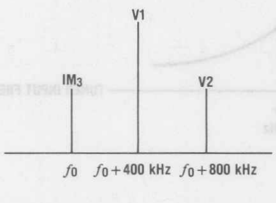


FIGURE 13. Spectrum Analyzer Display of Tuner Output

If the wide band threshold was set to V_{WBUL}, then when a single in-band station reached the level V_{WBUL} at the tuner output, AGC action would start to take place. For this reason it is hoped that V_{WBUL} is above the level that will allow for maximum signal-to-noise. If, however, this is not the case, consideration might be given to improving the intermodulation performance of the tuner.

The lower limit for V_{WB} is the minimum tuner output that achieves the best possible signal-to-noise ratio in the recovered audio. In general, it is desirable to set V_{WB} closer to the upper limit rather than the lower limit. This is done to prevent AGC action within the narrow band loop except when there is a possibility of an IM_3 greater than V_{NB}.

The wide band threshold at the pin 20 input to the LM1865/LM1965 is fixed at 9 mVrms. Generally speaking, if pin 20 were driven directly from the tuner output, V_{WB} would be too low. Therefore, in general, pin 20 is not connected directly to the tuner output. Instead the tuner output is attenuated and then applied to pin 20. Increasing attenuation increases the wide band threshold, V_{WB}.

Pin 20 has an input impedance at 10.7 MHz that can be modeled as a 500Ω resistor in series with a 19 pF capacitor, giving a total impedance of 940Ω $\angle -58°$. Thus an easy way to attenuate the input to pin 20 is with the arrangement shown in *Figure 14*.

Notice that pin 20 must be AC coupled to the tuner output and that C1 is a bypass capacitor. R1 adjusts the amount of attenuation to pin 20. The wide band threshold will roughly increase by a factor of (R1 + 940Ω)/940Ω.

AGC CIRCUIT USED AS A CONVENTIONAL AGC

If for some reason the dual AGC thresholds are not desired, it is easy to use the LM1865/LM1965 as a more conventional LM3189 type of AGC. This is accomplished by AC coupling the pin 20 input after the ceramic filters rather than before the filters. Thus, as with the LM3189, only in-band signals will be able to activate the AGC.

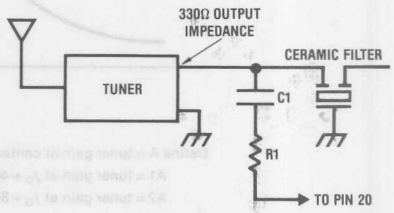
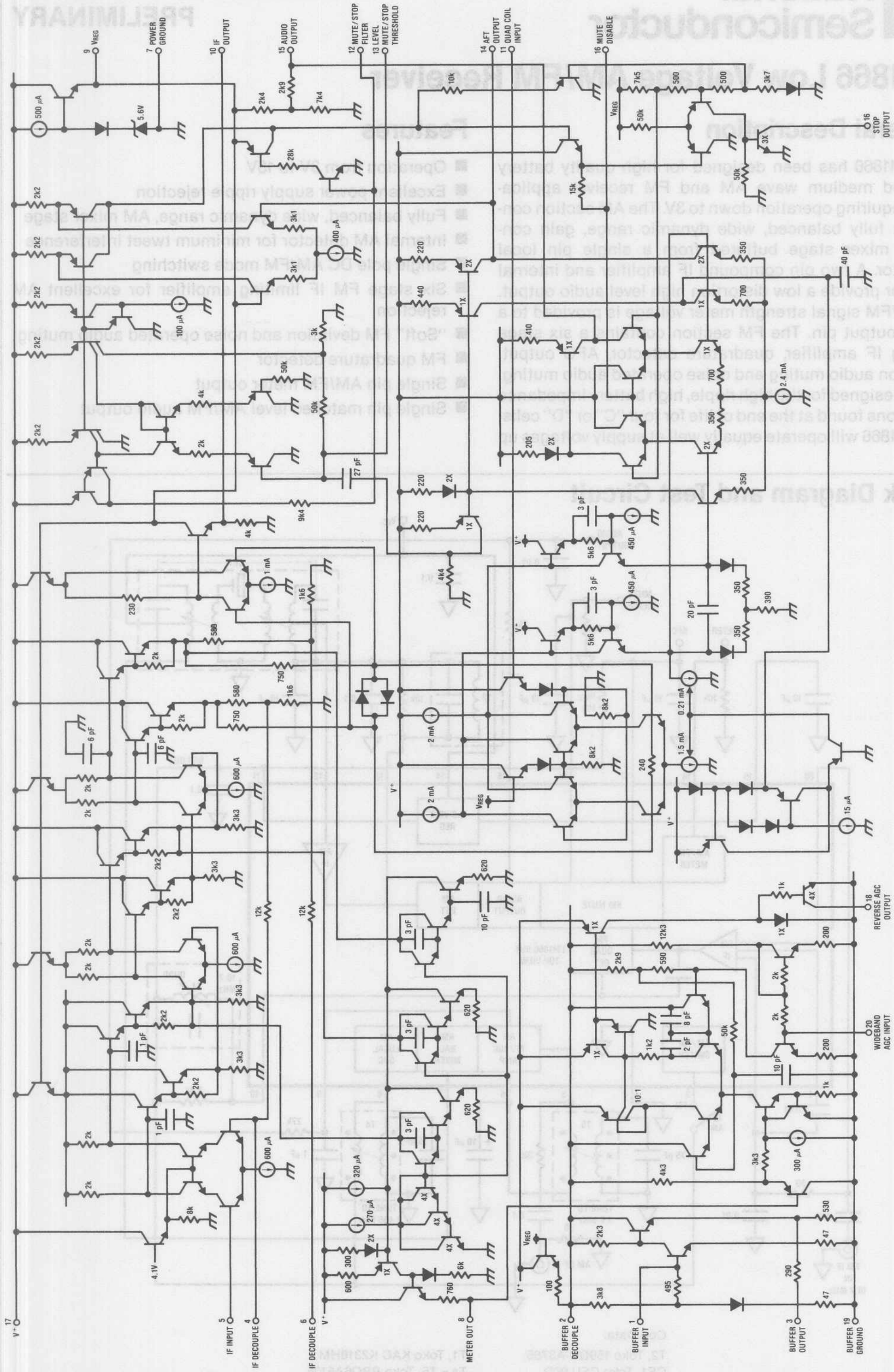


FIGURE 14. Wide Band Threshold Adjustment

Simplified Diagram



National Semiconductor

Audio/Radio Circuits
PRELIMINARY

LM1866 Low Voltage AM/FM Receiver

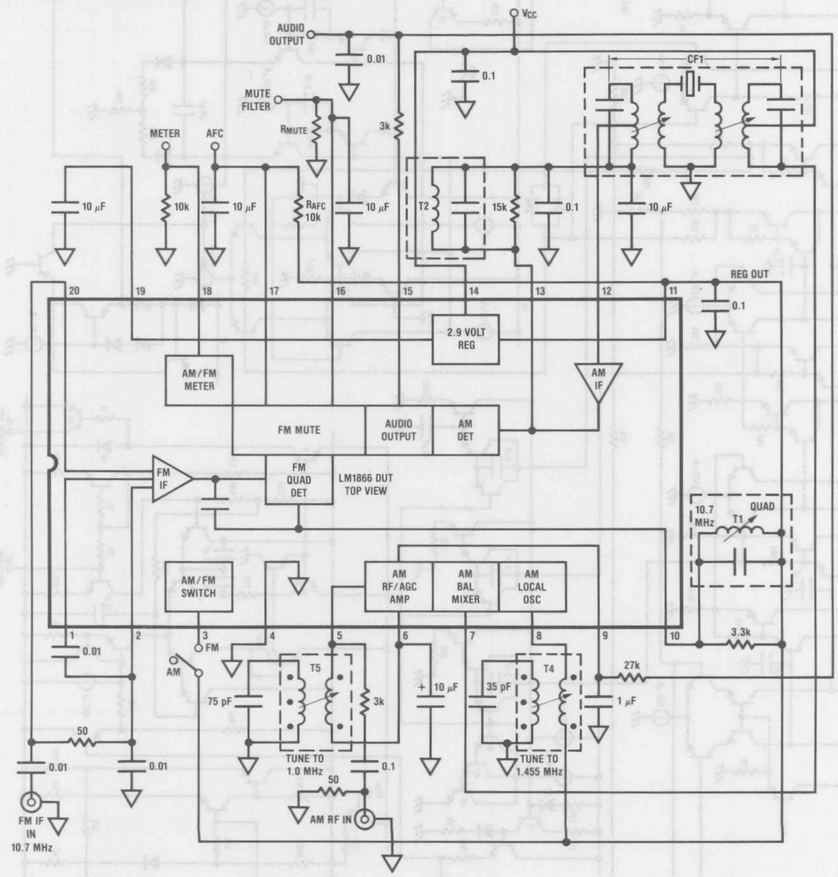
General Description

The LM1866 has been designed for high quality battery powered medium wave AM and FM receiver applications requiring operation down to 3V. The AM section contains a fully balanced, wide dynamic range, gain controlled mixer stage buffered from a single pin local oscillator. A two pin compound IF amplifier and internal detector provide a low distortion high level audio output. An AM/FM signal strength meter voltage is provided to a single output pin. The FM section contains a six stage limiting IF amplifier, quadrature detector, AFC output, deviation audio muting and noise operated audio muting. While designed for the high ripple, high battery impedance conditions found at the end of life for four "C" or "D" cells, the LM1866 will operate equally well at supply voltages up to 15V.

Features

- Operation from 3V to 15V
- Excellent power supply ripple rejection
- Fully balanced, wide dynamic range, AM mixer stage
- Internal AM detector for minimum tweet interference
- Single pole DC AM/FM mode switching
- Six stage FM IF limiting amplifier for excellent AM rejection
- "Soft" FM deviation and noise operated audio muting
- FM quadrature detector
- Single pin AM/FM meter output
- Single pin matched level AM/FM audio output

Block Diagram and Test Circuit



Coil Data:

T2, Toko 159GC-A3785
CF1, Toko CFU-90D

T1, Toko KAC K2318HM
T4 = T5, Toko RBO6A5105

LM1866

Absolute Maximum Ratings

Supply Voltage (Pin 14)	15V
Package Dissipation (Note 1)	1.7W
Storage Temperature Range	$-55°C$ to $+150°C$
Operating Temperature Range	$0°C$ to $+70°C$
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Test Circuit, $T_A = 25°C$)

Parameter	Conditions	Min	Typ	Max	Units
STATIC DC CHARACTERISTICS: $e_{IN} = 0$, $R_{MUTE} = 0\Omega$, $V_{CC} = 6V$					
Operating Supply Range, V14		3	6	15	V
Supply Current, I_{14}	AM Mode		15		mA
Supply Current, I_{14}	FM Mode		17		mA
Regulator Output Voltage, V11			2.9		V
Meter Output Voltage, V18	AM Mode		0	0.2	V
Meter Output Voltage, V18	FM Mode		0	0.2	V
AFC Output Voltage, V17	FM Mode		2.9		V
AM/FM Audio Output Resistance, R_o15			3		kΩ
AM DYNAMIC CHARACTERISTICS: $f_{AM} = 1$ MHz, $f_{MOD} = 1$ kHz, m = 0.3, $V_{CC} = 6V$					
Maximum Sensitivity	e_{AM} for $e_O = 6$ mV		9		μV
20 dB Quieting Sensitivity	e_{AM} for $e_O = 20$ dB S/N		25		μV
Signal to Noise Ratio	$e_{AM} = 10$ mV	40	50		dB
Total Harmonic Distortion	$e_{AM} = 10$ mV		0.3	1	%
Total Harmonic Distortion	$e_{AM} = 10$ mV, m = 0.8		1	2	%
Audio Output Level	$e_{AM} = 10$ mV	80	120	160	mV
Overload Distortion	$e_{AM} = 50$ mV, m = 0.8		2	10	%
Meter Output Voltage	$e_{AM} = 1$ mV		1.2		V
Meter Output Voltage	$e_{AM} = 50$ mV		2.5		V
FM DYNAMIC CHARACTERISTICS: $f_{FM} = 10.7$ MHz, $f_{MOD} = 400$ Hz, $\Delta f = \pm 75$ kHz, $V_{CC} = 6V$					
-3 dB Limiting Sensitivity	e_{FM} for -3 dB Limiting Sensitivity		12	25	μV
Signal to Noise Ratio	$e_{FM} = 10$ mV	60	76		dB
AM Rejection	$e_{FM} = 10$ mV, 30% AM Mod	40	55		dB
Total Harmonic Distortion	$e_{FM} = 10$ mV		0.5	1	%
Audio Output Level	$e_{FM} = 10$ mV, 30% FM Mod	80	120	160	mV
Meter Output Level	$e_{FM} = 1$ mV		0.8		V
Meter Output Level	$e_{FM} = 50$ mV		1.8		V
± Deviation Mute (Notes 2, 4)	$e_{FM} = 10$ mV, $R_{AFC} = 10k$		40		kHz
R_{MUTE} for Noise Mute (Notes 3, 4)	Set e_{FM} for -3 dB Limiting Sensitivity	2	5	10	kΩ
Max Audio Mute Attenuation		60	75		dB

Note 1: Above $T_A = 25°C$, derate based on $T_{J(max)} = 150°C$ and $\theta_{JA} = 75°C/W$.

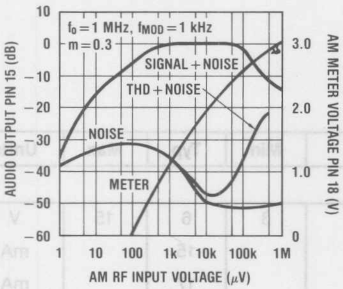
Note 2: $R_{MUTE} = 2$ kΩ, $e_{FM} = 10$ mV, adjust center frequency for $V_{AFC} = V_{REG}$, record f_{FM}, adjust $\pm f_{FM}$ for > 50 dB audio mute attenuation.

Note 3: Adjust R_{MUTE} from 2k to 10k for > 50 dB audio mute attenuation. Set $e_{FM} = 10$ mV and check for mute off.

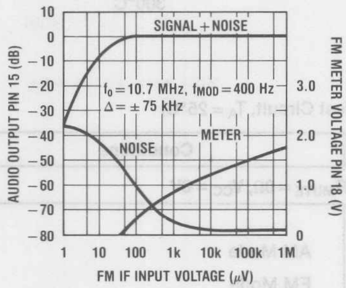
Note 4: When $R_{MUTE} = 0\Omega$, the deviation and noise operated mute functions are disabled. When $R_{MUTE} = 2$ kΩ, only the noise mute function is disabled. The deviation mute bandwidth is set by the R_{AFC} resistor. The noise mute threshold is set by the R_{MUTE} resistor. Test circuit noise bandwidth characteristics prevent noise mute operation for IF input levels below the -3 dB limiting threshold. When the FM IF is used with a tuner full noise mute capability is accessible (See Applications Information).

10

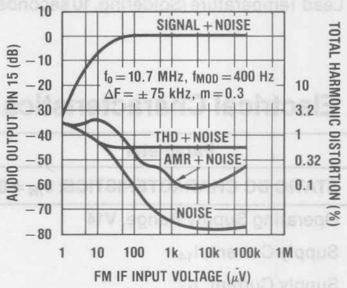
AM Characteristics
$V_{CC} = 6V$



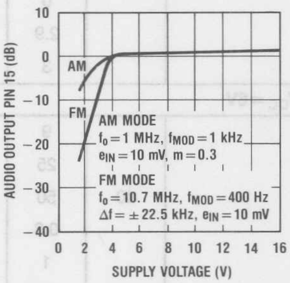
FM IF Characteristics
$V_{CC} = 6V$



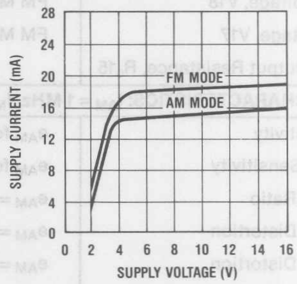
FM IF Characteristics
$V_{CC} = 6V$



Recovered Audio vs Supply



Quiescent Supply Current vs Supply Voltage



Applications Information

(See Typical Applications and LM1866 Schematic Diagram)

VOLTAGE REGULATOR SECTION

Because of the wide supply voltage range and high ripple conditions expected in battery or low cost transformer supplies, the LM1866 uses a band gap referenced active voltage regulator which is externally compensated at pin 19. This capacitor, when made large enough, improves the supply rejection and decreases the noise bandwidth to a level well below the AM reception frequencies. A 0.1 μF capacitor will compensate the regulator for low noise operation while 50 μF (max) will improve supply rejection and the maximum FM audio mute attenuation characteristics. During power turn on, the pin 19 capacitor is quick-charged to its normal operating voltage so that the AM or FM sections are in operation before the audio amplifier turn on delay has timed out. See LM1895/LM2895 and LM1896/LM2896 data sheets for additional audio amplifier information.

AM SECTION

The AM section contains a fully balanced mixer stage with the RF input applied to a differential, diode degenerated, transistor pair at pins 5 and 6. DC feedback is provided by the loopstick secondary winding. The mixer output 1st IF transformer at pin 7 should be returned to V_{CC} at pin 14 to allow maximum undistorted output swing when tuning between stations. RF and AGC decoupling at pin 6 removes noise and lowers audio distortion.

The mixer upper pairs are switched differentially by a buffer amplifier from the pin 8 local oscillator. DC feedback is provided by the oscillator coil secondary winding to the pin 11 regulator voltage.

The oscillator frequency is given by:

$$f_O = \frac{0.159}{\sqrt{LC}},$$

and the peak swing is given by: $V_P = IZ$ ($I = 700\ \mu A$, Z = tank impedance at resonance). V_P should be between 0.3V and 0.5V to maintain an undistorted output at low supplies.

The two stage AM IF amplifier at pins 12 and 13 requires output to input DC feedback and external decoupling. The IF gain is given by:

$$A_V = \frac{Z_L}{12}$$

Applications Information (Continued)

where Z_L equals resonant unloaded tank impedance in parallel with R_{EXT}. In most applications $Z_L = 10k$ and

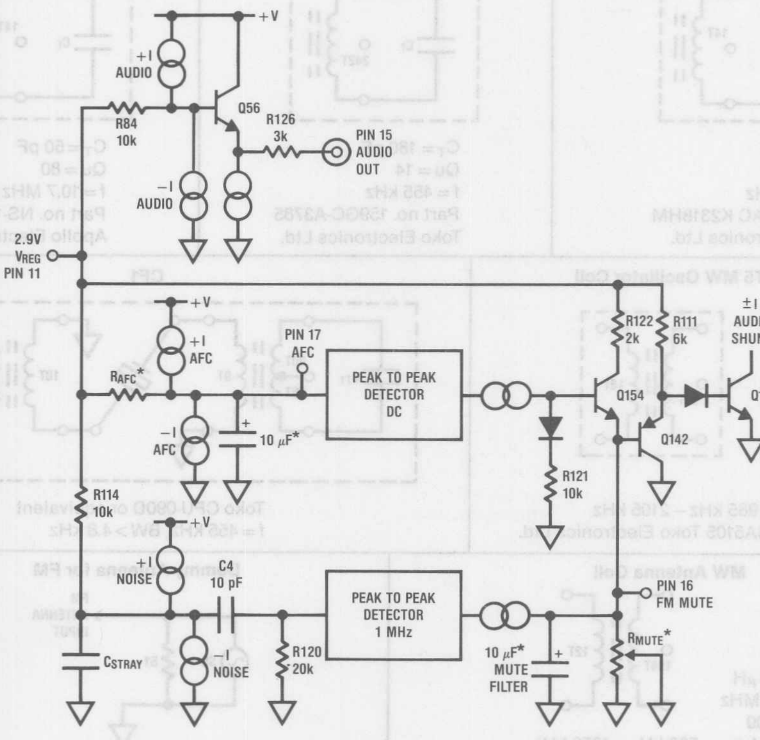
$$Q_L = \frac{Z_L}{X_C} = 5$$

where R_{EXT} = an external IF gain setting resistor and X_C = impedance of tank tuning capacitor. A rule of thumb for setting the IF gain would be to adjust R_{EXT} for 20 dB audio S/N when the audio has dropped 10 dB below the level found at the AGC threshold. (Because of the low Q_L, a non-tuned coil is acceptable.)

The output of the IF amplifier drives an internal detector which is operating at low currents. This results in very low 2nd and 3rd IF harmonic radiation for minimal tweet interference.

FM SECTION

The FM section contains a six stage limiting amplifier, quadrature detector, AFC output, deviation mute detector and a high frequency noise mute detector. (See *Figure 1* for the Simplified Mute Circuit Schematic.) The output of the quadrature detector is split into three current source pairs. The ± audio current and internal load resistor R84 provide the audio output voltage via Q56 to pin 15. The ± AFC current, external load resistor (R_{AFC}) and the 10 μF capacitor provide an audio decoupled AFC voltage to pin 17. The ± noise current and internal load resistor R114 provide a wideband detector output that is limited in frequency by C_{STRAY}. With the addition of internal C4 and R120 a band pass filter ($f_o \cong 1$ MHz) is realized at the input of the peak to peak detector. The output current, flowing in resistor R_{MUTE} and filtered by a capacitor, provides a mute voltage at pin 16. When the mute voltage rises to approximately one V_{BE}, transistor Q139 will start to shunt the ± audio current away from R84, muting the audio output. The value of the R_{MUTE} resistor will determine the minimum audio signal to noise ratio at which one wishes to mute. The deviation mute detector will output a current only when the AFC voltage is offset above or below the V_{REG} voltage. Load resistor R121 and transistor Q154 will convert this current to a mute voltage at pin 16. This is done to prevent interaction between the two detector output currents. The external R_{AFC} resistor is used to set the deviation mute bandwidth so that the pin 16 mute voltage is one V_{BE} at the desired frequency band edge. When disabling the mute functions, pin 16 is shorted to ground, preventing Q139 from becoming active.



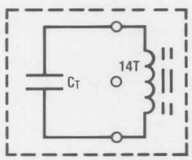
*External component

FIGURE 1. Simplified Mute Circuit Schematic

TABLE I. TYPICAL APPLICATION EXTERNAL COIL AND COMPONENT SELECTION GUIDE

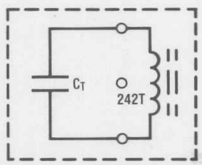
Component	Typical Value	Purpose
C1A, B, C, D	—	AM/FM tuning capacitor
R1, C2, C3	330Ω, 0.01 μF	FM IF decoupling, filter match and DC feedback
C4	1 μF–10 μF	AM RF/AGC decoupling
R5, C5	27k, 1 μF	Sets AM AGC time constant
R6	120k–150k	Optional: decreases AM audio output but improves AM meter threshold
C6	0.1 μF	Regulator output decoupling
C7, C8	0.1 μF, 10 μF	AM IF/audio decoupling
R4 (R_{EXT})	15k	Sets AM IF gain
R7, C15, C14	10Ω, 0.1 μF, 100 μF	Supply decoupling
R3, C10	3k, 0.01 μF	Sets FM de-emphasis/AM smoothing
		Audio post filter pole is given by: $f = \frac{0.159}{R_T C10}$, when $R_T = R3 + R_o 15 = R3 + 3\ k\Omega$
R_{MUTE}, C11	0 to 10k, 10 μF	Sets noise mute threshold, filter. 0Ω will turn off mute function.
R_{AFC}, C12	10k, 10 μF	Sets deviation mute bandwidth, audio decoupling
C13	10 μF	Regulator decoupling and supply rejection filter

T1



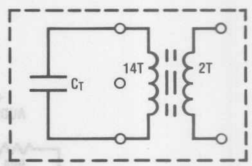
$C_T = 82$ pF
Qu = >70
f = 10.7 MHz
Part no. KAC K2318HM
Toko Electronics Ltd.

T2



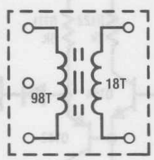
$C_T = 180$ pF
Qu = 14
f = 455 kHz
Part no. 159GC-A3785
Toko Electronics Ltd.

T3



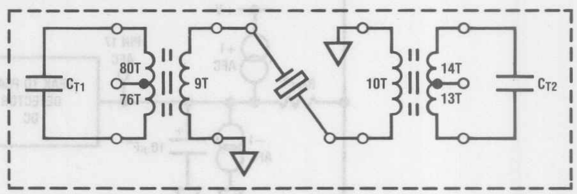
$C_T = 50$ pF
Qu = 80
f = 10.7 MHz
Part no. NS-107C
Apollo Electronics Corp.

T4 and T5 MW Oscillator Coil



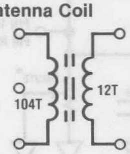
L = 360 μH
f = 796 MHz
Qu = 160
Tuning freq. = 985 kHz – 2105 kHz
Part no. RBO6A5105 Toko Electronics Ltd.

CF1



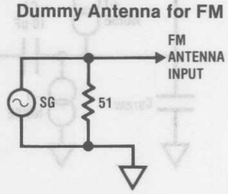
Toko CFU-090D or equivalent
f = 455 kHz, BW > 4.8 kHz

MW Antenna Coil



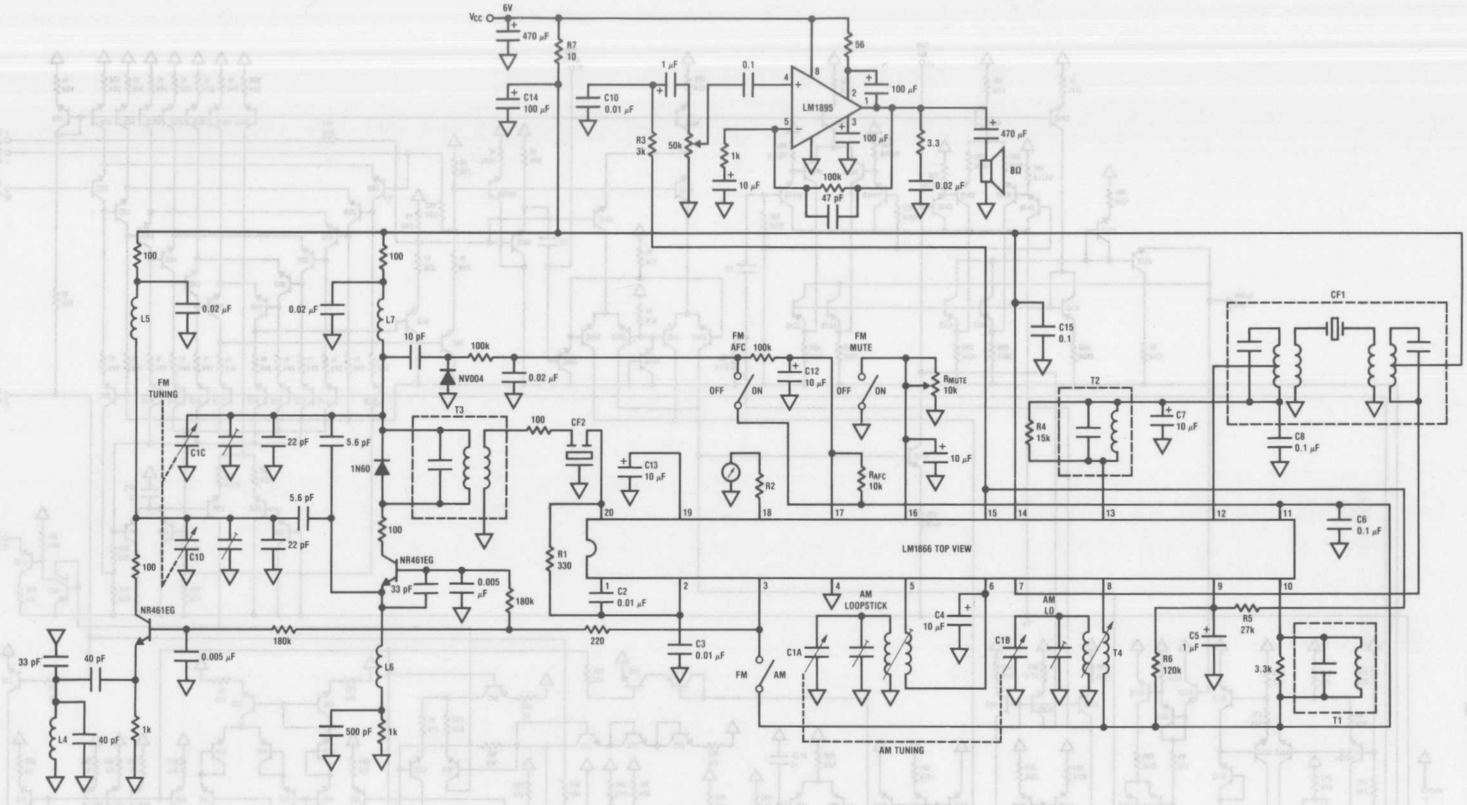
L = 650 μH
f = 796 MHz
Qu = 200
Tuning freq. = 530 kHz – 1650 kHz

Dummy Antenna for FM



L7 SWG #20, N = 3 1/2T, ID = 5mm
L5 SWG #20, N = 3 1/2T, ID = 5mm
L6 L = 0.44 μH, N = 4 1/2T, $Q_u = 70$

Variable Tuning Capacitor
Type: QT-22124 Toko Electronics Ltd.
Capacitance: AM C1A 4–142 pF, C1B 4–60 pF
FM 2.5 pF–20 pF C1C, C1D



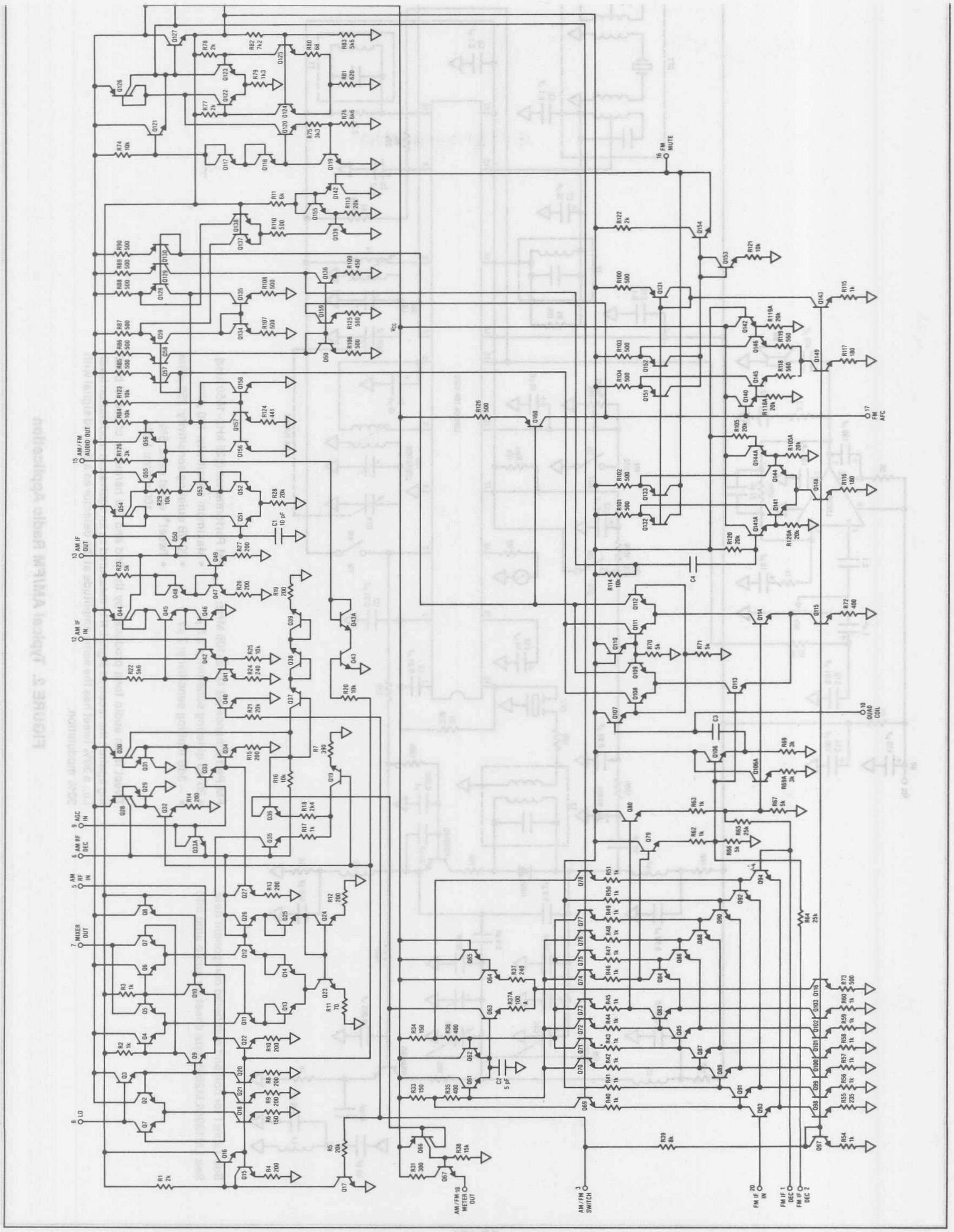
See Table I for coil and numbered component data
See LM1895/LM2895 data sheet for audio amp info

FM Performance (88 MHz–108 MHz)
- 30 dB quieting sensitivity: 3.5 μV
- −3dB limiting sensitivity: 7 μV

AM Performance (525 kHz–1650 kHz)
- Maximum sensitivity: 100 μV/m
- 20 dB quieting sensitivity: 250 μV/m
- Tweet* worst case: 5%
  100 mV/m: 1.5%

* Tweet is an audio tone produced by the 2nd and 3rd harmonic of the IF beating against the received signal. It is measured as an equivalent modulation level: i.e., a 30% tweet has the same amplitude at the detector as a desired signal with 30% modulation.

FIGURE 2. Typical AM/FM Radio Application



National Semiconductor

LM1868 AM/FM Radio System

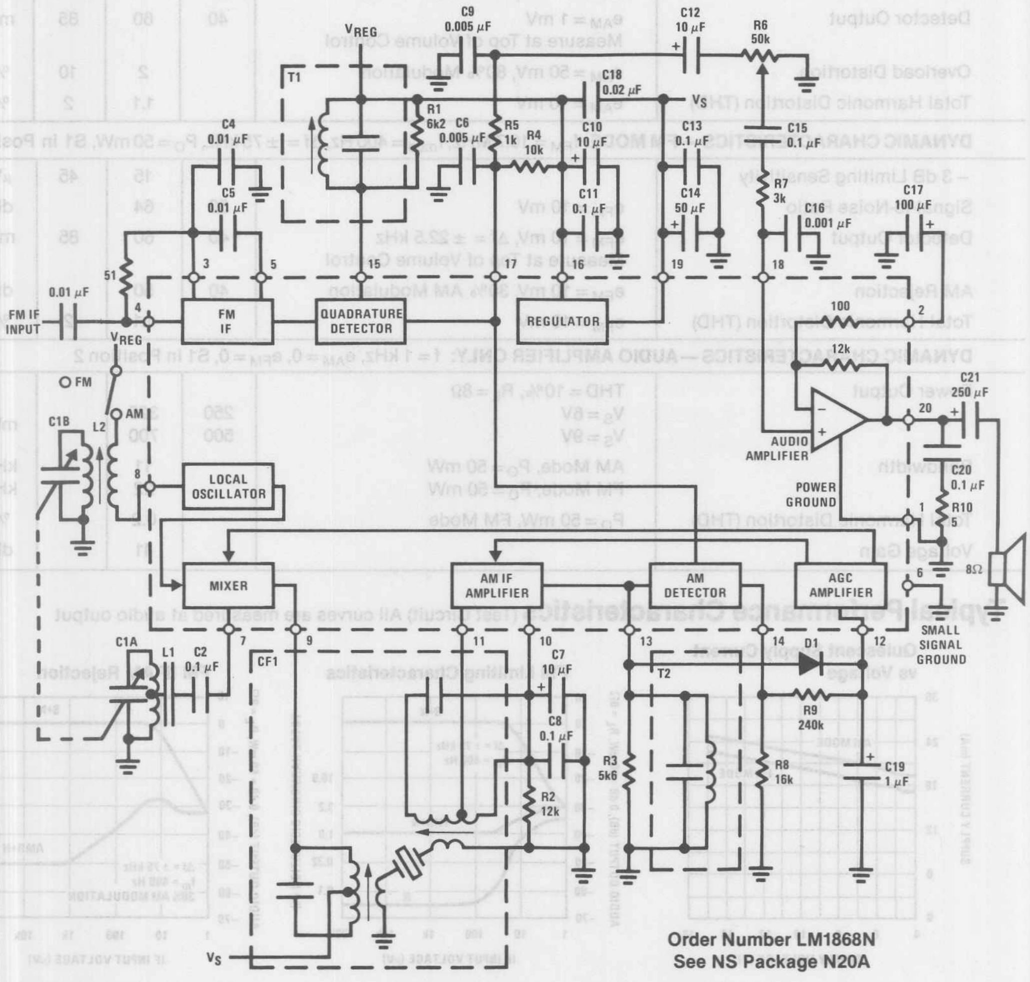
General Description

The combination of the LM1868 and an FM tuner will provide all the necessary functions for a 0.5 watt AM/FM radio. Included in the LM1868 are the audio power amplifier, FM IF and detector, and the AM converter, IF, and detector. The device is suitable for both line operated and 9V battery applications.

Features

- DC selection of AM/FM mode
- Regulated supply
- Audio amplifier bandwidth decreased in AM mode, reducing amplifier noise in the AM band
- AM converter AGC for excellent overload characteristics
- Low current internal AM detector for low tweet radiation

Block Diagram



Order Number LM1868N
See NS Package N20A

Note: See table for coil data

Absolute Maximum Ratings

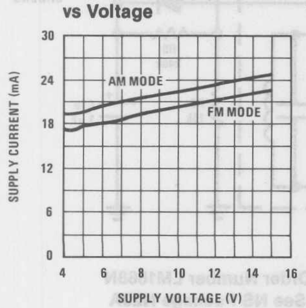
Supply Voltage (Pin 19)	15V
Package Dissipation	1.6W
Above $T_A = 25°C$, Derate Based on $T_{J(MAX)} = 150°C$ and $\theta_{JA} = 75°C/W$	
Storage Temperature Range	−55°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics Test Circuit, $T_A = 25°C$, $V_S = 9V$, $R_L = 8\Omega$ unless otherwise noted

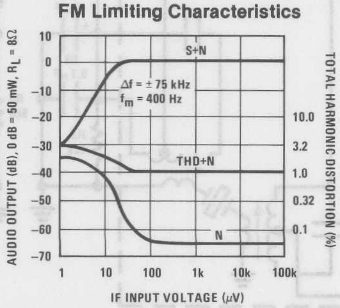
Parameter	Conditions	Min	Typ	Max	Units
STATIC CHARACTERISTICS: $e_{AM} = 0$, $e_{FM} = 0$					
Supply Current	AM Mode, S1 in Position 1		22	30	mA
Regulator Output Voltage (Pin 16)		3.5	3.9	4.5	V
Operating Voltage Range		4.5		15	
DYNAMIC CHARACTERISTICS—AM MODE: $f_{AM} = 1$ MHz, $f_{mod} = 1$ kHz, 30% Modulation, S1 in Position 1, P_O = 50 mW unless noted					
Maximum Sensitivity	Measure e_{AM} for $P_O = 50$ mW, Maximum Volume	8		16	μV
Signal-to-Noise	$e_{AM} = 10$ mV	40	50		dB
Detector Output	$e_{AM} = 1$ mV Measure at Top of Volume Control	40	60	85	mV
Overload Distortion	$e_{AM} = 50$ mV, 80% Modulation		2	10	%
Total Harmonic Distortion (THD)	$e_{AM} = 10$ mV		1.1	2	%
DYNAMIC CHARACTERISTICS—FM MODE: $f_{FM} = 10.7$ MHz, $f_{mod} = 400$ Hz, $\Delta f = \pm 75$ kHz, $P_O = 50$ mW, S1 in Position 1					
−3 dB Limiting Sensitivity			15	45	μV
Signal-to-Noise Ratio	$e_{FM} = 10$ mV	50	64		dB
Detector Output	$e_{FM} = 10$ mV, $\Delta f = \pm 22.5$ kHz Measure at Top of Volume Control	40	60	85	mV
AM Rejection	$e_{FM} = 10$ mV, 30% AM Modulation	40	50		dB
Total Harmonic Distortion (THD)	$e_{FM} = 10$ mV		1.1	2	%
DYNAMIC CHARACTERISTICS—AUDIO AMPLIFIER ONLY: f = 1 kHz, $e_{AM} = 0$, $e_{FM} = 0$, S1 in Position 2					
Power Output	THD = 10%, $R_L = 8\Omega$ $V_S = 6V$ $V_S = 9V$	 250 500	 325 700		mW
Bandwidth	AM Mode, $P_O = 50$ mW FM Mode, $P_O = 50$ mW		11 22		kHz kHz
Total Harmonic Distortion (THD)	$P_O = 50$ mW, FM Mode		0.2		%
Voltage Gain			41		dB

Typical Performance Characteristics (Test Circuit) All curves are measured at audio output

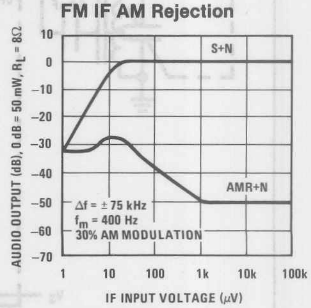
Quiescent Supply Current vs Voltage



FM Limiting Characteristics

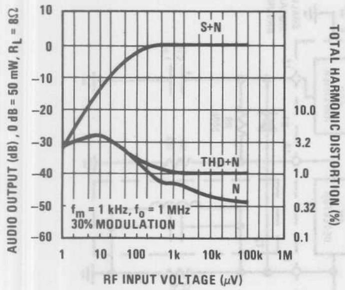


FM IF AM Rejection

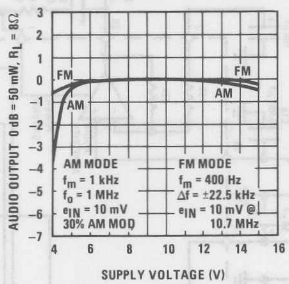


Typical Performance Characteristics (Continued) (Test Circuit) All curves are measured at audio output

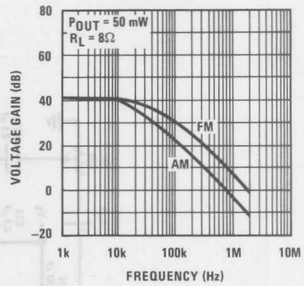
AM Characteristics



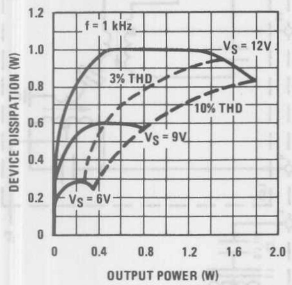
Recovered Audio vs Supply



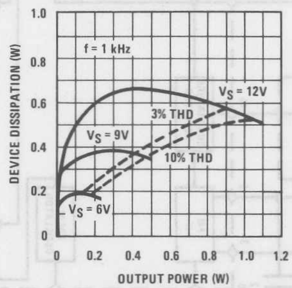
Gain vs Frequency Audio Amplifier Only



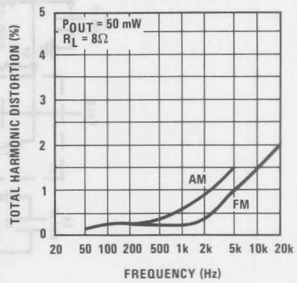
Power Dissipation vs Power Output, $R_L = 8\Omega$



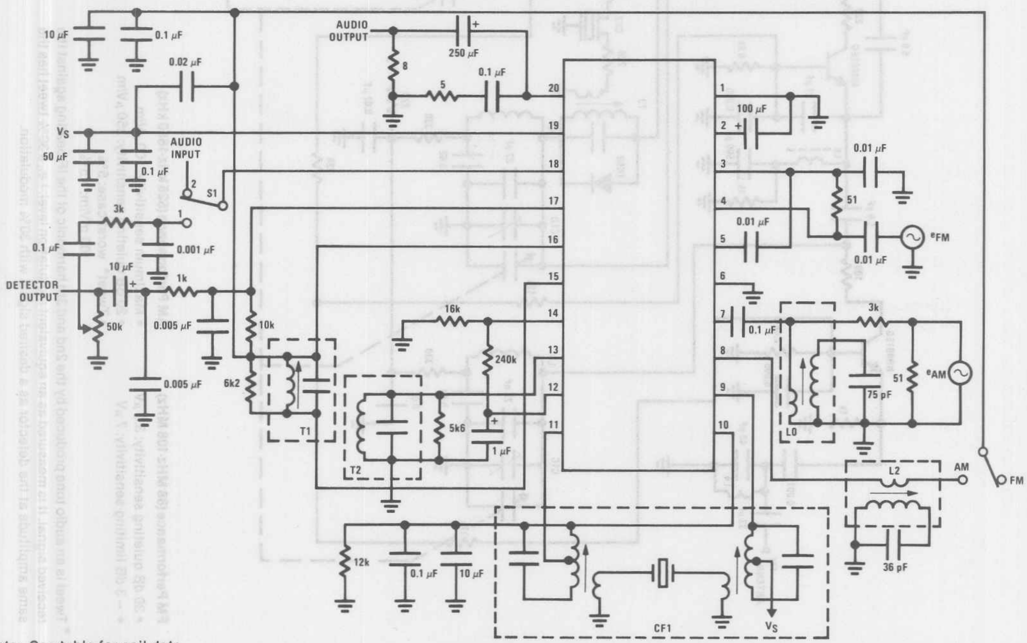
Power Dissipation vs Power Out, $R_L = 16\Omega$



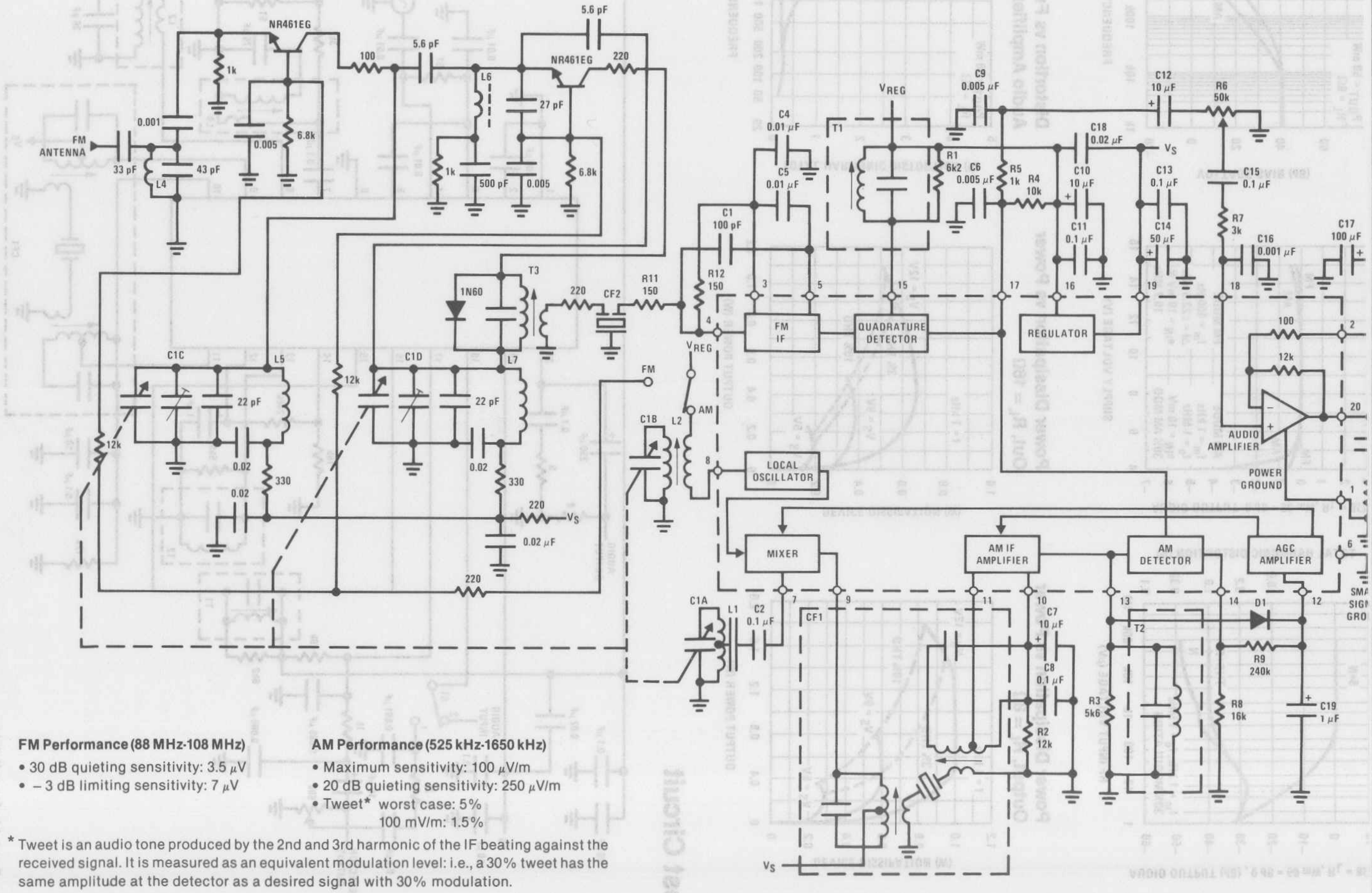
Distortion vs Frequency Audio Amplifier Only



Test Circuit



Note: See table for coil data



FM Performance (88 MHz-108 MHz)

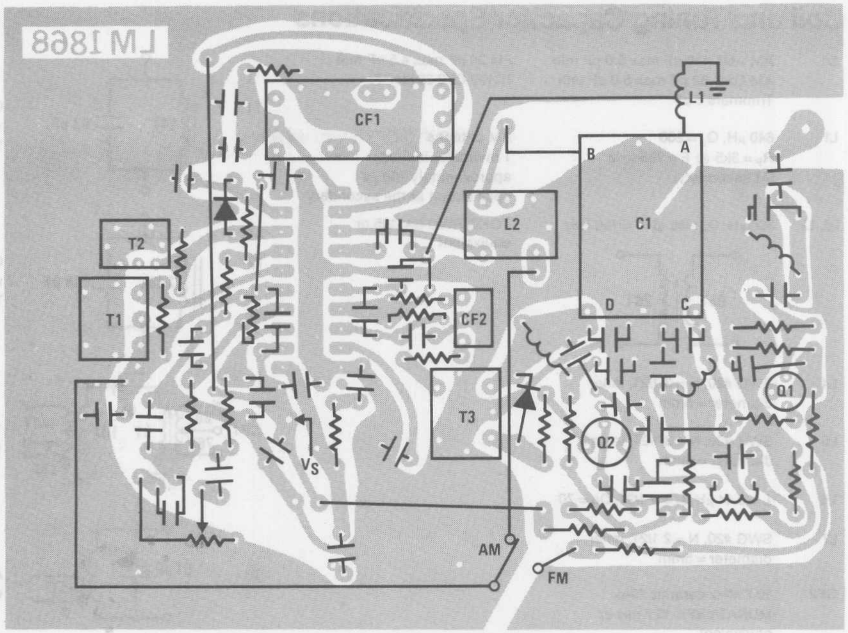
- 30 dB quieting sensitivity: 3.5 μV
- − 3 dB limiting sensitivity: 7 μV

AM Performance (525 kHz-1650 kHz)

- Maximum sensitivity: 100 μV/m
- 20 dB quieting sensitivity: 250 μV/m
- Tweet* worst case: 5%
  100 mV/m: 1.5%

* Tweet is an audio tone produced by the 2nd and 3rd harmonic of the IF beating against the received signal. It is measured as an equivalent modulation level: i.e., a 30% tweet has the same amplitude at the detector as a desired signal with 30% modulation.

PC Board Layout

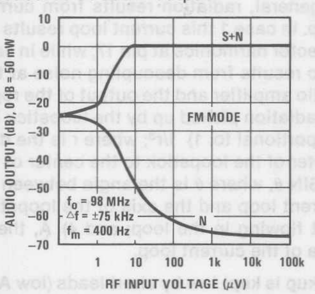


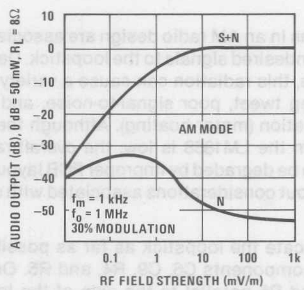
COMPONENT SIDE

Typical Performance Characteristics

Typical Application

All curves are measured at audio output





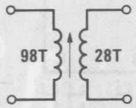
IC External Components (Application Circuit)

Component	Typical Value	Comments
C1	100 pF	Removes tuner LO from IF input
C2	0.1 μF	Antenna coupling capacitor
C4, C5	0.01 μF	FM IF decoupling capacitors
C6, C9	0.005 μF	AM smoothing/FM de-emphasis network, de-emphasis pole is given by: $f1 \cong \frac{1}{2\pi(C6+C9)\left(\frac{R4\ R6}{R4+R6}\right)}$
R5	1k	
C10	10 μF	Regulator decoupling capacitor
C11	0.1 μF	Regulator decoupling capacitor
C12	10 μF	AC coupling to volume control
C13	0.1 μF	Power supply decoupling
C14	50 μF	Power supply decoupling
C15	0.1 μF	Audio amplifier input coupling
R7	3k	Roll off signals from detector in the AM band to prevent radiation
C16	0.001 μF	
C17	100 μF	Power amplifier feedback decoupling, sets low frequency supply rejection

Component	Typical Value	Comments
R8	16k	AM detector bias resistor
R9	240k	Set AGC time constant
C19	1 μF	
C7	10 μF	IF decoupling
C8	0.1 μF	IF decoupling
C20	0.1 μF	High frequency load for audio amplifier, required to stabilize audio amplifier
R10	5Ω	
C21	250 μF	Output coupling capacitor
R1	6k2	Sets Q of quadrature coil, determining FM THD and recovered audio
R2	12k	IF amplifier bias R
R3	5k6	Sets gain of AM IF and Q of AM IF output tank
R4	10k	Detector load resistor
R6	50k	Volume control
C18	0.02 μF	Power supply decoupling
R11, R12	150Ω	Terminates the ceramic filter, biases FM IF input stage
D1	1N4148	Optional. Quickens the AGC response during turn on

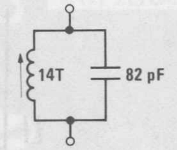
Coil and Tuning Capacitor Specifications

C1	AM ANT 140 pF max 5.0 pF min AM OSC 82 pF max 5.0 pF min Trimmers 5 pF	FM 20 pF max 4.5 pF min TOKO CY2-22124PT
L1	640 μH, Q_u = 200 R_P = 3k5 @ F = 796 kHz (At secondary)	AM antenna 1 mV/meter induces approximately 100 μV open circuit at the secondary
L0, L2	360 μH, Q_u > 80 @ F = 796 kHz	TOKO RWO-6A5105 or equivalent



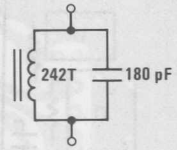
L4	SWG #20, N = 3 1/2T, inner diameter = 5mm	
L5	SWG #20, N = 3 1/2T, inner diameter = 5mm	
L6	L = 0.44 μH, N = 4 1/2T, Qu = 70	
L7	SWG #20, N = 2 1/2T, inner diameter = 5mm	
CF2	10.7 MHz ceramic filter MURATA SFE 10.7 mA or equivalent	

T1



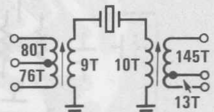
Q_u > 70 @ 10.7 MHz, L to resonate w/82 pF @ 10.7 MHz
TOKO KAC-K2318 or equivalent

T2



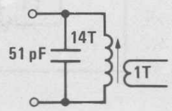
Q_u > 14 @ 455 kHz, L to resonate w/180 pF @ 455 kHz
TOKO 159GC-A3785 or equivalent

CF1



TOKO CFU-090D or equivalent
BW > 4.8 kHz @ 455 kHz

T3



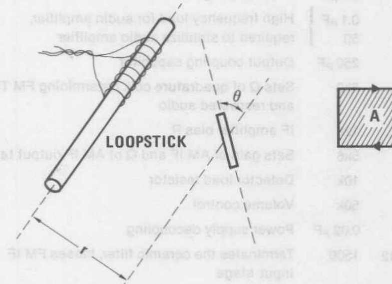
Apollo Electronics NS-107C or equivalent

Layout Considerations

AM Section

Most problems in an AM radio design are associated with radiation of undesired signals to the loopstick. Depending on the source, this radiation can cause a variety of problems including tweet, poor signal-to-noise, and low frequency oscillation (motor boating). Although the level of radiation from the LM1868 is low, the overall radio performance can be degraded by improper PCB layout. Listed below are layout considerations associated with common problems.

1. **Tweet:** Locate the loopstick as far as possible from detector components C6, C9, R4, and R5. Orient C6, C9, R4, and R5 parallel to the axis of the loopstick. Return R8, C6, C9, and C19 to a separate ground run (see Typical Application PCB).
2. **Poor Signal-to-Noise/Low Frequency Oscillation:** Twist speaker leads. Orient R10 and C20 parallel to the axis of the loopstick. Locate C11 away from the loopstick.



In general, radiation results from current flowing in a loop. In case 1 this current loop results from decoupling detector harmonics at pin 17; while in case 2, the current loop results from decoupling noise at the output of the audio amplifier and the output of the regulator. The level of radiation picked up by the loopstick is approximately proportional to: 1) $1/r^3$; where r is the distance from the center of the loopstick to the center of the current loop; 2) SIN θ, where θ is the angle between the plane of the current loop and the axis of the loopstick; 3) I, the current flowing in the loop; and 4) A, the cross-sectional area of the current loop.

Pickup is kept low by short leads (low A), proper orientation ($\theta \cong 0$ so SIN $\theta \cong 0$), maximizing distance from sources to loopstick, and keeping current levels low.

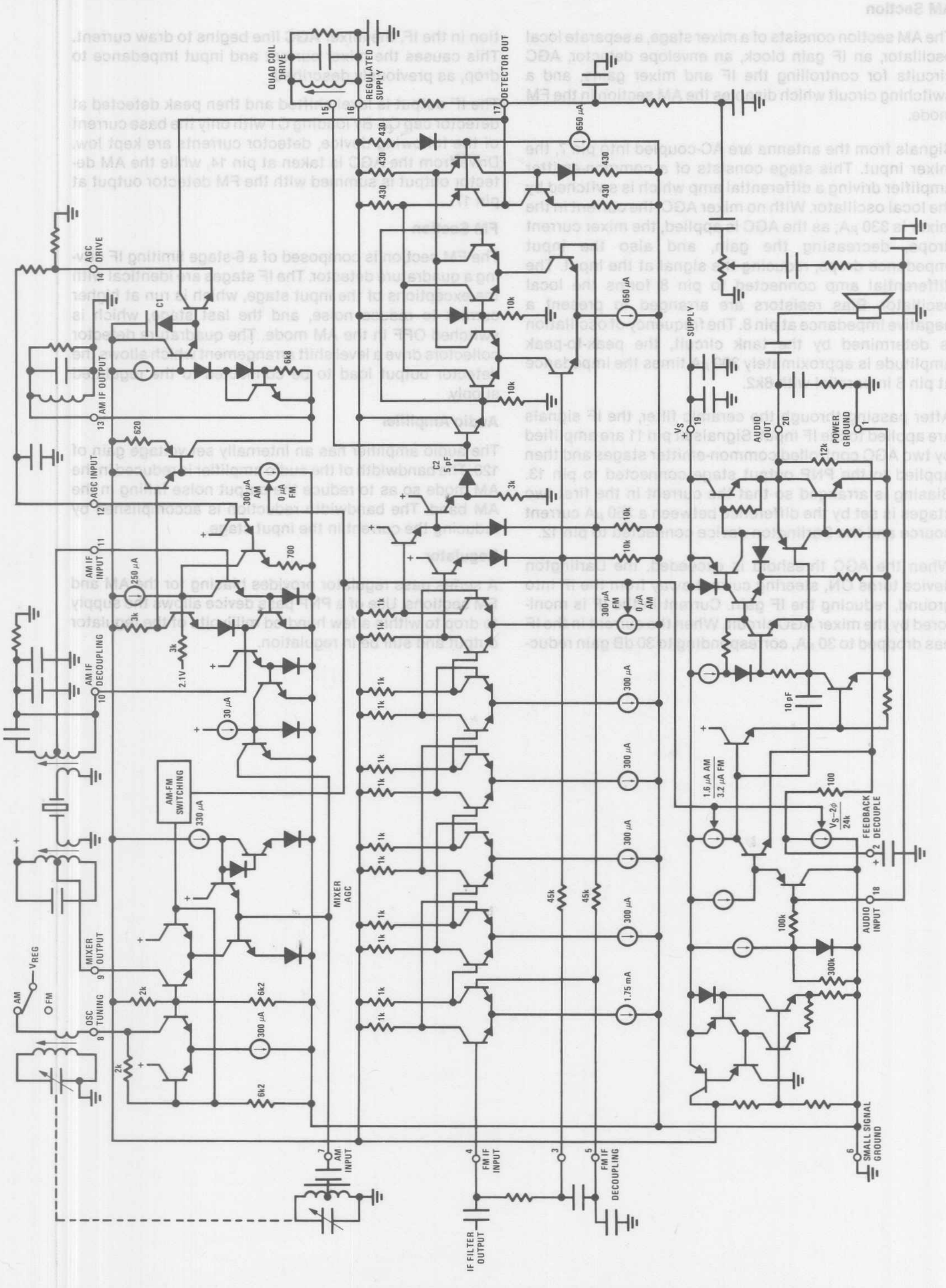
FM Section

The pinout of the LM1868 has been chosen to minimize layout problems, however some care in layout is required to insure stability. The input source ground should return to C4 ground.Capacitors C13 and C18 form the return path for signal currents flowing in the quadrature coil. They should connect directly to the proper pins with short PC traces (see Typical Application PCB). The quadrature coil and input circuitry should be separated from each other as far as possible.

Audio Amplifier

The standard layout considerations for audio amplifiers apply to the LM1868, that is: positive and negative inputs should be returned to the same ground point, and leads to the high frequency load should be kept short. In the case of the LM1868 this means returning the volume control ground (R6) to the same ground point as C17, and keeping the leads to C20 and R10 short.

Equivalent Schematic



oscillator, an IF gain block, an envelope detector, AGC circuits for controlling the IF and mixer gains, and a switching circuit which disables the AM section in the FM mode.

Signals from the antenna are AC-coupled into pin 7, the mixer input. This stage consists of a common-emitter amplifier driving a differential amp which is switched by the local oscillator. With no mixer AGC, the current in the mixer is 330 μA; as the AGC is applied, the mixer current drops, decreasing the gain, and also the input impedance drops, reducing the signal at the input. The differential amp connected to pin 8 forms the local oscillator. Bias resistors are arranged to present a negative impedance at pin 8. The frequency of oscillation is determined by the tank circuit, the peak-to-peak amplitude is approximately 300 μA times the impedance at pin 8 in parallel with 8k2.

After passing through the ceramic filter, the IF signals are applied to the IF input. Signals at pin 11 are amplified by two AGC controlled common-emitter stages and then applied to the PNP output stage connected to pin 13. Biasing is arranged so that the current in the first two stages is set by the difference between a 250 μA current source and the Darlington device connected to pin 12.

When the AGC threshold is exceeded, the Darlington device turns ON, steering current away from the IF into ground, reducing the IF gain. Current in the IF is monitored by the mixer AGC circuit. When the current in the IF has dropped to 30 μA, corresponding to 30 dB gain reduction in the IF, the mixer AGC line begins to draw current. This causes the mixer current and input impedance to drop, as previously described.

The IF output is level shifted and then peak detected at detector cap C1. By loading C1 with only the base current of the following device, detector currents are kept low. Drive from the AGC is taken at pin 14, while the AM detector output is summed with the FM detector output at pin 17.

FM Section

The FM section is composed of a 6-stage limiting IF driving a quadrature detector. The IF stages are identical with the exceptions of the input stage, which is run at higher current to reduce noise, and the last stage, which is switched OFF in the AM mode. The quadrature detector collectors drive a level shift arrangement which allows the detector output load to be connected to the regulated supply.

Audio Amplifier

The audio amplifier has an internally set voltage gain of 120. The bandwidth of the audio amplifier is reduced in the AM mode so as to reduce the output noise falling in the AM band. The bandwidth reduction is accomplished by reducing the current in the input stage.

Regulator

A series pass regulator provides biasing for the AM and FM sections. Use of a PNP pass device allows the supply to drop to within a few hundred millivolts of the regulator output and still be in regulation.

National Semiconductor

Audio/Radio Circuits

LM1870 Stereo Demodulator with Blend

General Description

The LM1870 is a phase locked loop FM stereo demodulator with a DC control pin for reducing noise by decreasing separation during weak signal conditions.

Applications

- Automobile radios
- Hi Fi receivers and tuners
- High performance portable radios

Features

- Blend control
- Large input overload
- Low beat note distortion
- Low THD diode switching outputs
- VCO stop function
- Wide supply range, 7V to 15V
- Mono override pin

Typical Application and Test Circuit

Order Number LM1870N
See NS Package N20A

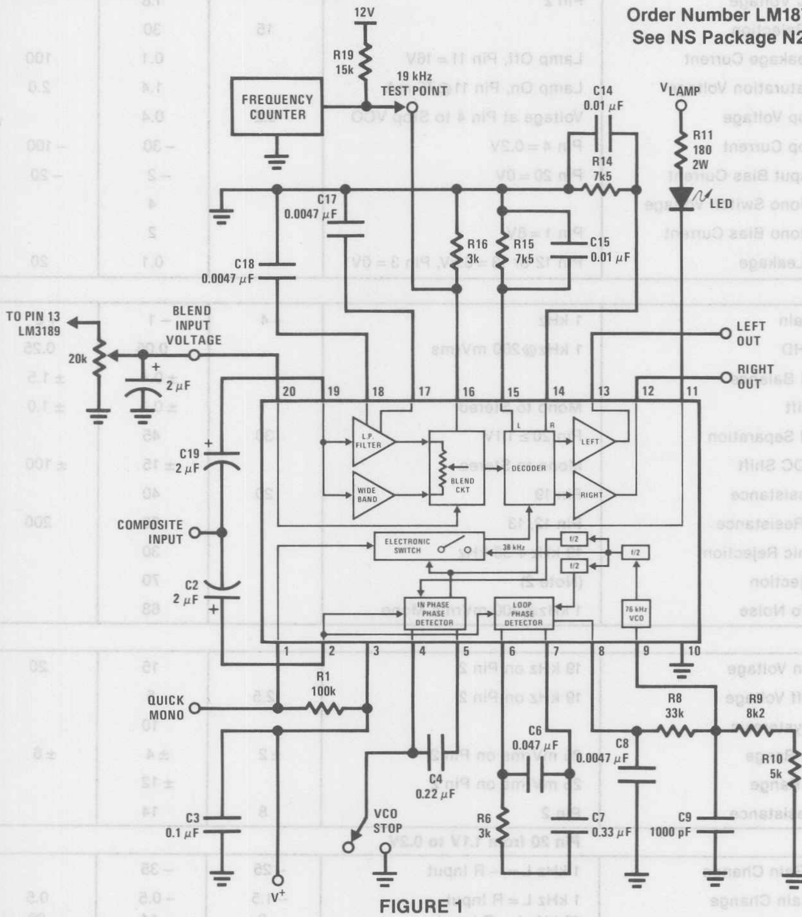


FIGURE 1

Pin Functions

1 Quick Mono	6 Loop Filter	11 Lamp Driver	16 Blend Resistor and 19 kHz Test Point
2 PLL Input	7 Loop Filter	12 Right Output	17 Blend Filter
3 V+	8 VCO Tuning	13 Left Output	18 Blend Filter
4 Lamp Filter and VCO Stop	9 VCO Tuning	14 Right Gain and Deemphasis	19 Audio Input
5 Lamp Filter	10 Ground	15 Left Gain and Deemphasis	20 Blend Control Voltage

Absolute Maximum Ratings

Supply Voltage, Pin 3	15V
Lamp Driver Voltage, Pin 11	18V
Output Voltage, Pin 12, 13, Supply Off	7V
Quick Mono Input (Pin 1)	V^+ (Pin 3)
Blend Input (Pin 20)	15V
Operating Temperature Range	0°C to +70°C
Power Dissipation (Note 1)	1W
Storage Temperature	−65°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics $T_A = 25°C$, $V^+ = 8V$, *Figure 1*

Parameter	Conditions	Min	Typ	Max	Units
DC					
Operating Supply Voltage		7	8	15	V
Supply Current			26	45	mA
Input DC Voltage	Pin 19		4		V
Input DC Voltage	Pin 2		1.8		V
Supply Rejection		15	30		dB
Lamp Leakage Current	Lamp Off, Pin 11 = 16V		0.1	100	μA
Lamp Saturation Voltage	Lamp On, Pin 11@75 mA		1.4	2.0	V
VCO Stop Voltage	Voltage at Pin 4 to Stop VCO	0.2	0.4		V
VCO Stop Current	Pin 4 = 0.2V		−30	−100	μA
Blend Input Bias Current	Pin 20 = 0V		−2	−20	μA
Quick Mono Switch Voltage			4		V
Quick Mono Bias Current	Pin 1 = 8V		2		μA
Output Leakage	Pin 12 or 13 = 6.5V, Pin 3 = 0V		0.1	20	μA
Audio					
Mono Gain	1 kHz	−4	−1	+2	dB
Mono THD	1 kHz@200 mVrms		0.05	0.25	%
Channel Balance			±0.4	±1.5	dB
Gain Shift	Mono to Stereo		±0.1	±1.0	dB
Channel Separation	Pin 20 ≥ 1.1V	30	45		dB
Output DC Shift	Mono to Stereo		±15	±100	mV
Input Resistance	Pin 19	20	40		kΩ
Output Resistance	Pin 12, 13		65	200	Ω
Ultrasonic Rejection	19 kHz + 38 kHz		30		dB
SCA Rejection	(Note 2)		70		dB
Signal To Noise	1 kHz@200 mVrms Mono		68		dB
PLL					
Lamp On Voltage	19 kHz on Pin 2		15	20	mV
Lamp Off Voltage	19 kHz on Pin 2	2.5	5		mV
Lamp Hysteresis			10		dB
Capture Range	25 mVrms on Pin 2	±2	±4	±6	%
Hold In Range	25 mVrms on Pin 2		±12		%
Input Resistance	Pin 2	8	14		kΩ
Blend	**Pin 20 from 1.1V to 0.2V**				
Stereo Gain Change	1 kHz L = −R Input	−25	−35		dB
Mono Gain Change	1 kHz L = R Input	−1.5	−0.5	0.5	dB
	10 kHz L = R Input	−8	−14	−20	dB
Output DC Shift			±40	±100	mV

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 125°C/W junction to ambient.

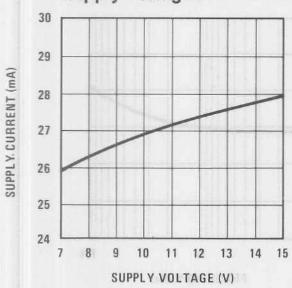
Note 2: Input is 10% SCA (74.5 kHz), 9% pilot and 1 kHz left or right. Rejection is ratio of 1 kHz output to 1.5 kHz output.

External Components

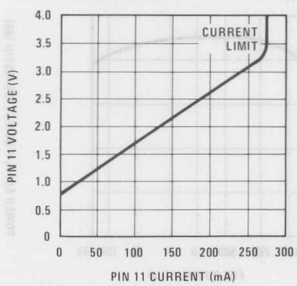
Part #	Recommended Value	Purpose	Affect: Smaller	Affect: Larger	Remarks
R1	100k	Pull Up for Quick Mono	OK	Errors Due to Pin 1 Bias Current	Pin 1 Can Be Shorted to Supply if Quick Mono is Not Used
C2	2 μF	PLL Input Coupling	Loading of Source varies with Frequency		For Source of Less Than 100Ω, Can Use 0.1 μF
C3	0.1 μF	Supply Bypass			
C4	0.22 μF	Lamp Filter	Shorter Time to Switch Mono to Stereo	Longer Time to Switch Mono to Stereo	High Dielectric Resistance
R6 C6 C7	3k 0.047 μF 0.33 μF	Loop Filter	High Stereo Distortion	Narrower Capture Range	
R8 C8	33k 0.0047 μF	Loop Filter	High Stereo Distortion	Loop not Lock Narrower Capture Range	
C9 R9 R10	1000 pF 8.2k 5k	Set VCO Free Running Frequency	High VCO Jitter VCO Not Adjustable with C9	Narrower Capture Range	NPO 5% Metalfilm
R11	180Ω	Sets Lamp Current	Excess IC Dissipation	Dim Lamp	
R14 R15	7.5k 7.5k	Load Resistors	Low Output Voltage	Output Clip Earlier	
C14 C15	0.01 μF 0.01 μF	Deemphasis			
R16	3k	Sets Blend Characteristic	See Curves		
C17 C18	0.0047 μF 0.0047 μF	Filter for Blend	Insufficient Blend	Reduced Blend Bandwidth	
C19	2 μF	Audio Input Coupling	Poor Low Frequency Response and Separation	Turn On Delay	
R19	15k	Allows VCO Monitoring	Excess IC Dissipation	Reduces 19 kHz Output Voltage	Only Need During Set Up

Typical Performance Characteristics Blend off unless otherwise stated

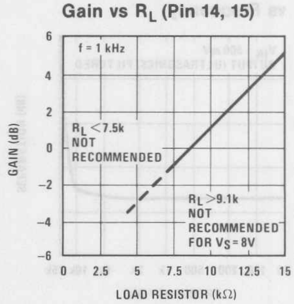
Supply Current vs Supply Voltage



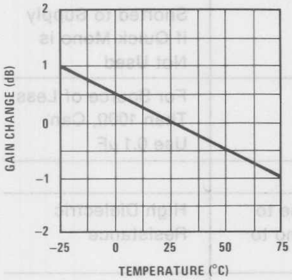
Lamp Driver Voltage vs Current



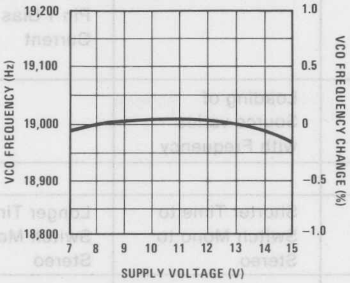
Gain vs R_L (Pin 14, 15)



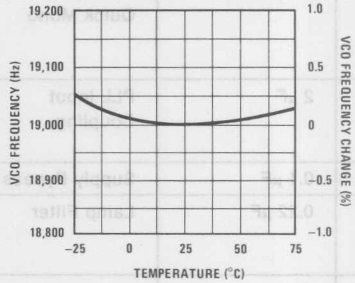
Gain Change vs Temperature



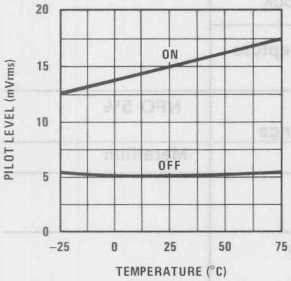
VCO Supply Sensitivity



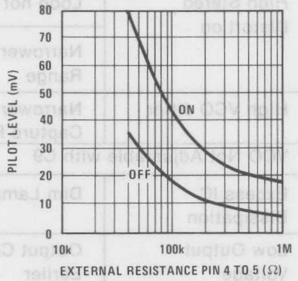
VCO Temperature Stability



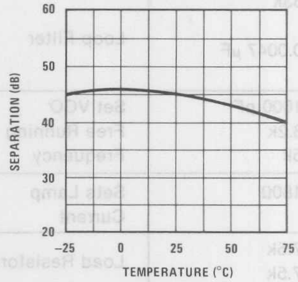
Lamp On/Off vs Temperature



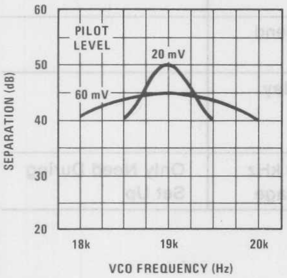
Lamp On/Off vs Resistance Pin 4 to 5



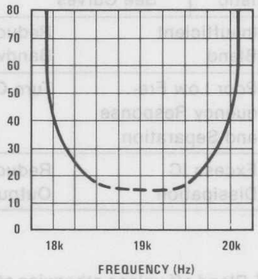
Separation vs Temperature



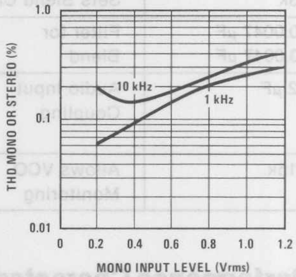
Separation vs VCO Tuning



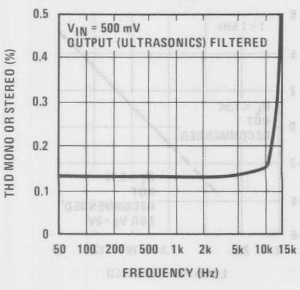
Capture Range vs Pilot Level



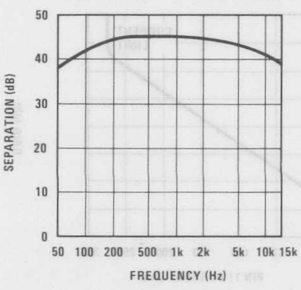
Total Harmonic Distortion vs Input Level



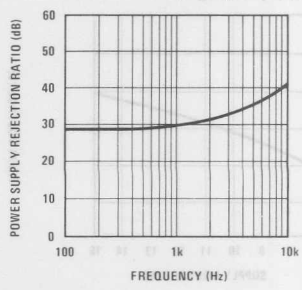
Total Harmonic Distortion vs Frequency



Separation vs Frequency

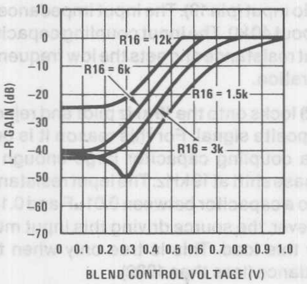


Power Supply Rejection Ratio vs Frequency

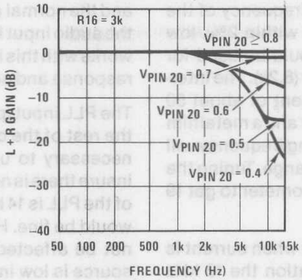


Typical Performance Characteristics Blend off unless otherwise stated

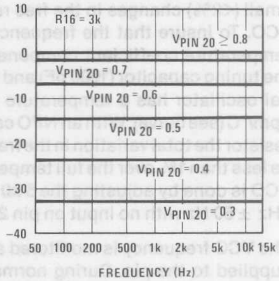
L-R Gain vs Blend Control



L + R Frequency Response with Blend Control



L-R Frequency Response with Blend Control



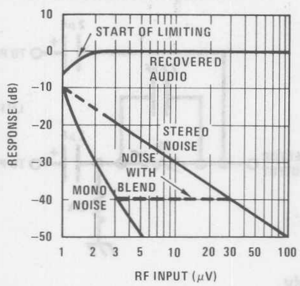
Application Hints

Blend—What & Why?

The signal to noise of a weak FM stereo signal is worse than that of an equally weak FM mono signal. For this reason FM mono radios often perform better than FM stereo radios, unless the latter is forced into mono.

The typical quieting curves of an FM stereo radio look like this:

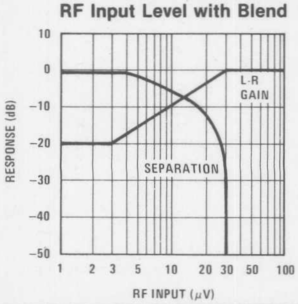
Typical Radio Quieting Characteristic



If an acceptable signal to noise is 40 dB, then 20 dB more signal is required in stereo compared to mono, 30 μV vs 3 μV. The degradation in noise is due to the L-R or difference channel. If the gain of the L-R is reduced, then the noise associated with it will be reduced. However, there will also be a reduction in separation.

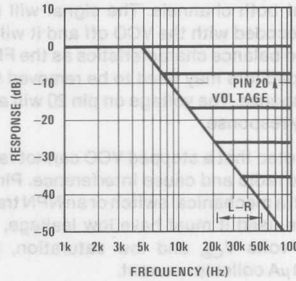
To maintain a 40 dB signal to noise in the above example, the gain of the L-R signal should be reduced from 0 dB gain@30 μV downward to −20 dB at 3 μV. If this is done properly the dashed line will result. Below is a plot of L-R gain and resulting separation.

L-R Gain and Separation vs RF Input Level with Blend



The LM1870 reduces the gain of the L-R channel before it is demodulated. This is done by a voltage controlled shelving filter. The Bode plot of this filter is shown below:

Blend Filter Response



The full blend response is a two pole roll-off with each pole set by an internal 6.8k resistor and the capacitance from pins 17 and 18 to ground. The standard value for both capacitors is 4.7 nF resulting in two 5 kHz poles. The blend input (pin 20) is derived from the meter drive output of the FM IF chip (LM3089 or LM3189 pin 13). To adjust for variations in RF gain and other IC parameters, it is recommended that an adjustment be made on each radio.

Mono-Stereo Switching

The LM1870 automatically switches from mono to stereo when the level of pilot at pin 2 is about 15 mV or more. This value can be increased by putting a resistor between pins 4 and 5, as shown graphically in the Typical Performance curves.

If it is desired to switch to mono without turning off the lamp driver, pin 1 should be taken below 4V. This is a high impedance input that can be electronically switched by a transistor with a pull up resistor to the IC supply.

Outputs

The LM1870 has emitter-follower outputs resulting in a low output impedance. The output wll sink or source one mA, therefore it will drive AC coupled loads greater than 2 kΩ.

In AM-FM radios the switching can be cumbersome at best. To ease the problem the outputs of the LM1870 (pins 12 and 13) are open circuit when the supply (pin 3) is open or grounded. This reduces the numbered switch poles required since the outputs can remain connected at all times. This technique is commonly called diode switching but the method used in the LM1870 results in substantially lower distortion than obtained with discrete diodes.

Application Hints (Continued)

VCO

The stereo performance of the LM1870 is very constant for small (<2%) changes in the free running frequency of the VCO. To insure that the frequency stays within 2%, low temperature coefficient components should be used for the tuning capacitor (1000 pF) and resistor (8.2k). The internal oscillator has a temperature coefficient of about 50 ppm/°C (see curve). With an NPO capacitor and a metalfilm resistor the total variation in the free running frequency will be less than 1% over the full temperature range. Tuning the VCO is done by adjusting the 5 kΩ potentiometer to get 19 kHz ± 50 Hz with no input on pin 2.

The VCO frequency is monitored at pin 16 when current is supplied to the pin. During normal operation the 19 kHz square wave is not available and the resistor from pin 16 to ground programs the blend characteristics (see curves).

The VCO of the LM1870 can be stopped by taking pin 4 low. In addition to being useful for turning off the stereo indicator and forcing mono FM reception, this also allows other mono sources, such as AM, to be fed into the decoder and come out both channels. The signal will not be inadvertently decoded with the VCO off and it will have the same gain and balance characteristics as the FM. The deemphasis capacitors may need to be removed for proper frequency response. The voltage on pin 20 will also affect the frequency response.

It should be noted that a stopped VCO cannot radiate into the rest of the radio and cause interference. Pin 4 can be taken low with a mechanical switch or an NPN transistor. If a transistor is used it must have low leakage, less than 100 nA at 3 volts V_{CE}, and low saturation, less than 200 mV at 100 μA collector current.

PLL

To properly demodulate the L-R signal the decoder must generate a 38 kHz signal that is locked in phase with the 19 kHz pilot signal at the input. This is done with a phase locked loop consisting of a phase detector, a loop filter (pins 6 and 7) and a VCO (pins 8 and 9).

The loop filter is similar to other standard decoders however the VCO incorporates an additional low pass filter (4.7 nF and 33 kΩ) to reduce beat note distortion an additional 20 dB.

Input Interface

There are two inputs to the LM1870, one for the PLL (pin 2) and the normal audio input (pin 19). The input impedance of the audio input is about 40 kΩ. The input coupling capacitor works with this input resistance and sets the low frequency response and separation.

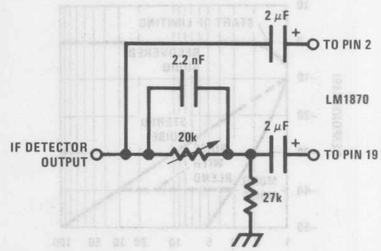
The PLL input (pin 2) locks onto the 19 kHz pilot and rejects the rest of the composite signal. For this reason it is only necessary to use a coupling capacitor large enough to insure there is no phase shift at 19 kHz. The input resistance of the PLL is 14 kΩ so a capacitor between 0.01 μF and 0.1 μF would be fine. However, the source driving this input must not be affected by this load. This is true only when the source is low impedance (less than 100Ω).

Typical FM IF circuits have detector output impedance of 5 kΩ or more. This will cause very poor low frequency response and separation unless the loading is made constant over frequency. For this reason the typical input coupling capacitor is 2 μF.

IF Correction

The separation in most radios is limited by the response of the IF. The input lead network below can often be used to improve radio separation.

IF Correction Lead Network



Power Supply

The LM1870 is designed to work on supplies from 7V to 15V. For automotive applications a regulator is recommended to protect against transients; the LM2930-8V is the ideal choice.

National Semiconductor

LM1877 Dual Power Audio Amplifier

General Description

The LM1877 is a monolithic dual power amplifier designed to deliver 2W/channel continuous into 8Ω loads. The LM1877 is designed to operate with a low number of external components, and still provide flexibility for use in stereo phonographs, tape recorders and AM–FM stereo receivers, etc. Each power amplifier is biased from a common internal regulator to provide high power supply rejection, and output Q point centering. The LM1877 is internally compensated for all gains greater than 10.

- Wide supply range, 6–24V
- Very low cross-over distortion
- Low audio band noise
- AC short circuit protected
- Internal thermal shutdown

Features

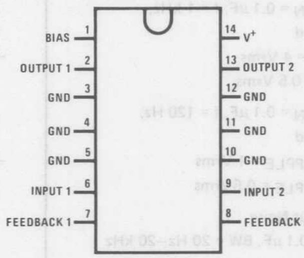
- 2W/channel
- −65 dB ripple rejection, output referred
- −65 dB channel separation, output referred

Applications

- Multi-channel audio systems
- Stereo phonographs
- Tape recorders and players
- AM–FM radio receivers
- Servo amplifiers
- Intercom systems
- Automotive products

Connection Diagram

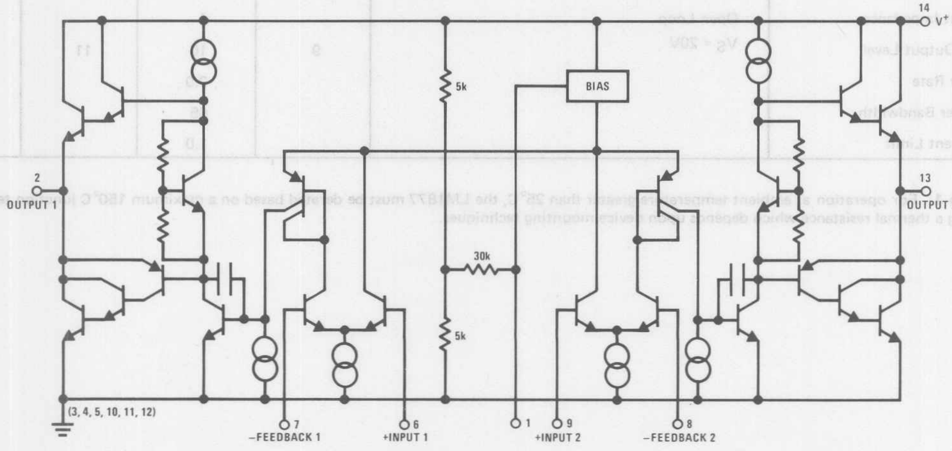
Dual-In-Line Package



TOP VIEW

Order Number LM1877N
See NS Package N14A

Equivalent Schematic Diagram



Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 seconds)	300°C

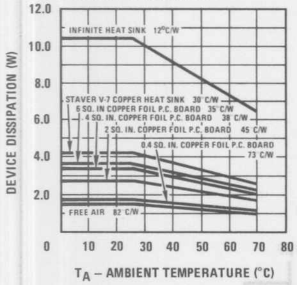
Electrical Characteristics $V_S = 20V$, $T_A = 25°C$, $R_L = 8\Omega$, $A_V = 50$ (34 dB) unless otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Total Supply Current	$P_O = 0W$		25	50	mA
Output Power	THD = 10%				
LM1877N	$V_S = 20V$, $R_L = 8\Omega$	2.0			W
Total Harmonic Distortion					
LM1877	f = 1 kHz, $V_S = 14V$				
	P_O = 50 mW/Channel		0.075		%
	P_O = 500 mW/Channel		0.045		%
	P_O = 1W/Channel		0.055		%
Output Swing	$R_L = 8\Omega$		V_S−6		Vp-p
Channel Separation	$C_F = 50\ \mu F$, $C_{IN} = 0.1\ \mu F$, f = 1 kHz,				
	Output Referred				
	$V_S = 20V$, V_O = 4 Vrms	−50	−70		dB
	$V_S = 7V$, V_O = 0.5 Vrms		−60		dB
PSRR Power Supply	$C_F = 50\ \mu F$, $C_{IN} = 0.1\ \mu F$, f = 120 Hz,				
Rejection Ratio	Output Referred				
	$V_S = 20V$, V_{RIPPLE} = 1 Vrms	−50	−65		dB
	$V_S = 7V$, V_{RIPPLE} = 0.5Vrms		−40		dB
Noise	Equivalent Input Noise				
	$R_S = 0$, $C_{IN} = 0.1\ \mu F$, BW = 20 Hz–20 kHz		2.5		μV
	Output Noise Wideband				
	$R_S = 0$, $C_{IN} = 0.1\ \mu F$, $A_V = 200$		0.80		mV
Open Loop Gain	$R_S = 0$, f = 100 kHz, $R_L = 8\Omega$		70		dB
Input Offset Voltage			15		mV
Input Bias Current			50		nA
Input Impedance	Open Loop		4		MΩ
DC Output Level	$V_S = 20V$	9	10	11	V
Slew Rate			2.0		V/μs
Power Bandwidth			65		kHz
Current Limit			1.0		A

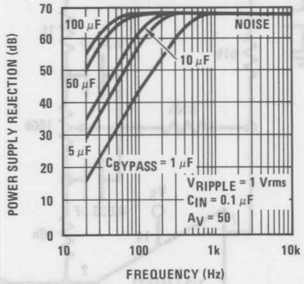
Note 1: For operation at ambient temperature greater than 25°C, the LM1877 must be derated based on a maximum 150°C junction temperature using a thermal resistance which depends upon device mounting techniques.

Typical Performance Characteristics

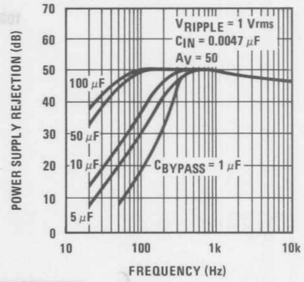
Device Dissipation vs Ambient Temperature



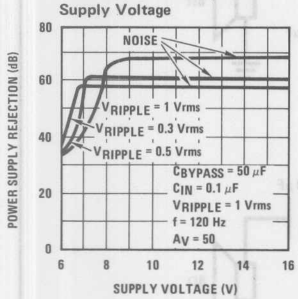
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



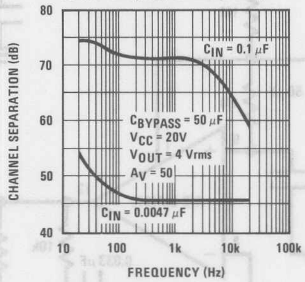
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



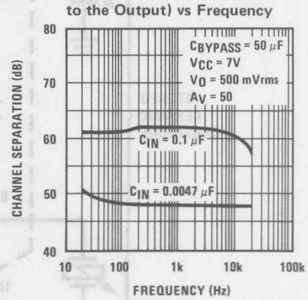
Power Supply Rejection Ratio (Referred to the Output) vs Supply Voltage



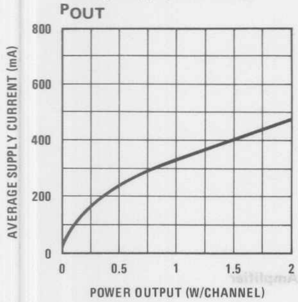
Channel Separation (Referred to the Output) vs Frequency



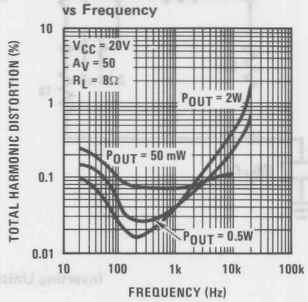
Channel Separation (Referred to the Output) vs Frequency



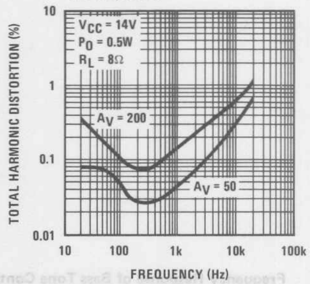
Average Supply Current vs P_{OUT}



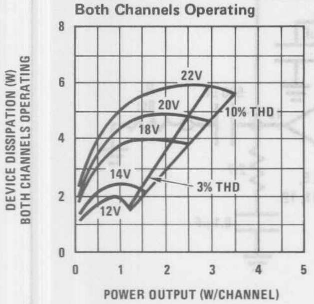
Total Harmonic Distortion vs Frequency



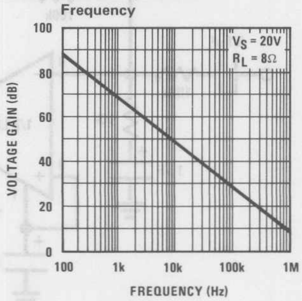
Total Harmonic Distortion vs Frequency



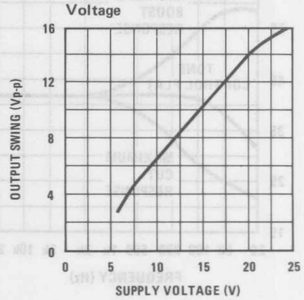
Power Dissipation (W) Both Channels Operating



Open Loop Gain vs Frequency

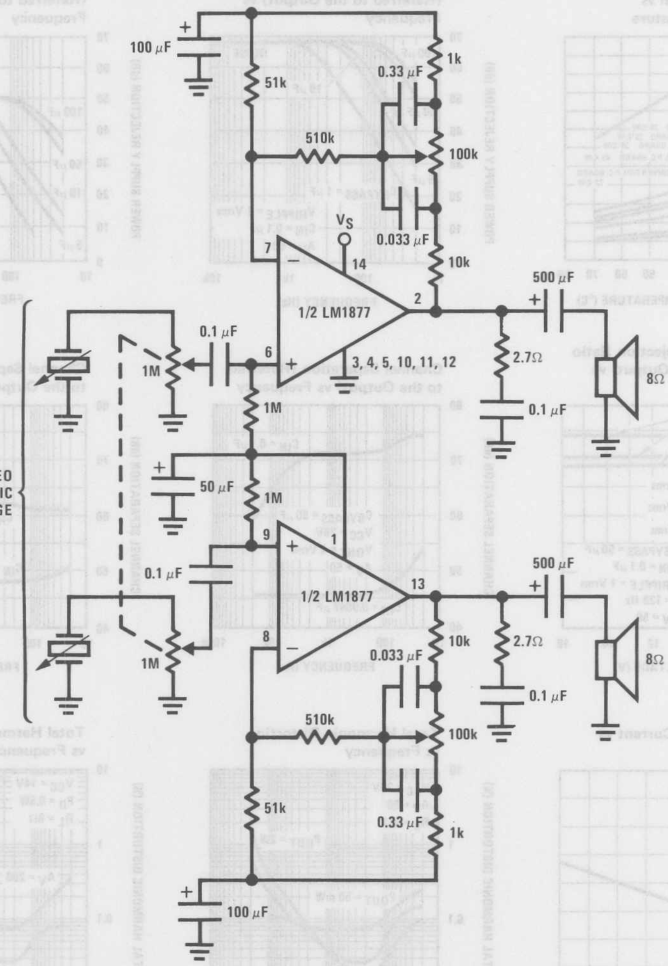


Output Swing vs Supply Voltage

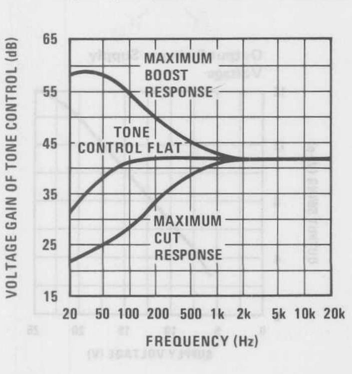


Typical Applications

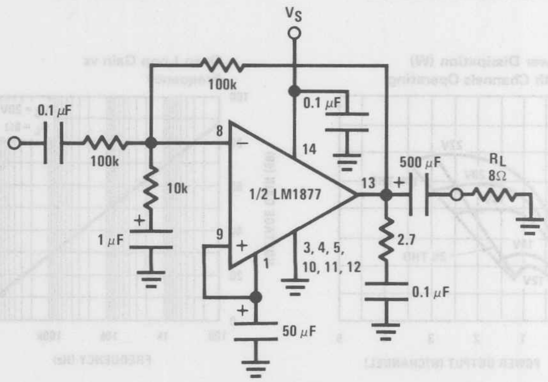
Stereo Phonograph Amplifier with Bass Tone Control



Frequency Response of Bass Tone Control

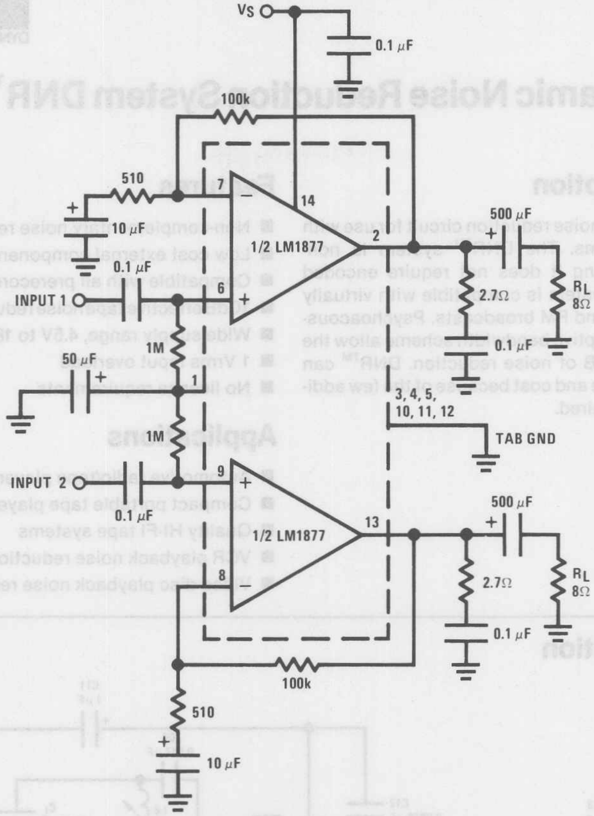


Inverting Unity Gain Amplifier

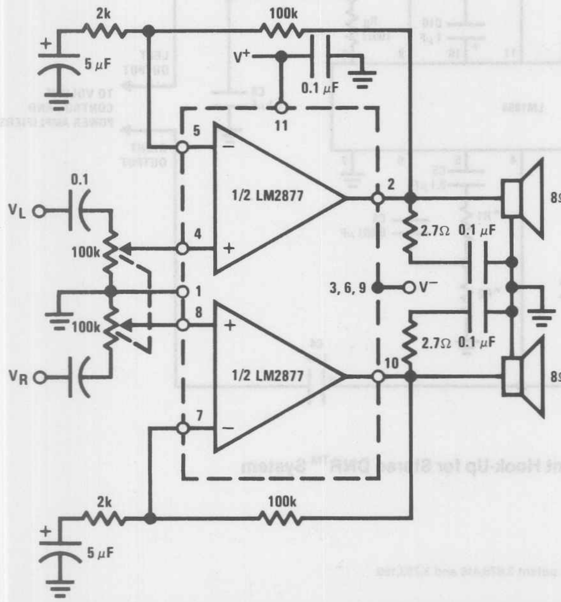


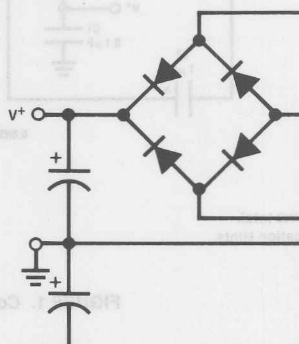
Typical Applications (Continued)

Stereo Amplifier with A_V = 200



Non-Inverting Amplifier Using Split Supply





TYPICAL SPLIT SUPPLY

LM1894 Dynamic Noise Reduction System DNR™

General Description

The LM1894 is a stereo noise reduction circuit for use with audio playback systems. The DNR™ system is non-complementary, meaning it does not require encoded source material. The system is compatible with virtually all prerecorded tapes and FM broadcasts. Psychoacoustic masking, and an adaptive bandwidth scheme allow the DNR™ to achieve 10 dB of noise reduction. DNR™ can save circuit board space and cost because of the few additional components required.

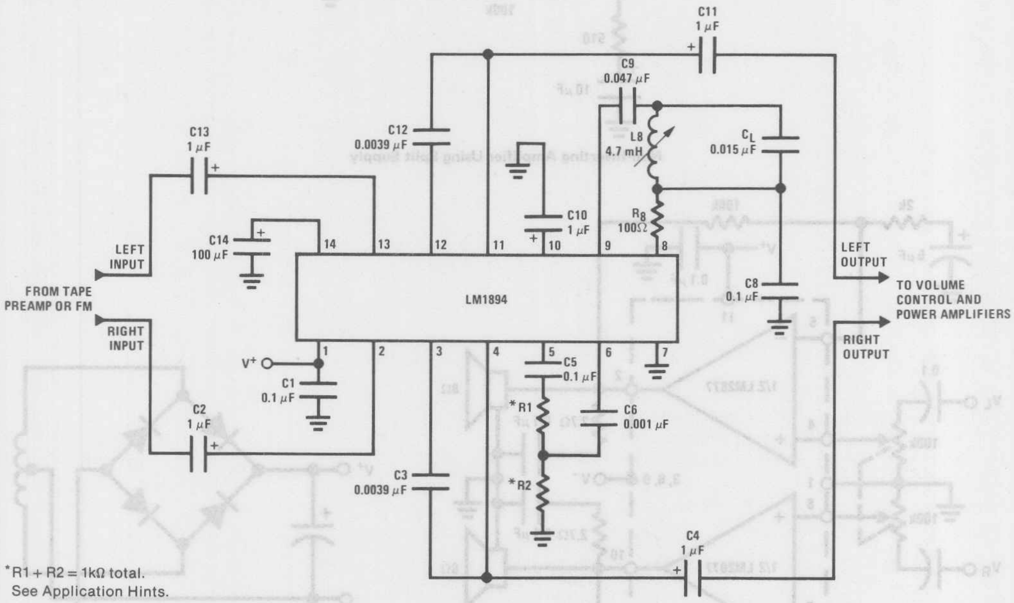
Features

- Non-complementary noise reduction, "single ended"
- Low cost external components, no critical matching
- Compatible with all prerecorded tapes and FM
- 10 dB effective tape noise reduction CCIR/ARM weighted
- Wide supply range, 4.5V to 18V
- 1 Vrms input overload
- No license requirements

Applications

- Automotive radio/tape players
- Compact portable tape players
- Quality HI-FI tape systems
- VCR playback noise reduction
- Video disc playback noise reduction

Typical Application



*R1 + R2 = 1kΩ total.
See Application Hints.

FIGURE 1. Component Hook-Up for Stereo DNR™ System

Electrical Characteristics

$V_S = 8V$, $T_A = 25°C$, $V_{IN} = 300$ mV at 1 kHz, circuit shown in *Figure 1* unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Operating Supply Range		4.5	8	18	V
Supply Current	$V_S = 8V$		17	25	mA
MAIN SIGNAL PATH					
Voltage Gain	DC Ground Pin 9, Note 2	−0.9	−1	−1.1	V/V
DC Output Voltage		3.7	4.0	4.3	V
Channel Balance	DC Ground Pin 9	−1.0		1.0	dB
Minimum Bandwidth	AC Ground Pin 9 with 0.1 μF Capacitor, Note 2	675	965	1400	Hz
Maximum Bandwidth	DC Ground Pin 9, Note 2	27	34	46	kHz
Effective Noise Reduction	CCIR/ARM Weighted, Note 3		−10	−14	dB
Total Harmonic Distortion	DC Ground Pin 9		0.05	0.1	%
Input Headroom	Maximum V_{IN} for 3% THD AC Ground Pin 9		1.0		Vrms
Output Headroom	Maximum V_{OUT} for 3% THD DC Ground Pin 9		$V_S - 1.5$		Vp-p
Signal to Noise	BW = 20 Hz–20 kHz, re 300 mV				
	AC Ground Pin 9		79		dB
	DC Ground Pin 9		77		dB
	CCIR/ARM Weighted re 300 mV, Note 4				
	AC Ground Pin 9	82	88		dB
	DC Ground Pin 9	70	76		dB
	CCIR Peak, re 300 mV, Note 5				
	AC Ground Pin 9		77		dB
	DC Ground Pin 9		64		dB
Input Impedance	Pin 2 and Pin 13	14	20	26	kΩ
Channel Separation	DC Ground Pin 9	−50	−70		dB
Power Supply Rejection	C14 = 100 μF, V_{RIPPLE} = 500 mVrms, f = 1 kHz	−40	−56		dB
Output DC Shift	Reference DVM to Pin 14 and Measure Output DC Shift from Minimum to Maximum Bandwidth, Note 6.		4.0	20	mV
CONTROL SIGNAL PATH					
Summing Amplifier Voltage Gain	Both Channels Driven	0.9	1	1.1	V/V
Gain Amplifier Input Impedance	Pin 6	24	30	39	kΩ
Voltage Gain	Pin 6 to Pin 8	21.5	24	26.5	V/V
Peak Detector Input Impedance	Pin 9	560	700	840	Ω
Voltage Gain	Pin 9 to Pin 10	30	33	36	V/V
Attack Time	Measured to 90% of Final Value with 10 kHz Tone Burst	300	500	700	μs
Decay Time	Measured to 90% of Final Value with 10 kHz Tone Burst	45	60	75	ms
DC Voltage Range	Minimum Bandwidth to Maximum Bandwidth	1.1		3.8	V

Notes

Note 1: For operation in ambient temperature above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 80°C/W junction to ambient.

Note 2: To force the DNR™ system into maximum bandwidth, DC ground the input to the peak detector, pin 9. A negative temperature coefficient of −0.5%/°C on the bandwidth, reduces the maximum bandwidth at increased ambient temperature or higher package dissipation. AC ground pin 9 or pin 6 to select minimum bandwidth. To change minimum and maximum bandwidth, see Application Hints.

Note 3: The maximum noise reduction CCIR/ARM weighted is about 14 dB. This is accomplished by changing the bandwidth from maximum to minimum. In actual operation, minimum bandwidth is not selected, a nominal minimum bandwidth of about 2 kHz gives −10 dB of noise reduction. See Application Hints.

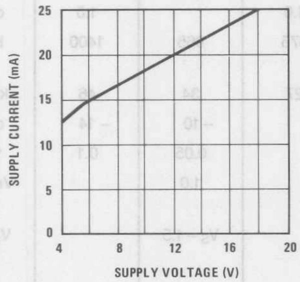
Note 4: The CCIR/ARM weighted noise is measured with a 40 dB gain amplifier between the DNR™ system and the CCIR weighting filter; it is then input referred.

Note 5: Measured using the Rhode-Schwartz psophometer.

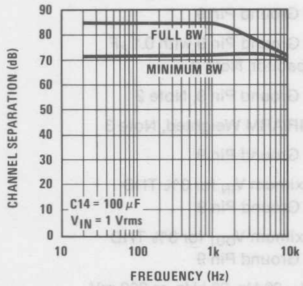
Note 6: Pin 10 is DC forced half way between the maximum bandwidth DC level and minimum bandwidth DC level. An AC 1 kHz signal is then applied to pin 10. Its peak-to-peak amplitude is V_{DC} (max BW) − V_{DC} (min BW).

Typical Performance Characteristics

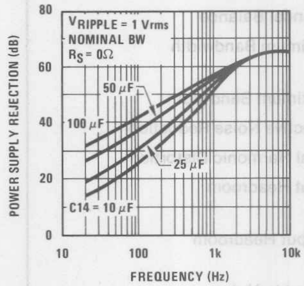
Supply Current vs Supply Voltage



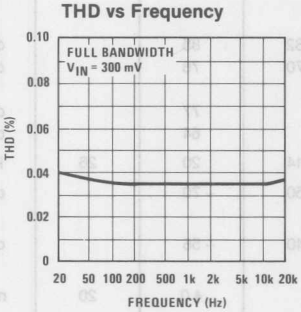
Channel Separation (Referred to the Output) vs Frequency



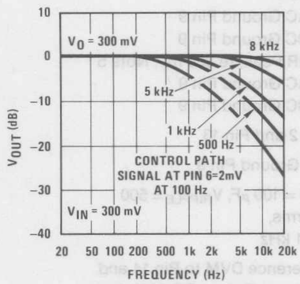
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



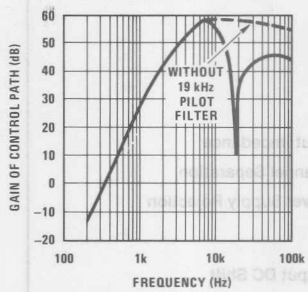
THD vs Frequency



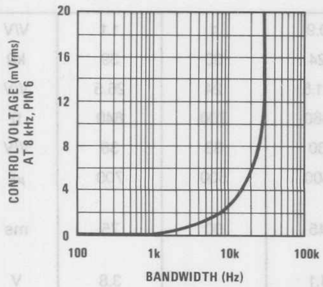
−3 dB Bandwidth vs Frequency and Control Signal



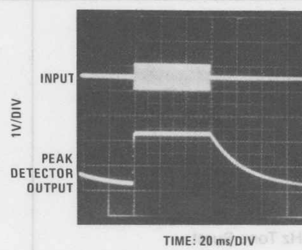
Gain of Control Path vs Frequency (with 19 kHz FM Pilot Filter)



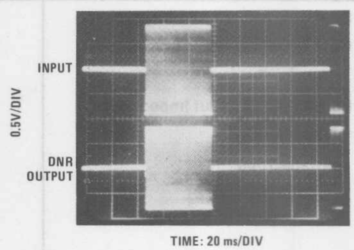
Main Signal Path Bandwidth vs Control Voltage



Peak Detector Response



Output Response

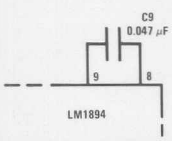


External Component Guide *(Figure 1)*

Component	Value	Purpose
C1	0.1 µF–100 µF	May be part of power supply, or may be added to suppress power supply oscillation.
C2, C13	1 µF	Blocks DC, pin 2 and pin 13 are at DC potential of $V_S/2$. C2, C13 form a low frequency pole with 20k R_{IN}. $f_L = \frac{1}{2\pi C2\, R_{IN}}$
C14	25 µF–100 µF	Improves power supply rejection.
C3, C12	0.0039 µF	Forms integrator with internal gm block and op amp. Sets bandwidth conversion gain of 27 Hz/µA of gm current.
C4, C11	1 µF	Output coupling capacitor. Output is at DC potential of $V_S/2$.
C5	0.1 µF	Works with R1 and R2 to attenuate low frequency transients which could disturb control path operation. $f_5 = \frac{1}{2\pi C5\,(R1 + R2)} = 1.6\ \text{kHz}$
C6	0.001 µF	Works with input resistance of pin 6 to form part of control path frequency weighting. $f_6 = \frac{1}{2\pi C6\, R_{PIN\,6}} = 5.3\ \text{kHz}$
C8	0.1 µF	Combined with L8 and C_L forms 19 kHz filter for FM pilot. This is only required in FM applications (Note 1).
L8, C_L	4.7 mH, 0.015 µF	Forms 19 kHz filter for FM pilot. L8 is Toko coil CAN-1A185HM* (Note 1).
C9	0.047 µF	Works with input resistance of pin 9 to form part of control path frequency weighting. $f_9 = \frac{1}{2\pi C9\, R_{PIN\,9}} = 4.8\ \text{kHz}$
C10	1 µF	Sets attack and decay time of peak detector.
R1, R2	1 kΩ	Sensitivity resistors set the noise threshold. Reducing attenuation causes larger signals to be peak detected and larger bandwidth in main signal path. Total value of R1 + R2 should equal 1 kΩ.
R8	100Ω	Forms RC roll-off with C8. This is only required in FM applications.

* Toko America Inc., 5520 W. Touhy Avenue, Skokie, Illinois 60077

Note 1: When FM applications are not required, pin 8 and pin 9 hook-up as follows:



Circuit Operation

The LM1894 has two signal paths, a main signal path and a bandwidth control path. The main path is an audio low pass filter comprised of a gm block with a variable current, and an op amp configured as an integrator. As seen in *Figure 2*, DC feedback constrains the low frequency gain to $A_V = -1$. Above the cutoff frequency of the filter, the output decreases at −6 dB/oct due to the action of the 0.0039 µF capacitor.

The purpose of the control path is to generate a bandwidth control signal which replicates the ear's sensitivity to noise in the presence of a tone. A single control path is used for both channels to keep the stereo image from wandering. This is done by adding the right and left channels together in the summing amplifier of *Figure 2*. The R1, R2 resistor divider adjusts the incoming noise level to open slightly the bandwidth of the low pass filter. Control path gain is about 60 dB and is set by the gain amplifier and peak detector gain. This large gain is needed to ensure the low pass filter bandwidth can be opened by very low noise floors. The capacitors between the summing amplifier output and the peak detector input determine the frequency weighting as shown in the typical performance curves. The 1 µF capacitor at pin 10, in conjunction with internal resistors, sets the attack and decay times. The voltage is converted into a proportional current which is fed into the gm blocks. The bandwidth sensitivity to gm current is 27 Hz/µA. In FM stereo applications a 19 kHz pilot filter is inserted between pin 8 and pin 9 as shown in *Figure 1.*

Figure 3 is an interesting curve and deserves some discussion. Although the output of the DNR™ system is a linear function of input signal, the −3 dB bandwidth is not. This is due to the non-linear nature of the control path. The DNR™ system has a uniform frequency response, but looking at the −3 dB bandwidth on a steady state basis with a single frequency input can be misleading. It must be remembered that a single input frequency can only give a single −3 dB bandwidth and the roll-off from this point must be a smooth −6 dB/oct.

A more accurate evaluation of the frequency response can be seen in *Figure 4*. In this case the main signal path is frequency swept, while the control path has a constant frequency applied. It can be seen that different control path frequencies each give a distinctive gain roll-off.

Psychoacoustic Basics

The dynamic noise reduction system is a low pass filter that has a variable bandwidth of 1 kHz to 30 kHz, dependent on music spectrum. The DNR™ system operates on three principles of psychoacoustics.

1. White noise can mask pure tones. The total noise energy required to mask a pure tone must equal the energy of the tone itself. Within certain limits, the wider the band of masking noise about the tone, the lower the noise amplitude need be. As long as the total energy of the noise is equal to or greater than the energy of the tone, the tone will be inaudible. This principle may be turned around; when music is present, it is capable of masking noise in the same bandwidth.

open the bandwidth to 90% of the maximum value in less

Block Diagram

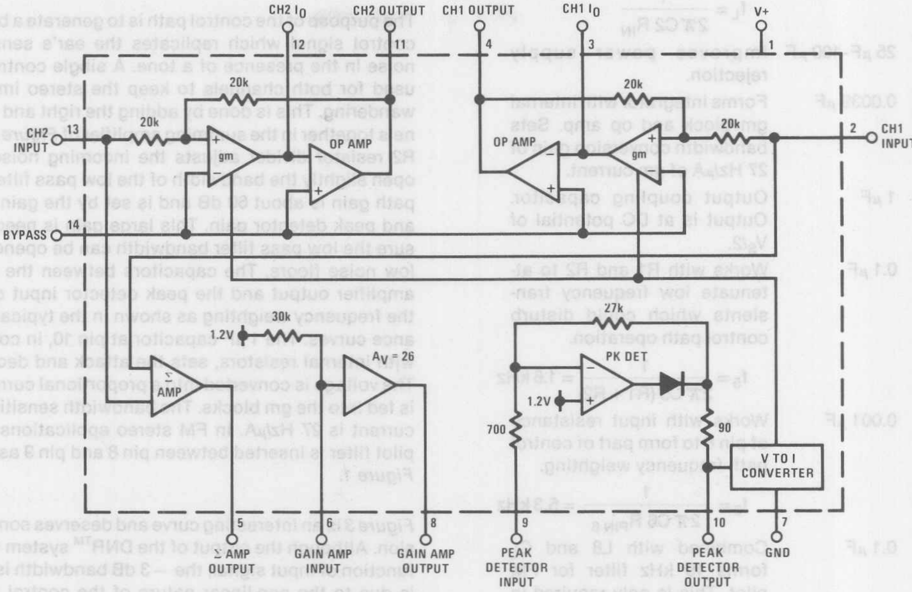


FIGURE 2

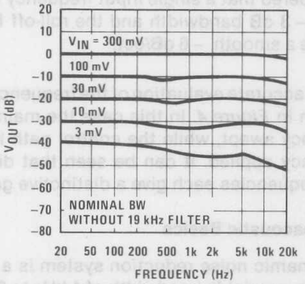


FIGURE 3. Output vs Frequency

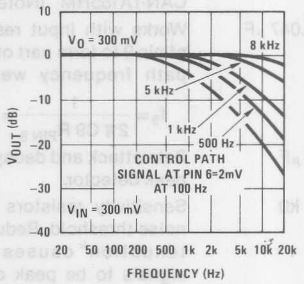


FIGURE 4. −3 dB Bandwidth vs Frequency and Control Signal

3. Reducing the audio bandwidth reduces the audibility of noise. Audibility of noise is dependent on noise spectrum, or how the noise energy is distributed with frequency. Depending on the tape and the recorder equalization, tape noise spectrum may be slightly rolled off with frequency on a per octave basis. The ear sensitivity on the other hand greatly increases between 2 kHz and 10 kHz. Noise in this region is extremely audible. The DNR™ system low pass filters this noise. Low frequency music will not appreciably open the DNR™ bandwidth, thus 2 kHz to 20 kHz noise is not heard.

Application Hints

The DNR™ system should always be placed before tone and volume controls as shown in *Figure 1*. This is because any adjustment of these controls would alter the noise floor seen by the DNR™ control path. The sensitivity resistors R1 and R2 may need to be switched with the input selector, depending on the noise floors of different sources, i.e., tape, FM, phono. To determine the value of R1 and R2 in a tape system for instance; apply tape noise (no program material) and adjust the ratio of R1 and R2 to open slightly the bandwidth of the main signal path. This can easily be done by viewing the capacitor voltage of pin 10 with an oscilloscope, or by using the circuit of *Figure 5*. This circuit gives an LED display of the voltage on the peak detector capacitor. Adjust the values of R1 and R2 (their sum is always 1 kΩ) to light the LEDs of pin 1 and pin 18. The LED bar graph does not indicate signal level, but rather instantaneous bandwidth of the two filters; it should not be used as a signal-level indicator. For greater flexibility in setting the bandwidth sensitivity, R1 and R2 could be replaced by a 1 kΩ potentiometer.

To change the minimum and maximum value of bandwidth, the integrating capacitors, C3 and C12, can be scaled up or down. Since the bandwidth is inversely proportional to the capacitance, changing this 0.0039 μF capacitor to 0.0033 μF will change the typical bandwidth from 965 Hz–34 kHz to 1.1 kHz–40 kHz. With C3 and C12 set at 0.0039 μF, the maximum bandwidth is typically 34 kHz. A double pole double throw switch can be used to completely bypass DNR.

The capacitor on pin 10 in conjunction with internal resistors sets the attack and decay times. The attack time can be altered by changing the size of C10. Decay times can be decreased by paralleling a resistor with C10, and increased by increasing the value of C10.

When measuring the amount of noise reduction of the DNR™ system, the frequency response of the cassette should be flat to 10 kHz. The CCIR weighting network has substantial gain to 8 kHz and any additional roll-off in the cassette player will reduce the benefits of DNR™ noise reduction. A typical signal-to-noise measurement circuit is shown in *Figure 6*. The DNR™ system should be switched from maximum bandwidth to nominal bandwidth with tape noise as a signal source. The reduction in measured noise is the signal-to-noise ratio improvement.

FOR FURTHER READING

Tape Noise Levels

1. "A Wide Range Dynamic Noise Reduction System", Blackmer, *'dB' Magazine,* August-September 1972, Volume 6, #8.

2. "Dolby B-Type Noise Reduction System", Berkowitz and Gundry, *Sert Journal,* May-June 1974, Volume 8.

3. "Cassette vs Elcaset vs Open Reel", Toole, *Audioscene Canada,* April 1978.

4. "CCIR/ARM: A Practical Noise Measurement Method", Dolby, Robinson, Gundry, *JAES,* 1978.

Noise Masking

1. "Masking and Discrimination", Bos and De Boer, *JAES,* Volume 39, #4, 1966.

2. "The Masking of Pure Tones and Speech by White Noise", Hawkins and Stevens, *JAES,* Volume 22, #1, 1950.

3. "Sound System Engineering", Davis, Howard W. Sams and Co.

4. "High Quality Sound Reproduction", Moir, Chapman Hall, 1960.

5. "Speech and Hearing in Communication", Fletcher, Van Nostrand, 1953.

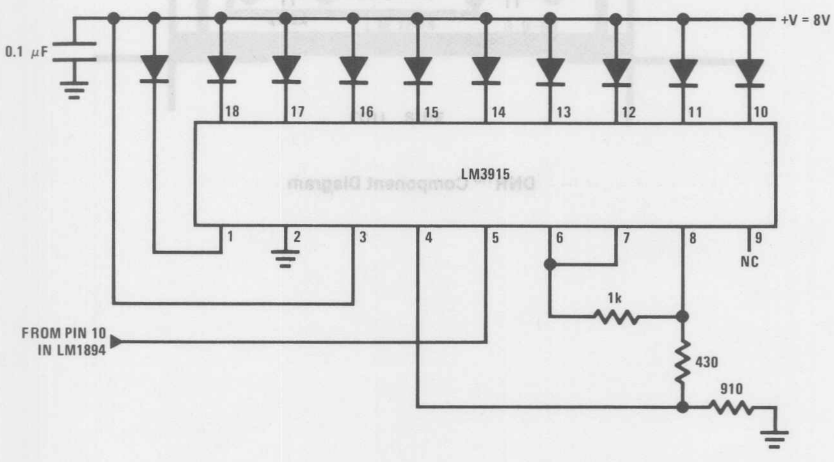


FIGURE 5. Bar Graph Display of Peak Detector Voltage

Application Hints (Continued)

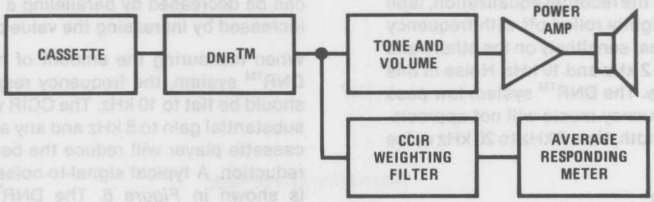
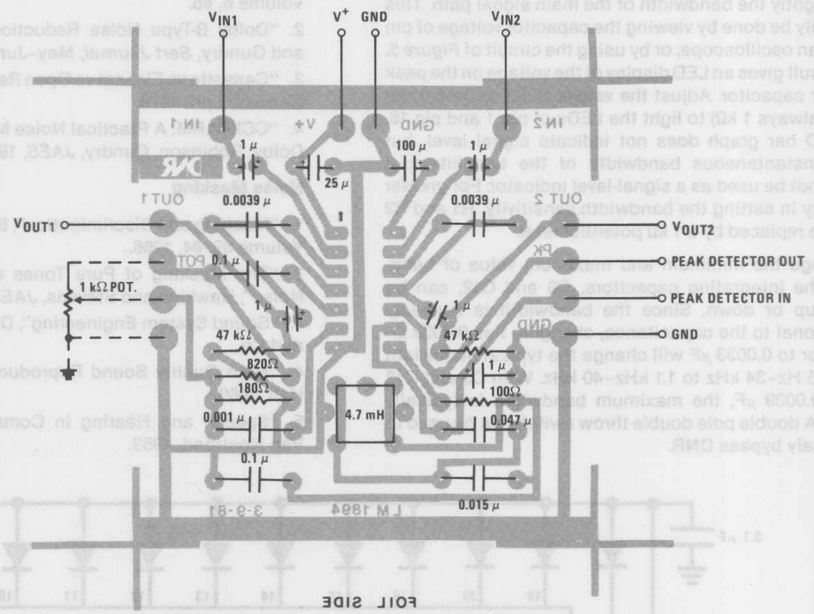


FIGURE 6. Technique for Measuring S/N Improvement of the DNR™ System

Printed Circuit Layout



DNR™ Component Diagram

National Semiconductor

LM1895/LM2895 Audio Power Amplifier

General Description

The LM1895 is a 6V audio power amplifier designed to deliver 1W into 4Ω. Utilizing a unique patented compensation scheme, the LM1895 is ideal for sensitive AM radio applications. This new circuit technique exhibits lower noise, lower distortion, and less AM radiation than conventional designs. The amplifier's supply range (3V–9V) is ideal for battery operation. The LM1895 is packaged in an 8-pin miniDIP for minimum PC board space. For higher supplies (V_S>9V) the LM2895 is available in an 11-lead single-in-line package. The 11-lead package has been redesigned, resulting in a slightly degraded thermal characteristic shown in the figure Device Dissipation vs Ambient Temperature.

Features

- Guaranteed low crossover distortion
- Low AM radiation
- Low noise
- 3V, 4Ω, P_O = 250 mW
- Wide supply operation 3V–15V (LM2895)
- Low distortion
- No turn on "pop"
- Smooth waveform clipping
- 8-pin miniDIP (LM1895)
- 12V, 4Ω, P_O = 4W (LM2895)
- Tested for low crossover distortion

Applications

- Compact AM-FM radios
- Battery operated tape player amplifiers
- Line driver

Typical Applications

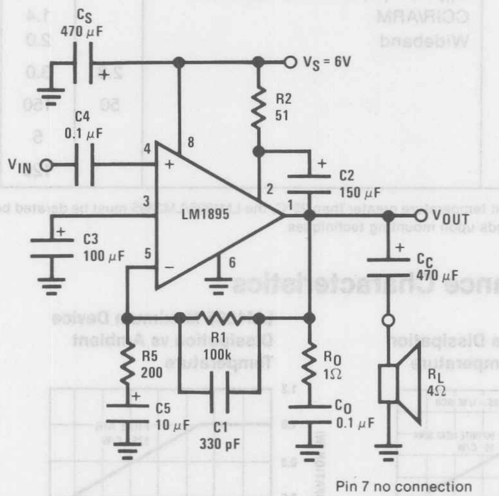


FIGURE 1. LM1895 with A_V = 500, BW = 5 kHz, AM Radio Application (V_{IN} = 4.2 mV for Full Power Output)

Order Number LM1895N
See NS Package N08A

Order Number LM2895P
See NS Package P11A

Operating Temperature (Note 1)	0°C to +70°C
Storage Temperature	−65°C to +150°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

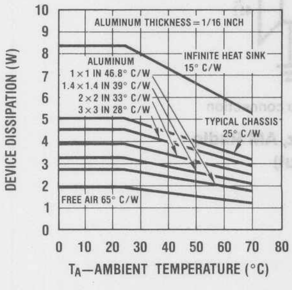
Unless otherwise specified, $T_A = 25°C$, $A_V = 200$(46 dB). For the LM1895, $V_S = 6V$ and $R_L = 4\Omega$. For the LM2895, $T_{TAB} = 25°C$, $V_S = 12V$ and $R_L = 4\Omega$. Test circuit shown in *Figure 2*.

Parameter	Conditions	LM1895 Min	LM1895 Typ	LM1895 Max	LM2895 Min	LM2895 Typ	LM2895 Max	Units
Supply Current	$P_O = 0W$,		8	14		12	20	mA
Operating Supply Voltage		3		10	3		15	V
Output Power	THD = 10%, f = 1 kHz							
LM1895N	$V_S = 6V$, $R_L = 4\Omega$ } $T_A = 25°C$	0.9	1.1					W
	$V_S = 9V$, $R_L = 8\Omega$		1.1					W
LM2895P	$V_S = 12V$, $R_L = 4\Omega$ } $T_{TAB} = 25°C$				3.6	4.3		W
	$V_S = 12V$, $R_L = 8\Omega$					2.5		W
Distortion	f = 1 kHz							
	$P_O = 50$ mW		0.27			0.27		%
	$P_O = 0.5W$		0.20			0.20		%
	$P_O = 1.0W$					0.15		%
	f = 20 kHz, $P_O = 100$ mW, $V_S = 3.6V$			3.0			3.0	%
Crossover Distortion	f = 20 kHz, $R_L = 4\Omega$, $P_O = 100$ mW, $V_{CC} = 3.6V$			3			3	%
Power Supply Rejection Ratio (PSRR)	$C_{BY} = 100\ \mu F$, f = 1 kHz, $C_{IN} = 0.1\ \mu F$ Output Referred, $V_{RIPPLE} = 250$ mV	40	52		40	52		dB
Noise	Equivalent Input Noise $R_S = 0$,							
	$C_{IN} = 0.1\ \mu F$, BW = 20 − 20 kHz		1.4			1.4		μV
	CCIR/ARM		1.4			1.4		μV
	Wideband		2.0			2.0		μV
DC Output Level		2.8	3.0	3.2	5.6	6.0	6.4	V
Input Impedance		50	150	350	50	150	350	kΩ
Input Offset Voltage			5			5		mV
Input Bias Current			120			120		nA

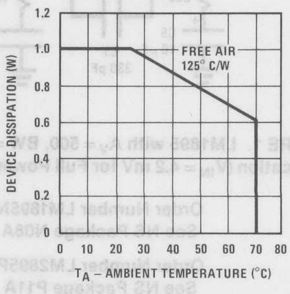
Note 1: For operation at ambient temperature greater than 25°C, the LM1895/LM2895 must be derated based on a maximum junction temperature using a thermal resistance which depends upon mounting techniques.

Typical Performance Characteristics

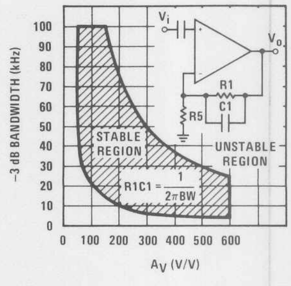
LM2895 Device Dissipation vs Ambient Temperature



LM1895 Maximum Device Dissipation vs Ambient Temperature

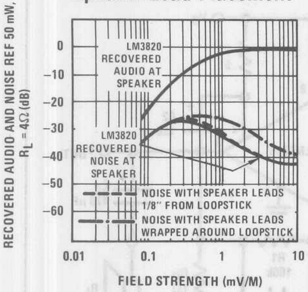


− 3 dB Bandwidth vs Voltage Gain for Stable Operation

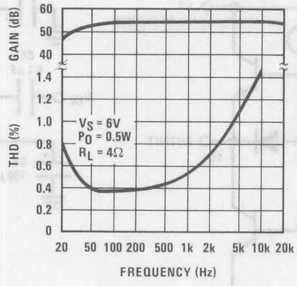


Typical Performance Characteristics (Continued)

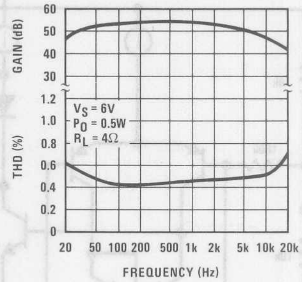
AM Recovered Audio and Noise vs Field Strength for Different Speaker Lead Placement



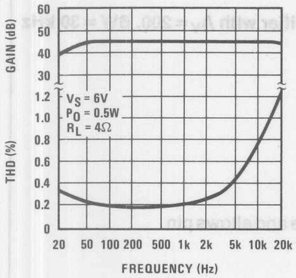
THD and Gain vs Frequency $A_V = 54$ dB, BW = 30 kHz



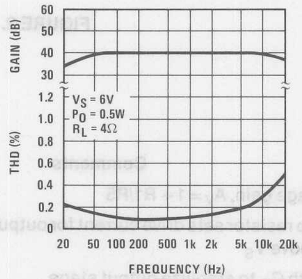
THD and Gain vs Frequency $A_V = 54$ dB, BW = 5 kHz



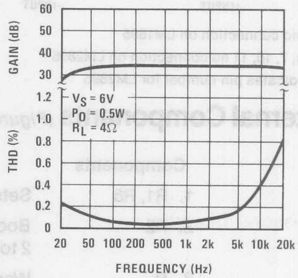
THD and Gain vs Frequency $A_V = 46$ dB, BW = 30 kHz



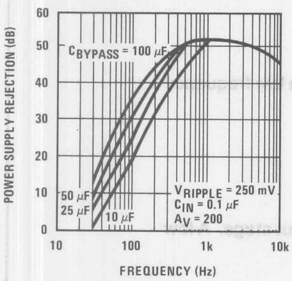
THD and Gain vs Frequency $A_V = 40$ dB, BW = 20 kHz



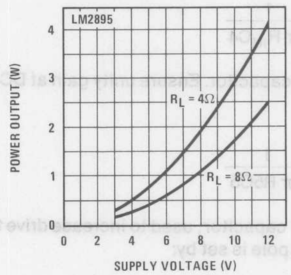
THD and Gain vs Frequency $A_V = 34$ dB, BW = 50 kHz



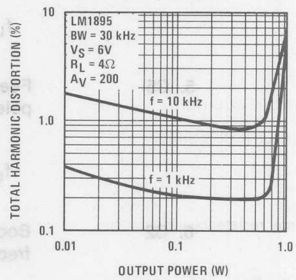
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



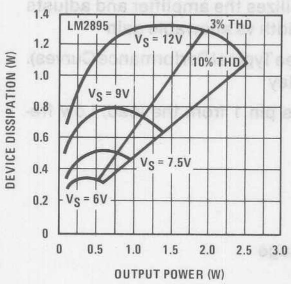
Power Output vs Supply Voltage



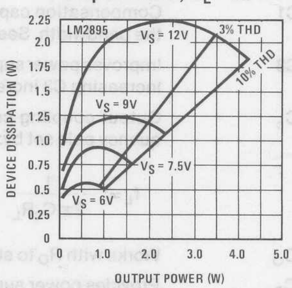
Total Harmonic Distortion vs Output Power



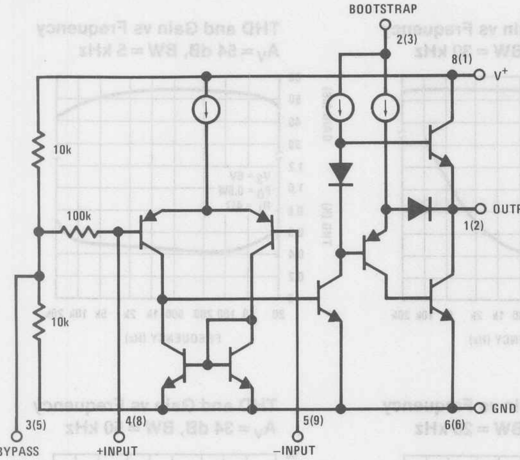
Power Dissipation vs Output Power, $R_L = 8\Omega$



Power Dissipation vs Output Power, $R_L = 4\Omega$



Equivalent Schematic



Pin 7 no connection on LM1895

Pins 4, 7, 10, 11 no connection on LM2895

( ) indicates pin number for LM2895

Typical Applications (Continued)

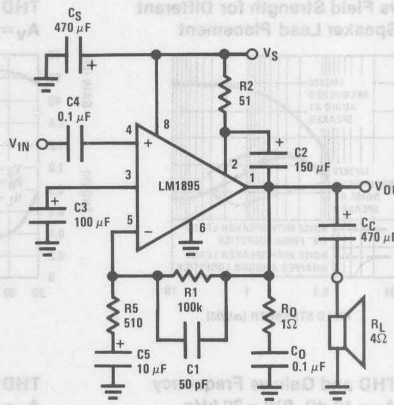


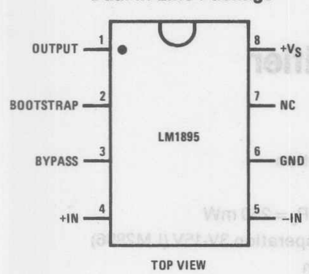
FIGURE 2. Amplifier with $A_V = 200$, BW = 30 kHz

External Components (*Figure 2*)

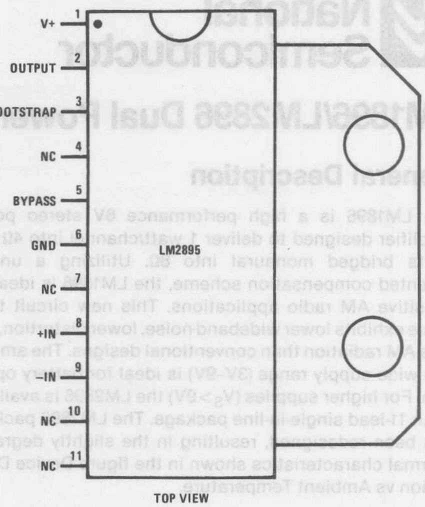
Components	Comments
1. R1, R5	Sets voltage gain, $A_V = 1 + R1/R5$
2. R2	Bootstrap resistor sets drive current for output stage and allows pin 2 to go above V_S
3. R_O	Works with C_O to stabilize output stage
4. C4	Input coupling capacitor. Pin 4 is at a DC potential of $V_S/2$. Low frequency pole set by: $$f_L = \frac{1}{2\pi R_{IN} C4}$$
5. C5	Feedback capacitor. Ensure unity gain at DC. Also a low frequency pole at: $$f_L = \frac{1}{2\pi\ R5C5}$$
6. C2	Bootstrap capacitor, used to increase drive to output stage. A low frequency pole is set by: $$f_L = \frac{1}{2\pi\ R2C2}$$
7. C1	Compensation capacitor. This stabilizes the amplifier and adjusts the bandwidth. See curve of bandwidth vs allowable gain
8. C3	Improves power supply rejection. (See Typical Performance Curves). Increasing C3 increases turn-on delay
9. C_c	Output coupling capacitor. Isolates pin 1 from the load. Low frequency pole set by: $$f_L = \frac{1}{2\pi\ C_c R_L}$$
10. C_O	Works with R_O to stabilize output stage
11. C_S	Provides power supply filtering

Connection Diagrams

Dual-In-Line Package



Single-In-Line Package



Application Hints

AM Radios

The LM1895/LM2895 have been designed to fill a wide range of audio power applications. A common problem with IC audio power amplifiers has been poor signal-to-noise performance when used in AM radio applications. In a typical radio application, the loopstick antenna is in close proximity to the audio amplifier. Current flowing in the speaker and power supply leads can cause electromagnetic coupling to the loopstick, resulting in system oscillation. In addition, most audio power amplifiers are not optimized for lowest noise because of compensation requirements. If noise from the audio amplifier radiates into the AM section, the sensitivity and signal-to-noise ratio will be degraded.

The LM1895 exhibits extremely low wideband noise due in part to an external capacitor C1 which is used to tailor the bandwidth. The circuit shown in *Figure 2* is capable of a signal-to-noise ratio in excess of 60 dB referred to 50 mW. Capacitor C1 not only limits the closed loop bandwidth, it also provides overall loop compensation. Neglecting C5 in *Figure 2*, the gain is:

$$A_V(S) = \frac{S + A_V\omega_o}{S + \omega_o}$$

$$\text{where} \quad A_V = \frac{R1 + R5}{R5}, \qquad \omega_o = \frac{1}{R1C1}$$

A curve of −3 dB BW (ω_o) vs A_V is shown in the Typical Performance Curves.

Figure 3 shows a plot of recovered audio as a function of field strength in μV/M. The receiver section in this example is an LM3820. The power amplifier is located about two inches from the loopstick antenna. Speaker leads run parallel to the loopstick and are 1/8 inch from it. Referenced to a 20 dB S/N ratio, the improvement in noise performance over conventional designs is about 10 dB. This corresponds to an increase in usable sensitivity of about 8.5 dB.

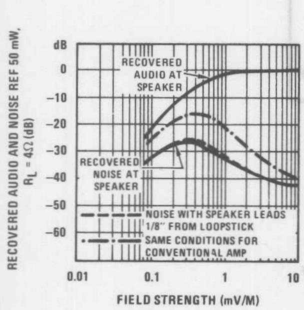


FIGURE 3. Improved AM Sensitivity Over Conventional Design

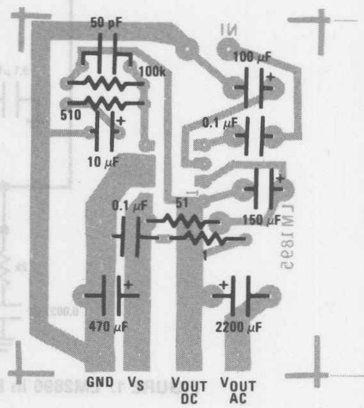


FIGURE 4. Printed Circuit Board Layout for LM1895

LM1896/LM2896 Dual Power Audio Amplifier

General Description

The LM1896 is a high performance 6V stereo power amplifier designed to deliver 1 watt/channel into 4Ω or 2 watts bridged monaural into 8Ω. Utilizing a unique patented compensation scheme, the LM1896 is ideal for sensitive AM radio applications. This new circuit technique exhibits lower wideband noise, lower distortion, and less AM radiation than conventional designs. The amplifier's wide supply range (3V–9V) is ideal for battery operation. For higher supplies ($V_S > 9V$) the LM2896 is available in an 11-lead single-in-line package. The LM2896 package has been redesigned, resulting in the slightly degraded thermal characteristics shown in the figure Device Dissipation vs Ambient Temperature.

Features

- Low AM radiation
- Low noise
- 3V, 4Ω, stereo $P_o = 250$ mW
- Wide supply operation 3V-15V (LM2896)
- Low distortion
- No turn on "pop"
- Adjustable voltage gain and bandwidth
- Smooth waveform clipping
- $P_o = 9W$ bridged, LM2896

Applications

- Compact AM-FM radios
- Stereo tape recorders and players
- High power portable stereos

Typical Applications

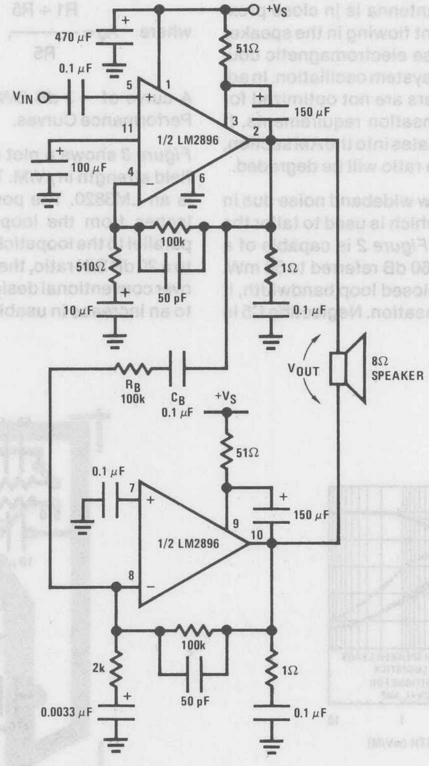


FIGURE 1. LM2896 in Bridge Configuration ($A_V = 400$, BW = 20 kHz)

Order Number LM1896N
See NS Package N14A

Order Number LM2896P
See NS Package P11A

Absolute Maximum Ratings

Supply Voltage	
LM1896	$V_S = 12V$
LM2896	$V_S = 18V$
Operating Temperature (Note 1)	0°C to +70°C
Storage Temperature	−65°C to +150°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

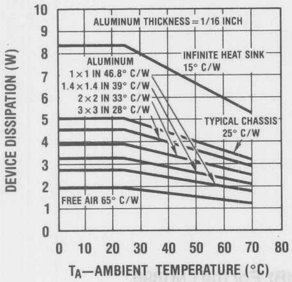
Unless otherwise specified, $T_A = 25°C$, $A_V = 200$ (46 dB). For the LM1896, $V_S = 6V$ and $R_L = 4\Omega$. For LM2896, $T_{TAB} = 25°C$, $V_S = 12V$ and $R_L = 8\Omega$. Test circuit shown in *Figure 2*.

Parameter	Conditions	LM1896 Min	LM1896 Typ	LM1896 Max	LM2896 Min	LM2896 Typ	LM2896 Max	Units
Supply Current	$P_o = 0W$, Dual Mode		15	25		25	40	mA
Operating Supply Voltage		3		10	3		15	V
Output Power	THD = 10%, f = 1 kHz							
LM1896N-1	$V_S = 6V$, $R_L = 4\Omega$ Dual Mode, $T_A = 25°C$	0.9	1.1					W
LM1896N-2	$V_S = 6V$, $R_L = 8\Omega$ Bridge Mode, $T_A = 25°C$	1.8	2.1					W
	$V_S = 9V$, $R_L = 8\Omega$ Dual Mode, $T_A = 25°C$		1.3					W
LM2896P-1	$V_S = 12V$, $R_L = 8\Omega$ Dual Mode, $T_{TAB} = 25°C$				2.0	2.5		W
LM2896P-2	$V_S = 12V$, $R_L = 8\Omega$ Bridge Mode, $T_{TAB} = 25°C$				7.2	9.0		W
	$V_S = 9V$, $R_L = 4\Omega$ Bridge Mode, $T_{TAB} = 25°C$					7.8		W
	$V_S = 9V$, $R_L = 4\Omega$ Dual Mode, $T_{TAB} = 25°C$					2.5		W
Distortion	f = 1 kHz							
	$P_o = 50$ mW		0.09			0.09		%
	$P_o = 0.5W$		0.11			0.11		%
	$P_o = 1W$					0.14		%
Power Supply Rejection Ratio (PSRR)	$C_{BY} = 100\ \mu F$, f = 1 kHz, $C_{IN} = 0.1\ \mu F$ Output Referred, $V_{RIPPLE} = 250$ mV	−40	−54		−40	−54		dB
Channel Separation	$C_{BY} = 100\ \mu F$, f = 1 kHz, $C_{IN} = 0.1\ \mu F$ Output Referred	−50	−64		−50	−64		dB
Noise	Equivalent Input Noise $R_S = 0$, $C_{IN} = 0.1\ \mu F$, BW = 20 − 20 kHz		1.4			1.4		μV
	CCIR/ARM		1.4			1.4		μV
	Wideband		2.0			2.0		μV
DC Output Level		2.8	3	3.2	5.6	6	6.4	V
Input Impedance		50	100	350	50	100	350	kΩ
Input Offset Voltage			5			5		mV
Voltage Difference Between Outputs	LM1896N-2, LM2896P-2		10	20		10	20	mV
Input Bias Current			120			120		nA

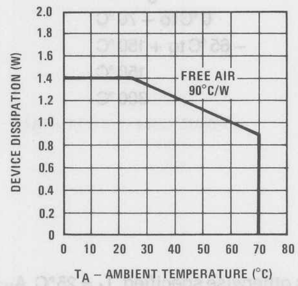
Note 1: For operation at ambient temperature greater than 25°C, the LM1896/LM2896 must be derated based on a maximum 150°C junction temperature using a thermal resistance which depends upon mounting techniques.

Typical Performance Curves

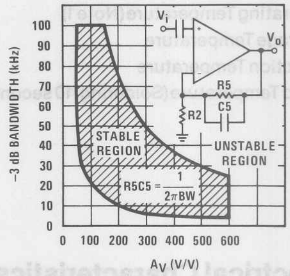
LM2896 Device Dissipation vs Ambient Temperature



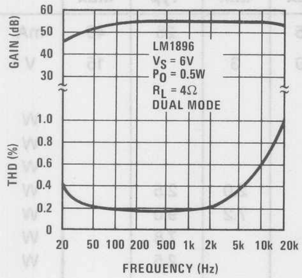
LM1896 Maximum Device Dissipation vs Ambient Temperature



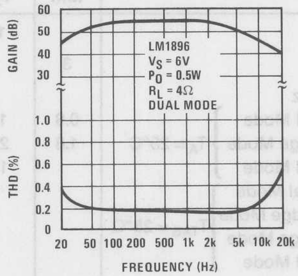
– 3 dB Bandwidth vs Voltage Gain for Stable Operation



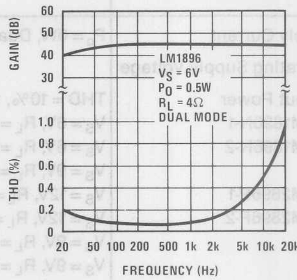
THD and Gain vs Frequency $A_V = 54$ dB, BW = 30 kHz



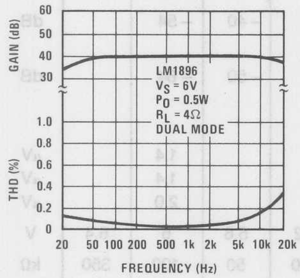
THD and Gain vs Frequency $A_V = 54$ dB, BW = 5 kHz



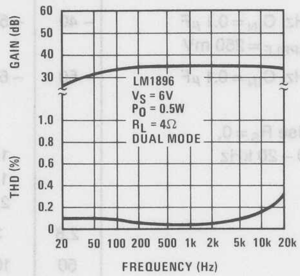
THD and Gain vs Frequency $A_V = 46$ dB, BW = 50 kHz



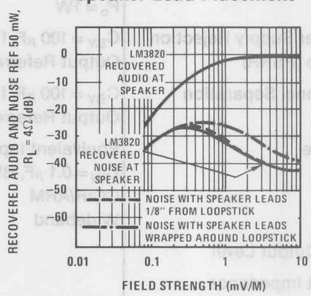
THD and Gain vs Frequency $A_V = 40$ dB, BW = 20 kHz



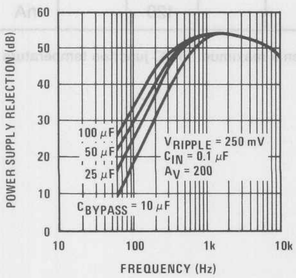
THD and Gain vs Frequency $A_V = 34$ dB, BW = 50 kHz



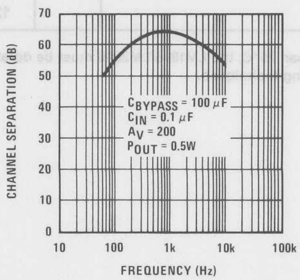
AM Recovered Audio and Noise vs Field Strength for Different Speaker Lead Placement



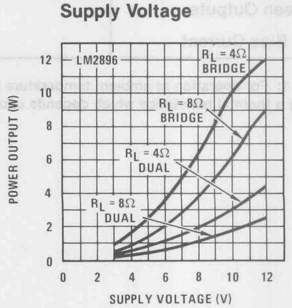
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



Channel Separation (Referred to the Output) vs Frequency

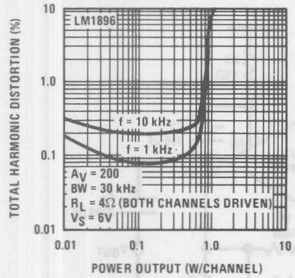


Power Output vs Supply Voltage

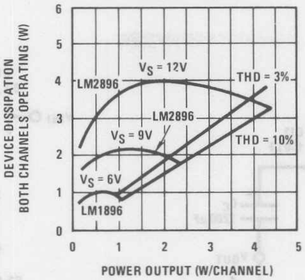


Typical Performance Curves (Continued)

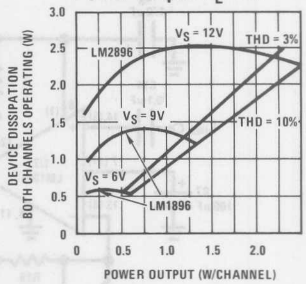
Total Harmonic Distortion vs Power Output



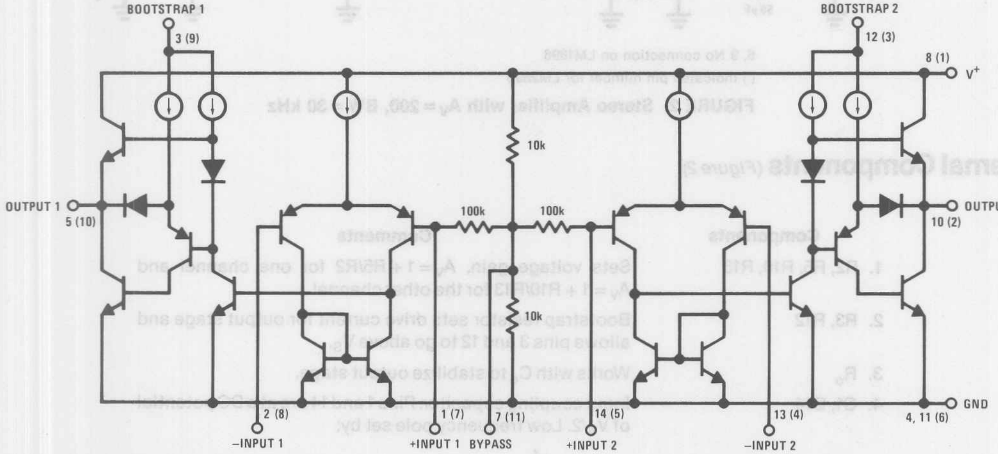
Power Dissipation vs Power Output $R_L = 4\Omega$



Power Dissipation vs Power Output $R_L = 8\Omega$



Equivalent Schematic

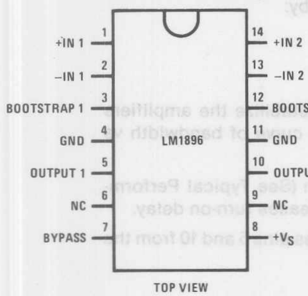


6, 9 No connection on LM1896

( ) Indicates pin number for LM2896

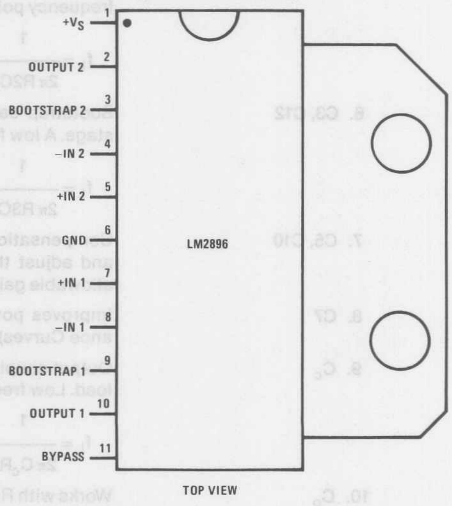
Connection Diagrams

Dual-In-Line Package

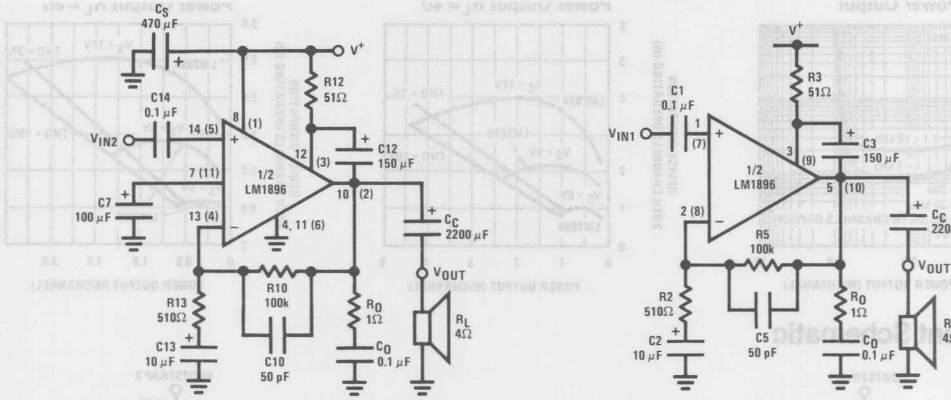


TOP VIEW

Single-In-Line Package



TOP VIEW



6, 9 No connection on LM1896

( ) Indicates pin number for LM2896

FIGURE 2. Stereo Amplifier with $A_V = 200$, BW = 30 kHz

External Components *(Figure 2)*

Components	Comments
1. R2, R5, R10, R13	Sets voltage gain, $A_V = 1 + R5/R2$ for one channel and $A_V = 1 + R10/R13$ for the other channel.
2. R3, R12	Bootstrap resistor sets drive current for output stage and allows pins 3 and 12 to go above V_S.
3. R_o	Works with C_o to stabilize output stage.
4. C1, C14	Input coupling capacitor. Pins 1 and 14 are at a DC potential of $V_S/2$. Low frequency pole set by: $$f_L = \frac{1}{2\pi R_{IN} C1}$$
5. C2, C13	Feedback capacitors. Ensure unity gain at DC. Also a low frequency pole at: $$f_L = \frac{1}{2\pi R2C2}$$
6. C3, C12	Bootstrap capacitors, used to increase drive to output stage. A low frequency pole is set by: $$f_L = \frac{1}{2\pi R3C3}$$
7. C5, C10	Compensation capacitor. These stabilize the amplifiers and adjust their bandwidth. See curve of bandwidth vs allowable gain.
8. C7	Improves power supply rejection (See Typical Performance Curves). Increasing C7 increases turn-on delay.
9. C_c	Output coupling capacitor. Isolates pins 5 and 10 from the load. Low frequency pole set by: $$f_L = \frac{1}{2\pi C_c R_L}$$
10. C_o	Works with R_o to stabilize output stage.
11. C_S	Provides power supply filtering.

Application Hints

AM Radios

The LM1896/LM2896 have been designed to fill a wide range of audio power applications. A common problem with IC audio power amplifiers has been poor signal-to-noise performance when used in AM radio applications. In a typical radio application, the loopstick antenna is in close proximity to the audio amplifier. Current flowing in the speaker and power supply leads can cause electromagnetic coupling to the loopstick, resulting in system oscillation. In addition, most audio power amplifiers are not optimized for lowest noise because of compensation requirements. If noise from the audio amplifier radiates into the AM section, the sensitivity and signal-to-noise ratio will be degraded.

The LM1896 exhibits extremely low wideband noise due in part to an external capacitor C5 which is used to tailor the bandwidth. The circuit shown in *Figure 2* is capable of a signal-to-noise ratio in excess of 60 dB referred to 50 mW. Capacitor C5 not only limits the closed loop bandwidth, it also provides overall loop compensation. Neglecting C2 in *Figure 2*, the gain is:

$$A_V(S) = \frac{S + A_V\omega_o}{S + \omega_o}$$

where $A_V = \dfrac{R2 + R5}{R2}$, $\quad \omega_o = \dfrac{1}{R5C5}$

A curve of -3 dB BW (ω_o) vs A_V is shown in the Typical Performance Curves.

Figure 3 shows a plot of recovered audio as a function of field strength in μV/M. The receiver section in this example is an LM3820. The power amplifier is located about two inches from the loopstick antenna. Speaker leads run parallel to the loopstick and are 1/8 inch from it. Referenced to a 20 dB S/N ratio, the improvement in noise performance over conventional designs is about 10 dB. This corresponds to an increase in usable sensitivity of about 8.5 dB.

Bridge Amplifiers

The LM1896/LM2896 can be used in the bridge mode as a monaural power amplifier. In addition to much higher power output, the bridge configuration does not require output coupling capacitors. The load is connected directly between the amplifier outputs as shown in *Figure 4*.

Amp 1 has a voltage gain set by 1 + R5/R2. The output of amp 1 drives amp 2 which is configured as an inverting amplifier with unity gain. Because of this phase inversion in amp 2, there is a 6 dB increase in voltage gain referenced to V_i. The voltage gain in bridge is:

$$\frac{V_o}{V_i} = 2\left(1 + \frac{R5}{R2}\right)$$

C_B is used to prevent DC voltage on the output of amp 1 from causing offset in amp 2. Low frequency response is influenced by:

$$f_L = \frac{1}{2\pi R_B C_B}$$

Several precautions should be observed when using the LM1896/LM2896 in bridge configuration. Because the amplifiers are driving the load out of phase, an 8Ω speaker will appear as a 4Ω load, and a 4Ω speaker will appear as a 2Ω load. Power dissipation is twice as severe in this situation. For example, if $V_S = 6V$ and $R_L = 8\Omega$ bridged, then the maximum dissipation is:

$$P_D = \frac{V_S^2}{20\,R_L} \times 2 = \frac{6^2}{20 \times 4} \times 2$$

$$P_D = 0.9 \text{ Watts}$$

This amount of dissipation is equivalent to driving two 4Ω loads in the stereo configuration.

When adjusting the frequency response in the bridge configuration, R5C5 and R10C10 form a 2 pole cascade and the -3 dB bandwidth is actually shifted to a lower frequency:

$$BW = \frac{0.707}{2\pi RC}$$

where R = feedback resistor

C = feedback capacitor

To measure the output voltage, a floating or differential meter should be used because a prolonged output short will over dissipate the package. *Figure 1* shows the complete bridge amplifier.

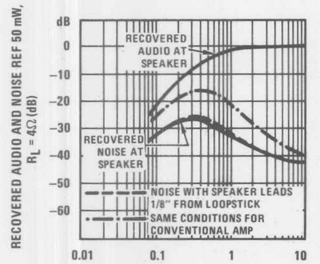


FIGURE 3. Improved AM Sensitivity Over Conventional Design

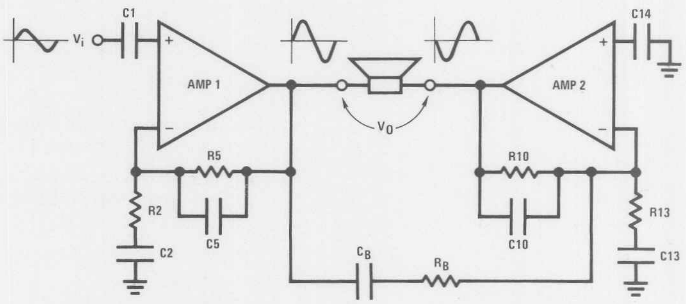


FIGURE 4. Bridge Amplifier Connection

Printed Circuit Layout

Printed Circuit Board Layout

Figure 5 and *Figure 6* show printed circuit board layouts for the LM1896 and LM2896. The circuits are wired as stereo amplifiers. The signal source ground should return to the input ground shown on the boards. Returning the loads to power supply ground through a separate wire will keep the THD at its lowest value. The inputs should be terminated in less than 50 kΩ to prevent an input-output oscillation. This oscillation is dependent on the gain and the proximity of the bridge elements R_B and C_B to the (+) input. If the bridge mode is not used, do not insert R_B, C_B into the PCB.

To wire the amplifier into the bridge configuration, short the capacitor on pin 7 (pin 1 of the LM1896) to ground. Connect together the nodes labeled BRIDGE and drive the capacitor connected to pin 5 (pin 14 of the LM1896).

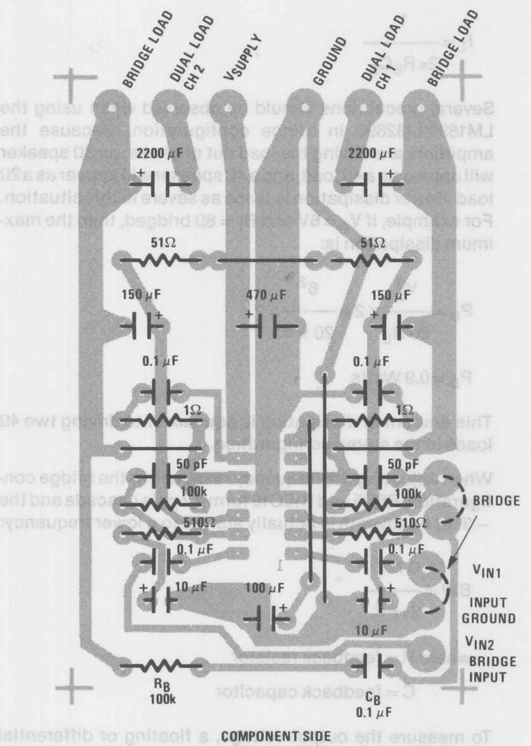


FIGURE 5. Printed Circuit Board Layout for the LM1896

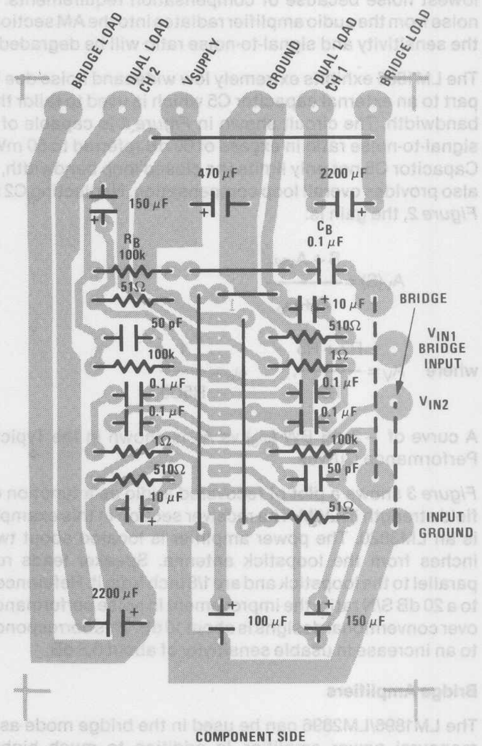


FIGURE 6. Printed Circuit Board Layout for the LM2896

National Semiconductor

LM1897 Low Noise Preamplifier for Tape Playback Systems

General Description

The LM1897 is a dual high gain preamplifier for applications requiring optimum noise performance. It is an ideal choice for a tape playback amplifier when a combination of low noise, high gain, good power supply rejection, and no power up transients are desired. The application also provides transient-free muting with a single pole grounding switch.

Features

- Programmable turn-on delay
- Transient-free power up — no pops
- Transient-free muting
- Low noise — 0.6μV CCIR/ARM in a DIN circuit referenced to gain at 1 kHz
- Low Voltage Battery Operation 4V
- Wide gain bandwidth due to broadband two amplifier approach 76 dB @ 20 kHz
- High power supply rejection 105 dB
- Low distortion 0.03%
- Fast slew rate 6V/μs
- Short circuit protection
- Internal diodes for diode switching applications
- Low cost external parts
- Excellent low frequency response
- Prevents "click" from being recorded onto the tape during power supply cycling in tape playback applications

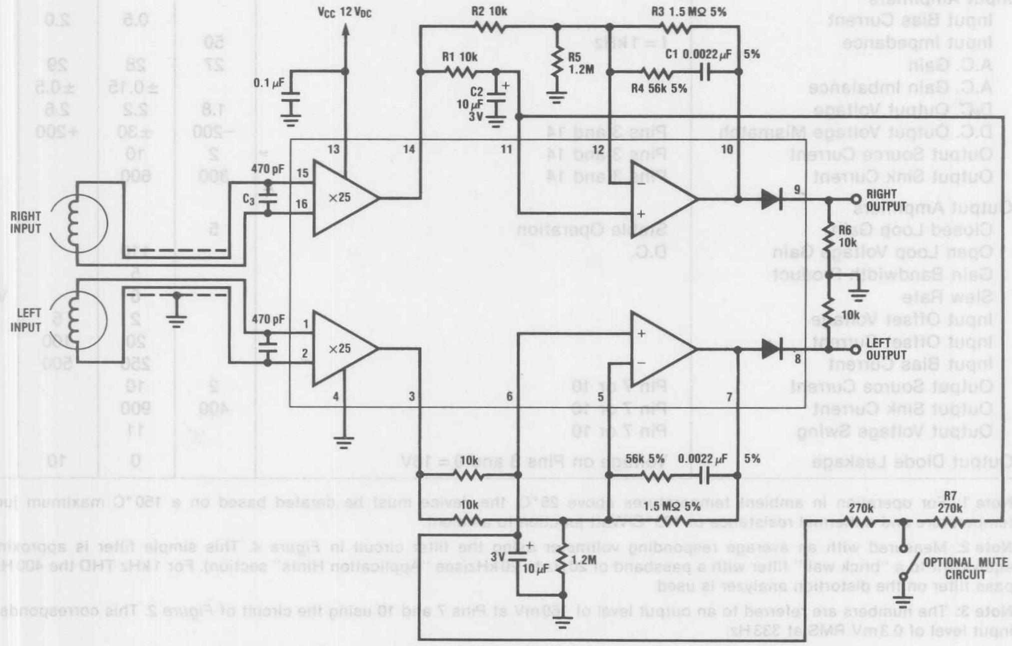


Figure 1. Typical Tape Playback Preamplifier Application

Order Number LM1897N
See NS Package N16E

Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Minimum Voltage On Any Pin	$-0.1\ V_{DC}$
Lead Temperature (soldering, 10 seconds)	300°C

Electrical Characteristics ($T_A = 25°C$, $V_{CC} = 12V$, See Test Circuit — *Figure 2)*

Parameter	Conditions	Min	Typ	Max	Units
Operating Supply Voltage Range	R_5 removed from circuit	4		18	V
Supply Current	$V_{CC} = 12V$		6	12	mA
Total Harmonic Distortion	f = 1 kHz, $V_{IN} = 0.3$ mV, Pins 7 & 10, *Figure 2*		0.03		%
THD + Noise (Note 2)	f = 1 kHz, $V_{OUT} = 1V$, Pins 7 & 10, *Figure 2*		0.10	0.25	%
Power Supply Rejection	Input Ref. f = 1 kHz, 1 V_{RMS}	85	105		dB
Channel Separation	f = 1 kHz, Output = 1 V_{RMS}, Output to Output	40	60		dB
Signal to Noise (Note 3)	Unweighted 32 Hz-12.74 kHz (Note 2)		58		dB
	CCIR/ARM (Note 4)		62		dB
	A Weighted		64		dB
	CCIR, Peak (Note 5)		52		dB
Noise	Output Voltage CCIR/ARM (Note 4)		120	200	μV
Input Amplifiers					
Input Bias Current			0.5	2.0	μA
Input Impedance	f = 1 kHz	50			kΩ
A.C. Gain		27	28	29	dB
A.C. Gain Imbalance			±0.15	±0.5	dB
D.C. Output Voltage		1.8	2.2	2.6	V
D.C. Output Voltage Mismatch	Pins 3 and 14	−200	±30	+200	mV
Output Source Current	Pins 3 and 14	2	10		mA
Output Sink Current	Pins 3 and 14	300	600		μA
Output Amplifiers					
Closed Loop Gain	Stable Operation	5			V/V
Open Loop Voltage Gain	D.C.		110		dB
Gain Bandwidth Product			5		MHz
Slew Rate			6		V/μsec
Input Offset Voltage			2	5	mV
Input Offset Current			20	100	nA
Input Bias Current			250	500	nA
Output Source Current	Pin 7 or 10	2	10		mA
Output Sink Current	Pin 7 or 10	400	900		μA
Output Voltage Swing	Pin 7 or 10		11		V_{PP}
Output Diode Leakage	Voltage on Pins 8 and 9 = 18V		0	10	μA

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 175°C/Watt junction to ambient.

Note 2: Measured with an average responding voltmeter using the filter circuit in *Figure 4*. This simple filter is approximately equivalent to a "brick wall" filter with a passband of 20 Hz to 20 kHz(see "Application Hints" section). For 1 kHz THD the 400 Hz high pass filter on the distortion analyzer is used.

Note 3: The numbers are referred to an output level of 160 mV at Pins 7 and 10 using the circuit of *Figure 2*. This corresponds to an input level of 0.3 mV RMS at 333 Hz.

Note 4: Measured with an average responding voltmeter using the Dolby lab's standard CCIR filter having a unity gain reference at 2 kHz.

Note 5: Measured using the Rhode-Schwarz psophometer, model UPGR.

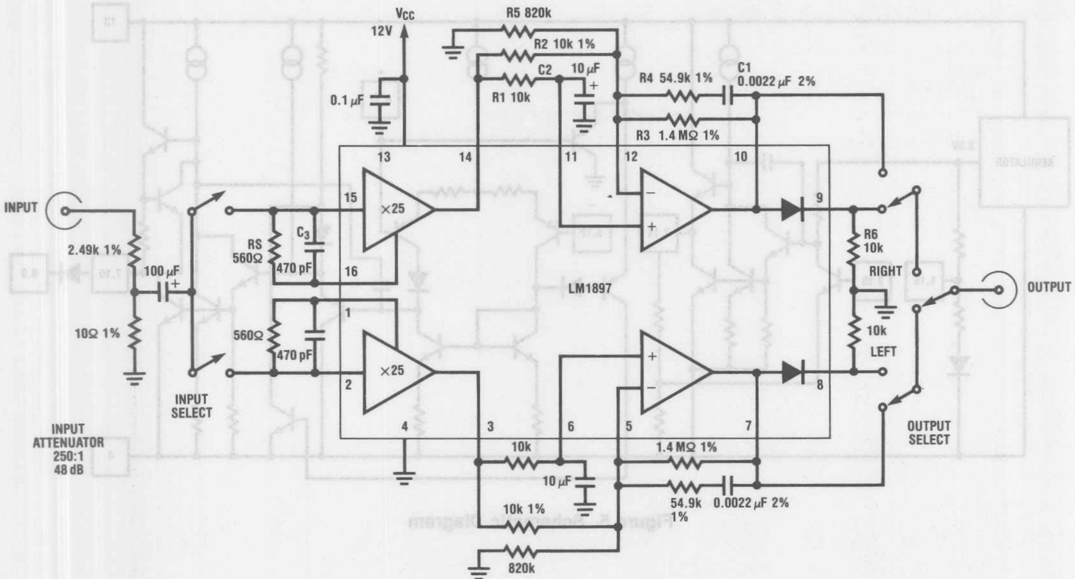


Figure 2. General Test Circuit

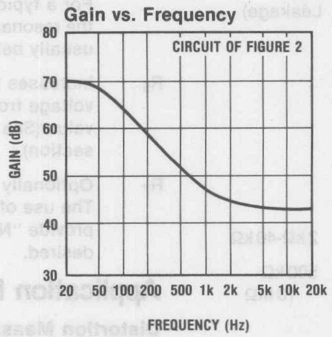


Figure 3. Frequency Response of Test Circuit

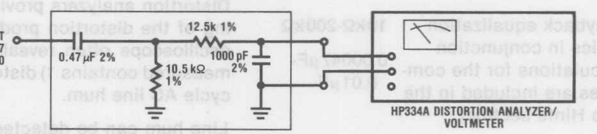


Figure 4. Simple 32-12740 Hz Filter and Meter

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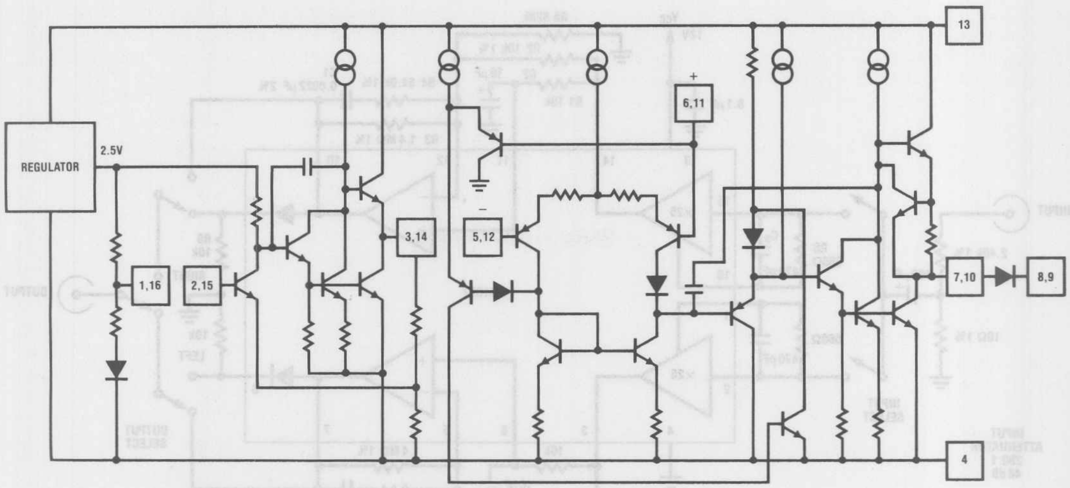


Figure 5. Schematic Diagram

External Component	Components (Refer to *Figure 1*) External Component Function	Normal Range of Value
R_1, C_2	Set turn-on delay and second amplifier's low frequency pole. Leakage current in C_2 results in DC offset between the amplifier's inputs and therefore this current should be kept low. R_1 is set equal to R_2 such that any input offset voltage due to bias current is effectively cancelled. An input offset voltage is generated by the input offset current multiplied by the value of these resistors.	2 kΩ-40 kΩ 0.1 μF-10 μF (Low Leakage)
R_2 R_3	Set the DC and low frequency gain of the output amplifier. The total input offset voltage will also be multiplied by the DC gain of this amplifier. It is therefore essential to keep the input offset voltage specification in mind when employing high DC gain in the output amplifier; i.e. 5 mV × 400 = 2V offset at the output.	2 kΩ-40 kΩ 500 kΩ-10 MΩ
R_4 C_1	Set tape playback equalization characteristics in conjunction with R_3 (calculations for the component values are included in the Applications Hints section).	10 kΩ-200 kΩ 0.00047 μF-0.01 μF
R_6	Biases the output diode when it is used in DC switching applications. This resistor can be excluded if diode switching is not desired.	2 kΩ-47 kΩ

External Component	Components (Refer to *Figure 1*) External Component Function	Normal Range of Value
C_3	Often used to resonate with tape head in order to compensate for tape playback losses including tape head gap and eddy current. For a typical cassette tape head, the resonant frequency selected is usually between 13 and 17 kHz.	100 pF-1000 pF
R_5	Increases the output DC bias voltage from the nominal 2.2V value (See the Application Hints section).	100 kΩ-10 MΩ
R_7	Optionally used for tape muting. The use of this resistor can also provide "No Pop" turn-off if desired.	

Application Hints

Distortion Measurement Method

In order to clearly interpret and compare specifications and measurements for low noise preamplifiers, it is necessary to understand several basic concepts of noise. An obvious example is the measurement of total harmonic distortion at very low input signal levels. Distortion analyzers provide outputs which allow viewing of the distortion products on an oscilloscope. The oscilloscope often reveals that the "distortion" being measured contains 1) distortion, 2) noise, and 3) 50 or 60 cycle AC line hum.

Line hum can be detected by using the "line sync" on the oscilloscope (horizontal sync selector). The triggering of a constant waveform indicates that AC line pickup is present. This is usually the result of electro-magnetic coupling into the preamplifier's input or improper test equipment grounding, which simply must be eliminated before making further measurements!

Input coupling problems can usually be corrected by any one of the following solutions: 1) shielding the source of the magnetic field (using mu metal or steel), 2) magnetically shielding the preamplifier, 3) physically moving the preamplifier far enough away from the magnetic field, or 4) using a high pass filter ($f_o = 200\,Hz$-$1\,kHz$) at the output of the preamplifier to prevent any line signal from entering the distortion analyzer. Ground loop problems can be solved by rearranging ground connections of the circuit and test equipment.

Separating noise from distortion products is necessary when it is desired to find the actual distortion and not the signal-to-noise ratio of an amplifier. The distortion produced by the LM1897 is predominately a second harmonic. It is for this reason that the third and higher order harmonics can be filtered without resulting in any appreciable error in the measurement. The filter also reduces the amount of noise in the measured data. Another more tedious technique for measuring THD is to use a wave analyzer. Each harmonic is measured and then summed in an RMS calculation. A typical curve is plotted for distortion vs. frequency using this method. A typical curve is also included using a 20 Hz to 20 kHz 4th order filter.

To specify the distortion of the LM1897 accurately and also not require unusual or tedious measurements the following method is used. The output level is set to one volt RMS at 1 kHz (approximately 5 millivolts at the input). The output is filtered with the circuit of *Figure 4* to limit the bandwidth of the noise and measured with a standard distortion analyzer. The analyzer has a filter that is switched in to remove line hum and ground loop pick-up as well as unrelated low frequency noise. The resulting measurement is fast and accurate.

Signal-To-Noise Ratio

In the measurement of the signal-to-noise ratio, misinterpretations of the numbers actually measured are common. One amplifier may sound much quieter than another, but due to improper testing techniques, they appear equal in measurements. This is often the case when comparing integrated circuit to discrete preamplifier designs. Discrete transistor preamps often "run out of gain" at high frequencies and therefore have small bandwidths to noise as indicated below.

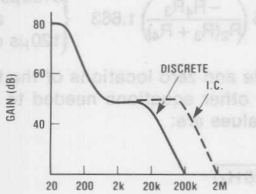


Figure 6.

Integrated circuits have additional open loop gain allowing additional feedback loop gain in order to lower harmonic distortion and improve frequency response. It is this additional bandwidth that can lead to erroneous signal to noise measurements if not considered during the measurement process. In the typical example above, the difference in bandwidth appears small on a log scale but the factor of 10 in bandwidth, (200 kHz to 2 MHz) can result in a 10 dB theoretical difference in the signal-to-noise ratio (white noise is proportional to the square root of the bandwidth in a system).

In comparing audio amplifiers it is necessary to measure the magnitude of noise in the audible bandwidth by using a "weighting" filter.[1] A "weighting" filter alters the frequency response in order to compensate for the average human ear's sensitivity to certain undesirable frequency spectra. The weighting filters at the same time provide the bandwidth limiting as discussed in the previous paragraph.

The 32 Hz to 12740 Hz filter shown in *Figure 4* is a simple two pole, one zero filter, approximately equivalent to a "brick wall" filter of 20 Hz to 20 kHz. This approximation is absolutely valid if the noise has a flat energy spectrum over the frequencies involved. In other words a measurement of a noise source with constant spectral density through either of the two filters would result in the same reading. The output frequency response of the two filters is shown in *Figure 7*.

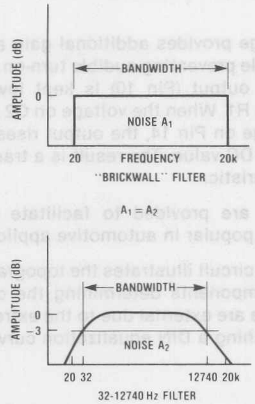


Figure 7.

Typical signal-to-noise figures are listed for several weighting filters which are commonly used in the measurement of noise. The shape of all weighting filters is similar, with the peak of the curve usually occuring in the 3-7 kHz region as shown below.

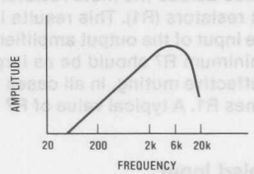


Figure 8.

In addition to noise filtering, differing meter types give different noise readings. Meter responses include: 1) RMS reading, 2) average responding, 3) peak reading, and 4) quasi peak reading. Although theoretical noise analysis is derived using true RMS (root mean square) based calculations, most actual measurement is taken with ARM (Average Responding Meter) test equipment.

The LM1897 IC incorporates a two stage broadband design which minimizes noise, attains overall DC stability and prevents audible transients during turn-on.

The first stage is a direct coupled amplifier with an internal gain of 25 V/V (28 dB). Direct coupling to the tape head reduces input source impedance and external component cost by removing the input coupling capacitor. A typical input coupling capacitor of $1\mu F$ has a reactance of $1.5 k\Omega$ at 100 Hz. The resulting noise due to the amplifier's input noise current can dominate the noise voltage at the output of the playback system. The input of the amplifier is biased from a reference voltage that is temperature compensated to produce a quiescent DC voltage of 2.2V at the output of the first stage. The input stage bias current that flows through the tape head is kept below $2\mu A$ in order to prevent any erasure of tape moving past the head. An added advantage of DC biasing is the prevention of large current transients during the charging of coupling capacitors at turn-on and turn-off.

The second stage provides additional gain and proper equalization while preventing audible turn-on transients or "pops". The output (Pin 10) is kept low until C2 charges through R1. When the voltage on C2 gets close to the DC voltage on Pin 14, the output rises exponentially to its final DC value. The result is a transient-free turn-on characteristic.

Internal diodes are provided to facilitate electronic diode switching popular in automotive applications.

The general test circuit illustrates the topography of the system. The components determining the overall frequency response are external due to the extreme sensitivity when matching a DIN equalization curve.

Mute Circuit

The LM1897 can be muted with the addition of two resistors and a grounding switch, as shown in *Figure 1*. When the circuit is not muted the additional resistors have no effect on the AC performance. They *do* have an effect on the DC Q point however.

The difference in the DC output voltages of the input amplifiers is applied across the mute resistors (R7) and the positive input resistors (R1). This results in an additional offset at the input of the output amplifiers. To keep this offset to a minimum R7 should be as large as possible to achieve effective muting. In all cases R7 should be at least ten times R1. A typical value of R7 is 25 to 50 times R1.

Capacitor-Coupled Input

The LM1897 is intended to be coupled directly to the signal source. Direct coupling permits faster turn-on and less low-frequency noise than would be possible with a capacitor-coupled input. However, there are some applications which require that the signal source be referred to ground and coupled to the input through a capacitor. *Figure 9* is an example of an LM1897 with a capacitor-coupled input. As shown, the circuit has a flat frequency response and is suitable for use as a microphone preamp. To eliminate turn-on pops, the inverting input of the second amplifier must be at a higher voltage than the non-inverting input when V_{CC} is applied. R_{10}, R_{11}, R_{12}, and D_1 ensure that this condition will be met. If later stages in the playback system employ turn-on muting circuitry, these extra components may not be needed. The value of R_{10} depends on V_{CC} as defined by the following relationship:

$$R_{10} = (V_{CC} - 1) \times 1k$$

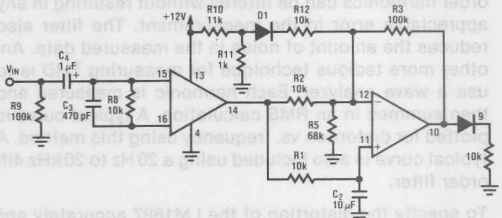


Figure 9. Microphone Preamplifier with Capacitor Coupled Input

Design Equations

The overall gain of the circuit is given by:

$$A_V = 25 \left[\frac{-R_4R_3}{R_2(R_3 + R_4)}\right] \frac{\left(s + \frac{1}{R_4C_1}\right)}{\left(s + \frac{1}{(R_3 + R_4)C_1}\right)} \quad (1)$$

Standard cassette tapes require equalization of $3180\mu sec$ (50 Hz) and $120\mu sec$ (1.3 kHz). These time constants result in an AC gain at 1 kHz given by:

$$A_V(1\,kHz) = 25 \left(\frac{-R_4R_3}{R_2(R_3 + R_4)}\right) 1.663 \quad \left\{\begin{matrix} 3180\mu s \text{ or } 50\,Hz \\ \text{and} \\ 120\mu s \text{ or } 1326\,Hz \end{matrix}\right\} \quad (2)$$

Using the pole and zero locations of the transfer function, the two other equations needed to solve for the component values are:

$$R_4 = \frac{1}{2\pi C_1(1326\,Hz)} \quad (3)$$

$$R_3 = \frac{1}{2\pi C_1(50\,Hz)} - \frac{1}{2\pi C_1(1326\,Hz)} = \frac{1}{2\pi C_1(51.96)} \quad (4)$$

We can now solve for C_1 as a function of R_2, or:

$$A_V(1\,kHz) = -25 \left(\frac{\left[\frac{1}{2\pi C_1(1326)}\right]\left[\frac{1}{2\pi C_1(51.96)}\right]}{\left[R_2 \frac{1}{2\pi C_1(50)}\right]}\right)(1.663) \quad (5)$$

$$C_1 = \frac{-4.80 \times 10^{-3}}{R_2[A_V(1\,kHz)]} \quad (6)$$

When chromium dioxide tape is used, the defined time constants are 3180 μsec and 70 μsec. This changes equation (3) to:

$$R_4 = \frac{1}{2\pi C_1 (2274\,\text{Hz})} \tag{7}$$

The value of R_3 is normally not changed. This results in an error of less than 0.2 dB in the low frequency response.

The output voltage of the LM1897 is set by the input amplifier DC voltage at pin 3 or 14, and by R_3 and R_5.

$$\text{Nominal } V_{OUT} \text{ (pin 7 or 10)} = 2.2\left(1 + \frac{R_3}{R_5}\right) \tag{8}$$

Pins 8 and 9 are biased 0.7 volts less than V_{OUT} (pin 7 or 10). When these diodes are used the output (pin 7 or 10) should be biased at one half the minimum operating supply voltage. Equation (8) can be rewritten to solve for R_5.

$$R_5 = \frac{2.2\,R_3}{V_O - 2.2} \tag{9}$$

The output voltage of the LM1897 will vary from that given in equation (8) due to variations in the input amplifier DC voltage as well as the output amplifier input bias current, input offset current and input offset voltage. The following equation gives the worst case variation in the output voltage.

$$\Delta V_{OUT} = \pm\left[\Delta V_{PIN3}\left(1 + \frac{R_3}{R_5}\right) + \frac{R_3}{R_2}\left(\Delta I_{BIAS}(R_1 - R_2) + \frac{I_{OS}}{2}(R_1 + R_2) + V_{OS}\right)\right] \tag{10}$$

Using the worst case values in the electrical characteristics reduces this to

$$\Delta V_{OUT} = \pm\left[0.4\left(1 + \frac{R_3}{R_5}\right) + \frac{R_3}{R_2}\left(200\,\text{nA}\,(R_1 - R_2) + 50\,\text{nA}\,(R_1 + R_2) + 5\,\text{mV}\right)\right] \tag{11}$$

The turn-on delay is set by R_1 and C_2; delay can be approximated by:

$$\text{Delay Time } t = R_1 C_2 \ln\left(\frac{2.2}{V_{ODC}}\right)\left(\frac{R_3}{R_2}\right) \tag{12}$$

Example

If we desire a tape preamp with 100 mV output signal from a tape head with a nominal output of 0.5 mV at 1 kHz for standard ferric cassette tape, the external components are determined as follows. The value of R_2 is arbitrarily set to 10 kΩ.

$$R_1 = R_2 = 10\text{k}$$

This minimizes errors due to the output amplifier bias currents.

$$C_1 = \frac{-4.80 \times 10^{-3}}{10\,\text{k}\Omega\left[\dfrac{-100\,\text{mV}}{0.5\,\text{mV}}\right]} = 2400\,\text{pF} \rightarrow 0.0022\,\mu\text{F}$$

Use 0.0022 μF and determine:

$$R_4 = \frac{1}{2\pi C_1 (1326)} = 54.6\,\text{k}\Omega \rightarrow 54.9\,\text{k}\Omega\ 1\%$$

$$R_3 = \frac{1}{2\pi C_1 (51.96)} = 1.39\,\text{M}\Omega \rightarrow 1.4\,\text{M}\Omega\ 1\%$$

To bias the output amplifier output voltage at 6 volts (half supply):

$$R_5 = \frac{2.2\,(1.4\,\text{M}\Omega)}{6 - 2.2} = 811\,\text{k}\Omega \rightarrow 820\,\text{k}\Omega$$

The maximum variation in the output voltage is found using equation (11):

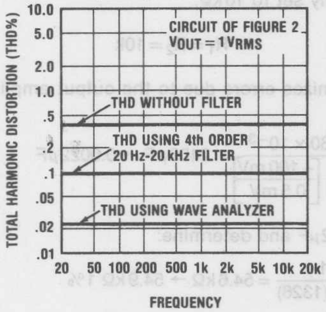
$$\Delta V_{OUT} = \pm 1.9 \text{ volts}$$

The low frequency response and turn-on delay determine the value of C_2. For $R_1 = 10\text{k}$ and $C_2 = 10\,\mu\text{F}$ the low frequency 3 dB point is 1.6 Hz and the turn-on delay is 0.4 seconds, from equation (12).

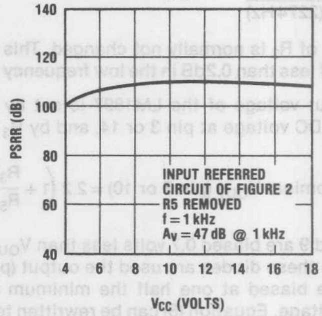
The complete circuit is shown in Figure 2. A circuit with 5% components and biased for a minimum supply of 10 volts is shown in Figure 1. If additional gain is needed R_1 and R_2 can be reduced without changing the frequency response of the circuit.

Reference 1: CCIR/ARM: *A Practical Noise Measurement Method*; by Ray Dolby, David Robinson and Kenneth Gundry, AES Preprint No. 1353 (F-3).

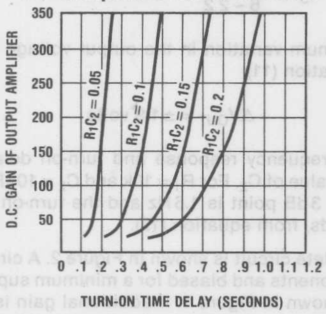
Total Harmonic Distortion vs. Frequency



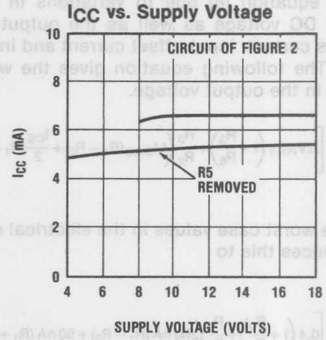
PSRR vs. V_{CC}



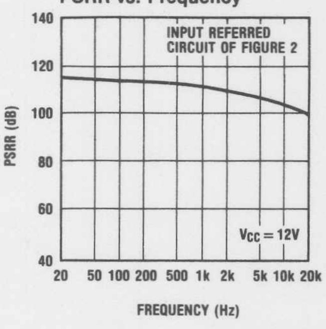
Turn On Delay vs. Component Values and Gain



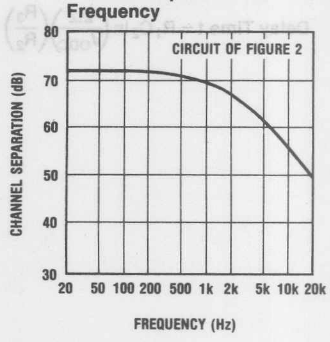
I_{CC} vs. Supply Voltage



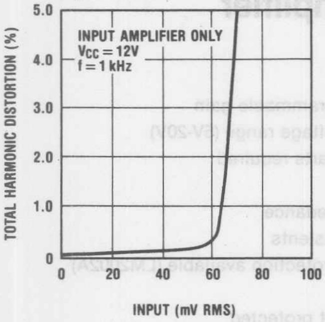
PSRR vs. Frequency



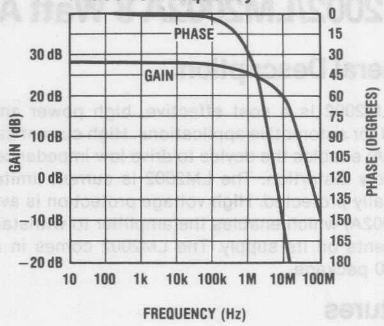
Channel Separation vs. Frequency



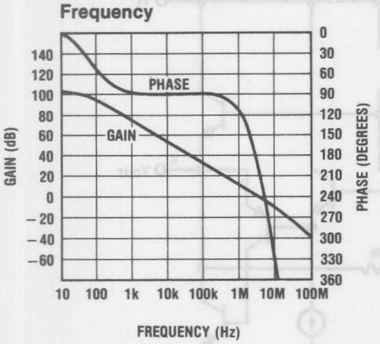
Input Amplifier THD vs. Input Level



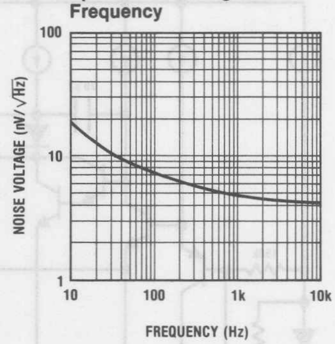
Input Amplifier Gain and Phase vs. Frequency



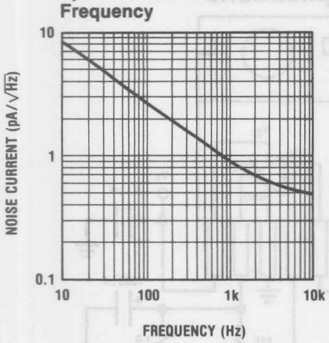
Output Amplifier Open Loop Gain and Phase vs. Frequency



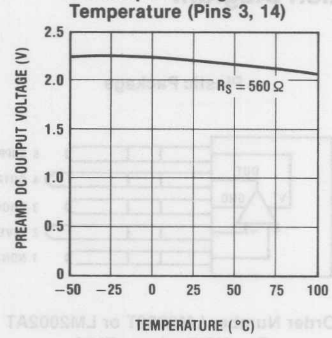
Spot Noise Voltage vs. Frequency



Spot Noise Current vs. Frequency



Input Amplifier DC Output Voltage vs. Temperature (Pins 3, 14)



Semiconductor

LM2002/LM2002A 8 Watt Audio Power Amplifier

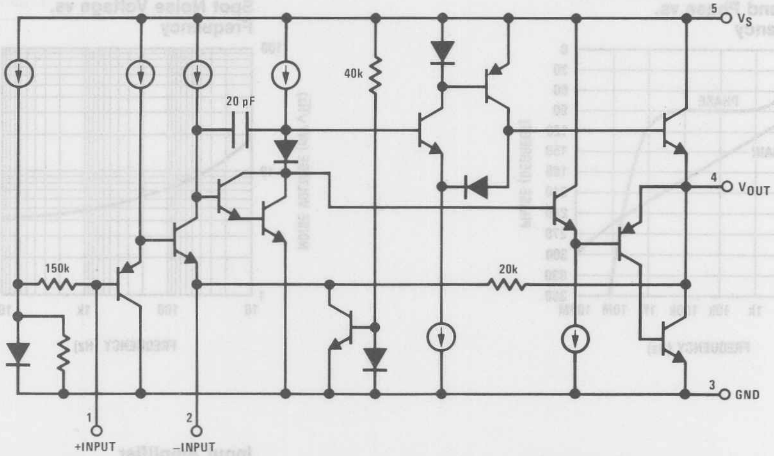
General Description

The LM2002 is a cost effective, high power amplifier suited for automotive applications. High current capability (3.5A) enables the device to drive low impedance loads with low distortion. The LM2002 is current limited and thermally protected. High voltage protection is available (LM2002A) which enables the amplifier to withstand 40V transients on its supply. The LM2002 comes in a 5-pin TO-220 package.

Features

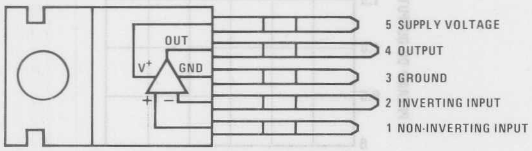
- High peak current capability (3.5A)
- Large output voltage swing
- Externally programmable gain
- Wide supply voltage range (5V-20V)
- Few external parts required
- Low distortion
- High input impedance
- No turn-on transients
- High voltage protection available (LM2002A)
- Low noise
- AC short circuit protected
- Pin for pin compatible with TDA2002

Equivalent Schematic



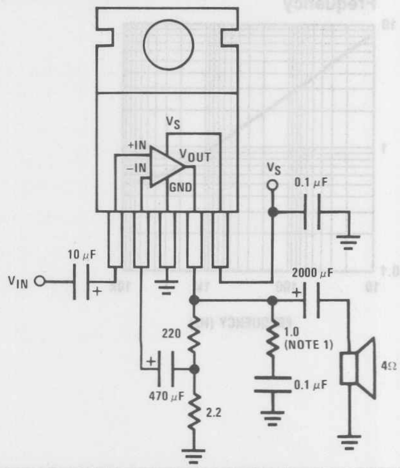
Connection Diagram

Plastic Package



Order Number LM2002T or LM2002AT
See NS Package T05A

Typical Applications



Absolute Maximum Ratings

Peak Supply Voltage (50 ms)	
LM2002A (Note 2)	40V
LM2002	25V
Operating Supply Voltage	20V
Output Current	
Repetitive	3.5A
Non-repetitive	4.5A
Input Voltage	± 0.5V
Power Dissipation (Note 3)	15W
Operating Temperature	0°C to + 70°C
Storage Temperature	− 60°C to + 150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics $V_S = 14.4V$, $T_{TAB} = 25°C$, $A_V = 100$ (40 dB), $R_L = 4\Omega$, unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
DC Output Level		6.4	7.2	8	V
Quiescent Supply Current	Excludes Current in Feedback Resistors		45	80	mA
Supply Voltage Range		5		20	V
Input Resistance			150		kΩ
Bandwidth	Gain = 40 dB		100		kHz
Output Power	$V_S = 13.2V$, f = 1 kHz				
	$R_L = 4\Omega$, THD = 10%		4.3		W
	$R_L = 2\Omega$, THD = 10%		6.5		W
	$V_S = 13.8V$, f = 1 kHz				
	$R_L = 4\Omega$, THD = 10%		4.8		W
	$R_L = 2\Omega$, THD = 10%		7.4		W
	$V_S = 14.4V$, f = 1 kHz				
	$R_L = 4\Omega$, THD = 10%	4.8	5.2		W
	$R_L = 2\Omega$, THD = 10%	7	8		W
	$R_L = 1.6\Omega$, THD = 10%		9		W
	$V_S = 16V$, f = 1 kHz				
	$R_L = 4\Omega$, THD = 10%		6.5		W
	$R_L = 2\Omega$, THD = 10%		10		W
	$R_L = 1.6\Omega$, THD = 10%		10.5		W
THD	$P_o = 2W$, $R_L = 4\Omega$, f = 1 kHz		0.1		%
	$P_o = 4W$, $R_L = 2\Omega$, f = 1 kHz		0.1		%
Ripple Rejection	$R_S = 50\Omega$, f = 100 Hz	30	40		dB
	$R_S = 50\Omega$, f = 1 kHz		44		dB
Input Noise Voltage	$R_S = 0$, 15 kHz Bandwidth		2		μV
Input Noise Current	$R_S = 100$ kΩ, 15 kHz Bandwidth		40		pA

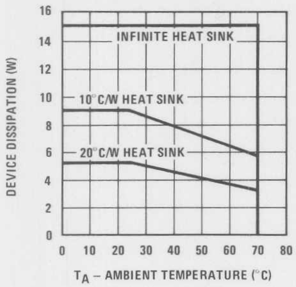
Note 1: A 1.0 resistor and 0.1 μF capacitor should be placed as close as possible to pins 3 and 4 for stability.

Note 2: The LM2002 shuts down above 25V.

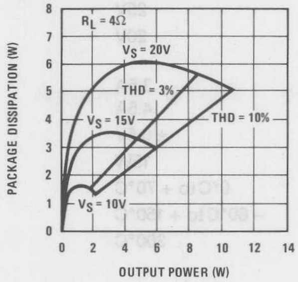
Note 3: For operating at elevated temperatures, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 4°C/W junction to case.

Typical Performance Characteristics

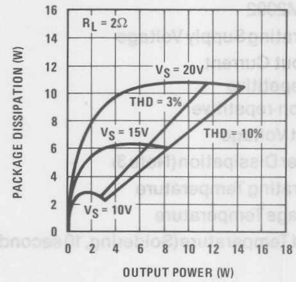
Device Dissipation vs Ambient Temperature



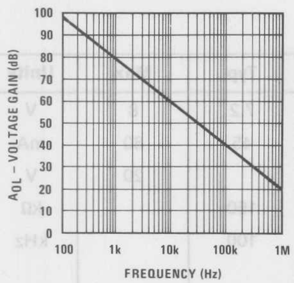
Power Dissipation vs Output Power



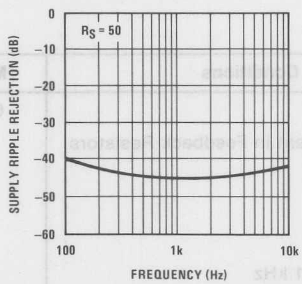
Power Dissipation vs Output Power



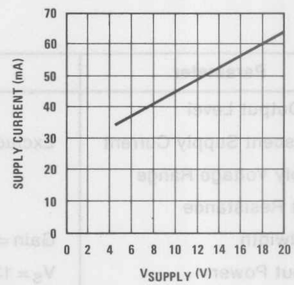
Open Loop Gain vs Frequency



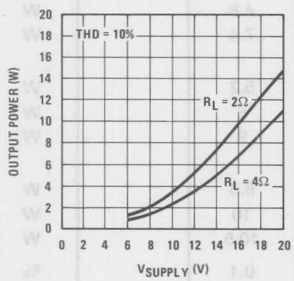
Supply Ripple Rejection vs Frequency



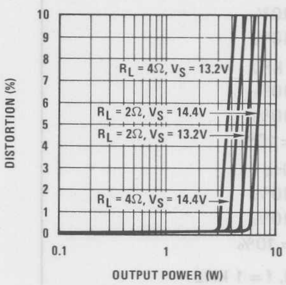
Supply Current vs Supply Voltage



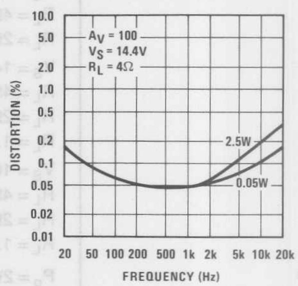
Output Power vs Supply Voltage



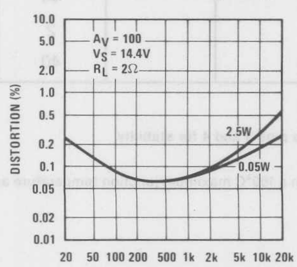
Distortion vs Output Power



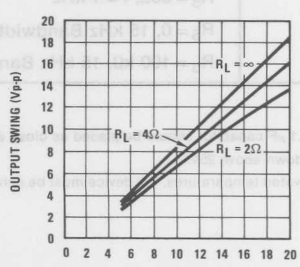
Distortion vs Frequency



Distortion vs Frequency

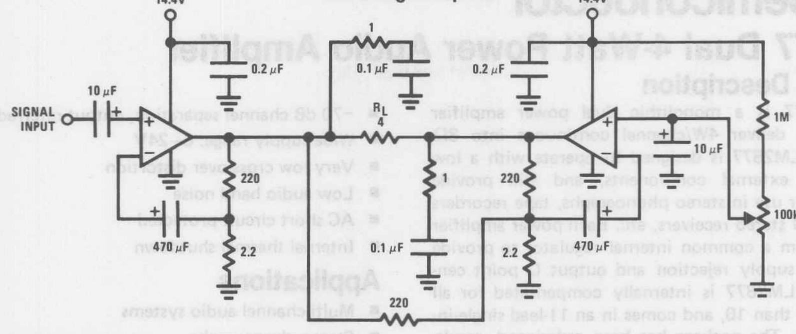


Output Swing vs Supply Voltage

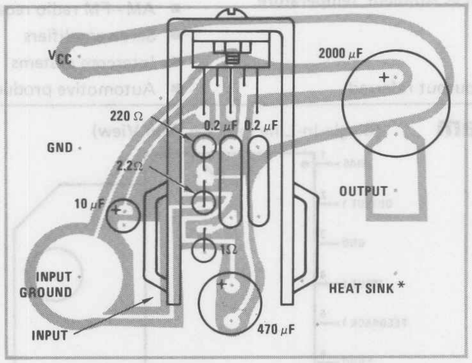


Typical Applications (Continued)

16W Bridge Amplifier



Component Layout



* Staver V-5

General Description

The LM2877 is a monolithic dual power amplifier designed to deliver 4W/channel continuous into 8Ω loads. The LM2877 is designed to operate with a low number of external components, and still provide flexibility for use in stereo phonographs, tape recorders and AM–FM stereo receivers, etc. Each power amplifier is biased from a common internal regulator to provide high power supply rejection and output Q point centering. The LM2877 is internally compensated for all gains greater than 10, and comes in an 11-lead single-in-line package. The package has been redesigned, resulting in a slightly degraded thermal characteristic shown in the figure Device Dissipation vs Ambient Temperature.

Features

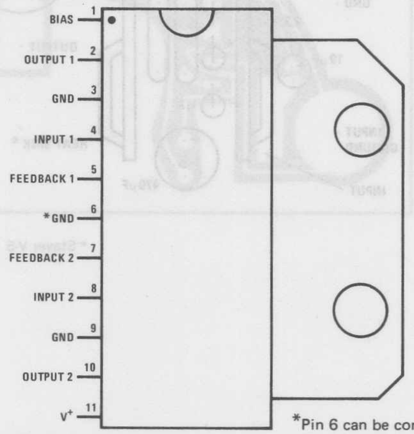
- 4W/channel
- −68 dB ripple rejection, output referred
- −70 dB channel separation, output referred
- Wide supply range, 6–24V
- Very low cross-over distortion
- Low audio band noise
- AC short circuit protected
- Internal thermal shutdown

Applications

- Multi-channel audio systems
- Stereo phonographs
- Tape recorders and players
- AM–FM radio receivers
- Servo amplifiers
- Intercom systems
- Automotive products

Connection Diagram

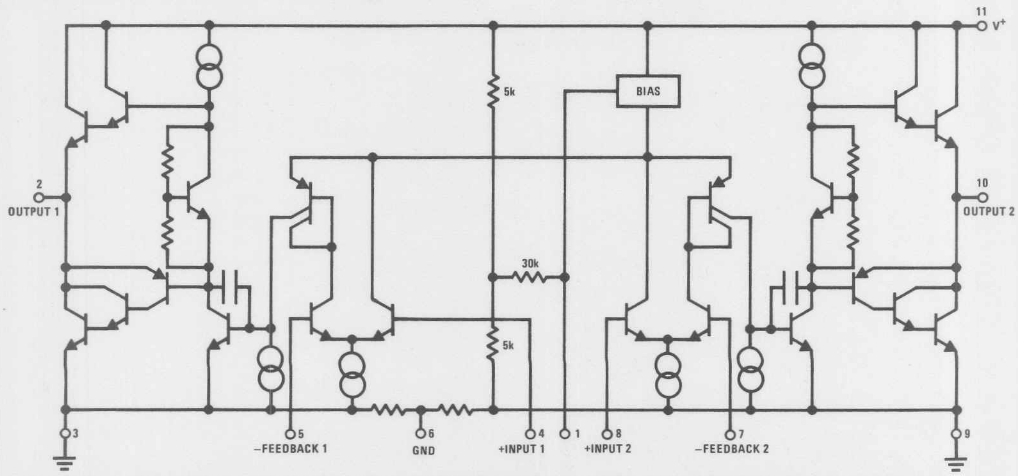
(Single-In-Line Package, Top View)



*Pin 6 can be connected to pin 3 or pin 9, if not, pin 6 must be left with NO connection.

Order Number LM2877P
See NS Package P11A

Equivalent Schematic Diagram



Absolute Maximum Ratings

Supply Voltage	26V
Input Voltage	±0.7V
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

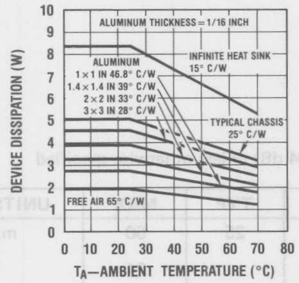
$V_S = 20V$, $T_{TAB} = 25°C$, $R_L = 8\Omega$, $A_V = 50$ (34 dB) unless otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Total Supply Current	$P_O = 0W$		25	50	mA
Operating Supply Voltage		6		24	V
Output Power/Channel	f = 1 kHz, THD = 10%, $T_{TAB} = 25°C$				
	$V_S = 20V$	4.0	4.5		W
	$V_S = 18V$		3.6		W
	$V_S = 12V$, $R_L = 4\,\Omega$	1.5	1.9		W
Distortion, THD	f = 1 kHz, $V_S = 20V$				
	$P_O = 50$ mW/Channel		0.1		%
	$P_O = 1W$/Channel		0.07		%
	$P_O = 2W$/Channel		0.07	1	%
	f = 1 kHz, $V_S = 12V$, $R_L = 4\,\Omega$				
	$P_O = 50$ mW/Channel		0.25		%
	$P_O = 500$ mW/Channel		0.20		%
	$P_O = 1W$/Channel		0.15	1	%
Output Swing	$R_L = 8\,\Omega$		V_S-4		Vp-p
Channel Separation	$C_F = 50\,\mu F$, $C_{IN} = 0.1\,\mu F$, f = 1 kHz, Output Referred				
	$V_S = 20V$, $V_O = 4$ Vrms	−50	−70		dB
	$V_S = 7V$, $V_O = 0.5$ Vrms		−60		dB
PSRR Power Supply Rejection Ratio	$C_F = 50\,\mu F$, $C_{IN} = 0.1\,\mu F$, f = 120 Hz, Output Referred				
	$V_S = 20V$, $V_{RIPPLE} = 1$ Vrms	−50	−68		dB
	$V_S = 7V$, $V_{RIPPLE} = 0.5$ Vrms		−40		dB
Noise	Equivalent Input Noise				
	$R_S = 0$, $C_{IN} = 0.1\,\mu F$, BW = 20 Hz–20 kHz		2.5		μV
	Output Noise Wideband				
	$R_S = 0$, $C_{IN} = 0.1\,\mu F$, $A_V = 200$		0.80		mV
Open Loop Gain	$R_S = 0$, f = 1 kHz, $R_L = 8\,\Omega$		70		dB
Input Offset Voltage			15		mV
Input Bias Current			50		nA
Input Impedance	Open Loop		4		MΩ
DC Output Level	$V_S = 20V$	9	10	11	V
Slew Rate			2.0		V/μs
Power Bandwidth			65		kHz
Current Limit			1.0		A

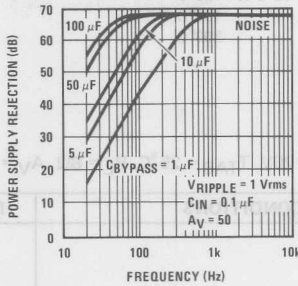
Note 1: For operation at ambient temperature greater than 25°C, the LM2877 must be derated based on a maximum 150°C junction temperature using a thermal resistance which depends upon device mounting techniques.

Typical Performance Characteristics

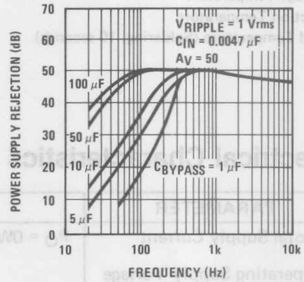
Device Dissipation vs Ambient Temperature



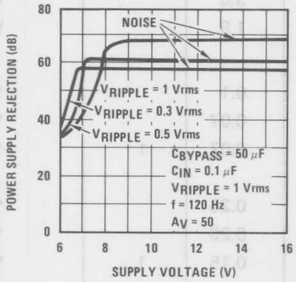
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



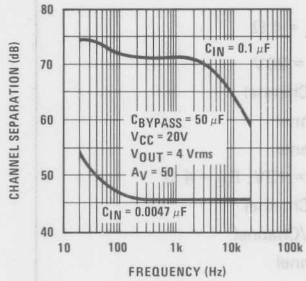
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



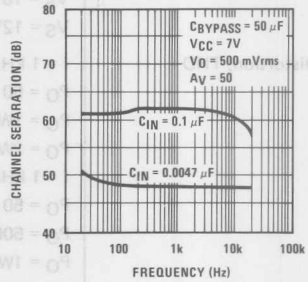
Power Supply Rejection Ratio (Referred to the Output) vs Supply Voltage



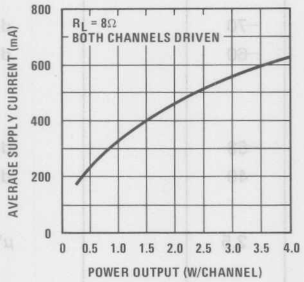
Channel Separation (Referred to the Output) vs Frequency



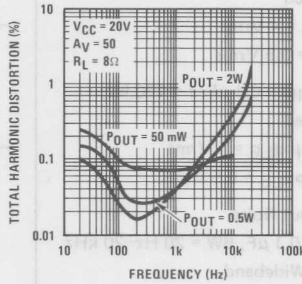
Channel Separation (Referred to the Output) vs Frequency



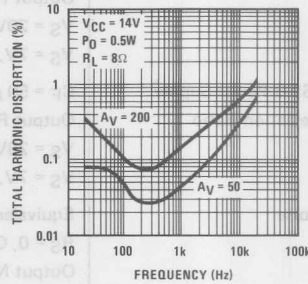
Average Supply Current vs Power Output



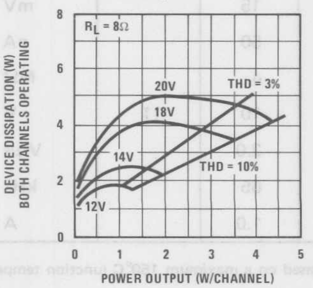
Total Harmonic Distortion vs Frequency



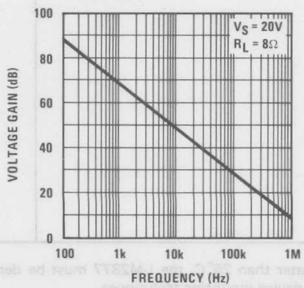
Total Harmonic Distortion vs Frequency



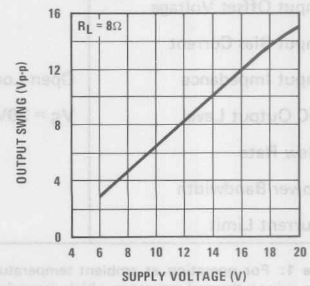
Power Dissipation vs Power Output



Open Loop Gain vs Frequency

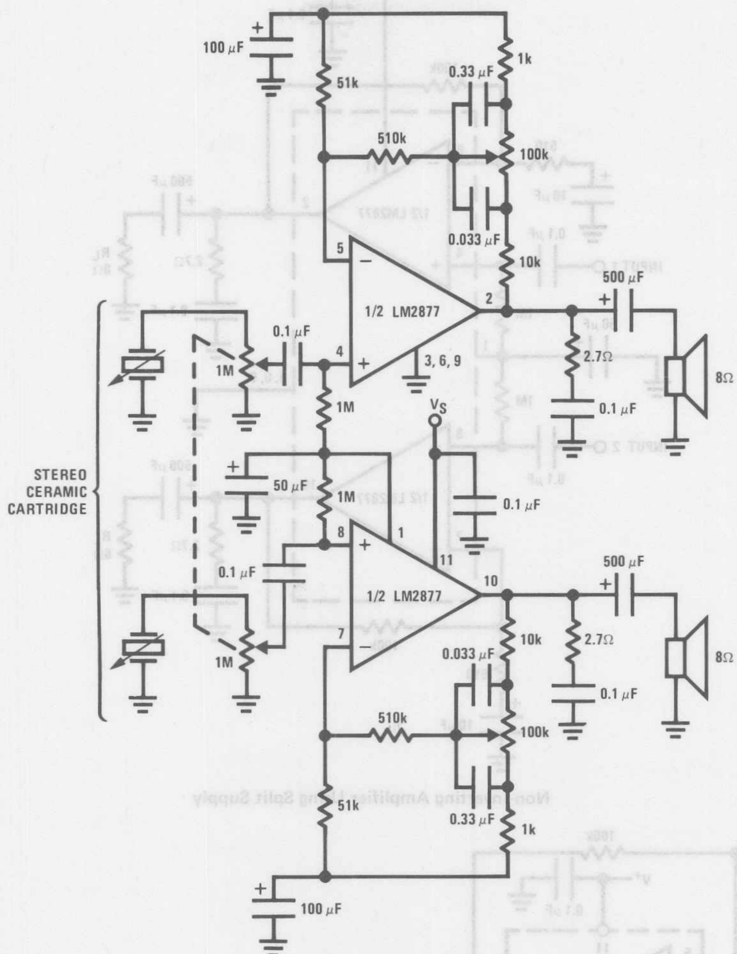


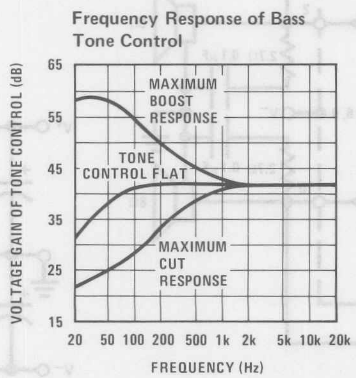
Output Swing vs Supply Voltage

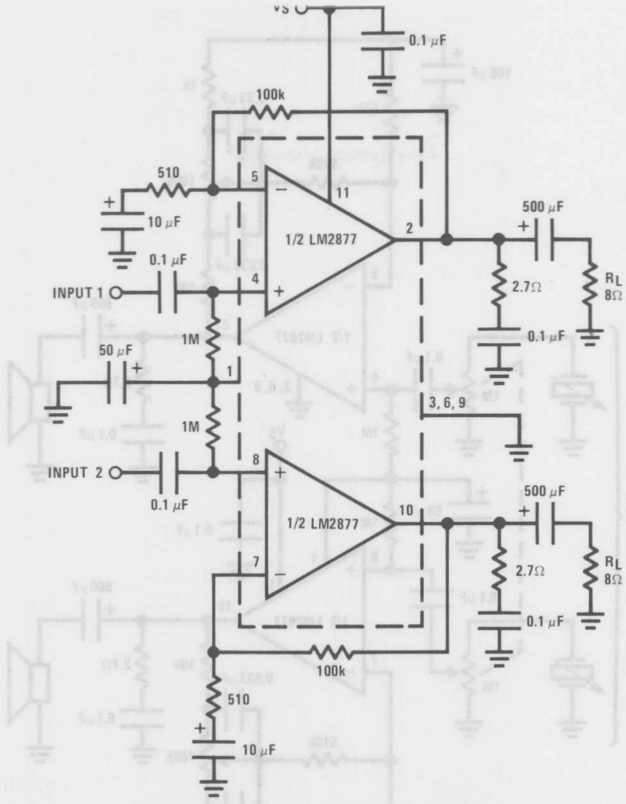


Typical Applications

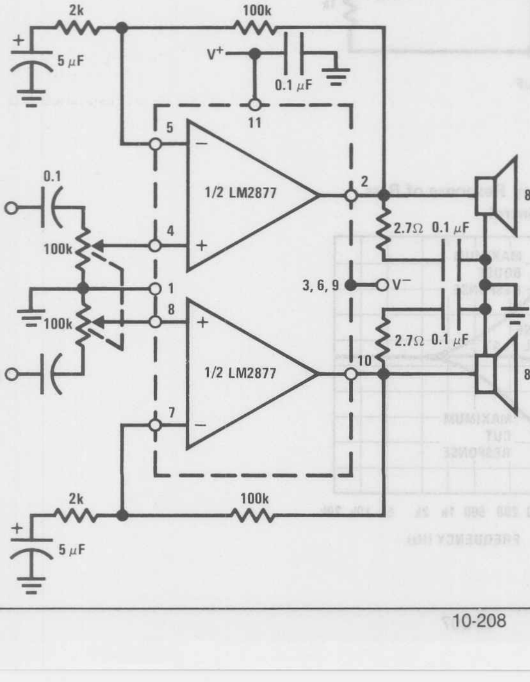
Stereo Phonograph Amplifier with Bass Tone Control

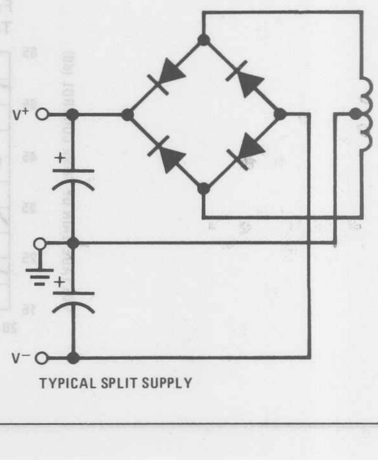






Non-Inverting Amplifier Using Split Supply

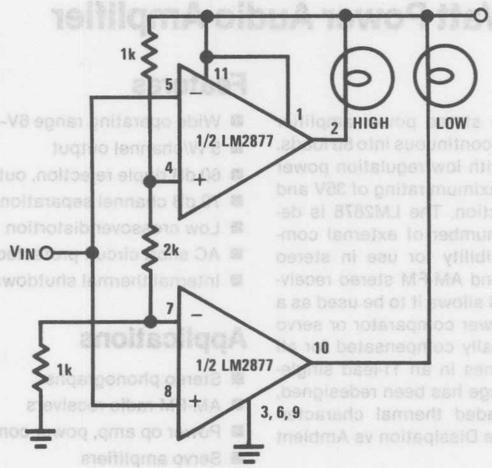




TYPICAL SPLIT SUPPLY

Typical Applications (Continued)

Window Comparator Driving High, Low Lamps



TRUTH TABLE

V_{IN}	High	Low
$< 1/4\ V^+$	Off	On
$1/4\ V^+$ to $3/4\ V^+$	Off	Off
$> 3/4\ V^+$	On	Off

Application Hints

The LM2877 is an improved LM377 in typical audio applications. In the LM2877, the internal voltage regulator for the input stage is generated from the voltage on pin 1. Normally the inputs cannot common-mode more than 0.7V above this pin 1 voltage. Nevertheless the common-mode range can be increased by externally forcing the voltage on pin 1. One way to do this is to short pin 1 to the positive supply, pin 11.

The only special care required with the LM2877 is to limit the maximum input differential voltage to ±7V. If this differential voltage is exceeded, the input characteristics may alter.

Figure 1 shows a power op amp application with $A_V = 1$. The 100k and 10k resistors set a noise gain of 10 and are dictated by amplifier stability. The 10k resistor is bootstrapped by the feedback so the input resistance is dominated by the 1 MΩ resistor.

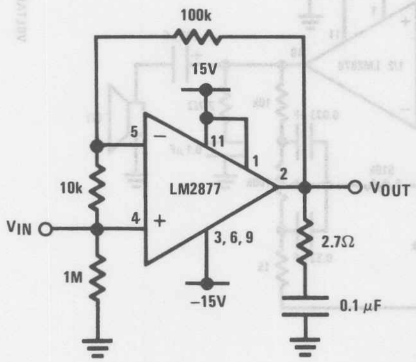


FIGURE 1

National Semiconductor

LM2878 Dual 5 Watt Power Audio Amplifier

General Description

The LM2878 is a high voltage stereo power amplifier designed to deliver 5 W/channel continuous into 8Ω loads. The amplifier is ideal for use with low regulation power supplies due to the absolute maximum rating of 35V and its superior power supply rejection. The LM2878 is designed to operate with a low number of external components, and still provide flexibility for use in stereo phonographs, tape recorders, and AM-FM stereo receivers. The flexibility of the LM2878 allows it to be used as a power operational amplifier, power comparator or servo amplifier. The LM2878 is internally compensated for all gains greater than 10, and comes in an 11-lead single-in-line package (SIP). The package has been redesigned, resulting in the slightly degraded thermal characteristics shown in the figure Device Dissipation vs Ambient Temperature.

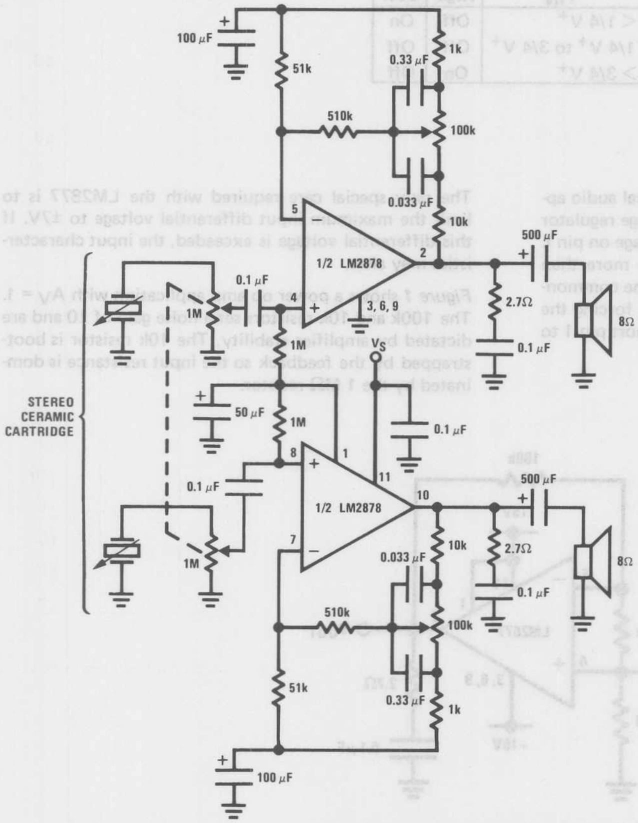
Features

- Wide operating range 6V–32V
- 5 W/channel output
- 60 dB ripple rejection, output referred
- 70 dB channel separation, output referred
- Low crossover distortion
- AC short circuit protected
- Internal thermal shutdown

Applications

- Stereo phonographs
- AM-FM radio receivers
- Power op amp, power comparator
- Servo amplifiers

Typical Applications



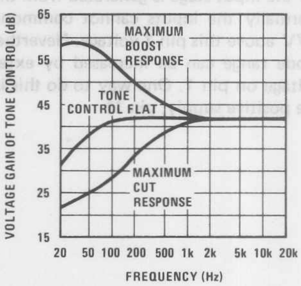


FIGURE 1. Stereo Phonograph Amplifier with Bass Tone Control

Absolute Maximum Ratings

Supply Voltage	35V
Input Voltage (Note 1)	± 0.7V
Operating Temperature (Note 2)	0°C to 70°C
Storage Temperature	− 65°C to 150°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 seconds)	300°C

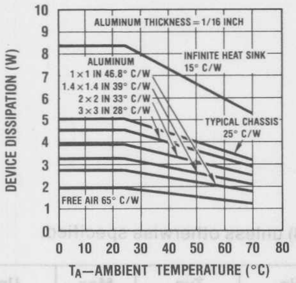
Electrical Characteristics $V_S = 22V$, $T_{TAB} = 25°C$, $R_L = 8\Omega$, $A_V = 50$ (34 dB) unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Total Supply Current	$P_O = 0W$		10	50	mA
Operating Supply Voltage		6		32	V
Output Power/Channel	f = 1 kHz, THD = 10%, $T_{TAB} = 25°C$	5	5.5		W
Distortion	f = 1 kHz, $R_L = 8\Omega$				
	$P_O = 50$ mW		0.20		%
	$P_O = 0.5W$		0.15		%
	$P_O = 2W$		0.14		%
Output Swing	$R_L = 8\Omega$		$V_S - 6V$		Vp-p
Channel Separation	$C_{BYPASS} = 50\ \mu F$, $C_{IN} = 0.1\ \mu F$ f = 1 kHz, Output Referred $V_O = 4$ Vrms	− 50	− 70		dB
PSRR Power Supply Rejection Ratio	$C_{BYPASS} = 50\ \mu F$, $C_{IN} = 0.1\ \mu F$ f = 120 Hz, Output Referred $V_{ripple} = 1$ Vrms	− 50	− 60		dB
PSRR Negative Supply	Measured at DC, Input Referred		− 60		dB
Common-Mode Range	Split Supplies ± 15V, Pin 1 Tied to Pin 11		± 13.5		V
Input Offset Voltage			10		mV
Noise	Equivalent Input Noise $R_S = 0$, $C_{IN} = 0.1\ \mu F$				
	BW = 20 − 20 kHz		2.5		μV
	CCIR·ARM		3.0		μV
	Output Noise Wideband $R_S = 0$, $C_{IN} = 0.1\ \mu F$, $A_V = 200$		0.8		mV
Open Loop Gain	$R_S = 51\Omega$, f = 1 kHz, $R_L = 8\Omega$		70		dB
Input Bias Current			100		nA
Input Impedance	Open Loop		4		MΩ
DC Output Voltage	$V_S = 22V$	10	11	12	V
Slew Rate			2		V/μs
Power Bandwidth	3 dB Bandwidth at 2.5W		65		kHz
Current Limit			1.5		A

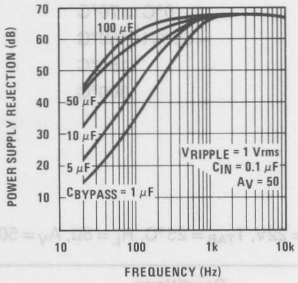
Note 1: ± 0.7V applies to audio applications; for extended range, see Application Hints.

Note 2: For operation at ambient temperature greater than 25°C, the LM2878 must be derated based on a maximum 150°C junction temperature using a thermal resistance which depends upon device mounting techniques.

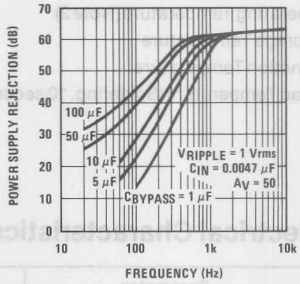
Device Dissipation vs Ambient Temperature



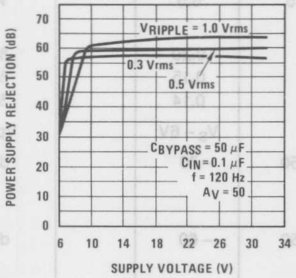
Ratio (Referred to the Output) vs Frequency



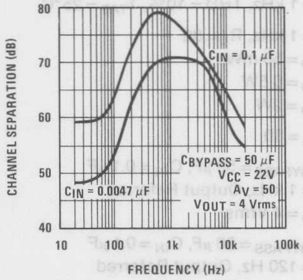
Ratio (Referred to the Output) vs Frequency



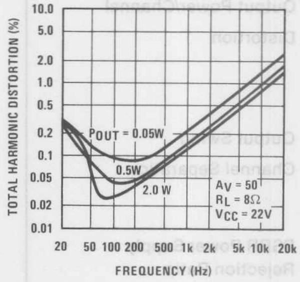
Power Supply Rejection Ratio (Referred to the Output) vs Supply Voltage



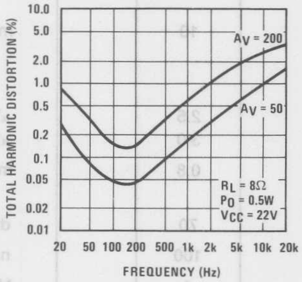
Channel Separation (Referred to the Output) vs Frequency



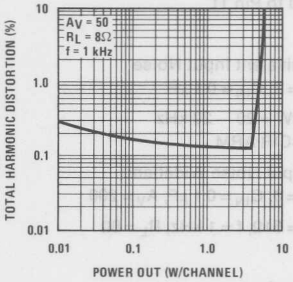
Total Harmonic Distortion vs Frequency



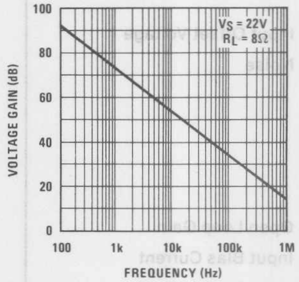
Total Harmonic Distortion vs Frequency



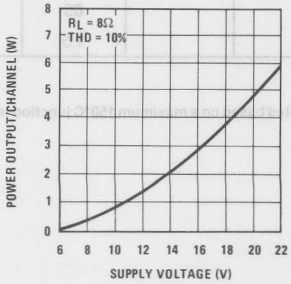
Total Harmonic Distortion vs Power Out



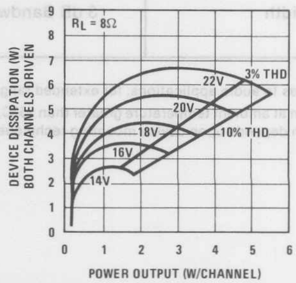
Open Loop Gain vs Frequency



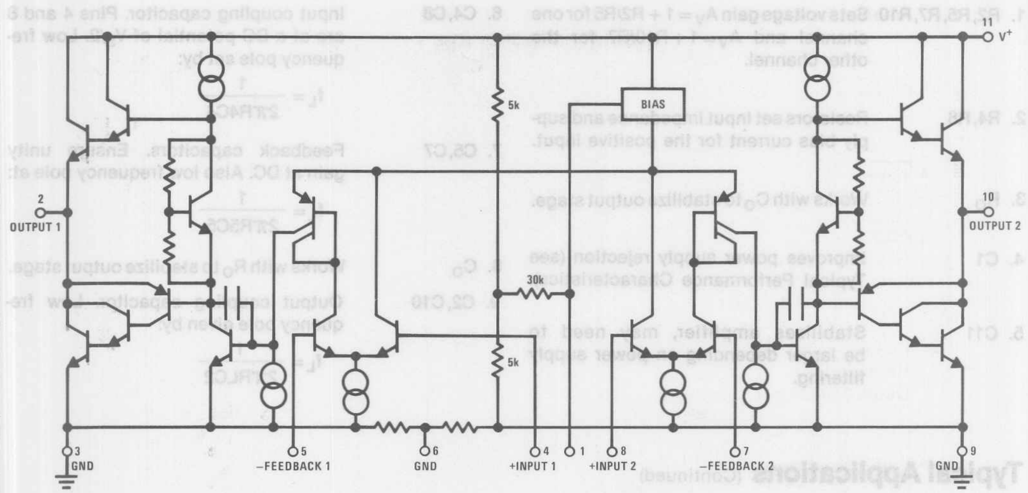
Power Output/Channel vs Supply Voltage



Power Dissipation vs Power Out

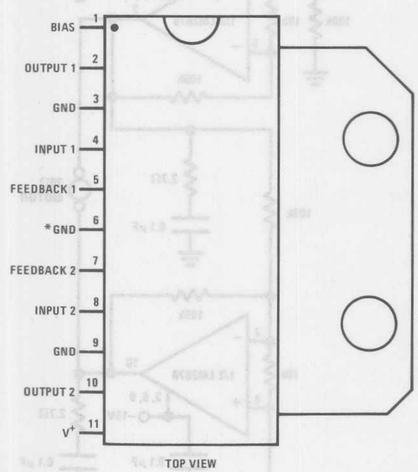


Equivalent Schematic Diagram



Connection Diagram

Single-In-Line Package



* Pin 6 can be connected to pin 3 or pin 9, if not, pin 6 must be left with NO connection.

Order Number LM2878P
See NS Package P11A

Application Hints

The LM2878 is an improved LM378 in typical audio applications. In the LM2878, the internal voltage regulator for the input stage is generated from the voltage on pin 1. Normally the inputs cannot common-mode more than 0.7V above this pin 1 voltage. Nevertheless the common-mode range can be increased by externally forcing the voltage on pin 1. One way to do this is to short pin 1 to the positive supply, pin 11.

The only special care required with the LM2878 is to limit the maximum input differential voltage to ±7V. If this differential voltage is exceeded, the input characteristics may alter.

Figure 2 shows a power op amp application with $A_V = 1$. The 100k and 10k resistors set a noise gain of 10 and are dictated by amplifier stability. The 10k resistor is bootstrapped by the feedback so the input resistance is dominated by the 1 MΩ resistor.

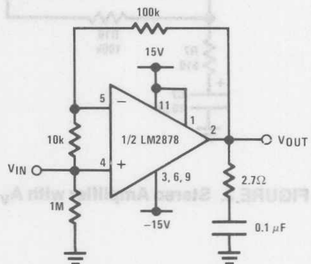


FIGURE 2. Operational Power Amplifier, $A_V = 1$

External Components *(Figure 3)*

1. R2, R5, R7, R10 — Sets voltage gain $A_V = 1 + R2/R5$ for one channel and $A_V = 1 + R10/R7$ for the other channel.
2. R4, R8 — Resistors set input impedance and supply bias current for the positive input.
3. R_O — Works with C_O to stabilize output stage.
4. C1 — Improves power supply rejection (see Typical Performance Characteristics).
5. C11 — Stabilizes amplifier, may need to be larger depending on power supply filtering.
6. C4, C8 — Input coupling capacitor. Pins 4 and 8 are at a DC potential of $V_S/2$. Low frequency pole set by:

$$f_L = \frac{1}{2\pi R4C4}$$

7. C5, C7 — Feedback capacitors. Ensure unity gain at DC. Also low frequency pole at:

$$f_L = \frac{1}{2\pi R5C5}$$

8. C_O — Works with R_O to stabilize output stage.
9. C2, C10 — Output coupling capacitor. Low frequency pole given by:

$$f_L = \frac{1}{2\pi RLC2}$$

Typical Applications (Continued)

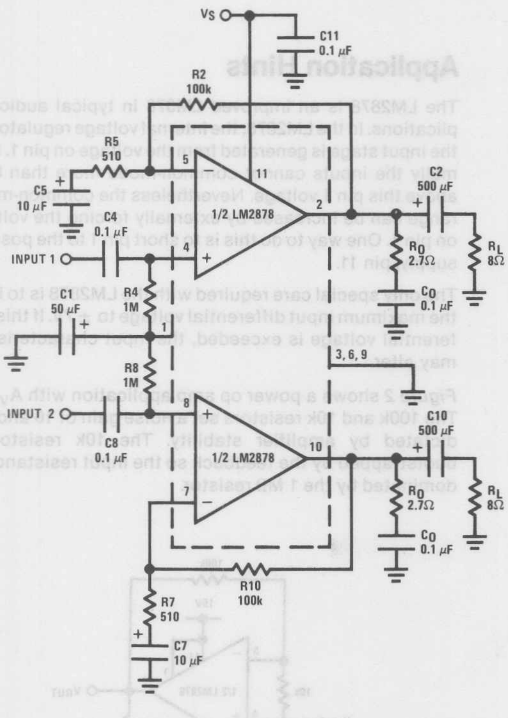


FIGURE 3. Stereo Amplifier with $A_V = 200$

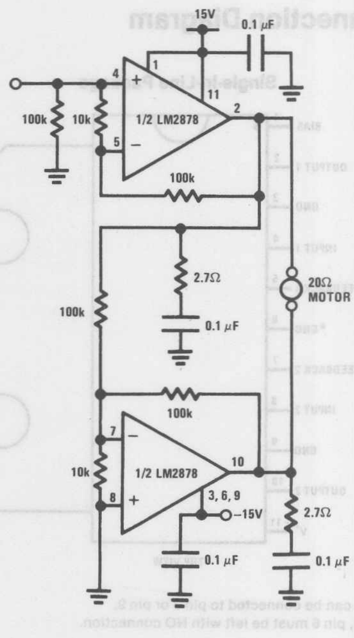
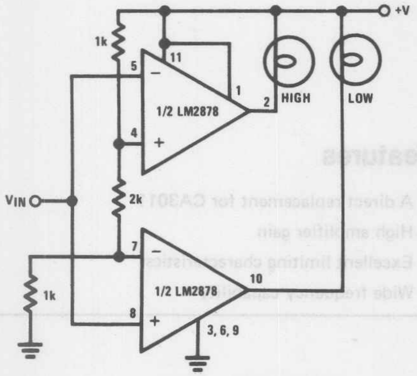


FIGURE 4. LM2878 Servo Amplifier in Bridge Configuration

Typical Applications (Continued)



TRUTH TABLE

V_{IN}	High	Low
< 1/4 V^+	Off	On
1/4 V^+ to 3/4 V^+	Off	Off
> 3/4 V^+	On	Off

FIGURE 5. Window Comparator Driving High, Low Lamps

LM3011 Wide Band Amplifier

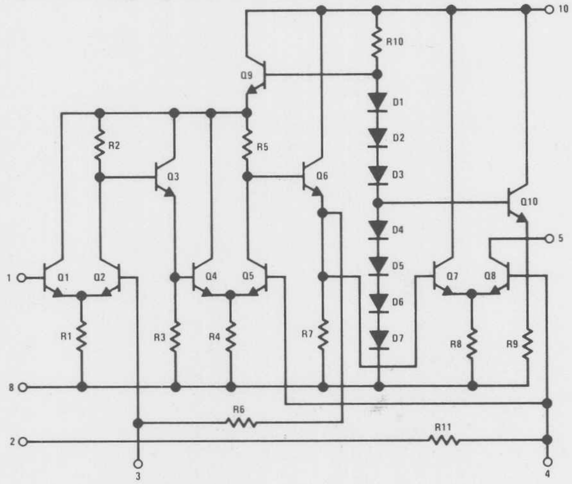
General Description

The LM3011 is a monolithic wide band amplifier circuit that requires a minimum of external components for operation. It includes three stages of limiting.

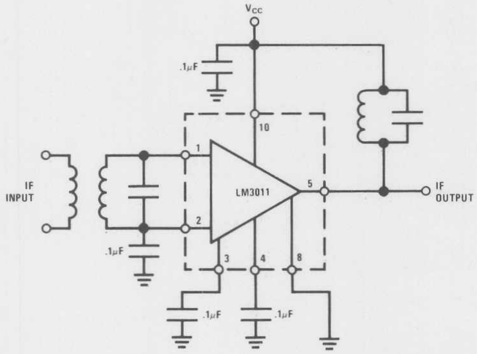
Features

- A direct replacement for CA3011
- High amplifier gain
- Excellent limiting characteristics
- Wide frequency capability

Schematic Diagram

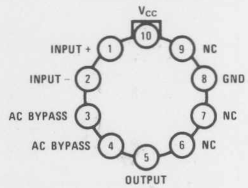


Block Diagram



Connection Diagram

Metal Can Package



Order Number LM3011H
See NS Package H10C

Absolute Maximum Ratings

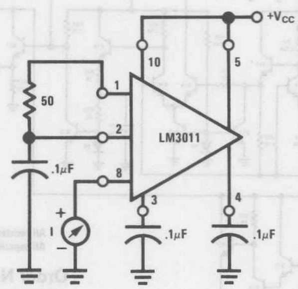
Supply Voltage	15V	Operating Temperature Range	−55°C to +75°C
Input Signal (Pin 1)	±3V	Storage Temperature Range	−65°C to +150°C
Power Dissipation (Note 1)	715 mW	Lead Temperature (Soldering, 10 sec)	300°C

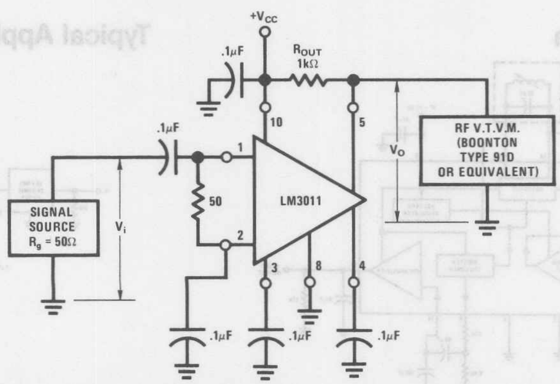
Electrical Characteristics (T_A = 25°C)

PARAMETER	CONDITIONS	LIMITS MIN	TYP	MAX	UNITS
STATIC CHARACTERISTICS					
Total Device Dissipation (P_T)	V_{CC} = 6V (Figure 1)	60	90	133	mW
Total Device Dissipation (P_T)	V_{CC} = 7.5V (Figure 1)	95	120	187	mW
DYNAMIC CHARACTERISTICS V_{CC} = 7.5V, F = 4.5 MHz, unless otherwise noted					
Voltage Gain (A)	V_{CC} = 6V, f = 1 MHz (Figure 2)	60	66		dB
Voltage Gain (A)	V_{CC} = 7.5V, f = 1 MHz (Figure 2)	65	70		dB
Voltage Gain (A)	V_{CC} = 7.5V, f = 10.7 MHz (Figure 2)	55	61		dB
Parallel Input Resistance (R_{IN})			3		kΩ
Parallel Input Capacitance (C_{IN})			7		pF
Parallel Output Resistance (R_{OUT})			31.5		kΩ
Parallel Output Capacitance (C_{OUT})			4.2		pF
Noise Figure (NF)			8.7		dB
Input Limiting Voltage ($V_{IN(Lim)}$)	(−3 dB) (Figure 2)		300	400	μV

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 175°C/W junction to ambient.

Test Circuits





National Semiconductor

LM3075 FM Detector/Limiter and Audio Preamplifier

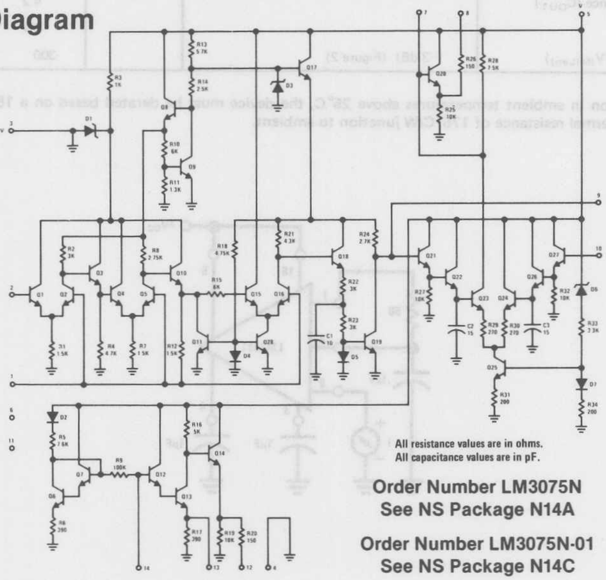
General Description

The LM3075 is a monolithic integrated circuit FM detector/limiter and audio preamplifier that requires a minimum of external components for operation. It includes three stages of IF limiting and a differential-peak-detection circuit.

Features

- A direct replacement for the CA3075
- Simple detector alignment: one coil
- Sensitivity: 3 dB limiting voltage 250 μV typical at 10.7 MHz
- Low harmonic distortion
- Excellent AM rejection 55 dB typ. at 10.7 MHz
- Internal audio preamplifier

Schematic Diagram

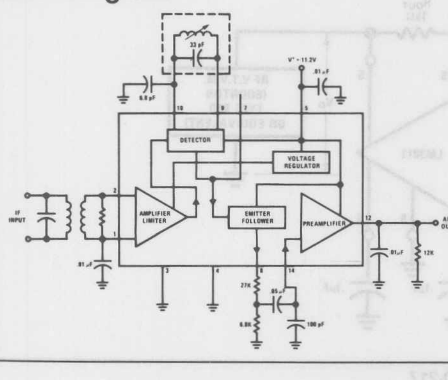


All resistance values are in ohms.
All capacitance values are in pF.

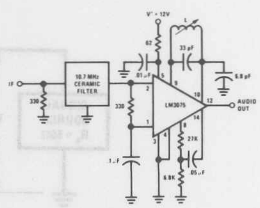
Order Number LM3075N
See NS Package N14A

Order Number LM3075N-01
See NS Package N14C

Block Diagram



Typical Application



Absolute Maximum Ratings

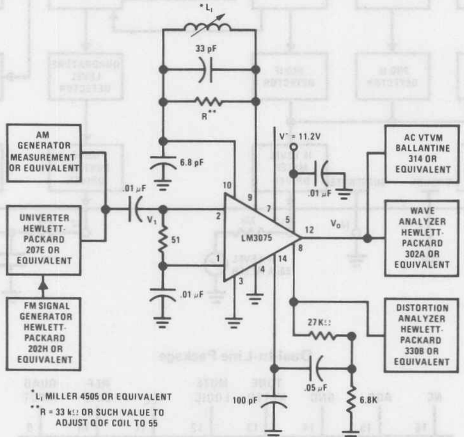
Power Supply Current (Pin 5)	30 mA	Operating Temperature Range	−40°C to +85°C
Supply Voltage (Pin 5)	12.5V	Storage Temperature Range	−65°C to +150°C
Power Dissipation (Note 1)	715 mW	Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics $T_A = 25°C$

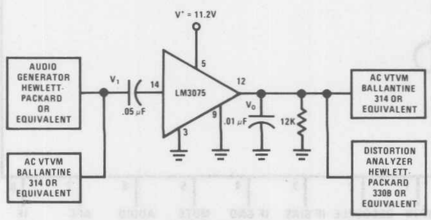
PARAMETER	SYMBOL	TEST CIRCUIT	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
STATIC CHARACTERISTICS							
Supply Current	I_5		$V_{CC} = 8.5V$	8.5	15		mA
			$V_{CC} = 11.2V$		17.5		mA
			$V_{CC} = 12.5V$		19	29	mA
Detector Output Level (High)	V_7				6.1		V
Detector Output Level (Low)	V_8		$V_{CC} = 11.2V$		5.4		V
Audio Amplifier Output Level	V_{12}				5.2		V
DYNAMIC CHARACTERISTICS AT $V^+ = 11.2V$, $f_0 = 10.7$ MHz, $\Delta f = \pm 75$ kHz, fm = 400 Hz							
Input Limiting Threshold	$V_{IN(LIM)}$	1			250	600	μV
AM Rejection	AMR	1	AM: 1 kHz @ 30%, $V_{IN} = 100$ mV		55		dB
Recovered AF Voltage (At Terminal 12)	V_O (AF)	1			1.5		V
Total Harmonic Distortion	T_{HD}	1			1	2	%
Audio Preamplifier							
Voltage Gain	$A_{V(af)}$	2	$V_{IN} = 100$ mV, f = 400 Hz		21		dB
Total Harmonic Distortion	T_{HD}	2	$V_{OUT} = 2V$, f = 400 Hz		1.5	5	%

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 175°C/W junction to ambient.

Test Circuits



TEST CIRCUIT 1



TEST CIRCUIT 2

LM3089 FM Receiver IF System

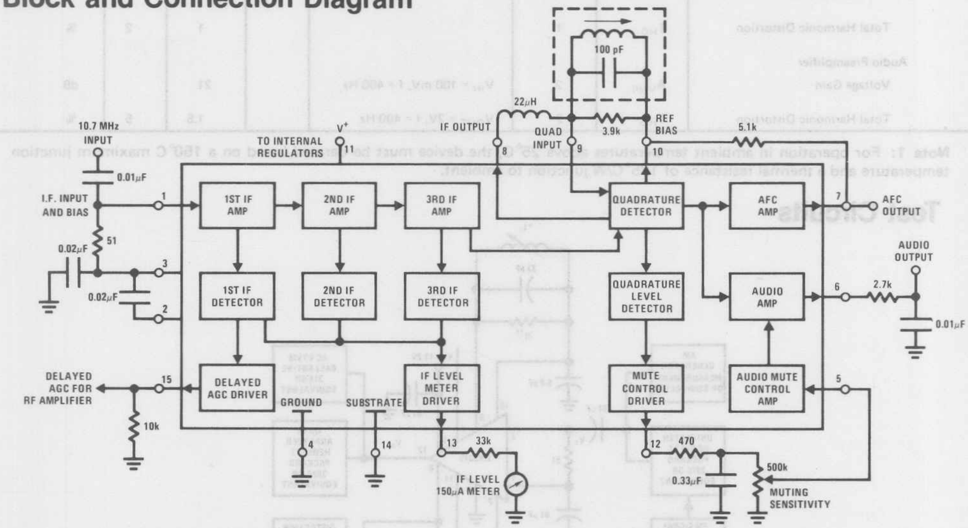
General Description

The LM3089 has been designed to provide all the major functions required for modern FM IF designs of automotive, high-fidelity and communications receivers.

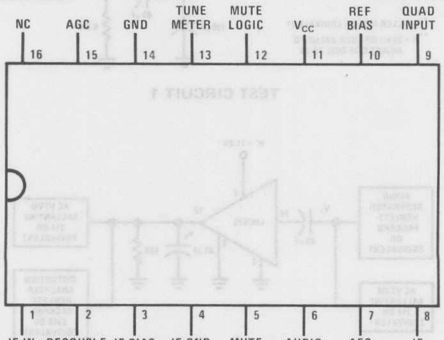
Features

- Three stage IF amplifier/limiter provides 12μV (typ) −3 dB limiting sensitivity
- Balanced product detector and audio amplifier provide 400 mV (typ) of recovered audio with distortion as low as 0.1% with proper external coil designs
- Four internal carrier level detectors provide delayed AGC signal to tuner, IF level meter drive current and interchannel mute control
- AFC amplifier provides AFC current for tuner and/or center tuning meters
- Improved operating and temperature performance, especially when using high Q quadrature coils in narrow band FM communications receivers
- No mute circuit latchup problems
- A direct replacement for CA3089E

Block and Connection Diagram



Dual-In-Line Package



TOP VIEW

Order Number LM3089N
See NS Package N16E

Absolute Maximum Ratings

Supply Voltage Between Pin 11 and Pins 4, 14	+16V	Power Dissipation (Note 2)	1390 mW
DC Current Out of Pin 12	5 mA	Operating Temperature Range	−40°C to +85°C
DC Current Out of Pin 13	5 mA	Storage Temperature Range	−65°C to +150°C
DC Current Out of Pin 15	2 mA	Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (T_A = 25°C, V_{CC} = +12V, see Test Circuit)

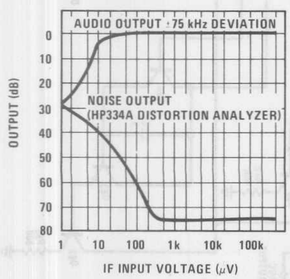
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS (V_{IN} = 0, NOT MUTED)						
I_{11}	Supply Current		16	23	30	mA
V1, 2, 3	IF Input and Bias		1.2	1.9	2.4	V
V6	Audio Output		5.0	5.6	6.0	V
V7	AFC Output		5.0	5.6	6.0	V
V10	Reference Bias		5.0	5.6	6.0	V
V12	Mute Control		5.0	5.4	6.0	V
V13	IF Level			0	0.5	V
V15	Delayed AGC		4.2	4.7	5.3	V
DYNAMIC CHARACTERISTICS f_o = 10.7 MHz, Δf = ±75 kHz @ 400 Hz						
V_{IN}(LIM)	Input Limiting −3 dB			12	25	μV
AMR	AM Rejection	V_{IN} = 100 mV, AM: 30%	45	55		−dB
V_O (AF)	Recovered Audio	V_{IN} = 10 mV	300	400	500	mVrms
THD	Total Harmonic Distortion					
	Single Tuned (Note 1)	V_{IN} = 100 mV		0.5	1.0	%
	Double Tuned (Note 1)	V_{IN} = 100 mV		0.1	0.3	%
S+N/N	Signal to Noise Ratio	V_{IN} = 100 mV	60	70		dB
V12	Mute Control	V_{IN} = 100 mV		0	0.5	V
V13	IF Level	V_{IN} = 100 mV	4.0	5.0	6.0	V
V13	IF Level	V_{IN} = 500μV	1.0	1.5	2.0	V
V15	Delayed AGC	V_{IN} = 100 mV		0.1	0.5	V
V15	Delayed AGC	V_{IN} = 30 mV		2.5		V
V_O(AF)	Audio Muted	V_{IN} = 100 mV, V5 = +2.5V		60		−dB

Note 1: Distortion is a function of quadrature coil used.

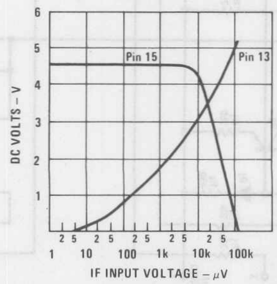
Note 2: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 90°C/W junction to ambient.

Typical Performance Characteristics

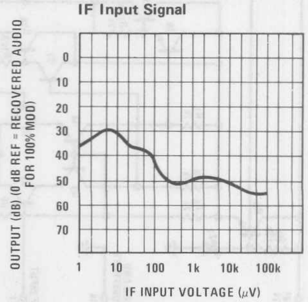
Typical S + N/N and IF Limiting Sensitivity vs IF Input Signal



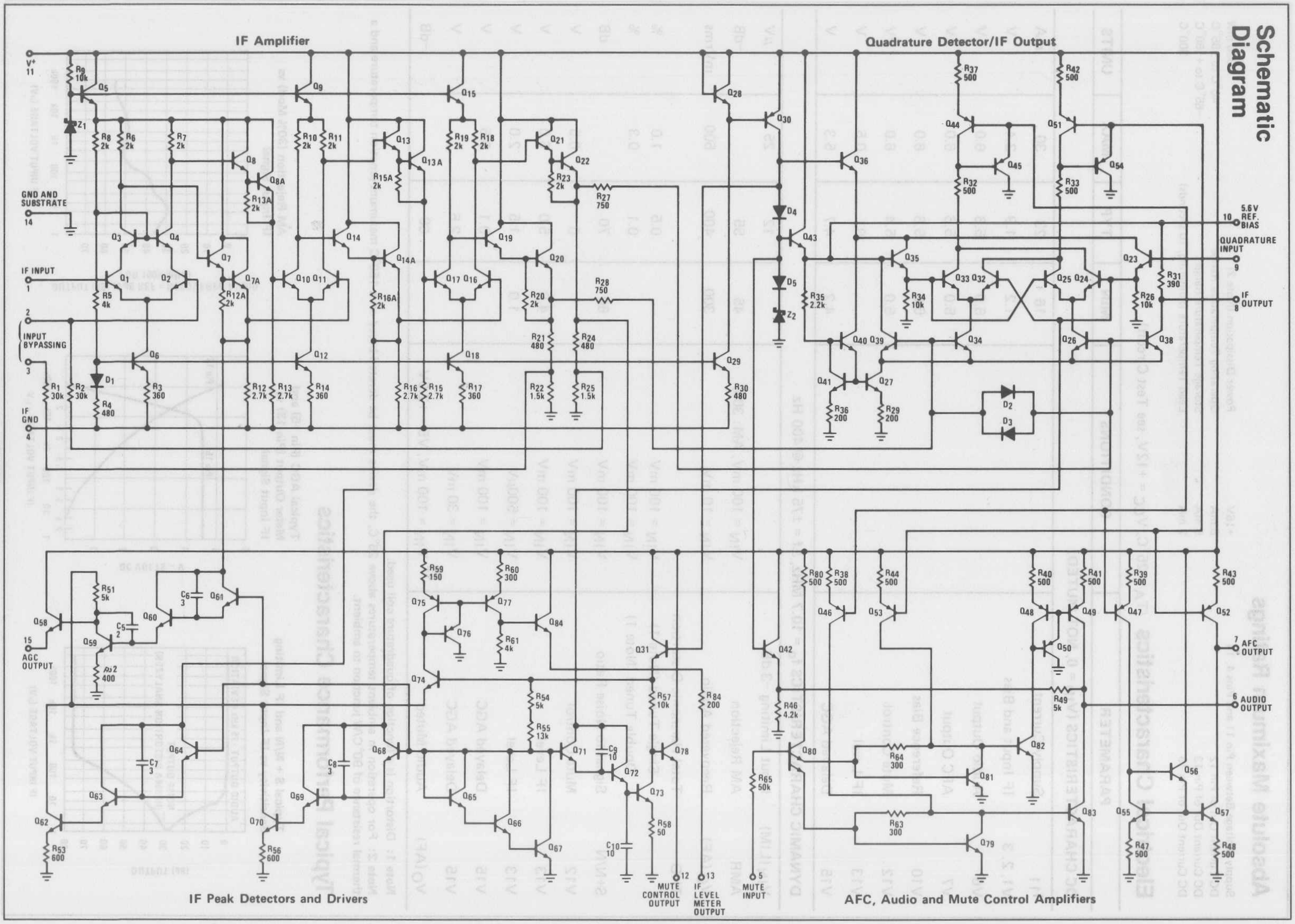
Typical AGC (Pin 15) and Meter Output (Pin 13) vs IF Input Signal



AM Rejection (30% Mod) vs IF Input Signal

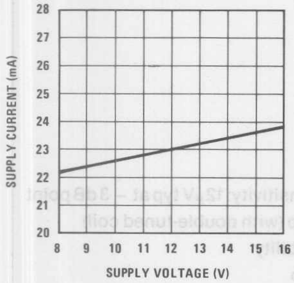


Schematic Diagram

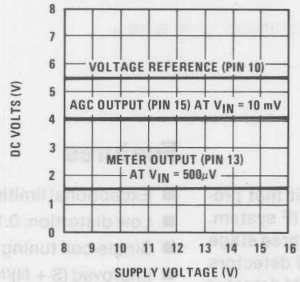


Typical Performance Characteristics (Continued)

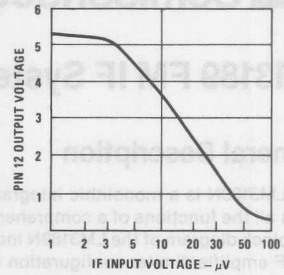
Supply Current (I_{11}) vs Supply Voltage (V11)



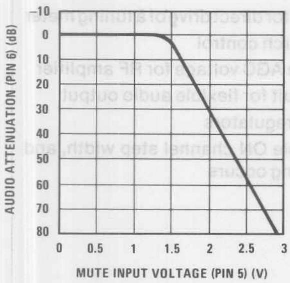
Reference Voltage, AGC and Meter Output vs Supply Voltage



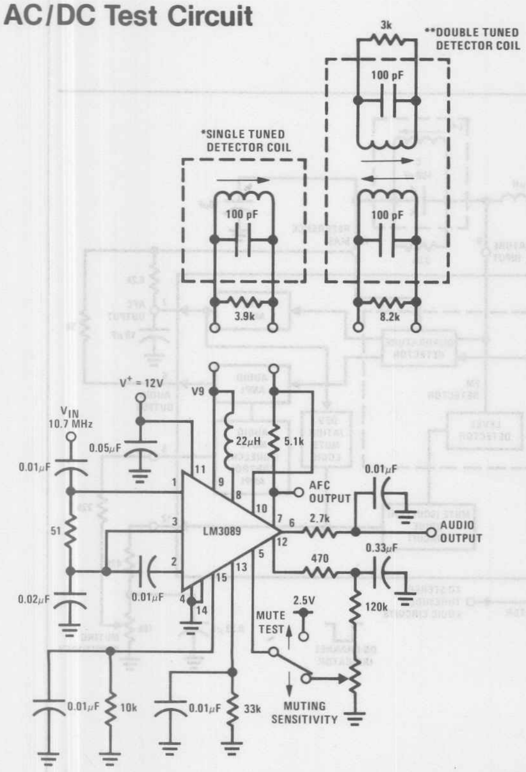
Mute Control Output (Pin 12) vs IF Input Signal



Typical Audio Attenuation (Pin 6) vs Mute Input Voltage (Pin 5)



AC/DC Test Circuit



*For single tuned detector coil:
L_O tunes with 100 pF at 10.7 MHz
Q_{UL} (unloaded) ≅ 75
Q_L (loaded) ≅ 13 for V9 ≅ 150 mVrms

**For double tuned detector coil:
$Q_{ULPRI} = Q_{ULSEC}$ ≅ 75
kQ ≅ 0.7 for V9 ≅ 150 mVrms

Note:
The recovered audio output voltage will be approximately 0.5 dB less when using the double tuned detector coil.

For proper operation of the mute circuit, the RF voltage at pin 9 should be 150 mVrms ±30 mV.

Semiconductor

LM3189 FM IF System

General Description

The LM3189N is a monolithic integrated circuit that provides all the functions of a comprehensive FM IF system. The block diagram of the LM3189N includes a three stage FM IF amplifier/limiter configuration with level detectors for each stage, a doubly balanced quadrature FM detector and an audio amplifier that features the optional use of a muting (squelch) circuit.

The advanced circuit design of the IF system includes desirable deluxe features such as programmable delayed AGC for the RF tuner, an AFC drive circuit, and an output signal to drive a tuning meter and/or provide stereo switching logic. In addition, internal power supply regulators maintain a nearly constant current drain over the voltage supply range of +8.5V to +16V.

The LM3189N is ideal for high fidelity operation. Distortion in an LM3189N FM IF system is primarily a function of the phase linearity characteristic of the outboard detector coil.

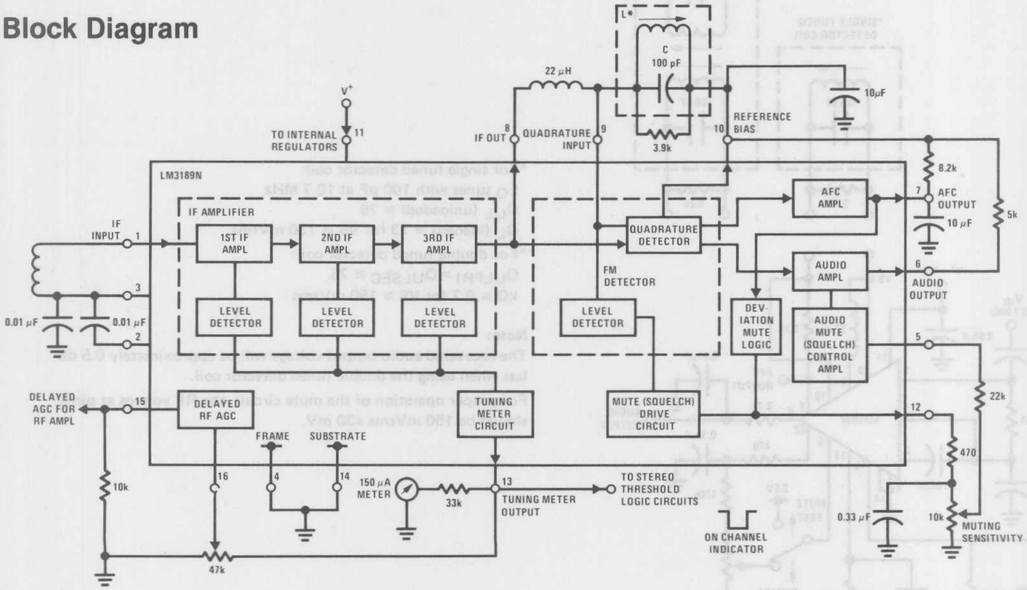
The LM3189N has all the features of the LM3039N plus additions.

The LM3189N utilizes the 16-lead dual-in-line plastic package and can operate over the ambient temperature range of −40°C to +85°C.

Features

- Exceptional limiting sensitivity: 12 μV typ at −3 dB point
- Low distortion: 0.1% typ (with double-tuned coil)
- Single-coil tuning capability
- Improved (S+N)/N ratio
- Externally programmable recovered audio level
- Provides specific signal for control of inter-channel muting (squelch)
- Provides specific signal for direct drive of a tuning meter
- On channel step for search control
- Provides programmable AGC voltage for RF amplifier
- Provides a specific circuit for flexible audio output
- Internal supply voltage regulators
- Externally programmable ON channel step width, and deviation at which muting occurs

Block Diagram



All resistance values are in ohms

* L tunes with 100 pF (C) at 10.7 MHz, $Q_O \cong 75$ (Toko No. KACS K586HM or equivalent)

Absolute Maximum Ratings

Supply Voltage Between Pin 11 and Pins 4, 14	16V
DC Current Out of Pin 12	5 mA
DC Current Out of Pin 13	5 mA
DC Current Out of Pin 15	2 mA
Power Dissipation (Note 2)	1390 mW
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics $T_A = 25°C$, $V^+ = 12V$

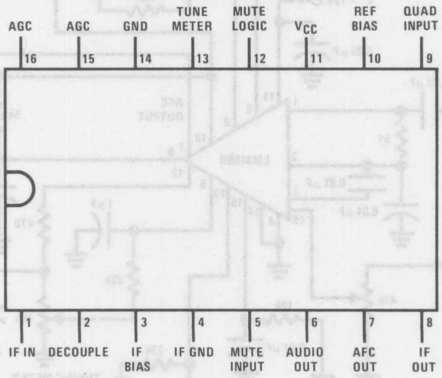
Symbol	Parameter	Conditions (see single-tuned test circuit)		Min	Typ	Max	Units
STATIC (DC) CHARACTERISTICS							
I_{11}	Quiescent Circuit Current	No Signal Input, Non Muted		20	31	44	mA
	DC Voltages:						
V1	Terminal 1 (IF Input)	No Signal Input, Non Muted		1.2	2.0	2.4	V
V2	Terminal 2 (AC Return to Input)	No Signal Input, Non Muted		1.2	2.0	2.4	V
V3	Terminal 3 (DC Bias to Input)	No Signal Input, Non Muted		1.2	2.0	2.4	V
V15	Terminal 15 (RF AGC)	No Signal Input, Non Muted		7.5	9.5	11	V
V10	Terminal 10 (DC Reference)	No Signal Input, Non Muted		5	5.75	6	V
DYNAMIC CHARACTERISTICS							
V_I(lim)	Input Limiting Voltage (−3 dB Point)		$f_o = 10.7$ MHz, $f_{mod} = 400$ Hz, Deviation ±75 kHz		12	25	μV
AMR	AM Rejection (Term. 6)	$V_{IN} = 0.1V$ AM Mod. = 30%	$f_o = 10.7$ MHz, $f_{mod} = 400$ Hz, Deviation ±75 kHz	45	55		dB
V_O(AF)	Recovered AF Voltage (Term. 6)	$V_{IN} = 0.1V$	$f_o = 10.7$ MHz, $f_{mod} = 400$ Hz, Deviation ±75 kHz	325	500	650	mV
THD	Total Harmonic Distortion (Note 1) Single Tuned (Term. 6) Double Tuned (Term. 6)	$V_{IN} = 0.1V$	$f_o = 10.7$ MHz, $f_{mod} = 400$ Hz, Deviation ±75 kHz		 0.5 0.1	 1	 % %
S + N/N	Signal plus Noise to Noise Ratio (Term. 6)	$V_{IN} = 0.1V$	$f_o = 10.7$ MHz, $f_{mod} = 400$ Hz, Deviation ±75 kHz	65	80		dB
f_{DEV}	Deviation Mute Frequency		$f_{mod} = 0$		±40		kHz
V16	RF AGC Threshold				1.25		V
V12	On Channel Step	$V_{IN} = 0.1V$	$f_{DEV} < \pm 40$ kHz $f_{DEV} > \pm 40$ kHz		0 5.6		V

Note 1: THD characteristics are essentially a function of the phase characteristics of the network connected between terminals 8, 9, and 10.

Note 2: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 90°C/W junction to ambient.

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number LM3189N
See NS Package N16E

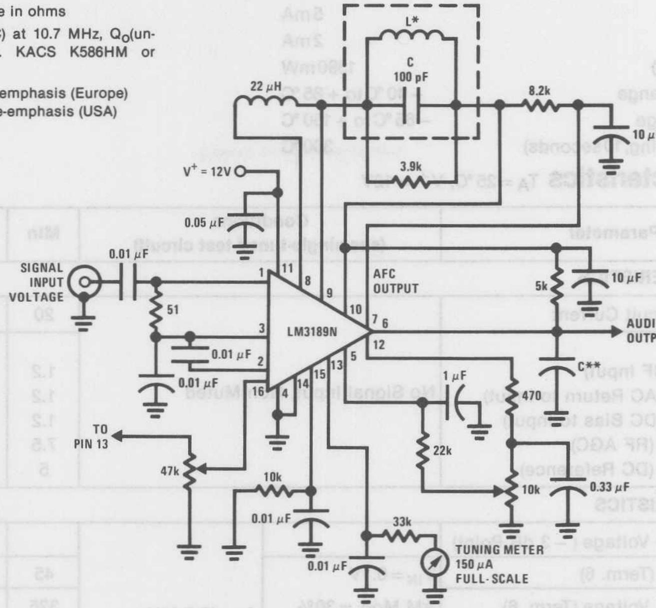
Test Circuits

Test Circuit for LM3189N Using a Single-Tuned Detector Coil

All resistance values are in ohms

* L tunes with 100 pF (C) at 10.7 MHz, Q_O(unloaded) ≅ 75 (Toko No. KACS K586HM or equivalent)

** C = 0.01 μF for 50 μs de-emphasis (Europe)
= 0.015 μF for 75 μs de-emphasis (USA)

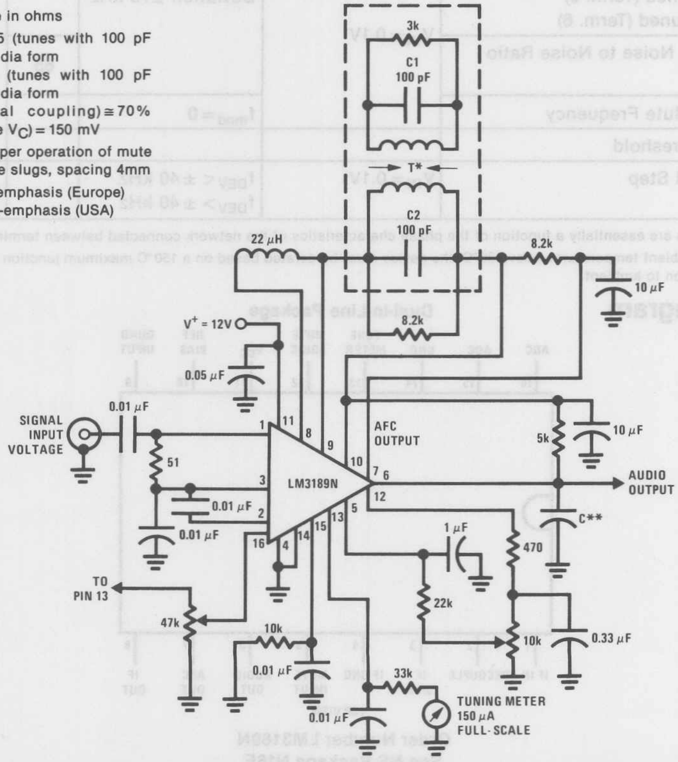


Test Circuit for LM3189N Using a Double-Tuned Detector Coil

All resistance values are in ohms

* T: PRI—Q_O(unloaded) ≅ 75 (tunes with 100 pF (C1)) 20t of 34e on 7/32" dia form
SEC—Q_O(unloaded) ≅ 75 (tunes with 100 pF (C2)) 20t of 34e on 7/32" dia form
kQ(percent of critical coupling) ≅ 70% (adjusted for coil voltage V_C) = 150 mV
Above values permit proper operation of mute (squelch) circuit "E" type slugs, spacing 4mm

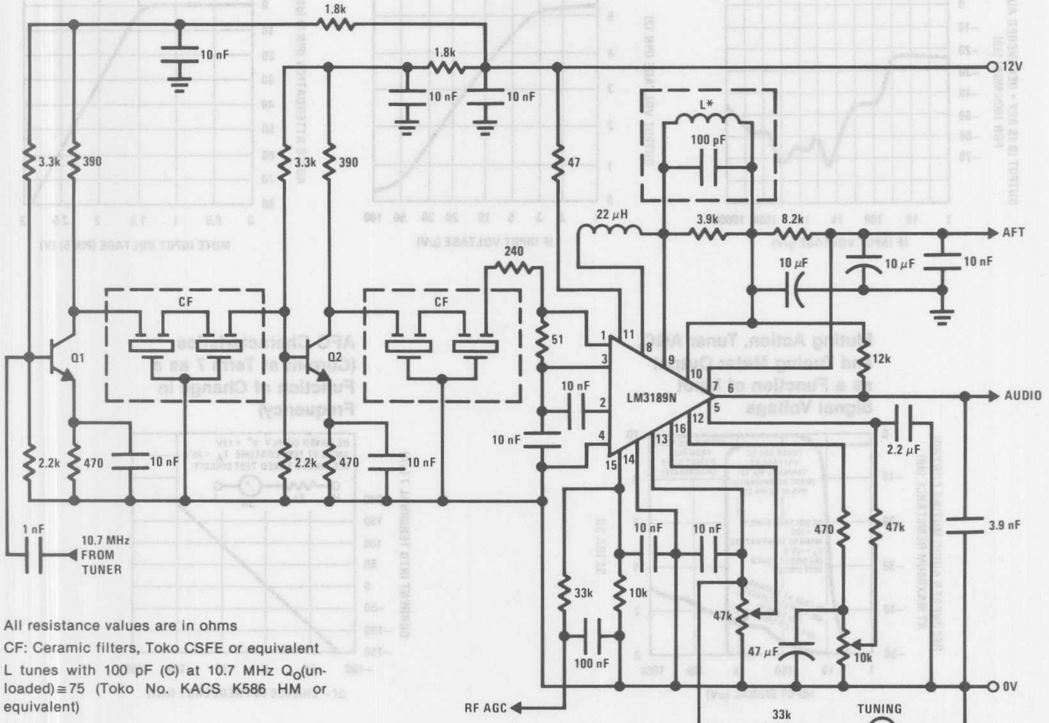
** C = 0.01 μF for 50 μs de-emphasis (Europe)
= 0.015 μF for 75 μs de-emphasis (USA)



Complete FM IF System for High Quality Tuners

The circuit provides a complete FM IF system for a high quality receiver. Either one or two stages of amplification and bandpass filtering may be desired, depending on the receiver requirements. See graph for Typical Limiting and Noise Characteristics for each circuit configuration which can be compared to the LM3189N alone.

Complete FM IF System for High Quality Receivers

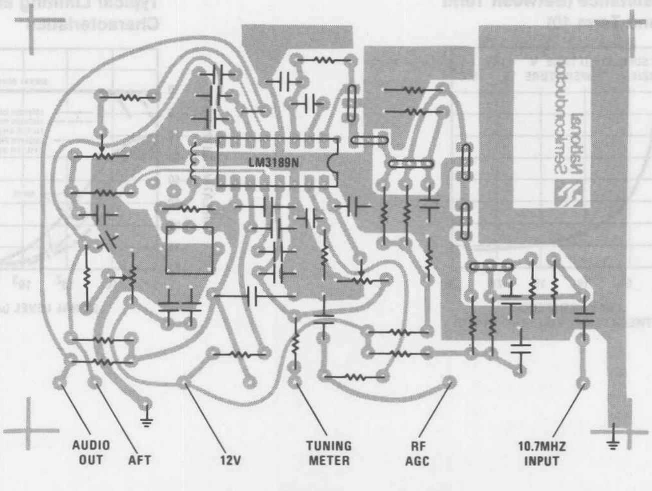


All resistance values are in ohms

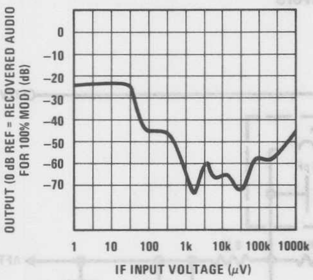
CF: Ceramic filters, Toko CSFE or equivalent

*L tunes with 100 pF (C) at 10.7 MHz Q_O(unloaded) ≅ 75 (Toko No. KACS K586 HM or equivalent)

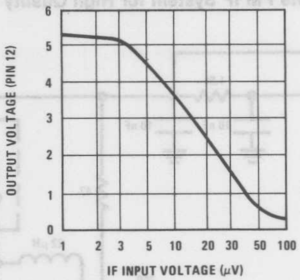
Printed Circuit Board and Component Layout



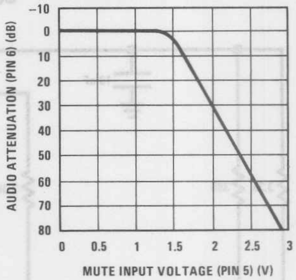
AM Rejection (30% Mod) vs IF Input Signal



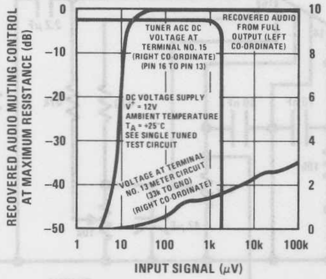
Mute Control Output (Pin 12) vs IF Input Signal



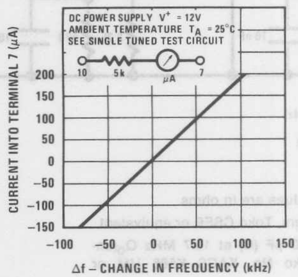
Typical Audio Attenuation (Pin 6) vs Mute Input Voltage (Pin 5)



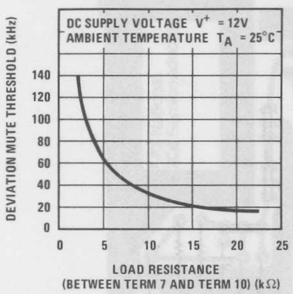
Muting Action, Tuner AGC, and Tuning Meter Output as a Function of Input Signal Voltage



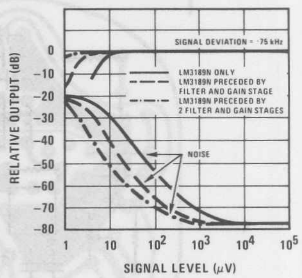
AFC Characteristics (Current at Term 7 as a Function of Change in Frequency)



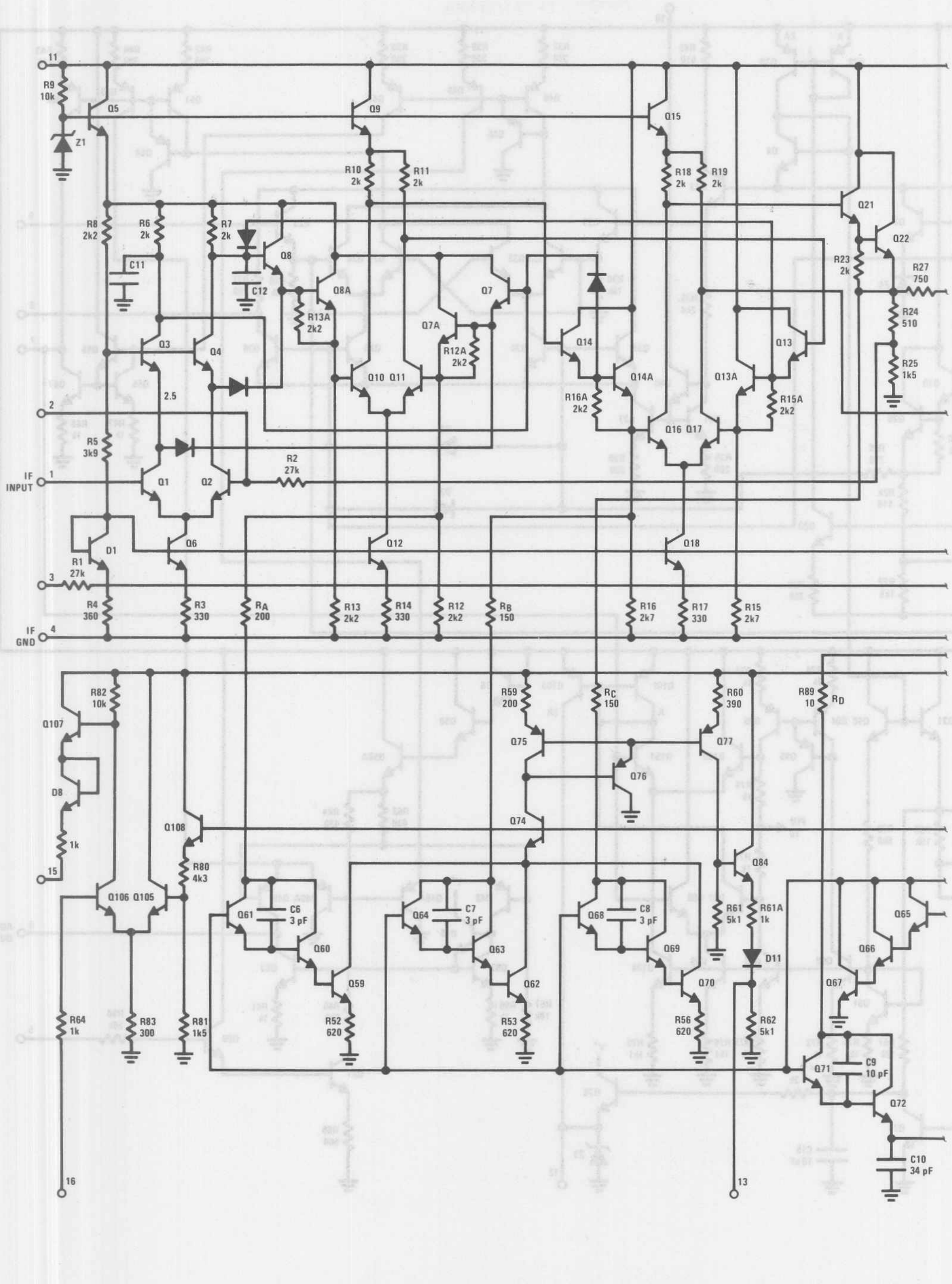
Deviation Mute Threshold as a Function of Load Resistance (Between Term 7 and Term 10)



Typical Limiting and Noise Characteristics



Schematic Diagram



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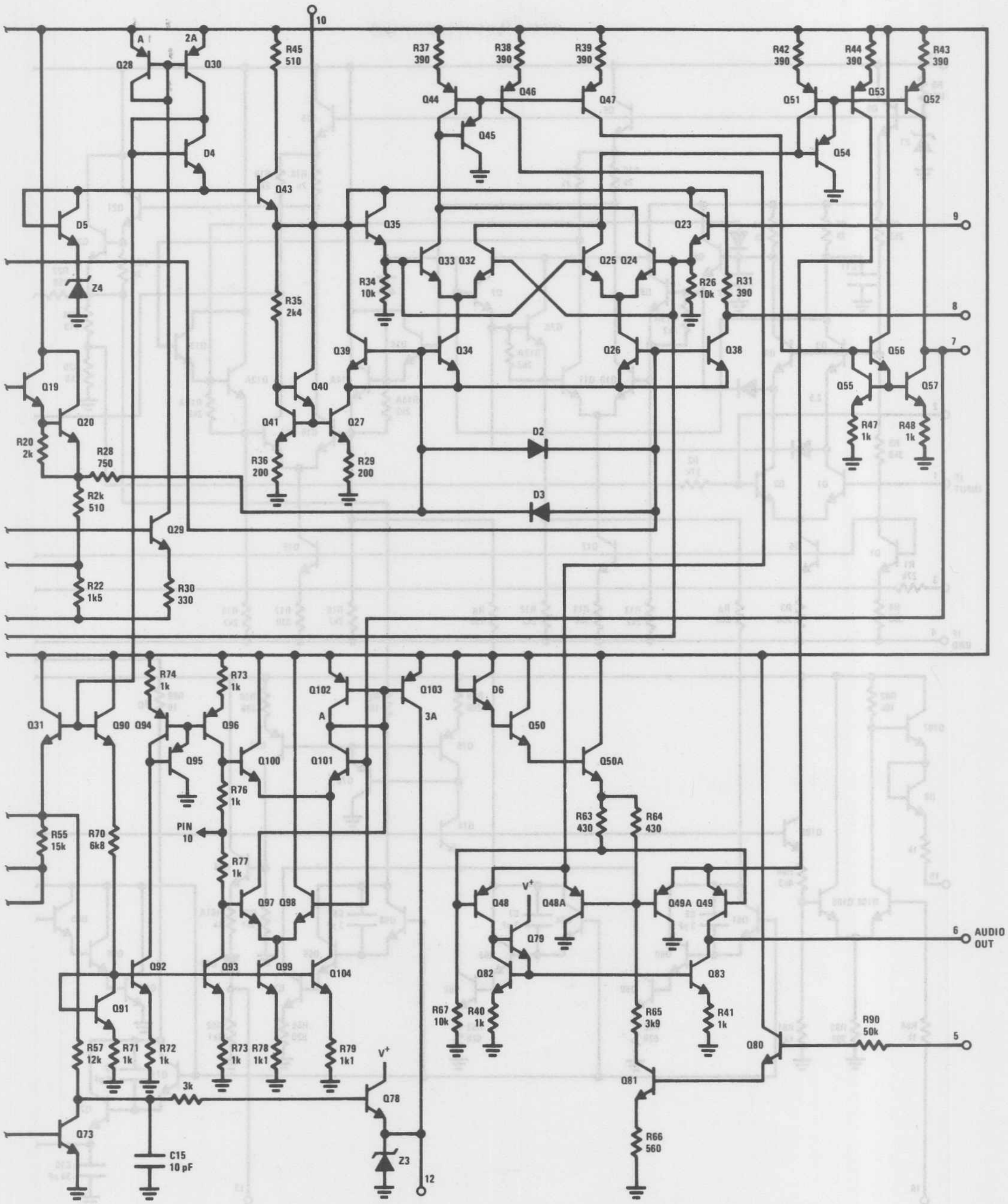
Schematic Diagram (Continued)



LM3820 AM Radio System

General Description

The LM3820 is a 3-stage AM radio IC consisting of an RF amplifier, oscillator, mixer, IF amplifier, AGC detector, and zener regulator.

The device was originally designed for use in slug-tuned auto radio applications, but is also suitable for capacitor-tuned portable radios.

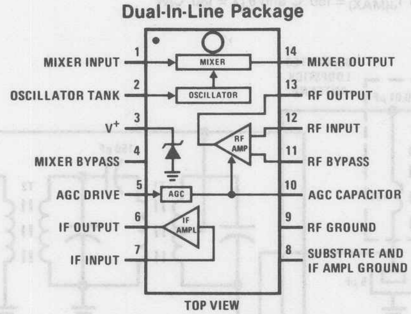
The LM3820 is an improved replacement for the LM1820.

Features

- Input protection diodes
- Good control on sensitivity
- Improved S/N and tweet
- Versatile building-block approach
- Gain-controlled RF stage
- Cascode IF amplifier
- Regulated supply
- Pin compatible with LM1820

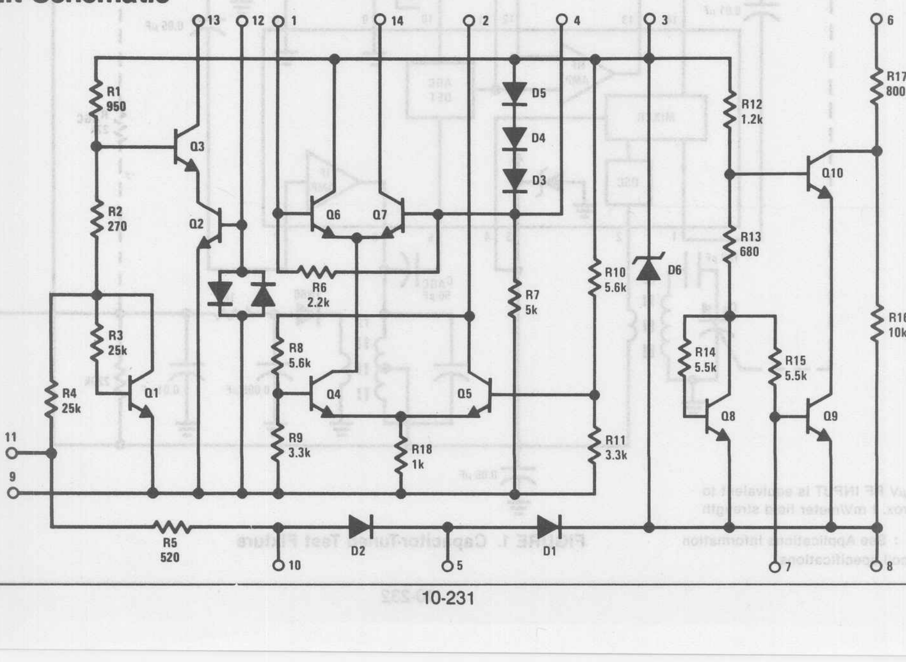
Connection Diagram

Dual-In-Line Package



Order Number LM3820N
See NS Package N14A

Circuit Schematic



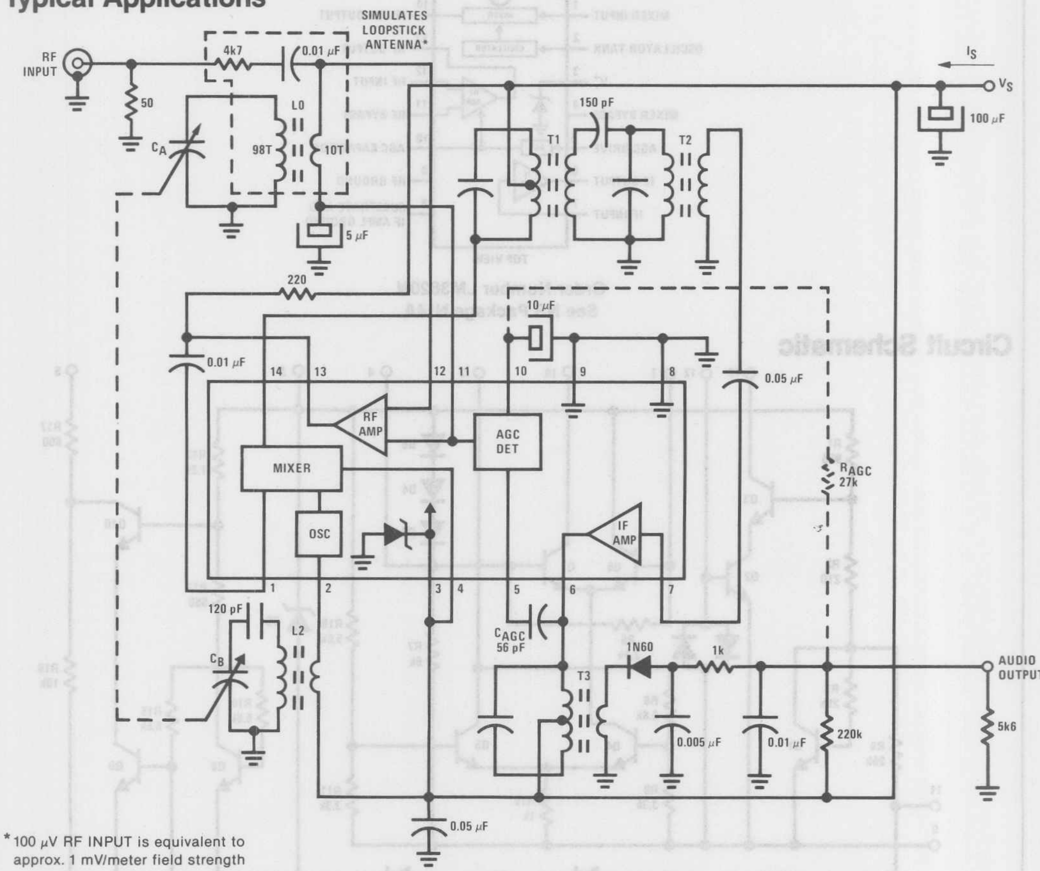
Current into Supply Terminal (Pin 3)	35 mA	Lead Temperature (Soldering, 10 seconds)	300 °C

Electrical Characteristics (*Figure 1*, $T_A = 25\,°C$, $V_S = 6V$ unless noted)

Parameter	Conditions	Min	Typ	Max	Units
Supply Current (I_S)	No RF Input	12	18	24	mA
Internal Zener Voltage (V_Z)		7.0	7.5	8.0	V
Input Sensitivity	f = 1 MHz, 30% Mod 400 Hz Measure RF Input Level for 10 mV Audio Output with Tuning Peaked	15	35	70	μV
Signal to Noise Ratio	f = 1 MHz, 30% Mod 1 kHz (S + N)/N at Audio Output with 100 μV RF Input	22	28	—	dB
Overload Distortion	f = 1 MHz, 90% Mod 1 kHz THD at Audio Output with 30 mV RF Input	—	6	10	%

Note 1: Above $T_A = 25\,°C$, derate based on $T_{J(MAX)} = 150\,°C$ and $\theta_{JA} = 180\,°C/W$

Typical Applications



*100 μV RF INPUT is equivalent to approx. 1 mV/meter field strength

: See Applications Information for coil specifications

FIGURE 1. Capacitor-Tuned Test Fixture

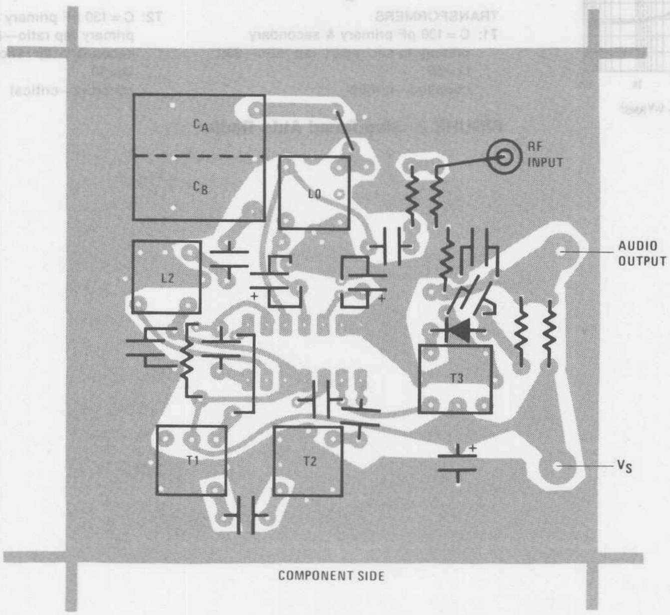
Applications Information

The circuit shown in *Figure 1* is recommended as a starting point for portable radio designs. Loopstick antenna L1 is used in place of L0, and the RF amplifier is used with a resistor load to drive the mixer. A double tuned circuit at the output of the mixer provides selectivity, while the remainder of the gain is provided by the IF section, which is matched to the diode through a unity turns ratio transformer. R_{AGC} may be used in place of C_{AGC} to bypass the internal AGC detector and provide more recovered audio.

An AM automobile radio design is shown in *Figure 2*. Tuning of both the input and the output of the RF amplifier and the mixer is accomplished with variable inductors. Better selectivity is obtained through the use of double tuned interstage transformers. Input circuits are inductively tuned to prevent microphonics and provide a linear tuning motion to facilitate push-button operation.

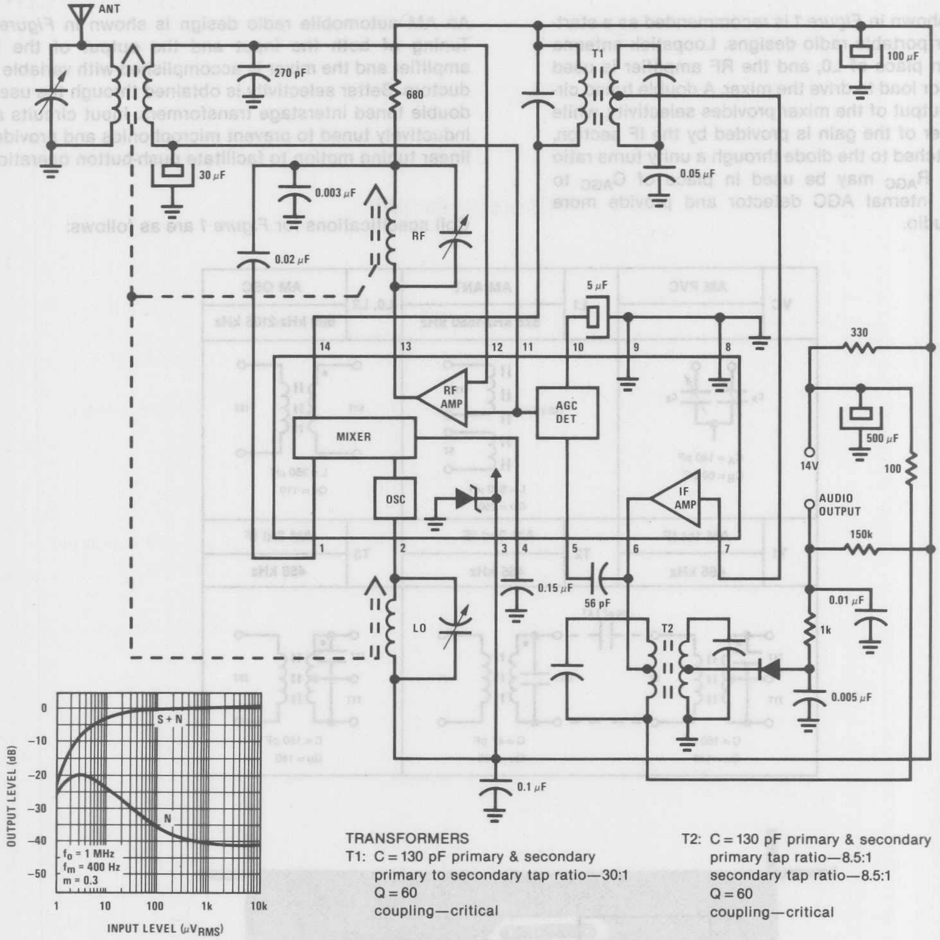
Coil specifications for *Figure 1* are as follows:

VC	AM PVC	L1	AM ANT 525 kHz-1650 kHz	L0, L2	AM OSC 980 kHz-2105 kHz
	C_A, C_B $C_A = 140$ pF $C_B = 60$ pF		100 x 8 mm, 110T, 5T L = 650 μH Qu = 250		98T, 10T L = 360 μH Qu = 110
T1	**AM 1st IF 455 kHz**	**T2**	**AM 2nd IF 455 kHz**	**T3**	**AM 3rd IF 455 kHz**
	71T, 71T, 2T C = 180 pF Qu = 140		150 pF EXT, 142T, 7T C = 47 pF Qu = 120		71T, 71T, 35T C = 180 pF Qu = 140



PCB Layout for *Figure 1* Circuit

Typical Applications (Continued)



TRANSFORMERS
T1: C = 130 pF primary & secondary
primary to secondary tap ratio—30:1
Q = 60
coupling—critical

T2: C = 130 pF primary & secondary
primary tap ratio—8.5:1
secondary tap ratio—8.5:1
Q = 60
coupling—critical

FIGURE 2. Slug-Tuned Auto Radio

National Semiconductor

Audio/Radio Circuits

LM4500A High Fidelity FM Stereo Demodulator with Blend

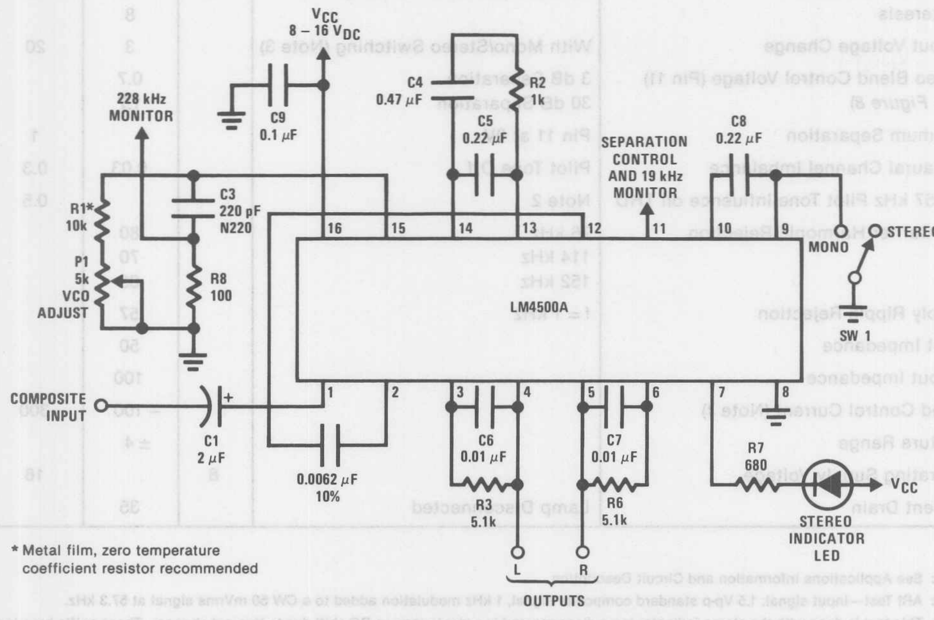
General Description

The LM4500A is an improved stereo demodulator IC offering very low audio distortion. A new demodulator technique minimizes adjacent station interference caused by subcarrier harmonics and prevents lock-up problems from pilot carrier frequency harmonics. The IC features a blend circuit which optimizes the signal-to-noise ratio under weak signal conditions by gradually combining left and right channel information.

Features

- Low distortion—0.1% typ
- High subcarrier harmonic rejection
- Large input dynamic range—2.5 Vp-p
- Voltage controlled blend
- High separation—fixed or adjustable
- Adjustable gain
- Reduced stereo-mono DC shift—5 mV typ
- 55 dB supply ripple rejection
- Low output impedance
- Requires no external inductors
- Wide supply range 8V-16V
- Excellent rejection of 57 kHz ARI subcarrier

Typical Application



* Metal film, zero temperature coefficient resistor recommended

FIGURE 1

Order Number LM4500AN
See NS Package N16A

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Power Dissipation (Package Limitation)	1800 mW
Derate above $T_A = +25°C$	15 mW/°C
Operating Temperature Range (Ambient)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lamp Drive Voltage	
Max Voltage at Pin 7 with Lamp "Off"	30V
Lamp Current	100 mA
Blend Control Input Voltage (Pin 11)	10V

Electrical Characteristics

Unless otherwise noted: $V_{CC} = 12\ V_{DC}$, $T_A = 25°C$, Vp-p standard multiplex composite signal with L or R channel only modulated at 1.0 kHz and with 10% pilot level, using circuit of *Figure 1*

Parameter	Conditions	Min	Typ	Max	Units
Stereo Channel Separation	Unadjusted	30			dB
	Optimized on Other Channel (Note 1)	40			dB
Measured Voltage Gain (Note 1)		0.8	1	1.2	
THD	2.5 Vp-p Composite Input Signal		0.15	0.3	%
	1.5 Vp-p Composite Input Signal		0.08		%
Signal-to-Noise Ratio	DIN45405 Quasi Peak Reading		83		dB
	rms 20 Hz-15 kHz		88		dB
Ultrasonic Frequency Rejection	19 kHz		31		dB
	38 kHz		45		dB
Stereo Switch Level	19 kHz Input Level for Lamp "On"	12	16	20	mVrms
Hysteresis			8		dB
Output Voltage Change	With Mono/Stereo Switching (Note 3)		3	20	mV_{DC}
Stereo Blend Control Voltage (Pin 11)	3 dB Separation		0.7		V
(See *Figure 8*)	30 dB Separation		1.7		V
Minimum Separation	Pin 11 at 0V			1	dB
Monaural Channel Imbalance	Pilot Tone Off		0.03	0.3	dB
ARI 57 kHz Pilot Tone Influence on THD	Note 2			0.5	%
Sub-Carrier Harmonic Rejection	76 kHz		80		dB
	114 kHz		70		dB
	152 kHz		83		dB
Supply Ripple Rejection	f = 1 kHz		57		dB
Input Impedance			50		kΩ
Output Impedance			100		Ω
Blend Control Current (Note 1)			−100	−300	μA
Capture Range			±4		%
Operating Supply Voltage		8		16	V
Current Drain	Lamp Disconnected		35		mA

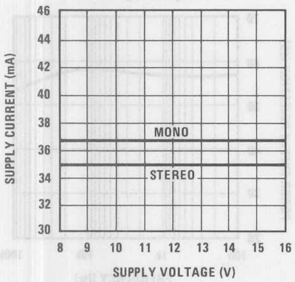
Note 1: See Applications Information and Circuit Description.

Note 2: ARI Test—input signal: 1.5 Vp-p standard composite signal, 1 kHz modulation added to a CW 50 mVrms signal at 57.3 kHz.

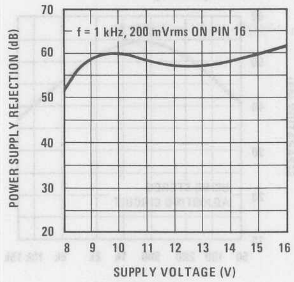
Note 3: This test is done with the stereo indicator lamp disconnected in order to remove DC shift due to thermal changes. These shifts have long time constants (100 ms) and therefore do not produce audible transients.

Typical Performance Characteristics

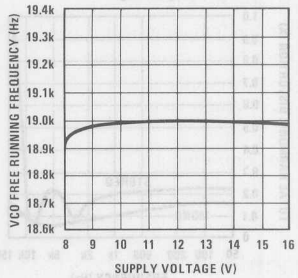
Supply Current vs Supply Voltage



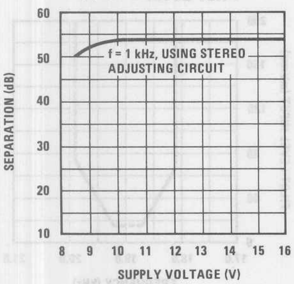
Power Supply Rejection vs Supply Voltage



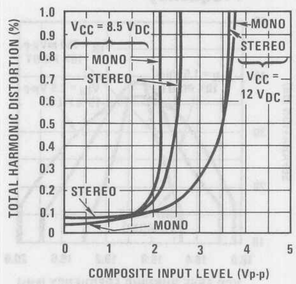
VCO Free Running Frequency vs Supply Voltage



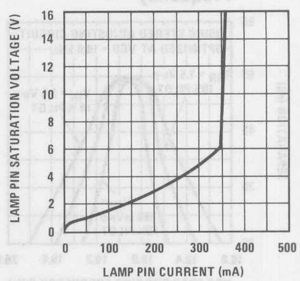
Channel Separation vs Supply Voltage



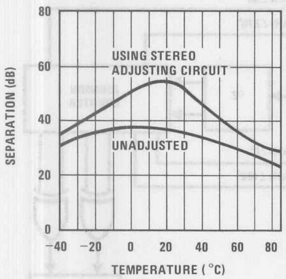
Total Harmonic Distortion vs Composite Input Level



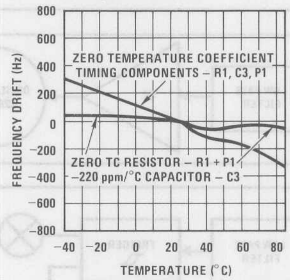
Lamp Pin Saturation Voltage vs Current



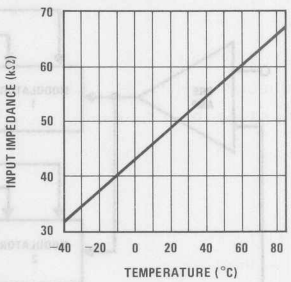
Stereo Separation vs Temperature



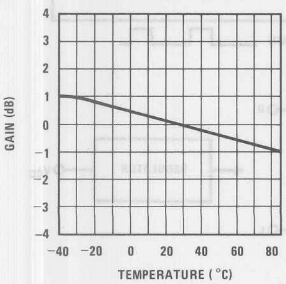
VCO Free Running Frequency Drift vs Temperature



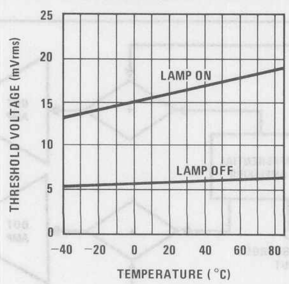
Input Impedance vs Temperature



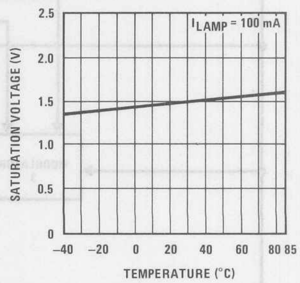
Gain vs Temperature



Stereo Switch Threshold vs Temperature

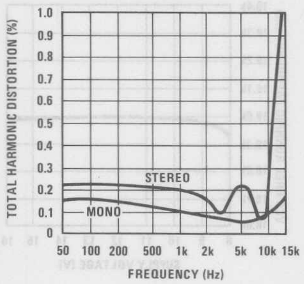


Lamp Pin Saturation Voltage vs Temperature

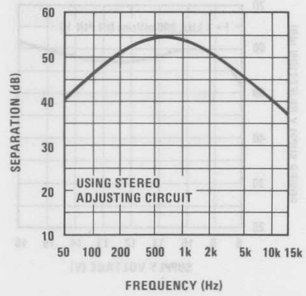


Typical Performance Characteristics (Continued)

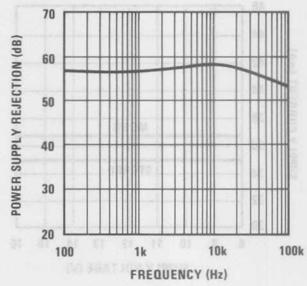
Total Harmonic Distortion vs Frequency



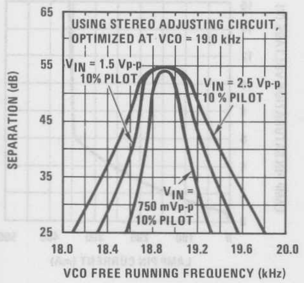
Separation vs Frequency



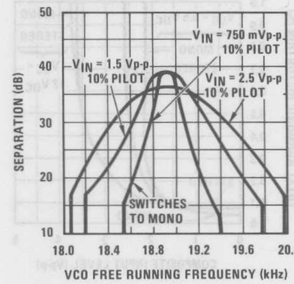
Power Supply Rejection vs Frequency



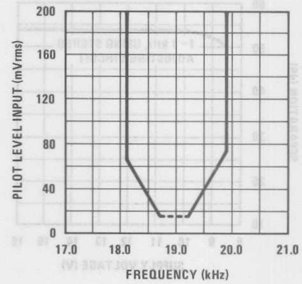
Adjusted Separation vs VCO Free Running Frequency



Unadjusted Separation vs VCO Free Running Frequency



Capture Range vs Pilot Level



Block Diagram

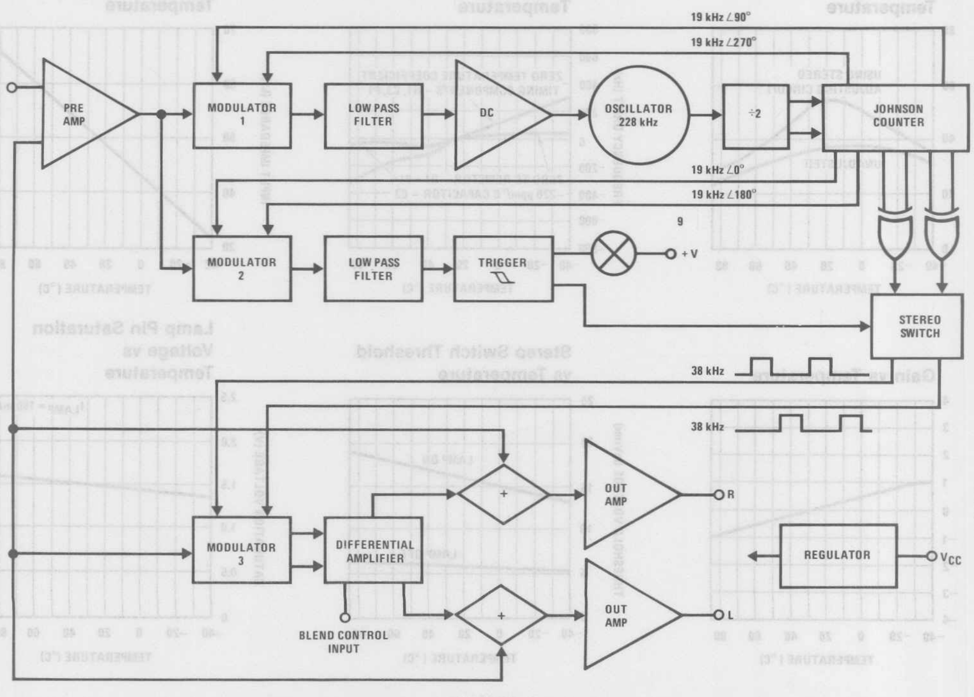


FIGURE 2

Circuit Description

Introduction

The LM4500A is a phase-lock-loop stereo decoder which incorporates a variable separation control, and in which sensitivity to the third harmonics of both the pilot and sub-carrier frequencies has been eliminated by the use of appropriate, digitally generated, waveforms in the phase-lock-loop and decoder sections.

The variable separation control may be operated manually, or by a receiver's AGC or S meter signals, to provide smooth transitions between monaural and stereo reception. It operates only during stereo reception: the circuit switches automatically to monaural if the 19 kHz pilot tone is absent.

The elimination of sensitivity to the third harmonic of the sub-carrier (114 kHz) excludes interference from the sidebands of adjacent transmitters, while the elimination of sensitivity to the third harmonic of the pilot tone (57 kHz) excludes interference from the ARI* system which employs this frequency.

Circuit Operation

The block diagram of the circuit, shown in *Figure 2*, consists of three sections, the phase-lock-loop, including the digital waveform generator, the stereo switch, and the decoder, in which the composite stereo signal is demodulated and matrixed to separate L and R channels.

In the phase-lock-loop the internal RC oscillator, operating at 228 kHz, feeds a 3-stage Johnson counter, via a binary divider, to generate a series of 19 kHz square waves. By the use of suitably connected NAND and EXCLUSIVE OR gates, the waveforms shown in *Figure 3*, which are used to drive the various modulators in the circuit, are developed.

*Auto Radio Information – used in Europe

The use of such drive waveforms produces the modulating functions also shown in *Figure 3*. The usual square waveforms have been replaced in the PLL and decoder sections by 3-level forms which contain no third harmonic (actually no harmonics which are multiples of 2 or 3 are present). This eliminates the frequency translation of interference from these bands into the low frequency region. Such translation may produce audible components in the decoder section from the sidebands of adjacent channel FM signals, and may produce phase jitter, and consequent intermodulation distortion, in the PLL, from the modulated 57 kHz tones of the ARI system. The LM4500A is inherently free from these effects.

The stereo switch section is of conventional form (e.g. LM1310).

The decoder section consists of a modulator (driven by the waveforms shown in *Figure 3*) whose outputs are the inverted and non-inverted channel difference signals. These signals pass to the output amplifiers via the variable blend circuit in which they are partially combined, and hence mutually attenuated, according to the control voltage applied.

Matrixing occurs at the inputs of the output amplifiers, where the unmodified composite signal is added to the blended channel difference signals. The stereo separation may be progressively reduced from maximum to zero; dependent on the blending. The control law has been made non-linear, as the major redistribution of sound energy occurs at very low separation levels. For monaural, or very weak stereo signals, the modulator in the decoder section is deactivated by the stereo switch circuit. The variable separation control is thus, also, automatically disabled.

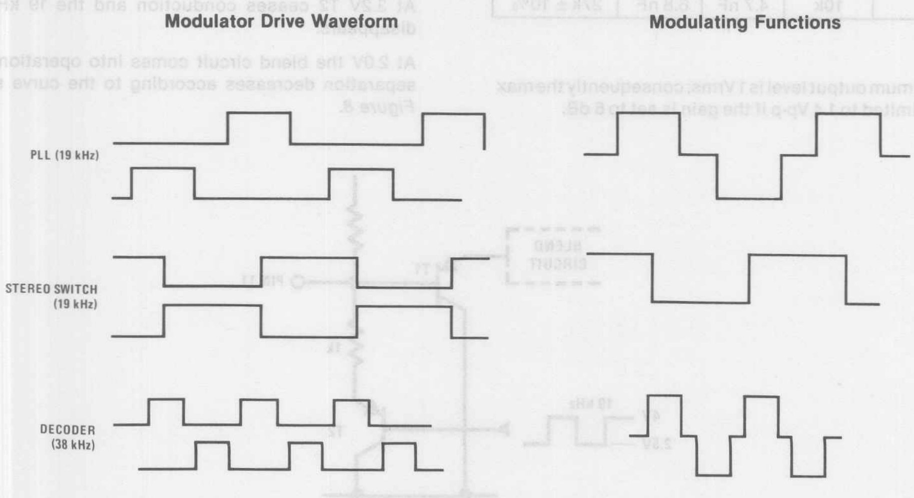


FIGURE 3. Digital Waveforms

defined by shunt feedback via the external RC networks (R3, C6, R4, C7 of *Figure 1*) around the output amplifiers. The gain is unity when resistors of 5.1 kΩ are used. Higher gains may be obtained by using networks of the form shown in *Figure 4*.

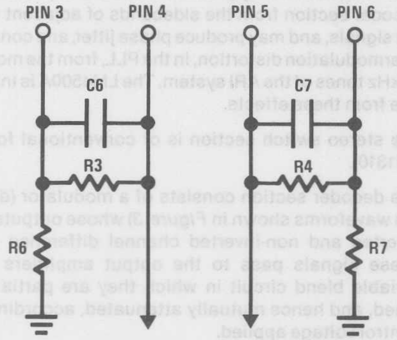


FIGURE 4. Output Amplifier Feedback Networks

The resistors R6, R7 are added to correct the output quiescent voltage levels which are optimised for R3,R4 = 5.1 kΩ and which would, if uncorrected, become too low with higher value resistors. Suitable network values are as follows:

Gain (dB)	R3, R4	C6, C7		R6, R7
		50 µs	75 µs	
0	5.1 kΩ	10 nF	15 nF	
3	6.8 kΩ	6.8 nF	10 nF	47k ± 10%
6	10k	4.7 nF	6.8 nF	27k ± 10%

The maximum output level is 1 Vrms; consequently the max input is limited to 1.4 Vp-p if the gain is set to 6 dB.

Figure 5, to compensate for the receiver's IF characteristics.

This network reduces the amplification of the channel sum signal in the decoder, to compensate the attenuation of the channel difference signal in the receiver's IF section. The network shown will compensate for up to 2 dB attenuation at 38 kHz. The decoder gain is, obviously, reduced by an amount equal to the compensation required. When used as described, the adjustment also corrects the inherent separation of the decoder, which may be optimised on one channel. Optimization of both channels is possible if separate potentiometers are used to feed each output amplifier.

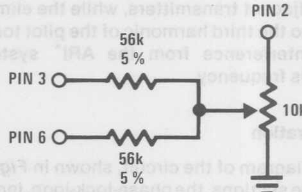


FIGURE 5. Network Providing Adjustable Separation

Variable Separation (Blend) Control and 19 kHz Output

To retain the 16-pin package the blend control has been combined with the 19 kHz output on pin 11. The internal circuit providing this combination is shown in *Figure 6*.

If pin 11 is left open-circuit the 19 kHz signal appears at a mean DC level of 4V. The blend circuit is inoperative at this level and the decoder provides full separation. The 19 kHz signal can be used to tune the internal oscillator.

To reduce the separation the voltage on pin 11 is reduced. At 3.2V T2 ceases conduction and the 19 kHz signal disappears.

At 2.0V the blend circuit comes into operation and the separation decreases according to the curve shown in *Figure 8*.

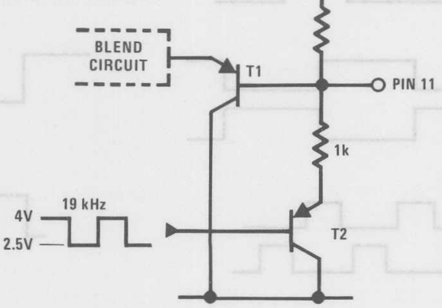


FIGURE 6. Blend Control Input Circuit

Applications Information (Continued)

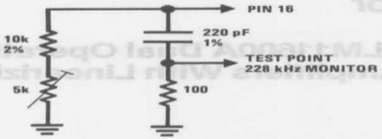


FIGURE 7. Oscillator Network for Direct Frequency Measurement

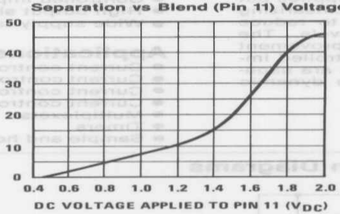


FIGURE 8

Oscillator Tuning

If the variable separation facility is not required pin 11 is left open-circuit and the 19 kHz signal which then appears may be used to indicate the oscillator frequency. If the variable separation is used, and the drive circuit prevents access to the 19 kHz signal, then the oscillator frequency must be measured directly. A test point should be obtained by modifying the oscillator RC network as in *Figure 7*.

The output is a pulse train of approximately 1.5V amplitude. Connecting frequency counters of up to 300 pF input capacitance produces less than 0.3% change of the oscillator frequency, which should be set to 228 kHz.

High Loop Gain Components

For applications demanding operation under low pilot level (e.g. car radio) the following component changes to *Figure 1* are recommended.

R1 = 12k	C3 = 150 pF
R2 = 1.5k	C4 = 330 nF
R8 = 330	C5 = 150 nF
P1 = 10k	

External Mono-Stereo Switching and Oscillator Killing

If required the LM4500A can be forced into mono mode simply by grounding pin 9 (see *Figure 1*). The 228 kHz oscillator will be automatically stopped.

The conditions governing mono/stereo switching on pin 9 are the following:

Quiescent voltage: + 2.3 V_{DC}

Current required to ensure mono operation (with 100 mVrms pilot level): 10 μA (from pin 9 to ground)

Hysteresis: 0.7 μA

Stereo/mono switching & oscillator killing: less than + 500 mV

Maximum stray capacitance between pin 9 and ground: 100 pF

External Component Functions

P1 19 kHz frequency adjustment

P2 Channel separation adjustment and compensation for IF roll-off.

R3, R6 Gain fixing resistors. The values shown in the schematic are for unity gain.

C6, C7 De-emphasis capacitors. Value to give: RC = 50 μs.

LM13600/LM13600A/LM11600A

National Semiconductor

LM13600/LM13600A/LM11600A Dual Operational Transconductance Amplifiers With Linearizing Diodes and Buffers

General Description

The LM13600 series consists of two current controlled transconductance amplifiers each with differential inputs and a push pull output. The two amplifiers share common supplies but otherwise operate independently. Linearizing diodes are provided at the inputs to reduce distortion and allow higher input levels. The results is a 10 dB signal-to-noise improvement referenced to 0.5 percent THD. Controlled impedance buffers are provided which are especially designed to complement the dynamic range of the amplifiers.

Features

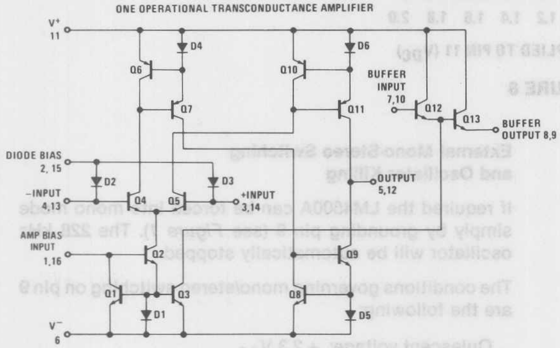
- gm adjustable over 6 decades
- Excellent gm linearity
- Excellent matching between amplifiers
- Linearizing diodes
- Controlled impedance buffers
- High output signal to noise ratio
- Wide supply range ± 2V to ± 22V.

Applications

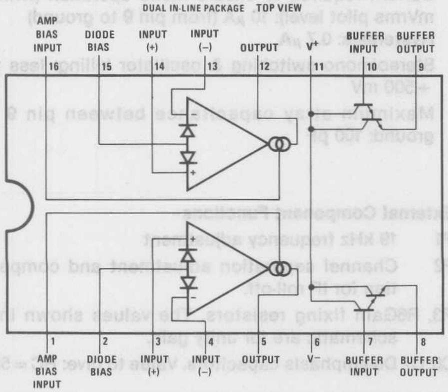
- Current controlled amplifiers
- Current controlled impedances
- Current controlled filters
- Current controlled oscillators
- Multiplexers
- Timers
- Sample and hold circuits

Schematic and Connection Diagrams

ONE OPERATIONAL TRANSCONDUCTANCE AMPLIFIER



DUAL IN-LINE PACKAGE TOP VIEW



Order Number LM13600J or LM11600AJ See NS Package J16A

Order Number LM13600N or LM13600AN See NS Package N16A

LM13600N, LM13600AN	570 mW
LM13600J, LM11600AJ	600mW
Differential Input Voltage	± 5 V
Diode Bias Current (I_D)	2 mA
Amplifier Bias Current (I_{ABC})	2 mA
Output Short Circuit Duration	Indefinite
Buffer Output Current (Note 3)	20 mA
Operating Temperature Range	
LM13600N, LM13600AN	0° C to + 70° C
LM13600J, LM11600AJ	-55° C to + 125° C
DC Input Voltage	$+V_S$ to $-V_S$
Storage Temperature Range	-65° C to + 150° C
Lead Temperature (Soldering, 10 seconds)	300° C

Electrical Characteristics (Note 4)

Parameters	Conditions	LM13600			LM13600A LM11600A			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (V_{OS})			0.4	4		0.4	1	mV
	Over Specified Temperature Range						2	mV
	I_{ABC} 5 μA		0.3	4		0.3	1	mV
V_{OS} Including Diodes	Diode Bias Current (I_D) = 500 μA		0.5	5		0.5	2	mV
Input Offset Change	5 μA ≤ I_{ABC} ≤ 500 μA		0.1	3		0.1	1	mV
Input Offset Current			0.1	0.6		0.1	0.6	μA
Input Bias Current			0.4	5		0.4	5	μA
	Over Specified Temperature Range		1	8		1	7	μA
Forward Transconductance(gm)		6700	9600	13000	7700	9600	12000	μmho
	Over specified Temp Range	5400			4000			μmho
gm Tracking			0.3			0.3		dB
Peak Output Current	RL = 0, I_{ABC} = 5 μA		5		3	5	7	μA
	RL = 0, I_{ABC} = 500 μA	350	500	650	350	500	650	μA
	RL = 0, Over Specified Temp Range	300			300			μA
Peak Output Voltage								
Positive	RL = ∞, 5 μA ≤ I_{ABC} ≤ 500 μA	+ 12	+ 14.2		+ 12	+ 14.2		V
Negative	RL = ∞, 5 μA ≤ I_{ABC} ≤ 500 μA	– 12	– 14.4		– 12	– 14.4		V
Supply Current	I_{ABC}=500μA, Both Channels		2.6			2.6		mA
V_{OS} Sensitivity								
Positive	$\triangle V_{OS}/\triangle V+$		20	150		20	150	μV/V
Negative	$\triangle V_{OS}/\triangle V-$		20	150		20	150	μV/V
CMRR		80	110		80	110		dB
Common Mode Range		± 12	± 13.5		± 12	± 13.5		V
Crosstalk	Referred to Input (Note 5) 20 Hz < f < 20 KHz		100			100		dB
Diff.Input Current	I_{ABC} = 0, Input = ± 4 V		0.02	100		0.02	10	nA
Leakage Current	I_{ABC} = 0 (Refer To Test Circuit)		0.2	100		0.2	5	nA
Input Resistance		10	26		10	26		KΩ
Open Loop Bandwith			2			2		MHz
Slew Rate	Unity Gain Compensated		50			50		V/μSec
Buff. Input Current	(Note 5, Except I_{ABC} = 0 μA)		0.2	0.4		0.2	0.4	μA
Peak Buffer Output Voltage	(Note 5)	10			10			V

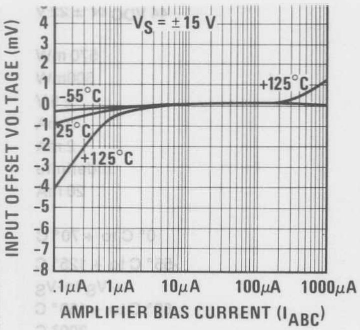
Note 1. For selections to a supply voltage above ± 22V, contact factory.

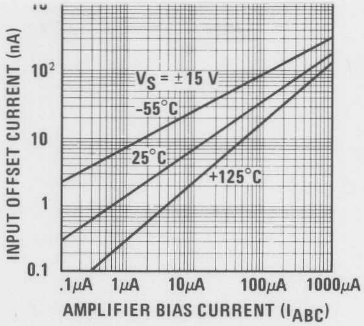
Note 2. For operating at high temperatures, the device must be derated based on a 150° C maximum junction temperature and a thermal resistance of 175° C/W which applies for the device soldered in a printed circuit board, operating in still air.

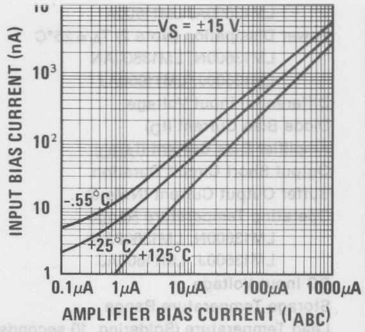
Note 3. Buffer output current should be limited so as to not exceed package dissipation.

Note 4. These specifications apply for V_S = ± 15 V, T_A = 25° C, amplifier bias current (I_{ABC}) = 500μA, pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.

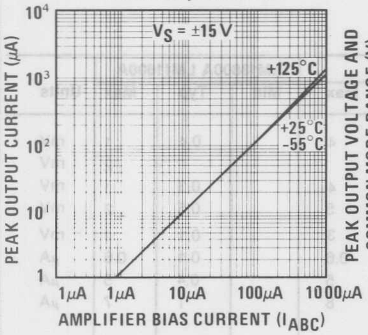
Note 5. These specifications apply for V_S = ± 15V, I_{ABC} = 500 μA, R_{OUT} = 5 KΩ connected from the buffer output to $-V_S$ and the input of the buffer is connected to the transconductance amplifier output.



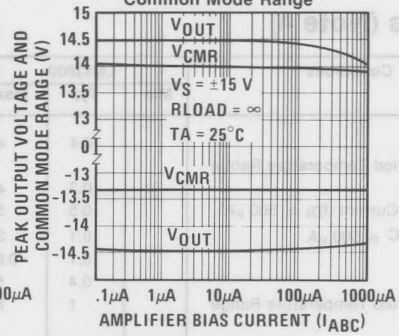




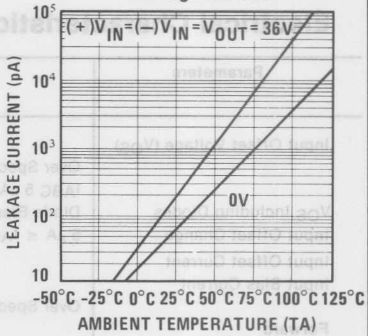
Peak Output Current



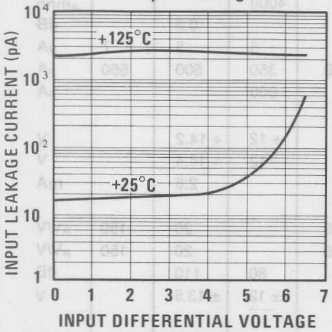
Peak Output Voltage and Common Mode Range



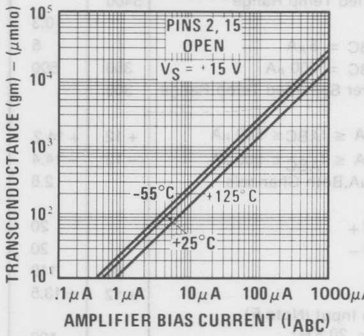
Leakage Current



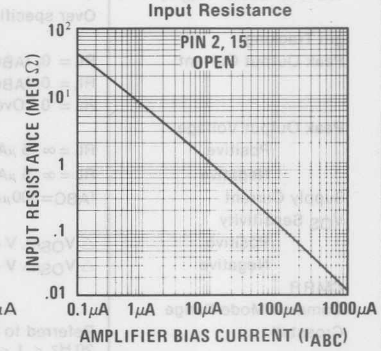
Input Leakage



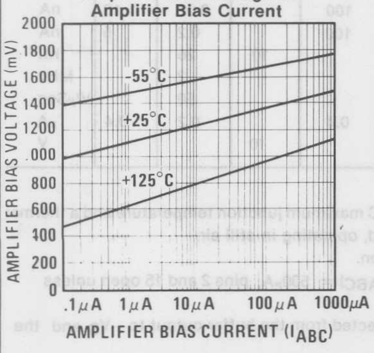
Transconductance



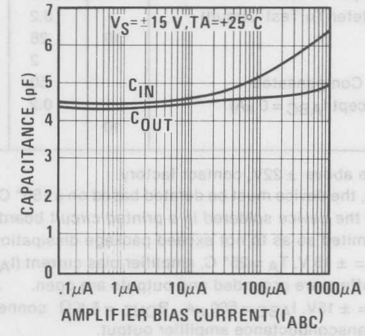
Input Resistance



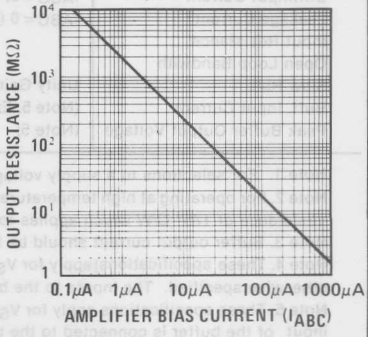
Amplifier Bias Voltage vs Amplifier Bias Current



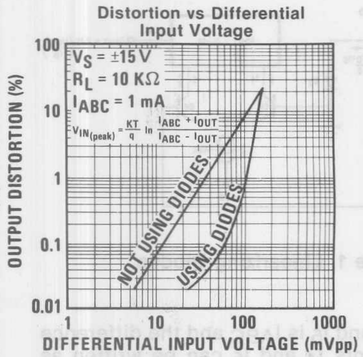
Input and Output Capacitance

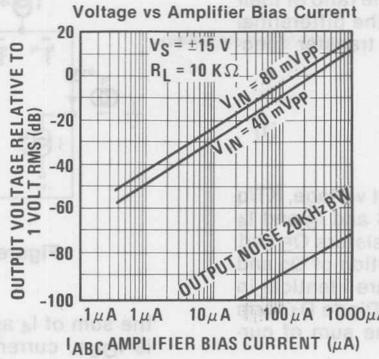


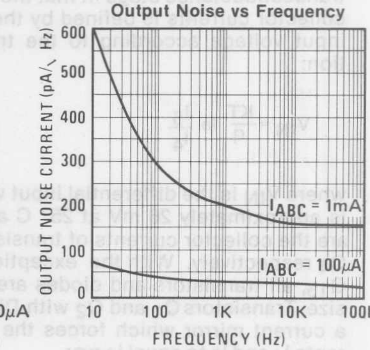
Output Resistance

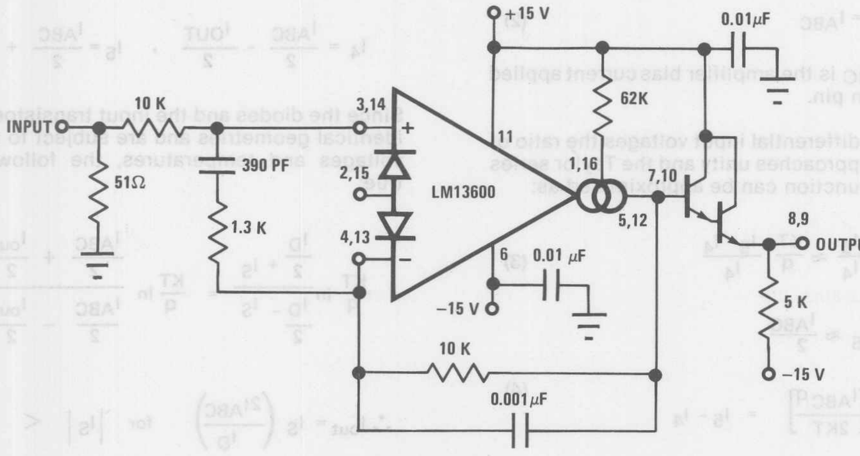


Typical Performance Characteristics (Cont'd)

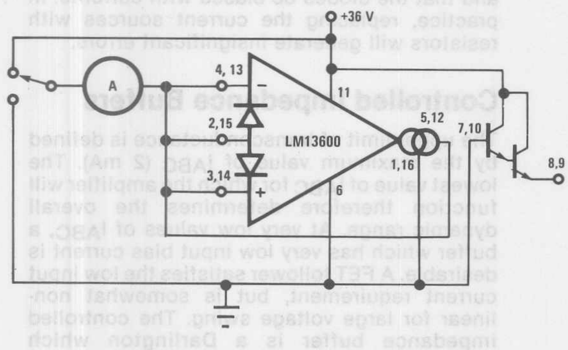




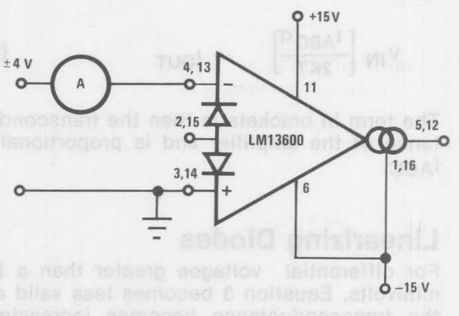




UNITY GAIN FOLLOWER



LEAKAGE CURRENT TEST CIRCUIT



DIFFERENTIAL INPUT CURRENT TEST CIRCUIT

10

Circuit Description

The differential transistor pair Q_4 and Q_5 form a transconductance stage in that the ratio of their collector currents is defined by the differential input voltage according to the transfer function:

$$V_{IN} = \frac{KT}{q} \ln \frac{I_5}{I_4} \qquad (1)$$

where V_{IN} is the differential input voltage, KT/q is approximately 26 mV at 25° C and I_5 and I_4 are the collector currents of transistors Q_5 and Q_4 respectively. With the exception of Q_3 and Q_{13}, all transistors and diodes are identical in size. Transistors Q_1 and Q_2 with Diode D_1 form a current mirror which forces the sum of currents I_4 and I_5 to equal I_{ABC};

$$I_4 + I_5 = I_{ABC} \qquad (2)$$

where I_{ABC} is the amplifier bias current applied to the gain pin.

For small differential input voltages the ratio of I_4 and I_5 approaches unity and the Taylor series of the ln function can be approximated as:

$$\frac{KT}{q} \ln \frac{I_5}{I_4} \approx \frac{KT}{q} \frac{I_5 - I_4}{I_4} \qquad (3)$$

$$I_4 \approx I_5 \approx \frac{I_{ABC}}{2}$$

$$V_{IN} \left[\frac{I_{ABC}\, q}{2KT}\right] = I_5 - I_4 \qquad (4)$$

Collector currents I_4 and I_5 are not very useful by themselves and it is necessary to subtract one current from the other. The remaining transistors and diodes form three current mirrors that produce an output current equal to I_5 minus I_4 thus:

$$V_{IN} \left[\frac{I_{ABC}\, q}{2KT}\right] = I_{OUT} \qquad (5)$$

The term in brackets is then the transconductance of the amplifier and is proportional to I_{ABC}.

Linearizing Diodes

For differential voltages greater than a few millivolts, Equation 3 becomes less valid and the transconductance becomes increasingly nonlinear. Figure 1 demonstrates how the internal diodes can linearize the transfer function of the amplifier. For convenience assume the diodes are biased with current sources and the input signal is in the form of current I_S. Since

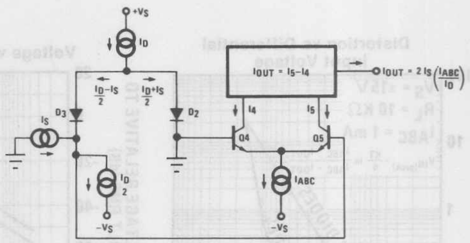


Figure 1. Linearizing Diodes

the sum of I_4 and I_5 is I_{ABC} and the difference is I_{OUT}, currents I_4 and I_5 can be written as follows:

$$I_4 = \frac{I_{ABC}}{2} - \frac{I_{OUT}}{2}, \quad I_5 = \frac{I_{ABC}}{2} + \frac{I_{OUT}}{2}$$

Since the diodes and the input transistors have identical geometries and are subject to similar voltages and temperatures, the following is true:

$$\frac{KT}{q} \ln \frac{\frac{I_D}{2} + I_S}{\frac{I_D}{2} - I_S} = \frac{KT}{q} \ln \frac{\frac{I_{ABC}}{2} + \frac{I_{out}}{2}}{\frac{I_{ABC}}{2} - \frac{I_{out}}{2}}$$

$$\therefore I_{out} = I_S \left(\frac{2 I_{ABC}}{I_D}\right) \quad \text{for} \quad |I_S| < \frac{I_D}{2} \qquad (6)$$

Notice that in deriving Equation 6 no approximations have been made and there are no temperature dependent terms. The limitations are that the signal current not exceed $I_D/2$ and that the diodes be biased with currents. In practice, replacing the current sources with resistors will generate insignificant errors.

Controlled Impedance Buffers

The upper limit of transconductance is defined by the maximum value of I_{ABC} (2 mA). The lowest value of I_{ABC} for which the amplifier will function therefore determines the overall dynamic range. At very low values of I_{ABC}, a buffer which has very low input bias current is desirable. A FET follower satisfies the low input current requirement, but is somewhat nonlinear for large voltage swing. The controlled impedance buffer is a Darlington which modifies its input bias current to suit the need. For low values of I_{ABC}, the buffer's input current is minimal. At higher levels of I_{ABC}, transistor Q_3 biases up Q_{12} with a current proportional to I_{ABC} for fast slew rate.

Applications/Voltage Controlled Amplifiers

Figure 2 shows how the linearizing diodes can be used in a voltage controlled amplifier. To understand the input biasing, it is best to consider the 13 KΩ resistor as a current source and use a Thevenin equivalent circuit as shown in Figure 3. This circuit is similar to Figure 1 and operates the same. The potentiometer in Figure 2 is adjusted to minimize the effects of the control signal at the output.

For optimum signal-to-noise performance, I_{ABC} should be as large as possible as shown by the Output Voltage vs. Amplifier Bias Current graph. Larger amplitudes of input signal also improve the S/N ratio. The linearizing diodes help here by allowing larger input signals for the same output distortion as shown by the Distortion vs. Differential Input Voltage graph. S/N may be optimized by adjusting the magnitude of the input signal via R_{IN} (Figure 2)until the output distortion is below some desired level. The output voltage swing can then be set at any level by selecting R_L.

Although the noise contribution of the linearizing diodes is negligible relative to the contribution of the amplifier's internal transistors, I_D should be as large as possible. This minimizes the dynamic junction resistance of the diodes (r_e) and maximizes their linearizing action when balanced against R_{IN}. A value of 1 mA is recommended for I_D unless the specific application demands otherwise.

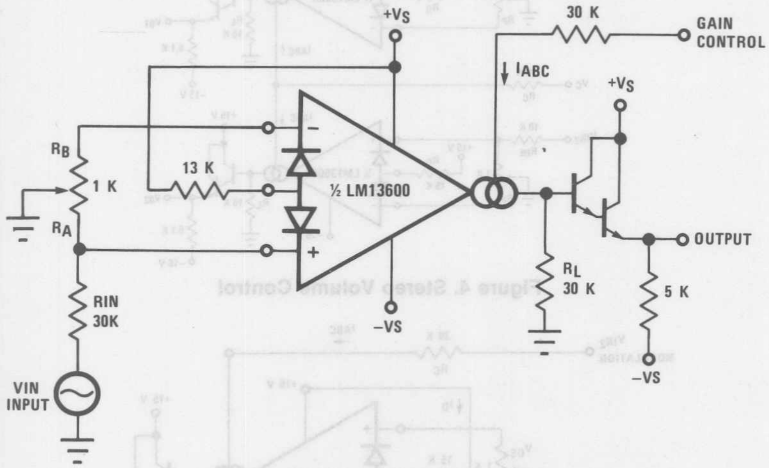


Figure. 2 Voltage Controlled Amplifier

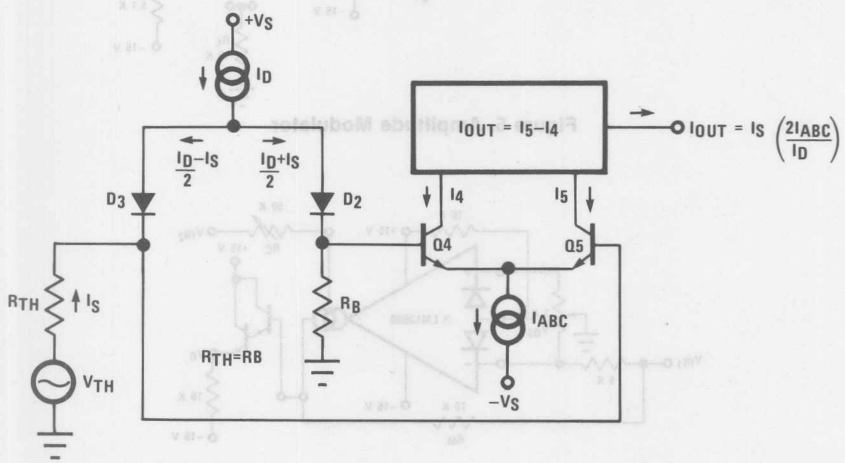


Figure 3. Equivalent VCA Input Circuit

matching of the two LM13600 amplifiers to provide a Stereo Volume Control with a typical channel-to-channel gain tracking of 0.3 dB. R_P is provided to minimize the output offset voltage and may be replaced with two 510Ω resistors in AC-coupled applications. For the component values given, amplifier gain is derived from Figure 2 as being:

$$\frac{V_O}{V_{IN}} = 940 \times I_{ABC}$$

modulator or two quadrant multiplier as shown, in Figure 5, where:

$$I_O = \frac{-2I_S}{I_D}(I_{ABC}) = \frac{-2I_S}{I_D}\frac{V_{IN2}}{R_C} - \frac{2I_S}{I_D}\frac{(V^-+1.4\ V)}{R_C}$$

The constant term in the above equation may be cancelled by feeding $I_S \times I_D R_C/2(V^-+1.4V)$ into I_O. The circuit of Figure 6 adds R_M to provide

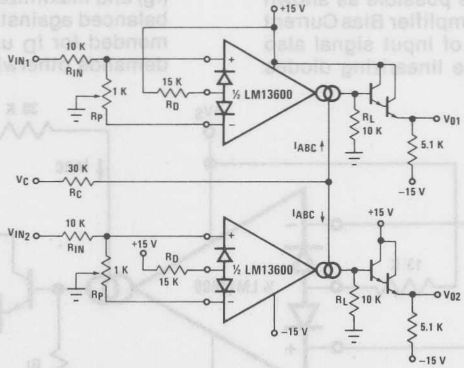


Figure 4. Stereo Volume Control

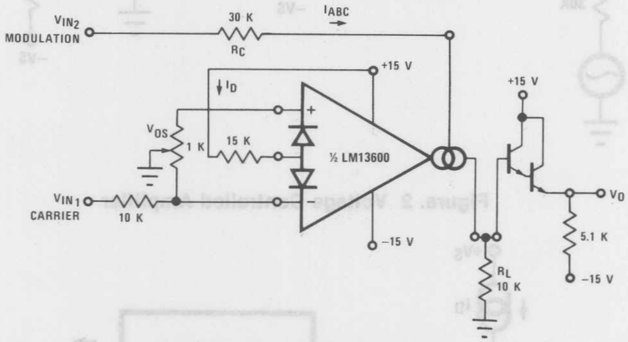


Figure 5. Amplitude Modulator

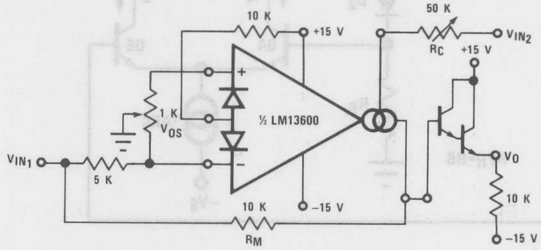


Figure 6. Four-Quadrant Multiplier

this current, resulting in a four-quadrant multiplier where R_C is trimmed such that $V_O = 0V$ for $V_{IN2} = 0V$. R_M also serves as the load resistor for I_O.

Noting that the gain of the LM13600 amplifier of Figure 3 may be controlled by varying the linearizing diode current I_D as well as by varying I_{ABC}, Figure 7 shows an AGC Amplifier using this approach. As V_O reaches a high enough amplitude ($3V_{BE}$) to turn on the Darlington transistors and the linearizing diodes, the increase in I_D reduces the amplifier gain so as to hold V_O at that level.

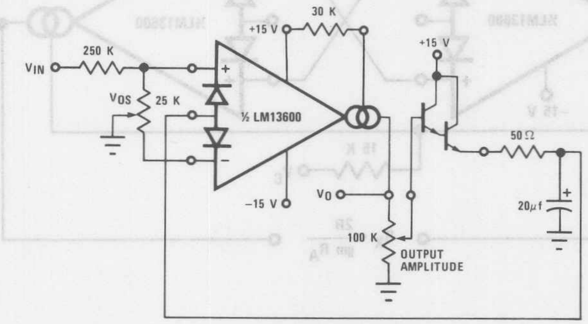
Voltage Controlled Resistors

An Operational Transconductance Amplifier (OTA) may be used to implement a Voltage Controlled Resistor as shown in Figure 8. A signal voltage applied at R_X generates a V_{IN} to the LM13600 which is then multiplied by the gm of the amplifier to produce an output current, thus:

$$R_X = \frac{R + R_A}{gmR_A}$$

where gm ≈ $19.2I_{ABC}$ at 25°C. Note that the attenuation of V_O by R and R_A is necessary to maintain V_{IN} within the linear range of the LM13600 input.

Figure 9 shows a similar VCR where the linearizing diodes are added, essentially improving the noise performance of the resistor. A floating VCR



7. AGC Amplifier

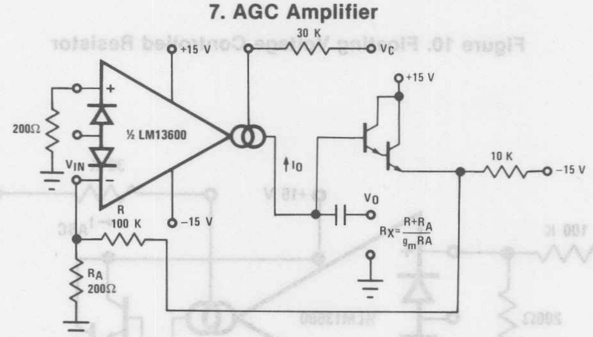


Figure 8. Voltage Controlled Resistor, Single-Ended

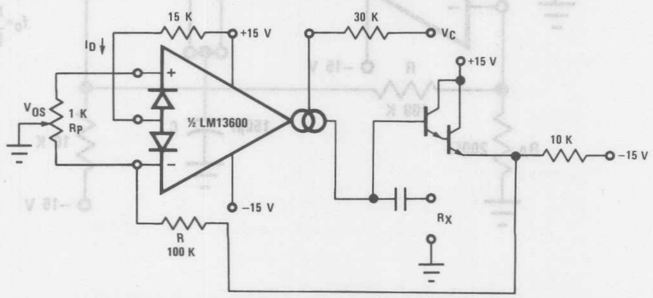


Figure 9. Voltage Controlled Resistor With Linearizing Diodes

is shown in Figure 10, where each "end" of the "resistor" may be at any voltage within the output voltage range of the LM13600.

Voltage Controlled Filters

OTA's are extremely useful for implementing voltage controlled filters, with the LM13600 having the advantage that the required buffers are included on the I.C. The VC Lo-Pass Filter of Figure 11 performs as a unity-gain buffer amplifier at frequencies below cut-off, with the cut-off frequency being the point at which X_C/gm equals the closed-loop gain of (R/R_A). At frequencies above cut-off the circuit provides a single RC roll-off (6 dB per octave) of the input signal amplitude with a -3 dB point defined by the given equation,

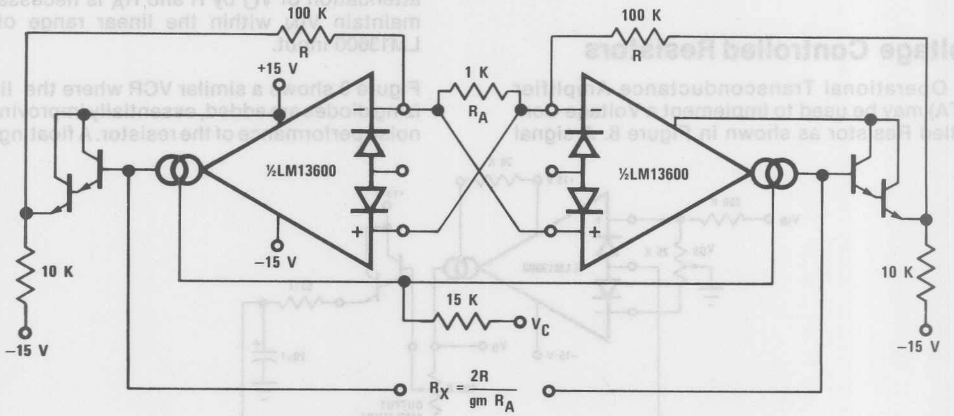


Figure 10. Floating Voltage Controlled Resistor

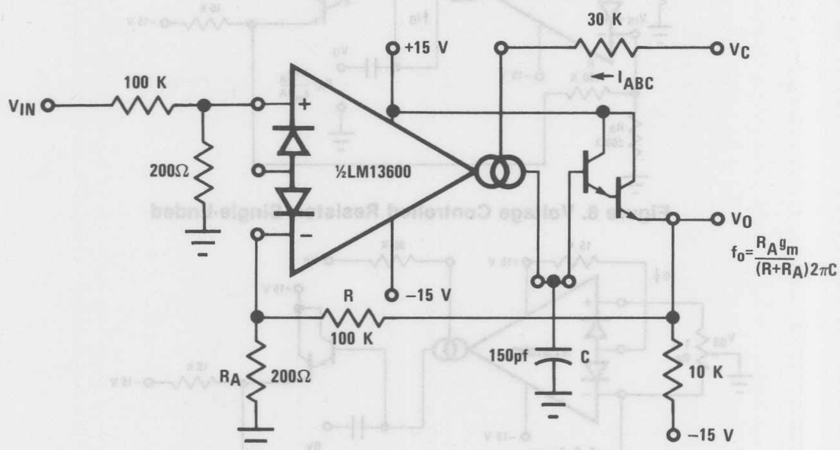


Figure 11. Voltage Controlled Low-Pass Filter

where gm is again 19.2 x I_{ABC} at room temperature. Figure 12 shows a VC High-Pass Filter which operates in much the same manner, providing a single RC roll-off below the defined cut-off frequency.

Additional amplifiers may be used to implement higher order filters as demonstrated by the two-pole Butterworth Lo-Pass Filter of Figure 13 and the state variable filter of Figure 14. Due to the excellent gm tracking of the two amplifiers and the varied bias of the buffer Darlingtons, these filters perform well over several decades of frequency.

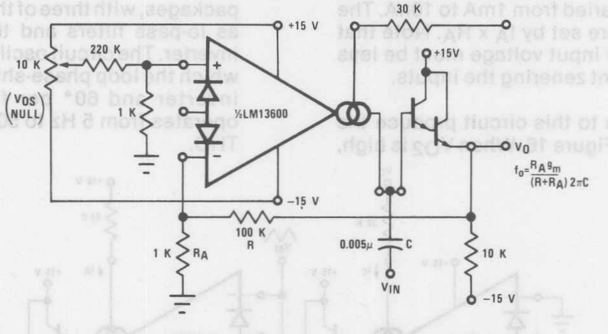


Figure 12. Voltage Controlled Hi-Pass Filter

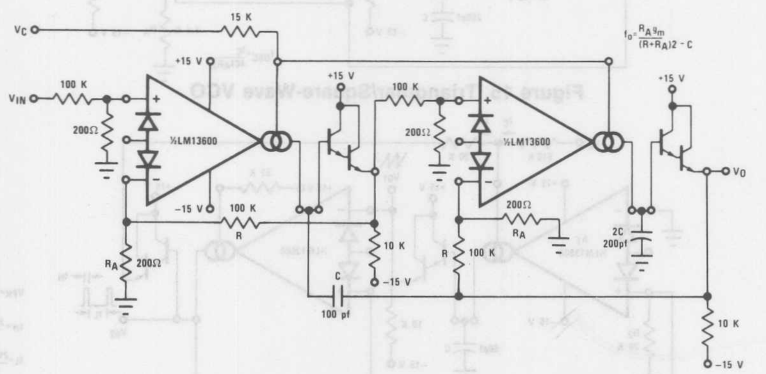


Figure 13. Voltage Controlled 2-pole Butterworth Lo-Pass Filter

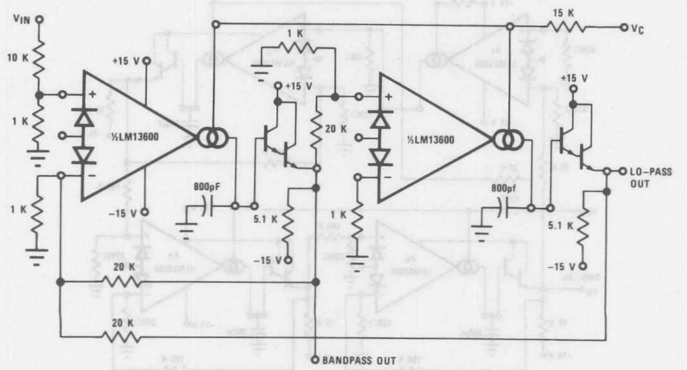


Figure 14. Voltage Controlled State Variable Filter

Oscillators which may be built utilizing the LM13600. With the component values shown, this oscillator provides signals from 200 kHz to below 2 Hz as I_C is varied from 1mA to 10nA. The output amplitudes are set by $I_A \times R_A$. Note that the peak differential input voltage must be less than 5 volts to prevent zenering the inputs.

A few modifications to this circuit produce the ramp/pulse VCO of Figure 16. When V_{O2} is high, I_F is added to I_C to increase amplifier A1's bias current and thus to increase the charging rate of capacitor C. When V_{O2} is low, I_F goes to zero and the capacitor discharge current is set by I_C.

The VC Lo-Pass Filter of Figure 11 may be used to produce a high-quality sinusoidal VCO. The circuit of Figure 16 employs two LM13600 packages, with three of the amplifiers configured as lo-pass filters and the fourth as a limiter/-inverter. The circuit oscillates at the frequency at which the loop phase-shift is 360° or 180° for the inverter and 60° per filter stage. This VCO operates from 5 Hz to 50 kHz with less than 1% THD.

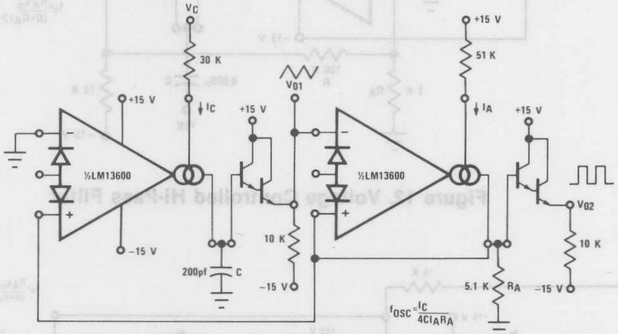


Figure 15. Triangular/Square-Wave VCO

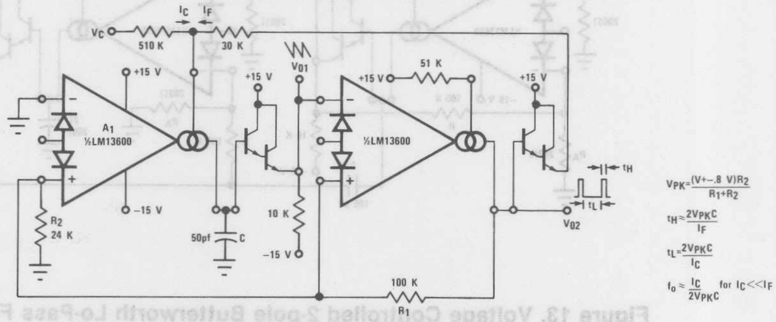


Figure 16. Ramp/Pulse VCO

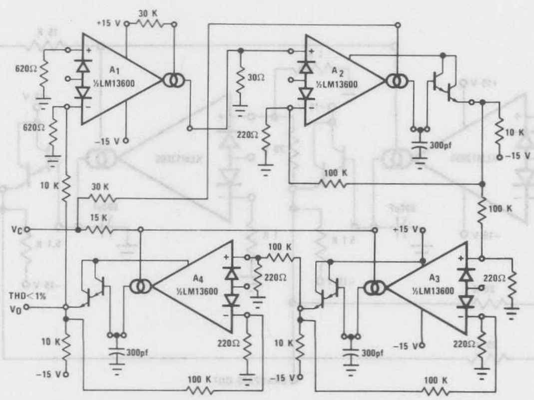


Figure 17. Sinusoidal VCO

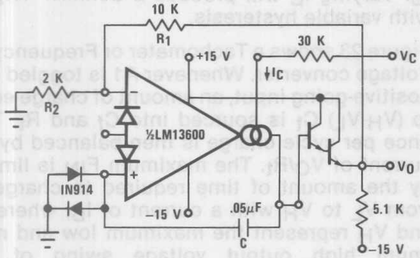


Figure 18. Single Amplifier VCO

Figure 18 shows how to build a VCO using one amplifier when the other amplifier is needed for another function.

Additional Applications

Figure 19 presents an interesting one-shot which draws no power supply current until it is triggered. A positive-going trigger pulse of at least 2V amplitude turns on the amplifier through R_B and pulls the non-inverting input high. The amplifier regenerates and latches its output high until capacitor C charges to the voltage level on the non-inverting input. The output then switches low, turning off the amplifier and discharging the capacitor. The capacitor discharge rate is speeded up by shorting the diode bias pin to the inverting input so that an additional discharge current flows through D_I when the amplifier output switches low. A special feature of this timer is that the other amplifier, when biased from V_O, can perform another function and draw zero stand-by power as well.

The operation of the multiplexer of Figure 20 is very straightforward. When A1 is turned on it holds V_O equal to V_{IN1} and when A2 is supplied with bias current then it controls V_O. C_C and R_C serve to stabilize the unity-gain

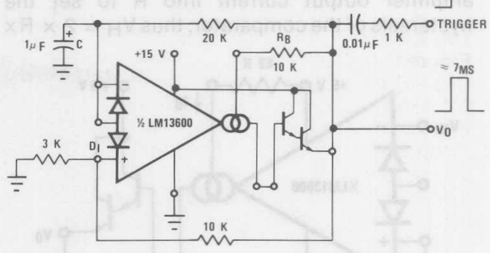


Figure 19. Zero Stand-by Power Timer

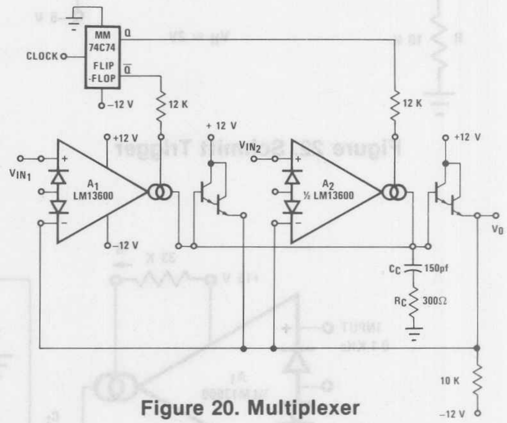


Figure 20. Multiplexer

configuration of amplifiers A1 and A2. The maximum clock rate is limited to about 200 KHz by the LM13600 slew rate into 150 pF when the $(V_{IN1}\text{-}V_{IN2})$ differential is at its maximum allowable value of 5 volts.

The Phase-Locked Loop of Figure 21 uses the four-quadrant multiplier of Figure 6 and the V_{CO} of Figure 18 to produce a PLL with a ± 5% hold-in range and an input sensitivity of about 300 mV.

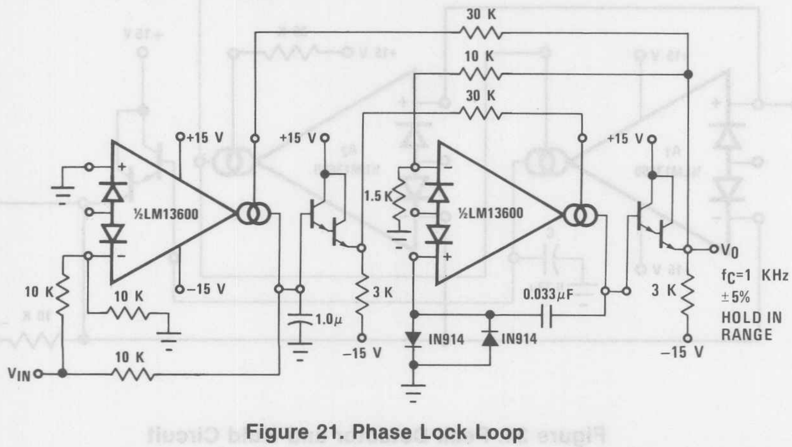


Figure 21. Phase Lock Loop

The Schmitt Trigger of Figure 22 uses the amplifier output current into R to set the hysteresis of the comparator; thus $V_H = 2 \times R \times I_B$. Varying I_B will produce a Schmitt Trigger with variable hysteresis.

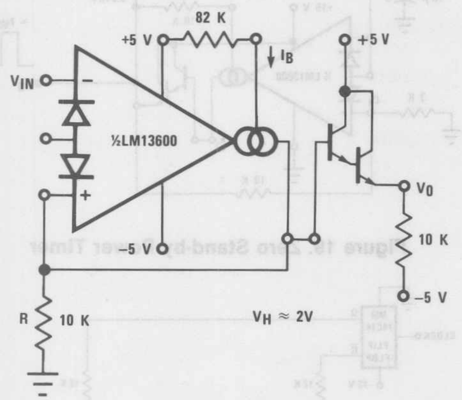


Figure 22. Schmitt Trigger

Figure 23 shows a Tachometer or Frequency-to-Voltage converter. Whenever A1 is toggled by a positive-going input, an amount of charge equal to $(V_H\text{-}V_L)$ C_t is sourced into C_f and R_t. This once per cycle charge is then balanced by the current of V_O/R_t. The maximum F_{IN} is limited by the amount of time required to charge C_t from V_L to V_H with a current of I_B, where V_L and V_H represent the maximum low and maximum high output voltage swing of the LM13600. D1 is added to provide a discharge path for C_t when A1 switches low.

The Peak Detector of Figure 24 uses A2 to turn on A1 whenever V_{IN} becomes more positive than V_O. A1 then charges storage capacitor C to hold V_O equal to $V_{IN}PK$. One precaution to observe when using this circuit: the Darlington transistor used must be on the same side of the package as A2 since the A1 Darlington will be turned on and off with A1. Pulling the output of A2 low through D1 serves to turn off A1 so that V_O remains constant.

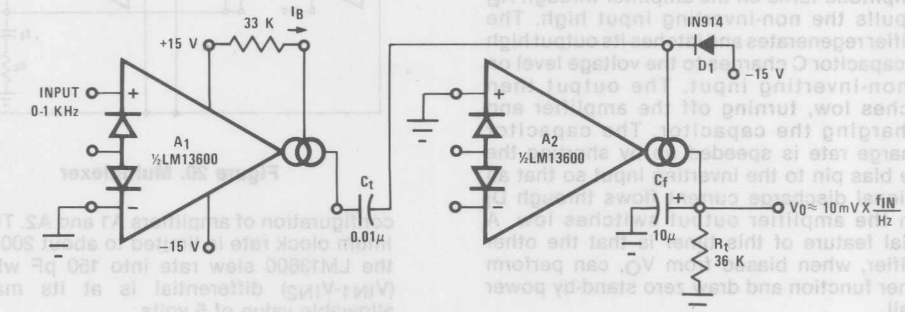


Figure 23. Tachometer

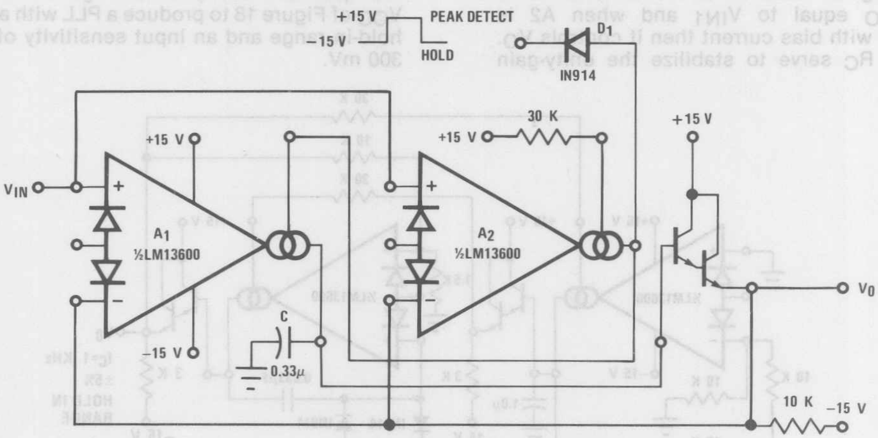


Figure 24. Peak Detector and Hold Circuit

The Sample-Hold circuit of Figure 25 also requires that the Darlington buffer used be from the other (A2) half of the package and that the corresponding amplifier be biased on continuously.

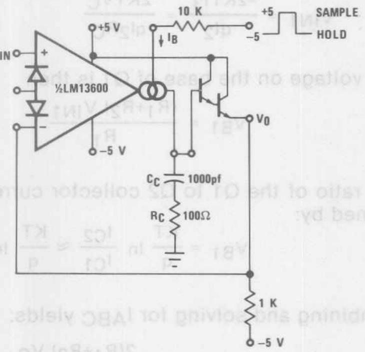


Figure 25. Sample-Hold Circuit

The Ramp-and-Hold of Figure 26 sources I_B into capacitor C whenever the input to A1 is brought high, giving a ramp-rate of about IV/ms for the component values shown.

The true RMS converter of Figure 27 is essentially an automatic gain control amplifier which adjusts its gain such that the AC power at the output of amplifier A1 is constant. The output power of amplifier A1 is monitored by squaring amplifier A2 and the average compared to a reference voltage with amplifier A3. The output of A3 provides bias current to the diodes of A1 to attenuate the input signal. Because the output power of A1 is held constant, the RMS value is constant and the attentuation is directly proportional to the RMS value of the input voltage. The attenuation is also proportional to the diode bias current. Amplifier A4 adjusts the ratio of currents through the diodes to be equal and therefore the voltage at the output of A4 is proportional to the RMS value of the input voltage. The calibration potentiometer is set such that V_O reads directly in RMS volts.

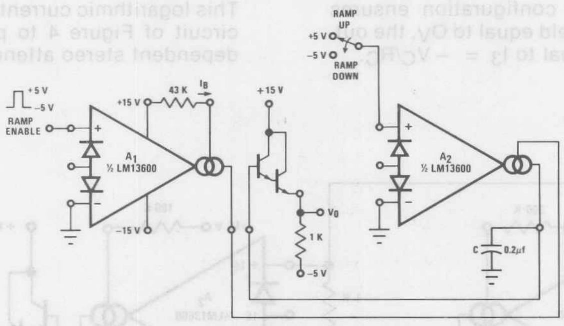


Figure 26. Ramp and Hold

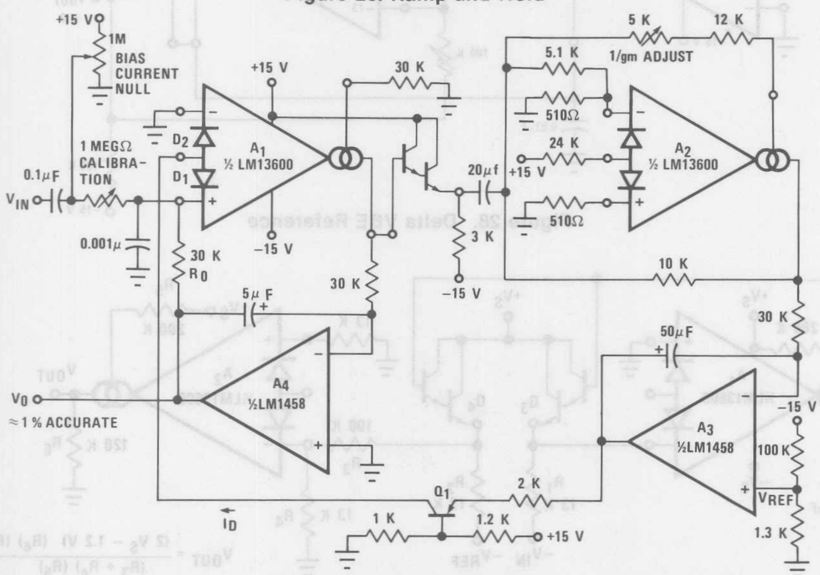


Figure 27. True RMS Converter

has a positive TC above 1.2 volts, zero TC at about 1.2 volts and negative TC below 1.2 volts. This is accomplished by balancing the TC of the A2 transfer function against the complementary TC of D1.

The log amplifier of Figure 29 responds to the ratio of current through buffer transistors Q3 and Q4. Zero temperature dependence for V_{OUT} is ensured in that the TC of the A2 transfer function is equal and opposite to the TC of the logging transistors Q3 and Q4.

The wide dynamic range of the LM13600 allows easy control of the output pulse width in the Pulse Width Modulator of Figure 30.

For generating I_{ABC} over a range of 4 to 6 decades of current, the system of Figure 31 provides a logarithmic current out for a linear voltage in.

Since the closed-loop configuration ensures that the input to A2 is held equal to O_V, the output current of A1 is equal to $I_3 = -V_C/R_C$.

range. From equation (5), the input voltage to A1 is:

$$V_{IN1} = \frac{-2KTI_3}{qI_2} = \frac{2KTV_C}{qI_2R_C}$$

The voltage on the base of Q1 is then

$$V_{B1} = \frac{(R_1+R_2)\,V_{IN1}}{R_1}$$

The ratio of the Q1 to Q2 collector currents is defined by:

$$V_{B1} = \frac{KT}{q}\ln\frac{I_{C2}}{I_{C1}} \approx \frac{KT}{q}\ln\frac{I_{ABC}}{I_1}$$

Combining and solving for I_{ABC} yields:

$$I_{ABC} = I_1 e^{\frac{2(R_1+R_2)\,V_C}{R_1 I_2 R_C}}$$

This logarithmic current can be used to bias the circuit of Figure 4 to provide temperature independent stereo attenuation characteristic.

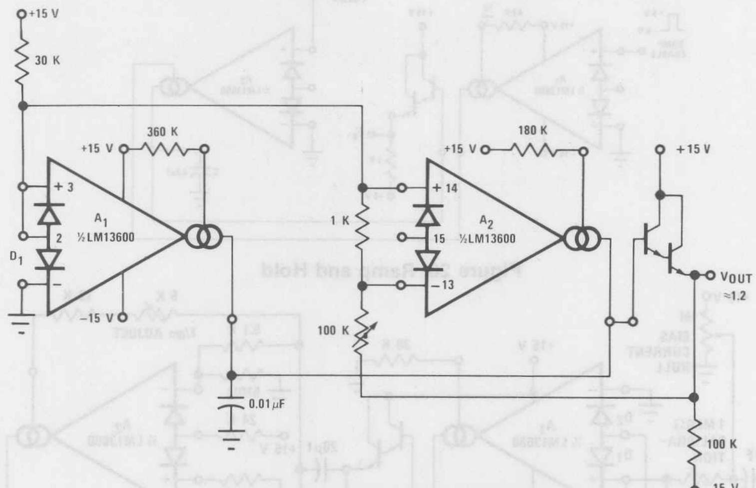
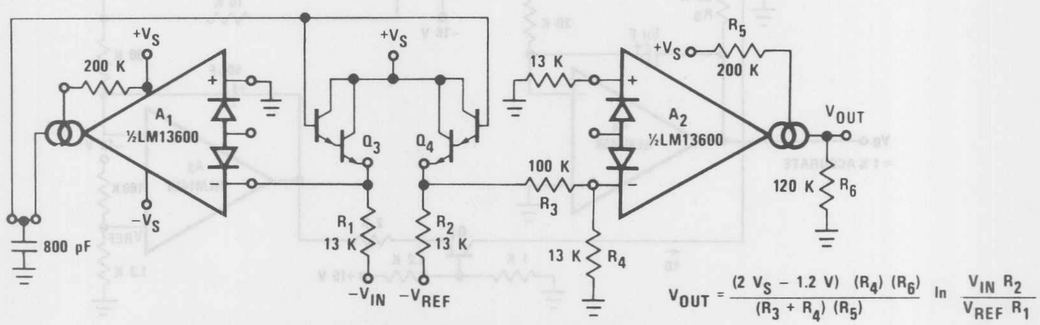


Figure 28. Delta VBE Reference



$$V_{OUT} = \frac{(2\,V_S - 1.2\ V)\ (R_4)\ (R_6)}{(R_3 + R_4)\ (R_5)}\ \ln\ \frac{V_{IN}\ R_2}{V_{REF}\ R_1}$$

Figure 29. Log Amplifier

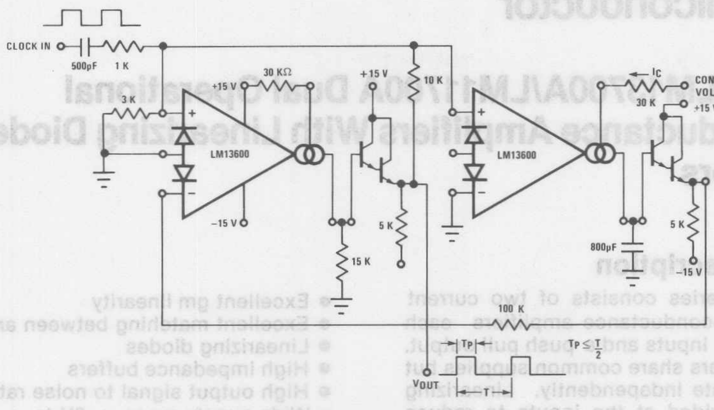


Figure 30. Pulse Width Modulator

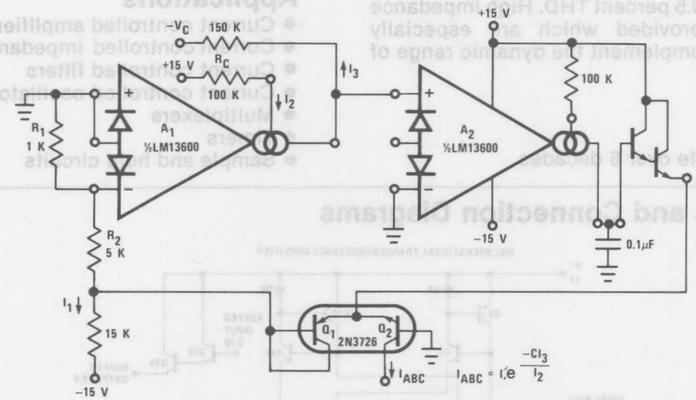


Figure 31. Logarithmic Current Source

National Semiconductor

Audio/Radio Circuits

LM13700/LM13700A/LM11700A Dual Operational Transconductance Amplifiers With Linearizing Diodes and Buffers

General Description

The LM13700 series consists of two current controlled transconductance amplifiers each with differential inputs and a push pull output. The two amplifiers share common supplies but otherwise operate independently. Linearizing diodes are provided at the inputs to reduce distortion and allow higher input levels. The results is a 10 dB signal-to-noise improvement referenced to 0.5 percent THD. High impedance buffers are provided which are especially designed to complement the dynamic range of the amplifiers.

Features

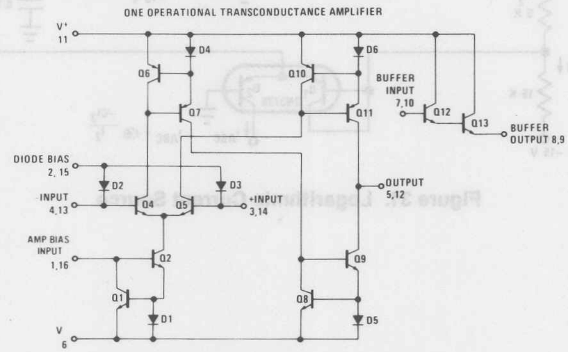
- gm adjustable over 6 decades
- Excellent gm linearity
- Excellent matching between amplifiers
- Linearizing diodes
- High impedance buffers
- High output signal to noise ratio
- Wide supply range ± 2V to ± 22V.

Applications

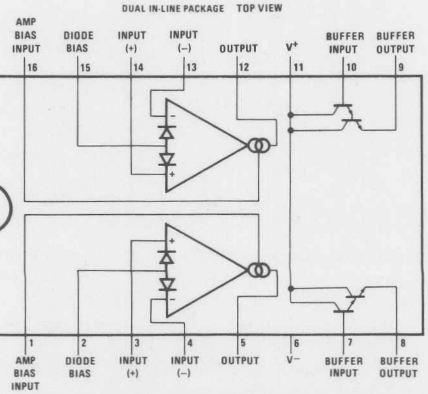
- Current controlled amplifiers
- Current controlled impedances
- Current controlled filters
- Current controlled oscillators
- Multiplexers
- Timers
- Sample and hold circuits

Schematic and Connection Diagrams

ONE OPERATIONAL TRANSCONDUCTANCE AMPLIFIER



DUAL IN-LINE PACKAGE TOP VIEW



Order Number LM13700J or LM11700AJ See NS Package J16A

Order Number LM13700N or LM13700AN See NS Package N16A

Absolute Maximum Ratings

Supply Voltage (Note 1)	
LM13700	36 V_{DC} or ± 18 V
LM13700A, LM11700A	44 V_{DC} or ± 22 V
Power Dissipation (Note 2) $T_A = 25°C$	
LM13700N, LM13700AN	570 mW
LM13700J, LM11700AJ	600mW
Differential Input Voltage	± 5 V
Diode Bias Current (I_D)	2 mA
Amplifier Bias Current (I_{ABC})	2 mA
Output Short Circuit Duration	Indefinite
Buffer Output Current (Note 3)	20 mA
Operating Temperature Range	
LM13700N, LM13700AN	0° C to + 70° C
LM13700J , LM11700AJ	-55° C to + 125° C
DC Input Voltage	+ V_S to -V_S
Storage Temperature Range	-65° C to + 150° C
Lead Temperature (Soldering, 10 Seconds)	300° C

Electrical Characteristics (Note 4)

Parameters	Conditions	LM13700			LM13700A LM11700A			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (V_{OS})			0.4	4		0.4	1	mV
	Over Specified Temperature Range						2	mV
	I_{ABC} 5 μA		0.3	4		0.3	1	mV
V_{OS} Including Diodes	Diode Bias Current (I_D) = 500 μA		0.5	5		0.5	2	mV
Input Offset Change	5 μA ≤ I_{ABC} ≤ 500 μA		0.1	3		0.1	1	mV
Input Offset Current			0.1	0.6		0.1	0.6	μA
Input Bias Current			0.4	5		0.4	5	μA
	Over Specified Temperature Range		1	8		1	7	μA
Forward Transconductance(gm)		6700	9600	13000	7700	9600	12000	μmho
	Over specified Temp Range	5400			4000			μmho
gm Tracking			0.3			0.3		dB
Peak Output Current	RL = 0, I_{ABC} = 5μA		5		3	5	7	μA
	RL = 0, I_{ABC} = 500 μA	350	500	650	350	500	650	μA
	RL = 0, Over Specified Temp Range	300			300			μA
Peak Output Voltage								
Positive	RL = ∞, 5 μA ≤ I_{ABC} ≤ 500 μA	+ 12	+ 14.2		+ 12	+ 14.2		V
Negative	RL = ∞, 5 μA ≤ I_{ABC} ≤ 500 μA	− 12	− 14.4		− 12	− 14.4		V
Supply Current	I_{ABC}=500μA,Both Channels		2.6			2.6		mA
V_{OS} Sensitivity								
Positive	$\Delta V_{OS}/\Delta V+$		20	150		20	150	μV/V
Negative	$\Delta V_{OS}/\Delta V-$		20	150		20	150	μV/V
CMRR		80	110		80	110		dB
Common Mode Range		± 12	± 13.5		± 12	± 13.5		V
Crosstalk	Referred to Input (Note 5) 20 Hz < f < 20 KHz		100			100		dB
Diff.Input Current	I_{ABC} = 0, Input = ± 4 V		0.02	100		0.02	10	nA
Leakage Current	I_{ABC} = 0 (Refer To Test Circuit)		0.2	100		0.2	5	nA
Input Resistance		10	26		10	26		KΩ
Open Loop Bandwith			2			2		MHz
Slew Rate	Unity Gain Compensated		50			50		V/μSec
Buff. Input Current	(Note 5)		0.5	2		0.5	2	μA
Peak Buffer Output Voltage	(Note 5)	10			10			V

Note 1. For selections to a supply voltage above ± 22V, contact factory.

Note 2. For operating at high temperatures, the device must be derated based on a 150° C maximum junction temperature and a thermal resistance of 175° C/W which applies for the device soldered in a printed circuit board, operating in still air.

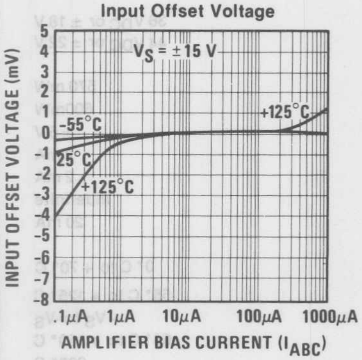
Note 3. Buffer output current should be limited so as to not exceed package dissipation.

Note 4. These specifications apply for V_S = ± 15 V, T_A = 25° C, amplifier bias current (I_{ABC}) = 500μA, pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.

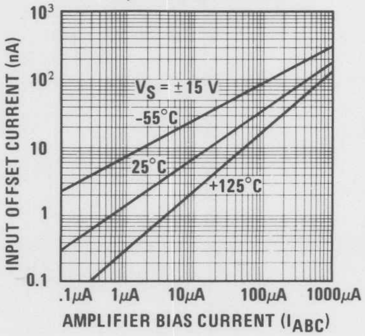
Note 5. These specifications apply for V_S = ± 15V, I_{ABC} = 500 μA, R_{OUT} = 5 KΩ connected from the buffer output to − V_S and the input of the buffer is connected to the transconductance amplifier output.

Typical Performance Characteristics

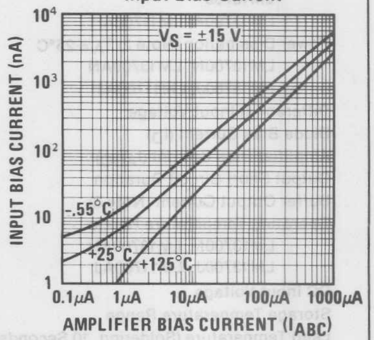
Input Offset Voltage



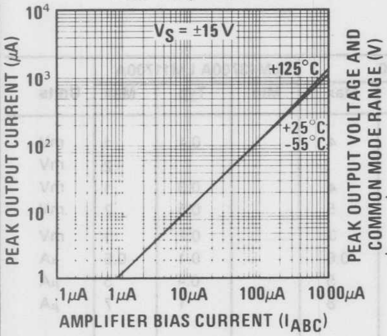
Input Offset Current



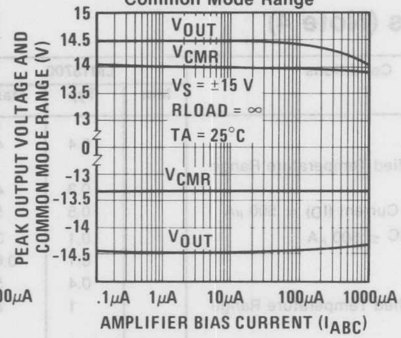
Input Bias Current



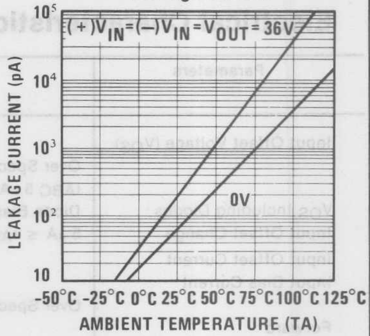
Peak Output Current



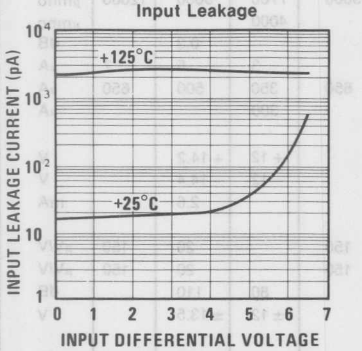
Peak Output Voltage and Common Mode Range



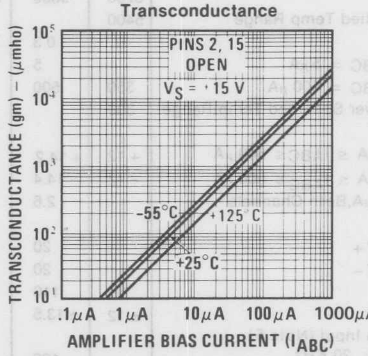
Leakage Current



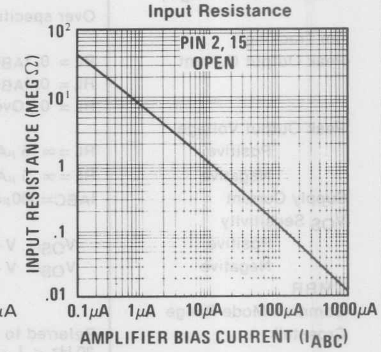
Input Leakage



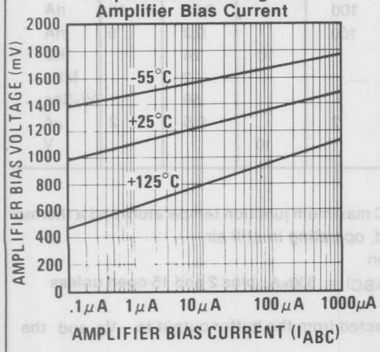
Transconductance



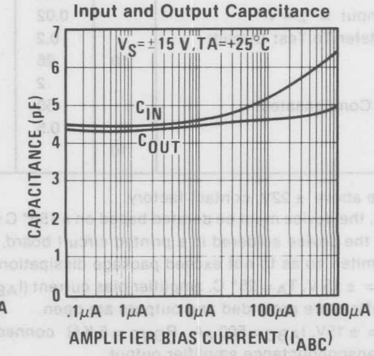
Input Resistance



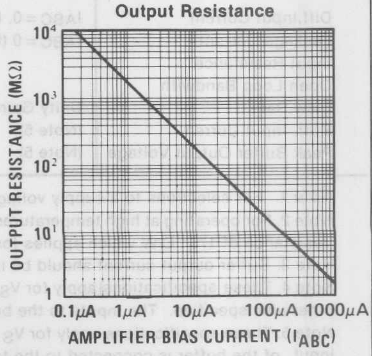
Amplifier Bias Voltage vs Amplifier Bias Current



Input and Output Capacitance

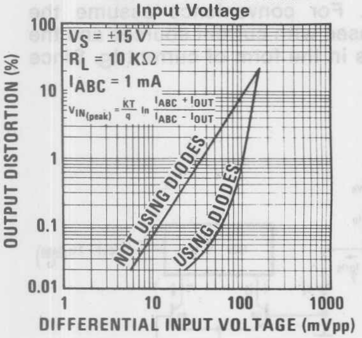


Output Resistance

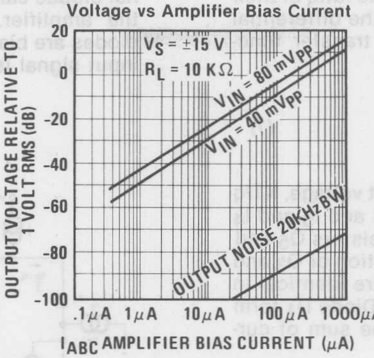


Typical Performance Characteristics (Cont'd)

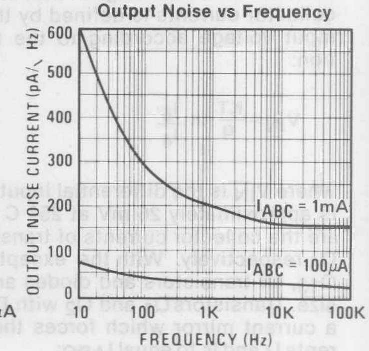
Distortion vs Differential Input Voltage

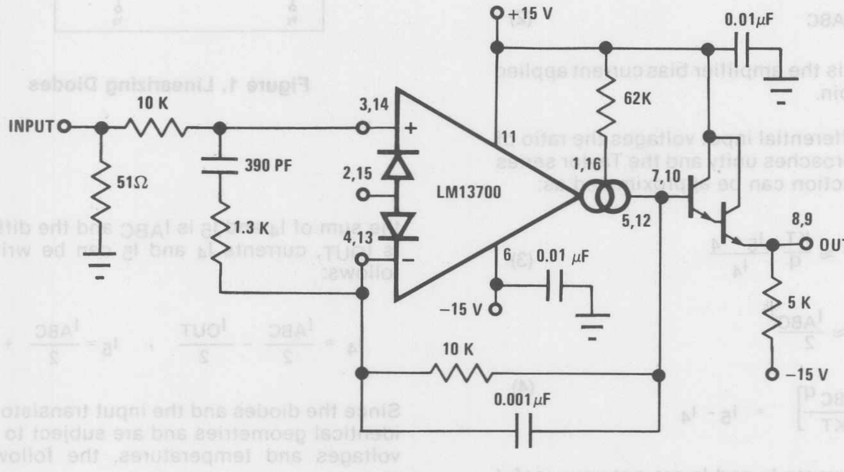


Voltage vs Amplifier Bias Current

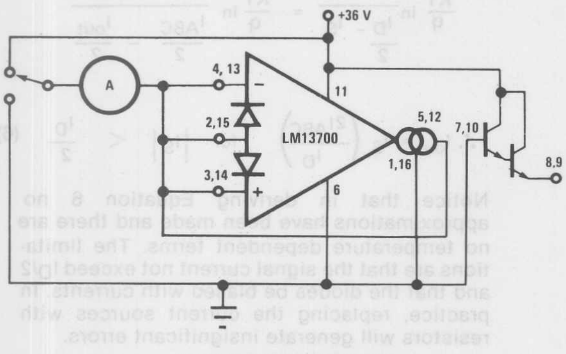


Output Noise vs Frequency

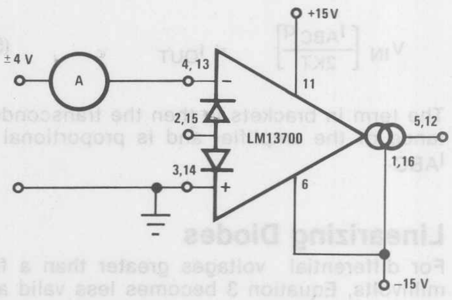




UNITY GAIN FOLLOWER



LEAKAGE CURRENT TEST CIRCUIT



DIFFERENTIAL INPUT CURRENT TEST CIRCUIT

10

Circuit Description

The differential transistor pair Q_4 and Q_5 form a transconductance stage in that the ratio of their collector currents is defined by the differential input voltage according to the transfer function:

$$V_{IN} = \frac{KT}{q} \ln \frac{I_5}{I_4} \tag{1}$$

where V_{IN} is the differential input voltage, KT/q is approximately 26 mV at 25° C and I_5 and I_4 are the collector currents of transistors Q_5 and Q_4 respectively. With the exception of Q_3 and Q_{13}, all transistors and diodes are identical in size. Transistors Q_1 and Q_2 with Diode D_1 form a current mirror which forces the sum of currents I_4 and I_5 to equal I_{ABC};

$$I_4 + I_5 = I_{ABC} \tag{2}$$

where I_{ABC} is the amplifier bias current applied to the gain pin.

For small differential input voltages the ratio of I_4 and I_5 approaches unity and the Taylor series of the ln function can be approximated as:

$$\frac{KT}{q} \ln \frac{I_5}{I_4} \approx \frac{KT}{q} \frac{I_5 - I_4}{I_4} \tag{3}$$

$$I_4 \approx I_5 \approx \frac{I_{ABC}}{2}$$

$$V_{IN} \left[\frac{I_{ABC}\, q}{2KT}\right] = I_5 - I_4 \tag{4}$$

Collector currents I_4 and I_5 are not very useful by themselves and it is necessary to subtract one current from the other. The remaining transistors and diodes form three current mirrors that produce an output current equal to I_5 minus I_4 thus:

$$V_{IN} \left[\frac{I_{ABC}\, q}{2KT}\right] = I_{OUT} \tag{5}$$

The term in brackets is then the transconductance of the amplifier and is proportional to I_{ABC}.

Linearizing Diodes

For differential voltages greater than a few millivolts, Equation 3 becomes less valid and the transconductance becomes increasingly nonlinear. Figure 1 demonstrates how the internal diodes can linearize the transfer function of the amplifier. For convenience assume the diodes are biased with current sources and the input signal is in the form of current I_S. Since

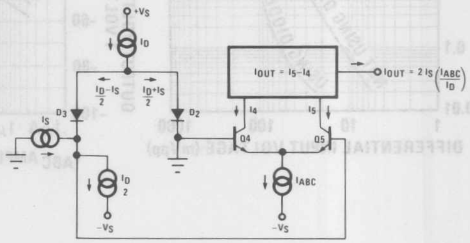


Figure 1. Linearizing Diodes

the sum of I_4 and I_5 is I_{ABC} and the difference is I_{OUT}, currents I_4 and I_5 can be written as follows:

$$I_4 = \frac{I_{ABC}}{2} - \frac{I_{OUT}}{2}, \quad I_5 = \frac{I_{ABC}}{2} + \frac{I_{OUT}}{2}$$

Since the diodes and the input transistors have identical geometries and are subject to similar voltages and temperatures, the following is true:

$$\frac{KT}{q} \ln \frac{\frac{I_D}{2} + I_S}{\frac{I_D}{2} - I_S} = \frac{KT}{q} \ln \frac{\frac{I_{ABC}}{2} + \frac{I_{out}}{2}}{\frac{I_{ABC}}{2} - \frac{I_{out}}{2}}$$

$$\therefore I_{out} = I_S \left(\frac{2 I_{ABC}}{I_D}\right) \quad \text{for} \quad |I_S| < \frac{I_D}{2} \tag{6}$$

Notice that in deriving Equation 6 no approximations have been made and there are no temperature dependent terms. The limitations are that the signal current not exceed $I_D/2$ and that the diodes be biased with currents. In practice, replacing the current sources with resistors will generate insignificant errors.

Applications/Voltage Controlled Amplifiers

Figure 2 shows how the linearizing diodes can be used in a voltage controlled amplifier. To understand the input biasing, it is best to consider the 13 KΩ resistor as a current source and use a Thevenin equivalent circuit as shown in Figure 3. This circuit is similar to Figure 1 and operates the same. The potentiometer in Figure 2 is adjusted to minimize the effects of the control signal at the output.

For optimum signal-to-noise performance, I_{ABC} should be as large as possible as shown by the Output Voltage vs. Amplifier Bias Current graph. Larger amplitudes of input signal also improve the S/N ratio. The linearizing diodes help here by allowing larger input signals for the same output distortion as shown by the Distortion vs. Differential Input Voltage graph. S/N may be optimized by adjusting the magnitude of the input signal via R_{IN} (Figure 2)until the output distortion is below some desired level. The output voltage swing can then be set at any level by selecting R_L.

Although the noise contribution of the linearizing diodes is negligible relative to the contribution of the amplifier's internal transistors, I_D should be as large as possible. This minimizes the dynamic junction resistance of the diodes (r_e) and maximizes their linearizing action when balanced against R_{IN}. A value of 1 mA is recommended for I_D unless the specific application demands otherwise.

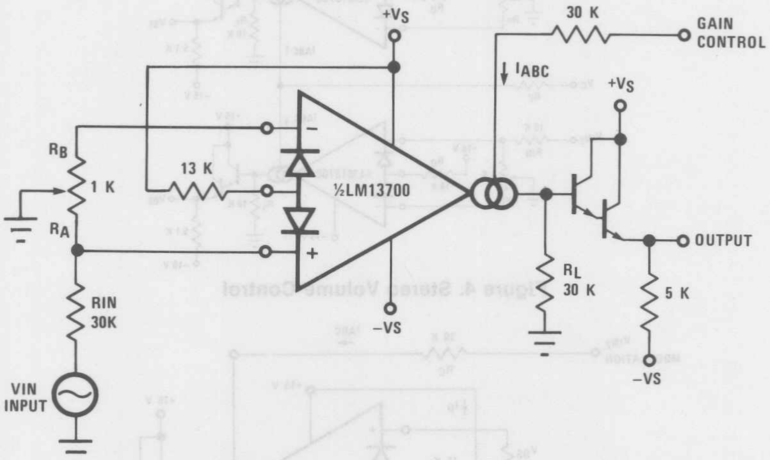


Figure. 2 Voltage Controlled Amplifier

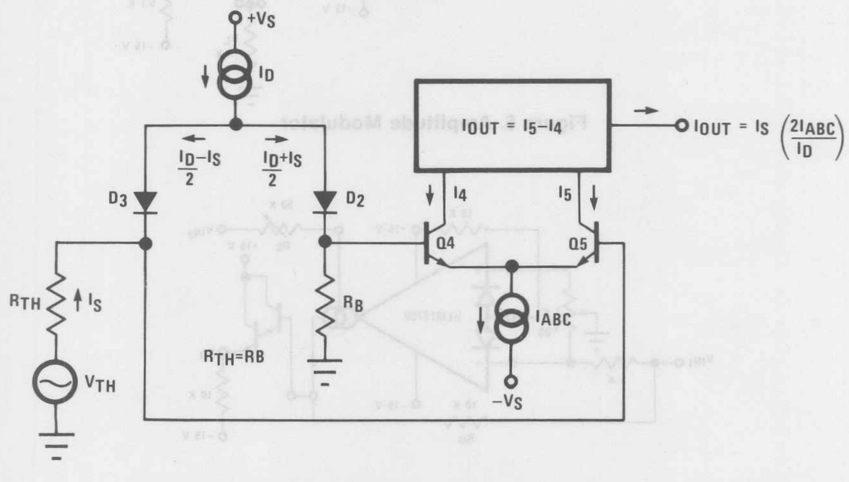


Figure 3. Equivalent VCA Input Circuit

Stereo Volume Control

The circuit of Figure 4 uses the excellent matching of the two LM13700 amplifiers to provide a Stereo Volume Control with a typical channel-to-channel gain tracking of 0.3 dB. Rp is provided to minimize the output offset voltage and may be replaced with two 510Ω resistors in AC-coupled applications. For the component values given, amplifier gain is derived from Figure 2 as being:

$$\frac{V_O}{V_{IN}} = 940 \times I_{ABC}$$

If V_C is derived from a second signal source then the circuit becomes an amplitude modulator or two-quadrant multiplier as shown in Figure 5, where:

$$I_O = \frac{-2I_S}{I_D}(I_{ABC}) = \frac{-2I_S}{I_D}\frac{V_{IN2}}{R_C} - \frac{2I_S}{I_D}\frac{(V^- + 1.4\ V)}{R_C}$$

The constant term in the above equation may be cancelled by feeding $I_S \times I_D R_C / 2(V^- + 1.4V)$ into I_O. The circuit of Figure 6 adds R_M to provide

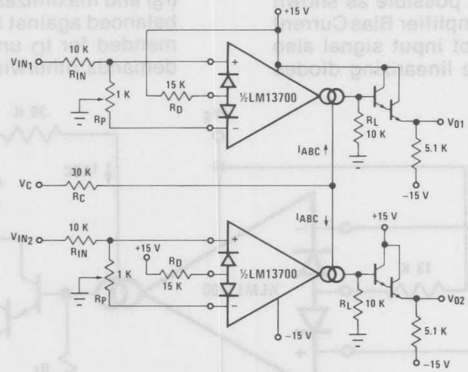


Figure 4. Stereo Volume Control

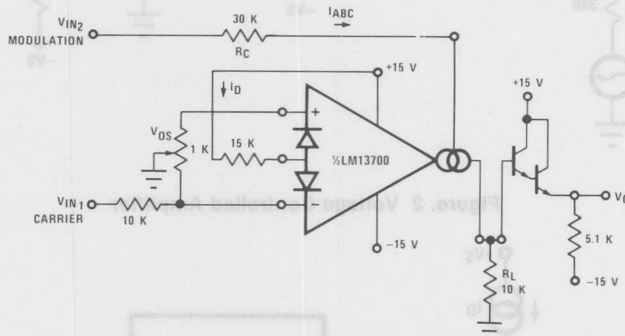


Figure 5. Amplitude Modulator

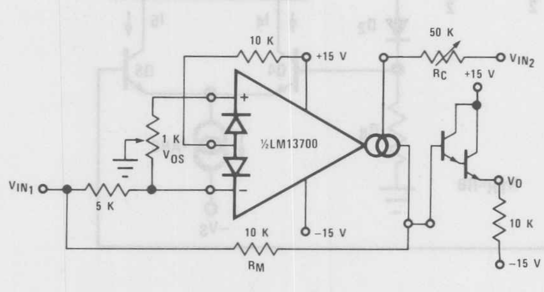


Figure 6. Four-Quadrant Multiplier

this current, resulting in a four-quadrant multiplier where R_C is trimmed such that $V_O = 0V$ for $V_{IN2} = 0V$. R_M also serves as the load resistor for I_O.

Noting that the gain of the LM13700 amplifier of Figure 3 may be controlled by varying the linearizing diode current I_D as well as by varying I_{ABC}, Figure 7 shows an AGC Amplifier using this approach. As V_O reaches a high enough amplitude ($3V_{BE}$) to turn on the Darlington transistors and the linearizing diodes, the increase in I_D reduces the amplifier gain so as to hold V_O at that level.

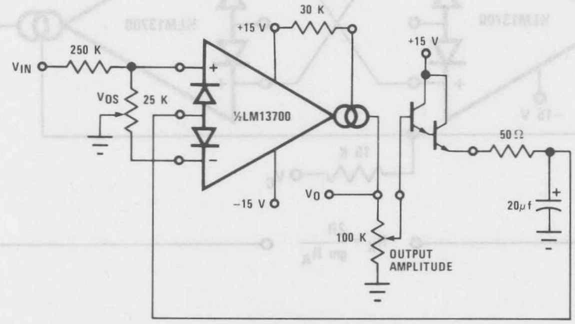
Voltage Controlled Resistors

An Operational Transconductance Amplifier (OTA) may be used to implement a Voltage Controlled Resistor as shown in Figure 8. A signal voltage applied at R_X generates a V_{IN} to the LM13700 which is then multiplied by the gm of the amplifier to produce an output current, thus:

$$R_X = \frac{R + R_A}{g_m R_A}$$

where $g_m \approx 19.2 I_{ABC}$ at 25°C. Note that the attenuation of V_O by R and R_A is necessary to maintain V_{IN} within the linear range of the LM13700 input.

Figure 9 shows a similar VCR where the linearizing diodes are added, essentially improving the noise performance of the resistor. A floating VCR



7. AGC Amplifier

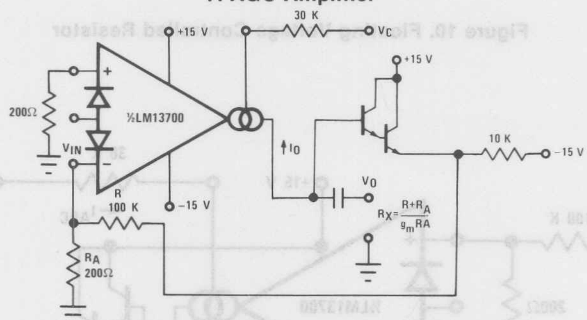


Figure 8. Voltage Controlled Resistor, Single-Ended

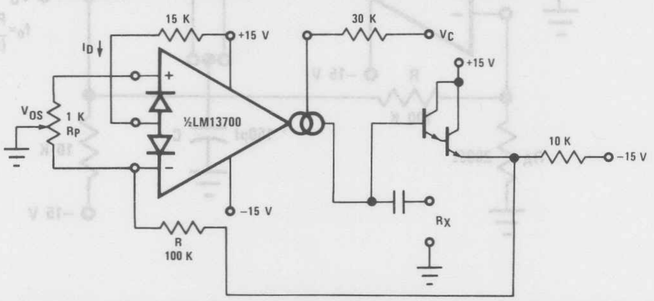


Figure 9. Voltage Controlled Resistor With Linearizing Diodes

...g range of the LM13700.

Voltage Controlled Filters

OTA's are extremely useful for implementing voltage controlled filters, with the LM13700 Figure 11 performs as a unity-gain buffer amplifier at frequencies below cut-off, with the cut-off frequency being the point at which X_C/gm equals the closed-loop gain of (R/R_A). At frequencies above cut-off the circuit provides a single RC roll-off (6 dB per octave) of the input signal amplitude with a -3 dB point defined by the given equation,

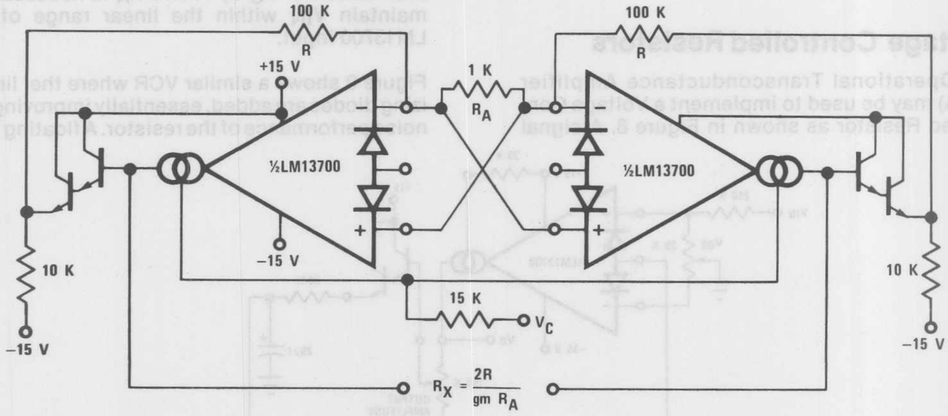


Figure 10. Floating Voltage Controlled Resistor

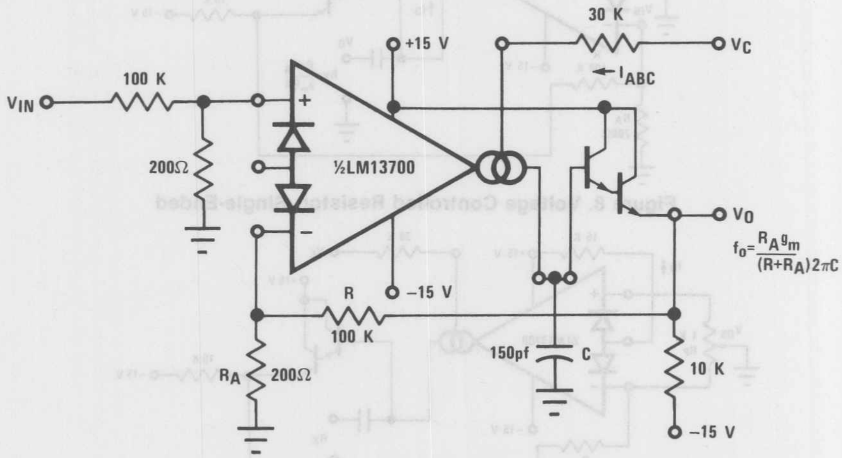


Figure 11. Voltage Controlled Low-Pass Filter

where gm is again 19.2 x I_{ABC} at room temperature. Figure 12 shows a VC High-Pass Filter which operates in much the same manner, providing a single RC roll-off below the defined cut-off frequency.

Additional amplifiers may be used to implement higher order filters as demonstrated by the two-pole Butterworth Lo-Pass Filter of Figure 13 and the state variable filter of Figure 14. Due to the excellent gm tracking of the two amplifiers, these filters perform well over several decades of frequency.

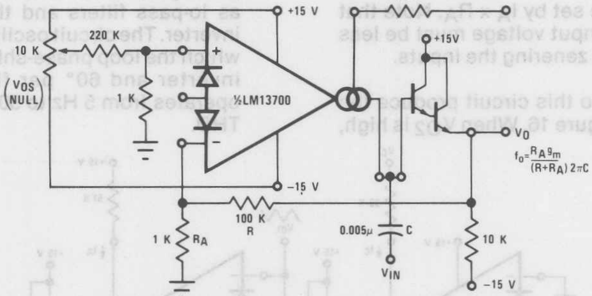


Figure 12. Voltage Controlled Hi-Pass Filter

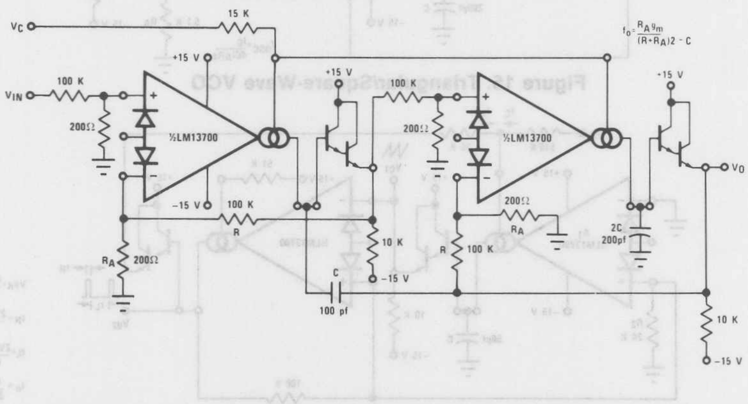


Figure 13. Voltage Controlled 2-pole Butterworth Lo-Pass Filter

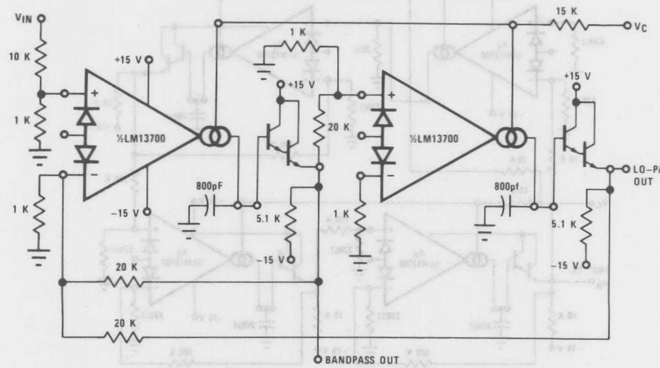


Figure 14. Voltage Controlled State Variable Filter

Voltage Controlled Oscillators

The classic Triangular/Square Wave VCO of Figure 15 is one of a variety of Voltage Controlled Oscillators which may be built utilizing the LM13700. With the component values shown, this oscillator provides signals from 200 kHz to below 2 Hz as I_C is varied from 1mA to 10nA. The output amplitudes are set by $I_A \times R_A$. Note that the peak differential input voltage must be less than 5 volts to prevent zenering the inputs.

A few modifications to this circuit produce the ramp/pulse VCO of Figure 16. When V_{O2} is high, I_F is added to I_C to increase amplifier A1's bias current and thus to increase the charging rate of capacitor C. When V_{O2} is low, I_F goes to zero and the capacitor discharge current is set by I_C.

The VC Lo-Pass Filter of Figure 11 may be used to produce a high-quality sinusoidal VCO. The circuit of Figure 16 employs two LM13700 packages, with three of the amplifiers configured as lo-pass filters and the fourth as a limiter/-inverter. The circuit oscillates at the frequency at which the loop phase-shift is 360° or 180° for the inverter and 60° per filter stage. This VCO operates from 5 Hz to 50 kHz with less than 1% THD.

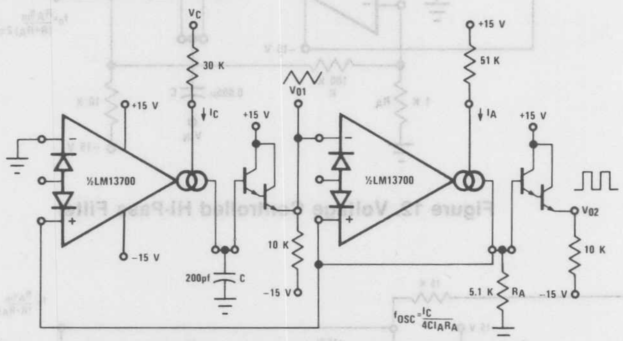


Figure 15. Triangular/Square-Wave VCO

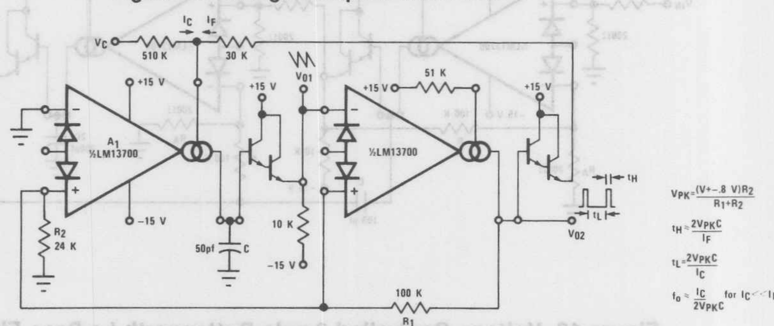


Figure 16. Ramp/Pulse VCO

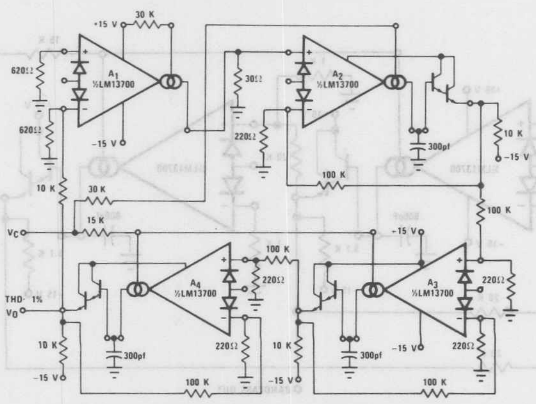


Figure 17. Sinusoidal VCO

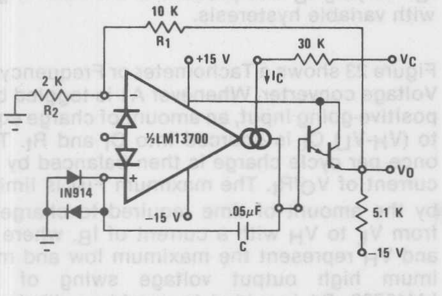


Figure 18. Single Amplifier VCO

Figure 18 shows how to build a VCO using one amplifier when the other amplifier is needed for another function.

Additional Applications

Figure 19 presents an interesting one-shot which draws no power supply current until it is triggered. A positive-going trigger pulse of at least 2V amplitude turns on the amplifier through R_B and pulls the non-inverting input high. The amplifier regenerates and latches its output high until capacitor C charges to the voltage level on the non-inverting input. The output then switches low, turning off the amplifier and discharging the capacitor. The capacitor discharge rate is speeded up by shorting the diode bias pin to the inverting input so that an additional discharge current flows through D_I when the amplifier output switches low. A special feature of this timer is that the other amplifier, when biased from V_O, can perform another function and draw zero stand-by power as well.

The operation of the multiplexer of Figure 20 is very straightforward. When A1 is turned on it holds V_O equal to V_{IN1} and when A2 is supplied with bias current then it controls V_O. C_C and R_C serve to stabilize the unity-gain

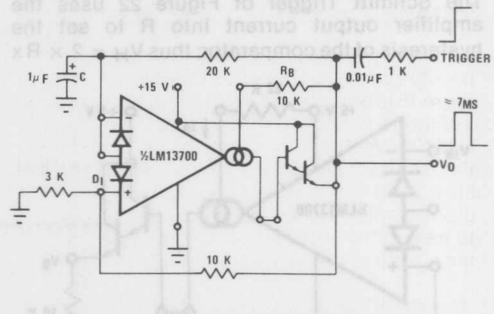


Figure 19. Zero Stand-by Power Timer

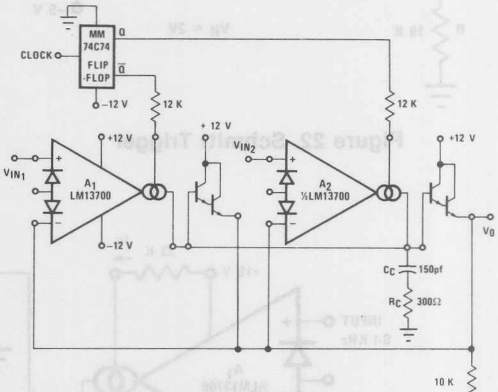


Figure 20. Multiplexer

configuration of amplifiers A1 and A2. The maximum clock rate is limited to about 200 KHz by the LM13700 slew rate into 150 pF when the $(V_{IN1}\text{-}V_{IN2})$ differential is at its maximum allowable value of 5 volts.

The Phase-Locked Loop of Figure 21 uses the four-quadrant multiplier of Figure 6 and the V_{CO} of Figure 18 to produce a PLL with a ± 5% hold-in range and an input sensitivity of about 300 mV.

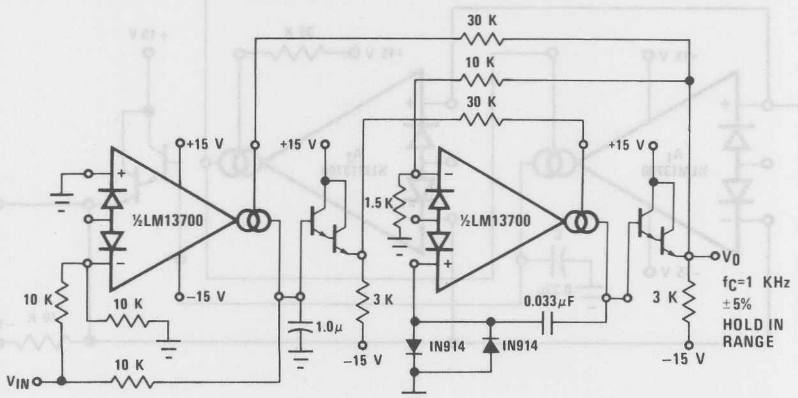


Figure 21. Phase Lock Loop

The Schmitt Trigger of Figure 22 uses the amplifier output current into R to set the hysteresis of the comparator; thus $V_H = 2 \times R \times I_B$. Varying I_B will produce a Schmitt Trigger with variable hysteresis.

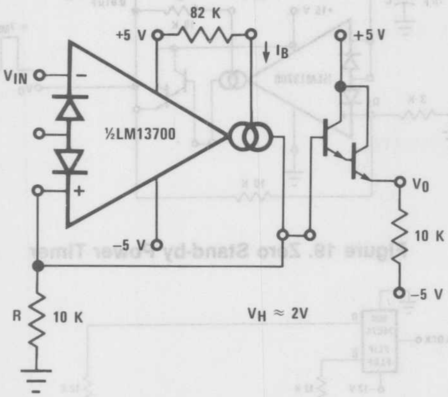


Figure 22. Schmitt Trigger

Figure 23 shows a Tachometer or Frequency-to-Voltage converter. Whenever A1 is toggled by a positive-going input, an amount of charge equal to $(V_H-V_L)\,C_t$ is sourced into C_f and R_t. This once per cycle charge is then balanced by the current of V_O/R_t. The maximum F_{IN} is limited by the amount of time required to charge C_t from V_L to V_H with a current of I_B, where V_L and V_H represent the maximum low and maximum high output voltage swing of the LM13700. D1 is added to provide a discharge path for C_t when A1 switches low.

The Peak Detector of Figure 24 uses A2 to turn on A1 whenever V_{IN} becomes more positive than V_O. A1 then charges storage capacitor C to hold V_O equal to V_{IN} PK. Pulling the output of A2 low through D1 serves to turn off A1 so that V_O remains constant.

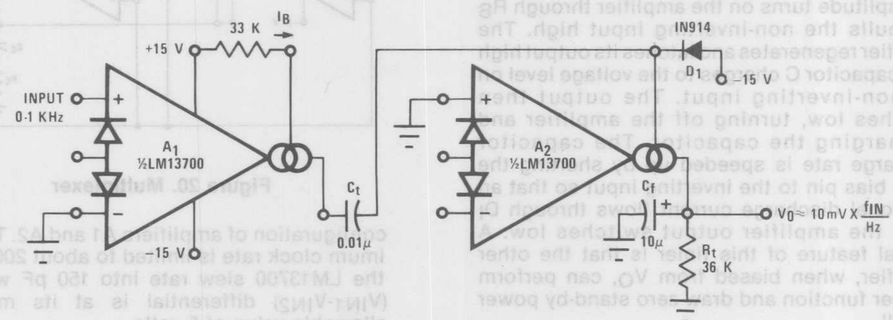


Figure 23. Tachometer

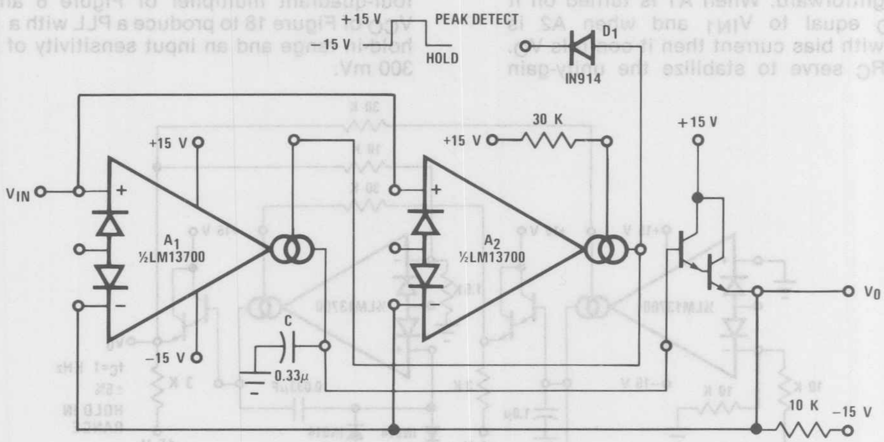


Figure 24. Peak Detector and Hold Circuit

The Ramp-and-Hold of Figure 26 sources I_B into capacitor C whenever the input to A1 is brought high, giving a ramp-rate of about lV/ms for the component values shown.

The true RMS converter of Figure 27 is essentially an automatic gain control amplifier which adjusts its gain such that the AC power at the output of amplifier A1 is constant. The output power of amplifier A1 is monitored by squaring amplifier A2 and the average compared to a reference voltage with amplifier A3. The output of A3 provides bias current to the diodes of A1 to attenuate the input signal. Because the output power of A1 is held constant, the RMS value is constant and the attentuation is directly proportional to the RMS value of the input voltage. The attenuation is also proportional to the diode bias current. Amplifier A4 adjusts the ratio of currents through the diodes to be equal and therefore the voltage at the output of A4 is proportional to the RMS value of the input voltage. The calibration potentiometer is set such that V_O reads directly in RMS volts.

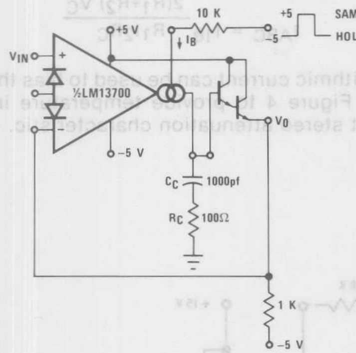


Figure 25. Sample-Hold Circuit

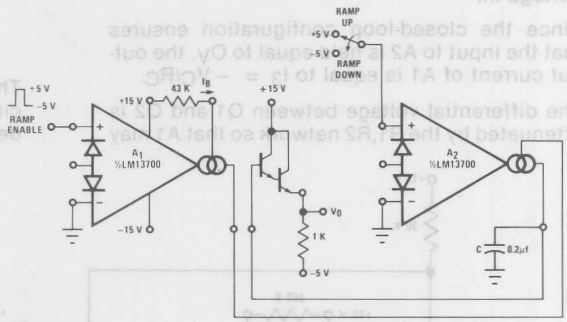


Figure 26. Ramp and Hold

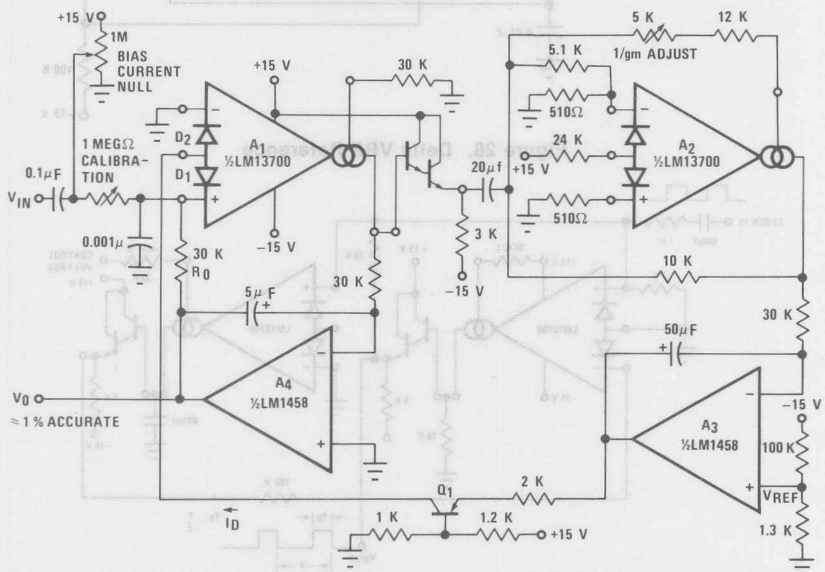


Figure 27. True RMS Converter

about 1.2 volts and negative TC below 1.2 volts. This is accomplished by balancing the TC of the A2 transfer function against the complementary TC of D1.

The wide dynamic range of the LM13700 allows easy control of the output pulse width in the Pulse Width Modulator of Figure 29.

For generating I_{ABC} over a range of 4 to 6 decades of current, the system of Figure 30 provides a logarithmic current out for a linear voltage in.

Since the closed-loop configuration ensures that the input to A2 is held equal to 0_V, the output current of A1 is equal to $I_3 = -V_C/R_C$.

The differential voltage between Q1 and Q2 is attenuated by the R1,R2 network so that A1 may

$\dots \quad qI_2 \qquad qI_2R_C$

The voltage on the base of Q1 is then

$$V_{B1} = \frac{(R_1+R_2)\ V_{IN1}}{R_1}$$

The ratio of the Q1 to Q2 collector currents is defined by:

$$V_{B1} = \frac{KT}{q} \ln \frac{I_{C2}}{I_{C1}} \approx \frac{KT}{q} \ln \frac{I_{ABC}}{I_1}$$

Combining and solving for I_{ABC} yields:

$$I_{ABC} = I_{1e} \frac{2(R_1+R_2)\ V_C}{R_1 I_2 R_C}$$

This logarithmic current can be used to bias the circuit of Figure 4 to provide temperature independent stereo attenuation characteristic.

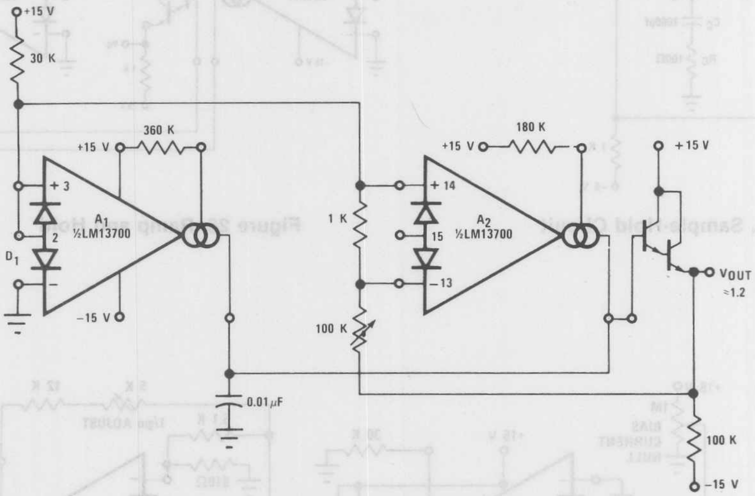


Figure 28. Delta VBE Reference

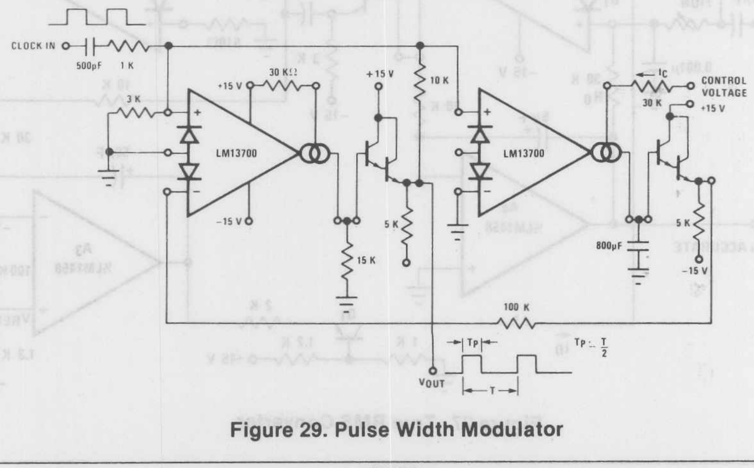


Figure 29. Pulse Width Modulator

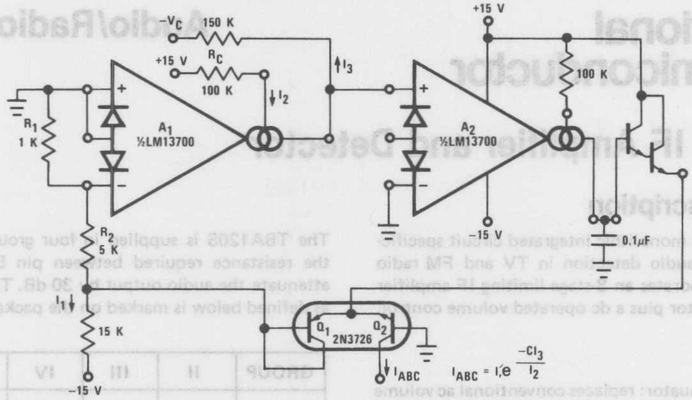


Figure 30. Logarithmic Current Source

National Semiconductor

Audio/Radio Circuits

TBA120S IF Amplifier and Detector

General Description

The TBA120S is a monolithic integrated circuit specifically designed for audio detection in TV and FM radio receivers. It incorporates an 8-stage limiting IF amplifier and balanced detector plus a dc operated volume control.

The TBA120S is supplied in four groups depending on the resistance required between pin 5 and ground to attenuate the audio output by 30 dB. The group number as defined below is marked on the package.

GROUP	II	III	IV	V	
R5-Gnd	1.9-2.2	2.1-2.5	2.4-2.9	2.8-3.3	kΩ

Pins 3 and 4 are connected to the collector and base of a transistor which may be used as an AF-preamplifier or as a switch.

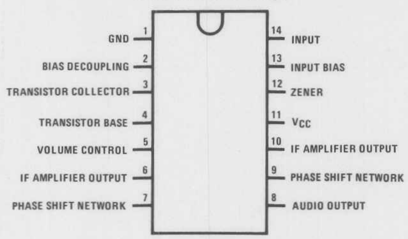
At pin 12 a zener-diode is accessible which can be used to stabilize the supply voltage of this integrated circuit or the voltage of other circuit elements in the set.

Features

- Electronic attenuator: replaces conventional ac volume control
- Volume reduction range 85 dB typ
- Sensitivity: 3 dB limiting voltage 30μV typ
- Excellent AM rejection 68 dB typ at 10 mV
- Audio output voltage 1V typ
- Wide supply voltage range (6-18V)
- Internal zener diode regulator
- Very low external component requirement
- Simple detector alignment: one coil

Connection Diagram

Dual-In-Line Package

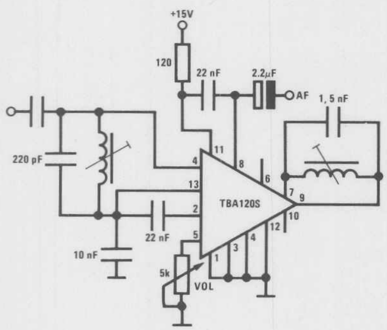


TOP VIEW

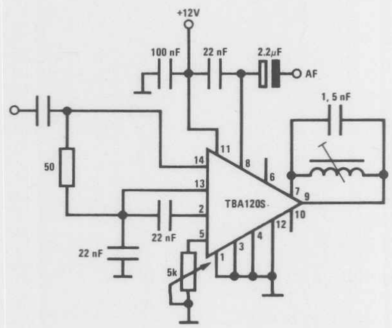
Order Number TBA120S II, TBA120S III, TBA120S IV or TBA120S V
See NS Package N14A

Order Number TBA120SQ II, TBA120SQ III, TBA120SQ IV, TBA120SQ V
See NS Package N14C

Typical Application (5.5 MHz)



Test Circuit (5.5 MHz)



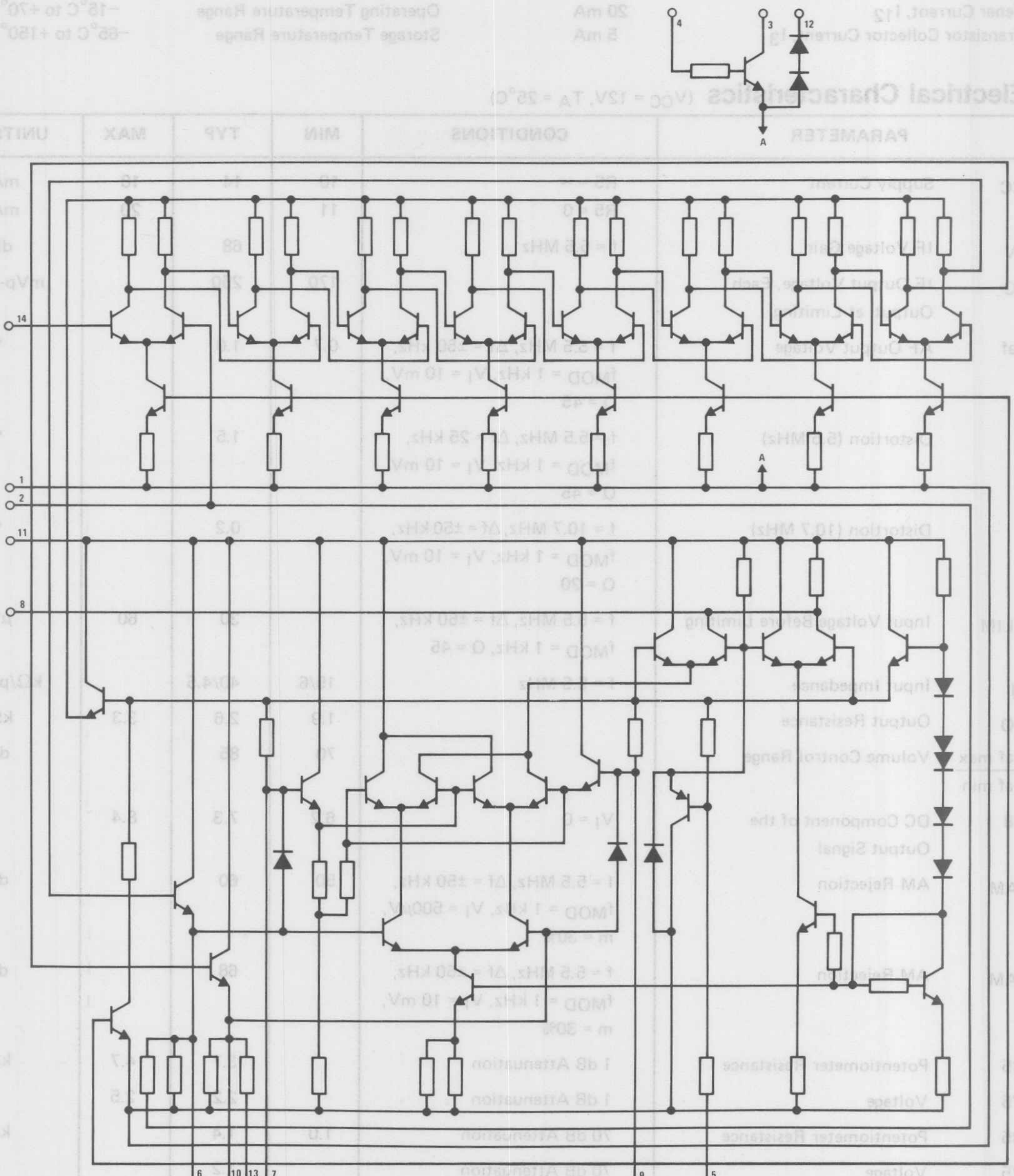
Absolute Maximum Ratings

Supply Voltage, V11	18V	Transistor Base Current, I_4	2 mA
Volume Control Voltage, V5	4V	Bias Resistance (Max), R13-14	1 kΩ
Zener Current, I_{12}	20 mA	Operating Temperature Range	−15°C to +70°C
Transistor Collector Current, I_3	5 mA	Storage Temperature Range	−65°C to +150°C

Electrical Characteristics (V_{CC} = 12V, T_A = 25°C)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{CC}	Supply Current	R5 = ∞	10	14	18	mA
		R5 = 0	11		20	mA
G_V	IF Voltage Gain	f = 5.5 MHz		68		dB
V_O	IF Output Voltage, Each Output, at Limiting		170	250		mVp-p
Vaf	AF Output Voltage	f = 5.5 MHz, Δf = ±50 kHz, f_{MOD} = 1 kHz, V_I = 10 mV, Q = 45	0.7	1.0		V
	Distortion (5.5 MHz)	f = 5.5 MHz, Δf = 25 kHz, f_{MOD} = 1 kHz, V_I = 10 mV, Q = 45		1.5		%
	Distortion (10.7 MHz)	f = 10.7 MHz, Δf = ±50 kHz, f_{MOD} = 1 kHz, V_I = 10 mV, Q = 20		0.2		%
V_{LIM}	Input Voltage Before Limiting	f = 5.5 MHz, Δf = ±50 kHz, f_{MOD} = 1 kHz, Q = 45		30	60	μV
Z_I	Input Impedance	f = 5.5 MHz	15/6	40/4.5		kΩ/pF
R_O	Output Resistance		1.9	2.6	3.3	kΩ
$\frac{\text{Vaf max}}{\text{Vaf min}}$	Volume Control Range		70	85		dB
V8	DC Component of the Output Signal	V_I = 0	6.2	7.3	8.4	V
a_{AM}	AM Rejection	f = 5.5 MHz, Δf = ±50 kHz, f_{MOD} = 1 kHz, V_I = 500μV, m = 30%	50	60		dB
a_{AM}	AM Rejection	f = 5.5 MHz, Δf = ±50 kHz, f_{MOD} = 1 kHz, V_I = 10 mV, m = 30%		68		dB
R5	Potentiometer Resistance	1 dB Attenuation		3.7	4.7	kΩ
V5	Voltage	1 dB Attenuation		2.2	2.5	V
R5	Potentiometer Resistance	70 dB Attenuation	1.0	1.4		kΩ
V5	Voltage	70 dB Attenuation		1.2		V
	Noise Voltage at Output	V_I = 10 mV		30		μV
V12	Zener Voltage	I_{12} = 5 mA	11.2	12	13.4	V
R_Z	Zener Slope Resistance			30	50	Ω
V_{cbo}	Breakdown Voltage		45	65		V
V_{ceo}	Breakdown Voltage	I_3 = 500μA	18	24		V
h_{fe}	Current Gain	I_3 = 1 mA	50	100	500	

Schematic Diagram



TBA120U, TBA120T IF Amplifier and Detector

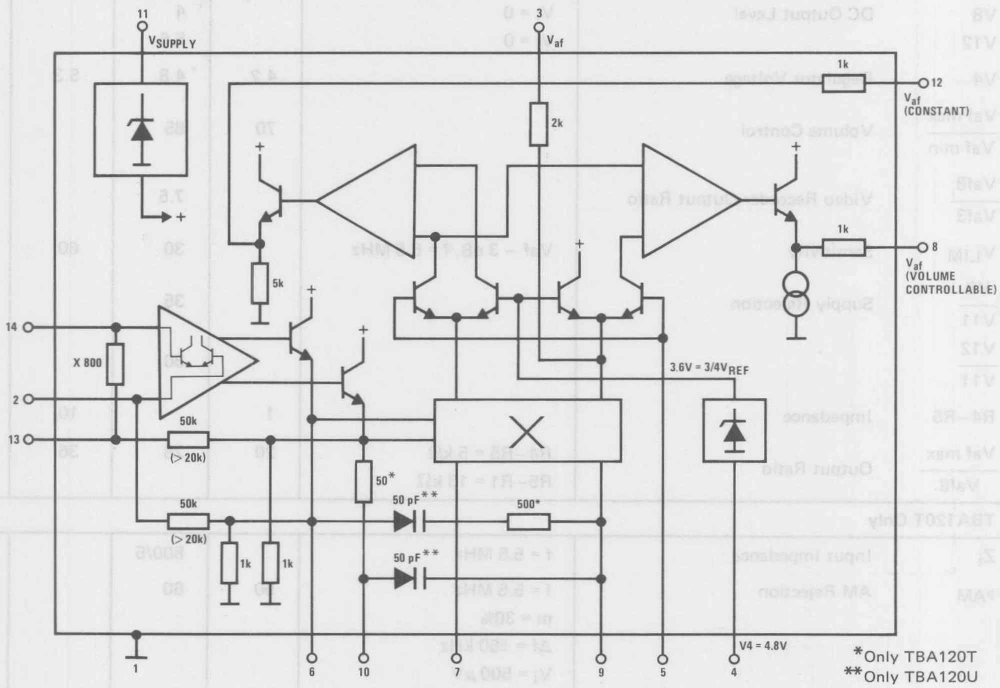
General Description

The TBA120U, TBA120T is a monolithic integrated circuit specifically designed for audio detection in TV and FM radio receivers. It incorporates an 8 stage limiting IF amplifier and balanced detector plus a DC operated volume control. The circuit also provides connection facilities for a video tape recorder. The TBA120T is designed primarily for use with ceramic filters while the TBA120U is optimized for inductive tuning.

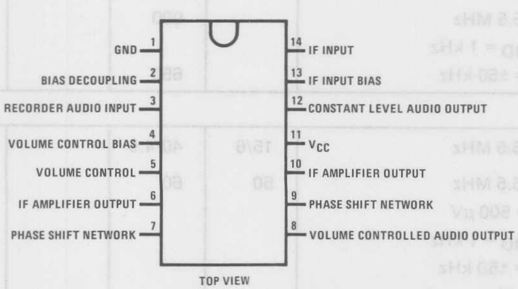
Features

- Electronic attenuator: replaces conventional AC volume control
- Volume reduction range: 85 dB typ
- Sensitivity: 3 dB limiting voltage 30 μV typ
- Excellent AM rejection 68 dB typ 500 μV
- Wide supply voltage range (6 to 18V)
- Easy video recorder connection
- Very low external component requirement
- Simple detector alignment: one coil

Block and Connection Diagrams



*Only TBA120T
**Only TBA120U



TOP VIEW

Order Number TBA120U or TBA120T
See NS Package N14A

Order Number TBA120TQ or TBA120UQ
See NS Package N14C

Absolute Maximum Ratings

Supply Voltage, $V11$	18V	Current Pin 4, I_4	5 mA
Operating Temperature Range, T_u	−15°C to +70°C	Operating Frequency Range, f	0 to 12 MHz
Storage Temperature Range, T_s	−40°C to +125°C	Power Dissipation, P_{tot}	400 mW
Voltage Pin 5, $V5$	6V	Resistor Parallel to Pins 13 and 14	1 kΩ

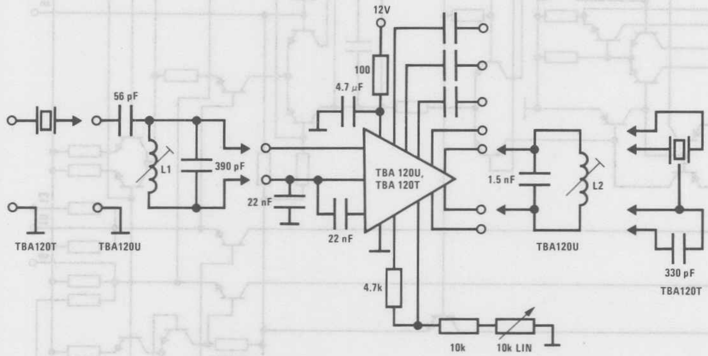
Electrical Characteristics ($V_{CC} = 12V, T_A = 25°C$)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
I_{CC}	Supply Current		9.5	13.5	17.5	mA
G_V	IF Voltage Gain	f = 5.5 MHz		68		dB
V_O	IF Output Voltage (Each Output Limiting)			250		mVp-p
R8	Output Impedance			1.1		kΩ
R12				1.1		kΩ
R3	Input Impedance			2		kΩ
R4	Regulator Impedance			12		Ω
V8	DC Output Level	$V_i = 0$		4		V
V12		$V_i = 0$		5.6		V
V4	Regulator Voltage		4.2	4.8	5.3	V
$\frac{V_{af\,max}}{V_{af\,min}}$	Volume Control		70	85		dB
$\frac{V_{af8}}{V_{af3}}$	Video Recorder Output Ratio			7.5		
V_{LIM}	Sensitivity	Vaf − 3 dB, f = 5.5 MHz		30	60	μV
$\frac{V8}{V11}$	Supply Rejection			35		dB
$\frac{V12}{V11}$				30		dB
R4–R5	Impedance		1		10	kΩ
$\frac{V_{af\,max}}{V_{af8}}$	Output Ratio	R4–R5 = 5 kΩ R5–R1 = 13 kΩ	20	28	36	dB
TBA120T Only						
Z_i	Input Impedance	f = 5.5 MHz		800/5		Ω/pF
a_{AM}	AM Rejection	f = 5.5 MHz m = 30% Δf = ±50 kHz $V_i = 500\ \mu V$ $f_{MOD} = 1$ kHz	50	60		dB
Vaf8	A.F. Output Voltage	f = 5.5 MHz $f_{MOD} = 1$ kHz Δf = ±50 kHz		900		mV
Vaf12				650		mV
TBA120U Only						
Z_i	Input Impedance	f = 5.5 MHz	15/6	40/4.5		kΩ/pF
a_{AM}	AM Rejection	f = 5.5 MHz $V_i = 500\ \mu V$ $f_{MOD} = 1$ kHz Δf = ±50 kHz m = 30%	50	60		dB

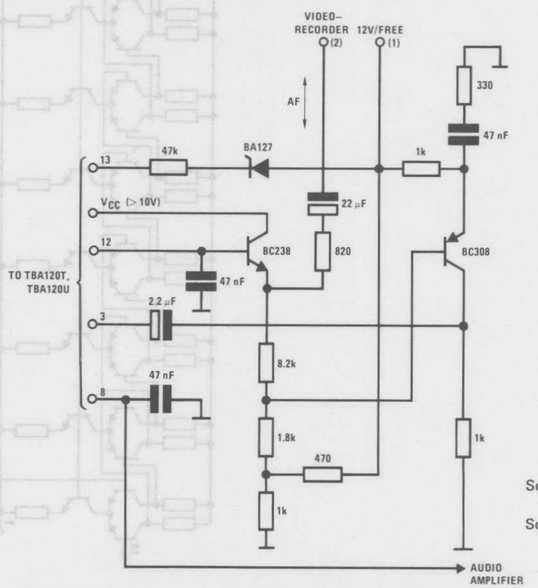
Electrical Characteristics (Continued) (V_{CC} = 12V, T_A = 25°C)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
TBA120U Only (Continued)						
Vaf8	A.F. Output Voltage	f = 5.5 MHz f_{MOD} = 1 kHz Δf = ±50 kHz V_i = 10 mV Q_B = 45		1.3		V
Vaf12	A.F. Output Voltage			1.0		V
k	Distortion	f = 5.5 MHz Δf = ±50 kHz f_{MOD} = 1 kHz Q_B = 45 V_i = 10 mV		1		%

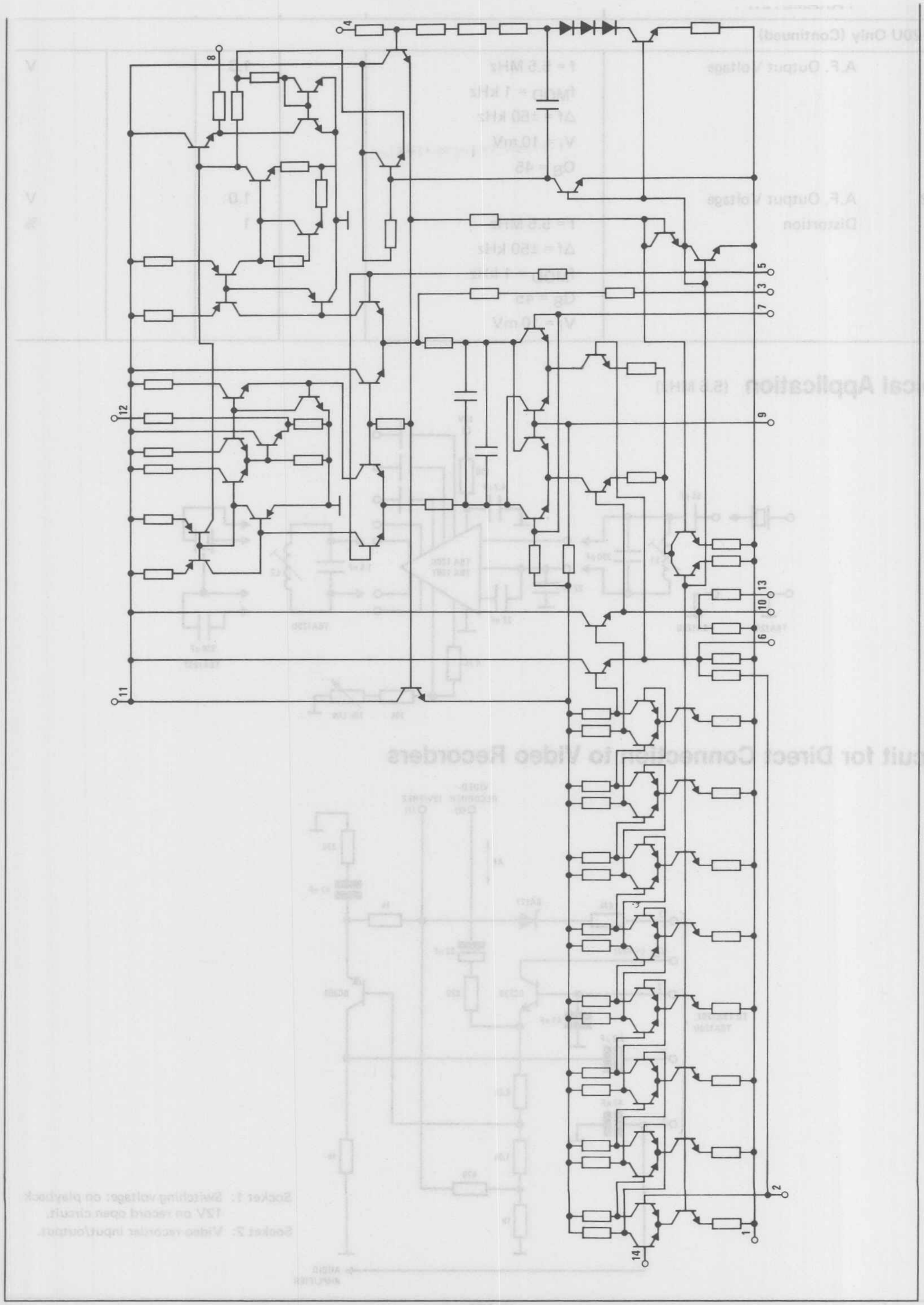
Typical Application (5.5 MHz)



Circuit for Direct Connection to Video Recorders



Socket 1: Switching voltage: on playback 12V on record open circuit.
Socket 2: Video recorder input/output.


4
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1
14

TDA2003 Audio Power Amplifier

General Description

The TDA2003 is an audio power amplifier designed primarily for automotive applications. Its high current capability and low saturation resistance of the output drivers enables the device to deliver large power outputs into low impedance loads where supply voltage is a limiting factor.

Features

- Short circuit protection
- Supply over-voltage protection
- Thermal shutdown protection
- Low distortion
- Low noise
- Externally programmable gain

Typical Application

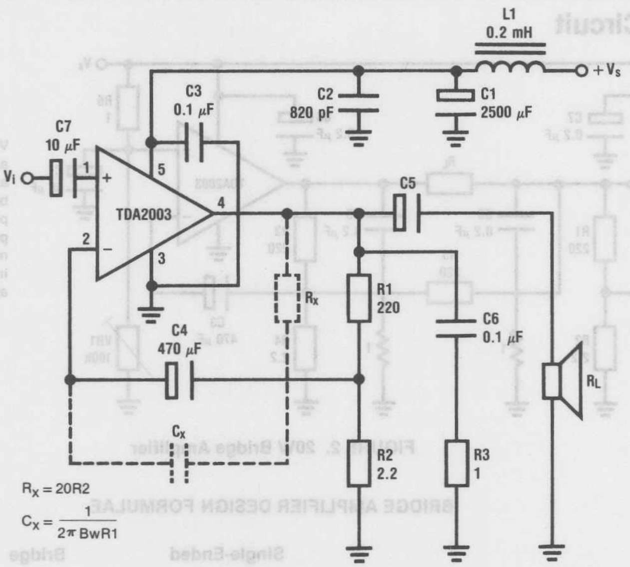


FIGURE 1

Order Number TDA2003T
See NS package T05B

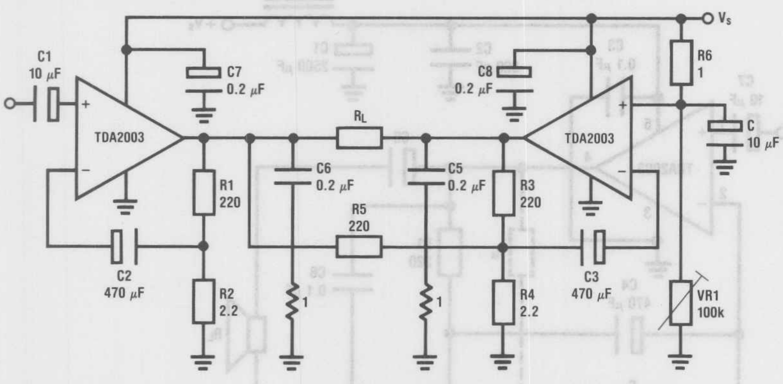
Absolute Maximum Ratings

Peak Supply Voltage 50 ms (Load Dump, see Test Circuit)	50V
DC Supply Voltage (Continuous)	30V
Operating Supply Voltage	20V
Output Peak Current (Repetitive)	3.5A
Output Peak Current (Non-Repetitive)	4.5A

Electrical Characteristics $T_A = 25°C$, $V_s = 14.4V$ (unless stated otherwise)

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage		6		20	V
Quiescent Current (Pin 5)		50		100	mA
Quiescent Voltage (Pin 4)		6.1	6.9	7.7	V
Output Power					
$R_L = 4\Omega$	THD = 10%, f = 1 kHz $A_v = 40$ dB	5.5	6		W
$R_L = 2\Omega$	THD = 10%, f = 1 kHz $A_v = 40$ dB	9.5	10		W
Distortion (THD)					
$R_L = 4\Omega$	$P_o = 0.05W–4.5W$ $A_v = 40$ dB, f = 1 kHz		0.12		%
$R_L = 2\Omega$	$P_o = 0.05W–7.5W$ $A_v = 40$ dB, f = 1 kHz		0.18		%
Open Loop Voltage Gain			80		dB
Closed Loop Voltage Gain			40		dB
Input Noise Voltage			1	5	μV
Input Resistance	f = 1 kHz	70	150		kΩ

Application Circuit



Voltage and current swings for a bridge amplifier are twice that of a single-ended amplifier; i.e., with the same R_L, the bridge configuration can deliver an output power that is four times the output power of a single-ended amplifier. Care must be taken when selecting V_S and R_L in order to avoid an output peak current above the maximum rating,

i.e., $R_L \text{ min} = \dfrac{V_S - 2\,V_{CE} \text{ sat}}{I_O \text{ max}}$

FIGURE 2. 20W Bridge Amplifier

BRIDGE AMPLIFIER DESIGN FORMULAE

	Single-Ended	Bridge
Max output voltage swing (1/2 wave before clipping)	$1/2\,(V_s - 2\,V_{CE} \text{ sat})$	$V_s - 2\,V_{CE} \text{ sat}$
Max output current swing (1/2 wave before clipping)	$\dfrac{(V_s - 2\,V_{CE} \text{ sat})}{2R_L}$	$\dfrac{V_s - 2\,V_{CE} \text{ sat}}{R_L}$
Max output power (before clipping)	$\dfrac{(V_s - 2\,V_{CE} \text{ sat})^2}{8R_L}$	$\dfrac{(V_s - 2\,V_{CE} \text{ sat})^2}{2R_L}$

Test Circuits

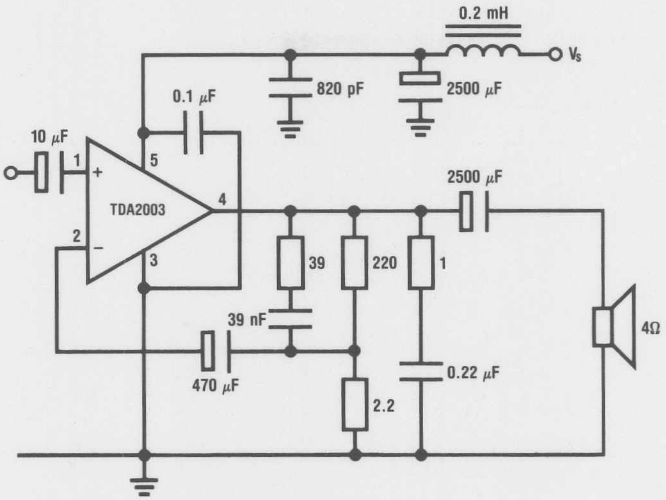


FIGURE 3. IC Audio Amplifier

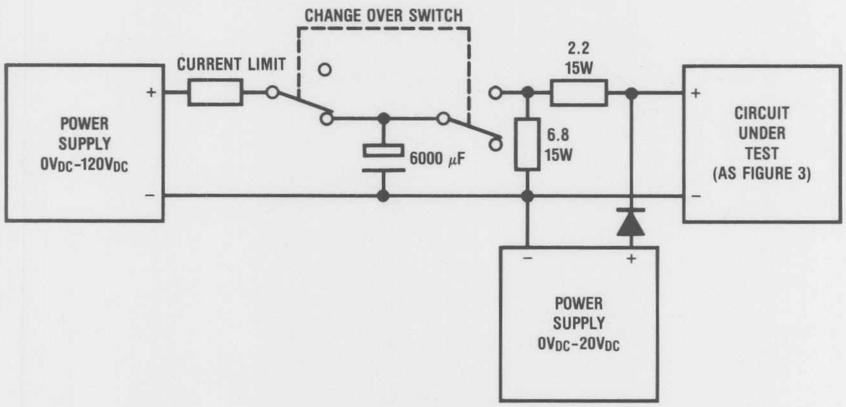


FIGURE 4. Load Dump

Section 11

TV Circuits

TV Circuits

Section Contents

National Semiconductor

TV Circuits

LM1017 4-Bit Binary 7-Segment Decoder/Driver

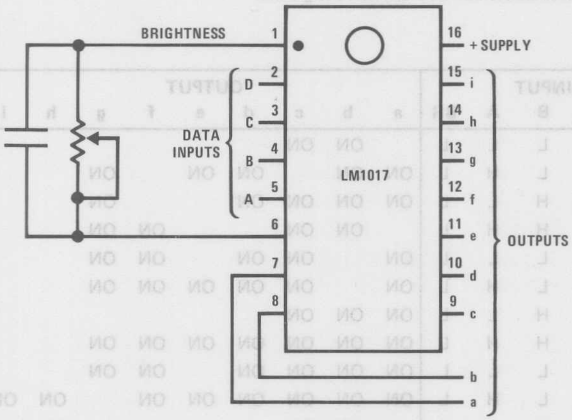
General Description

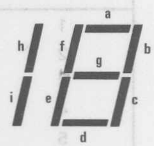
The LM1017 is a monolithic IC which decodes 4-bit "binary plus one" coded input signals and supplies 1 1/2-digit TV channel display information. The outputs are designed to drive a 7-segment common cathode LED display with up to 25 mA depending on thermal dissipation requirements. Improvements in circuit design enable the device to operate from 5V to 12V supply. A brightness control facility is included.

Features

- A direct replacement for SN29764 but with 12V supply capability
- TTL compatible inputs with high input voltage immunity
- Channel displays are from 1 to 16
- Current-driven output stages for LEDs protect against excess thermal dissipation
- Continuously variable brightness control
- Low stand-by quiescent current supply consumption
- Suitable for NSN583 0.5 inch LED display
- Inputs are suitable for direct drive from MOS outputs

Connection Diagram





Order Number LM1017N
See NS Package N16A

$V_{SUPPLY} = 5V$
For 12V supply, external resistors must be used between the output pin and segment to limit device dissipation.

Absolute Maximum Ratings

Supply Voltage, Pin 16	13.5V	Storage Temperature Range	−55°C to +150°C
Input Voltage, Pins 2–5	30V	Junction Temperature	150°C
Input Voltage, Pin 1	13.5V	Lead Temperature (Soldering, 10 seconds)	300°C
Operating Temperature Range	0°C to +70°C		

Electrical Characteristics $V16 = 5V, T_A = 25°C$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Current per Segment Quiescent Current, Pin 16	Pin 1 = 2V		12	20	mA
	Pin 1 = 5V		4		mA
Input Logic Voltage	Pins 2–5				
H Signal		2			V
L Signal				0.8	V
Input Current, Pins 2–5	V2–5 = 2.4V			1	μA
	V2–5 = 0V			−5	μA
Input Current, Pin 1	I_{7-15} = −15 mA		−350		μA
Output Current, Pins 7–15	V1 = 0V	−16	−22		mA
	V1 = 2V		−12		mA
	V1 = V16			−20	μA
Minimum Saturation Between Output Terminals 7–15 and 16	I_{OUT} = −20 mA		1.4		V
Package Thermal Resistance, θ_{JA}				100	°C/W

Note. To limit device temperature at supply voltages > 5V, the following condition must be maintained: $8\,(V_{SUPPLY} - V_{OUT})\,I_{OUT} < \dfrac{150 - T_A}{\theta_{JA}}$.

Eg. For 12V supply and 20 mA I_{OUT} into 2V LED, $T_A = 25°C$: $8\,(12 - V_O)\,0.02 < \dfrac{125}{100}$

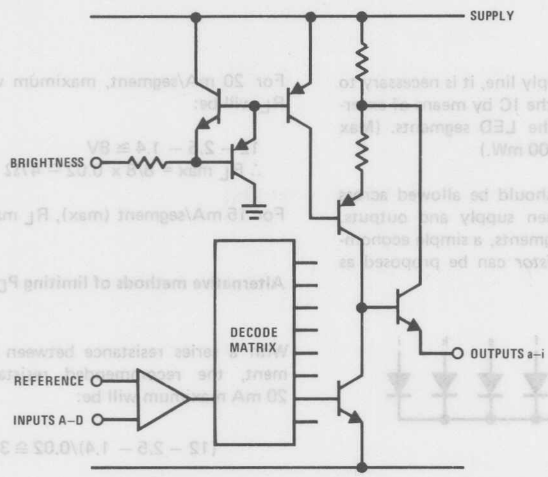
i.e., $V_O > 4.2V$ ∴ series output resistance $= \dfrac{2.2V}{20\text{ mA}} = 110\Omega$.

See application notes for use of common series resistance between LED cathodes and ground.

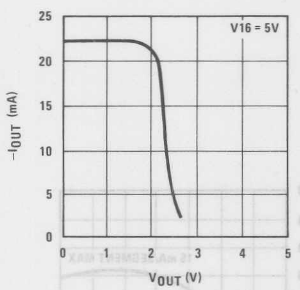
Truth Table

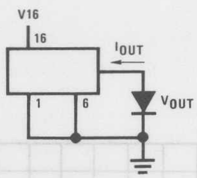
CHANNEL	INPUT D	INPUT C	INPUT B	INPUT A	INPUT BR	OUTPUT a	b	c	d	e	f	g	h	i
1	L	L	L	L	L		ON	ON						
2	L	L	L	H	L	ON	ON		ON	ON		ON		
3	L	L	H	L	L	ON	ON	ON	ON			ON		
4	L	L	H	H	L		ON	ON			ON	ON		
5	L	H	L	L	L	ON		ON	ON		ON	ON		
6	L	H	L	H	L	ON		ON	ON	ON	ON	ON		
7	L	H	H	L	L	ON	ON	ON						
8	L	H	H	H	L	ON	ON	ON	ON	ON	ON	ON		
9	H	L	L	L	L	ON	ON	ON	ON		ON	ON		
10	H	L	L	H	L	ON	ON	ON	ON	ON	ON		ON	ON
11	H	L	H	L	L		ON	ON					ON	ON
12	H	L	H	H	L	ON	ON		ON	ON		ON	ON	ON
13	H	H	L	L	L	ON	ON	ON	ON			ON	ON	ON
14	H	H	L	H	L		ON	ON			ON	ON	ON	ON
15	H	H	H	L	L	ON		ON	ON		ON	ON	ON	ON
16	H	H	H	H	L	ON		ON	ON	ON	ON	ON	ON	ON
OFF	X	X	X	X	H									

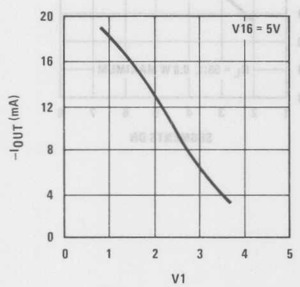
Circuit Schematic (One Circuit Shown)

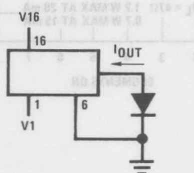


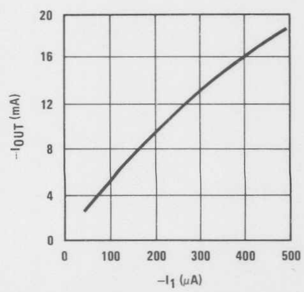
Output Characteristics

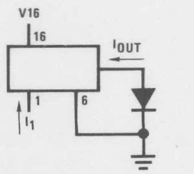








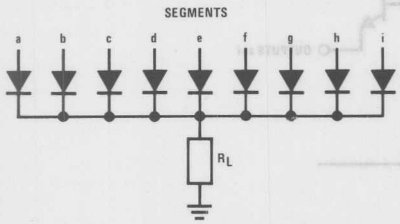




Typical Applications

When operating with a 12V supply line, it is necessary to limit the power dissipation in the IC by means of external resistance in series with the LED segments. (Max package dissipation at 70°C = 800 mW.)

A minimum voltage of 2.5V should be allowed across the output driver pins between supply and outputs. Allowing 1.4V for the LED segments, a simple economical solution using *only 1 resistor* can be proposed as follows:



Maximum no of ON segments = 8

For 20 mA/segment, maximum voltage allowed across R_L will be:

$12 - 2.5 - 1.4 \cong 8V$

$\therefore R_L \text{ max} = 8/8 \times 0.02 \hat{=} 47\Omega$

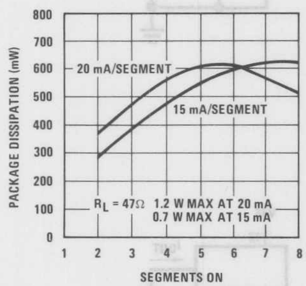
For 15 mA/segment (max), R_L max = 56Ω.

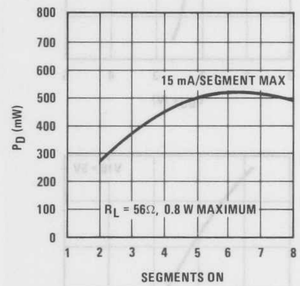
Alternative methods of limiting P_D at 12V supply.

With a series resistance between each output and segment, the recommended resistance per segment at 20 mA maximum will be:

$$(12 - 2.5 - 1.4)/0.02 \hat{=} 390\Omega$$

If a zener is used, maximum zener voltage = 8V. (The zener can be common between LED display cathode and ground.)





LM1019N Digital Tuning Station Detector

General Description

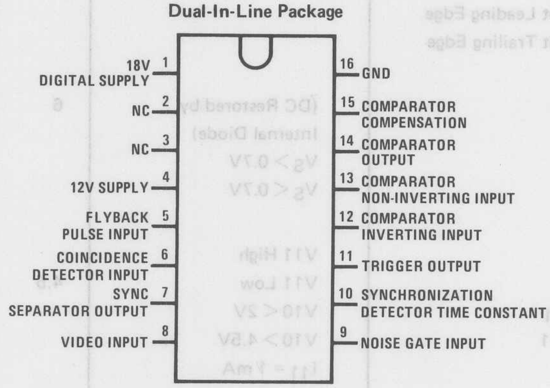
The LM1019N is a monolithic integrated circuit for identifying a valid picture when digitally tuned television receivers are used in the "search" mode.

Features

- Noise gated sync separator
- Coincidence detector between sync and flyback
- Comparator to set AFC voltage at which output triggers

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number LM1019N
See NS Package N16A

V1–16	20V
V3–16	14V
I_{11}	10 mA
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics V1–16 = 18V, V3–16 = 12V, T_A = 25°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current, I_3			6		mA
Supply Current, I_1			2		mA
Video Signal					
Input Voltage Range		1		7	Vp-p
Input Current Driving Sync Pulse			100		μA
Noise Gating					
Input Voltage		0.7			V
Input Current		0.03		10	mA
Flyback Pulse					
Input Voltage		0.7			V
Input Current		0.05	1		mA
Input Resistance			400		Ω
Pulse Deviation	f = 15,625 Hz	10			μs
Composite Sync Pulse Output (Pin 7)					
Output Voltage			10		Vp-p
Output Resistance at Leading Edge			50		Ω
Output Resistance at Trailing Edge			2		kΩ
Coincidence Detector					
Sync Input Voltage	(DC Restored by Internal Diode)	6			V
Input Resistance	$V_S > 0.7V$		5		kΩ
	$V_S < 0.7V$		10		kΩ
Trigger Circuit					
Input Voltage, V10	V11 High			2	V
	V11 Low	4.5			V
Output Leakage, I_{11}	V10 < 2V			100	μA
Output Voltage, V11	V10 > 4.5V, I_{11} = 1 mA		0.2	0.5	V
Comparator					
Input Bias Current			1	10	μA
Input Offset Voltage				25	mV
Voltage Gain	Pin 14 Open Circuit		5000		
Output Current				10	mA
Internal Load Resistance R1–14		7		13	kΩ
Input Common-Mode Range		0		V1–5	V

Typical Applications

The LM1019 provides a "stop" signal to the tuning system when a picture is received but because of the delay in the system when operating in the fast ramp mode, the tuner will normally have passed the optimum tuning point. The "stop" signal therefore ceases and the tuning system reverses direction at a reduced rate. When the AFC reaches its correct level a further "stop" signal is given which ends the search routine.

Figure 1 shows the block schematic of the LM1019 with the required external components for a typical application.

Video with positive-going sync pulses is fed through a low pass filter to prevent noise being mistaken as sync pulses. It is then fed to a sync separator which gives a positive signal output at pin 7 during the sync period.

A noise gate is also provided such that when the voltage on pin 9 exceeds 0.7V the sync separator is inhibited. This can be utilized by coupling video through a high pass filter into pin 9. However, the system works well even without this, and if not required, pin 9 can either be grounded or left open.

The processed sync pulses are AC coupled to the coincidence detector on pin 6 because in the event of there being no video input, pin 7 rises to the high state. Flyback pulses of greater than 1V in amplitude are applied to pin 5 and when this is coincident with the video sync pulse, a current pulse is provided by pin 10.

After a predetermined number of coincident pulses (set by the delay capacitor on pin 10), the Schmitt trigger operates, grounding pin 11. This brings down the voltage applied to the final comparator input from 12V to the required AFC trigger level set by R1 and R2. Typically this will be in the range of 6–10V.

The AFC control voltage is applied to pin 13. This is always less than 12V so that until the sync pulses and the flyback are synchronized, the main output on pin 14 is always low. However, once synchronization is achieved and pin 12 is at a lower reference level, the AFC voltage will rise above this reference and then below it as the tuner passes through the AFC detector range.

Pin 14 thus rises to 18V and then returns to a low level. As the tuner then reverses slowly, pin 14 again goes high when the AFC voltage equals the reference on pin12. This terminates the search routine.

Positive feedback can be provided to give a clean transition and to prevent multiple pulses being sent to the tuning circuits.

This is merely one possible configuration of the circuit. The output amplifier can be used in the inverting mode if the AFC S curve is inverted. A compensation point is also provided for application involving negative feedback where the amplifier may need stabilizing.

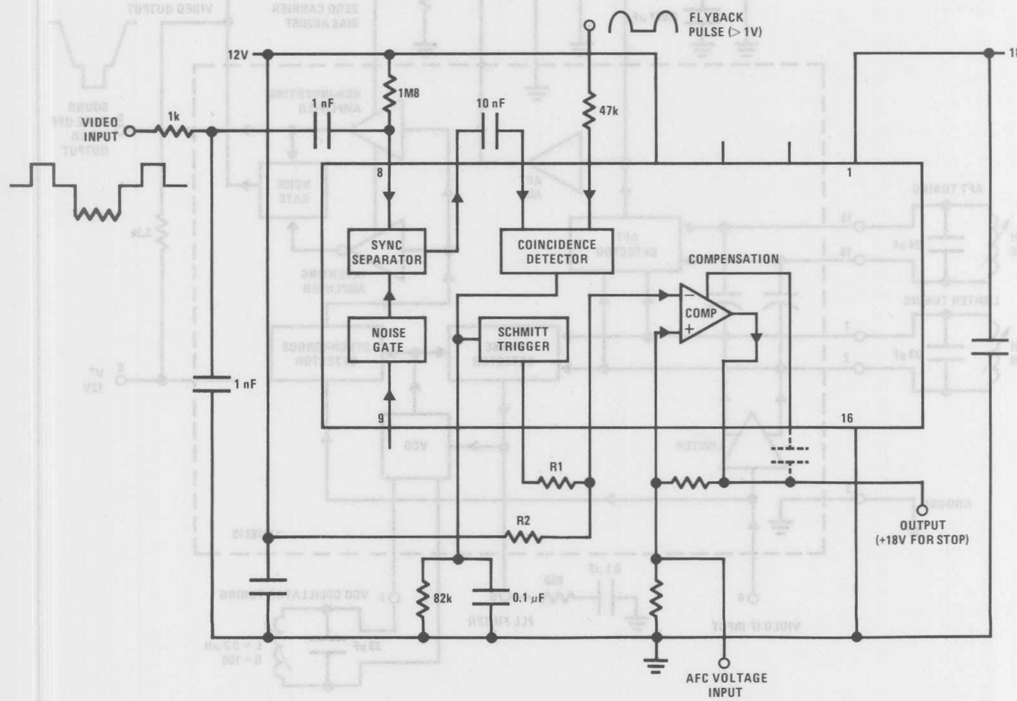


FIGURE 1

National Semiconductor

LM1821S Video IF PLL Synchronous Detector

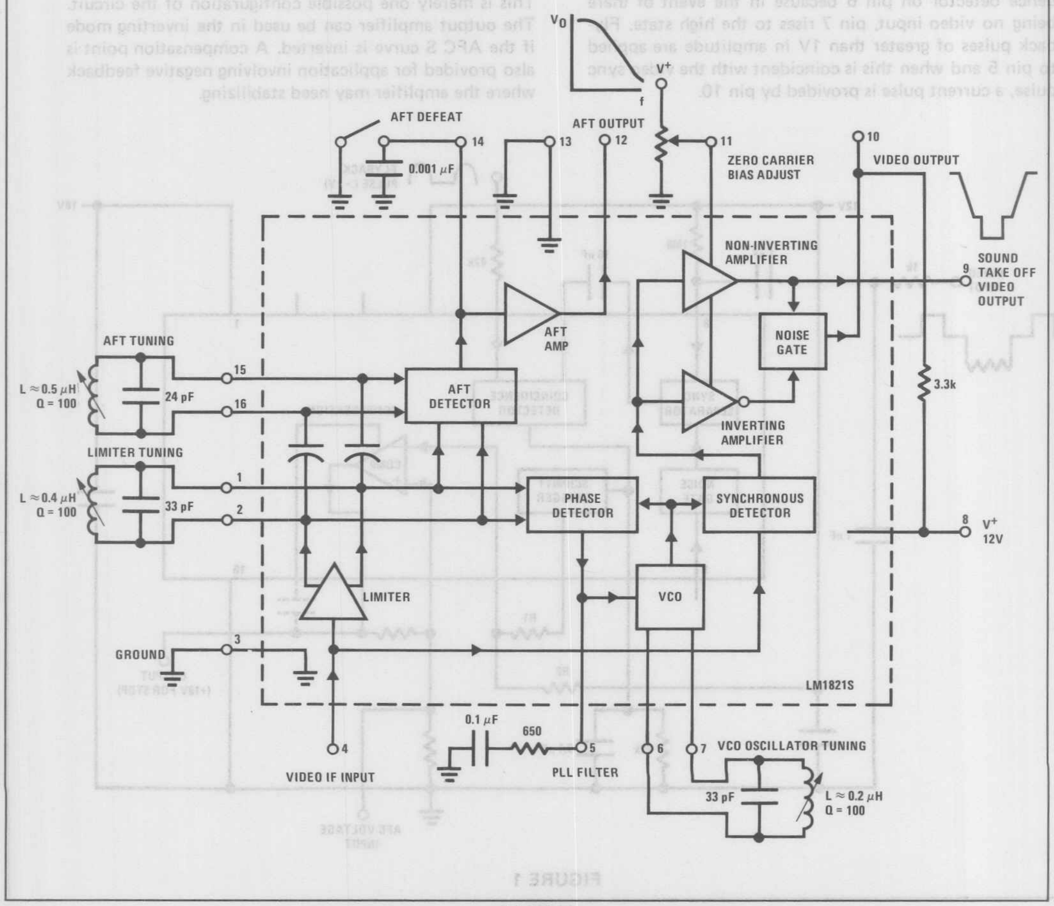
General Description

The LM1821S is a monolithic integrated circuit specifically designed to perform video detection in a color television receiver or cable TV decoder. The device employs a phase-locked loop (PLL) for true synchronous detection, and includes post video amplification with noise inversion and buffered outputs. An automatic fine tuning (AFT) detector with a defeat pin is also provided.

Features

- Wide range PLL oscillator
- Detector very linear at low levels
- Adjustable zero-carrier level
- White-spot noise inversion
- Second video output for sound carrier
- Automatic fine tuning detector
- Ease of detector alignment
- Usable to 70 MHz

Typical Application



Absolute Maximum Ratings

Power Supply Voltage	15V
Power Supply Current	100 mA
Input Signal Voltage	1 Vrms
Device Dissipation	1.5W
Thermal Resistance, θ_{JA}	55°C/W
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	265°C

DC Electrical Characteristics (Reference Test Circuit, all SW position 1 unless noted)

Parameter	Conditions	Min	Typ	Max	Units
Supply Current, I8 + I10		35	55	75	mA
0 Carrier Adjust Voltage, V11	SW 1 Position 2	7.9	8.5	9.0	V
0 Carrier Output Voltage, V9	SW 1 Position 2	6.8	8.5	10.2	V
0 Carrier Bias Difference, V11-V9	SW 1 Position 2		0	±1.3	V
0 Carrier Output Voltage, V10	Adjust V11 for V9 = 7.0V	6.0	6.3	6.5	V
AFT Output Reference, V12		2.5	3.0	3.5	V

AC Electrical Characteristics (SW 2 position 2, V_{IN} = 100 mVrms, see Set-Up Procedure)

Parameter	Conditions	Min	Typ	Max	Units
Detector Gain, V10		2.3	3.6	4.4	V
Output Capability, V10	V_{IN} = 500 mVrms		1	2	V
AFT Maximum Output, V12	SW 4 Position 2, f_{IN} = 44.5 MHz	9	10		V
AFT Minimum Output, V12	SW 4 Position 2, f_{IN} = 45.5 MHz		0.4	1	V
APT Pull-In Range	Difference Between Upper and Lower Lock Frequencies	1	3		MHz
Noise Inversion Defeat Voltage	SW 3 Position 2, Adjust V5 for Beat Frequency at Pin 10, Measure Difference in (−) Peaks		0.3	±0.6	V

Set-Up Procedure

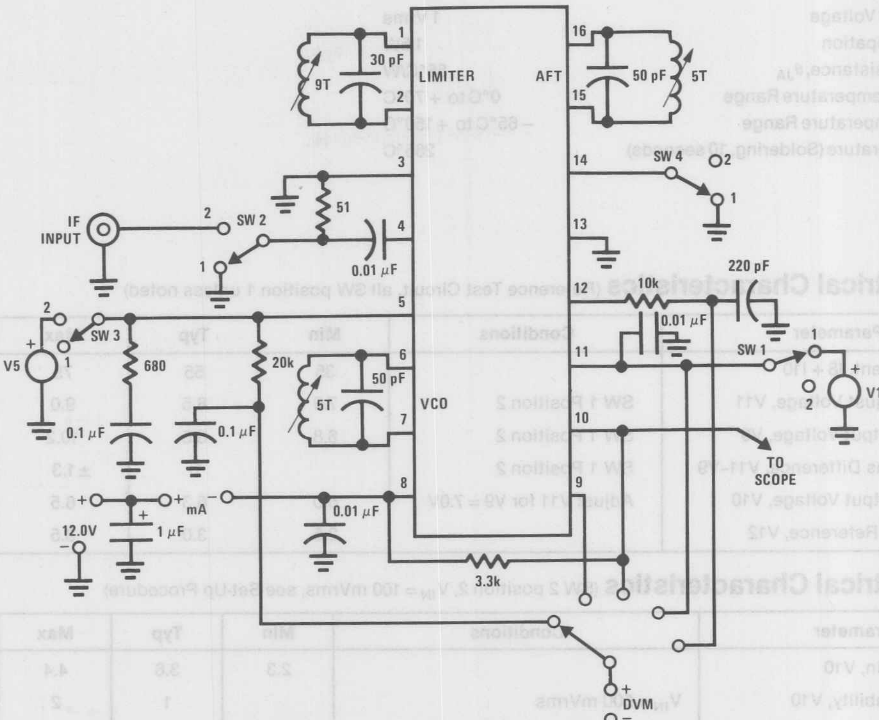
f_{IN} = 45.0 MHz, V_{IN} = 100 mVrms, CW.

a) Monitor pin 10 and adjust VCO tank for DC output, indicating lock. Continue to adjust for V5 = 5.2V.

b) Adjust limiter tank for minimum pin 10 voltage.

c) With SW 4 in position 2, adjust AFT tank for 3V on pin 12.

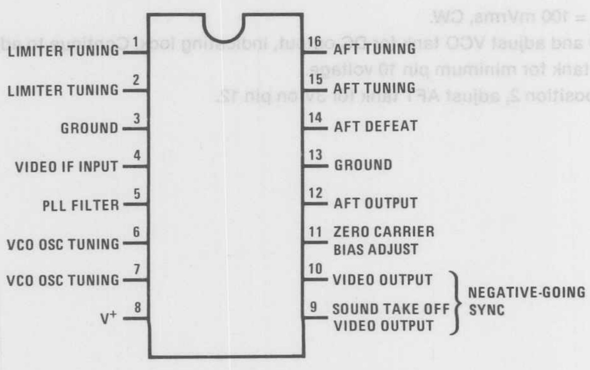
Test Circuit



T indicates # turns on 1/8″ form
High frequency operation requires tight layout

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number LM1821S
See NS Package S16A

National Semiconductor

LM1828, LM1848 Color Television Chroma Demodulator

General Description

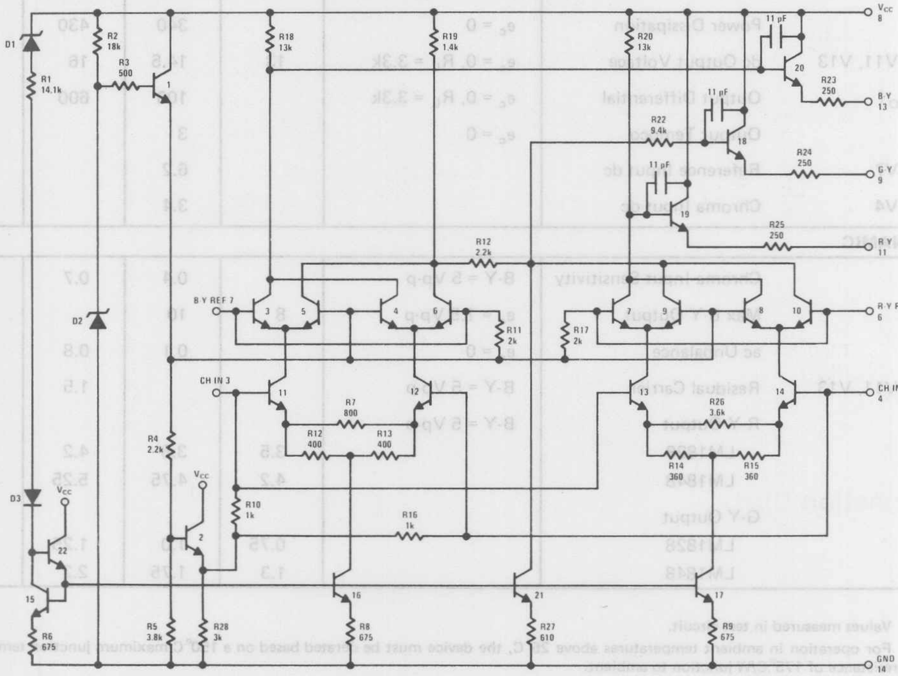
The LM1828, LM1848 are monolithic silicon integrated circuits which demodulate the chroma sub-carrier information contained in a color television video signal and provide color-difference signals at the outputs.

The low dc voltage drift of the outputs insures excellent performance in direct-coupled chrominance output circuitry.

Features

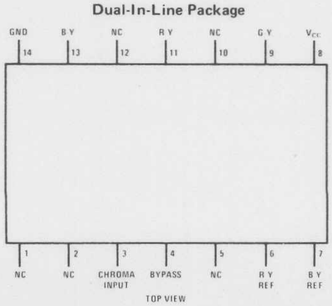
- Low output voltage drift with temperature
- Doubly balanced demodulation
- 10 Vp-p $E_B - E_Y$ output
- Built-in ripple filter capacitors
- Standard matrix in LM1828
- Revised matrix in LM1848
- Pin compatible with LM746, CA3072

Schematic Diagram



Connection Diagram

Dual-In-Line Package



Order Number LM1828N or LM1848N
See NS Package N14A

Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Supply Voltage	30V
Reference Input	5 Vp-p
Chroma Input	5 Vp-p

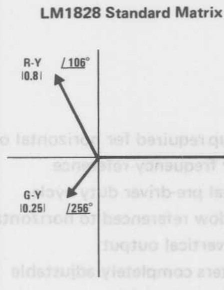
Electrical Characteristics $T_A = 25°C$, $V_{CC} = 24V$, $R_L = 3.3k$, Note 1

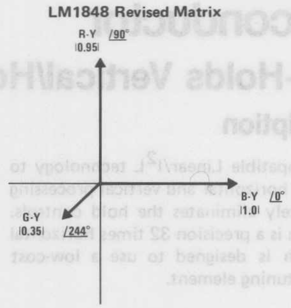
	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC						
I_S	Supply Current	$e_c = 0$, $R_L = 1M$	5.5	9.0	12.5	mA
		$e_c = 0$, $R_L = 3.3k$	16.5	22	25.5	mA
P_D	Power Dissipation	$e_c = 0$		340	430	mW
V9, V11, V13	dc Output Voltage	$e_c = 0$, $R_L = 3.3k$	13	14.5	16	V
$\|\Delta V_O\|$	Output Differential	$e_c = 0$, $R_L = 3.3k$		100	600	mV
	Output Tempco	$e_c = 0$		3		mV/°C
V6, V7	Reference Input dc			6.2		V
V3, V4	Chroma Input dc			3.4		V
DYNAMIC						
e_c	Chroma Input Sensitivity	B-Y = 5 Vp-p		0.4	0.7	Vp-p
V13	Max B-Y Output	$e_c = 1.5$ Vp-p	8	10		Vp-p
	ac Unbalance	$e_c = 0$		0.1	0.8	Vp-p
V9, V11, V13	Residual Carrier	B-Y = 5 Vp-p			1.5	Vp-p
	R-Y Output	B-Y = 5 Vp-p				
	LM1828		3.5	3.8	4.2	Vp-p
	LM1848		4.2	4.75	5.25	Vp-p
	G-Y Output					
	LM1828		0.75	1.0	1.25	Vp-p
	LM1848		1.3	1.75	2.2	Vp-p

Note 1: Values measured in test circuit.

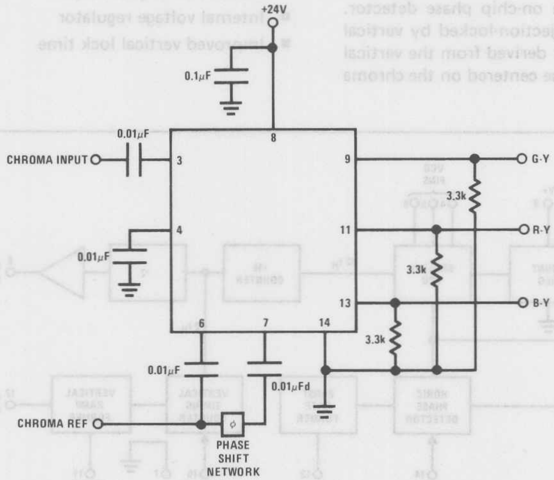
Note 2: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 175°C/W junction to ambient.

Typical Vector Output Diagrams

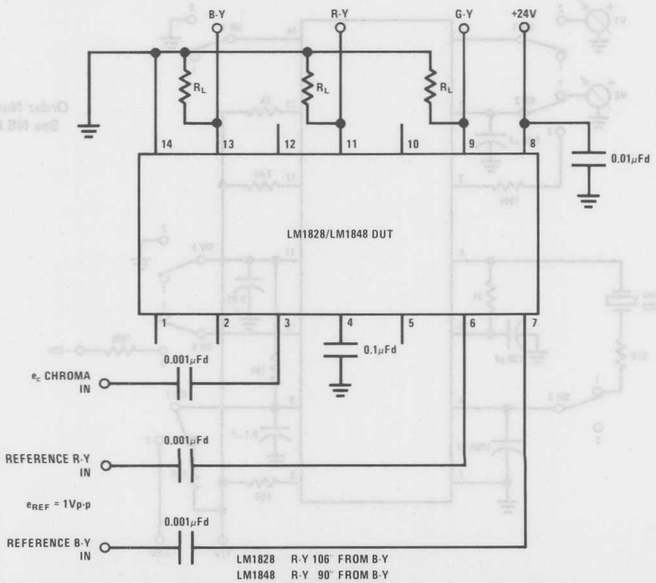




Typical Application



Test Circuit



National Semiconductor

LM1880 No-Holds Vertical/Horizontal

General Description

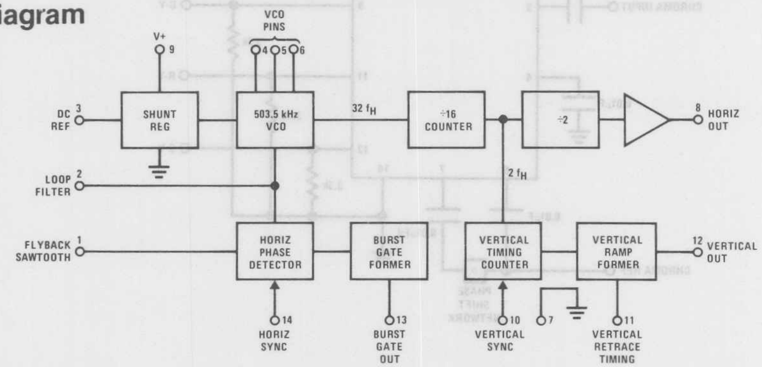
The LM1880 uses compatible Linear/I^2L technology to produce the first T.V. horizontal and vertical processing system which completely eliminates the hold controls. The heart of the system is a precision 32 times horizontal frequency VCO which is designed to use a low-cost ceramic resonator as a tuning element.

The VCO signal is divided down in the horizontal section to produce a pre-driver output which is locked to negative sync by means of an on-chip phase detector. The vertical output ramp is injection-locked by vertical sync subject to a sync window derived from the vertical countdown section. A gate pulse centered on the chroma burst is also provided.

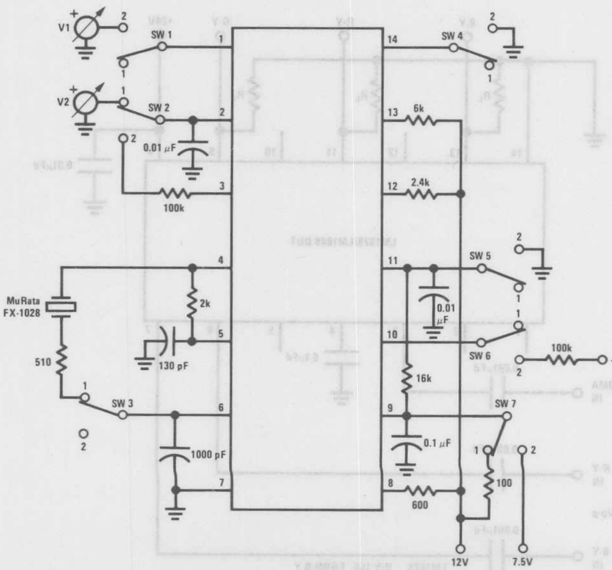
Features

- No frequency set-up required for horizontal or vertical
- Ceramic resonator frequency reference
- Accurate horizontal pre-driver duty cycle
- Vertical sync window referenced to horizontal
- Precise interlaced vertical output
- APC loop parameters completely adjustable
- Vertical retrace time adjustable
- Chroma burst gate output
- Internal voltage regulator
- Improved vertical lock time

Block Diagram



Test Circuit



Order Number LM1880N
See NS Package N14A

Absolute Maximum Ratings

Supply Current (Pin 9)	40 mA
Output Voltage (Pins 8, 12, 13)	12V
Output Current	
Pin 8	50 mA
Pin 12	15 mA
Pin 13	10 mA
Sync. Input Voltage (Pins 10, 14)	5 Vp-p
Sawtooth Input Voltage (Pin 1)	5 Vp-p
Package Dissipation, $T_A = 25^\circ C$	0.83W
Above $T_A = 25^\circ C$, Derate Based on $T_{J(MAX)} = 150^\circ C$ and $\theta_{JA} = 150^\circ C/W$	
Storage Temperature Range	$-55^\circ C$ to $+150^\circ C$
Operating Temperature Range	$0^\circ C$ to $+70^\circ C$
Lead Temperature (Soldering, 10 seconds)	$300^\circ C$

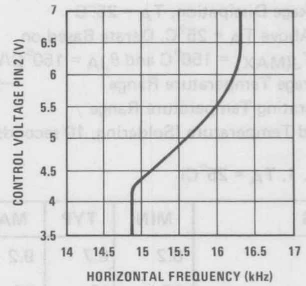
Electrical Characteristics (Test circuit, all SW normally pos. 1, $T_A = 25^\circ C$)

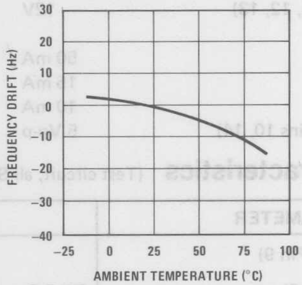
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Regulated Voltage (Pin 9)		8.2	8.7	9.2	V
Supply Current (Pin 9)	SW 7 Pos. 2	12	18	24	mA
VCO Reference Voltage (Pin 3)			5.1		V
VCO Control Current (Pin 2)	V2 = 5V		0.25	1.0	μA
Horizontal Phase Detector Sink Current (Pin 2)	SW 1, SW 4 Pos. 2, V1 = 3.9V, V2 = 5V	0.3	0 5		mA
Horizontal Phase Detector Source Current (Pin 2)	SW 1, SW 4 Pos. 2, V1 = 1.9V, V2 = 5V	0.3	0.5		mA
Horizontal Output Leakage (Pin 8, OFF Condition)	Change SW 3 to Pos. 2 with Pin 8 High			150	μA
Horizontal Output Saturation Voltage (Pin 8, ON Condition)	Change SW 3 to Pos. 2 with Pin 8 Low		0.15	0.4	V
Vertical Output Saturation Voltage (Pin 12)	SW 3, SW 5 Pos. 2		0.25	0.5	V
Burst Gate Saturation Voltage (Pin 13)	SW 1, SW 4 Pos. 2, V1 = 1.9V		0.15	0.4	V
Horizontal Oscillator Free-Running Frequency (Pin 8), (Note 1)	SW 2 Pos. 2	15,550	15,750	15,950	Hz
Horizontal Oscillator Maximum Frequency (Pin 8)	V2 = 7V	16,300			Hz
Horizontal Oscillator Minimum Frequency (Pin 8)	V2 = 3V			15,150	Hz
Vertical Minimum Lock Frequency (Pin 12)	$f_H = 15{,}734$ Hz			55.0	Hz
Vertical Maximum Lock Frequency (Pin 12)	SW 6 Pos. 2, $f_H = 15{,}734$ Hz	61.7			Hz

Note 1: Assumes ceramic resonator $f_R = 503.48$ kHz.

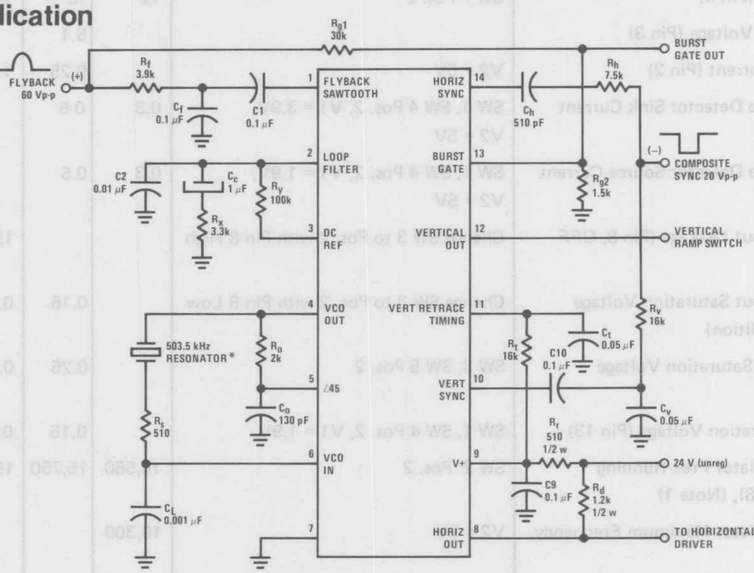
Design Parameters (Application Circuit)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Horizontal Pull-In Range			±600		Hz
Horizontal Static Phase Error (S.P.E.)	$\Delta f_H = \pm 600$ Hz		±0.5		μs
Horizontal Output Duty Cycle			50		%
Horizontal Oscillator Supply Sensitivity			−1		Hz/V
Vertical Output Retrace Time			600		μs
Burst Gate Width	Flyback Width = 12 μs		5		μs





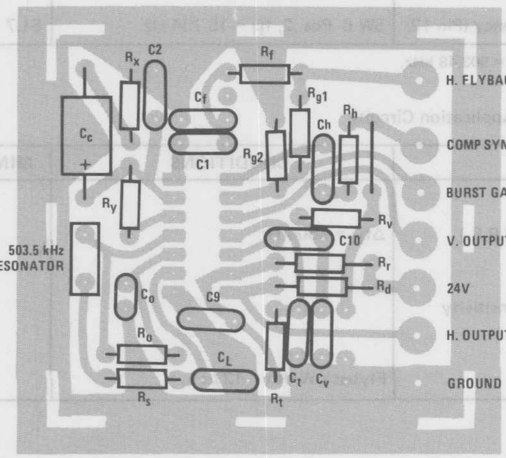
Typical Application



*MuRata Corporation of America, Part No. FX-1028, Vernitron Corp. VTFA3-01-503.5

Printed Circuit Layout

(COMPONENT SIDE)



External Components (Application Circuit)

Component	Typical Value	Comments
R_{g1}	30k	Burst Gate series resistor.
R_{g2}	1.5k	Burst Gate shunt resistor, works with R_{g1} to divide flyback pulse and set Burst Gate amplitude. $V_{B.G.\ pk} = \frac{R_{g2}}{R_{g1} + R_{g2}} V_{FLYBACK}$
R_f	3.9k	Flyback Sawtooth integrator resistor, works with C_f to integrate flyback pulse to 1 Vp-p min sawtooth. For C_f = 0.1 μF, $V_{SAW\ p\text{-}p} \simeq \frac{85\ V_{FLYBACK}}{R_f}$
C_f	0.1 μF	Flyback Sawtooth integrator capacitor.
C1	0.1 μF	Sawtooth input coupling capacitor.
R_h	7.5k	Horizontal Sync input coupling resistor. $R_h = 0.4 \times V_{SYNC\ p\text{-}p}\ k\Omega$
C_h	510 pF	Horizontal Sync input coupling capacitor, blocks vertical sync components.
R_v	16k	Vertical sync input integrator resistor.
C_v	0.05 μF	Vertical sync input integrator capacitor, works with R_v to integrate composite sync to −2 Vp-p min pulse. For N.T.S.C. sync, Vert. sync $\simeq \frac{1.4 \times 10^{-4}}{R_v C_v}$ (Comp. sync) Vp-p
C10	0.1 μF	Vertical sync coupling capacitor.
R_t	16k	Vertical Retrace timing resistor.
C_t	0.05 μF	Vertical Retrace timing capacitor, works with R_t to determine ON time of vertical ramp switch at pin 12. $t_{V.\ RETRACE} \simeq 0.75\ R_t C_t$ sec.
R_o	2k	Oscillator phase shift resistor.
C_o	130 pF	Works with R_o to produce 45° lag required by VCO phase shifter.
R_s	510 Ω	Defines Q of ceramic resonator tuned network, which affects VCO control curve.
C_L	1000pF	Completes VCO loop with phase lag, required to sustain oscillation and suppress resonator overtones.
R_r	510 Ω	Series resistor to device supply pin 9. Must supply sufficient current to activate internal shunt regulator. $R_r = \frac{V_{(unreg)} - 9V}{0.03}\ \Omega$
C9	0.1 μF	Device supply decoupling capacitor.
R_d	1.2k	Horizontal pre-driver output resistor, supplies base current to Horizontal driver transistor when pin 8 is OFF.
C2	0.01 μF	Horizontal APC loop filter high frequency roll-off. C2 also prevents signal on loop filter from saturating phase detector output.
R_x	3.3k	R_x, R_y and C_c form the Horizontal APC loop filter. See Applications Information to modify loop parameters.
R_y	100k	
C_c	1 μF	

Applications Information

I. VERTICAL COUNTER

The vertical counter in the LM1880 replaces the conventional vertical oscillator in a television reciever. The vertical lock-in range is governed by the width of the vertical sync window, which opens from count 510 to count 542 following a vertical reset. The vertical lock frequencies are referenced to twice horizontal frequency to insure interlaced vertical and horizontal outputs. For f_{HORIZ} = 15,734 Hz, the vertical lock frequencies are calculated as follows:

$$f_{V.HIGH} = \frac{2\ (15{,}734)}{510} = 61.7\ \text{Hz.}$$

$$f_{V.LOW} = \frac{2\ (15{,}734)}{542} = 58\ \text{Hz.}$$

In virtually all standard and non-standard sync signals the vertical sync is also derived from the horizontal, so that as long as the horizontal sync frequency is within the pull-in range of the LM1880 (approximately ±600 Hz), the vertical lock window will remain centered on the vertical sync. Thus, the effective vertical lock range is increased by the horizontal APC:

$$f_{V.HIGH\ (EFF)} = \frac{2\ (15{,}734 + 600)}{510} = 64\ \text{Hz.}$$

$$f_{V.LOW\ (EFF)} = \frac{2\ (15{,}734 - 600)}{542} = 55.8\ \text{Hz.}$$

The time required for the vertical to "roll-thru" and lock is a function of the difference frequency and relative phase of $f_{V.LOW}$ and the vertical sync:

$$t_{ROLL\text{-}THRU\ (AVG)} = \frac{1}{2}\ \frac{1}{60 - 58\ \text{Hz}} = 250\ \text{ms}$$

II. HORIZONTAL APC LOOP PARAMETERS

The following information is given to provide a basis for modifying the filter to achieve the desired loop performance. Although the VCO is actually running at 503.5 kHz, for convenience all parameters are referenced to the actual horizontal output frequency at pin 8.

DC Loop Gain

The DC loop gain is the product of the phase detector conversion gain (μ) and the VCO sensitivity (β). For the typical application circuit,

$\mu = 1.6 \times 10^{-4}\ R_y$ V/Rad
and
β = 800 Hz/V
$\mu\beta = 0.13\ R_y$ Hz/Rad
for $R_y = 100\ k\Omega$, $\mu\beta$ = 13,000 Hz/Rad

In order to determine static phase error (S.P.E.), the loop gain may be expressed in Hz/μs:

$$\mu\beta = \frac{13{,}000 \times 2\pi}{63.5\ \mu s} = 1{,}286\ \text{Hz}/\mu s$$

For comparison, this value is nearly double the loop gain of the LM1391. The increased loop gain (reduced phase error) guarantees accurate centering of the burst gate pulse on pin 13 of the LM1880.

The following equations cover AC loop parameters of interest:

Noise Bandwidth

$$f_{NN} \cong \frac{1 + 2\pi\ (R_x^2/R_y)\ C_C\ \mu\beta}{4R_xC_C}\ \text{Hz}$$

Damping Factor

$$K \cong \frac{\pi}{2}\ \frac{R_x^2}{R_y}\ C_C\ \mu\beta$$

Pull-In Range

The pull-in and hold-in range of the LM1880 horizontal APC loop are directly determined by the VCO control range. Thus the loop would be capable of pulling the VCO further than ±600 Hz, but it has well defined frequency limits which prevent it from doing so. As a result of these built-in "stops", the loop parameters may be varied over a large range without affecting pull-in performance.

The VCO control range, and hence pull-in, can be modified to some extent by varying the Q of the ceramic resonator with resistor R_s:

Incr. $R_s \rightarrow$ Incr. Pull-in
Reduce $R_s \rightarrow$ Reduce Pull-in

However, because of the non-linearity of the resonator, R_s has a much greater effect on the negative side pull-in than the positive side.

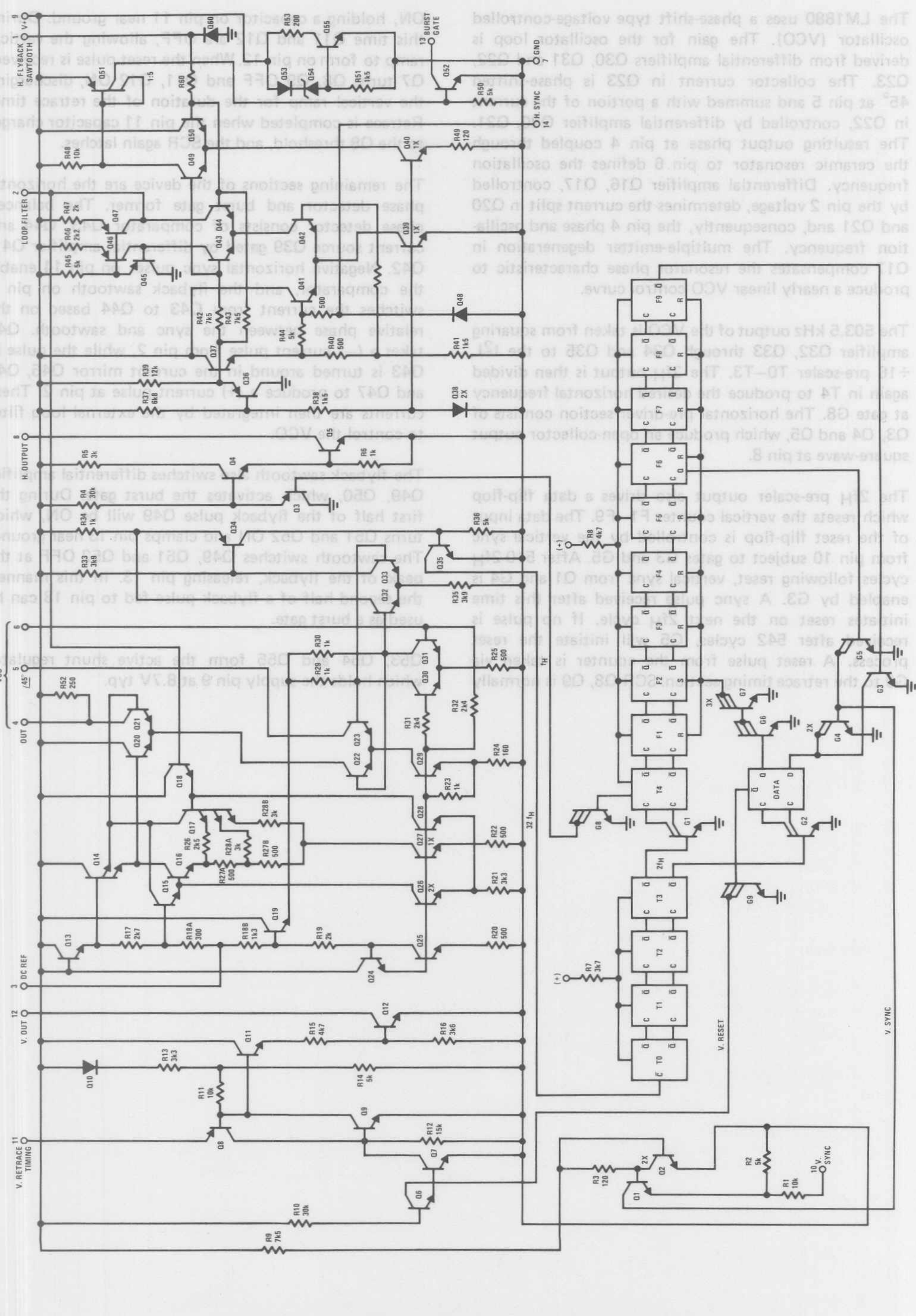
III. LAYOUT NOTES

Since the LM1880 uses a counter to derive the horizontal frequency, care must be taken to prevent extraneous signals from the horizontal driver and output stages from feeding back to the VCO where they could cause false counts and consequent severe phase jitter. The following guidelines will prevent this problem from occurring:

A. Keep the VCO feedback capacitor, C_L, as close as possible to device pins 6 and 7.

B. Limit the lead length on the horizontal output pin 8. If a long line is required to the driver base, isolate it with a small series resistor (200–300Ω) next to pin 8.

Schematic Diagram



Circuit Description (See Schematic Diagram)

The LM1880 uses a phase-shift type voltage-controlled oscillator (VCO). The gain for the oscillator loop is derived from differential amplifiers Q30, Q31 and Q22, Q23. The collector current in Q23 is phase-shifted 45° at pin 5 and summed with a portion of the current in Q22, controlled by differential amplifier Q20, Q21. The resulting output phase at pin 4 coupled through the ceramic resonator to pin 6 defines the oscillation frequency. Differential amplifier Q16, Q17, controlled by the pin 2 voltage, determines the current split in Q20 and Q21 and, consequently, the pin 4 phase and oscillation frequency. The multiple-emitter degeneration in Q17 compensates the resonator phase characteristic to produce a nearly linear VCO control curve.

The 503.5 kHz output of the VCO is taken from squaring amplifier Q32, Q33 through Q34 and Q35 to the I^2L ÷16 pre-scaler T0–T3. The $2f_H$ output is then divided again in T4 to produce the desired horizontal frequency at gate G8. The horizontal pre-driver section consists of Q3, Q4 and Q5, which produce an open-collector output square-wave at pin 8.

The $2f_H$ pre-scaler output also drives a data flip-flop which resets the vertical counter F1–F9. The data input of the reset flip-flop is controlled by the vertical sync from pin 10 subject to gates G3 and G5. After 510 $2f_H$ cycles following reset, vertical sync from Q1 and G4 is enabled by G3. A sync pulse received after this time initiates reset on the next $2f_H$ cycle. If no pulse is received after 542 cycles, G5 will initiate the reset process. A reset pulse from the counter is taken via G9 to the retrace timing section. SCR Q8, Q9 is normally ON, holding a capacitor on pin 11 near ground. During this time Q11 and Q12 are OFF, allowing the vertical ramp to form on pin 12. When the reset pulse is received, Q7 turns Q8, Q9 OFF and Q11, Q12 ON, discharging the vertical ramp for the duration of the retrace time. Retrace is completed when the pin 11 capacitor charges to the Q8 threshold, and the SCR again latches.

The remaining sections of the device are the horizontal phase detector and burst gate former. The balanced phase detector consists of comparator Q43, Q44 and current source Q39 gated by differential amplifier Q41, Q42. Negative horizontal sync pulses on pin 14 enable the comparator, and the flyback sawtooth on pin 1 switches the current from Q43 to Q44 based on the relative phase between the sync and sawtooth. Q44 takes a (–) current pulse from pin 2, while the pulse in Q43 is turned around in the current mirror Q45, Q46 and Q47 to produce a (+) current pulse at pin 2. These currents are then integrated by the external loop filter to control the VCO.

The flyback sawtooth also switches differential amplifier Q49, Q50, which activates the burst gate. During the first half of the flyback pulse Q49 will be ON, which turns Q51 and Q52 ON and clamps pin 13 near ground. The sawtooth switches Q49, Q51 and Q52 OFF at the peak of the flyback, releasing pin 13. In this manner, the second half of a flyback pulse fed to pin 13 can be used as a burst gate.

Q53, Q54 and Q55 form the active shunt regulator which holds the supply pin 9 at 8.7V typ.

National Semiconductor

LM1886 TV Video Matrix D to A

General Description

The LM1886 is a TV video matrix D to A converter which encodes luminance and color difference signals from 3-bit red, green and blue inputs. The luminance output is encoded from the NTSC equation Y = 0.3R + 0.59G + 0.11B and the R-Y and B-Y outputs are weighted to prevent over-modulation. A built-in R-Y and burst gate polarity switch allow European PAL compatible signals to be encoded. All output levels including an RF O Carrier Bias Voltage have been referenced to 5V for direct connection to the LM1889 TV video modulator. When used in combination with the LM1889 and a suitable sync generator, 3-bit R, G and B information may be encoded to both composite video and RF channel carrier.

Features

- Complete digital to RF encoding with LM1889
- 1-pin PAL/NTSC mode select
- True NTSC matrix
- 8 levels of grey scale
- Allows wide range of colorimetry
- Low power TTL inputs
- Wideband luminance output
- Weighted R-Y, B-Y outputs

Connection Diagram

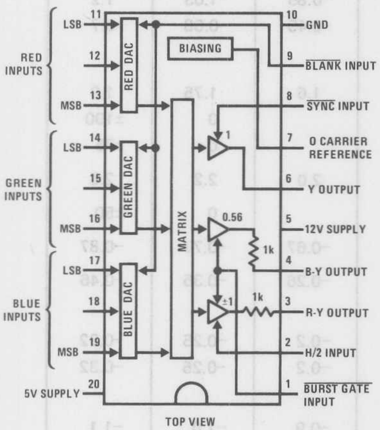


FIGURE 1

Order Number LM1886N
See NS Package N20A

Test Circuits

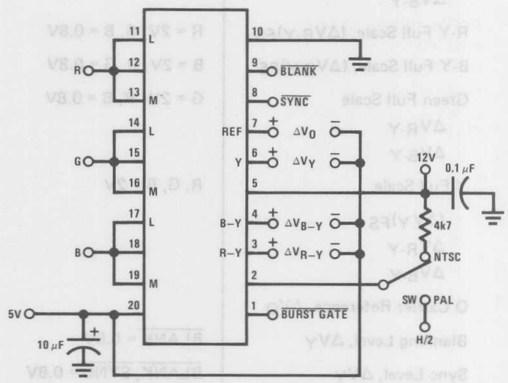


FIGURE 2a. 6-Color Input Connection

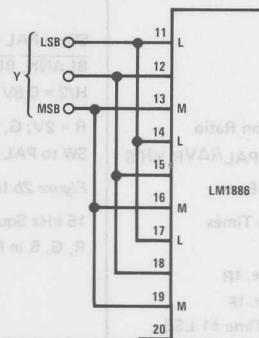


FIGURE 2b. 8-Level Grey Scale Input Connection

Absolute Maximum Ratings

Supply Voltage	
Pin 5	15V
Pin 20	6V
Input Voltage (Pins 1, 8, 9, 11–19)	−0.5V, +12V
Pin 2 Voltage Relative to Pin 20	0.8V
Output Current	5 mA
Power Dissipation, $T_A = 25^\circ C$ (Note 1)	1.67 W
Storage Temperature Range	−55°C to +150°C
Operating Temperature Range	0°C to 70°C
Lead Temperature (Soldering, 10 seconds)	300°C

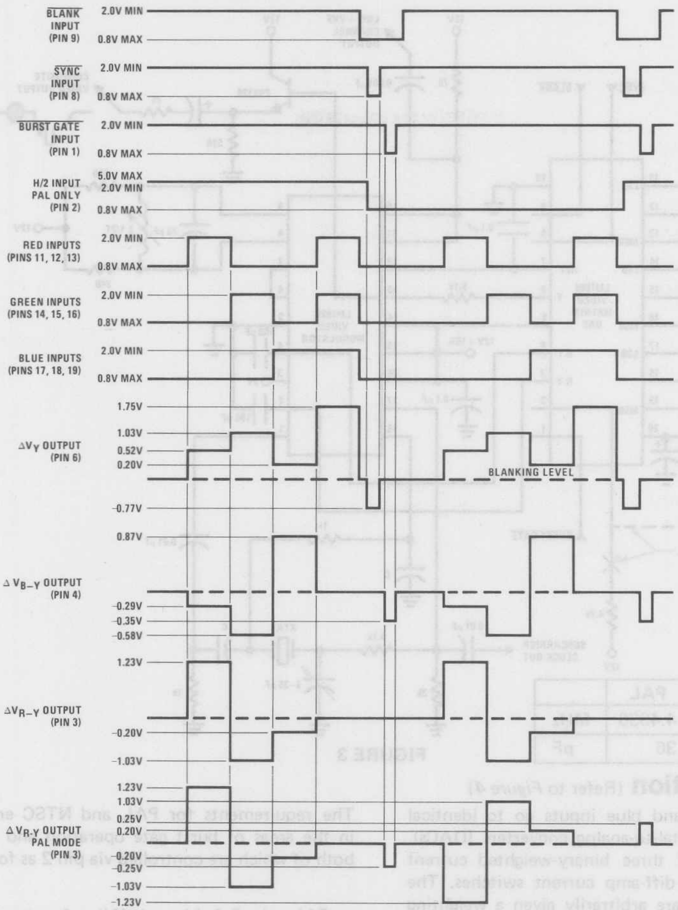
Electrical Characteristics $T_A = 25^\circ C$, (*Figure 2*, Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
5V Supply Current (Pin 20)	$\overline{\text{BLANK}}$ = 0.8V	7	11	16	mA
12V Supply Current (Pin 5)	$\overline{\text{BLANK}}$ = 0.8V	9	13	17	mA
Logic "1" Input Current (Pins 1, 2, 8, 9, 11–19)	Input Voltage = 5.0V		0	10	μA
Logic "0" Input Current (Pins 1, 2, 8, 9, 11–19)	Input Voltage = 0.3V		−0.01	−0.18	mA
Output Offsets	R, G, B = 0.8V				
ΔV_Y			0	±50	mV
$\Delta V_{R\text{-}Y}$			0	±50	mV
$\Delta V_{B\text{-}Y}$			0	±50	mV
R-Y Full Scale, $(\Delta V_{R\text{-}Y})_{FS}$	R = 2V; G, B = 0.8V	1.0	1.23	1.4	V
B-Y Full Scale, $(\Delta V_{B\text{-}Y})_{FS}$	B = 2V; R, G = 0.8V	0.7	0.87	1.0	V
Green Full Scale	G = 2V; R, B = 0.8V				
$\Delta V_{R\text{-}Y}$		−0.85	−1.03	−1.2	V
$\Delta V_{B\text{-}Y}$		−0.45	−0.58	−0.7	V
Y Full Scale	R, G, B = 2V				
$(\Delta V_Y)_{FS}$		1.6	1.75	1.9	V
$\Delta V_{R\text{-}Y}$			0	±100	mV
$\Delta V_{B\text{-}Y}$			0	±75	mV
O Carrier Reference, ΔV_O		2.0	2.2	2.5	V
Blanking Level, ΔV_Y	$\overline{\text{BLANK}}$ = 0.8V		0	±50	mV
Sync Level, ΔV_Y	$\overline{\text{BLANK}}$, $\overline{\text{SYNC}}$ = 0.8V	−0.67	−0.77	−0.87	V
NTSC Burst, $\Delta V_{B\text{-}Y}$	$\overline{\text{BLANK}}$, $\overline{\text{BURST GATE}}$ = 0.8V	−0.26	−0.35	−0.46	V
PAL Burst					
$\Delta V_{R\text{-}Y}$	SW in PAL Position;	−0.2	−0.25	−0.32	V
$\Delta V_{B\text{-}Y}$	$\overline{\text{BLANK}}$, $\overline{\text{BURST GATE}}$, H/2 = 0.8V	−0.2	−0.25	−0.32	V
PAL Inversion Ratio $(\Delta V_{R\text{-}Y})_{PAL}/(\Delta V_{R\text{-}Y})_{FS}$	R = 2V; G, B, H/2 = 0.8V SW to PAL Position	−0.9	−1.0	−1.1	
Y Linearity Error	*Figure 2b* Input Connection		±1	±6	%FS
Y Switching Times	15 kHz Square Wave Switching R, G, B in Parallel				
Rise Time, t_R			35		ns
Fall Time, t_F			30		ns
Settling Time ±1 LSB			50		ns

Note 1: Above $T_A = 25^\circ C$, derate based on $T_{J(MAX)} = 150^\circ C$ and $\theta_{JA} = 75^\circ C/W$.

Note 2: Unless otherwise noted, $\overline{\text{BLANK}}$, $\overline{\text{SYNC}}$, $\overline{\text{BURST GATE}}$ = 2V and SW is in NTSC position. All outputs are referenced to the +5V supply as shown in *Figure 2a*.

Typical Input and Output Waveforms



Application Notes (Refer to *Figure 3*)

SYNC, BLANK, and BURST GATE may be obtained from a sync generator IC similar to MM5320 or MM5321. For PAL operation, the H/2 square wave may be obtained by a ÷2 from horizontal sync.

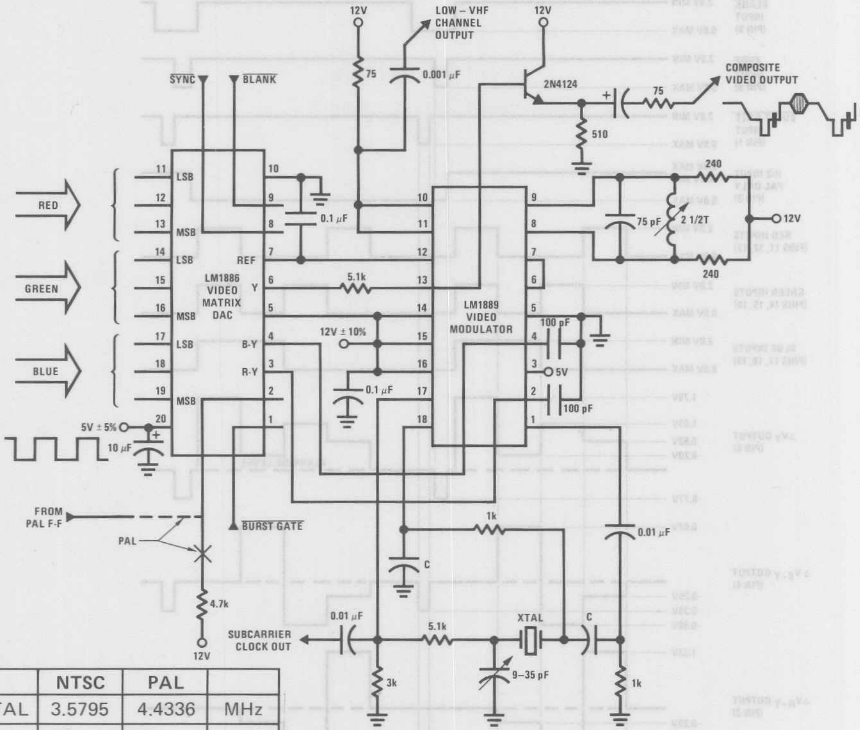
All inputs are low-power TTL compatible. Because of the very low typical input currents, the color inputs may be paralleled in various combinations. For simple color requirements, the *Figure 2a* input connection may be used to produce the 6 primary and complementary colors listed in Table I, along with black and white. To add complex colors such as those at the bottom of Table I, all 9 input bits may be required separately. When choosing input codes for other colors, always check the new color against both light and dark backgrounds.

All outputs are referenced to the +5V supply for direct connection to the LM1889. The resistor on the luminance output pin 6 is used to sum the chroma subcarrier from the LM1889 and must be wired as tightly as possible to preserve the video bandwidth. For the addition of sound or a second RF channel, refer to the LM1889 data sheet.

TABLE I. INPUT CODE EXAMPLES FOR COMMON COLORS

		INPUT CODE		
		RED	GREEN	BLUE
	COLOR	M L	M L	M L
	Black	0 0 0	0 0 0	0 0 0
	Dark Grey	0 1 0	0 1 0	0 1 0
	Light Grey	1 0 1	1 0 1	1 0 1
	White	1 1 1	1 1 1	1 1 1
Primary	Red	1 1 1	0 0 0	0 0 0
Primary	Green	0 0 0	1 1 1	0 0 0
Primary	Blue	0 0 0	0 0 0	1 1 1
Complementary	Cyan	0 0 0	1 1 1	1 1 1
Complementary	Magenta	1 1 1	0 0 0	1 1 1
Complementary	Yellow	1 1 1	1 1 1	0 0 0
	Brown	0 1 1	0 1 1	0 0 0
	Orange	1 1 1	1 0 0	0 0 0
	Flesh tone	1 1 1	1 1 0	1 0 1
	Pink	1 1 1	1 1 0	1 1 0
	Sky Blue	1 0 1	1 0 1	1 1 1

Typical Application



	NTSC	PAL	
XTAL	3.5795	4.4336	MHz
C	43	36	pF

FIGURE 3

Circuit Description (Refer to *Figure 4*)

The 3-bit red, green, and blue inputs go to identical 3-bit current-mode digital-to-analog converters (DACs). Each DAC consists of three binary-weighted current sources controlled by diff-amp current switches. The DAC output currents are arbitrarily given a weighting factor of 0.59, which is the green coefficient in the luminance equation. Portions of the red and blue currents are split off, so that the remaining currents combined with the green current form the luminance current $I_Y = 0.3\ I_R + 0.59\ I_G + 0.11\ I_B$. I_Y develops the luminance voltage V_Y across R_O in a summing amplifier referenced to the +5V supply. A current switch operated by pin 8 adds (−) sync pulses to the Y output at pin 6.

The portions of red and blue currents previously split off flow through resistors $R_O/0.29$ and $R_O/0.48$, which are weighted to form the red and blue voltages respectively. Since the opposite ends of the 2 resistors are connected to V_Y, the red and blue voltages across the resistors subtract from V_Y to develop the color difference voltages $V_{Y\text{-}R}$ and $V_{Y\text{-}B}$. $V_{Y\text{-}B}$ is coupled through a X.56 gain, 5V-referenced inverting amplifier to the B-Y output at pin 4. $V_{Y\text{-}R}$ feeds parallel inverting and non-inverting unity gain amplifiers which allow either polarity to be coupled to the R-Y output pin 3. Switching between the 2 amplifiers is controlled by a current switch activated by the H/2 pin 2. A (−) burst gate pulse on pin 1 controls current switches which add the burst pulse components to the B-Y and R-Y outputs.

The requirements for PAL and NTSC encoding differ in the areas of burst gate operation and R-Y polarity, both of which are controlled via pin 2 as follows:

PAL, pin 2 fed by a half-line frequency TTL square wave—in this mode a PNP switch between pin 2 and +5V is held off continuously, which results in equal burst pulse components on the B-Y and R-Y outputs. In addition, the H/2 square wave causes the R-Y output polarity to reverse every line. (When fed to the LM1889 chroma modulator this causes the phase of the R-Y subcarrier to change 180° as required in PAL.)

NTSC, pin 2 tied through an external resistor to +12V—this turns on the PNP switch continuously, which eliminates the burst pulse on the R-Y output and increases the amplitude of the B-Y pulse. Since pin 2 is being held high, the R-Y output is locked in the positive polarity.

Blanking is activated by a low on pin 9, which de-biases the left side of the DAC diff-amps, so that $I_R = I_G = I_B = 0$ independent of the input states. When blanked, the Y, B-Y and R-Y outputs all go to +5V. An additional amplifier produces a 0 carrier reference voltage at pin 7 which is 25% above the peak white voltage on the Y output, relative to +5V.

Equivalent Schematic

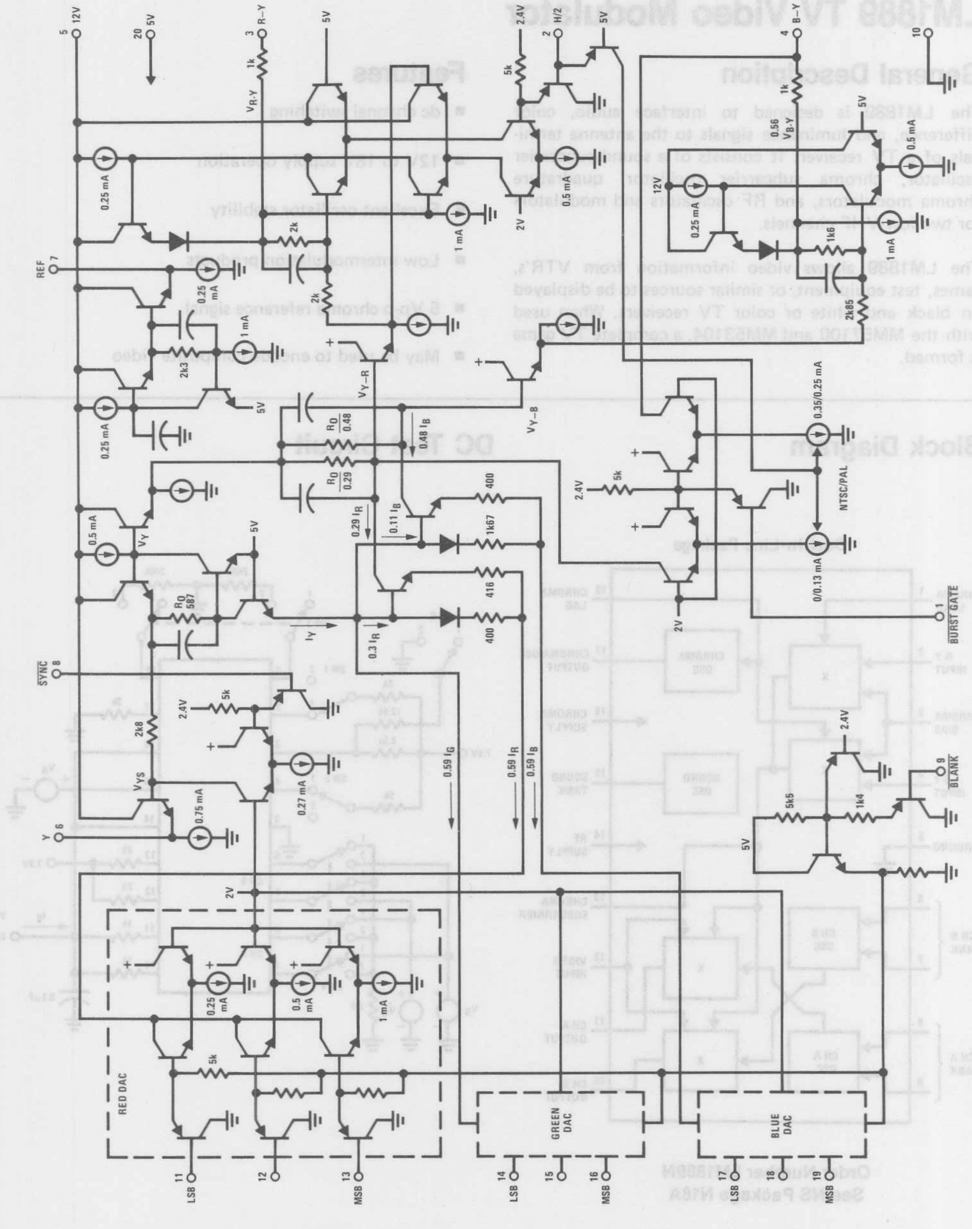


FIGURE 4. LM1886 Equivalent Schematic

National Semiconductor

LM1889 TV Video Modulator

General Description

The LM1889 is designed to interface audio, color difference, and luminance signals to the antenna terminals of a TV receiver. It consists of a sound subcarrier oscillator, chroma subcarrier oscillator, quadrature chroma modulators, and RF oscillators and modulators for two low-VHF channels.

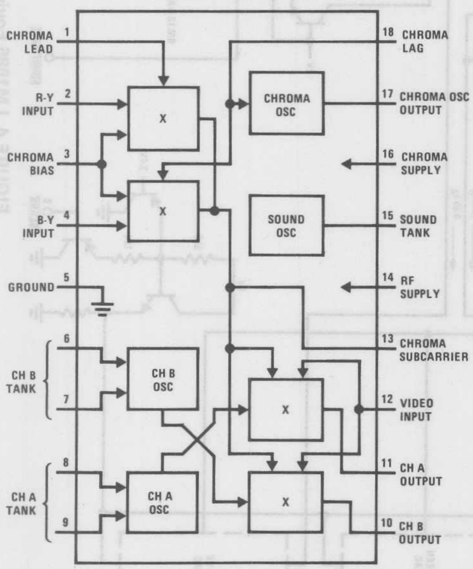
The LM1889 allows video information from VTR's, games, test equipment, or similar sources to be displayed on black and white or color TV receivers. When used with the MM57100 and MM53104, a complete TV game is formed.

Features

- dc channel switching
- 12V to 18V supply operation
- Excellent oscillator stability
- Low intermodulation products
- 5 Vp-p chroma reference signal
- May be used to encode composite video

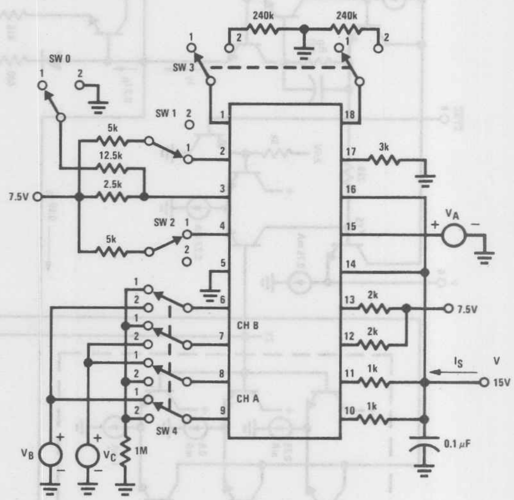
Block Diagram

Dual-In-Line Package



Order Number LM1889N
See NS Package N18A

DC Test Circuit



Absolute Maximum Ratings

Supply Voltage V14, V16 max	19 V_{dc}
Power Dissipation Package (Note 1)	1390 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Chroma Osc Current I_{17} max	10 mA_{dc}
(V16−V15) max	±5 V_{dc}
(V14−V10) max	7V
(V14−V11) max	7V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics (dc Test Circuit, All SW Normally Pos. 1, V_A = 15V, V_B = V_C = 12V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current, I_S		20	35	45	mA
Sound Oscillator, Current Change, ΔI_{15}	Change V_A From 12.5V to 17.5V	0.3	0.6	0.9	mA
Chroma Oscillator Balance, V17		9.5	11.0	12.5	V
Chroma Modulator Balance, V13		7.0	7.4	7.8	V
R-Y Modulator Output Level, ΔV13	SW 3, Pos. 2, Change SW 1 From Pos. 1 to Pos. 2	0.6	0.9	1.2	V
B-Y Modulator Output Level, ΔV13	SW 3, Pos. 2, Change SW 2 From Pos. 1 to Pos. 2	0.6	0.9	1.2	V
Chroma Modulator Conversion Ratio, ΔV13/ΔV3	SW 3, Pos. 2, Change SW 0 From Pos. 1 to Pos. 2. Divide ΔV13 by ΔV3	0.45	0.70	0.95	V/V
Ch. A Oscillator "OFF" Voltage, V8, V9	SW 4, Pos. 2	0.5	1.5	3.0	V
Ch. A Oscillator Current Level, I_9	V_B = 12V, V_C = 13V	2.5	3.5	5	mA
Ch. B Oscillator "OFF" Voltage, V6, V7		0.5	1.5	3.0	V
Ch. B Oscillator Current Level, I_6	SW 4, Pos. 2, V_B = 12V, V_C = 13V	2.5	3.5	5	mA
Ch. A Modulator Conversion Ratio, ΔV11/(V13−V12)	SW 1, SW 2, SW 3, Pos. 2, V_B = 12V, Change V_C From 13V to 11V For ΔV11 Divide By V13−V12	0.35	0.55	0.75	V/V
Ch. B Modulator Conversion Ratio, ΔV10/(V13−V12)	All SW, Pos. 2, V_B = 12V, Change V_C From 13V to 11V Divide as Above	0.35	0.55	0.75	V/V

AC Electrical Characteristics (ac Test Circuit, V = 15V)

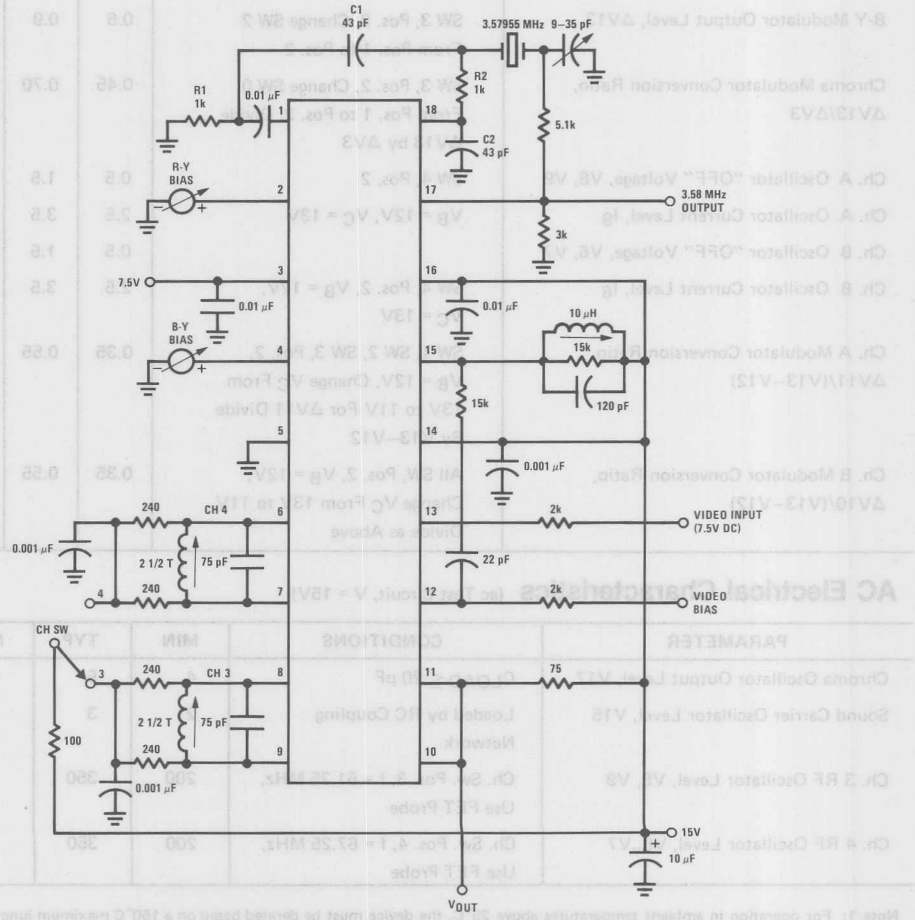
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Chroma Oscillator Output Level, V17	$C_{LOAD} \leq 20$ pF	4	5		Vp-p
Sound Carrier Oscillator Level, V15	Loaded by RC Coupling Network	2	3	4	Vp-p
Ch. 3 RF Oscillator Level, V8, V9	Ch. Sw. Pos. 3, f = 61.25 MHz, Use FET Probe	200	350		mVp-p
Ch. 4 RF Oscillator Level, V6, V7	Ch. Sw. Pos. 4, f = 67.25 MHz, Use FET Probe	200	350		mVp-p

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 90°C/W junction to ambient.

Chroma, f_o = 3.579545 MHz	3	Hz/V
Sound Carrier, RF	See Curves	
Oscillator Temperature Dependence (IC Only)		
Chroma	0.05	ppm/°C
Sound Carrier	−15	ppm/°C
RF	−50	ppm/°C
Chroma Oscillator Output, Pin 17		
t_{RISE}, 10–90%	20	ns
t_{FALL}, 90–10%	30	ns
Duty Cycle (+) Half Cycle	51	%
(−) Half Cycle	49	%
RF Oscillator Maximum Operating Frequency (Temperature Stability Degraded)	100	MHz
Chroma Modulator (f = 3.58 MHz)		
B-Y Conversion Gain V13/(V4−V3)	0.6	Vp-p/V
R-Y Conversion Gain V13/(V2−V3)	0.6	Vp-p/V
Gain Balance	±0.5	dB
Bandwidth	See Curve	

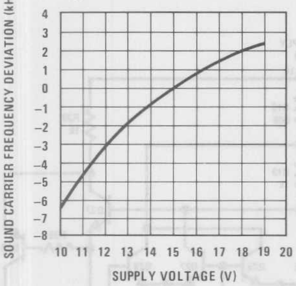
RF Modulator		
Conversion Gain, f = 61.25 MHz, V_{OUT}/(V13−V12)	10	mVrms/V
3.58 MHz Differential Gain	5	%
Differential Phase	3	degrees
2.5 Vp-p Video, 87.5% mod.		
Output Harmonics Below Carrier		
2nd, 3rd	−12	dB
4th and above	−20	dB
Input Impedances		
Chroma Modulator, Pins 2, 4	500k//2 pF	
RF Modulator, Pin 12	1M//2 pF	
Pin 13	250k//3.5 pF	

AC Test Circuit

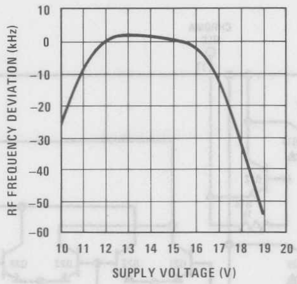


Typical Performance Characteristics

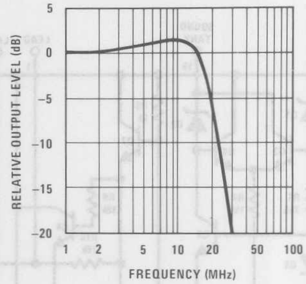
Sound Carrier Oscillator
Supply Dependence
(f_o = 4.5 MHz)



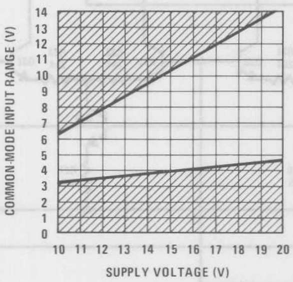
RF Oscillator Frequency
Supply Dependence
f_o = 67.25 MHz



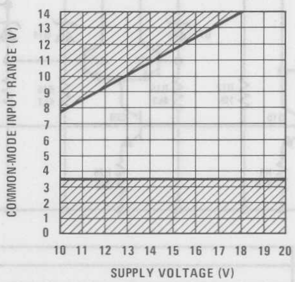
Chroma Modulator
Transconductance Bandwidth
$I_{OUT\ 13}/V1$ or 18



Chroma Modulator
Common-Mode Input Range
Pins 2, 3, 4



RF Modulator
Common-Mode Input Range
Pins 12, 13 (Applications Circuit)



Circuit Description (Refer to Circuit Diagram)

The sound carrier oscillator is formed by differential amplifier Q3, Q4 operated with positive feedback from the pin 15 tank to the base of Q4.

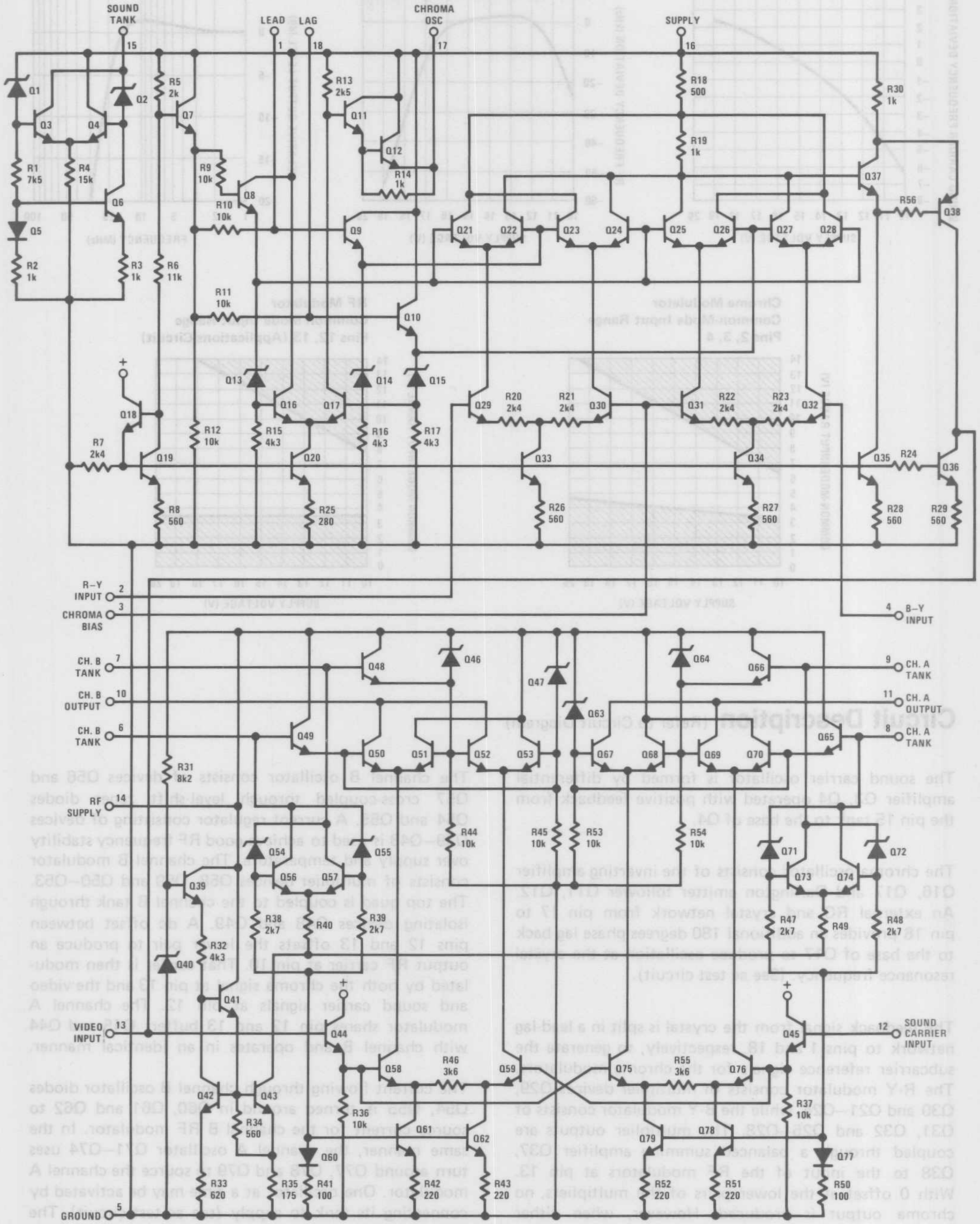
The chroma oscillator consists of the inverting amplifier Q16, Q17 and Darlington emitter follower Q11, Q12. An external RC and crystal network from pin 17 to pin 18 provides an additional 180 degrees phase lag back to the base of Q17 to produce oscillation at the crystal resonance frequency. (See ac test circuit).

The feedback signal from the crystal is split in a lead-lag network to pins 1 and 18, respectively, to generate the subcarrier reference signals for the chroma modulators. The R-Y modulator consists of multiplier devices Q29, Q30 and Q21–Q24, while the B-Y modulator consists of Q31, Q32 and Q25–Q28. The multiplier outputs are coupled through a balanced summing amplifier Q37, Q38 to the input of the RF modulators at pin 13. With 0 offset at the lower pairs of the multipliers, no chroma output is produced. However, when either pin 2 or pin 4 is offset relative to pin 3 a subcarrier output current of the appropriate phase is produced at pin 13.

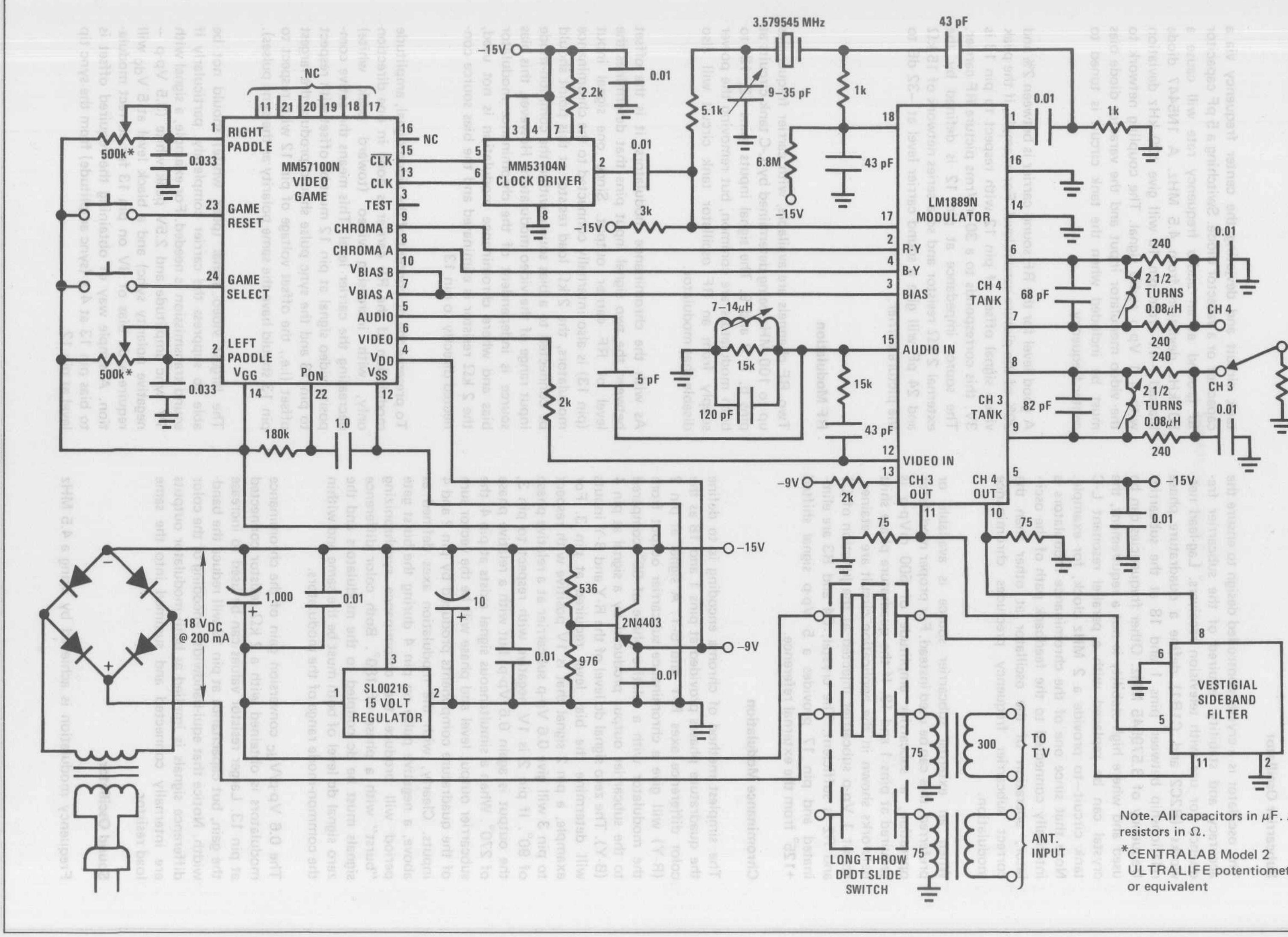
The channel B oscillator consists of devices Q56 and Q57 cross-coupled through level-shift zener diodes Q54 and Q55. A current regulator consisting of devices Q39–Q43 is used to achieve good RF frequency stability over supply and temperature. The channel B modulator consists of multiplier devices Q58, Q59 and Q50–Q53. The top quad is coupled to the channel B tank through isolating devices Q48 and Q49. A dc offset between pins 12 and 13 offsets the lower pair to produce an output RF carrier at pin 10. That carrier is then modulated by both the chroma signal at pin 13 and the video and sound carrier signals at pin 12. The channel A modulator shares pin 12 and 13 buffers Q45 and Q44 with channel B and operates in an identical manner.

The current flowing through channel B oscillator diodes Q54, Q55 is turned around in Q60, Q61 and Q62 to source current for the channel B RF modulator. In the same manner, the channel A oscillator Q71–Q74 uses turn around Q77, Q78 and Q79 to source the channel A modulator. One oscillator at a time may be activated by connecting its tank to supply (see ac test circuit). The corresponding modulator is then activated by its current turn-around, and the other oscillator/modulator combination remains "OFF".

Circuit Diagram



TV Game Schematic



Note. All capacitors in μF. All resistors in Ω.

*CENTRALAB Model 2 ULTRALIFE potentiometer or equivalent

The oscillator is a crystal-controlled design to ensure the accuracy and stability required of the subcarrier frequency for use with television receivers. Lag-lead networks (R2C2 and C1R1) define a quadrature phase relationship between pins 1 and 18 at the subcarrier frequency of 3.579545 MHz. Other frequencies can be used and where high stability is not a requirement, the crystal can be replaced with a parallel resonant L-C tank circuit—to provide a 2 MHz clock, for example. Note that since one of the chrominance modulators is internally connected to the feedback path of the oscillator, operation of the oscillator at other than the correct subcarrier frequency precludes chrominance modulation.

When an external subcarrier source is available or preferred, this can be used instead. For proper modulator operation, a subcarrier amplitude of 500 mVp-p is required at pins 1 and 18. If the quadrature phase shift networks shown in the application circuit are retained, about 1 Vp-p subcarrier injected at the junction of C1 and R2 is sufficient. The crystal, C4 and R3 are eliminated and pin 17 provides a 5 Vp-p signal shifted $+125^{\circ}$ from the external reference.

Chrominance Modulation

The simplest method of chroma encoding is to define the quadrature phases provided at pins 1 and 18 as the color difference axes R-Y and B-Y. A signal at pin 2 (R-Y) will give a chrominance subcarrier output from the modulator with a relative phase of 90° compared to the subcarrier output produced by a signal at pin 4 (B-Y). The zero signal dc level of the R-Y and B-Y inputs will determine the bias level required at pin 3. For example, a pin 2 signal that is 1V positive with respect to pin 3 will give 0.6 Vp-p subcarrier at a relative phase of 90°. If pin 2 is 1V negative with respect to pin 3, the output is again 0.6 Vp-p, but with a relative phase of 270°. When a simultaneous signal exists at pin 4, the subcarrier output level and phase will be the vector sum of the quadrature components produced by pin 2 and 4 inputs. Clearly, with the modulation axes defined as above, a negative pulse on pin 4 during the burst gate period will produce the chrominance synchronizing "burst" with a phase of 180°. Both color difference signals must be dc coupled to the modulators and the zero signal dc level of both must be the same and within the common-mode range of the modulators.

The 0.6 Vp-p/V_{dc} conversion gain of the chrominance modulators is obtained with a 2 kΩ resistor connected at pin 13. Larger resistor values can be used to increase the gain, but capacitance at pin 13 will reduce the bandwidth. Notice that equi-bandwidth encoding of the color difference signals is implied as both modulator outputs are internally connected and summed into the same load resistor.

Sound Oscillator

Frequency modulation is achieved by using a 4.5 MHz tank circuit and deviating the center frequency via a capacitor or a varactor diode. Switching a 5 pF capacitor to ground at an audio frequency rate will cause a 50 kHz deviation from 4.5 MHz. A 1N5447 diode biassed −4V from pin 16 will give ±20 kHz deviation with a 1 Vp-p audio signal. The coupling network to the video modulator input and the varactor diode bias must be included when the tank circuit is tuned to center frequency.

A good level for the RF sound carrier is between 2% and 20% of the picture carrier level. For example, if the peak video signal offset of pin 12 with respect to pin 13 is 3V, this corresponds to a 30 mVrms picture RF carrier. The source impedance at pin 12 is defined by the external 2 kΩ resistor and so a series network of 15 kΩ and 24 pF will give a sound carrier level at −32 dB to the picture carrier.

RF Modulation

Two RF channels are available, with carrier frequencies up to 100 MHz being determined by L-C tank circuits at pins 6, 7, 8 and 9. The signal inputs (pins 12, 13) to both modulators are common, but removing the power supply from an RF oscillator tank circuit will also disable that modulator.

As with the chrominance modulators, it is the offset between the two signal input pins that determines the level of RF carrier output. Since one signal input (pin 13) is also internally connected to the chrominance modulators, the 2 kΩ load resistor at this point should be connected to a bias source within the common-mode input range of the video modulators. However, this bias source is independent of the chrominance modulator bias and where chrominance modulation is not used, the 2 kΩ resistor is eliminated and the bias source connected directly to pin 13.

To preserve the dc content of the video signal, amplitude modulation of the RF carrier is done in one direction only, with increasing video (toward peak white) decreasing the carrier level. This means the active composite video signal at pin 12 must be offset with respect to pin 13 and the sync pulse should produce the largest offset (i.e., the offset voltage of pin 12 with respect to pin 13 should have the same polarity as the sync pulses).

The largest video signal (peak white) should not be able to suppress the carrier completely, particularly if sound transmission is needed. For example, a signal with 1V sync amplitude and 2.5V peak white (3.5 Vp-p — negative polarity sync) and a black level at 5 V_{dc} will require a dc bias of 8V on pin 13 for correct modulation. A simple way of obtaining the required offset is to bias pin 13 at 4 x (sync amplitude) from the sync tip level at pin 12.

Applications Information (Continued)

Split Power Supplies

The LM1889 is designed to operate over a wide range of supply voltages so that much of the time it can utilize the signal source power supplies. An example of this is shown in *Figure 2* where the composite video signal from a character generator is modulated onto an RF carrier for display on a conventional home TV receiver. The LM1889 is biased between the −12V and +5V supplies and pin 13 is put at ground. A 9.1 kΩ resistor from pin 12 to −12V dc offsets the video input signal (which has sync tips at ground) to establish the proper modulation depth — $R1/R2 = V_{IN}/12 \times 0.875$. This design is for monochrome transmission and features an extremely low external parts count.

DC Clamped Inputs

Utilizing a DC clamp will make matching the LM1889 to available signal generator outputs a simple process. *Figure 3* shows the LM1889 configured to accept the composite video patterns available from a Tektronix Type 144 generator that has black level at ground and negative polarity syncs. In this application, the chroma oscillator amplifier is used to provide a gain of two. The 100k pot adjusts the overall DC level of the amplified signal which determines the modulation depth of the RF output. Clamping the input requires a minimum of DC correction to obtain the correct DC output level. This allows the adjustment to be a high impedance that will have minimum effect on the amplifier closed loop gain.

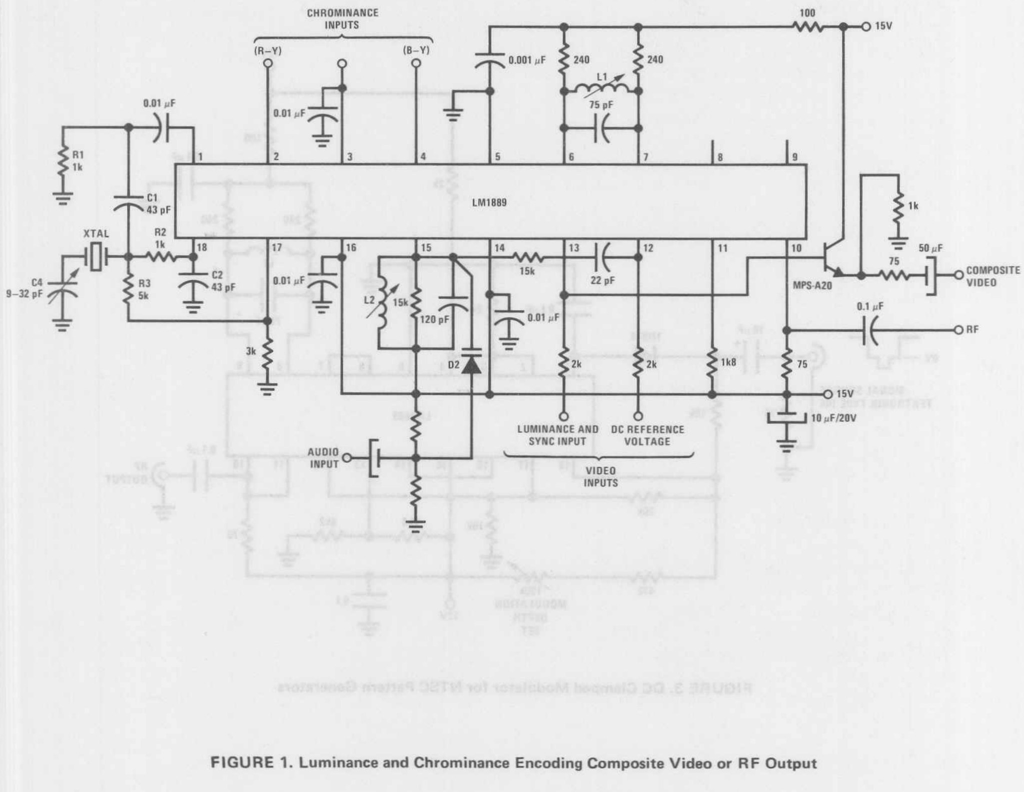


FIGURE 1. Luminance and Chrominance Encoding Composite Video or RF Output

Applications Information (Continued)

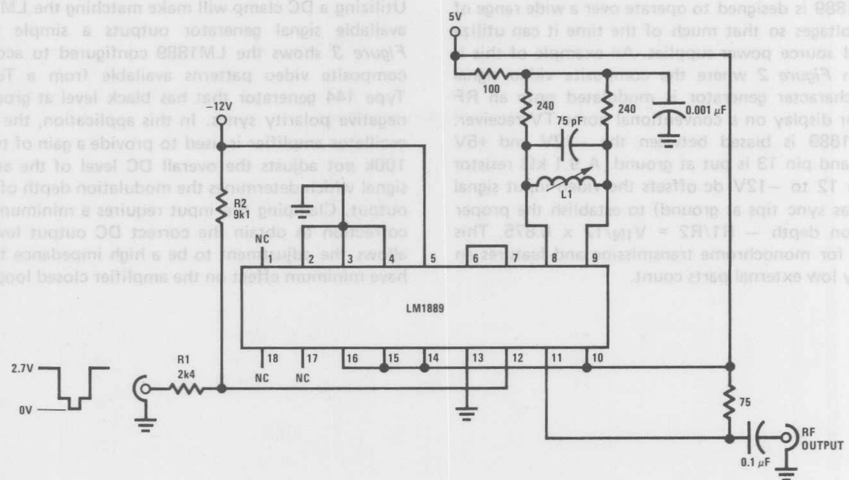


FIGURE 2. Low-Cost Monochrome Modulator for Character Generator Display

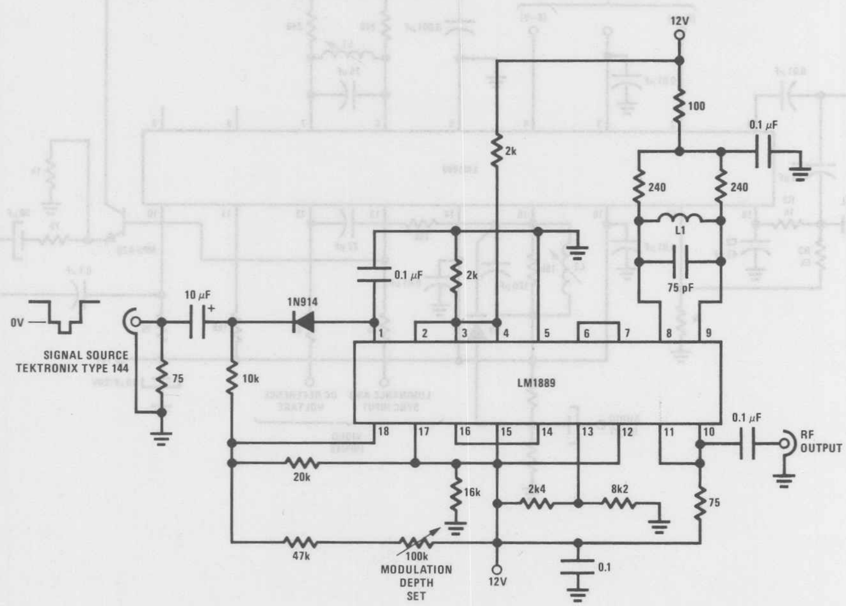


FIGURE 3. DC Clamped Modulator for NTSC Pattern Generators

National Semiconductor

LM2808 Monolithic TV Sound System

General Description

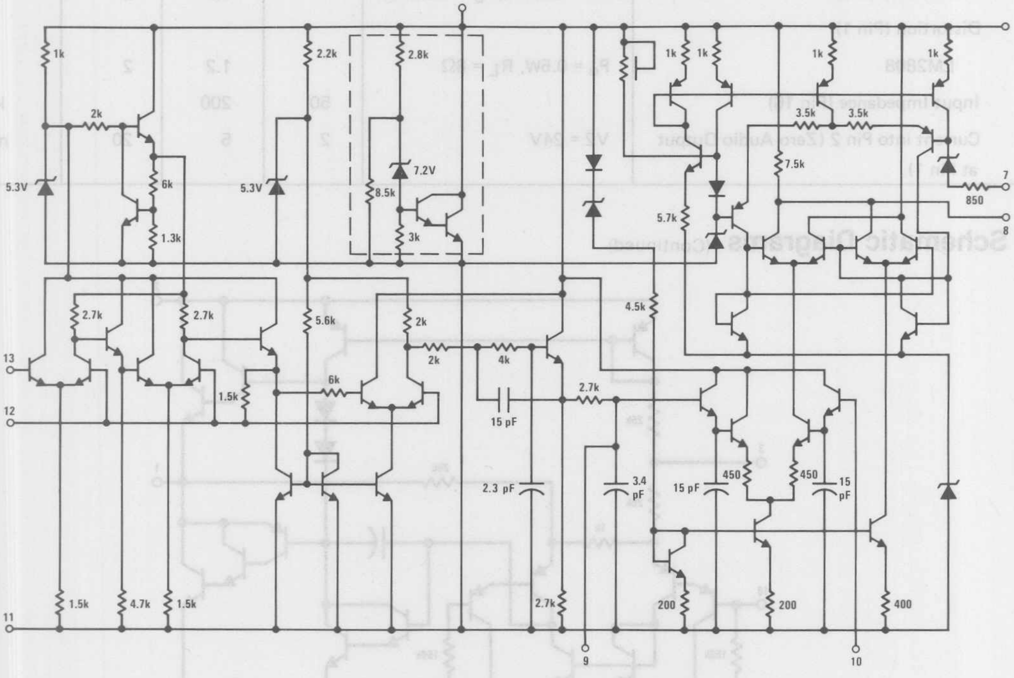
The LM2808 2W sound IF circuit is designed for television and related applications. The circuit is comprised of 2 independent functions: a sound IF and an audio power amplifier. An improved volume control circuit is included, however, so that recovered audio is a linear function of the resistance of the control potentiometer. Audio power amplification is accomplished with circuitry similar to the popular LM380 audio power amplifier, featuring both short circuit and thermal protection.

Features

- Minimum undistorted output
  LM2808 – 0.5W
- Linear volume control – 75 dB range
- Fixed voltage gain in audio amplifier
- Short circuit and thermal protection
- Standard dual-in-line package

Schematic Diagrams

(For power amplifier section of schematic, see next page)



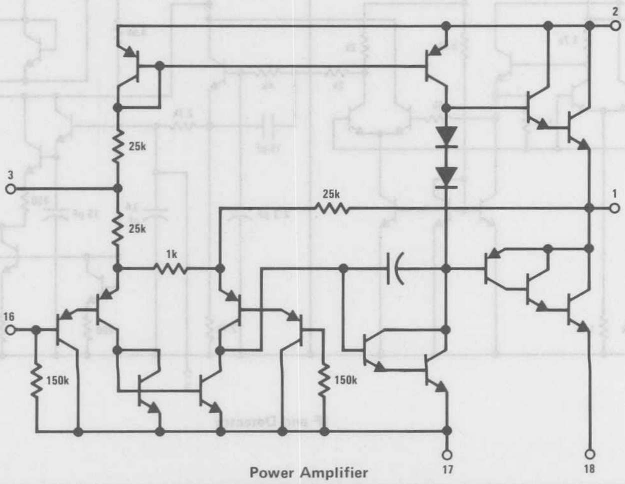
IF and Detector

		Maximum Junction Temperature	150°C
Input Signal Voltage (Between Pins 12 and 13)	3 Vp-p	Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (See test circuit)

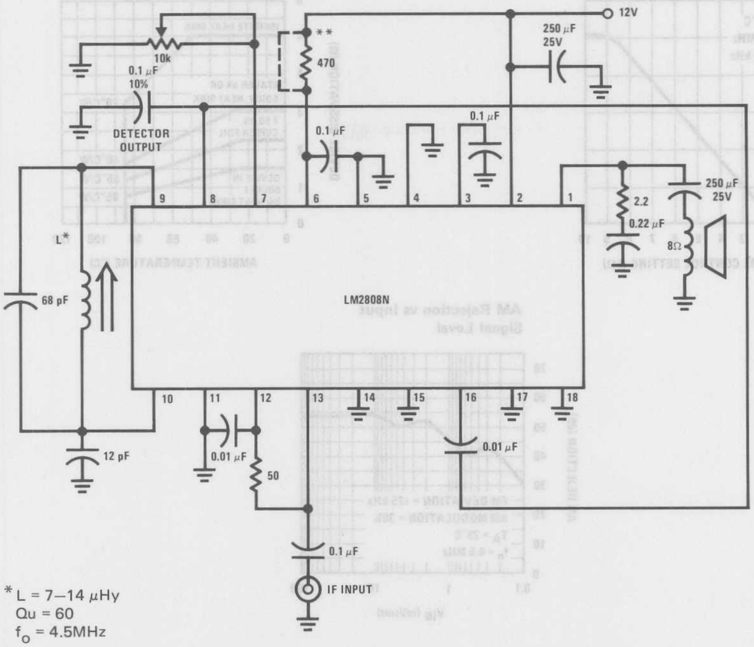
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
P_O @ 10% THD					
LM2808	V_{CC} = 16V, $R_L = 8\Omega$		2.6		W
	V_{CC} = 14V, $R_L = 8\Omega$		1.9		W
	V_{CC} = 12V, $R_L = 8\Omega$		1.3		W
Feedthrough Signal (Pin 1)	R Pin 7 = 0Ω			15	mVrms
Current into Pin 6	V Pin 6 = 10V	7	10.8	15	mA
AM Rejection	V_{IN} = 10 mVrms, Δf = 25 kHz, AM = 30%	40			dB
Recovered Audio (Pin 8)		350	500		mVrms
Input Limiting Voltage at 4.5 MHz			200	400	μV
Audio Power Amp Voltage Gain (Pin 16 to Pin 1)		40		60	V/V
Output Noise, Input Signal Removed (Pin 1)	R Pin 7 = 0Ω		70	150	mVrms
Distortion (Pin 8)	ΔF = 25 kHz, f_O = 4.5 MHz		1.2	2	%
Distortion (Pin 1)					
LM2808	P_O = 0.5W, $R_L = 8\Omega$		1.2	2	%
Input Impedance (Pin 16)		50	200		kΩ
Current into Pin 2 (Zero Audio Output at Pin 1)	V2 = 24V	2	5	20	mA

Schematic Diagrams (Continued)



Power Amplifier

Typical Application and Test Circuit

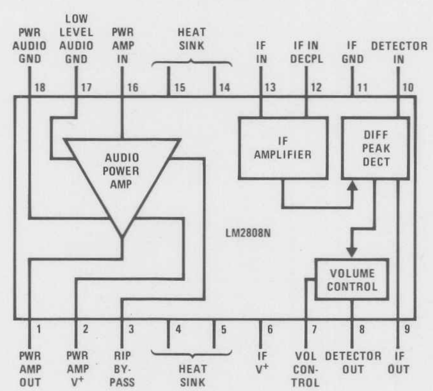


*L = 7–14 μHy
Qu = 60
f_o = 4.5MHz

Television Sound System

Connection Diagram

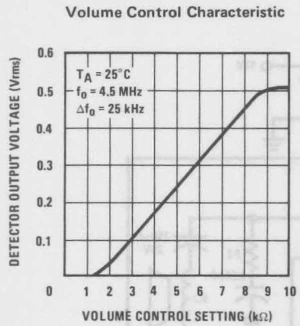
Dual-In-Line Package

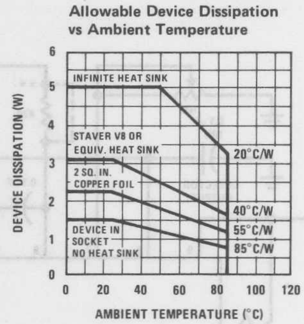


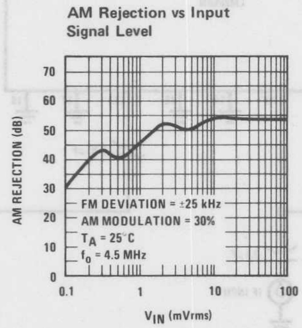
TOP VIEW

Order Number LM2808N
See NS Package N18A

Typical Performance Characteristics







LM3064 Television Automatic Fine Tuning

General Description

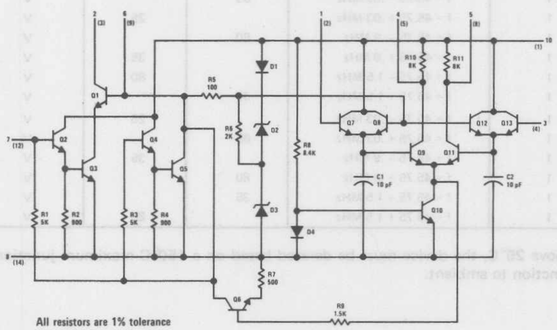
The LM3064 is a monolithic integrated circuit designed primarily for AFT (automatic fine tuning) applications. It includes a zener regulated power supply, IF amp, differential peak detector, and an AGC circuit.

The LM3064 is supplied in both the formed and straight lead 14-lead dual-in-line package.

Features

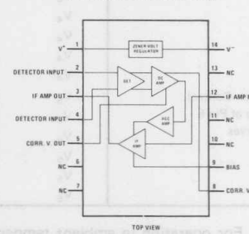
- Primarily intended for AFT applications
- High gain input amp (18 mV for rated output)
- Differential output correction voltage
- Wide operating temperature −40°C to +85°C
- Formed leads available for easy PC board design

Schematic and Connection Diagrams



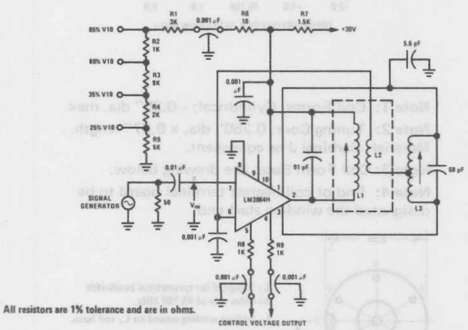
All resistors are 1% tolerance and are in ohms.

Dual-In-Line Package



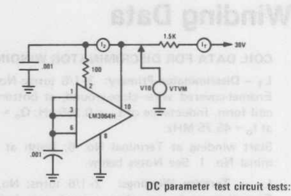
Order Number LM3064N
See NS Package N14A
Order Number LM3064N-01
See NS Package N14C

Test Circuits



All resistors are 1% tolerance and are in ohms.

Test Circuit 1
Correction Voltage Test Circuit



DC parameter test circuit tests:
- Total device dissipation.
- Zener regulating voltage.
- Quiescent operating current.
- Quiescent current into pin 2.

Test Circuit 2
DC Parameter Test Circuit

Absolute Maximum Ratings

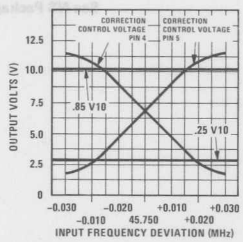
Power Dissipation (Note 1)	715 mW
Operating Temperature Range	$-40^\circ C$ to $+85^\circ C$
Storage Temperature Range	$-65^\circ C$ to $+150^\circ C$
Power Supply Current	50 mA

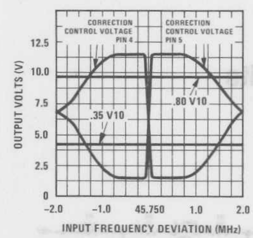
Electrical Characteristics ($T_A = 25^\circ C$)

PARAMETER	SYMBOL	TEST CIRCUIT	CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
STATIC						
Device Dissipation	P_T	2	$V_{CC} = 30V; R_S = 1.5k$	130	150	mW
Current Drain	I_1	2	$V_{10} = 10.5V$	4.0	9.5	mA
Zener Regulating Voltage	V_{10}	2	$V_{CC} = 30V; R_S = 1.5k$	10.9	12.8	V
Quiescent Current into Pin 2	I_2	2	$V_{CC} = 30V; R_S = 1.5k$	1	4	mA
Quiescent Voltage at Pin 4	V_4	1	$V_{CC} = 30V; R_S = 1.5k$	5.0	8.0	V
Quiescent Voltage at Pin 5	V_5	1	$V_{CC} = 30V; R_S = 1.5k$	5.0	8.0	V
Output Offset Voltage between Pins 4 & 5	V_4-V_5	1	$V_{CC} = 30V; R_S = 1.5k$	−1.0	+1.0	V
DYNAMIC – Output Voltage vs Frequency Deviation AFT						
				Correction Voltage as Shown Below		
Correction Control Voltage at Pin 4			$V_{CC} = 30V; R_S = 1.5k$; $V_i = 18$ mV	% of V_{10}	% of V_{10}	
	V_4	1	f = 45.75 − .03 MHz	85		V
	V_4	1	f = 45.75 + .03 MHz		25	V
	V_4	1	f = 45.75 − .9 MHz	80		V
	V_4	1	f = 45.75 + .9 MHz		35	V
	V_4	1	f = 45.75 − 1.5 MHz		80	V
	V_4	1	f = 45.75 + 1.5 MHz	35		V
Correction Control Voltage at Pin 5 See Curves	V_5	1	f = 45.75 − .03 MHz		25	V
	V_5	1	f = 45.75 + .03 MHz	85		V
	V_5	1	f = 45.75 − .9 MHz		35	V
	V_5	1	f = 45.75 + .9 MHz	80		V
	V_5	1	f = 45.75 − 1.5 MHz	35		V
	V_5	1	f = 45.75 + 1.5 MHz		80	V

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 175°C/W junction to ambient.

Correction Control Voltage





Coil Winding Data

COIL DATA FOR DISCRIMINATOR WINDINGS

L_1 – Discriminator Primary: 3-1/6 turns; No. 20 Enamel-covered wire–close-wound, at bottom of coil form. Inductance of $L_1 = 0.165\ \mu H$; $Q_o = 120$ at $f_o = 45.75$ MHz.

Start winding at Terminal No. 6; finish at Terminal No. 1. See Notes below.

L_2 – Tertiary Windings: 2-1/6 turns; No. 20 Enamel-covered wire–close- wound over bottom end of L_1. Start winding at Terminal No. 3; finish at Terminal No. 4. See Notes below.

L_3 – Discriminator Secondary: 3-1/2 turns; center-tapped, space wound at bottom of coil form. Inductance of $L_3 = 0.180\ \mu H$; $Q_o = 150$ at $f_o = 45.75$ MHz.

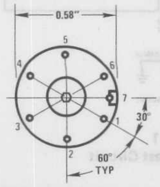
Start winding at Terminal No. 2; finish at Terminal No. 5, connect center tap to Terminal No. 7. See Notes.

Note 1: Coil Forms; Cylindrical; –0.30" dia. max.

Note 2: Tuning Core: 0.250" dia. x 0.37" length. Material: Carbinal J or equivalent.

Note 3: Coil Form Base: See drawing below.

Note 4: End of coil nearest terminal board to be designated the winding start end.



L_1 is aligned for symmetrical bandwidth on either side of 45.750 MHz.
L_2 tertiary winding wound on L_1 coil form.
L_3 is aligned for zero differential output between terminals 4 and 5 at f_O = 45.750 MHz.

National Semiconductor

TBA440C Monolithic Video IF Amplifier

General Description

The TBA440C is a monolithic video IF amplifier for color and monochrome television receivers.

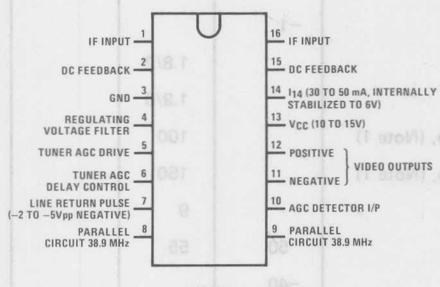
The circuit includes three IF amplifier stages, a balanced video IF detector and a gated AGC section for the IF amplifier and PNP tuner.

Features

- High gain—high stability
- Minimal noise increase, incurred by use of AGC
- Minimum RF breakthrough to video outputs
- Fast AGC action—gating largely independent of pulse shape and amplitude
- Very low intermodulation products
- Positive and negative video signals are available from low impedance outputs
- Integrated temperature compensating circuit

Connection Diagram

Dual-In-Line Package

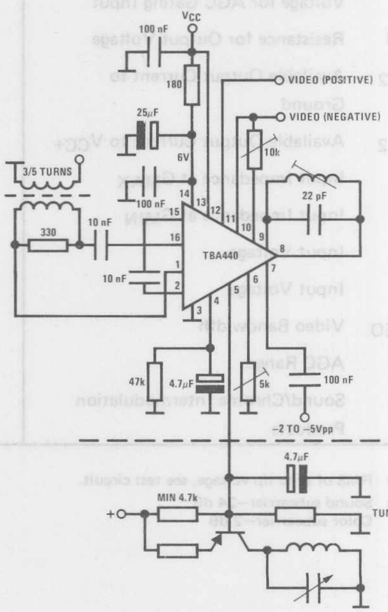


TOP VIEW

Order Number TBA440C
See NS Package N16A

Order Number TBA440CQ
See NS Package N16C

Test Circuit



Absolute Maximum Ratings

Supply Voltage	15V
Current Into Pin 14	50 mA
Power Dissipation	700 mW
Maximum Resistance Between Pins 8 and 9	20Ω
Operating Temperature Range	−25°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (T_A = 25°C, V_{CC} = 13V, I_{14} = 40 mA, unless otherwise specified)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{13}	Current Consumption	V13 = 15V	14.5	17.5	20.5	mA
V14	Internal Supply Voltage	I_{14} = 40 mA, V_{IN} = 0	5.5	6.0	6.8	V
V11	DC Voltage at Output	V_{IN} = 0	5.5	7	8.5	V
V12	DC Voltage at Output		1.7	3	4.3	V
I_5	Control Current for Tuner AGC	(10 dB After Beginning of the Tuner AGC, V5 ≥ 2V)	3			mA
V4	IF Control Voltage for G_{MAX}		0		0.5	V
V4	IF Control Voltage for G_{MIN}		2.5			V
V7	Voltage for AGC Gating Input		−5		−2	V
R10-11	Resistance for Output Voltage	V11 = 3 Vp-p	3	4	10	kΩ
I_{11}, I_{12}	Available Output Current to Ground				5	mA
I_{11}, I_{12}	Available Output Current to V_{CC+}		−1			mA
Z1-16	Input Impedance at G_{MAX}			1.8/2		kΩ/pF
Z1-16	Input Impedance at G_{MIN}			1.9/0		kΩ/pF
V_{IN}	Input Voltage	V11 = 2 Vp-p, (Note 1)		100		μV
V_{IN}	Input Voltage	V11 = 3 Vp-p, (Note 1)		150		μV
B_{VIDEO}	Video Bandwidth			9		MHz
G_V	AGC Range		50	55		dB
	Sound/Chroma Intermodulation Products	(Note 2)	−40			dB

Note 1: RMS of sync tip voltage, see test circuit.
Note 2: Sound subcarrier—24 dB
Color subcarrier—2 dB

National Semiconductor

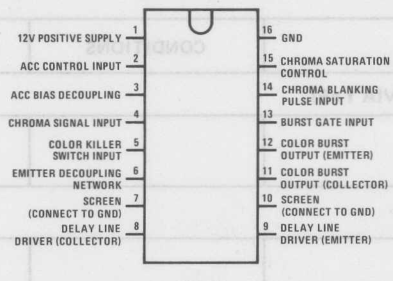
TBA510 Chrominance Combination

General Description

The TBA510 is an integrated chrominance amplifier circuit for color TV receivers incorporating a variable gain ACC circuit, a dc control for chroma saturation which can be ganged to the receiver contrast control, chroma blanking and burst gating functions, a burst output stage, a color killer and a PAL delay line driver.

Connection Diagram

Dual-In-Line Package

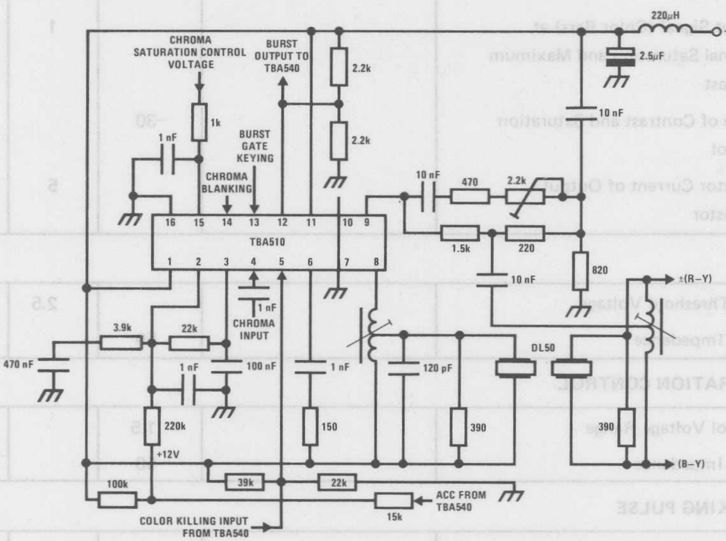


TOP VIEW

Dual-In-Line Package, Order Number TBA510
See NS Package N16A

Quad-In-Line Package, Order Number TBA510Q
See NS Package N16C

Typical Application



Note: The A.C.C. loop gain can be defined by inserting a suitable resistor between pins 2 & 3. (Example 22 kΩ).

Absolute Maximum Ratings

Power Dissipation, (T_A = 60°C)	550 mW
V1-16	13.2V
V13-16	−5V
V14-16	−5V
V8-16	+20V
V11-16	+20V
$I_8 = -I_9$	20 mA
$I_{11} = -I_{12}$	20 mA
Operating Temperature Range	−20°C to +60°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (V1-16 = 12V, T_A = 25°C)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CHROMINANCE SIGNAL (FED IN VIA 1 nF)						
V4-16	Input Voltage Range		15		300	mVp-p
|Z4-16|	Input Impedance		2	3		kΩ
BURST SIGNAL OUTPUT						
V12-16	DC Voltage			7.7		V
V12-16	Output Signal			1		Vp-p
I_{11}	Collector Current of Output Transistor			4		mA
CHROMINANCE SIGNAL OUTPUT (BURST BLANKED INTERNALLY)						
V9-16	DC Voltage			6.8		V
V9-16	Output Signal (Color Bars) at Nominal Saturation and Maximum Contrast			1		Vp-p
	Range of Contrast and Saturation Control		−30		+6	dB
I_8	Collector Current of Output Transistor			5		mA
ACC INPUT						
V2-16	ACC Threshold Voltage			2.5		V
|Z2-16|	Input Impedance		50			kΩ
CHROMA-SATURATION CONTROL						
V15-16	Control Voltage Range		1.5		4.5	V
|Z15-16|	Input Impedance		50			kΩ
CHROMA BLANKING PULSE						
V14-16	Switching Level			−1		V
|Z14-16|	Input Impedance			2		kΩ

Electrical Characteristics (Continued) ($V1\text{-}16 = 12V$, $T_A = 25°C$)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
BURST GATE PULSE						
V13-16	Switching Level			−2.2		V
|Z13-16|	Input Impedance			4		kΩ
COLOR KILLER						
V5-16	Input Voltage For:					
	Color "ON"		2.3			V
	Color "OFF"				1.9	V
	Signal Suppression at Color "OFF"			50		dB
|Z5-16|	Input Impedance		50			kΩ

Note 1: The phase difference between the chroma and burst outputs at nominal saturation is less than 5°.

Note 2: Phase shift of chroma output signal over saturation control range +6 to −10 dB is less than 5°.

Pin Function Description

1. Positive 12V supply.

2. ACC control potential input. The potential required at pin 2 for maximum gain is about 2.5V; gain reduction occurs when this potential is reduced, $Z_{IN} > 50$ kΩ.

3. ACC gain adjustment point. The internal ACC circuit consists of a long-tailed pair system. The "cold" side of the pair is internally established at a dc potential of 2.5V and is brought out on pin 3. This enables a decoupling capacitor to be connected. A very high loop gain in the ACC system is possible but as this is not necessarily desirable, because of stability and ripple considerations, a resistor of a suitable value can be connected between pins 2 and 3 to reduce the control sensitivity to any desired level.

4. Chroma input signal. The input voltage range is 15 to 300 mVp-p (26 dB) with a color bar signal.

5. Color killer switching input. The input impedance is greater than 50 kΩ. Color "ON" 2.3V; color "OFF" 1.9V. The chroma signal suppression when killed is greater than 50 dB.

6. Emitter decoupling network. The series network decouples an emitter of an amplifier stage. The value of resistance influences the gain of both the chroma channel and the burst channel.

7. Screen. This pin must be connected to pin 10 and taken via a direct path to earth. The function of this is to minimize crosstalk between burst and chroma channels.

8. Delay line driver (collector). Supplies the chroma signal drive to the delay line driver transformer, the cold end of which is connected to +12V. The maximum permitted voltage excursion at this pin is to 20V peak. Maximum ac signal current swing, 12 mAp-p.

9. Delay line driver (emitter). Supplies the chroma to the network which provides the non-delayed signal to the delay line output transformer. The emitter is established internally at a potential of 6.8 ±1V and the external network, which must incorporate a resistive dc path to earth, must not demand more than 20 mA peak current.

10. Screen. Connect to pin 7 and then to earth.

11. Color burst output (collector). If a low impedance color burst is required (from the emitter of the color burst output, pin 12) pin 11 will be connected to the +12V supply. The maximum voltage and current excursions permitted on pin 11 are 20V peak and 20 mA peak.

12. Color burst output (emitter). An external load resistor of 2 kΩ is required, connected to earth, and a dc potential of 7.7V is established on pin 11 due to the internal circuitry. The burst output voltage is 1 Vp-p ±1 dB over the chroma input signal range of amplitudes.

13. Burst gate gating pulse. A pulse derived from the horizontal flyback pulse can be used as a source of gating waveform. A negative-going pulse of not greater than 5V amplitude is necessary, the input impedance is 4 kΩ and the switching is about −2.2V.

14. Chroma blanking pulse input. A negative-going horizontal flyback pulse can be used here. Its amplitude should not exceed 5V. The input impedance at this pin is 2 kΩ and the switching level is about −1.0V. This pulse is used to blank the burst output from the chroma channel.

15. Chroma saturation control. The dc control voltage range required is from 1.5-4.5V (highest gain at −4.5V). The input impedance is greater than 50k and a control range of from +6 to −30 dB is given.

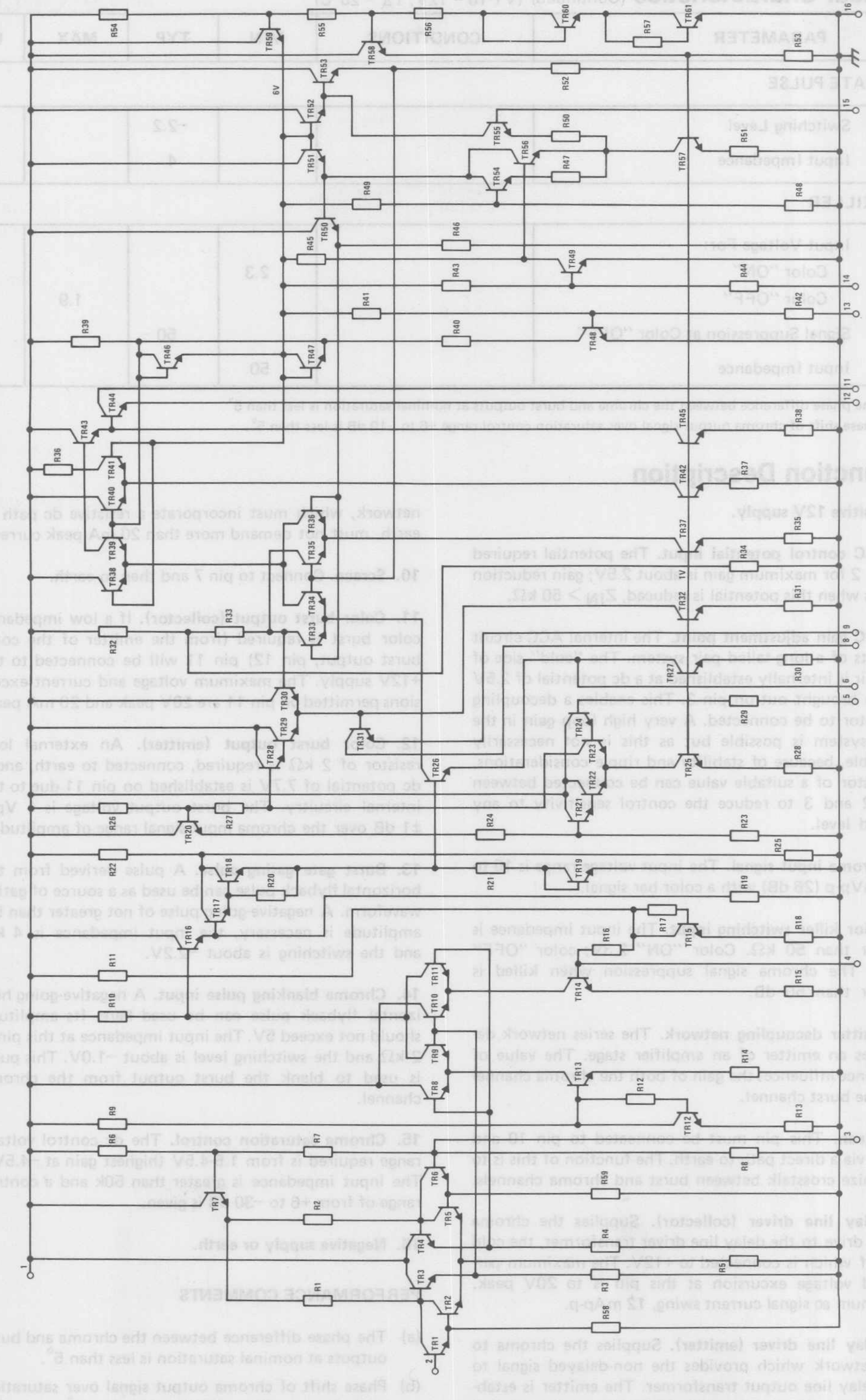
16. Negative supply or earth.

PERFORMANCE COMMENTS

(a) The phase difference between the chroma and burst outputs at nominal saturation is less than 5°.

(b) Phase shift of chroma output signal over saturation control range +6 to −10 dB is less than 5°.

Schematic Diagram



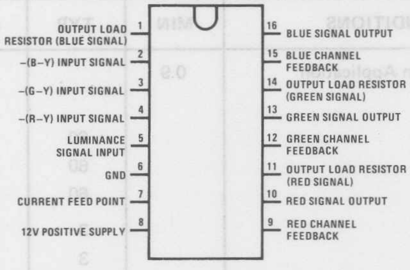
TBA530 RGB Matrix Preamplifier

General Description

The TBA530 is an integrated circuit for color TV receivers incorporating a matrix preamplifier for R-G-B cathode or grid drive of the picture tube without clamping circuits. It has been designed to be driven from the TBA990 or TBA520 synchronous demodulator circuits and exhibits excellent channel matching and stability.

Connection Diagram

Dual-In-Line Package

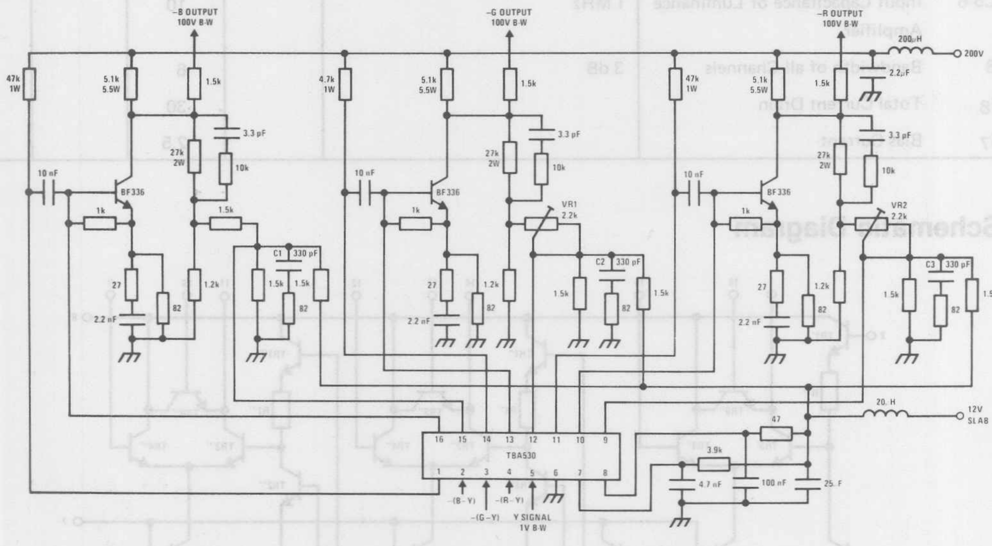


TOP VIEW

Dual-In-Line Package, Order Number TBA530
See NS Package N16A

Quad-In-Line Package, Order Number TBA530Q
See NS Package N16C

Typical Application



Note 1: DC output voltages R, G and B are typically 140V in this circuit.

Note 2: The voltage gain between pins 2, 3, 4 and collectors (BF336) is typically 100.

Note 3: The normal bias voltage on pins 1, 11, 14 is 8V.

Note 4: Pin 7 requires a 4.7 nF decoupling capacitor.

Note 5: DC bias level shift, provided by internal zeners between pins 1-16, 14-13 and 11-10, requires 10 nF bypass capacitors for H.F.

Absolute Maximum Ratings

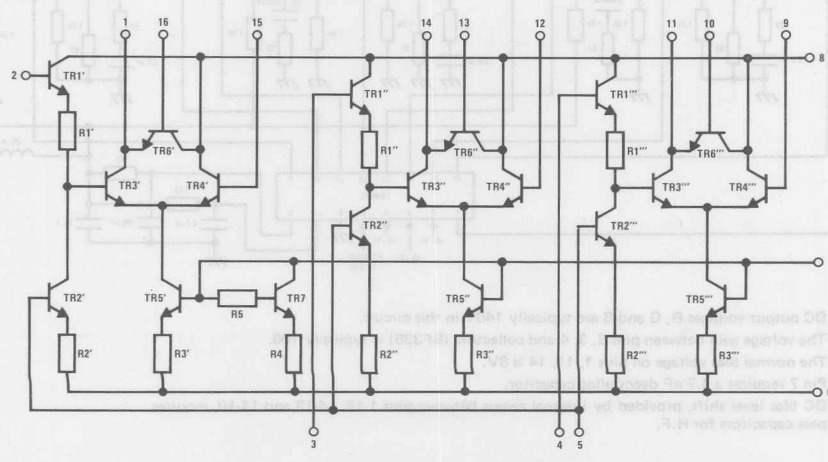
V8-6	13.2V
I_1, I_{11}, I_{14}	10 mA
I_{10}, I_{13}, I_{16}	50 mA
Power Dissipation ($T_A = 60^\circ C$)	400 mW
Operating Temperature Range	$-20^\circ C$ to $+60^\circ C$
Storage Temperature Range	$-65^\circ C$ to $+150^\circ C$
Lead Temperature (Soldering, 10 seconds)	$300^\circ C$

Electrical Characteristics

Measuring Conditions: Black Level: $V_{R\text{-}Y} = V_{G\text{-}Y} = V_{B\text{-}Y} = 7.5V$, $V_Y = 1.5V$, V8–6 = 12V, $T_A = 25^\circ C$

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Ratio of Gain of Luminance Amplifier to Color Amplifiers	As Measured in Application Circuit	0.9		1.1	
R2-6	Input Resistance of Color Difference Amplifiers	1 kHz		60		kΩ
R3-6				60		kΩ
R4-6				60		kΩ
C2-6	Input Capacitance of Color Difference Amplifiers	1 MHz		3		pF
C3-6				3		pF
C4-6				3		pF
R5-6	Input Resistance of Luminance Amplifier	1 kHz		20		kΩ
C5-6	Input Capacitance of Luminance Amplifier	1 MHz		10		pF
B	Bandwidth of all Channels	3 dB		6		MHz
I_8	Total Current Drain			30		mA
I_7	Bias Current			2.5		mA

Schematic Diagram



Pin Function Description

The function is quoted against the corresponding pin number.

1. Output load resistor, blue signal. (Also pins 11 and 14 for red and green signals respectively.) Resistors (47 kΩ, 1W) connected to +200V provide the high value loads for the internal amplifying stages. The nominal operating potential on these pins is defined by the IC and dc feedback and is approximately +8V. The maximum current which can be allowed at each of these pins is 10 mA.

2. −(B-Y) input signal. This signal is fed via a low-pass filter from the TBA520 demodulator IC (pin 7) having a dc level of about +7.5V. The input resistance for this pin is typically 60 kΩ with an input capacitance of less than 5 pF (similarly for pins 3 and 4).

3. −(G-Y) input signal. The dc black level of this signal is about +7.5V. (See pin 2.)

4. −(R-Y) input signal. The dc black level of this signal is about +7.5V. (See pin 2.)

5. Luminance signal input. The dc level on this pin for picture black is +1.6V. The required signal amplitude is 1V black-to-white with negative-going syncs (or blanking) for cathode drive as shown. The input resistance at this pin is 20 kΩ approximately with a capacitance of less than 15 pF.

6. Negative supply (earth).

7. Current feed point. A current of approximately 2.5 mA is required at this pin, fed via a 3.9 kΩ resistor from +12V, to bias the internal differential amplifiers. A decoupling capacitor of 4.7 nF is necessary.

8. Positive 12V supply. Maximum supply voltage permitted, 13.2V. Current consumption approximately 30 mA.

9. Red channel feedback (green channel, pin 12; blue channel, pin 15). The dc working points and gains of both the output stages and the IC amplifier stages are stabilized by the feedback circuits. The black level potentials at the collectors of the output stages (tube cut-off) are adjusted by setting correctly the dc levels of the color difference signals produced by the TBA520 demodulator IC. The gains of the R-G-B output stages are adjusted to give the correct white points setting on the picture tube by adjusting the potentiometers in the feedback paths (VR1, VR2). (See notes on setting up decoder.)

10. Red signal output (green and blue signal outputs on 13 and 16). These pins are internally connected with pins 11, 14 and 1 respectively via zener type junctions to give a dc level shift appropriate for driving the output transistor bases directly. To bypass the zener junctions at h.f. three 10 nF capacitors are required.

11. Output load resistor, red channel (see pin 1).

12. Green channel feedback (see pin 9).

13. Green signal output (see pin 10).

14. Output load resistors, green channel (see pin 1).

15. Blue channel feedback (see pin 9).

16. Blue signal output (see pin 10).

Note 1: Careful attention to earth paths should be given, avoiding common impedances between the input (decoder) side and the output stages. Also, to enable matched performance to be achieved, a symmetrical board and component layout should be adopted for the three output stages. To compensate for the effect upon h.f. response of inevitable differences the compensating capacitors C1 and C2 and C3 may be appropriately selected for any given board layout.

Note 2: The signal black level at the collectors of the R-G-B output stages depends upon the +12V supply, the dc level of the color difference signals from the TBA520 demodulator IC and the black level potential of the luminance signal applied to the TBA530 matrix IC. The dc levels of the signals produced and handled by the IC's are designed to have approximately proportional tracking with the 12V supply potential,

$$\text{i.e., } \frac{\Delta V_{(\text{dc level, signal})}}{\Delta V_{12V}} \triangleq \frac{V_{\text{nom (dc level, signal)}}}{12}$$

To ensure that changes in picture black level due to variations on the 12V supply to the IC's occur in a predictable way, all the IC's should be operated from a common supply line. This is specially important for the TBA520 and TBA530. Furthermore, to limit the changes in picture black level during receiver operation, the 12V supply should have a stability of not worse than ±3% due to operational variations.

Note 3: To reduce the possibility of patterning on the picture due to radiation of the harmonics of the products of the demodulation process, the leads carrying the drive signals to the picture tube should be as short as the receiver layout will allow. Resistors (typically 1k 5Ω) connected in series with the leads and mounted close to the collectors of the output transistors provide useful additional filtering of harmonics.

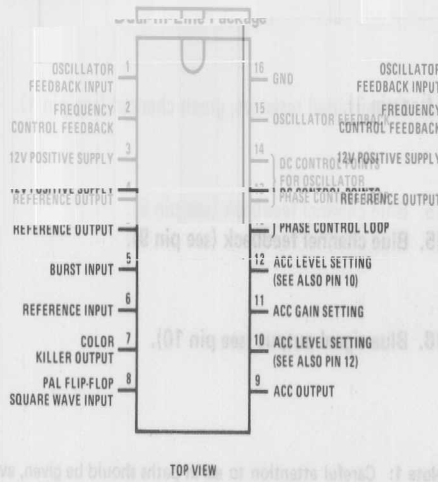
TBA540 Reference Combination

General Description

The TBA540 is an integrated 'color reference' oscillator circuit for PAL TV receivers. The oscillator employs a quartz crystal and incorporates automatic phase and amplitude control. A synchronous demodulator is used to compare the phase and amplitude of the swinging burst ripple with the PAL flip-flop waveform and generates appropriate ACC color killer and identification signals. A high standard of noise immunity has been obtained by using synchronous demodulation.

Connection Diagram

Dual-In-Line Package

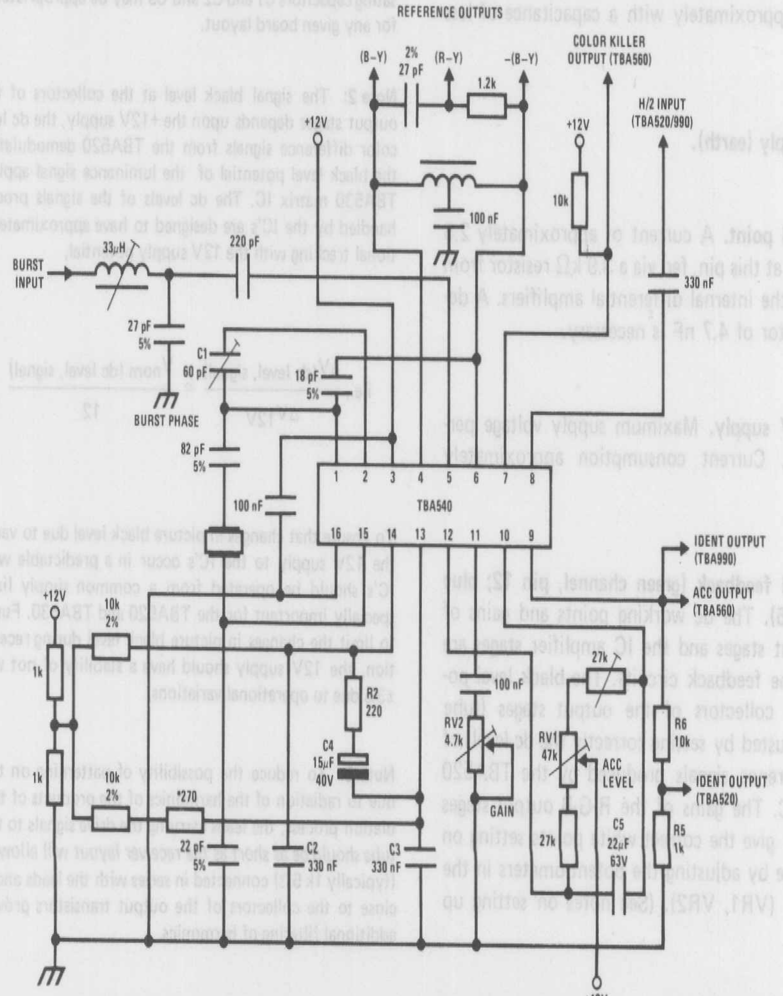


TOP VIEW

Dual-In-Line Package, Order Number TBA540
See NS Package N16A

Quad-In-Line Package, Order Number TBA540Q
See NS Package N16C

Typical Application



Absolute Maximum Ratings

V3-16	13.2V	Storage Temperature Range	−65°C to +150°C
Power Dissipation (T_A = 60°C)	780 mW	Lead Temperature (Soldering, 10 seconds)	300°C
Operating Temperature Range	−20°C to +60°C		

Electrical Characteristics (V3-16 = 12V, T_A = 25°C as measured in typical application circuit)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Output Signals					
V4-16	B-Y Reference Signal Output		1	1.4	2	Vp-p
V7-16	Color Killer Output					
	Color "ON"			12		V
	Color "OFF"			100	250	mV
V9-16	ACC Output Signal Range					
	At Correct Phase of PAL Switch			4 to 0.2		V
	At Incorrect Phase of PAL Switch			4 to 11		V
	Oscillator Section (Amplifier)					
R15-16	Input Resistance			3.5		kΩ
C15-16	Input Capacitance			5		pF
G15-1	Voltage Gain			4.7		
	Reactance Control Section					
G15-2	Voltage Gain With Pins 13 and 14 Shorted			1.3		
ΔG15-2	Rate of Change of Gain G15-2			5		rad^{-1}
Δφ5-4	With Phase Difference Between Burst and Reference Signal					
	Burst Input					
R5-16	Input Resistance			1		kΩ
	Burst Input Level		0.7	1.5		Vp-p
	Flip-Flop Input					
V8-16	Voltage			2.5		Vp-p
R8-16	Resistance			3.3		kΩ
	Phase Lock Loop					
	Oscillator Phase Error for a Burst Signal	Crystal Frequency I400 Hz			±10	DEG
	Holding Range			±600		Hz
	Pull-in Range			±300		Hz
	Temperature Coefficient of Oscillator			2		Hz/°C

Application Notes

A dc connection between pins 4 and 6 is necessary via the bifilar coupling inductor. The function of this inductor is to produce, on pin 6, a signal of equal amplitude and opposite phase (B-Y) to that on pin 4. A center tap on the inductor, connected to earth via a dc blocking capacitor, is therefore necessary.

DC Control Points in Reference Control Loop

Pins 13 and 14 are connected to opposite sides of a differential amplifier circuit and are brought out for the purpose of dc balancing of the reactance stage and the connection of the bandwidth—determining filter network. Two 2% tolerance 10k resistors with the addition of a 270Ω resistor at pin 13 are used in place of the previous balancing network. The 270Ω resistor may be modified according to the nature of the noise that appears at pin 5.

Initial Adjustment

(a) Remove burst signal.

(b) Short-circuit pins 13-14. Adjust oscillator to correct frequency by C1.

(c) Set the ACC level adjustment RV1, to give +4V on pin 9. Remove short circuit.

(d) Apply burst signal.

(e) Adjust ACC gain, RV2, to give a burst amplitude of 1.5Vp-p on pin 5.

energy from this pin. The output impedance is approximately 2 kΩ in parallel with 5 pF.

2. Reactance control stage feedback. This pin is fed internally with a sinewave derived from the reference output (pin 4) and controlled in amplitude by the internal reactance control circuit. The phase of the feedback from pin 2 to the crystal via C1 is such that the value of C1 is effectively increased. Pin 2 is held internally at a very low impedance, therefore the tuning of the crystal is controlled automatically by the amplitude of the feedback waveform and its influence on the effective value of C1.

3. Positive 12V supply. The maximum voltage must not exceed 13.2V.

4. Reference waveform output. This pin is driven internally by the regenerated subcarrier waveform in B-Y phase. (The output is in B-Y rather than R-Y phase as the burst phase network produces a lag of 90° of the burst applied to pin 5). An output amplitude of nominally 1.4Vp-p is produced at low impedance. No dc load to earth is required. A dc connection between pins 4 and 6 is, however, necessary via the bifilar coupling inductor. The function of this inductor is to produce, on pin 6, a signal of equal amplitude and opposite phase (−(B-Y)) to that on pin 4. A center tap on the inductor, connected to earth via a dc blocking capacitor, is therefore necessary.

5. Burst waveform input. A burst waveform amplitude of 1.5Vp-p is required to be ac-coupled to this pin. The amplitude of the burst will normally be controlled by the adjustment and operation of the ACC circuit. The input impedance at this pin is approximately 1 kΩ and a threshold level of 0.7V must be exceeded before the burst signal becomes effective. A dc bias of 400 mV is internally derived for pin 5.

The absolute level of the tip of the burst at pin 5 will normally reach 1.5V (1.5Vp-p burst amplitude).

6. Reference waveform input. This pin requires a reference waveform in the −(B-Y) phase, derived from pin 4 via a bifilar transformer (see pin 4), to drive the internal balanced reactance control stage. A dc connection between pins 4 and 6 must be made via the transformer.

7. Color killer output. This pin is driven from the collector of an internal switching transistor and requires an external load resistor (typically 10 kΩ) connected to +12V. The unkilled and killed voltages on this pin are then pin 9 over which switching of the color killed output on pin 7 occurs is nominally +2.5V.)

8. PAL flip-flop square wave input. A 2.5Vp-p square wave derived from the PAL flip-flop (in the TBA520 or TBA990 demodulator IC) is required at this pin, ac-coupled via a capacitor. The input impedance is about 3.3 kΩ.

9. ACC output. An emitter follower provides a low impedance output potential which is negative-going with a rising burst input amplitude. With zero burst input signal the dc potential produced at pin 9 is set to be +4V (RV1). The appearance of a burst signal on pin 5 will cause the potential on pin 9 to go in a negative direction in the event that the PAL flip-flop is identified to be in the correct phase. The range of potential over which full ACC control is exercised at pin 9 is determined by the control characteristic of the ACC amplifier, i.e., for the TBA560 from 0.8 to 1V. The potential on pin 9 will fall to a value within this range as the burst input signal is stabilized to an amplitude of 1.5Vp-p. The latter condition is achieved by correct adjustment of RV2. If, however, the PAL flip-flop phase is wrong the potential on pin 9 will move positively. The potential divider R5, R6 will then operate a PAL switch cut-off function in the TBA520 demodulator IC.

10. ACC level setting. The network connected between pins 10 and 12 balances the ACC circuit and RV1 is adjusted to give +4V on pin 9 with no burst input signal to pin 5. C5 provides filtering.

11. ACC gain control. RV2 is adjusted to give the correct amplitude of burst signal on pin 5 (1.5 Vp-p) under ACC control.

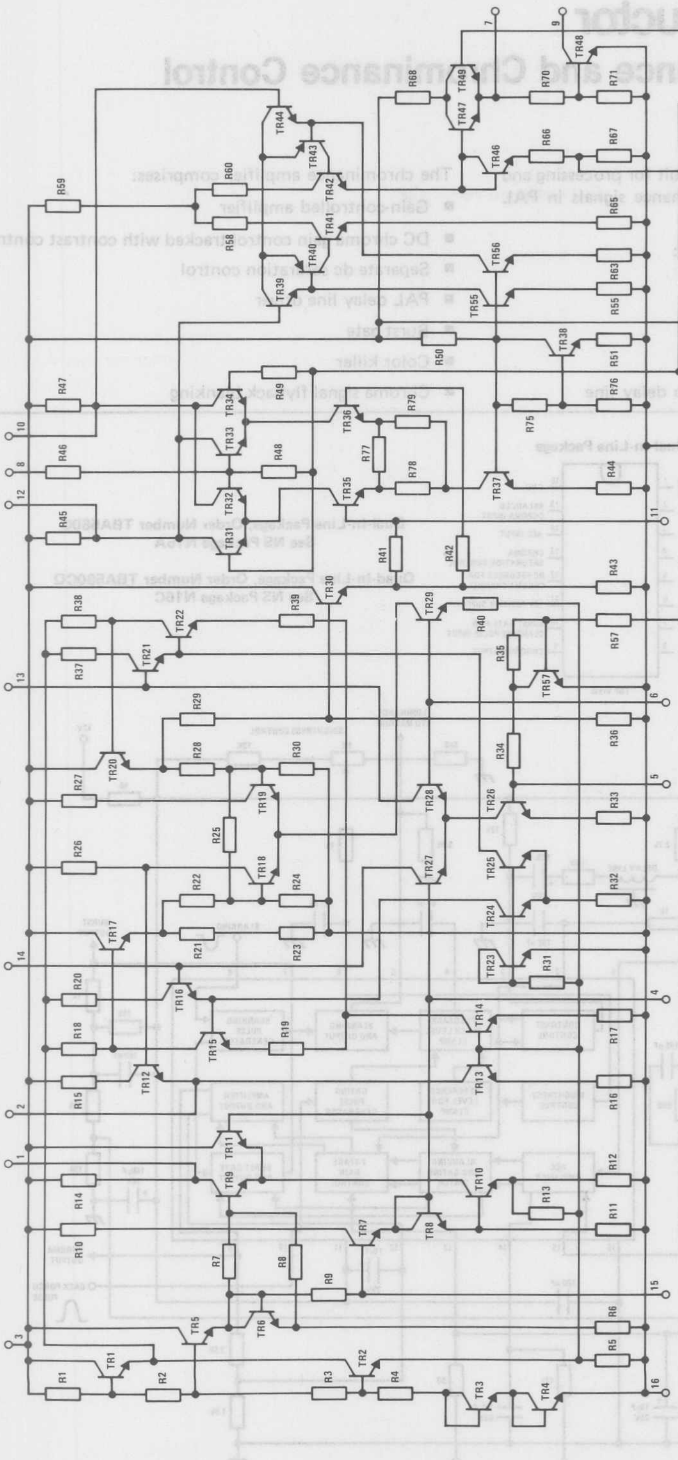
12. See pin 10.

13. See pin 14.

14. DC control points in reference control loop. Pins 13 and 14 are connected to opposite sides of a differential amplifier circuit and are brought out for the purpose of dc balancing of the reactance stage and the connection of the bandwidth-determining filter network. Two 2% tolerance 10k resistors with the addition of a 270Ω resistor at pin 13 are used in place of the previous balancing network. The 270Ω resistor may be modified according to the nature of the noise that appears at pin 5.

The filter network consists of R2, C2, C3 and C4. The dc potentials on these pins are nominally +6V.

Schematic Diagram



National Semiconductor

TBA560C Luminance and Chrominance Control Combination

General Description

The TBA560C is an integrated circuit for processing and controlling luminance and chrominance signals in PAL TV receivers.

The luminance amplifier comprises:

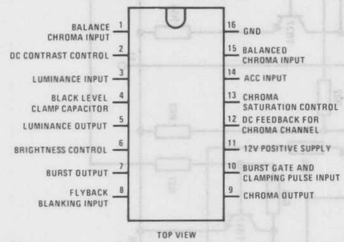
- DC contrast control
- Brightness control
- Black level clamping
- Blanking of flyback
- Input matched to the luminance delay line

The chrominance amplifier comprises:

- Gain-controlled amplifier
- DC chroma gain control tracked with contrast control
- Separate dc saturation control
- PAL delay line driver
- Burst gate
- Color killer
- Chroma signal flyback blanking

Connection Diagram

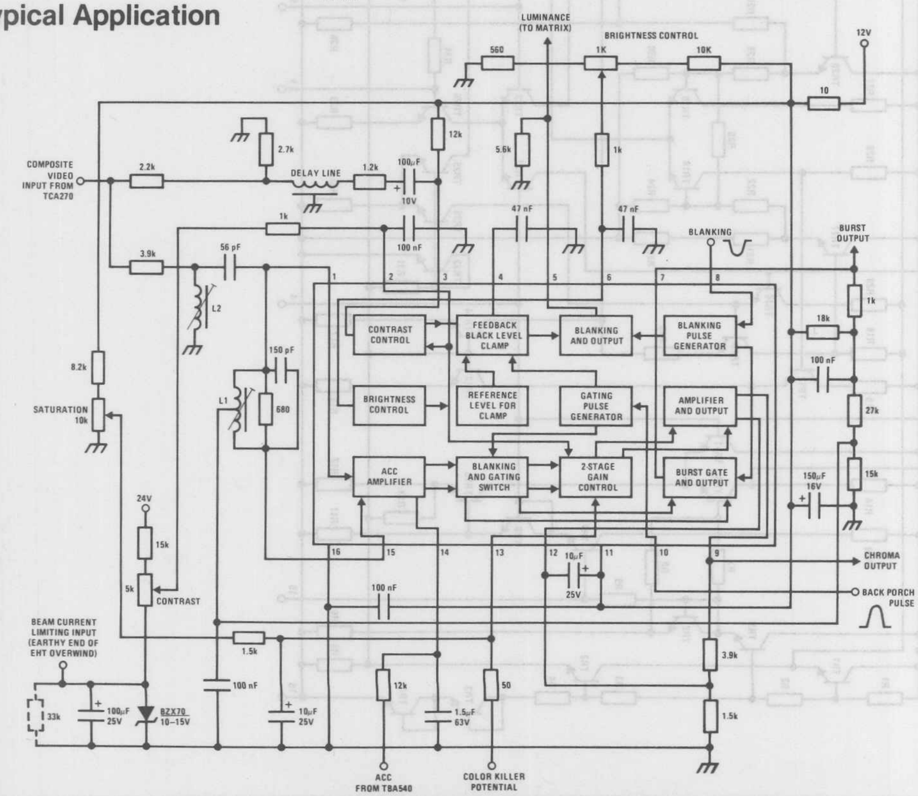
Dual-In-Line Package



Dual-In-Line Package, Order Number TBA560C
See NS Package N16A

Quad-In-Line Package, Order Number TBA560CQ
See NS Package N16C

Typical Application



Absolute Maximum Ratings (Note 1)

V11-16	13.2V	I_Q	−10 mA
V8-16 Min.	−5V	Continuous Total Power Dissipation	550 mW
V10-16 Min.	5V	Operating Free Air Temperature Range	−20°C to +60°C
V12-16	−5V to +6V	Storage Temperature Range	−65°C to +150°C
V13-16	−3V to +6.5V	Lead Temperature (Soldering, 10 seconds)	300°C
V14-16 Min.	−5V		

Electrical Characteristics with V11-16 = 12V, T_A = 25°C (as measured in typical application circuit)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V1-15	Chrominance Input Signal Range (Value of Color Bars With 75% Saturation)		4		80	mVp-p
I_3	Luminance Input Current Black to White			0.5	1.5	mAp-p
V2-16	Contrast Control Characteristic	Full Gain		5.6		V
		6 dB Attenuation		3.7		V
		20 dB Attenuation (Note 2)		2.0		V
V6-16	Brightness Control Voltage for Black Level of 1.5V at Pin 5	(Note 3)		1.3		V
V8-16	Flyback Blanking Pulses					
V8-16	For 0V Blanking Level at Pin 5		0	−0.5	−1	Vp-p
	For 1.5V Blanking Level at Pin 5		−2	−2.5	−3	Vp-p
V13-16	Saturation Control Characteristic	Full Gain		6.2		V
		6 dB Attenuation		4.4		V
		20 dB Attenuation (Note 2)		2.7		V
I_{10}	Burst Gating Pulse		0.05		1	mAp-p
V13-16	Color Killer		0.5		1	V
	Automatic Chrominance Control					
V14-16	Voltage for Maximum Gain			1.2		V
	Voltage for Minimum Gain			0.5		V
	Gain Reduction			26		dB
	Input Resistance		50			kΩ
V5-16	Luminance Output Voltage (Black-White) at Nominal Contrast and Input Current as above	(Note 2)		1	3	Vp-p
	Black Level Shift Due to Changes of Contrast and Video Content at Constant Brightness Setting				100	mV
V7-16	Burst Output			1		Vp-p
V9-16	Chrominance Output at Nominal Contrast and Saturation	(Note 2)		1		Vp-p
	3 dB Bandwidth of Chrominance and Luminance Amplifier			5		MHz
	Matching of Luminance to Chrominance Ratio at 10 dB Contrast Control			2		dB

Note 1: V2-16 and V13-16 must always be lower than V11-16.

Note 2: Typical or nominal contrast or saturation = maximum value −6 dB. Thus the control is +6 to −14 dB on the nominal.

Note 3: When V6-16 is increased above 1.7V the black level of the output signal remains at 2.7V.

1. **Balanced chroma signal input (in conjunction with pin 15).** This is derived from the chroma signal bandpass filter, designed to provide a push-pull input. An input signal amplitude of at least 4 mVp-p is required between pins 1 and 15. Both pins require a dc potential of approximately +3.0V. This is derived as a common mode signal from a network connected to pin 7 (burst output). In this way dc feedback is provided over the burst channel to stabilize its operation. All figures for the chrominance signal are based on a color bar signal with 75% saturation; i.e., burst-to-chroma ratio of input signal is 1:2.

2. **DC contrast control.** With +3.7V on this pin, the gain in the luminance channel is such that a 0.5 mA black-to-white input signal to pin 3 gives a luminance output signal amplitude on pin 5 of 1V black-to-white. A variation of voltage on pin 2 between +5.6V and +2V gives a corresponding gain variation of +6 to > −14 dB. A similar variation in gain in the chroma channel occurs in order to provide the correct tracking between the two signals. Beam current limiting can be applied via the contrast control network as shown in the peripheral circuit, when a separate overwind is available on the line output transformer.

3. **Luminance signal input.** This terminal has a very low input impedance and acts as a current sink. The luminance signal from the delay line is fed via a series terminating resistor and a dc blocking capacitor and requires to be about 0.5 mAp-p amplitude. A dc bias current is required via a 12 kΩ resistor to the +12V line.

4. **Charge storage capacitor for black level clamp.**

5. **Luminance signal output.** An emitter follower provides a low impedance output signal of 1V black-to-white amplitude at nominal contrast setting having a nominal black level in the range 0 to +2.7V. An external emitter load resistor is required, not less than 1 kΩ. If a greater luminance output is required than 1V, with normal control settings, the input current swing at pin 3 should be increased in proportion.

6. **Brightness control.** Over the range of potential +0.9 to +1.7V the black level of the luminance output signal (pin 5) is increased from 0 to +2.7V. The output signal black level remains at +2.7V when the potential on pin 6 is increased above +1.7V.

7. **Burst output.** A 1 Vp-p burst (controlled by the ACC system) is produced here. Also, to achieve good dc stability by negative feedback in the burst channel the dc potential at this pin is fed back to pins 1 and 15 via the chroma input transformer.

8. **Flyback blanking input waveform.** Negative-going horizontal and vertical blanking pulses may be applied here. If rectangular blanking pulses of not greater than −1V negative excursion, or dc coupled pulses of similar amplitude whose negative excursion is at zero volts dc are applied, the signal level at the luminance output (pin 5) during blanking will be 0V. However, if the blanking pulses applied to pin 8 have an amplitude of −2 to −3V the signal level at the luminance output during blanking will be +1.5V. The negative pulse amplitude should not exceed −5V.

9. **Chroma signal output.** With a 1 Vp-p burst output signal (pin 7) and at nominal contrast and saturation setting (pins 2 and 13) the chroma signal output amplitude is 1 Vp-p. An external network is required which provides dc negative feedback in the chroma channel via pin 12.

10. **Burst gating and clamping pulse input.** A positive pulse of not less than 50μA is required on this pin to provide gating in the burst channel and luminance channel black-level clamp circuit. The timing and width of this current pulse should be such that no appreciable encroachment occurs into the sync pulse or picture line periods during normal operation of the receiver.

11. **+12V LT supply.** Correct operation occurs within the range 10.8 to 13.2V. All signal and control levels have a linear dependency on supply voltage but, in any given receiver design this range may be restricted due to considerations of tracking between the power supply variations and picture contrast and chroma levels. The power dissipation must not exceed 550 mW at 60°C ambient temperature.

12. **DC feedback for chroma channel (see pin 9).**

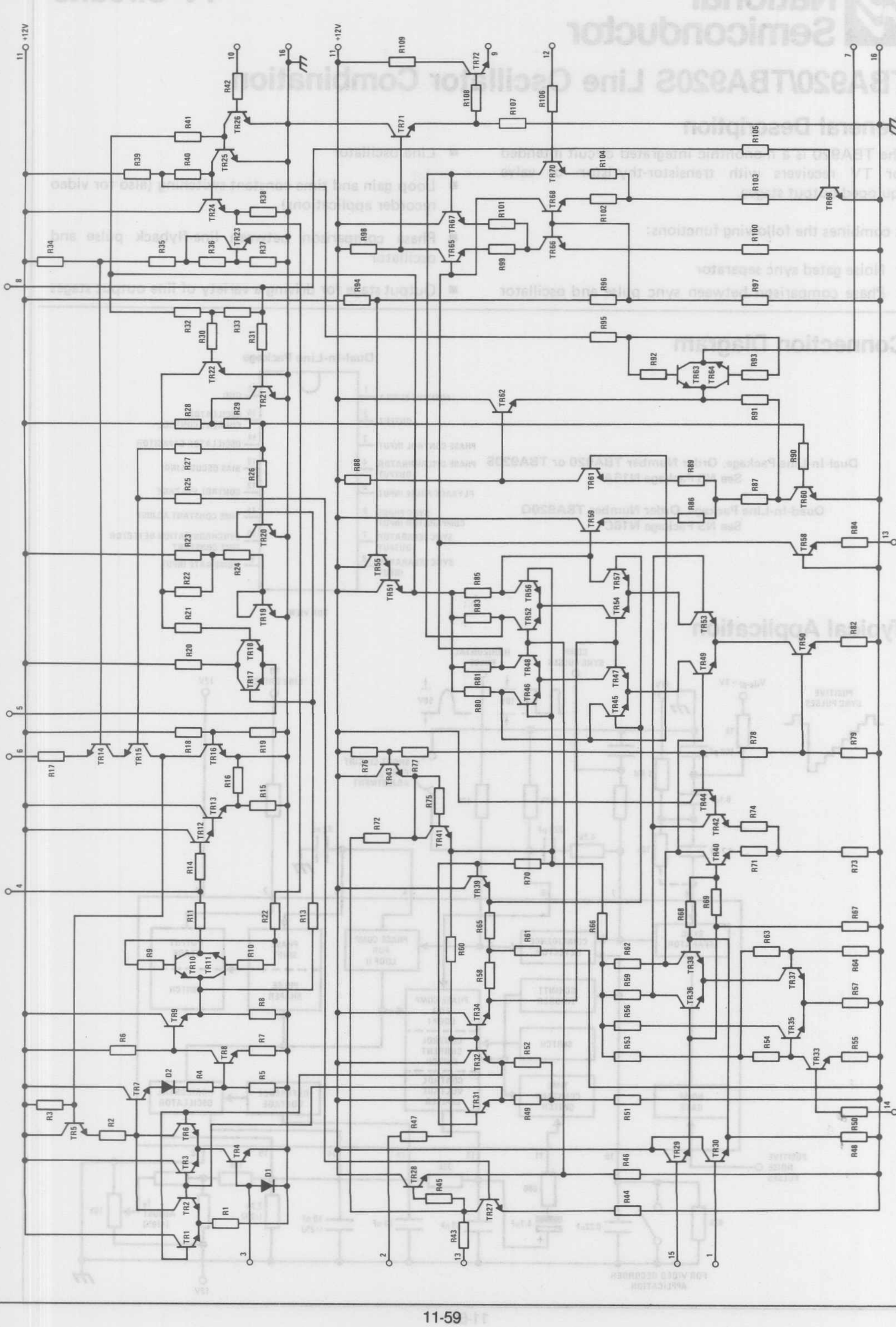
13. **Chroma saturation control.** A control range of +6 to > −14 dB is provided over a range of dc potential on pin 13 from 6.2 to 2.7V. Color killing is also achieved at this terminal by reducing the dc potential to less than +1V, e.g., from the TBA540 color killer output terminal. The minimum "kill factor" is 40 dB.

14. **ACC input.** A negative-going potential gives an ACC range of about 26 dB starting at +1.2V. From 1V to 800 mV the steepest part of the characteristic occurs, but a small amount of gain reduction also occurs from 800 mV to 500 mV. The input resistance is at least 50 kΩ.

15. **Chroma signal input (see pin 1).**

16. **Negative supply, 0V (Earth).**

Schematic Diagram



National Semiconductor

TV Circuits

TBA920/TBA920S Line Oscillator Combination

General Description

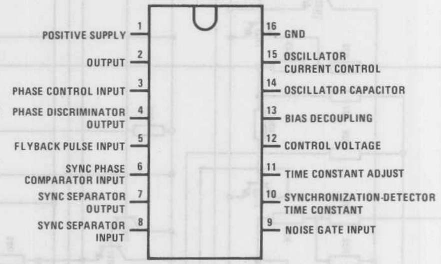
The TBA920 is a monolithic integrated circuit intended for TV receivers with transistor-thyristor- or valve equipped output stages.

It combines the following functions:

- Noise gated sync separator
- Phase comparison between sync pulse and oscillator
- Line oscillator
- Loop gain and time constant switching (also for video recorder applications)
- Phase comparison between line-flyback pulse and oscillator
- Output stage for driving a variety of line output stages

Connection Diagram

Dual-In-Line Package

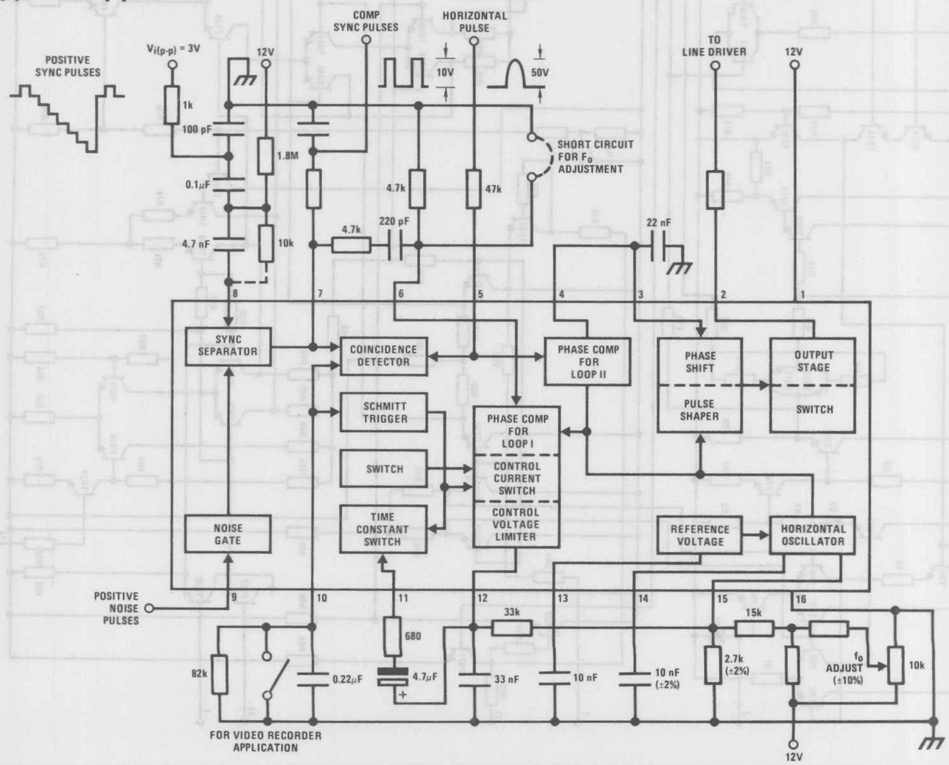


TOP VIEW

Dual-In-Line Package, Order Number TBA920 or TBA920S
See NS Package N16A

Quad-In-Line Package, Order Number TBA920Q
See NS Package N16C

Typical Application



Absolute Maximum Ratings

V1-16	13.2V	Operating Temperature Range	−20°C to +60°C
I_2 (Mean)	20 mA	Storage Temperature Range	−65°C to +150°C
I_2 (Peak)	200 mA	Lead Temperature (Soldering, 10 seconds)	300°C
I_5, I_7, I_9	10 mA	Power Dissipation (T_A = 60°C)	600 mW

Electrical Characteristics at V1-16 = 12V, T_A = 25°C as measured in application circuit

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Current Consumption					
I_1		I_2 = 0		36		mA
	Video Signal					
V1	Input Voltage Range		1		7	Vp-p
I_Q	Input Current During Sync Pulse			100		μA
	Noise Gating (Pin 9)					
V9-16	Input Voltage (Peak Value)		0.7			V
I_9	Input Current (Peak Value)		0.03		10	mA
	Flyback Pulse (Pin 5)					
V5-16	Input Voltage (Peak Value)			±1		V
I_5	Input Current (Peak Value)		0.05	1		mA
R5-16	Input Resistance			400		Ω
t_5	Pulse Duration at 15,625 Hz		10			μs
	Composite Sync Pulses (Positive: Pin 7)					
V7-16	Output Voltage			10		Vp-p
	Output Resistance					
R7-16	At Leading Edge of Pulse (Emitter Follower)			50		Ω
R7-16	At Trailing Edge			2.2		kΩ
R7-16 (ext)	Additional External Load Resistance		2			kΩ
	Driver Pulse (Pin 2)					
V2-16	Output Voltage			10		Vp-p
I_2	Average Output Current				20	mA
I_2	Peak Output Current				200	mA
t_2	Output Pulse Duration When Synchronized		12		32	μs
$t_{o\ tot}$	Permissible Delay Between Leading Edge of Output Pulse and Flyback Pulse at t_5 = 12μs		0		15	μs
V1-16	Supply Voltage at Which Output Pulses are Obtained		4			V
	Oscillator					
f_o	Frequency; Free Running	R15-16 = 3.3 kΩ, (Note 1)		15,625		Hz
$\frac{\Delta f_o}{f_o}$	Spread of Frequency at Nominal Values of Peripheral Components				±5	%
$\left\lvert\frac{\Delta f_o}{f_o}\right\rvert$	Frequency Change When Decreasing the Supply Down to Minimun 4V				10	%
$\frac{\delta f_o}{f_o} / \frac{\delta V_P}{V_{Pnom}}$	Influence of Supply Voltage on Frequency at V_P = 12V				5	%
$\delta f_o/\delta I_{15}$	Frequency Control Sensitivity			16.5		Hz/μA
	Control Loop I (Between Sync Pulse and Oscillator)					
V12-16	Control Voltage Range		0.8		5.5	V
	Control Current (Peak Values)					
I_{12M}		V10-16 > 4.5V, V6-16 > 1.5V		±2		mA
I_{12M}		V10-16 < 2V, V6-16 > 1.5V		±6		mA

	Loop Gain of APC System					
$\frac{\Delta f}{\Delta t}$	Time Coincidence Between Sync Pulse and Flyback Pulse or V10-16 > 4.5V			1		kHz/μs
$\frac{\Delta f}{\Delta t}$	No Time Coincidence or V10-16 < 2V			3		kHz/μs
Δf	Catching and Holding Range	(Note 2)		±1		kHz
t	Pull-in Time	$\Delta f/f_o$ = ±3% (Δf = 470 Hz)		20		ms
t	Switch-over From Large Control Sensitivity to Small Control Sensitivity After Catching			20		ms
	Control Loop II (Between Flyback Pulse and Oscillator)					
$t_{d\ tot}$	Permissible Delay Between Leading Edge of Output Pulse (Pin 2) and Leading Edge of Flyback Pulse		0		15	μs
$\frac{\Delta t}{\Delta t_d}$	Static Control Error	(Note 3)			0.5	%
	Overall Phase Relation					
t	Phase Relation Between Leading Edge of Sync Pulse and Middle of Flyback Pulse	(Note 4)		4.9		μs
$\lvert\Delta t\rvert$	Tolerance of Phase Relation	(Note 5)			1	μs
$\frac{\Delta f}{f_o}$	Spread of Frequency at Nominal Values of Peripheral Components					
	TBA920				±5	%
	TBA920S				±2	%
V3-16	Voltage	$t_2 = 12\mu s$		6		V
V3-16		$t_1 = 32\mu s$		8		V
I_3	Input Current				2	μA
	Time Constant Switch Voltage on Pin 10					
V10-16		For Internal R11 = 150Ω	4.5			V
V10-16		For Internal R11 = 2 kΩ			2	V

Note 1: The oscillator frequency can be changed for other TV standards by an appropriate value of C14-16.

Note 2: Adjustable with R12-15.

Note 3: The control error is the remaining error in reference to the nominal phase position between leading edge of the sync pulse and the middle of the flyback pulse caused by a variation in delay of the line output stage.

Note 4: This phase relation assumes a luminance delay line with a delay of 500 ns between the input of the sync separator and the drive to the picture tube. If the sync separator is inserted after the luminance delay line or if there is no delay line at all (black-and-white sets), then the phase relation is achieved by C5-16 = 560 pF.

Note 5: The adjustment of the overall phase relation and consequently the leading edge of the output pulse at pin 2 occurs automatically by the control loop II or by applying a dc voltage to pin 3.

National Semiconductor

TBA950-2 Television Signal Processing Circuit

General Description

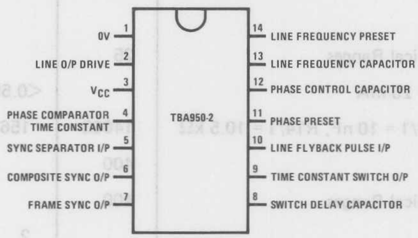
The TBA950-2 is a monolithic integrated circuit for pulse separation and line synchronization in TV receivers with transistor output stages.

The TBA950 comprises the sync separator with noise suppression, the frame pulse integrator, the phase comparator, a switching stage for automatic changeover of noise immunity, the line oscillator with frequency range limiter, a phase control circuit and the output stage.

It delivers prepared frame sync pulses for triggering the frame oscillator. The phase comparator may be switched for video recording operation. Due to the large scale of integration, few external components are needed.

Connection and Block Diagrams

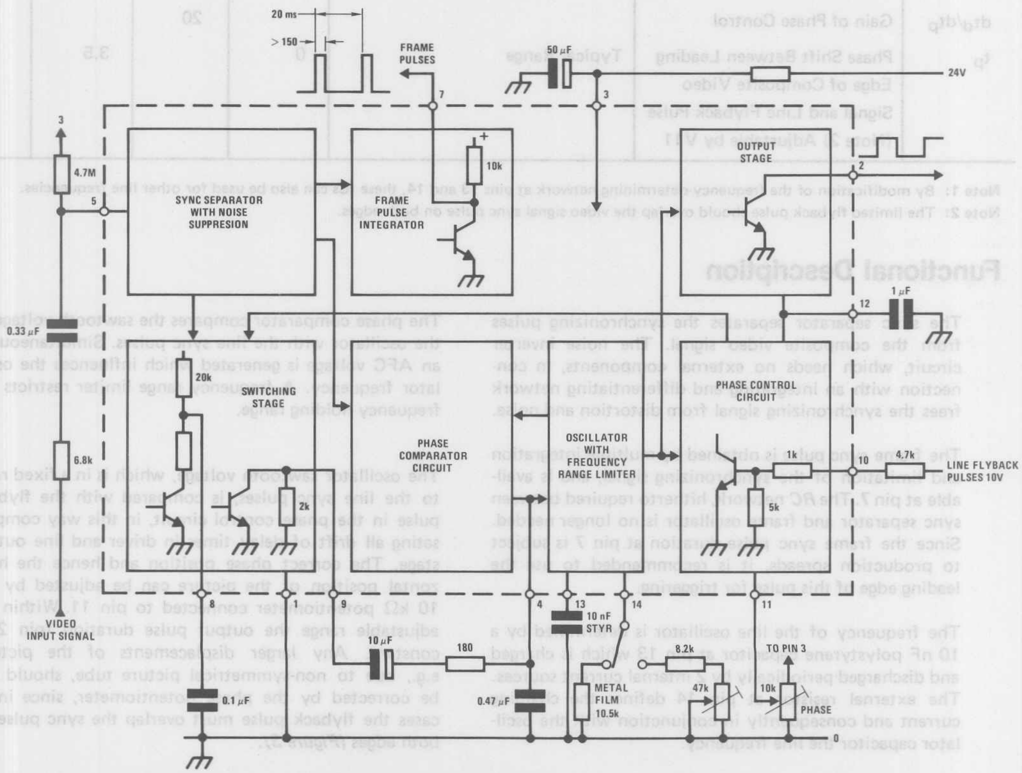
Dual-In-Line Package



TOP VIEW

Dual-In-Line Package, Order Number TBA950-2
See NS Package N14A

Quad-In-Line Package, Order Number TBA950-2Q
See NS Package N14C



Absolute Maximum Ratings

All voltages are referred to pin 1

I_3, Supply Current *(Figure 6)*	45 mA
I_5, Input Current	2 mA
V5, Input Voltage	−6V
I_2, Output Current	22 mA
V2, Output Voltage	12V
I_8, Switch-Over Current for Video Recording	5 mA
I_{10}, Flyback Peak Pulse Current	5 mA
V11, Phase Correction Voltage	0 to V3
T_A, Ambient Temperature	60°C

Recommended Operating Conditions

(For operating circuits ***Figures 4 and 5*****)**

I_5, Input Current During Sync Pulse	>5 μA
V_{IN} p-p, Composite Video Input Signal	3 (1 to 6)V
I_{10}, Input Current During Line Flyback Pulse	0.2 to 2 mA
I_8, Switch-Over Current	>2 mA
t_d, Time Difference Between the Output Pulse at Pin 2 and the Line Flyback Pulse at 10	<20 μs
I_3, Current Consumption *(Figure 6)*	≤45 mA
T_A, Ambient Operating Temperature Range	0°C to +60°C

Electrical Characteristics $T_A = 25°C$, f_o = 15,625 Hz in the test circuit *Figure 2* (Note 1)

SYMBOL	CHARACTERISTIC	CONDITIONS	MIN	TYP	MAX	UNITS
V7	Amplitude of the Frame Pulse			>8		V
t7	Frame Pulse Durations			>150		μs
$R_{OUT\ 7}$	Output Resistance at Pin 7 (High State)		7.5	10	13	kΩ
t2	Output Pulse Duration	Typical Ranges	25		28	μs
V2 Res	Residual Output Voltage	I_2 = 20 mA		<0.55		V
f_o	Oscillator Frequency	C13/1 = 10 nF, R14/1 = 10.5 kΩ	14063	15625	17187	Hz
$\pm\Delta f_F$	Frequency Pull-In Range		400		1000	Hz
$\pm\Delta f_H$	Frequency Holding Range	Typical Ranges	400		1000	Hz
df_o/dt_d	Slope of Phase Comparator Control Loop			2		kHz/μs
dt_d/dt_p	Gain of Phase Control			20		
t_p	Phase Shift Between Leading Edge of Composite Video Signal and Line Flyback Pulse (Note 2) Adjustable by V11	Typical Range	0		3.5	μs

Note 1: By modification of the frequency-determining network at pins 13 and 14, these ICs can also be used for other line frequencies.

Note 2: The limited flyback pulse should overlap the video signal sync pulse on both edges.

Functional Description

The sync separator separates the synchronizing pulses from the composite video signal. The noise inverter circuit, which needs no external components, in connection with an integrating and differentiating network frees the synchronizing signal from distortion and noise.

The frame sync pulse is obtained by multiple integration and limitation of the synchronizing signal, and is available at pin 7. The *RC* network, hitherto required between sync separator and frame oscillator is no longer needed. Since the frame sync pulse duration at pin 7 is subject to production spreads, it is recommended to use the leading edge of this pulse for triggering.

The frequency of the line oscillator is determined by a 10 nF polystyrene capacitor at pin 13 which is charged and discharged periodically by 2 internal current sources. The external resistor at pin 14 defines the charging current and consequently in conjunction with the oscillator capacitor the line frequency.

The phase comparator compares the sawtooth voltage of the oscillator with the line sync pulses. Simultaneously, an AFC voltage is generated which influences the oscillator frequency. A frequency range limiter restricts the frequency holding range.

The oscillator sawtooth voltage, which is in a fixed ratio to the line sync pulses, is compared with the flyback pulse in the phase control circuit, in this way compensating all drift of delay times in driver and line output stage. The correct phase position and hence the horizontal position of the picture can be adjusted by the 10 kΩ potentiometer connected to pin 11. Within the adjustable range the output pulse duration (pin 2) is constant. Any larger displacements of the picture, e.g., due to non-symmetrical picture tube, should not be corrected by the phase potentiometer, since in all cases the flyback pulse must overlap the sync pulse on both edges *(Figure 3)*.

Functional Description (Continued)

The switching stage has an auxiliary function. When the 2 signals supplied by the sync separator and the phase control circuit, respectively, are in synchronism, a saturated transistor is in parallel with the integrated 2 kΩ resistor at pin 9. Thus the time constant of the filter network at pin 4 increases and consequently reduces the pull-in range of the phase comparator circuit for the synchronized state to approximately 50 Hz. This arrangement ensures disturbance-free operation.

For video recording operation, this automatic switchover can be blocked by a positive current fed into pin 8, e.g., via a resistor connected to pin 3. It may also be useful to connect a resistor of about 680 Ω or 1 kΩ between pin 9 and earth. The capacitor at pin 4 may be lowered, e.g., to 0.1 μF. These alterations do not significantly influence the normal operation of the IC and thus do not need to be switched.

The output stage delivers at pin 2 output pulses of duration and polarity suitable for driving the line driver stage. If the supply voltage goes down (e.g., by switching off the mains) a built-in protection circuit ensures defined line frequency pulses down to V3 = 4V and shuts off when V3 falls below 4V, thus preventing pulses of undefined duration and frequency. Conversely, if the supply voltage rises, pulses defined in duration and frequency will appear at the output pin as soon as V3 reaches 4.5V. In the range between V3 = 4.5V and full supply the shape and frequency of the output pulses are practically constant.

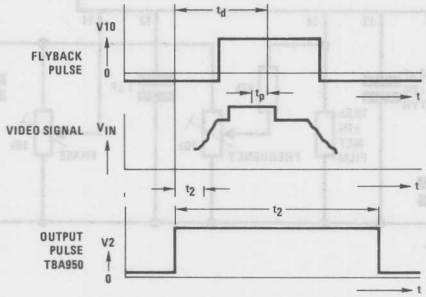
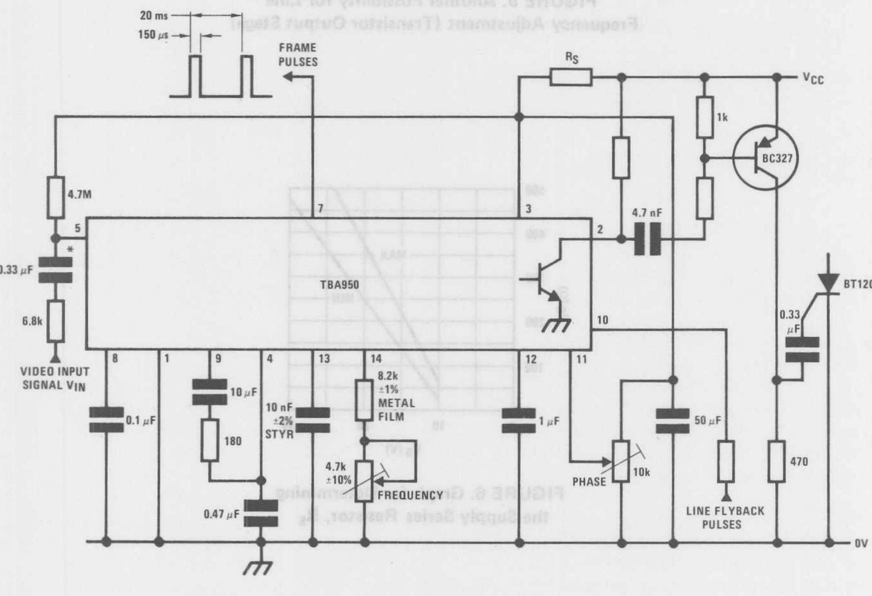


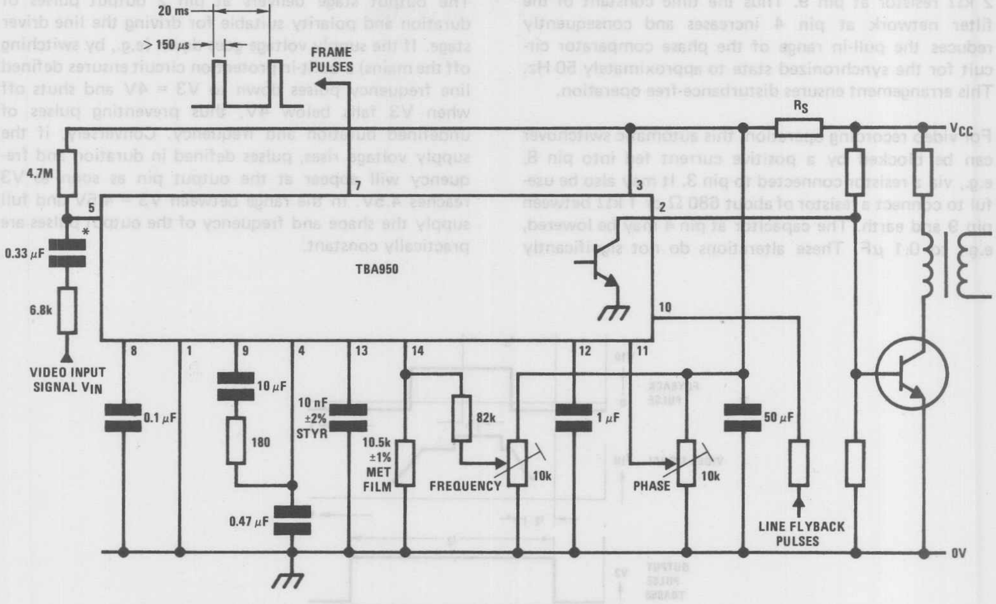
FIGURE 3. Phase Relationships



*Input circuitry must be optimized

FIGURE 4. Operating Circuit (Thyristor Output Stage)

Functional Description (Continued)



*Input circuitry must be optimized

FIGURE 5. Another Possibility for Line Frequency Adjustment (Transistor Output Stage)

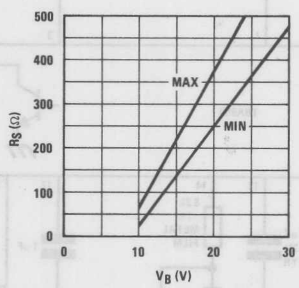


FIGURE 6. Graph for Determining the Supply Series Resistor, R_S

National Semiconductor

TBA970 Television Video Amplifier

General Description

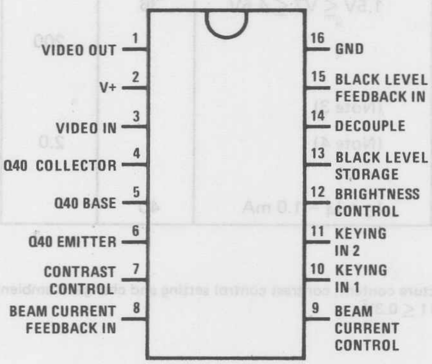
The TBA970 is a monolithic video amplifier for television receivers. The circuitry includes a video preamplifier, DC contrast control utilizing a linear potentiometer which can be ganged to the chroma gain control, beam current limiting via contrast. Beam current limiting could be obtained with either positive or negative control voltage. Black level control is achieved by a clamped feedback circuit combined with the brightness control. Emitter follower output could be used to directly drive the video output stage. A separate NPN transistor (Q40) is provided on the chip.

Features

- DC contrast control
- DC brightness control
- Black level clamping
- Beam current limiting
- Low impedance output

Connection Diagram

Dual-In-Line Package

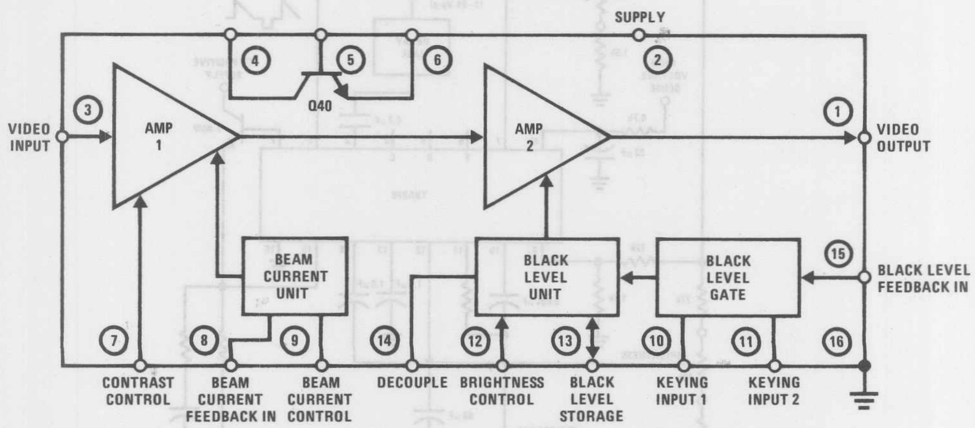


TOP VIEW

Dual-In-Line Package, Order Number TBA970
See NS Package N16A

Quad-In-Line Package, Order Number TBA970Q
See NS Package N16C

Block Diagram



Absolute Maximum Ratings

Supply Voltage	15.5V
Internal Power Dissipation	750 mW
Collector Current Q40	10 mA
Power Dissipation Q40	20 mW
V_{CEO} Q40	13.2V
V_{CES} Q40	15.5V
Operating Temperature Range	−20°C to +45°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 10 seconds)	260°C

Electrical Characteristics $T_A = 25°C$, $V^+ = 15V$, See Test Circuit, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_2	Supply Current	(Note 1)		27	36	mA
V3 p-p	Peak-to-Peak Input Voltage	(Note 2)			1.6	Vp-p
R3	Input Resistance			12		kΩ
	Voltage Gain			2.4		
	3.0 dB Bandwidth			6.0		MHz
	6.0 dB Bandwidth			9.0		MHz
	Linearity of Black-to-White Video Output Signal		0.9			
V15	Low Black Level Voltage				0.2	V
V15	High Black Level Voltage		3.0			V
	Contrast Control Range	$1.5V \leq V7 \leq 4.5V$	36			dB
R12	Input Resistance for Brightness Control			200		kΩ
ΔV15	Change of Black Level	(Note 3)			20	mV
V8, V9	DC Voltage for Beam Current Limiting Inputs	(Note 4)		2.0		V
	Separate Transistor Q40 Gain	$I_C = I_4 = 1.0$ mA	40			

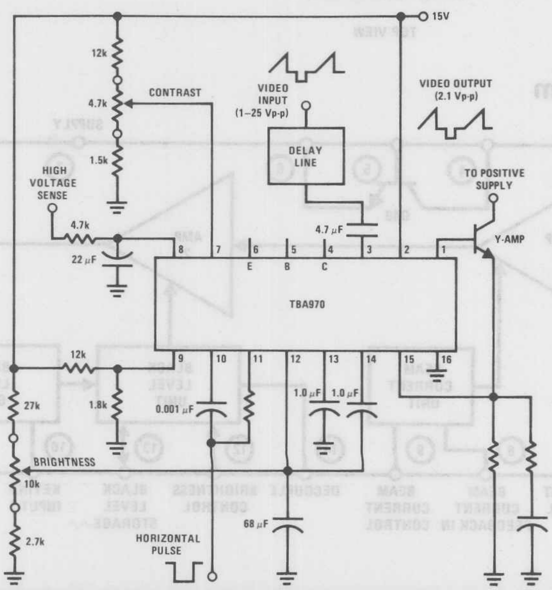
Note 1: No input signal and at minimum brightness.

Note 2: With negative-going synchronizing pulse.

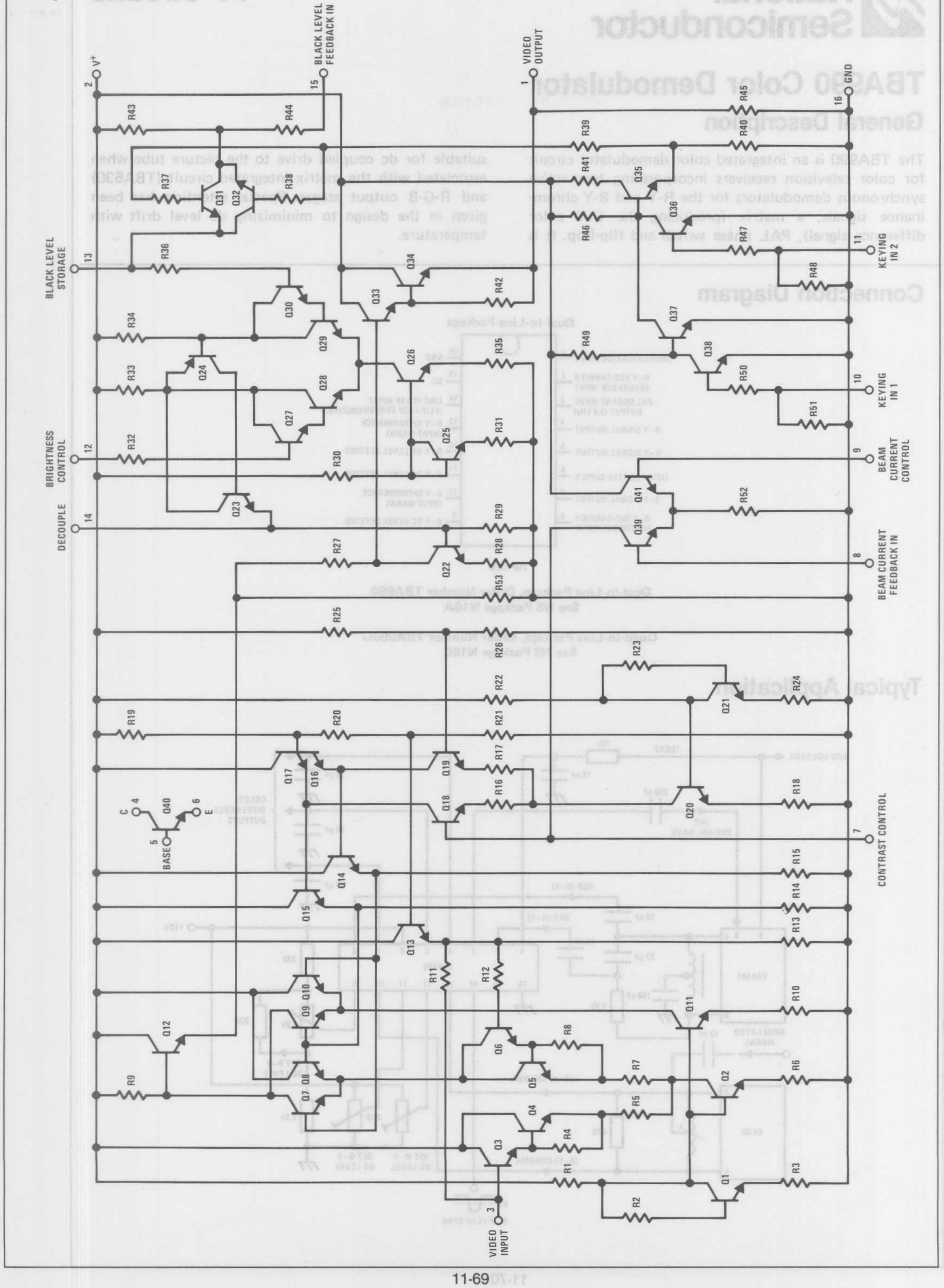
Note 3: With constant brightness setting, due to change of picture content, contrast control setting and change in ambient temperature (ΔT_A = 20°C); black level clamping with $t_c = 1\ \mu s$, $I_{10} \geq 0.25$ mA, $V11 \leq 0.3V$.

Note 4: Beam current limiting occurs at $V8 \geq V9$.

Test Circuit



Equivalent Circuit

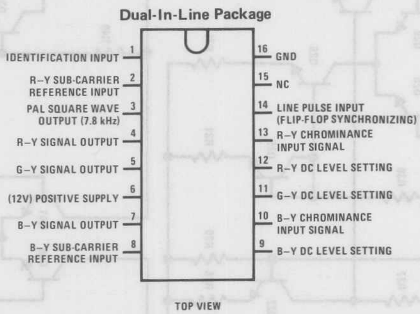


TBA990 Color Demodulator

General Description

The TBA990 is an integrated color demodulator circuit for color television receivers incorporating two active synchronous demodulators for the R-Y and B-Y chrominance signals, a matrix (producing the G-Y color difference signal), PAL phase switch and flip-flop. It is suitable for dc coupled drive to the picture tube when associated with the matrix integrated circuit (TBA530) and R-G-B output stages. Special attention has been given in the design to minimizing dc level drift with temperature.

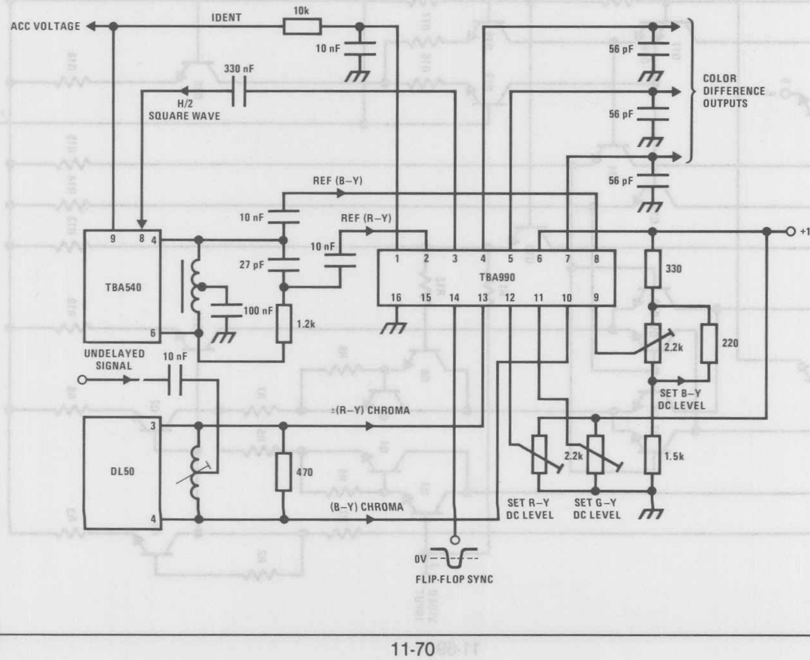
Connection Diagram



Dual-In-Line Package, Order Number TBA990
See NS Package N16A

Quad-In-Line Package, Order Number TBA990Q
See NS Package N16C

Typical Application



Pin Function Description

1. Identification bias. The PAL flip-flop is stopped, for identification purposes, when the voltage on pin 1 increases above 6V. This threshold is internally generated and has a porportional behavior with the 12V supply voltage. The threshold level of 6V is chosen to match the output characteristic of the TBA540 and has a sufficiently high safety margin above the zero chroma signal level of 4V to eliminate spurious identifying.

2. R-Y subcarrier reference input. A 1Vp-p signal is required via a dc blocking capacitor. Under no circumstances should this signal be less than 0.5 Vp-p. The input resistance at this pin is typically 5 kΩ.

3. PAL square wave output. The amplitude is 3Vp-p from an emitter follower. No external load resistor is required.

4. R-Y signal output (G-Y at pin 5 and B-Y at pin 7). These outputs require no external dc loads except that direct connection must be made via the low pass filters to the appropriate pins on the R-G-B matrix TBA530. In a complete circuit using the TBA530 and video output stages the dc levels of these outputs will be adjusted to give the correct setting of the picture tube drive black levels. The changes in dc level with supply voltage are proportional and track together.

The unwanted products of demodulation occurring in the color difference outputs are chiefly 8.86 MHz and harmonics together with a small amount of 4.43 MHz due to possible unbalance in the demodulators. To avoid possible troubles in the receiver because of radiation of these demodulation products from the R-G-B drive circuits, low-pass filters must be employed in each of the color difference outputs. The filters shown have a −3 dB bandwidth of 1 MHz, adequate attenuation of the 8.8 MHz component, and sufficient attenuation of the 4.4 MHz component to give less than 4 Vp-p amplitude at the picture tube cathodes.

5. G-Y signal output (see pin 4).

6. Positive supply. The maximum allowable voltage on this pin is 13.2V.

7. B-Y signal output (see pin 4).

8. B-Y subcarrier reference input. The requirements here are identical with those for pin 2.

9. DC level setting for B-Y output signal. This is a "common adjustment" which controls all three output dc levels together.

10. Chrominance B-Y input signal. An input signal of approximately 360 mVp-p (color bars) is required at this pin. The input resistance is greater than 800Ω and the input capacitance is less than 10 pF. The spread in gain of the internal circuitry in the chrominance channel is ±10% maximum.

11. DC level setting for G-Y output signal. This adjusts the G-Y output dc level relative to the B-Y dc level.

12. DC level setting for R-Y output signal. This adjusts the R-Y output dc level relative to the B-Y dc level.

13. Chrominance R-Y input signal. An input signal of approximately 500 mVp-p (color bars) is required at this pin. The input impedance and spread in gain is the same as for pin 9.

14. Line pulse input (flip-flop synchronizing). A waveform derived from the line timebase can be used for synchronizing providing that its amplitude lies between 2V and 5Vp-p. The trigger point occurs where the negative-going edge crosses approximately +0.6V. Prior to this sufficient current must be supplied to pin 14 to turn the input transistor fully on.

15. N.C. This pin should not be used for external connections.

16. Negative supply (earth).

National Semiconductor

TDA440 Video IF Amplifier

General Description

The integrated circuit has the following functions incorporated: 3 symmetrical IF (broad band) amplifier with first and second regulated stages, controlled color carrier demodulator; video post-amplifier with low pass response and output independent of supply fluctuations; gated AGC section for the IF amplifier; delayed regulated output voltage for the tuner pre-stage.

Features

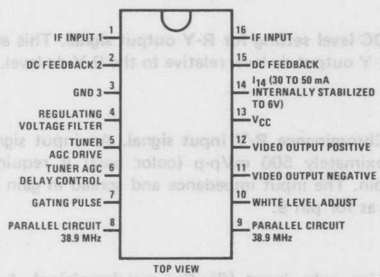
- High gain — high stability
- Constant input impedance indepedent of AGC
- Poor noise increase due to AGC action
- Negative video signal hardly affected by supply voltage variations
- Minimum RF breakthrough to video outputs
- Fast AGC action — gating largely independent of pulse shape and amplitude
- Very low intermodulation products
- Minimum differential error
- Positive as well as negative video signal available from low impedance outputs
- Integrated temperature compensating circuit
- DC output component adjustable (peak white)

Applications

- Video IF amplifier for color and monochrome television receivers

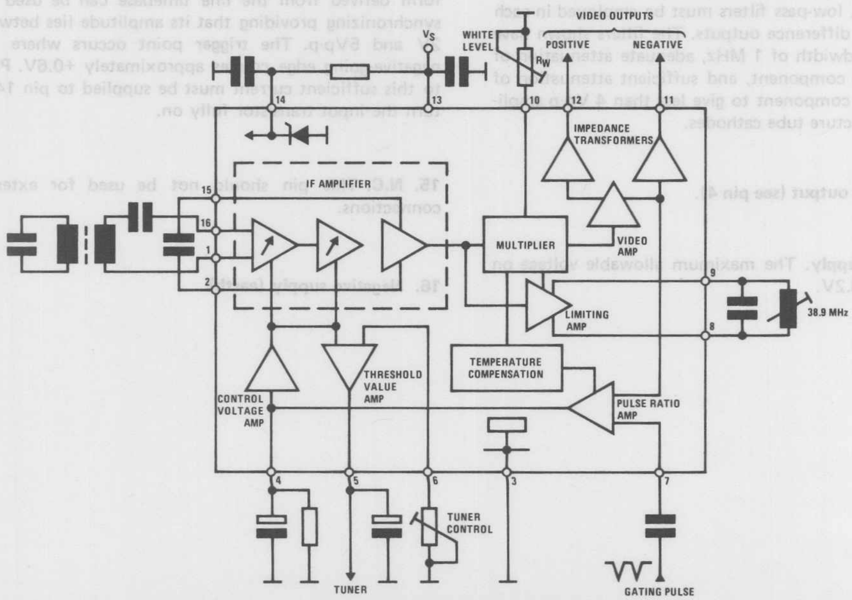
Connection and Block Diagrams

Dual-In-Line Package



Dual-In-Line Package, Order Number TDA440
See NS Package N16A

Quad-In-Line Package, Order Number TDA440Q
See NS Package N16C



Absolute Maximum Ratings

V_S, Supply Voltage Range (Pin 13)	10 to 15V
I_S, Supply Current of Low Voltage Stabilizer (Pin 14)	50 mA
V_Q, Open Loop Voltage (Pin 5)	15V
Video DC Output Current	
I_Q, Positive (Pin 12)	5 mA
I_Q, Positive (Pin 12)	30 mA
I_Q, Negative (Pin 11)	5 mA
I_Q, Negative (Pin 11)	30 mA
V_W, White Level Control (R_W) (Pin 10)	−1 to +3V
V_{EXT}, External Voltage (Pin 4)	3.2V
Power Dissipation	
P_{TOT}, $T_A \leq 55°C$	700 mW
T_J, Junction Temperature	125°C
T_A, Ambient Temperature Range	−25°C to +70°C
t_{STG}, Storage Temperature Range	−25°C to +125°C
Thermal Resistance	
R_{thJA}, Junction Ambient	100°C/W Max

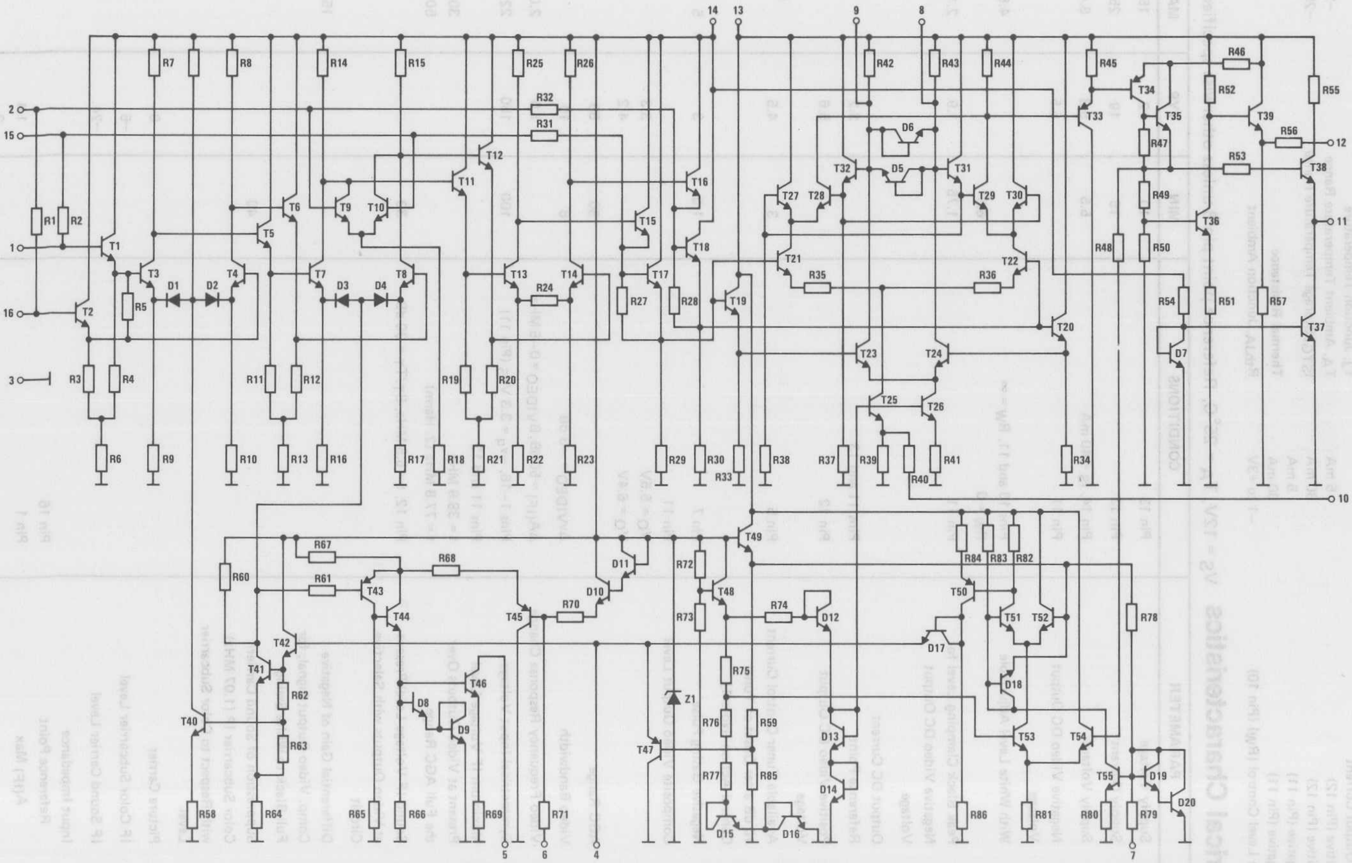
Electrical Characteristics $V_S = 12V$, $T_A = 25°C$, Reference point pin 3 unless otherwise specified

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_S	Supply Voltage	Pin 13	10	12	15	V
I_S	Supply Current	Pin 13	15	19	25	mA
V_S	Supply Voltage	Pin 14, I_S = 40 mA	5.5	5.8	6.4	V
V_Q	Negative Video DC Output Voltage	Pin 11		5.5		V
V_Q	With White Level Adjustable	Pins 10 and 11, $R_W = \infty$			4.8	V
		$R_W = 0$	6.5			V
V_Q	Peak Black Clamping Level for Negative Video DC Output Voltage	Pin 11	1.75	1.9	2.15	V
I_Q	Output DC Current Reference Point	Pins 11 and 13		3.2		mA
V_Q	Positive Video DC Output Voltage	Pin 12		5.6		V
I_Q	Available Tuner Control Current 10 dB after Onset of Tuner Control Action (Note 1)	Pin 5	3	4.5		mA
V_i	Negative Gating Pulse	Pin 7	1.5	3	5	V_{SS}
$-v_q$	Composite Video Output Level	Pin 11				
		V_Q = 5.5V		3.3		V_{SS}
		V_Q = 6.4V		4.2		V_{SS}
$\Delta A_{(IF)}$	AGC Range		50	56		dB
B_{VIDEO}	Video Bandwidth	$\Delta v_{VIDEO} = -3$ dB	8	10		MHz
Δv_{VIDEO}	Video Frequency Response Change	$\Delta A_{(IF)}$ = 50 dB, B_{VIDEO} = 0–5 MHz		1.0	2.0	dB
v_i	Symmetrical Input Voltage	Pins 1–16, $-v_q$ = 3.3 V_{SS} (Pin 11)	100	150	220	μV
	Maximum IF Voltage Level Present at Video Outputs Over the Full AGC Range	Pins 11 and 12				
		f = 38.9 MHz			30	mV
		f = 77.8 MHz (2. Harm)			50	mV
	Sound IF Voltage Level Present at Video Outputs with Selective Circuit	Pin 12, f = 5.5 MHz, B_T/T_T = 30 dB	30			mV
d	Differential Gain of Negative Comp. Video Output Signal, for Full Black to White Swing				15	%
a_{IM}	Suppression of Sound Carrier/ Color Subcarrier IP (1.07 MHz) with Respect to Color Subcarrier Level		40			dB
	Picture Carrier			0		dB
	IF Color Subcarrier Level			−6		dB
	IF Sound Carrier Level			−24		dB
	Input Impedance Reference Point	Pin 16				
R_i	$A_{(IF)}$ Max	Pin 1		1.4		kΩ
C_i				2		pF
R_i	$A_{(IF)}$ Min	Pin 1		1.4		kΩ
C_i				1.9		pF

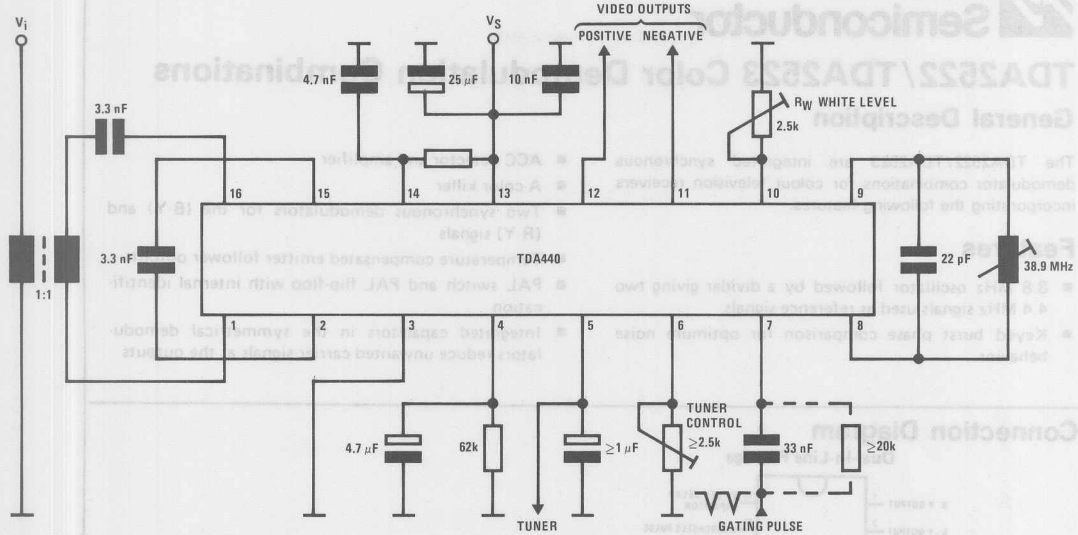
Note 1: On request $\geq$ 7 mA

T

Application Note for Reference Circuit to Improve Audio Interference and Cross Color Characteristics



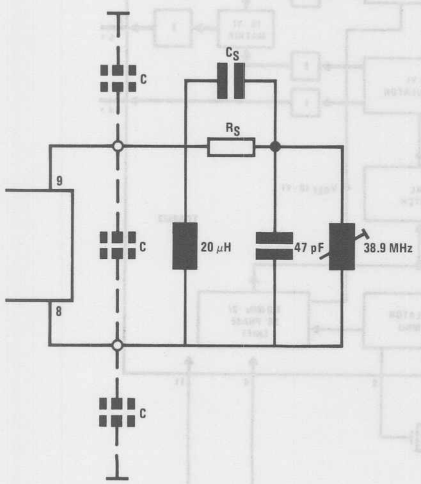
Test Circuit



Note. Supply voltage *must be disconnected* before inserting the integrated circuit in the socket.

Typical Application

Improved Tank Circuit to Reduce Audio Interference and Chroma Beat



C = Parasitic capacitance at pins 8 and 9 should be kept minimum

C_S = 6–10 pF -- series capacitance

f_o = 38.9–(1.8–2.75) MHz—series resonance frequency

R_S = 1.8–3.3 kΩ — series resonance damping determine the tuning characteristics

i.e., R_S = 2.4 kΩ tuning range, f = 3 MHz

National Semiconductor

TV Circuits

TDA2522/TDA2523 Color Demodulation Combinations

General Description

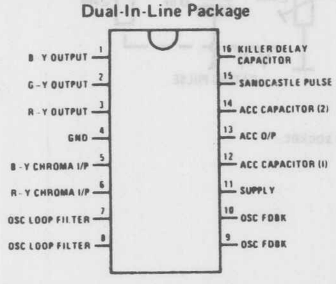
The TDA2522/TDA2523 are integrated synchronous demodulator combinations for colour television receivers incorporating the following features.

Features

- 8.8 MHz oscillator followed by a divider giving two 4.4 MHz signals used as reference signals
- Keyed burst phase comparison for optimum noise behavior
- ACC detector and amplifier
- A color killer
- Two synchronous demodulators for the (B-Y) and (R-Y) signals
- Temperature compensated emitter follower outputs
- PAL switch and PAL flip-flop with internal identification
- Integrated capacitors in the symmetrical demodulators reduce unwanted carrier-signals at the outputs

Connection Diagram

Dual-In-Line Package



TOP VIEW

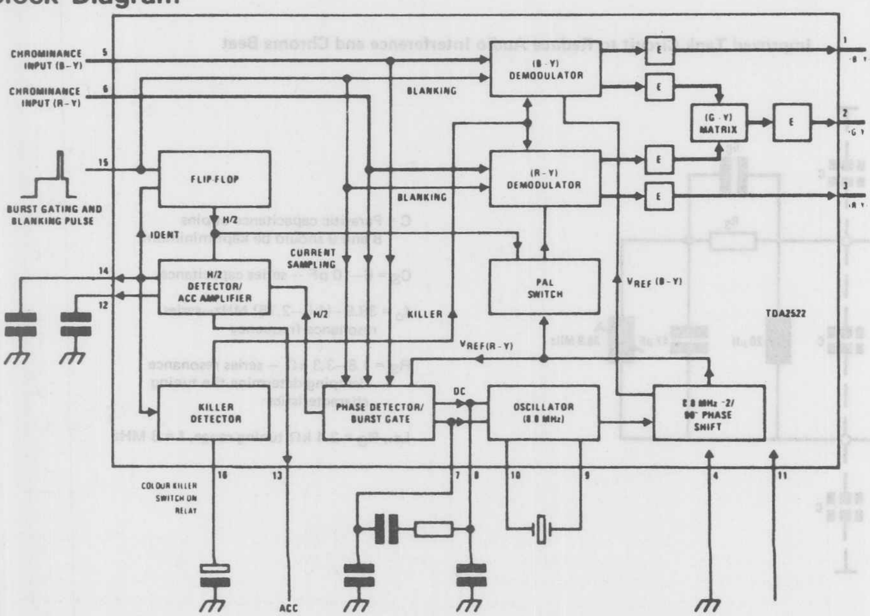
Dual-In-Line Package, Order Number TDA2522
See NS Package N16A

Quad-In-Line Package, Order Number TDA2522Q
See NS Package N16C

Dual-In-Line Package, Order Number TDA2523
See NS Package N16A

Quad-In-Line Package, Order Number TDA2523Q
See NS Package N16C

Block Diagram



NOTE: The outputs of the TDA2522 are −(B-Y), −(R-Y) and −(G-Y).
The outputs of the TDA2523 are (B-Y), (R-Y) and (G-Y).

Absolute Maximum Ratings

V11–4, Supply Voltage	14V
P_{TOT}, Total Power Dissipation (Note 3)	600 mW
T_{STG}, Storage Temperature	−20°C to +125°C
T_A, Operating Ambient Temperature	−20°C to +60°C

Electrical Characteristics V11–4 = 12V, T_A = 25°C

	PARAMETER	MIN	TYP	MAX	UNITS
	Supply Current		40		mA
	Demodulator Section				
	Ratio of Demodulator Signals				
B−Y/R−Y, $\frac{V1-4}{V3-4}$			1.78		
G-Y/R-Y, $\frac{V2-4}{V3-4}$	(Note 1)		0.85		
G-Y/R-Y, $\frac{V2-4}{V3-4}$	(Note 2)		0.17		
	Color Difference Output Signals, Peak-to-Peak Values				
R-Y, V3–4 (p-p)		2.40			V
G-Y, V2–4 (p-p)		1.35			V
B-Y, V1–4 (p-p)		3.00			V
	Impedance of Color Difference Signal Outputs				
|Z3–4|			250		Ω
|Z2–4|			250		Ω
|Z1–4|			250		Ω
	H/2 Ripple at R-Y Output (Peak-to-Peak Value)			10	mV
V15–4	Burst Keying Pulse (Positive-Going)	1.5			V
	Chrominance Input Signal (Including Burst) Peak-to-Peak Value				
R-Y, V6–4			500		mV
B-Y, V5–4			350		mV
	Reference Section				
	Phase Difference Between Reference Burst Signals for ±400 Hz Deviation of Crystal Frequency	−5		5	Deg.
	Holding Range with Typical Crystal		±500		Hz
V12–4	ACC Reference Voltage		7		V
	ACC Voltage with 0.5V Peak-to-Peak Burst				
V14–4	At Correct Phase		5.5		V
V14–4	With Zero Burst		7.0		V
V13–4	ACC Amplifier Output with 0.5V Peak-to-Peak Burst of Correct Phase			1.5	V
R_{G-F}	Oscillator Input Resistance		270		Ω
R_{H-F}	Oscillator Output Resistance		200		Ω

Note 1: The demodulators are driven by a chrominance signal of equal amplitude for the (R-Y) and the (B-Y) components. The phase of the (R-Y) chrominance signal equals the phase of the (R-Y) reference signal. The same holds for the (B-Y) signals.

Note 2: As under note 1, but the phase of the (R-Y) reference signal reversed.

Note 3: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 175°C/W junction to ambient.

TDA2530 R-G-B Matrix Preamplifier With Clamps

General Description

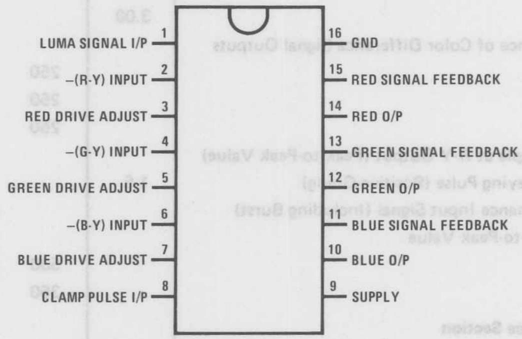
The TDA2530 is an integrated R-G-B matrix preamplifier for color television receivers, incorporating a matrix preamplifier for R-G-B cathode drive of the picture tube with clamping circuits. The TDA2530 has a base driver amplifier. Also, each channel follows an identical layout to ensure equal frequency behavior of the 3 channels.

This integrated circuit has been designed to be driven from the TDA2522 synchronous demodulator and oscillator integrated circuit.

The device is also available in a zig-zag quad-in-line package, this version being denoted by the suffix Q, i.e., TDA2530Q.

Connection Diagram

Dual-In-Line Package



TOP VIEW

Dual-In-Line Package, Order Number TDA2530
See NS Package N16A

Quad-In-Line Package, Order Number TDA2530Q
See NS Package N16C

Reference Data

Supply Voltage (Nominal)	12V
Operating Ambient Temperature Range	−25°C to +60°C
Gain of Luminance and Color-Difference Channels (Typical)	100

Absolute Maximum Ratings

Supply Voltage (V8–6 Maximum)	13.2V
Storage Temperature, T_{STG}	−25°C to +125°C
Operating Ambient Temperature, T_A	−25°C to +60°C

Electrical Characteristics $V8–6 = 12V, V1–16 = 1.5V, T_A = 25°C$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Gain of Color Channels (B-Y; G-Y; R-Y) at f = 0.5 MHz (Note 1)	G2–16		100		
	G4–16		100		
	G6–16		100		
Ratio of Gain of Luminance Amplifier to Color Amplifiers		0.9		1.1	
Input Resistance of Color Difference Amplifiers at f = 1 kHz	R2–6	100			kΩ
	R3–6	100			kΩ
	R4–6	100			kΩ
Input Resistance of Luminance Amplifier at f = 1 kHz	R5–6	100			kΩ

Note 1: G is defined as the voltage ratio between the input signals at the pins 2, 4 and 6 and the output signals at the collectors of the output transistors.

Pin Function Description

1. **Luminance signal input.** A 1V black to white positive-going luminance input signal is required. Blanking level should be at 1.5V and black level at 1.7V.

2. **−(R-Y) input signal.** The input signal is required to be AC coupled from a low impedance source such as the TDA2522. The coupling capacitor also acts as a clamp capacitor for the TDA2530 red output. As the color difference input impedance is at least 100 kΩ, low value coupling capacitors may be used.

3. **Red drive adjustment.** A gain variation of the red channel of at least ±3 dB about the typical, is obtained as the DC potential at this pin is varied by ±5V about the typical of 5V. If no connection is made to a gain controlling pin the channel concerned assumes the typical gain.

4. **−(G-Y) input signal (see pin 2).**

5. **Green drive adjustment (see pin 3).**

6. **−(B-Y) input signal (see pin 2).**

7. **Blue drive adjustment (see pin 3).**

8. **Clamp pulse input.** A positive-going line pulse input is required and the pulse should exceed a threshold DC level set by the TDA2530 of 7V. An input current of about 1 mA is required.

9. **Positive 12V supply.**

10. **Blue signal output.** The TDA2530 blue signal output has polarity appropriate for base drive of typical video output stages.

11. **Blue signal feedback.** The signal gain of both the video output stages and IC amplifier are stabilized by the feedback circuits. DC clamping is achieved by sampling of the feedback level during blanking. The black level potentials at the collectors of the video output stages may be varied independently by adjustable DC current sources applied to the feedback input pins. The DC levels at these pins are such that the feedback resistor and a resistor network between the 12V supply and earth provide a potential of 6V during blanking.

12. **Green signal output (see pin 10).**

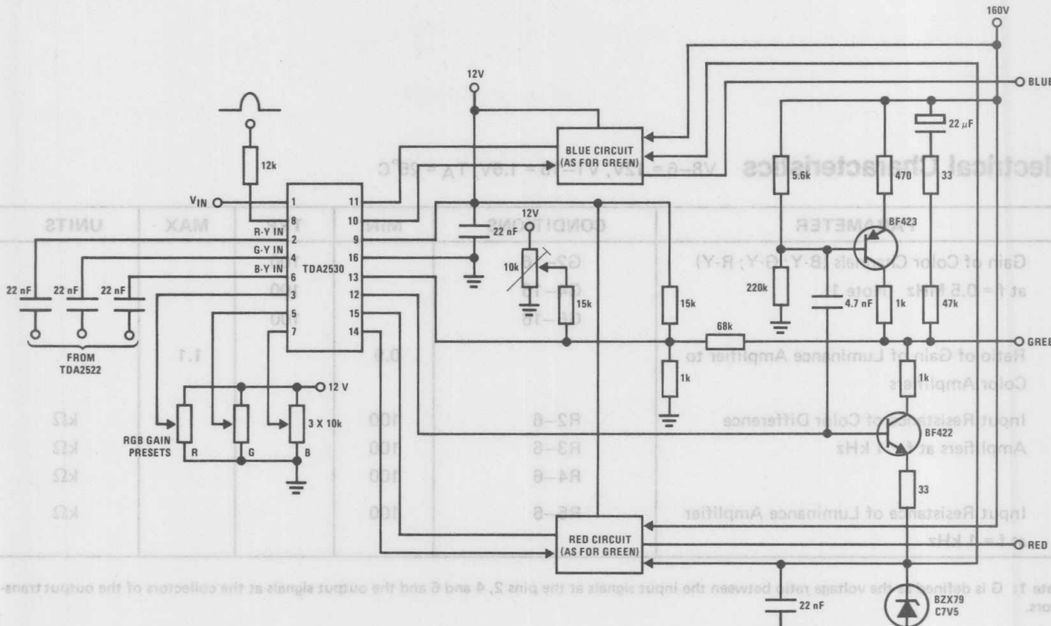
13. **Green signal feedback (see pin 11).**

14. **Red signal output (see pin 10).**

15. **Red signal feedback (see pin 11).**

16. **Negative supply (earth).**

Application Information (Peripheral Circuitry)



Note 1: Attention should be given to earth paths, avoiding common impedances betwen the input (decoder) side and the output stages.

Note 2: Printed track area connected to the feedback pins should be kept to a minimum.

Note 3: To ensure a matched performance of the video output stages, a symmetrical layout of the 3 stages should be employed.

National Semiconductor

TV Circuits

TDA2540 Video I.F. Amplifier and Demodulator

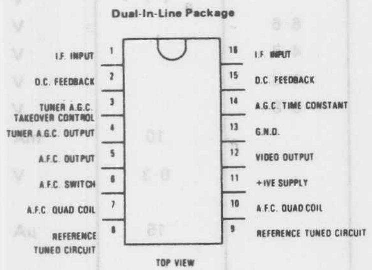
General Description

The TDA2540 is an i.f. amplifier and demodulator integrated circuit for colour and black and white television receivers using n-p-n tuners.

Features

- Wide-band gain-controlled i.f. amplifier.
- Synchronous demodulator.
- Video preamplifier with white spot and noise inverters.
- Noise gated a.g.c.
- a.f.c. circuit switched on/off by a dc level.
- a.g.c. output for n-p-n- tuners.
- V.C.R. switch allows insertion of VCR playback signal.

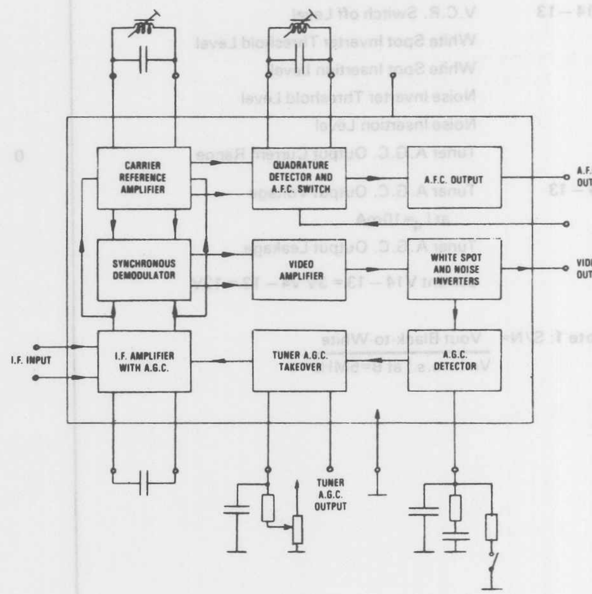
Connection Diagram



Dual-In-Line Package, Order Number TDA2540
See NS Package N16A

Quad-In-Line Package, Order Number TDA2540Q
See NS Package N16C

Block Diagram



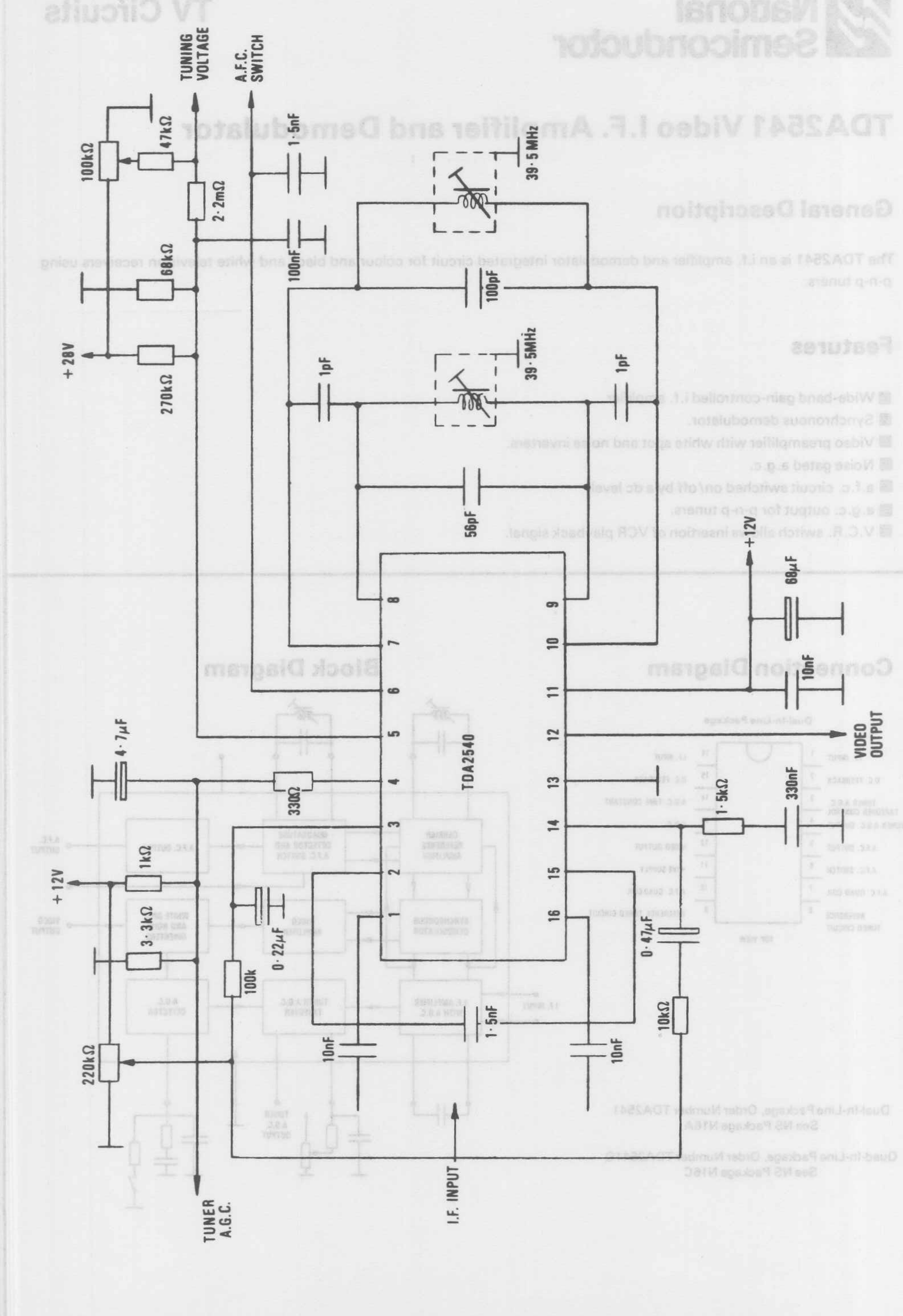
V11 – 13 Supply Voltage	14V
P_{TOT} Power Dissipation	900mW
T_{STG} Storage Temperature	– 55 to +125°C
Tamb Operating Ambient Temperature	–25 to +60°C

Electrical Characteristics V11 – 13 = 12V Tamb=25°C

PARAMETER		MIN	TYP	MAX	UNITS
V1 – 16 (r.m.s.)	I.F. Input Voltage for onset of A.G.C.		100	150	μV
V12 – 13	Zero Signal Output Level		6.0		V
	Top Sync Output Level	2.9		3.2	V
V6 – 13	A.F.C. Output Voltage Swing for ΔF=100KHz	10	11		V
	I.F. Voltage Gain Control Range		64		dB
S/N	Signal to Noise Ratio at V1=10mV (Note 1)		58		dB
B	3dB Bandwidth of Video Amplifier		6		MHz
ΔG	Differential Gain		4	10	%
ΔØ	Differential Phase		2	10	Deg.
	Carrier Signal at Video Output		4	30	mV
	2nd Harmonic of Carrier at Video Output		20	30	mV
	Intermodulation Ratio at 1·5 MHz	46			dB
V6 – 13	A.F.C. Switch off Level			2·5	V
V14 – 13	V.C.R. Switch off Level			1·1	V
	White Spot Inverter Threshold Level		6·6		V
	White Spot Insertion Level		4·7		V
	Noise Inverter Threshold Level		1·8		V
	Noise Insertion Level		3·8		V
I_4	Tuner A.G.C. Output Current Range	0		10	mA
V4 – 13	Tuner A.G.C. Output Voltage at I_4=10mA			0·3	V
I_4	Tuner A.G.C. Output Leakage current V14 – 13 = 3V V4 – 13 = 12V			15	μA

Note 1: $S/N = \dfrac{\text{Vout Black-to-White}}{\text{Vn (r.m.s.) at B=5MHz}}$

Application Information



National Semiconductor

TV Circuits

TDA2541 Video I.F. Amplifier and Demodulator

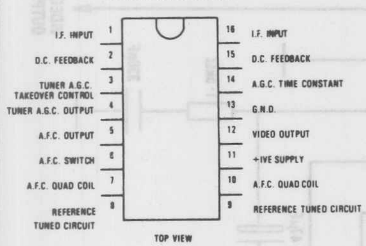
General Description

The TDA2541 is an i.f. amplifier and demodulator integrated circuit for colour and black and white television receivers using p-n-p tuners.

Features

- Wide-band gain-controlled i.f. amplifier.
- Synchronous demodulator.
- Video preamplifier with white spot and noise inverters.
- Noise gated a.g.c.
- a.f.c. circuit switched on/off by a dc level.
- a.g.c. output for p-n-p tuners.
- V.C.R. switch allows insertion of VCR playback signal.

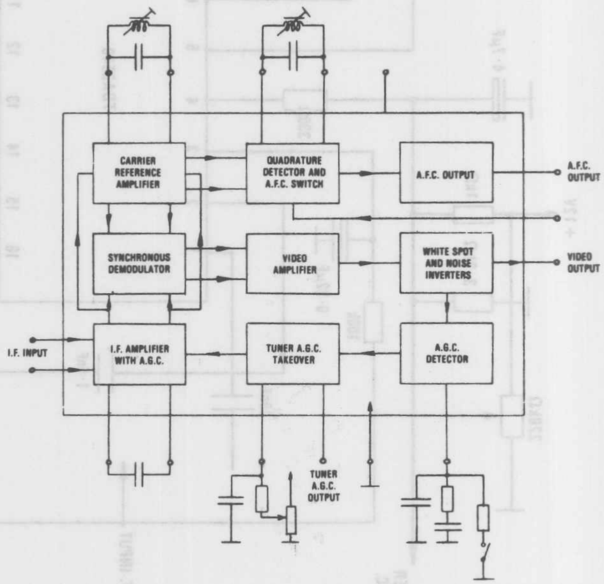
Connection Diagram



Dual-In-Line Package, Order Number TDA2541
See NS Package N16A

Quad-In-Line Package, Order Number TDA2541Q
See NS Package N16C

Block Diagram



Absolute Maximum Ratings

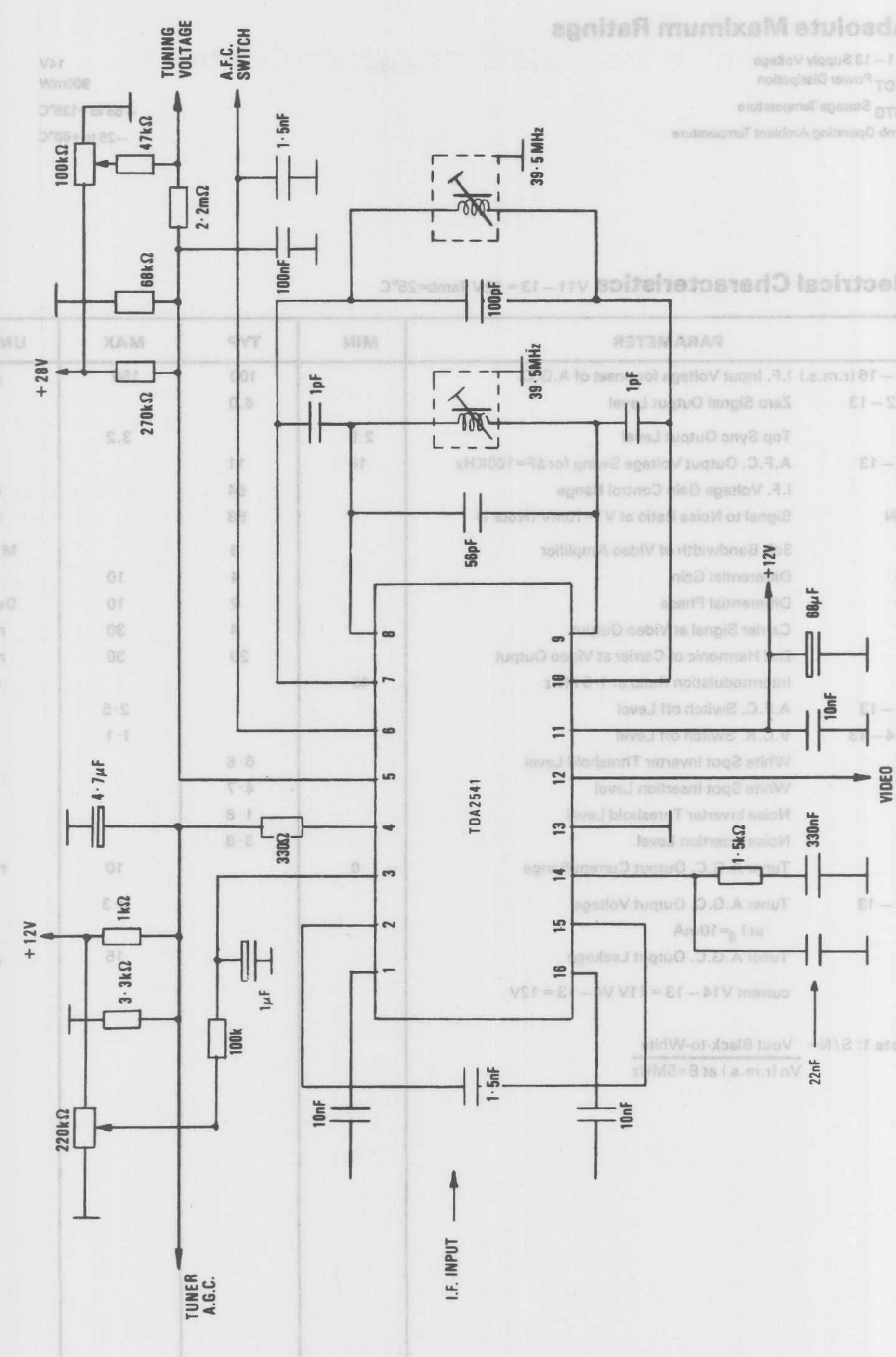
V11 – 13 Supply Voltage	14V
P_{TOT} Power Dissipation	900mW
T_{STG} Storage Temperature	–55 to +125°C
Tamb Operating Ambient Temperature	–25 to +60°C

Electrical Characteristics V11 – 13 = 12V Tamb=25°C

PARAMETER		MIN	TYP	MAX	UNITS
V1 – 16 (r.m.s.)	I.F. Input Voltage for onset of A.G.C.		100	150	µV
V12 – 13	Zero Signal Output Level		6.0		V
	Top Sync Output Level	2.9		3.2	V
V6 – 13	A.F.C. Output Voltage Swing for ΔF=100KHz	10	11		V
	I.F. Voltage Gain Control Range		64		dB
S/N	Signal to Noise Ratio at V1=10mV (Note 1)		58		dB
B	3dB Bandwidth of Video Amplifier		6		MHz
ΔG	Differential Gain		4	10	%
ΔØ	Differential Phase		2	10	Deg.
	Carrier Signal at Video Output		4	30	mV
	2nd Harmonic of Carrier at Video Output		20	30	mV
	Intermodulation Ratio at 1·5 MHz	46			dB
V6 – 13	A.F.C. Switch off Level			2·5	V
V14 – 13	V.C.R. Switch off Level			1·1	V
	White Spot Inverter Threshold Level		6·6		V
	White Spot Insertion Level		4·7		V
	Noise Inverter Threshold Level		1·8		V
	Noise Insertion Level		3·8		V
I_4	Tuner A.G.C. Output Current Range	0		10	mA
V4 – 13	Tuner A.G.C. Output Voltage at I_4=10mA			0·3	V
I_4	Tuner A.G.C. Output Leakage current V14 – 13 = 11V V4 – 13 = 12V			15	µA

Note 1: $S/N = \dfrac{\text{Vout Black-to-White}}{\text{Vn (r.m.s.) at B=5MHz}}$

Application Information



TDA2560 Luminance and Chrominance Control Combination

General Description

The TDA2560 is a monolithic integrated circuit for use in decoding systems of color television receivers. The circuit consists of a luminance and chrominance amplifier. The luminance amplifier has a low input impedance so that matching of the luminance delay line is very easy.

Features

- DC contrast control
- Brightness control
- Black level clamp
- Blanking
- Additional video output with positive-going sync

The chrominance amplifier comprises:

- Gain controlled amplifier
- Chrominance gain control tracked with contrast control
- Separate DC saturation control
- Combined chroma and burst output, burst signal amplitude not affected by contrast and saturation control
- The delay line can directly be driven by the IC

Connection Diagram

Dual-In-Line Package

TOP VIEW

Dual-In-Line Package, Order Number TDA2560
See NS Package N16A

Quad-In-Line Package, Order Number TDA2560Q
See NS Package N16C

Absolute Maximum Ratings

V8–5, Supply Voltage	14V
T_{STG}, Storage Temperature	−55°C to +125°C
T_A, Operating Ambient Temperature	−25°C to +70°C

Electrical Characteristics

PARAMETER		MIN	TYP	MAX	UNITS
V8–5	Supply Voltage Range	9	12	14	V
I_8	Supply Current		46		mA
V8–5 (p-p)	Allowable Hum on Supply Line (Peak-to-Peak Value)			100	mA
The following data are measured at V8 = 12V, T_A = 25°C					
	Luminance Amplifier				
$I_{R(p\text{-}p)}$	Input Current; Black-to-White Level (Peak-to-Peak Value)		0.2		mA
|Z|	Input Impedance		75		Ω
	Gain (Pin D), (Note 1)				
V6–5	Burst Signal (Peak-to-Peak Value)			6	V
	Contrast Control Range	20			dB
V11	Brightness Control Range (Black Level)	1		3	V
	Black Level Stability When Changing Contrast, Video Contents and Temperature		±20		mV
B	Bandwidth (−3 dB)		5		MHz
V15–5	Output Voltage (Additional; Positive-Going Sync) Peak-to-Peak Value		3.4		V
V7–5	Black Level Clamp Pulse (Note 2)		6		V
	Blanking Pulse (Note 3)				
V9	At 0V at the Output		2		V
V9	At 1.5V at the Output		5		V
	Chrominance Amplifier				
V1–2 (p-p)	Input Signal Range (Peak-to-Peak Value)	4		80	mV
V6–5 (p-p)	Obtainable Chrominance Output Signal (Note 4) Peak-to-Peak Value		2		
	Ratio of Burst and Chrominance at Nominal Contrast and Saturation, (Note 5)				
V3–5	ACC Starting Voltage (Note 6)		1.2		V
	ACC Range	30			dB
	Tracking with Contrast Control (10 dB Control)	−1		1	dB
	Saturation Control Range	20			dB
V7–5	Burst Gate Pulse (Note 2)		1.5		V
S/N	Signal to Noise Ratio at Nominal Input Voltage	50			dB
	Phase of Burst to Chrominance	−5		5	Deg.

Note 1: The gain of the luminance amplifier can be adjusted, by setting the gain of the contrast control circuit by selection of discrete resistor R_G (see also circuits on pages xx and xx). This circuit configuration has been chosen to reduce the spread of the gain to a minimum (main cause of spread is now the spread of the ratio of the delay line matching resistors and the resistor R_G). At R_G = 2.7 kΩ the output voltage at nominal contrast (maximum − 3 dB) is 3V black to white.

Note 2: This pin (7) is used for burst gate and black level clamping. The latter function is actuated at a 6V level. The input pulse must have such an amplitude that the clamping circuit is active only during the back porch of the blanking interval. The burst gate, which switches the gain of the chroma amplifier to maximum during the flyback time, is actuated at a 1.5V level.

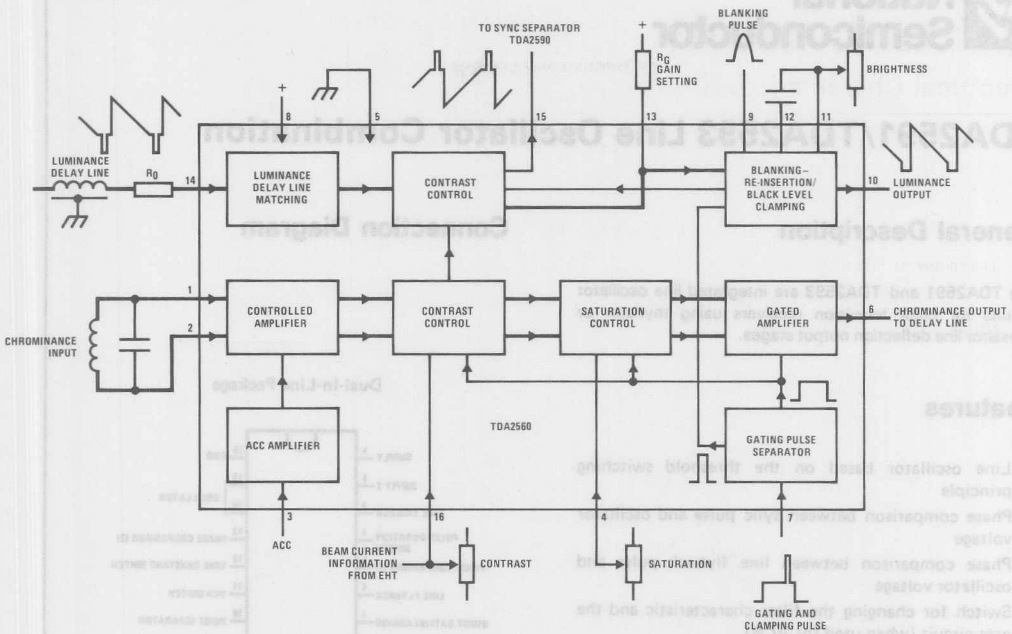
Note 3: This pin (9) is used for blanking the luminance amplifier. When the input pulse exceeds the 2V level the output signal is blanked to a level of about 0V. When the input exceeds a 5V level, a fixed level of about 1.5V is available at the output. This level can be used for clamping purposes.

Note 4: The chrominance and burst signal are both available on this pin (6). The burst signal is not affected by the contrast and saturation control and is kept constant by the ACC circuit of the TDA2522. The output signal amplitude is, therefore, determined by the losses in the delay line. At nominal contrast and saturation setting, the burst to chrominance ratio at the output is typically identical to the ratio at the input.

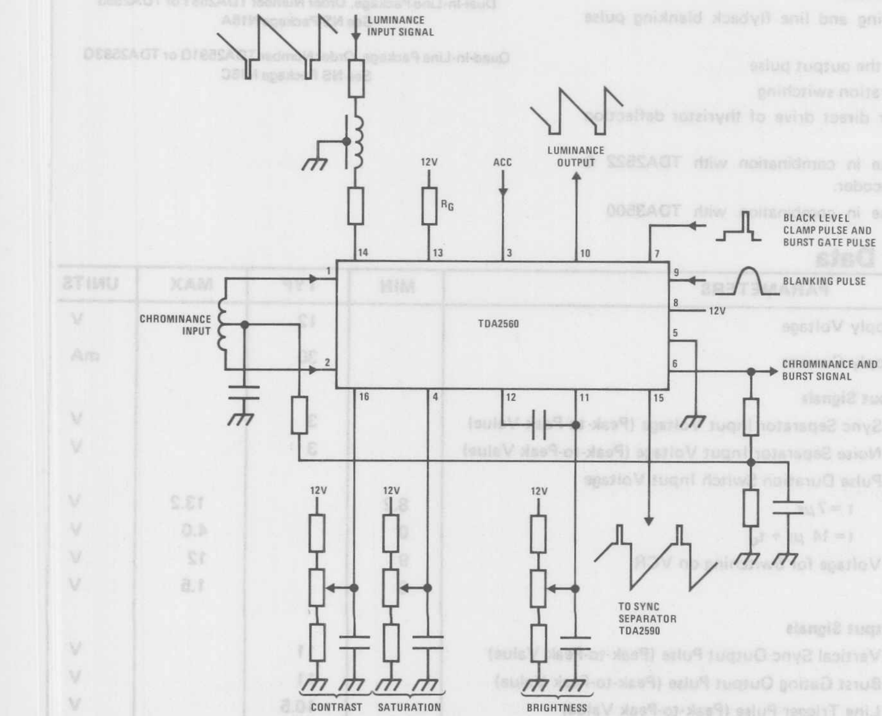
Note 5: Nominal contrast is specified as maximum contrast −3 dB. Nominal saturation is specified as maximum saturation −6 dB.

Note 6: A negative-going control voltage gives a decrease in gain.

Block Diagram



Application Information



Semiconductor

TDA2591/TDA2593 Line Oscillator Combination

General Description

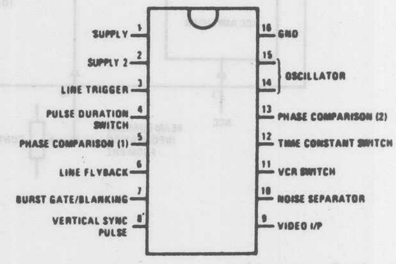
The TDA2591 and TDA2593 are integrated line oscillator circuits for color television receivers using thyristor or transistor line deflection output stages.

Features

- Line oscillator based on the threshold switching principle
- Phase comparison between sync pulse and oscillator voltage
- Phase comparison between line flyback pulse and oscillator voltage
- Switch for changing the filter characteristic and the gate circuit (when used for VCR)
- Coincidence detector
- Sync separator
- Noise separator
- Vertical sync separator
- Color burst keying and line flyback blanking pulse generator
- Phase shifter for the output pulse
- Output pulse duration switching
- Output stage for direct drive of thyristor deflection circuits
- TDA2591 for use in combination with TDA2522 & TDA2560 PAL decoder.
- TDA2593 for use in combination with TDA3500 PAL decoder.

Connection Diagram

Dual-In-Line Package



TOP VIEW

Dual-In-Line Package, Order Number TDA2591 or TDA2593
See NS Package N16A

Quad-In-Line Package, Order Number TDA2591Q or TDA2593Q
See NS Package N16C

Reference Data

PARAMETERS		MIN	TYP	MAX	UNITS
V1–16	Supply Voltage		12		V
I_1	Supply Current		30		mA
	Input Signals				
V9–16 (p-p)	Sync Separator Input Voltage (Peak-to-Peak Value)		3		V
V10–16 (p-p)	Noise Separator Input Voltage (Peak-to-Peak Value)		3		V
	Pulse Duration Switch Input Voltage				
V4–16	$t = 7\,\mu s$	8.2		13.2	V
V4–16	$t = 14\,\mu s + t_d$	0		4.0	V
V11–16	Voltage for Switching on VCR	9		12	V
		0		1.5	V
	Output Signals				
V8–16 (p-p)	Vertical Sync Output Pulse (Peak-to-Peak Value)		11		V
V7–16 (p-p)	Burst Gating Output Pulse (Peak-to-Peak Value)		11		V
V3–16 (p-p)	Line Trigger Pulse (Peak-to-Peak Value)		10.5		V

Absolute Maximum Ratings

Voltages	
V1–16, Supply Voltage at Pin 1 (When Supplied by the IC)	13.2V
V2–16, Supply Voltage at Pin 2	18V
V4–16, Pin 4 Voltage	0 to 13.2V
V9–16, Pin 9 Voltage	−6 to +6V
V10–16, Pin 10 Voltage	−6 to +6V
V11–16, Pin 11 Voltage	0 to 13.2V
Currents	
I_{2M}, Pin 2 Current (Peak Value)	650 mA
I_{3M}, Pin 3 Current (Peak Value)	650 mA
I_4, Pin 4 Current	1 mA
$\pm I_6$, Pin 6 Current	10 mA
I_7, Pin 7 Current	10 mA
I_{11}, Pin 11 Current	2 mA
Power Dissipation	
P_{TOT}, Total Power Dissipation (Note 6)	800mW
Temperatures	
T_{STG}, Storage Temperature	−25°C to +125°C
T_A, Operating Ambient Temperature	−20° to +60°C

Electrical Characteristics V1–16 = 12V; T_A = 25°C

	PARAMETER	MIN	TYP	MAX	UNITS
REQUIRED INPUT SIGNALS					
	Sync Separator				
V9–16	Input Switching Voltage		0.8		V
I_9	Input Switching Current	5		100	μA
I_9	Input Blocking Current at V9–16 = −5V		<1		μA
	Noise Separator				
V10–16	Input Keying Voltage		1.0		V
V10–16	Input Switching Voltage		1.4		V
I_{10}	Input Keying Current	5		100	μA
I_{10}	Input Switching Current		150		μA
I_{10}	Input Blocking Current at V10–16 = −5V		<1		μA
	Line Flyback Pulse				
I_6	Input Current		>10		μA
V6–16	Input Switching Voltage		0.8		V
V6–16	Input Limiting Voltage	−0.7		1.4	V
R6–16	Input Resistance		0.4		kΩ
	Pulse Duration Switch				
	For t = 7 μs				
V4–16	Input Voltage	8.2		13.2	V
I_4	Input Current		>200		μA
	For t = 14 μs + t_d				
V4–16	Input Voltage	0		4.0	V
$-I_4$	Input Current		>200		μA
	For t = 0; V4–16 = 0				
V4–16	Input Voltage, (Note 1)		6.0		V
I_4	Input Current (Input Open)		0		μA
	Switching on VCR				
V11–16	Input Voltage, (Note 2)	0		1.5	V
V11–16		9		13.2	V
$-I_{11}$	Input Current, (Note 2)		>200		μA
I_{11}		1		2	mA
DELIVERED OUTPUT SIGNALS					
	Vertical Sync Pulse (Positive-Going)				
V8–16 (p-p)	Output Voltage (Peak-to-Peak Value)	10	11		V
R8	Output Resistance		2		kΩ
	Burst Gating Pulse (Positive-Going)				
V7–16	Output Voltage (Peak-to-Peak Value)	10	11		V
R7	Output Resistance		70		Ω

Electrical Characteristics (Continued)

	PARAMETER	MIN	TYP	MAX	UNITS
	DELIVERED OUTPUT SIGNALS (CONTINUED)				
	Blanking Pulse				
V_{7-16} (p-p)	Output Voltage (Peak-to-Peak Value) TDA 2591		3.0		V
	TDA2593		4.5		V
R_7	Output Resistance		70		Ω
	Line Trigger Pulse (Positive-Going)				
V_{3-16} (p-p)	Output Voltage (Peak-to-Peak Value)		10.5		V
$I_{3(AV)}$	Output Current (Average Value), (Note 3)		100		mA
R_{3-16}	Output Resistance for Leading Edge of Line Pulse		2.5		Ω
R_{3-16}	Output Resistance for Trailing Edge of Line Pulse		20		Ω
	Oscillator				
V_{14-16}	Threshold Voltage Low Level		4.4		V
V_{14-16}	Threshold Voltage High Level		7.6		V
$\pm I_{14}$	Discharge Current		0.47		mA
V_{15-16}	Current Source Supply Voltage		6.0		V
$-I_{15}$	Current Source Supply Current		0.5		mA
	Phase Comparison (φ1; Sync Pulse-Oscillator)				
V_{13-16}	Control Voltage Range	3.8		8.2	V
$\pm I_{13M}$	Control Current (Peak Value)	1.9	2.1	2.3	mA
I_{13}	Output Blocking Current				
	At V_{13-16} = 4–8V			1	μA
	Output Resistance				
	At V_{13-16} = 4–8V, High Ohmic (Note 4)				
	At V_{13-16} < 3.8V or > 8.2V, Low Ohmic, (Note 5)				
	Time Constant Switch				
V_{12-16}	Output Voltage		6		V
$\pm I_{12}$	Output Current			1	mA
	Output Resistance				
R_{12-16}	At V_{11-16} = 2.5 to 7V		0.1		kΩ
R_{12-16}	At V_{11-16} < 1.5V or > 9V		60		kΩ
	Coincidence Detector (φ3)				
V_{11-16}	Output Voltage	0.5		6	V
	Output Current (Peak Value)				
I_{11M}	Without Coincidence		0.1		mA
$-I_{11M}$	With Coincidence		0.5		mA
	Phase Comparison (φ2; Oscillator-Line Flyback Pulse)				
V_{5-16}	Control Voltage Range	5.4		7.6	V
$\pm I_5$	Control Current (Peak Value)		1		mA
	Output (Input) Resistance				
	At V_{5-16} = 5.4 to 7.6V, High Ohmic, (Note 4)				
R_{5-16}	At V_{5-16} < 5.4V or > 7.6V		8		kΩ
	Input Current at Blocked Phase Detector				
I_5	V_{5-16} = 6.5V			5	μA

Note 1: Can also be not connected.

Note 2: When supplied by the IC.

Note 3: Higher values are allowed when reducing P_{tot}.

Note 4: Current source.

Note 5: Emitter follower.

Note 6: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 175°C/W junction to ambient.

Applications Information

	PARAMETER	MIN	TYP	MAX	UNITS
	Sync Separator				
V9−16 (p-p)	Input Voltage (Without Video; Peak-to-Peak Value)	1	3	7	V
I_9	Input Keying Control			100	μA
	Noise Signal Keying				
V10−16 (p-p)	Input Voltage (Without Video; Peak-to-Peak Value)	1	3	7	V
I_{10}	Input Keying Current			100	μA
$V_{n(p\text{-}p)}$	Superimposed Noise Voltage (Peak-to-Peak Value)			7	V
	Vertical Sync Pulse Separator				
t_{ON}	Delay Between Leading Edge of Input and Output Signal		12		μs
t_{OFF}	Delay Between Trailing Edge of Input and Output Signal	t_{ON}			μs
V8−16 (p-p)	Output Voltage (Peak-to-Peak Value)	10	11		V
R8−16	Output Resistance		2		kΩ
	Oscillator				
f_o	Frequency; Free Running (C14-16 = 4.7 nF, R15−16 = 12 kΩ)		15.625		kHz
$\Delta f_o/f_o$	Spread of Frequency, (Note 7)		<±5		%
$\Delta f_o/\Delta I_{15}$	Frequency Control Sensitivity		31		Hz/μA
$\Delta f_o/f_o$	Adjustment Range of Network in *Figure 1*		±10		%
$\frac{\Delta f_o/f_o}{\Delta V/V_{TYP.}}$	Influence of Supply Voltage on Frequency at V1−16 = 12V, (Note 7)			5	%
Δf_o	Change of Frequency when V1−16 Drops to 4V			10	%
	Phase Comparison (φ1; Sync Pulse-Oscillator)				
	Control Sensitivity		2		kHz/μs
	Spread of Control Sensitivity, (Note 7)		±10		%
Δf	Catching and Holding Range (82 kΩ)		±780		Hz
$\Delta f/f$	Spread of Catching and Holding Range, (Note 7)		±10		%
	Phase Comparison (φ2; Oscillator-Line Flyback Pulse)				
t_d	Permissible Delay Between Leading Edge of Output Pulse and Leading Edge of Flyback Pulse			15	μs
$\Delta t/\Delta t_d$	Static Control Error		<0.2		%
	Overall Phase Relation				
t	Phase Relation Between Middle of Sync Pulse and the Middle of the Flyback Pulse		2.6		μs
|Δt|	Tolerance of Phase Relation			0.7	μs
	Adjustment Sensitivity, Caused By: (Note 8)				
$\Delta V5-16/\Delta t$	Adjustment Voltage		0.1		V/μs
$\Delta I_5/\Delta t$	Adjustment Current		30		μA/μs
	Spread of Adjustment Current, (Note 7)		<10		%
	Burst Gating Pulse				
t	Phase Relation Between Middle of Sync Pulse at the Input and the Leading Edge of the Burst Gating Pulse; V7−16 = 7V	2.15	2.65	3.15	μs
t7	Burst Gating Pulse Duration		4.0		μs

	PARAMETER	MIN	TYP	MAX	UNITS
	Line Trigger Pulse				
	Output Pulse Duration				
t_p	At V4–16 > 8.2V	5.5	7	8.5	μs
t_p	At V4–16 < 4V		14 + td		μs
V1–16	Supply Voltage for Switching Off the Output Pulse		4		V
	Internal Gating Pulse				
t_p	Pulse Duration		7.5		μs

Note 7: Exclusive external components tolerances.

Note 8: The adjustment of the overall phase relation and consequently the leading edge of the output pulse occurs automatically by phase control φ2. The values beyond this point count if additional adjustment is required.

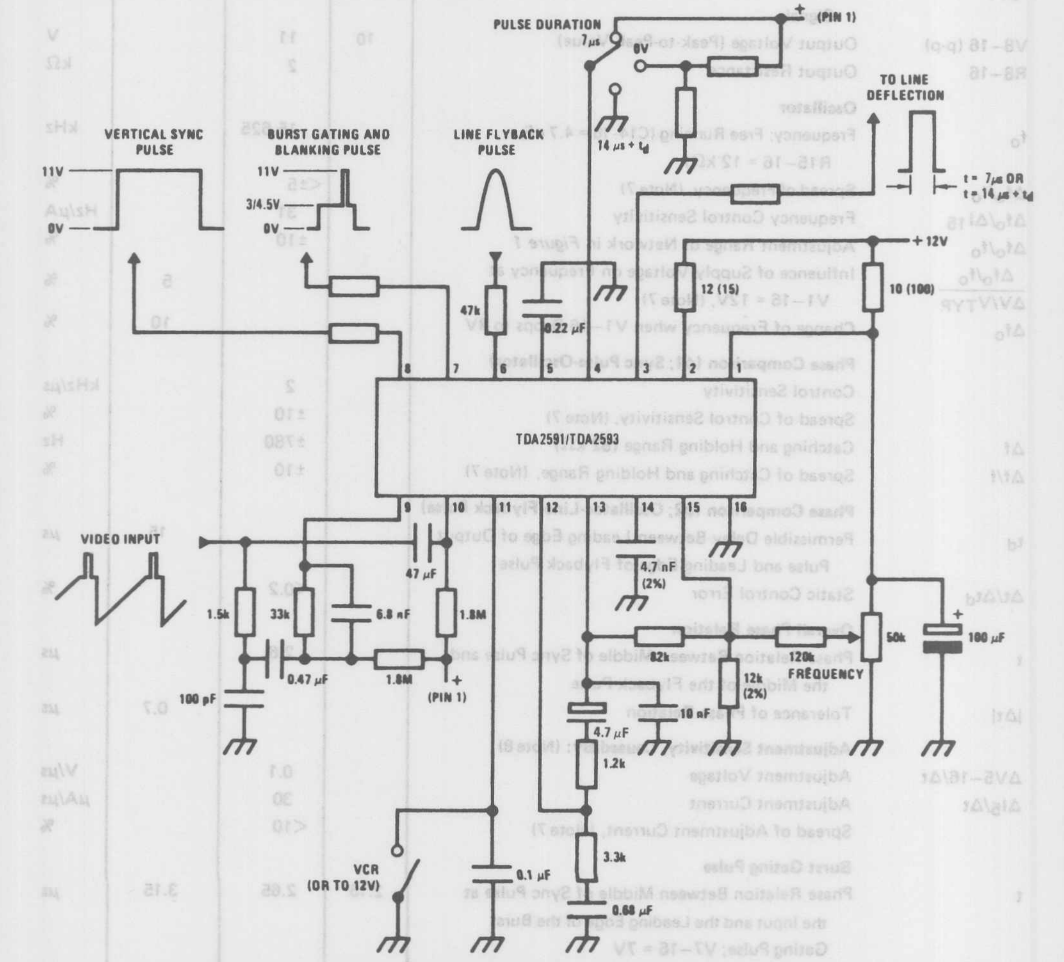
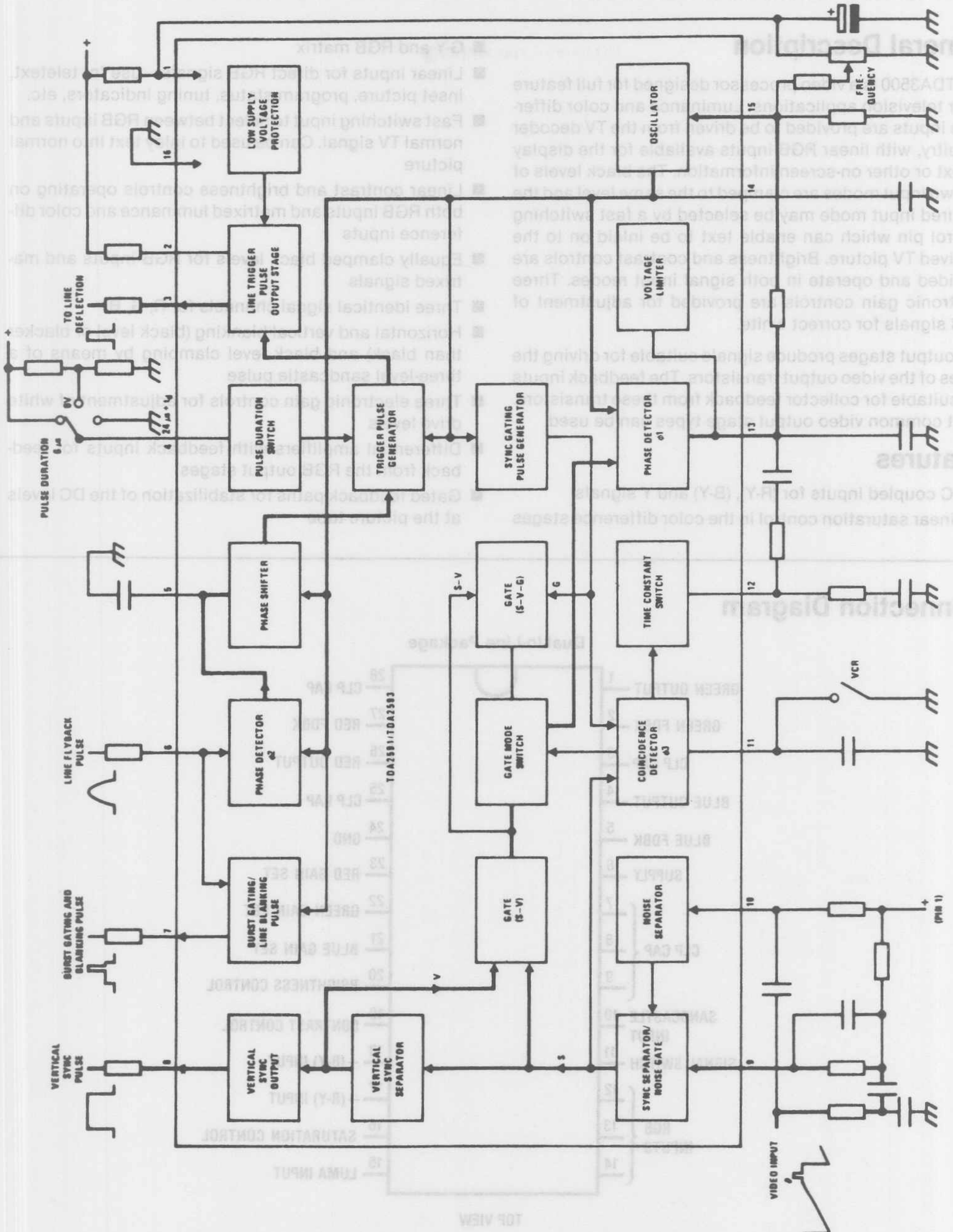


FIGURE 1

Block Diagram



National Semiconductor

TDA3500 Chroma Processor + RGB Drive Combination

General Description

The TDA3500 is a video processor designed for full feature color television applications. Luminance and color difference inputs are provided to be driven from the TV decoder circuitry, with linear RGB inputs available for the display of text or other on-screen information. The black levels of the two input modes are clamped to the same level and the required input mode may be selected by a fast switching control pin which can enable text to be inlaid on to the received TV picture. Brightness and contrast controls are provided and operate in both signal input modes. Three electronic gain controls are provided for adjustment of RGB signals for correct white.

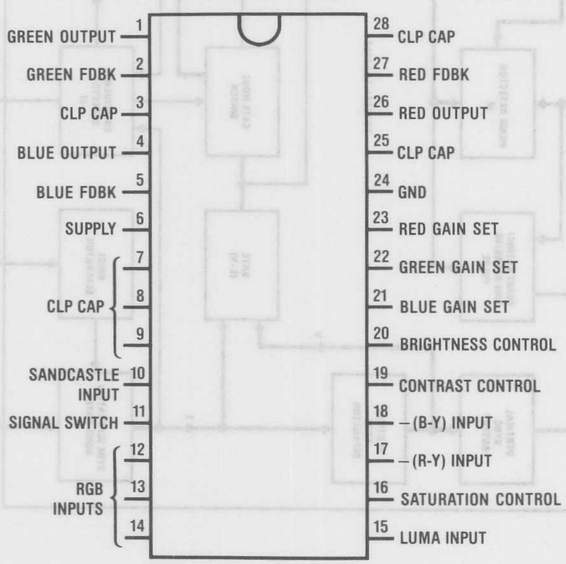
The output stages produce signals suitable for driving the bases of the video output transistors. The feedback inputs are suitable for collector feedback from these transistors. Most common video output stage types can be used.

Features

- AC coupled inputs for (R-Y), (B-Y) and Y signals
- Linear saturation control in the color difference stages
- G-Y and RGB matrix
- Linear inputs for direct RGB signals—use for teletext, inset picture, program status, tuning indicators, etc.
- Fast switching input to select between RGB inputs and normal TV signal. Can be used to inlay text into normal picture
- Linear contrast and brightness controls operating on both RGB inputs and matrixed luminance and color difference inputs
- Equally clamped black levels for RGB inputs and matrixed signals
- Three identical signal channels for R, G, B
- Horizontal and vertical blanking (black level or blacker than black) and black level clamping by means of a three-level sandcastle pulse
- Three electronic gain controls for adjustment of white drive levels
- Differential amplifiers with feedback inputs for feedback from the RGB output stages
- Gated feedback paths for stabilization of the DC levels at the picture tube

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number TDA3500N
See NS Package N28A

Absolute Maximum Ratings

	Min	Max
Supply Voltage, V_S (Pin 6)		13.2V
Operating Temperature Range, T_U	−20°C	+60°C
Storage Temperature Range, T_S	−65°C	+150°C
Power Dissipation, P_{TOT}		1.7W
Voltages		
V1, 4, 26	$V_S/2$	$V_S + 1V$
V2, 5, 27	0V	V_S
V3, 25, 28	Note 1	
V7, 8, 9	Note 1	

	Min	Max
V10	0V	V_S
V11	−0.5V	3V
V12, 13, 14	Note 1	
V16, 19, 20	0V	$V_S/2$
V15, 17, 18	Note 1	
V21, 22, 23	0V	V_S
Current		
I_{20}		5 mA

Electrical Characteristics $V_S = 12V$ (Note 2), $T_A = 25°C$

	Parameter	Conditions	Min	Typ	Max	Units
I_S	Supply Current			110		mA
COLOR DIFFERENCE STAGES						
V18	−(B-Y) Signal Input for 75% Saturated Color Bars			1.33		Vp-p
R18	Input Impedance		100			kΩ
V18	Internal DC Clamp Voltage			4.2		V
V17	−(R-Y) Signal Input for 75% Saturated Color Bars			1.05		Vp-p
R17	Input Impedance		100			kΩ
V17	Internal DC Clamp Voltage			4.2		V
SATURATION CONTROL (Pin 16)						
V16	Nominal Saturation	0 dB		3.0		V
		6 dB		4.0		V
		−20 dB		2.1		V
		> −40 dB		1.8		V
I_{16}	Input Current				20	μA
LUMINANCE SIGNAL INPUT (Pin 15)						
V15				0.45		Vp-p
R15	Input Impedance			12		kΩ
V15	Internal Bias Voltage			2.7		V
RGB CHANNELS						
	Signal Switching (Pin 11)					
V11	Matrixed Y, (B-Y), (R-Y) Signals Selected		−0.5		0.3	V
V11	RGB Signal Inputs Selected		0.9		1.5	V
I_{11}	Input Current		−100		200	μA
V12, 13, 14	RGB Input Signal Level (Note 3)	Pin 12 = B, Pin 13 = G, Pin 14 = R			1	Vp-p
V12, 13, 14	Internal DC Clamp Voltage			3.5		V
$I_{12, 13, 14}$	Input Current				5	μA
CONTRAST CONTROL (Pin 19)						
V19	Nominal Contrast	0 dB		3.4		V
		3 dB		4.0		V
		−6 dB		2.7		V
		−17 dB		2.0		V
I_{19}	Input Current				10	μA
BRIGHTNESS CONTROL (Pin 20)						
V20	Input Voltage Range		1		3	V
I_{20}	Input Current				10	μA
V20	Input Voltage for Nominal Black Level	Black Level Equal to Output Stage Clamp Level		2		V
	Range of Black Level Adjustment Referred to Nominal Video Signal	V20 1V–3V		±50		1%

Electrical Characteristics (Continued) $V_S = 12V$ (Note 2), $T_A = 25°C$

	Parameter	Conditions	Min	Typ	Max	Units
INTERNAL SIGNAL HANDLING						
	Referred to Nominal Video Signal and Black Level	Towards White Towards Black		125 −25		% %
WHITE DRIVE ADJUSTMENT (Pin 21 = B, Pin 22 = G, Pin 23 = R)						
	Nominal Gain	V21, 22, 23 = 6V (Note 4)		100		%
	Gain Reduction	V21, 22, 23 = 0V		40		%
	Gain Increase	V21, 22, 23 = 12V		40		%
R21, 22, 23	Input Impedance		20			kΩ
OUTPUT STAGES						
	Feedback Inputs	Pin 2(G), Pin 5(B), Pin 23(R)				
V2, 5, 27	Voltage During Clamping		5.79		5.95	V
ΔV2, 5, 27	Voltage Difference Between the Feedback Inputs				80	mV
R2, 5, 27	Input Resistance		100			kΩ
	Amplifier Outputs	Pin 1(G), Pin 4(B), Pin 26(R) Conductance of Error Amplifier $\frac{\Delta I_1}{\Delta V2} = \frac{\Delta I_4}{\Delta V5} = \frac{\Delta I_{26}}{\Delta V27}$		20		mA/V
R1, 4, 26	Integrated Load Resistance			610		Ω
$I_{1, 4, 26}$	Peak Output Current		−5		5	mA
V2, 5, 27/V15	Gain Between Luminance Input and the Feedback Inputs	Nominal Contrast, Saturation and Drive Settings		10		dB
ΔV2, 5, 27/V15	Frequency Response	0 MHz–5 MHz			3	dB
$\frac{V5}{V18} = \frac{V27}{V17}$	Gain Between Color Difference Inputs and the Feedback Inputs	Nominal Contrast, Saturation and Drive Settings		0		dB
$\frac{\Delta V5}{V18} = \frac{\Delta V27}{V17}$	Frequency Response	0 MHz–2 MHz			3	dB
$\frac{V2}{V13} = \frac{V5}{V12} = \frac{V27}{V14}$	Gain Between the RGB Inputs and the Feedback Inputs	Nominal Contrast and Drive Settings		0		dB
$\frac{\Delta V2}{V13} = \frac{\Delta V5}{V12} = \frac{\Delta V27}{V14}$	Frequency Response	0 MHz–5 MHz			3	dB
SANDCASTLE DETECTOR (Pin 10)						
	Three Internal Switching Levels for the Separation of the Sandcastle Pulse Information	Proportional to V_S				
V10	H and V Pulse (Note 5)		2		3	V
	H Pulse (Note 6)		4		5	V
	Clamp Pulse (Note 7)		7.5			V
	Low Level				1	V
$-I_{10}$	Input Current				100	µA

Note 1: No externally applied voltages.

Note 2: Supply voltage range (pin 6), $V_S = 10.8V - 13.2V$.

Note 3: During the clamp pulse period, the RGB inputs should be at black level as they are clamped to be equal to the matrixed luminance and color difference signal black levels. The output impedance of the drive to the RGB inputs should be less than 200Ω for correct clamp operation.

Note 4: With no external connection, pins 21, 22, 23 are internally biased to 6V.

Note 5: Blanking level = −20%.

Note 6: Blanking level = 0% = clamp level.

Note 7: Minimum pulse width = 3.5 µs. The clamps are permanently activated if pin 10 is open.

Pin Function Description

Pin	Function
1	Green output signal.
2	Green signal feedback. The signal gain of both the video output stages and IC amplifier are stabilized by the feedback circuits. DC clamping is achieved by sampling the feedback level during blanking. The black level potentials at the collectors of the video output stages may be varied independently by adjustable DC current sources applied to the feedback input pins. The DC levels at these pins are such that the feedback resistor and a resistor network between the 12V supply and earth provide a potential of 6V during blanking.
3	Clamp capacitor for blue output stage.
4	Blue output signal.
5	Blue signal feedback (see pin 2).
6	Positive 12V supply.
7	Blue black level clamp capacitor.
8	Green black level clamp capacitor.
9	Red black level clamp capacitor.
10	Sandcastle pulse input. A sandcastle pulse derived, for example, from a TDA2593 line oscillator should be applied to this pin. A voltage between 4V and 5V will operate the line blanking to nominal clamp level. For frame blanking 20% below clamp level, a voltage between 2V and 3V may be applied. A pulse greater than 7.5V is required to operate the clamp circuits.
11	Signal switching input. A voltage less than 0.3V will enable the matrixed Y, (B-Y), (R-Y) signals. An input greater than 0.9V will select the RGB input signals. If no connection is made, the matrixed signals are selected.
12	Blue input. The positive-going input signal is required to be AC coupled from a low impedance source. The coupling capacitor also acts as a clamp capacitor. The high input impedance enables low value coupling capacitors to be used.
13	Green input (see pin 12).
14	Red input (see pin 12).
15	Luminance signal input. A positive-going input signal is required. This pin is internally biased to 2.7V with an input impedance of 12 kΩ.
16	Saturation control input.
17	−(R-Y) signal input. The negative, −(R-Y), input should be AC coupled from a low impedance source. The coupling capacitor also acts as a clamp capacitor. The high input impedance enables low value coupling capacitors to be used.
18	B-Y signal input (see pin 17).
19	Contrast control input.
20	Brightness control input.
21	Blue drive adjustment. A gain variation of typ ±40% about the nominal is obtained as the voltage of this pin is varied ±6V about the nominal value of 6V. If no connection is made, nominal gain is obtained.
22	Green drive adjustment (see pin 21).
23	Red drive adjustment (see pin 21).
24	Negative supply, 0V (earth).
25	Clamp capacitor for red output stage.
26	Red output signal.
27	Red signal feedback (see pin 2).
28	Clamp capacitor for green output stage.

Application Hints

To use the TDA3500 as a VDU driver with RGB input only, the Y input (pin 15) may be left open. The B-Y and R-Y input capacitors, pins 17 and 18, should be connected to ground to act as clamp capacitors.

If operation without RGB inputs is required, pins 12, 13 and 14 may be left unconnected. Pin 11 may be unconnected or grounded.

The input coupling capacitor to pin 15 is not used as a clamp capacitor and may be omitted if AC coupling has been carried out in an earlier stage, or if the signal amplitude is so well defined as to remain within the window of the IC when DC coupled. A nominal bias of 2.7V at black level should be provided.

The nominal control ranges for brightness, contrast and saturation given in the data may be changed with suitable potential dividers. The application circuit shows control ranges arranged for 0V–12V operation.

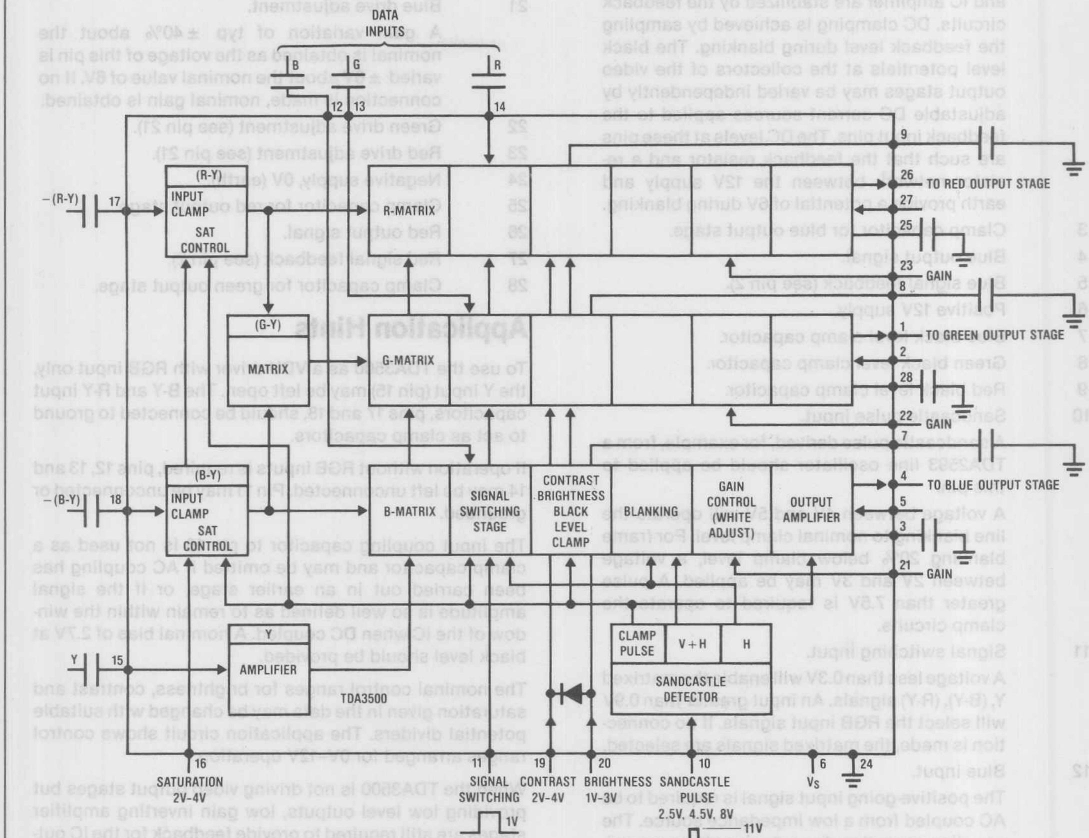
When the TDA3500 is not driving video output stages but providing low level outputs, low gain inverting amplifier stages are still required to provide feedback for the IC output stages.

Class AB video output stages are shown in the application circuit. Though using more components than class A types, they offer reduced power dissipation and better transient response. For good frequency response and stability, care is required with the stray capacitances on the printed circuit board. In a compact board layout this applies particularly to the capacitance between the video output and the feedback pins. The feedback resistor should be a low capacitance type.

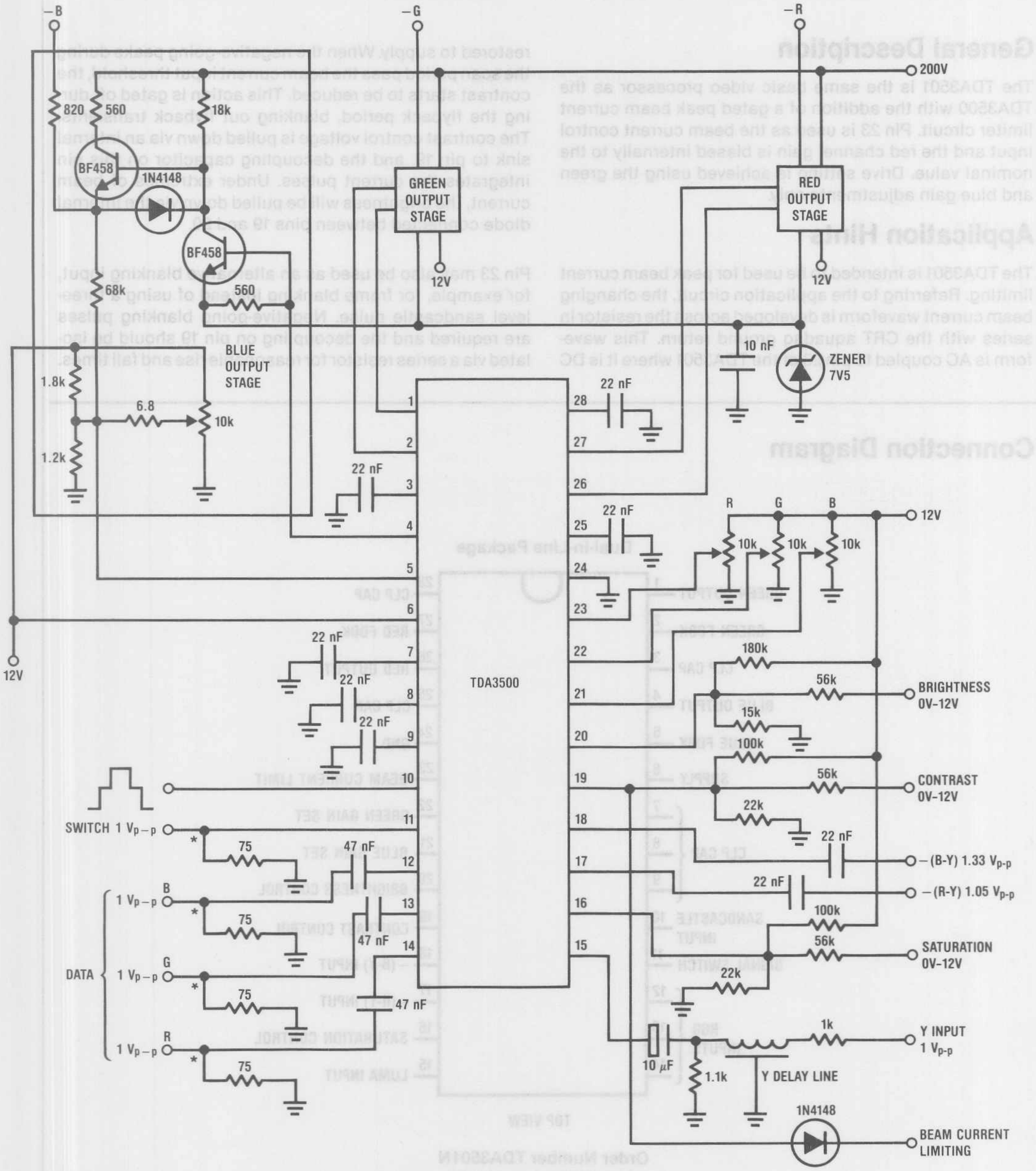
Note 1: Attention should be given to earth paths, avoiding common impedances between the input (decoder) side and the output stages.

Note 2: Printed track area connected to the feedback pins should be kept to a minimum.

Note 3: To ensure a matched performance of the video output stages, a symmetrical layout of three stages should be employed.


DATA INPUTS
B
G
R
12
13
14
(R-Y)
INPUT CLAMP
SAT CONTROL
R-MATRIX
−(R-Y)
17
(G-Y)
MATRIX
G-MATRIX
(B-Y)
INPUT CLAMP
SAT CONTROL
−(B-Y)
18
B-MATRIX
SIGNAL SWITCHING STAGE
CONTRAST BRIGHTNESS BLACK LEVEL CLAMP
BLANKING
GAIN CONTROL (WHITE ADJUST)
OUTPUT AMPLIFIER
Y
15
Y AMPLIFIER
TDA3500
CLAMP PULSE
V+H
H
SANDCASTLE DETECTOR
9
26
TO RED OUTPUT STAGE
27
25
23
GAIN
8
1
TO GREEN OUTPUT STAGE
2
28
22
GAIN
7
4
TO BLUE OUTPUT STAGE
5
3
21
GAIN
16
SATURATION 2V-4V
11
SIGNAL SWITCHING
1V
19
CONTRAST 2V-4V
20
BRIGHTNESS 1V-3V
10
SANDCASTLE PULSE 2.5V, 4.5V, 8V
11V
4.5V
0V
6
V_S
24

Typical Application and Test Circuit



* Input termination 200Ω max

11

National Semiconductor

TDA3501 Chroma Processor + RGB Drive Combination

General Description

The TDA3501 is the same basic video processor as the TDA3500 with the addition of a gated peak beam current limiter circuit. Pin 23 is used as the beam current control input and the red channel gain is biased internally to the nominal value. Drive setting is achieved using the green and blue gain adjustments only.

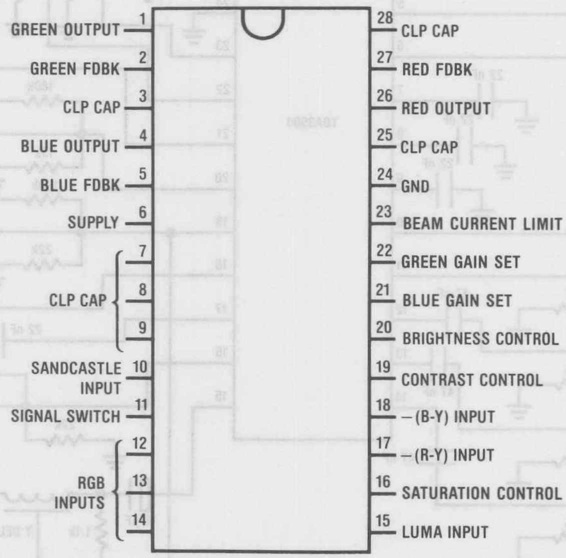
Application Hints

The TDA3501 is intended to be used for peak beam current limiting. Referring to the application circuit, the changing beam current waveform is developed across the resistor in series with the CRT aquadag ground return. This waveform is AC coupled to pin 23 of the TDA3501 where it is DC restored to supply. When the negative-going peaks during the scan period pass the beam current input threshold, the contrast starts to be reduced. This action is gated off during the flyback period, blanking out flyback transients. The contrast control voltage is pulled down via an internal sink to pin 19, and the decoupling capacitor on this pin integrates the current pulses. Under extremes of beam current, the brightness will be pulled down via the internal diode connected between pins 19 and 20.

Pin 23 may also be used as an alternative blanking input, for example, for frame blanking instead of using a three-level sandcastle pulse. Negative-going blanking pulses are required and the decoupling on pin 19 should be isolated via a series resistor for reasonable rise and fall times.

Connection Diagram

Dual-In-Line Package



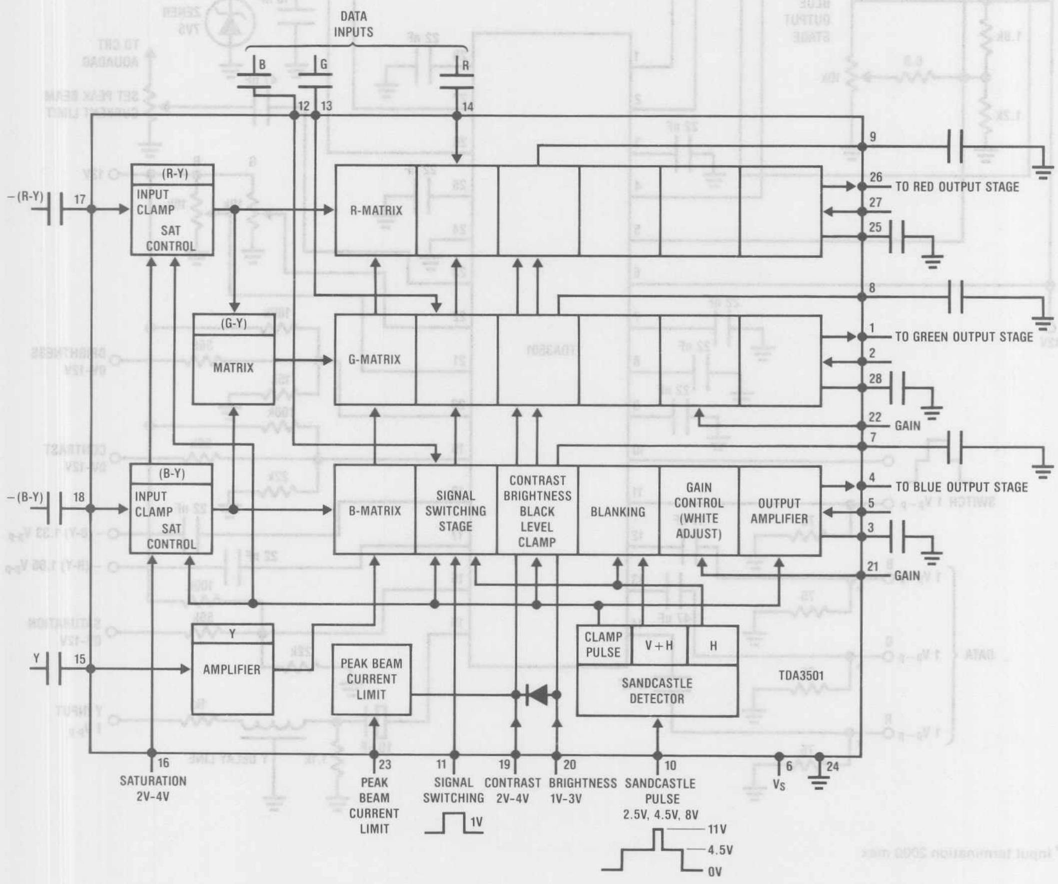
TOP VIEW

Order Number TDA3501N
See NS Package N28A

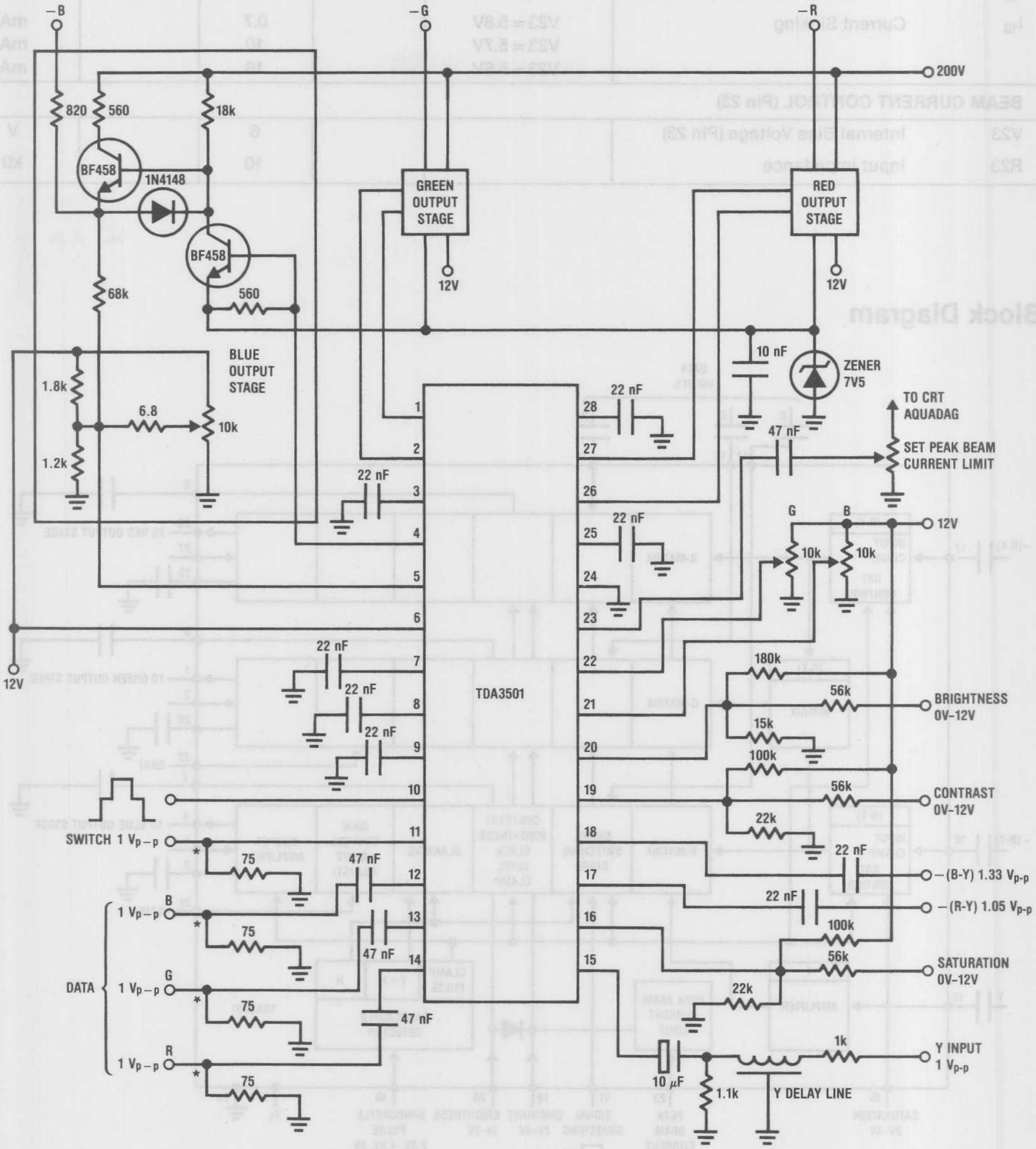
Electrical Characteristics $V_S = 12V$, $T_A = 25°C$. The TDA3500 data applies except for the following parameters.

	Parameter	Conditions	Min	Typ	Max	Units
CONTRAST CONTROL (Pin 19)						
I_{19}	Contrast Control Input Current	$V23 \geq 6V$			10	μA
I_{19}	Current Sinking	$V23 = 5.8V$		0.7		mA
		$V23 = 5.7V$		10		mA
		$V23 = 5.6V$		16		mA
BEAM CURRENT CONTROL (Pin 23)						
V23	Internal Bias Voltage (Pin 23)			6		V
R23	Input Impedance			10		kΩ

Block Diagram



Typical Application and Test Circuit



* Input termination 200Ω max

Section 12

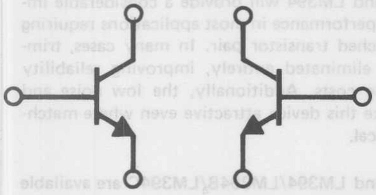
**Transistor/
Diode Arrays**

12

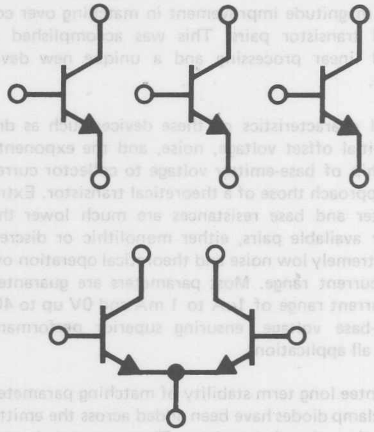
Section Contents

Transistor/Diode Arrays

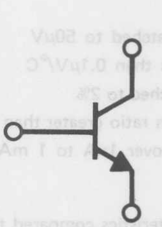
Selection Guide



LM194/LM394



LM3045
LM3046
LM3086
LM3146



LM195/LM295/LM395
(Current Limit, Thermal Limit, Safe Area Protection)

National Semiconductor

Transistor/Diode Arrays

LM194/LM394 Supermatch Pair

General Description

The LM194 and LM394 are junction isolated ultra well-matched monolithic NPN transistor pairs with an order of magnitude improvement in matching over conventional transistor pairs. This was accomplished by advanced linear processing and a unique new device structure.

Electrical characteristics of these devices such as drift versus initial offset voltage, noise, and the exponential relationship of base-emitter voltage to collector current closely approach those of a theoretical transistor. Extrinsic emitter and base resistances are much lower than presently available pairs, either monolithic or discrete, giving extremely low noise and theoretical operation over a wide current range. Most parameters are guaranteed over a current range of 1μA to 1 mA and 0V up to 40V collector-base voltage, ensuring superior performance in nearly all applications.

To guarantee long term stability of matching parameters, internal clamp diodes have been added across the emitter-base junction of each transistor. These prevent degradation due to reverse biased emitter current—the most common cause of field failures in matched devices. The parasitic isolation junction formed by the diodes also clamps the substrate region to the most negative emitter to ensure complete isolation between devices.

The LM194 and LM394 will provide a considerable improvement in performance in most applications requiring a closely matched transistor pair. In many cases, trimming can be eliminated entirely, improving reliability and decreasing costs. Additionally, the low noise and high gain make this device attractive even where matching is not critical.

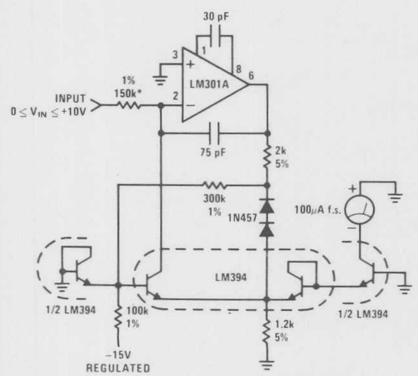
The LM194 and LM394/LM394B/LM394C are available in an isolated header 6-lead TO-5 metal can package. The LM194 is identical to the LM394 except for tighter electrical specifications and wider temperature range.

Features

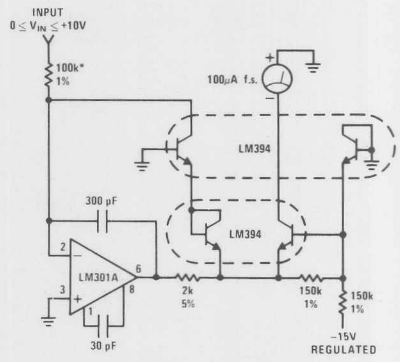
- Emitter-base voltage matched to 50μV
- Offset voltage drift less than 0.1μV/°C
- Current gain (h_{FE}) matched to 2%
- Common-mode rejection ratio greater than 120 dB
- Parameters guaranteed over 1μA to 1 mA collector current
- Extremely low noise
- Superior logging characteristics compared to conventional pairs
- Plug-in replacement for presently available devices

Typical Applications

Low Cost Accurate Square Root Circuit
$I_{OUT} = 10^{-5} \cdot \sqrt{10\ V_{IN}}$



Low Cost Accurate Squaring Circuit
$I_{OUT} = 10^{-6}\ (V_{IN})^2$



*Trim for full scale accuracy

Absolute Maximum Ratings

Collector Current	20 mA
Collector-Emitter Voltage	V_{MAX}
Collector-Emitter Voltage	40V
LM394C	20V
Collector-Base Voltage	40V
LM394C	20V
Collector-Substrate Voltage	40V
LM394C	20V
Collector-Collector Voltage	40V
LM394C	20V
Base-Emitter Current	±10 mA
Power Dissipation	500 mW
Junction Temperature	
LM194	−55°C to +125°C
LM394/LM394B/LM394C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (T_J = 25°C)

PARAMETER	CONDITIONS	LM194			LM394			LM394B/LM394C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Current Gain (h_{FE})	V_{CB} = 0V to V_{MAX} (Note 1)										
	I_C = 1 mA	500	700		300	700		225	500		
	I_C = 100μA	400	550		250	550		200	400		
	I_C = 10μA	300	450		200	450		150	300		
	I_C = 1μA	200	300		150	300		100	200		
Current Gain Match (h_{FE} Match) $= \frac{100\,[\Delta I_B]\,[h_{FE(MIN)}]}{I_C}$	V_{CB} = 0V to V_{MAX}										
	I_C = 10μA to 1 mA		0.5	2		0.5	4		1.0	5	%
	I_C = 1μA		1.0			1.0			2.0		%
Emitter-Base Offset Voltage	V_{CB} = 0, I_C = 1μA to 1 mA		25	50		25	150		50	200	μV
Change in Emitter-Base Offset Voltage vs Collector-Base Voltage (CMRR)	(Note 1) I_C = 1μA to 1 mA, V_{CB} = 0V to V_{MAX}		10	25		10	50		10	100	μV
Change in Emitter-Base Offset Voltage vs Collector Current	V_{CB} = 0V, I_C = 1μA to 0.3 mA		5	25		5	50		5	50	μV
Emitter-Base Offset Voltage Temperature Drift	I_C = 10μA to 1 mA (Note 2)										
	$I_{C1} = I_{C2}$		0.08	0.3		0.08	1.0		0.2	1.5	μV/°C
	V_{OS} Trimmed to 0 at 25°C		0.03	0.1		0.03	0.3		0.03	0.5	μV/°C
Logging Conformity	I_C = 3 nA to 300μA, V_{CB}=0, (Note 3)		150			150			150		μV
Collector-Base Leakage	$V_{CB} = V_{MAX}$		0.05	0.25		0.05	0.5		0.05	0.5	nA
Collector-Collector Leakage	$V_{CC} = V_{MAX}$		0.1	2.0		0.1	5.0		0.1	5.0	nA
Input Voltage Noise	I_C = 100μA, V_{CB} = 0V, f = 100 Hz to 100 kHz		1.8			1.8			1.8		$nV/\sqrt{Hz}$
Collector to Emitter Saturation Voltage	I_C = 1 mA, I_B = 10μA		0.2			0.2			0.2		V
	I_C = 1 mA, I_B = 100μA		0.1			0.1			0.1		V

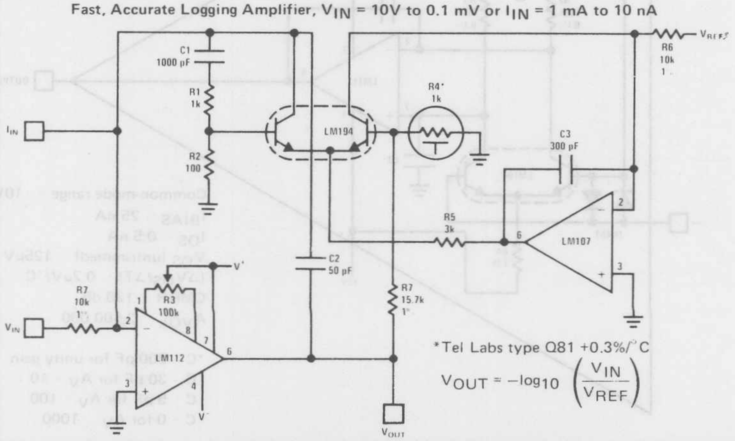
Note 1: Collector-base voltage is swept from 0 to V_{MAX} at a collector current of 1μA, 10μA, 100μA, and 1 mA.

Note 2: Offset voltage drift with V_{OS} = 0 at T_A = 25°C is valid only when the ratio of I_{C1} to I_{C2} is adjusted to give the initial zero offset. This ratio must be held to within 0.003% over the entire temperature range. Measurements taken at +25°C and temperature extremes.

Note 3: Logging conformity is measured by computing the best fit to a true exponential and expressing the error as a base-emitter voltage deviation.

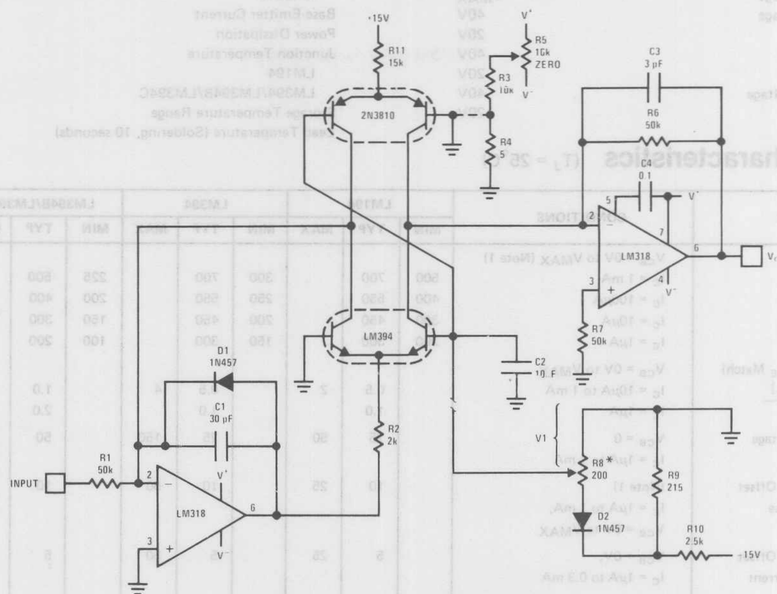
Typical Applications (Continued)

Fast, Accurate Logging Amplifier, V_{IN} = 10V to 0.1 mV or I_{IN} = 1 mA to 10 nA



Typical Applications (Continued)

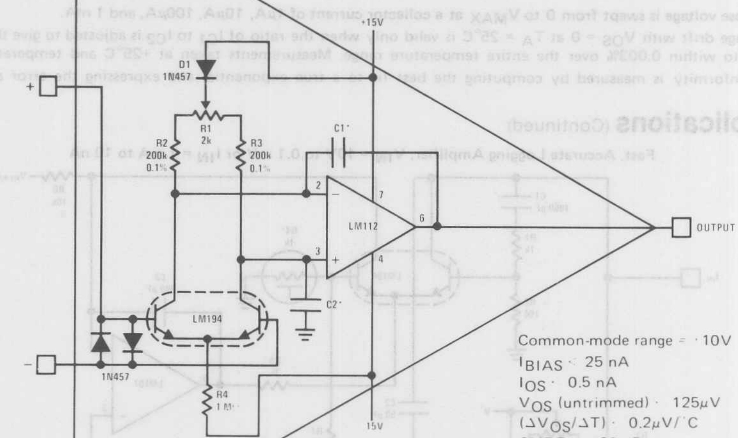
Voltage Controlled Variable Gain Amplifier



*R8–R10 and D2 povide a temperature independent gain control.
G = −336 V1 (dB)

Distortion < 0.1%
Bandwidth ≈ 1 MHz
100 dB gain range

Precision Low Drift Operational Amplifier

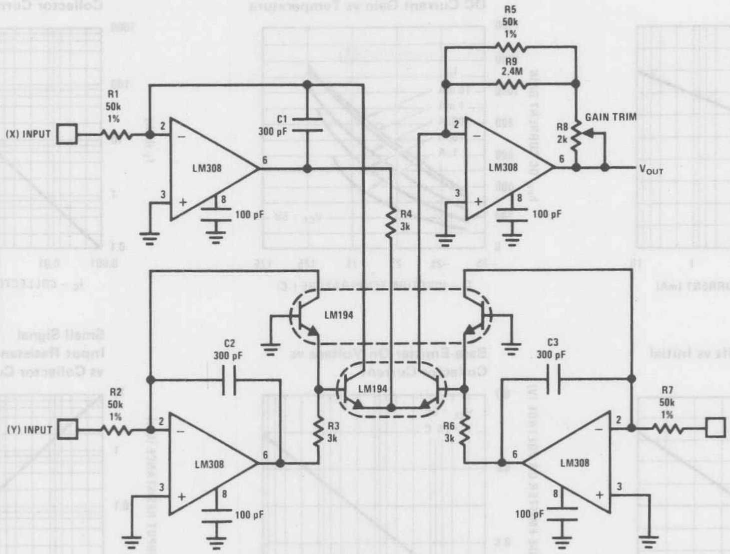


Common-mode range ≈ ±10V
I_{BIAS} ≤ 25 nA
I_{OS} ≤ 0.5 nA
V_{OS} (untrimmed) ≤ 125μV
$(\Delta V_{OS}/\Delta T)$ ≤ 0.2μV/°C
CMRR ≥ 120 dB
A_{VOL} ≥ 2,500,000

*C = 200 pF for unity gain
C = 30 pF for A_V = 10
C = 5 pF for A_V = 100
C = 0 for A_V ≥ 1000

Typical Applications (Continued)

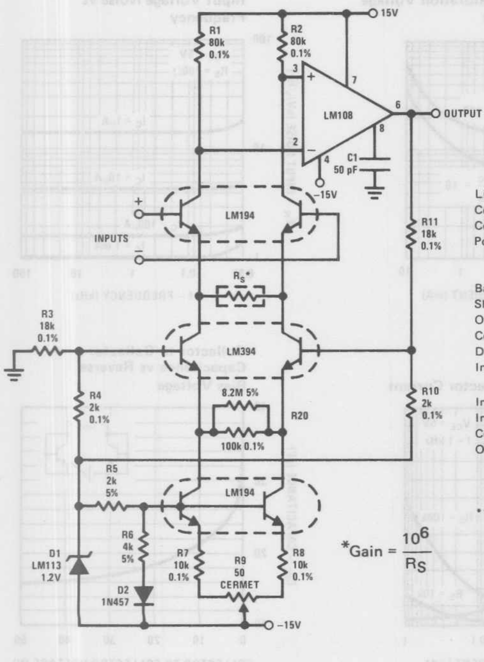
High Accuracy One Quadrant Multiplier/Divider



$$V_{OUT} = \frac{(X)\ (Y)}{(Z)}\ ;\ \text{positive inputs only.}$$

*Typical linearity 0.1%

High Performance Instrumentation Amplifier



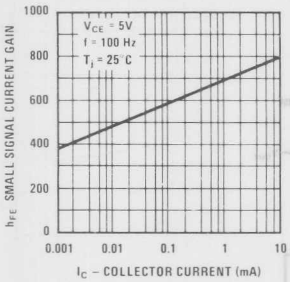
$$^{*}\text{Gain} = \frac{10^6}{R_S}$$

Performance Characteristics

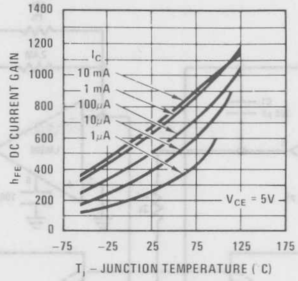
	G = 10,000	G = 1,000	G = 100	G = 10	
Linearity of Gain (±10V Output)	≤ 0.01	≤ 0.01	≤ 0.02	≤ 0.05	%
Common-Mode Rejection Ratio (60 Hz)	≥ 120	≥ 120	≥ 110	≥ 90	dB
Common-Mode Rejection Ratio (1 kHz)	≥ 110	≥ 110	≥ 90	≥ 70	dB
Power Supply Rejection Ratio					
+ Supply	> 110	>110	> 110	> 110	dB
− Supply	> 110	>110	> 90	> 70	dB
Bandwidth (−3 dB)	50	50	50	50	kHz
Slew Rate	0.3	0.3	0.3	0.3	V/μs
Offset Voltage Drift**	≤ 0.25	≤ 0.4	≤ 2	≤ 10	μV/°C
Common-Mode Input Resistance	$> 10^9$	$> 10^9$	$> 10^9$	$> 10^9$	Ω
Differential Input Resistance	$> 3 \times 10^8$	$> 3 \times 10^8$	$> 3 \times 10^8$	$> 3 \times 10^8$	Ω
Input Referred Noise (100 Hz ≤ f ≤ 10 kHz)	5	6	12	70	$\frac{nV}{\sqrt{Hz}}$
Input Bias Current	75	75	75	75	nA
Input Offset Current	1.5	1.5	1.5	1.5	nA
Common-Mode Range	± 11	±11	±11	±10	V
Output Swing (R_L = 10 kΩ)	±13	±13	±13	±13	V

**Assumes ≤ 5 ppm/°C tracking of resistors

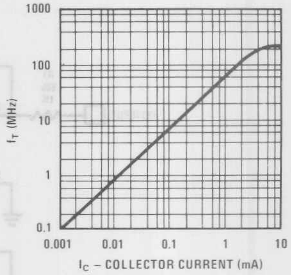
Small Signal Current Gain vs Collector Current



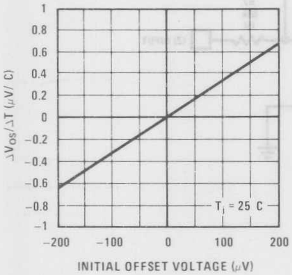
DC Current Gain vs Temperature



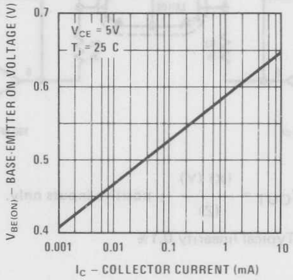
Unity Gain Frequency (f_t) vs Collector Current



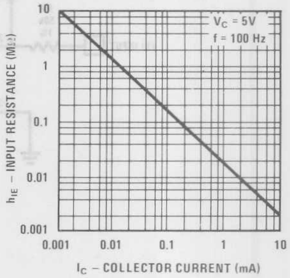
Offset Voltage Drift vs Initial Offset Voltage



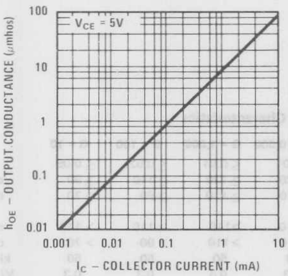
Base-Emitter On Voltage vs Collector Current



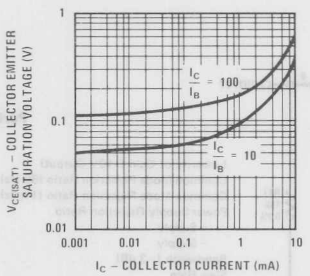
Small Signal Input Resistance (h_{ie}) vs Collector Current



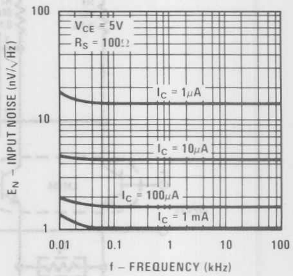
Small Signal Output Conductance vs Collector Current



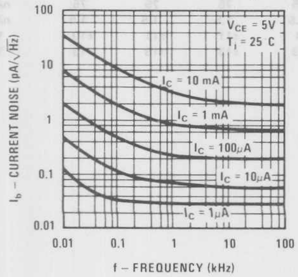
Collector-Emitter Saturation Voltage vs Collector Current



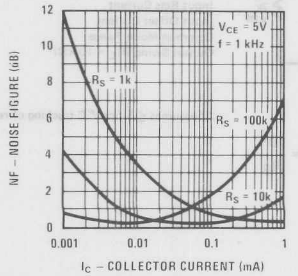
Input Voltage Noise vs Frequency



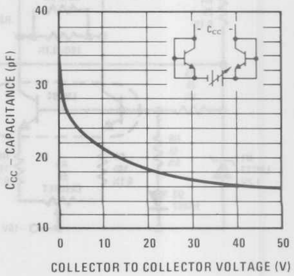
Base Current Noise vs Frequency



Noise Figure vs Collector Current

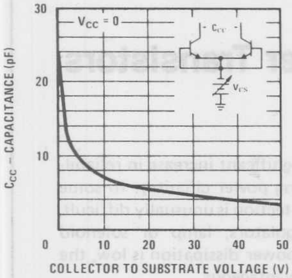


Collector to Collector Capacitance vs Reverse Bias Voltage

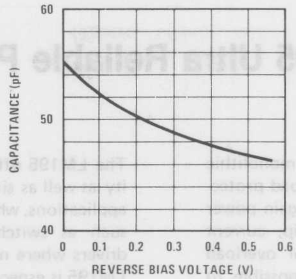


Typical Performance Characteristics (Continued)

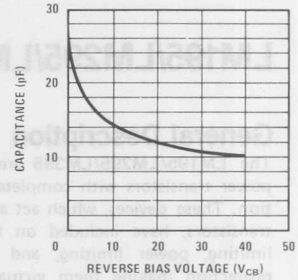
Collector to Collector Capacitance vs Collector-Substrate Voltage



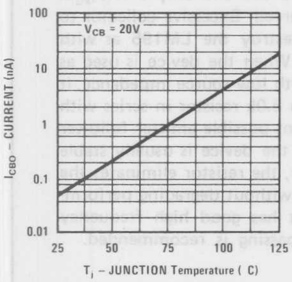
Emitter-Base Capacitance vs Reverse Bias Voltage



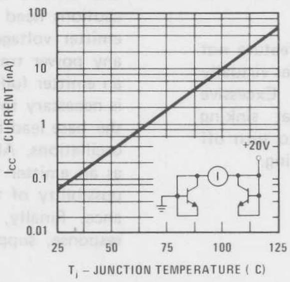
Collector-Base Capacitance vs Reverse Bias Voltage



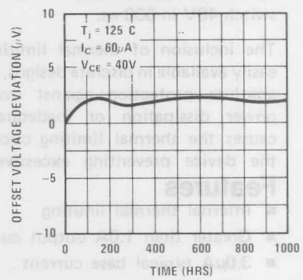
Collector-Base Leakage vs Temperature



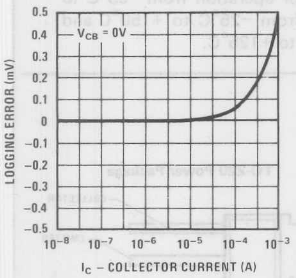
Collector to Collector Leakage vs Temperature



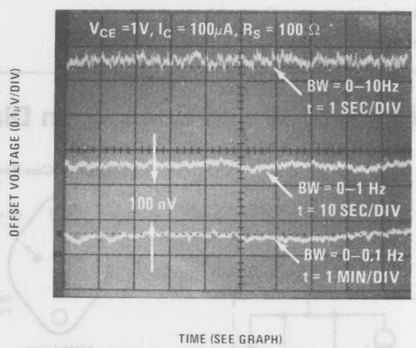
Offset Voltage Long Term Stability at High Temperature



Emitter-Base Log Conformity



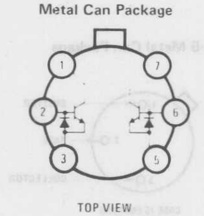
Low Frequency Noise of Differential Pair*



*Unit must be in still air environment so that differential lead temperature is held to less than 0.0003°C.

Connection Diagram

Metal Can Package



Order Number LM194H, LM394H LM394BH or LM394CH See NS Package H06C

National Semiconductor

Transistor/Diode Arrays

LM195/LM295/LM395 Ultra Reliable Power Transistors

General Description

The LM195/LM295/LM395 are fast, monolithic power transistors with complete overload protection. These devices, which act as high gain power transistors, have included on the chip, current limiting, power limiting, and thermal overload protection making them virtually impossible to destroy from any type of overload. In the standard TO-3 transistor power package, the LM195 will deliver load currents in excess of 1.0A and can switch 40V in 500 ns.

The inclusion of thermal limiting, a feature not easily available in discrete designs, provides virtually absolute protection against overload. Excessive power dissipation or inadequate heat sinking causes the thermal limiting circuitry to turn off the device preventing excessive heating.

The LM195 offers a significant increase in reliability as well as simplifying power circuitry. In some applications, where protection is unusually difficult, such as switching regulators, lamp or solenoid drivers where normal power dissipation is low, the LM195 is especially advantageous.

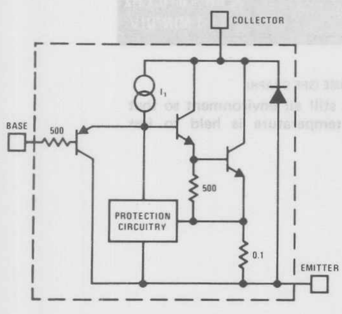
The LM195 is easy to use and only a few precautions need be observed. Excessive collector to emitter voltage can destroy the LM195 as with any power transistor. When the device is used as an emitter follower with low source impedance, it is necessary to insert a 5.0k resistor in series with the base lead to prevent possible emitter follower oscillations. Although the device is usually stable as an emitter follower, the resistor eliminates the possibility of trouble without degrading performance. Finally, since it has good high frequency response, supply by passing is recommended.

The LM195/LM295/LM395 are available in standard TO-3 power packages and solid Kovar TO-5. The LM195 is rated for operation from −55°C to +150°C, the LM295 from −25°C to +150°C and the LM395 from 0°C to +125°C.

Features

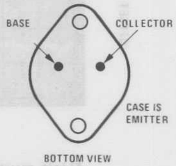
- Internal thermal limiting
- Greater than 1.0A output current
- 3.0μA typical base current
- 500 ns switching time
- 2.0V saturation
- Base can be driven up to 40V without damage
- Directly interfaces with CMOS or TTL
- 100% electrical burn-in

Simplified Circuit and Connection Diagrams



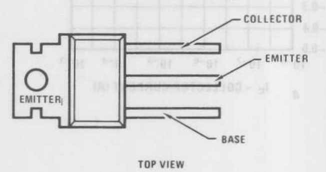
Simplified Circuit of the LM195

TO-3 Metal Can Package



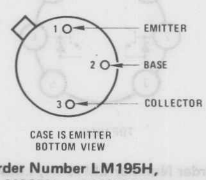
Order Number LM195K, LM295K or LM395K
See NS Package K02A

TO-220 Power Package



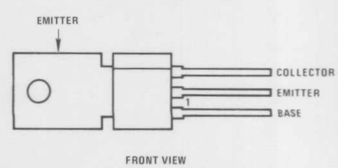
Order Number LM395T
See NS Package T03B

TO-5 Metal Can Package



Order Number LM195H, LM295H or LM395H
See NS Package H03B

TO-202 Power Package



Order Number LM395P
See NS Package P03A

Absolute Maximum Ratings

Collector to Emitter Voltage	
LM195, LM295	42V
LM395	36V
Collector to Base Voltage	
LM195, LM295	42V
LM395	36V
Base to Emitter Voltage (Forward)	
LM195, LM295	42V
LM395	36V
Base to Emitter Voltage (Reverse)	20V
Collector Current	Internally Limited
Power Dissipation	Internally Limited
Operating Temperature Range	
LM195	$-55^\circ C$ to $+150^\circ C$
LM295	$-25^\circ C$ to $+150^\circ C$
LM395	$0^\circ C$ to $+125^\circ C$
Storage Temperature Range	$-65^\circ C$ to $+150^\circ C$
Lead Temperature (Soldering, 10 seconds)	$300^\circ C$

Preconditioning

100% Burn-In In Thermal Limit

Electrical Characteristics (Note 1)

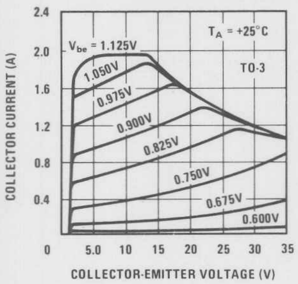
PARAMETER	CONDITIONS	LM195, LM295			LM395			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Collector-Emitter Operating Voltage (Note 3)	$I_Q \le I_C \le I_{MAX}$			42			36	V
Base to Emitter Breakdown Voltage	$0 \le V_{CE} \le V_{CEMAX}$	42			36	60		V
Collector Current								
TO-3, TO-220	$V_{CE} \le 15V$	1.2	2.2		1.0	2.2		A
TO-5, TO-202	$V_{CE} \le 7.0V$	1.2	1.8		1.0	1.8		A
Saturation Voltage	$I_C \le 1.0A$, $T_A = 25^\circ C$		1.8	2.0		1.8	2.2	V
Base Current	$0 \le I_C \le I_{MAX}$ $0 \le V_{CE} \le V_{CEMAX}$		3.0	5.0		3.0	10	μA
Quiescent Current (I_Q)	$V_{be} = 0$ $0 \le V_{CE} \le V_{CEMAX}$		2.0	5.0		2.0	10	mA
Base to Emitter Voltage	$I_C = 1.0A$, $T_A = +25^\circ C$		0.9			0.9		V
Switching Time	$V_{CE} = 36V$, $R_L = 36\Omega$, $T_A = +25^\circ C$		500			500		ns
Thermal Resistance Junction to Case (Note 2)	TO-3 Package TO-5 Package		2.3 12	3.0 15		2.3 12	3.0 15	°C/W °C/W

Note 1: Unless otherwise specified, these specifications apply for $-55^\circ C \le T_j \le +150^\circ C$ for the LM195, $-25^\circ C \le T_j \le +150^\circ C$ for the LM295 and $0^\circ C \le +125^\circ C$ for the LM395.

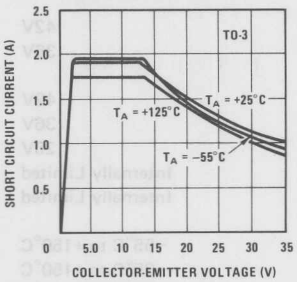
Note 2: Without a heat sink, the thermal resistance of the TO-5 package is about $+150^\circ C/W$, while that of the TO-3 package is $+35^\circ C/W$.

Note 3: Selected devices with higher breakdown available.

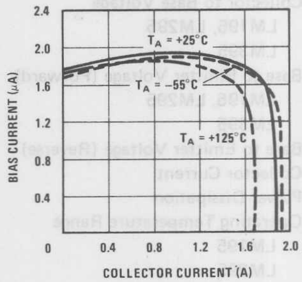
Collector Characteristics



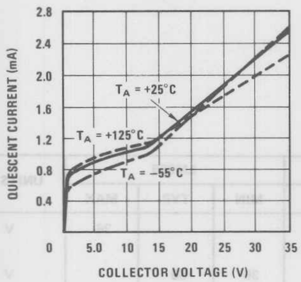
Short Circuit Current



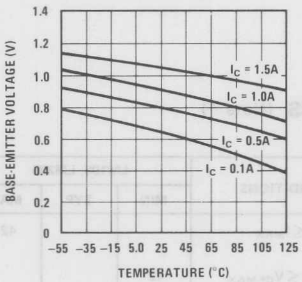
Bias Current



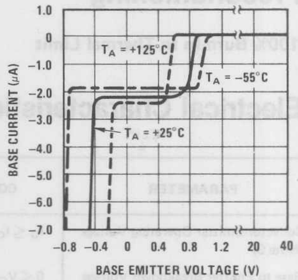
Quiescent Current



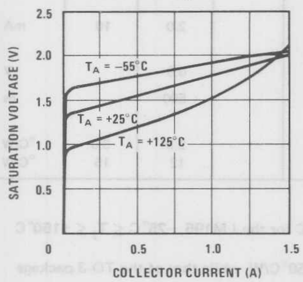
Base Emitter Voltage



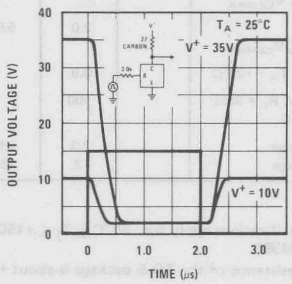
Base Current



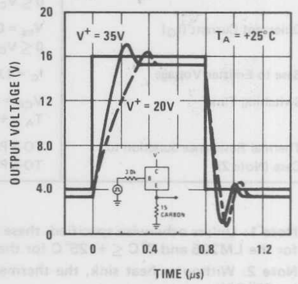
Saturation Voltage



Response Time

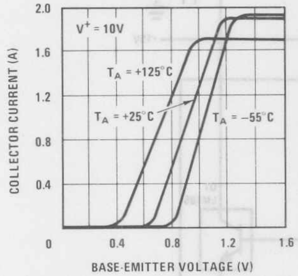


Response Time

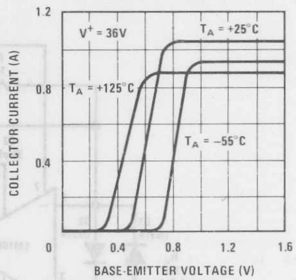


Typical Performance Characteristics (Continued)

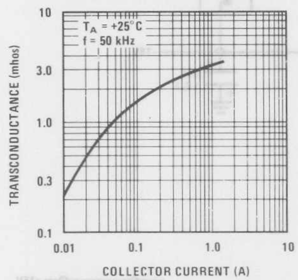
10V Transfer Function



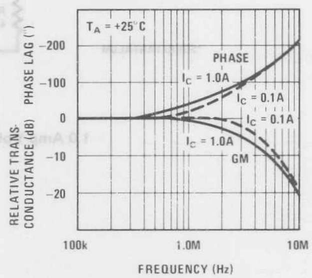
36V Transfer Function



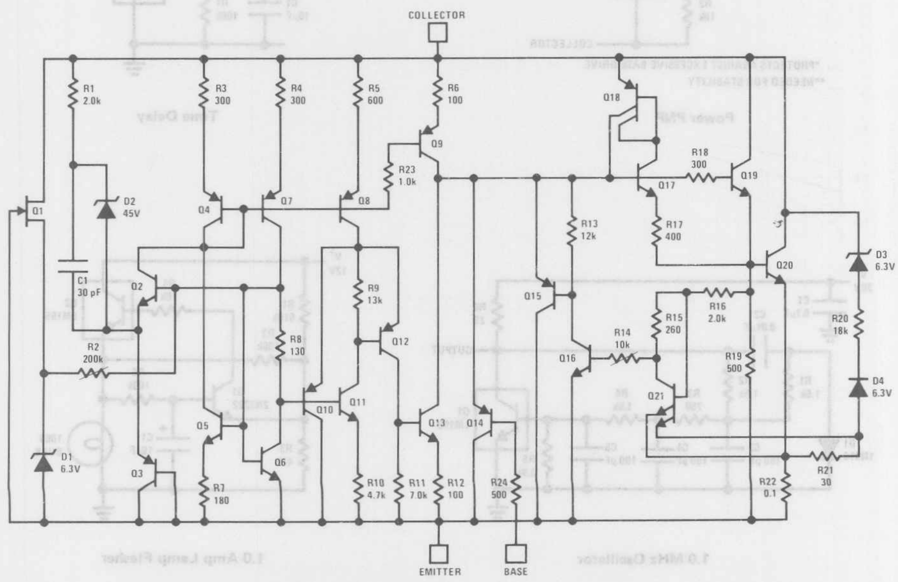
Transconductance



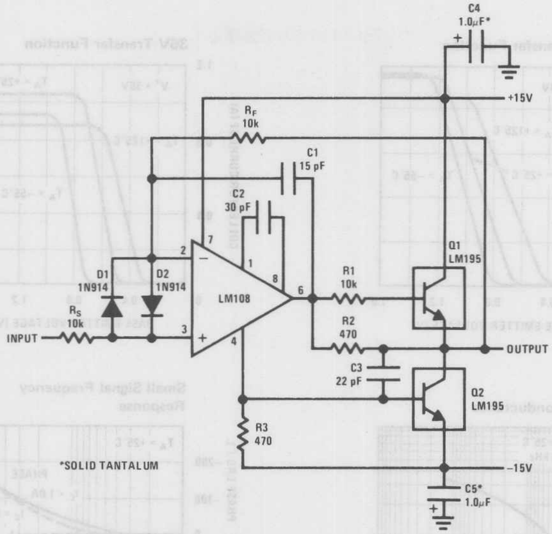
Small Signal Frequency Response



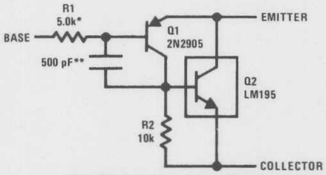
Schematic Diagram



Typical Applications

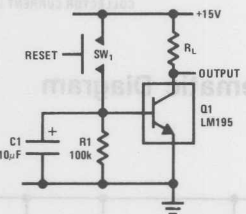


1.0 Amp Voltage Follower

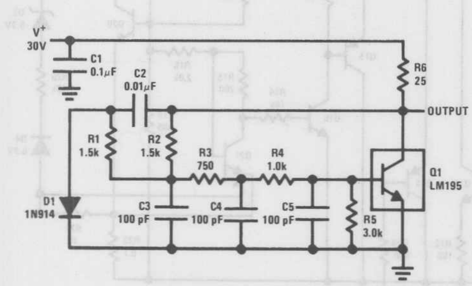


*PROTECTS AGAINST EXCESSIVE BASE DRIVE
**NEEDED FOR STABILITY

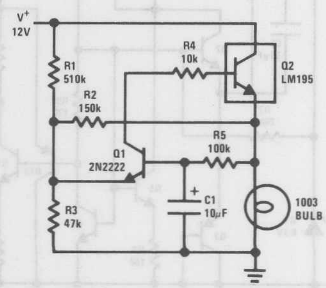
Power PNP



Time Delay

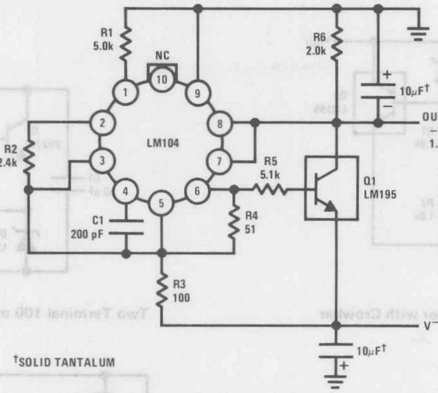


1.0 MHz Oscillator



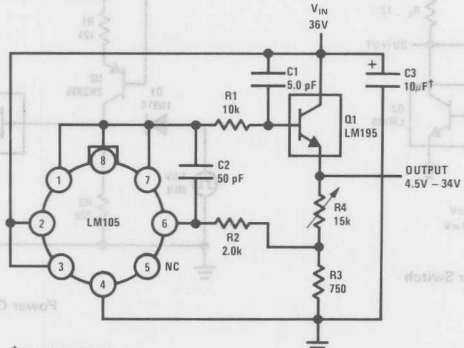
1.0 Amp Lamp Flasher

Typical Applications (Continued)



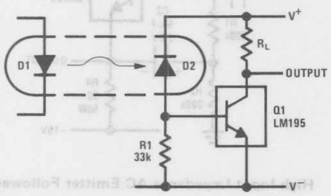
†SOLID TANTALUM

1.0 Amp Negative Regulator

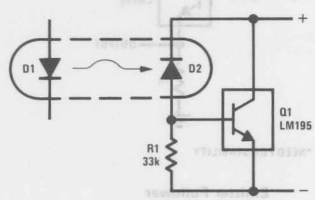


†SOLID TANTALUM

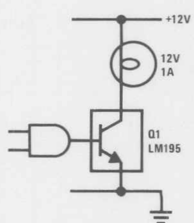
1.0 Amp Positive Voltage Regulator



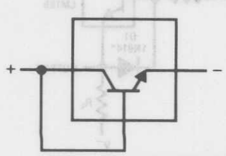
Fast Optically Isolated Switch



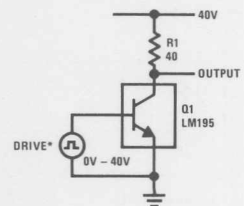
Optically Isolated Power Transistor



CMOS or TTL Lamp Interface

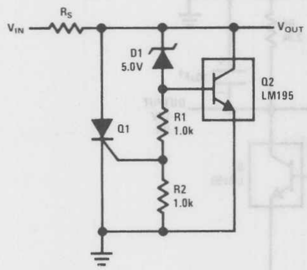


Two Terminal Current Limiter

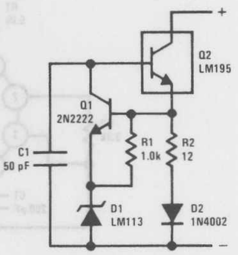


*DRIVE VOLTAGE 0V TO ≥ 1.0V ≤ 42V

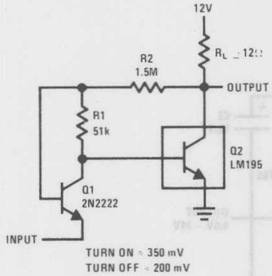
40V Switch



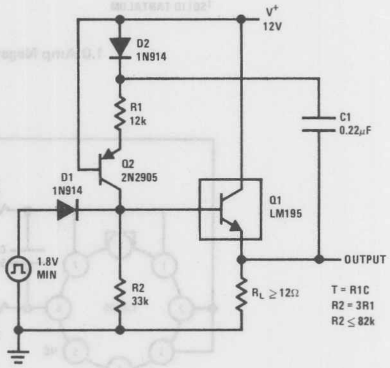
6.0V Shunt Regulator with Crowbar



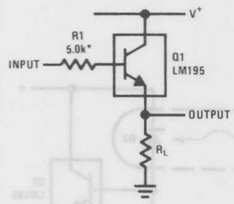
Two Terminal 100 mA Current Regulator



Low Level Power Switch

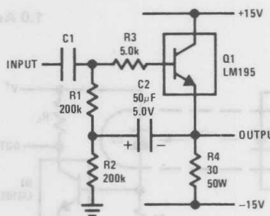


Power One-Shot

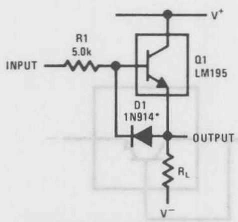


*NEED FOR STABILITY

Emitter Follower



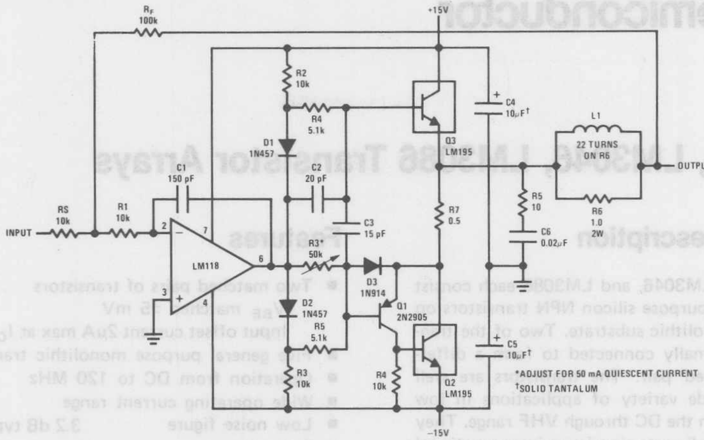
High Input Impedance AC Emitter Follower



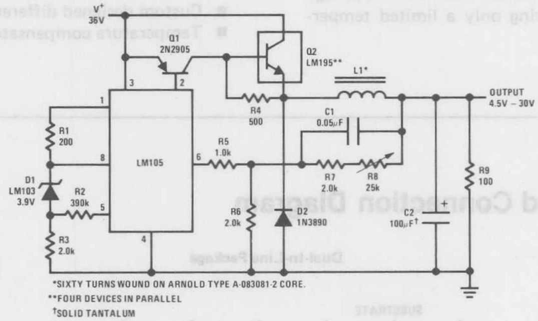
*PREVENTS STORAGE WITH FAST FALL TIME SQUARE WAVE DRIVE

Fast Follower

Typical Applications (Continued)



Power Op Amp



6.0 Amp Variable Output Switching Regulator

National Semiconductor

LM3045, LM3046, LM3086 Transistor Arrays

General Description

The LM3045, LM3046, and LM3086 each consist of five general purpose silicon NPN transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair. The transistors are well suited to a wide variety of applications in low power system in the DC through VHF range. They may be used as discrete transistors in conventional circuits however, in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching. The LM3045 is supplied in a 14-lead cavity dual-in-line package rated for operation over the full military temperature range. The LM3046 and LM3086 are electrically identical to the LM3045 but are supplied in a 14-lead molded dual-in-line package for applications requiring only a limited temperature range.

Features

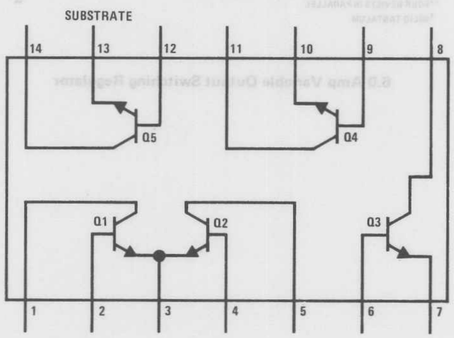
- Two matched pairs of transistors
  - V_{BE} matched ±5 mV
  - Input offset current $2\mu A$ max at $I_C = 1$ mA
- Five general purpose monolithic transistors
- Operation from DC to 120 MHz
- Wide operating current range
- Low noise figure 3.2 dB typ at 1 kHz
- Full military temperature range (LM3045) −55°C to +125°C

Applications

- General use in all types of signal processing systems operating anywhere in the frequency range from DC to VHF
- Custom designed differential amplifiers
- Temperature compensated amplifiers

Schematic and Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number LM3045J
See NS Package J14A
Order Number LM3046N
or LM3086N
See NS Package N14A

Absolute Maximum Ratings (T_A = 25°C)

	LM3045 Each Transistor	LM3045 Total Package	LM3046/LM3086 Each Transistor	LM3046/LM3086 Total Package	Units
Power Dissipation:					
T_A = 25°C	300	750	300	750	mW
T_A = 25°C to 55°C			300	750	mW
$T_A > 55°C$			Derate at 6.67		mW/°C
T_A = 25°C to 75°C	300	750			mW
$T_A > 75°C$	Derate at 8				mW/°C
Collector to Emitter Voltage, V_{CEO}	15		15		V
Collector to Base Voltage, V_{CBO}	20		20		V
Collector to Substrate Voltage, V_{CIO} (Note 1)	20		20		V
Emitter to Base Voltage, V_{EBO}	5		5		V
Collector Current, I_C	50		50		mA
Operating Temperature Range	−55°C to +125°C		−40°C to +85°C		
Storage Temperature Range	−65°C to +150°C		−65°C to +85°C		
Lead Temperature (Soldering, 10 sec)	300		300		°C

Electrical Characteristics (T_A = 25°C unless otherwise specified)

PARAMETER	CONDITIONS	LIMITS LM3045, LM3046			LIMITS LM3086			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Collector to Base Breakdown Voltage ($V_{(BR)CBO}$)	I_C = 10µA, I_E = 0	20	60		20	60		V
Collector to Emitter Breakdown Voltage ($V_{(BR)CEO}$)	I_C = 1 mA, I_B = 0	15	24		15	24		V
Collector to Substrate Breakdown Voltage ($V_{(BR)CIO}$)	I_C = 10µA, I_{CI} = 0	20	60		20	60		V
Emitter to Base Breakdown Voltage ($V_{(BR)EBO}$)	I_E = 10µA, I_C = 0	5	7		5	7		V
Collector Cutoff Current (I_{CBO})	V_{CB} = 10V, I_E = 0		.002	40		.002	100	nA
Collector Cutoff Current (I_{CEO})	V_{CE} = 10V, I_B = 0			.5			5	µA
Static Forward Current Transfer Ratio (Static Beta) (h_{FE})	V_{CE} = 3V: I_C = 10 mA I_C = 1 mA I_C = 10 µA	 40 	100 100 54		 40 	100 100 54		
Input Offset Current for Matched Pair Q_1 and Q_2 $\|I_{IO1} - I_{IO2}\|$	V_{CE} = 3V, I_C = 1 mA		.3	2				µA
Base to Emitter Voltage (V_{BE})	V_{CE} = 3V: I_E = 1 mA I_E = 10 mA		.715 .800			.715 .800		V
Magnitude of Input Offset Voltage for Differential Pair $\|V_{BE1} - V_{BE2}\|$	V_{CE} = 3V, I_C = 1 mA		.45	5				mV
Magnitude of Input Offset Voltage for Isolated Transistors $\|V_{BE3} - V_{BE4}\|$, $\|V_{BE4} - V_{BE5}\|$, $\|V_{BE5} - V_{BE3}\|$	V_{CE} = 3V, I_C = 1 mA		.45	5				mV
Temperature Coefficient of Base to Emitter Voltage $\left(\frac{\Delta V_{BE}}{\Delta T}\right)$	V_{CE} = 3V, I_C = 1 mA		−1.9			−1.9		mV/°C
Collector to Emitter Saturation Voltage ($V_{CE(SAT)}$)	I_B = 1 mA, I_C = 10 mA		.23			.23		V
Temperature Coefficient of Input Offset Voltage $\left(\frac{\Delta V_{IO}}{\Delta T}\right)$	V_{CE} = 3V, I_C = 1 mA		1.1					µV/°C

Note 1: The collector of each transistor of the LM3045, LM3046, and LM3086 is isolated from the substrate by an integral diode. The substrate (terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

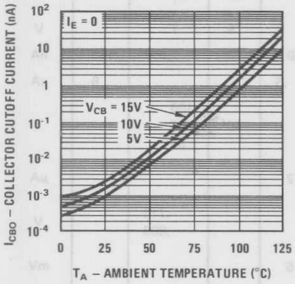
LM3045, LM3046, LM3086

Electrical Characteristics (Continued)

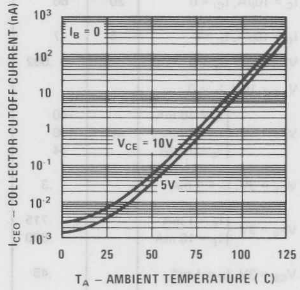
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Low Frequency Noise Figure (NF)	f = 1 kHz, V_{CE} = 3V, I_C = 100μA R_S = 1 kΩ		3.25		dB
Low Frequency, Small Signal Equivalent Circuit Characteristics:					
Forward Current Transfer Ratio (h_{fe})			110 (LM3045, LM3046) (LM3086)		
Short Circuit Input Impedance (h_{ie})	f = 1 kHz, V_{CE} = 3V, I_C = 1 mA		3.5		kΩ
Open Circuit Output Impedance (h_{oe})			15.6		μmho
Open Circuit Reverse Voltage Transfer Ratio (h_{re})			1.8×10^{-4}		
Admittance Characteristics:					
Forward Transfer Admittance (Y_{fe})			31 - j 1.5		
Input Admittance (Y_{ie})	f = 1 MHz, V_{CE} = 3V, I_C = 1 mA		0.3+j 0.04		
Output Admittance (Y_{oe})			0.001+j 0.03		
Reverse Transfer Admittance (Y_{re})			See curve		
Gain Bandwidth Product (f_T)	V_{CE} = 3V, I_C = 3 mA	300	550		
Emitter to Base Capacitance (C_{EB})	V_{EB} = 3V, I_E = 0		.6		pF
Collector to Base Capacitance (C_{CB})	V_{CB} = 3V, I_C = 0		.58		pF
Collector to Substrate Capacitance (C_{CI})	V_{CS} = 3V, I_C = 0		2.8		pF

Typical Performance Characteristics

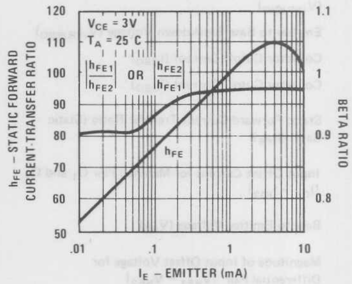
Typical Collector To Base Cutoff Current vs Ambient Temperature for Each Transistor



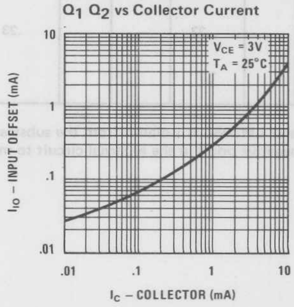
Typical Collector To Emitter Cutoff Current vs Ambient Temperature for Each Transistor



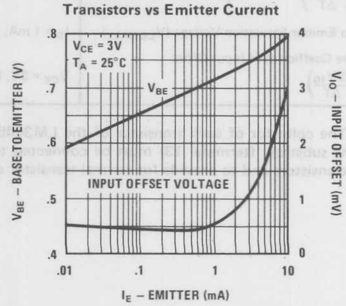
Typical Static Forward Current-Transfer Ratio and Beta Ratio for Transistors Q_1 and Q_2 vs Emitter Current



Typical Input Offset Current for Matched Transistor Pair Q_1 Q_2 vs Collector Current

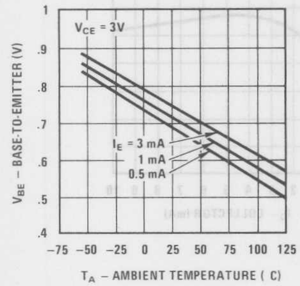


Typical Static Base To Emitter Voltage Characteristic and Input Offset Voltage for Differential Pair and Paired Isolated Transistors vs Emitter Current

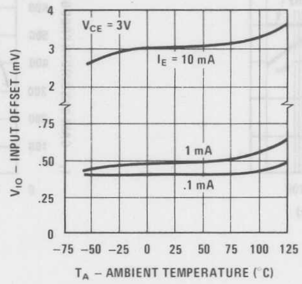


Typical Performance Characteristics (Continued)

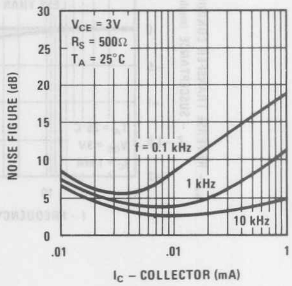
Typical Base To Emitter Voltage Characteristic for Each Transistor vs Ambient Temperature



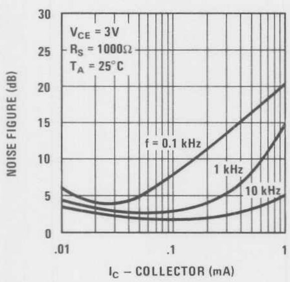
Typical Input Offset Voltage Characteristics for Differential Pair and Paired Isolated Transistors vs Ambient Temperature



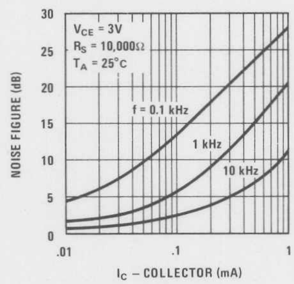
Typical Noise Figure vs Collector Current



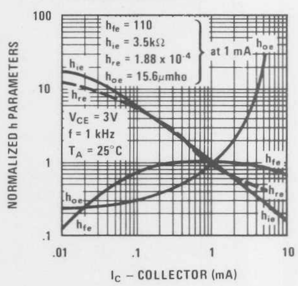
Typical Noise Figure vs Collector Current



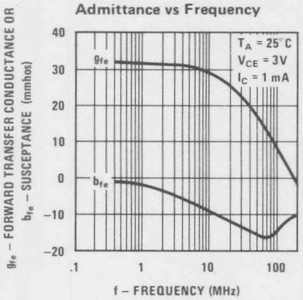
Typical Noise Figure vs Collector Current



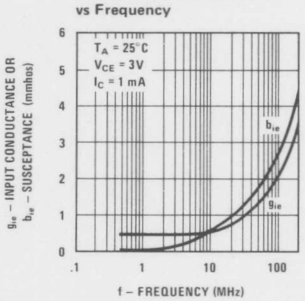
Typical Normalized Forward Current Transfer Ratio, Short Circuit Input Impedance, Open Circuit Output Impedance, and Open Circuit Reverse Voltage Transfer Ratio vs Collector Current



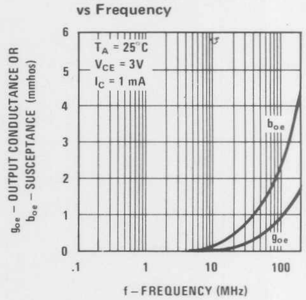
Typical Forward Transfer Admittance vs Frequency



Typical Input Admittance vs Frequency

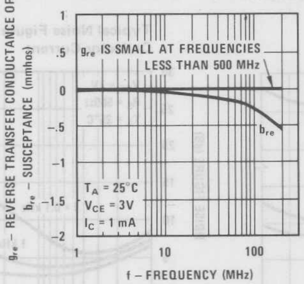


Typical Output Admittance vs Frequency

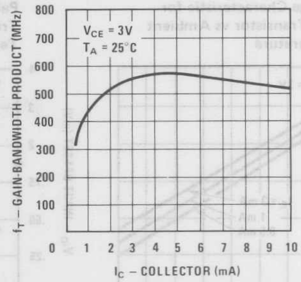


Typical Performance Characteristics (Continued)

Typical Reverse Transfer Admittance vs Frequency



Typical Gain-Bandwidth Product vs Collector Current



National Semiconductor

LM3146 High Voltage Transistor Array

General Description

The LM3146 consists of five high voltage general purpose silicon NPN transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair. The transistors are well suited to a wide variety of applications in low power system in the dc through VHF range. They may be used as discrete transistors in conventional circuits however, in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching. The LM3146 is supplied in a 14-lead molded dual-in-line package for applications requiring only a limited temperature range.

Features

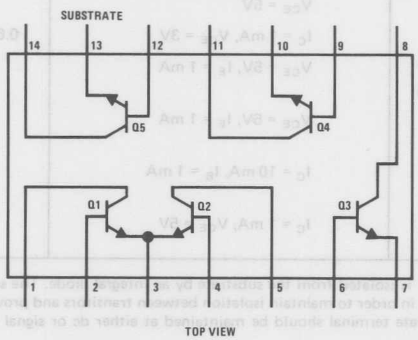
- High voltage matched pairs of transistors, V_{BE} matched ±5 mV, input offset current 2μA max at I_C = 1 mA
- Five general purpose monolithic transistors
- Operation from dc to 120 MHz
- Wide operating current range
- Low noise figure 3.2 dB typ at 1 kHz

Applications

- General use in all types of signal processing systems operating anywhere in the frequency range from dc to VHF
- Custom designed differential amplifiers
- Temperature compensated amplifiers

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number LM3146N
See NS Package N14A

Power Dissipation: Each Transistor		
$T_A = 25°C$ to $55°C$	300	mW
$T_A > 55°C$	Derate at 6.67	mW/°C
Power Dissipation: Total Package		
$T_A = 25°C$	500	mW
$T_A > 25°C$	Derate at 6.67	mW/°C
Collector to Emitter Voltage, V_{CEO}	30	V
Collector to Base Voltage, V_{CBO}	40	V
Collector to Substrate Voltage, V_{CIO} (Note 1)	40	V
Emitter to Base Voltage, V_{EBO} (Note 2)	5	V
Collector Current, I_C	50	mA
Operating Temperature Range	−40 to +85	°C
Storage Temperature Range	−65 to +150	°C
Lead Temperature (Soldering, 10 seconds)	300	°C

DC Electrical Characteristics $T_A = 25°C$

PARAMETER	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Collector to Base Breakdown Voltage ($V_{(BR)CBO}$)	$I_C = 10\mu A$, $I_E = 0$	40	72		V
Collector to Emitter Breakdown Voltage ($V_{(BR)CEO}$)	$I_C = 1$ mA, $I_B = 0$	30	56		V
Collector to Substrate Breakdown Voltage ($V_{(BR)CIO}$)	$I_{CI} = 10\mu A$, $I_B = 0$, $I_E = 0$	40	72		V
Emitter to Base Breakdown Voltage ($V_{(BR)EBO}$) (Note 2)	$I_C = 0$, $I_E = 10\mu A$	5	7		V
Collector Cutoff Current (I_{CBO})	$V_{CB} = 10V$, $I_E = 0$		0.002	100	nA
Collector Cutoff Current (I_{CEO})	$V_{CE} = 10V$, $I_B = 0$		(Note 3)	5	μA
Static Forward Current Transfer Ratio (Static Beta) (h_{FE})	$I_C = 10$ mA, $V_{CE} = 5V$ $I_C = 1$ mA, $V_{CE} = 5V$ $I_C = 10\mu A$, $V_{CE} = 5V$	30	85 100 90		
Input Offset Current for Matched Pair Q1 and Q2 $\lvert I_{B1} - I_{B2}\rvert$	$I_{C1} = I_{C2} = 1$ mA, $V_{CE} = 5V$		0.3	2	μA
Base to Emitter Voltage (V_{BE})	$I_C = 1$ mA, $V_{CE} = 3V$	0.63	0.73	0.83	V
Magnitude of Input Offset Voltage for Differential Pair $\lvert V_{BE1} - V_{BE2}\rvert$	$V_{CE} = 5V$, $I_E = 1$ mA		0.48	5	mV
Temperature Coefficient of Base to Emitter Voltage ($\Delta V_{BE}/\Delta T$)	$V_{CE} = 5V$, $I_E = 1$ mA		−1.9		mV/°C
Collector to Emitter Saturation Voltage ($V_{CE(SAT)}$)	$I_C = 10$ mA, $I_B = 1$ mA		0.33		V
Temperature Coefficient of Input Offset Voltage ($\Delta V_{10}/\Delta T$)	$I_C = 1$ mA, $V_{CE} = 5V$		1.1		μV/°C

Note 1: The collector of each transistor is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transitors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal should be maintained at either dc or signal (ac) ground. A suitable bypass capacitor can be used to establish a signal ground.

Note 2: If the transistors are forced into zener breakdown ($V_{(BR)EBO}$), degradation of forward transfer current ratio (h_{FE}) can occur.

Note 3: See curve.

AC Electrical Characteristics

PARAMETER	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Low Frequency Noise Figure (NF)	f = 1 kHz, V_{CE} = 5V, I_C = 100μA, R_S = 1 kΩ		3.25		dB
Gain Bandwidth Product (f_T)	V_{CE} = 5V, I_C = 3 mA	300	500		MHz
Emitter to Base Capacitance (C_{EB})	V_{EB} = 5V, I_E = 0		0.70		pF
Collector to Base Capacitance (C_{CB})	V_{CB} = 5V, I_C = 0		0.37		pF
Collector to Substrate Capacitance (C_{CI})	V_{CI} = 5V, I_C = 0		2.2		pF
LOW FREQUENCY, SMALL SIGNAL EQUIVALENT CIRCUIT CHARACTERISTICS					
Forward Current Transfer Ratio (h_{fe})	f = 1 kHz, V_{CE} = 3V, I_C = 1 mA		100		
Short Circuit Input Impedance (h_{ie})	f = 1 kHz, V_{CE} = 3V, I_C = 1 mA		3.5		kΩ
Open Circuit Output Impedance (h_{oe})	f = 1 kHz, V_{CE} = 3V, I_C = 1 mA		15.6		μmho
Open Circuit Reverse Voltage Transfer Ratio (h_{re})	f = 1 kHz, V_{CE} = 3V, I_C = 1 mA		1.8×10^{-4}		
ADMITTANCE CHARACTERISTICS					
Forward Transfer Admittance (Y_{fe})	f = 1 MHz, V_{CE} = 3V, I_C = 1 mA		31 − j 1.5		mmho
Input Admittance (Y_{ie})	f = 1 MHz, V_{CE} = 3V, I_C = 1 mA		0.3 + j 0.04		mmho
Output Admittance (Y_{oe})	f = 1 MHz, V_{CE} = 3V, I_C = 1 mA		0.001 + j 0.03		mmho
Reverse Transfer Admittance (Y_{re})	f = 1 MHz, V_{CE} = 3V, I_C = 1 mA		(Note 3)		mmho

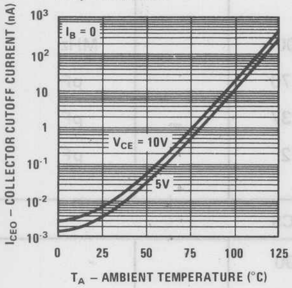
Note 1: The collector of each transistor is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transitors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal should be maintained at either dc or signal (ac) ground. A suitable bypass capacitor can be used to establish a signal ground.

Note 2: If the transistors are forced into zener breakdown ($V_{(BR)EBO}$), degradation of forward transfer current ratio (h_{FE}) can occur.

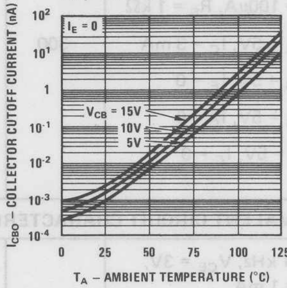
Note 3: See curve.

Typical Performance Characteristics

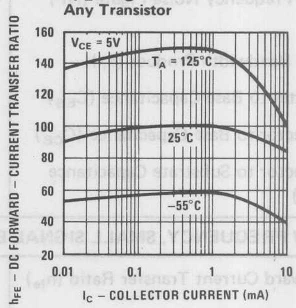
I_{CEO} vs T_A for Any Transistor



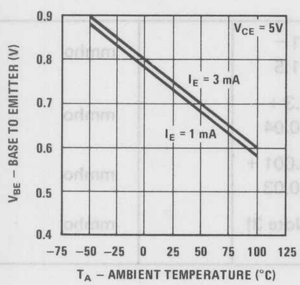
I_{CBO} vs T_A for Any Transistor



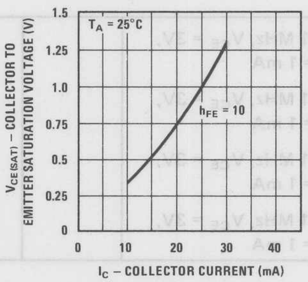
h_{FE} vs I_C for Any Transistor



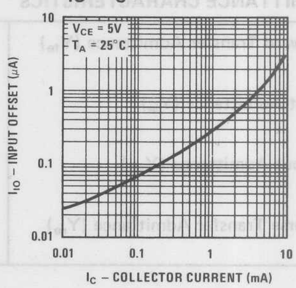
V_{BE} vs T_A for Any Transistor



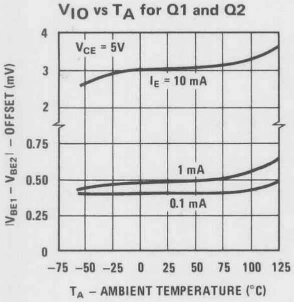
$V_{CE(SAT)}$ vs I_C for Any Transistor



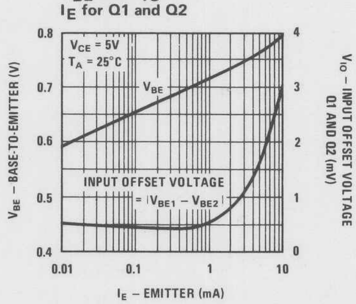
I_{IO} vs I_C (Q1 and Q2)



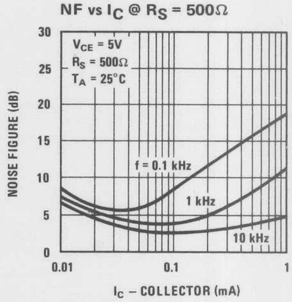
V_{IO} vs T_A for Q1 and Q2



V_{BE} and V_{IO} vs I_E for Q1 and Q2

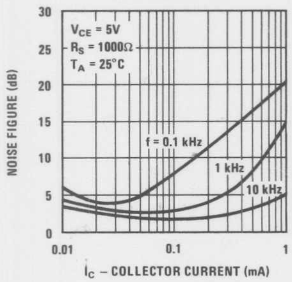


NF vs I_C @ R_S = 500Ω

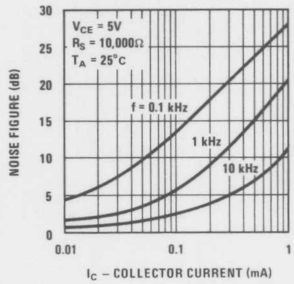


Typical Performance Characteristics (Continued)

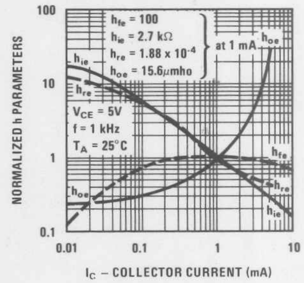
NF vs I_C @ R_S = 1 kΩ



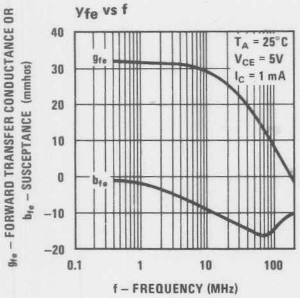
NF vs I_C = R_S = 10 kΩ



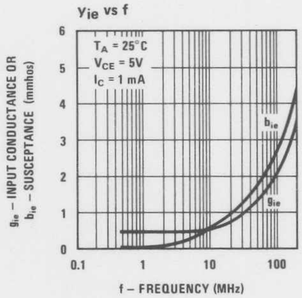
h_{fe}, h_{ie}, h_{oe}, h_{re} vs I_C



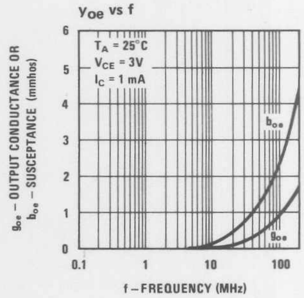
y_{fe} vs f



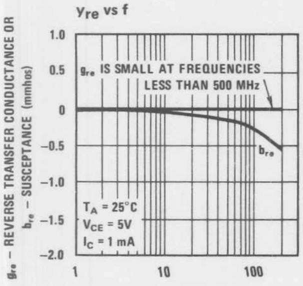
y_{ie} vs f



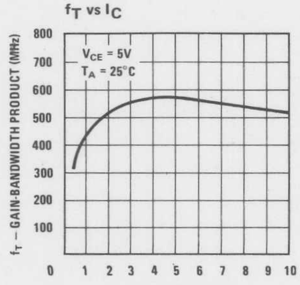
y_{oe} vs f



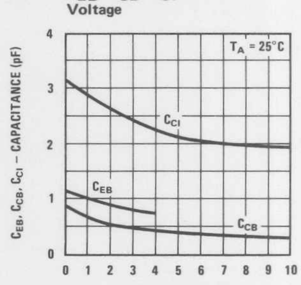
y_{re} vs f



f_T vs I_C



C_{EB}, C_{CB}, C_{CI} vs Bias Voltage



Section 13
DIGITALKER™ Speech Synthesis

13

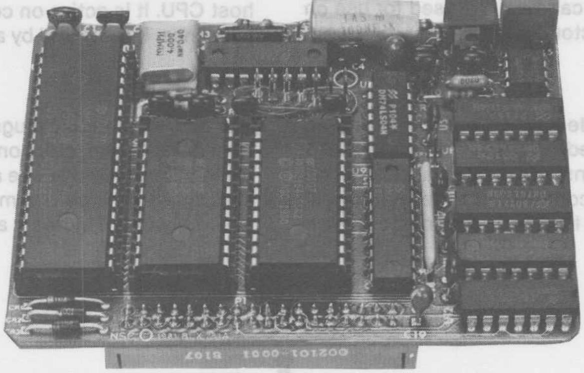
DIGITALKER™ Speech Synthesis

Section Contents

National Semiconductor

DIGITALKER™ Speech Synthesis

BLX-281
Speech Synthesis Expansion Module



- **BLX bus-compatible I/O expansion**
- **Speech synthesis based on DIGITALKER™**
- **Large vocabulary adequate for most applications**
- **On-board filter and half-watt amplifier**
- **Simple operation for user**
  - I/O write with word/sound address
  - Interrupt asserted when complete
- **BLX bus on-board expansion elimates Multibus™ system bus latency and increases system throughput**

Product Overview

The BLX-281 Speech Synthesis Expansion Module is a member of the new line of BLX bus-compatible expansion module products from National Semiconductor Corporation. The BLX-281 plugs directly into any BLX bus-compatible host board offering low cost incremental on-board expansion. As a result, any BLX bus-compatible host board may be given the ability to "speak". By merely adding a speaker to a system containing the BLX-281, many users can do away with CRTs, printers, rows of LEDs, or similar communications devices. This lowers the cost of most systems, and has the added benefit of removing messages which are potentially ambiguous and hard-to-understand for untrained users. The BLX-281 contains 144 words, sounds, tones, and durations of silence, each of which has a unique address. A table of addresses (desired words/sounds) is built, and passed to the BLX-281. An on-board filter and amplifier provide the actual speech signal to a standard miniature phone jack. The BLX module is closely coupled to the host board through the BLX bus, and as such, offers maximum on-board performance, and frees Multibus system traffic for other system resources. Incremental power dissipation is minimal, requiring only 3.7 watts.

DIGITALKER is a trademark of National Semiconductor Corp.

Functional Description

The BLX-281 Speech Synthesis Expansion Module uses the MM54104 Speech Processor Chip from National Semiconductor Corporation. The digitized and compressed speech data are contained in an MM52164 Maxi-ROM. The system software communicates with the BLX-281 across the BLX bus using I/O read/write commands.

Vocabulary

The standard vocabulary set offered on the BLX-281 is shown in Table I, along with the assigned addresses for each item. By combining the appropriate words, sounds, tones, and silence durations, speech can be generated to satisfy many applications.

Words required, but not found in the table, can frequently be built. Examples of this are: combine "RE" with "SET" for "RESET", or combine "DEGREE" with "SS" for "DEGREES".

In normal human speech, the brain puts durations of silence between the words to make the sentence flow smoothly. This is provided for in the BLX-281 (see Table I). A suggestion for improved phrase quality is to insert 80 milliseconds of silence prior

Multibus is a trademark of Intel Corp.

The "voice" output of the BLX-281 is a highly intelligible, male voice. If another voice is required, or the application is non-English, or involves unusual terminology, any voice can be processed for use on the BLX-281 by the factory.

Host Interface

The BLX bus-compatible host board merely passes the address of the desired word/sound to the BLX-281 Speech Synthesis Expansion Module via an I/O write. When the operation is complete, an interrupt is generated. This informs the host of the end of the speech

Interrupt Requests

There is one interrupt line from the Speech Processor Chip that generates an interrupt request to the host CPU. It is active on completion of each speech sequence. It is cleared by an I/O read to the BLX-281.

Installation

The BLX-281 module plugs directly into either of the female BLX connectors on the host board. The module is then secured at one additional point with nylon hardware to insure the mechanical security of the assembly (see Figures 1 and 2).

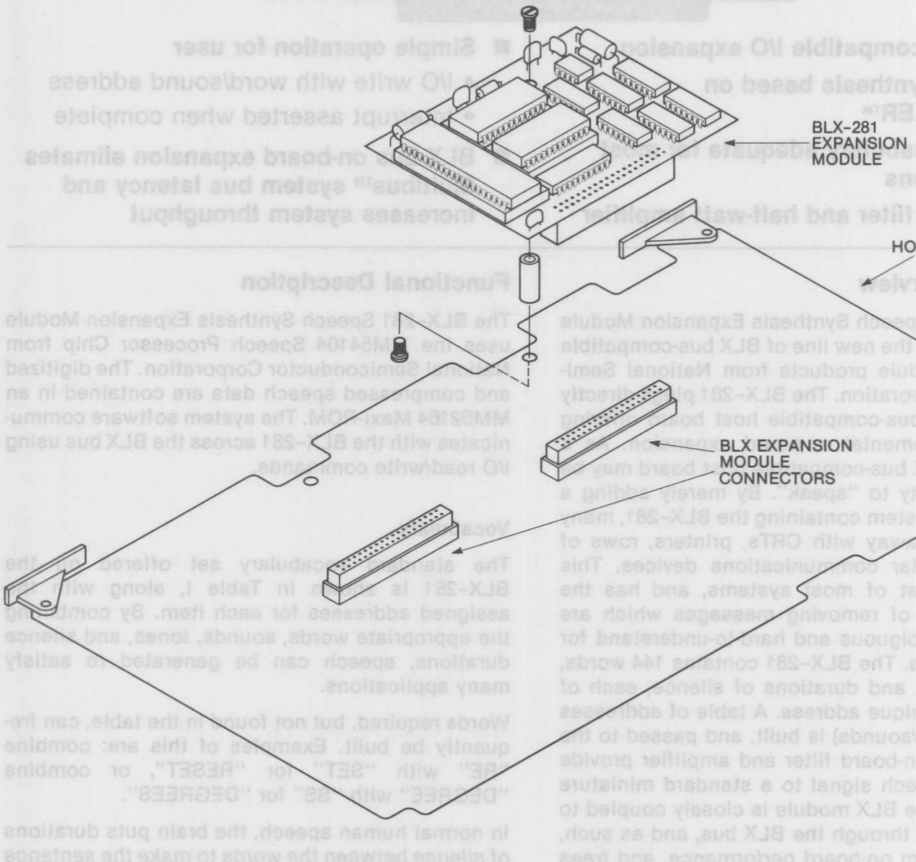


Figure 1. Installation of the BLX-281 Module on a Host Board

Table I. Master Word List

Word	8-Bit Binary Address Bit 7 Bit 0	Word	8-Bit Binary Address Bit 7 Bit 0	Word	8-Bit Binary Address Bit 7 Bit 0
THIS IS DIGITALKER	0 0 0 0 0 0 0 0	Q	0 0 1 1 0 0 0 0	IS	0 1 1 0 0 0 0 0
ONE	0 0 0 0 0 0 0 1	R	0 0 1 1 0 0 0 1	IT	0 1 1 0 0 0 0 1
TWO	0 0 0 0 0 0 1 0	S	0 0 1 1 0 0 1 0	KILO	0 1 1 0 0 0 1 0
THREE	0 0 0 0 0 0 1 1	T	0 0 1 1 0 0 1 1	LEFT	0 1 1 0 0 0 1 1
FOUR	0 0 0 0 0 1 0 0	U	0 0 1 1 0 1 0 0	LESS	0 1 1 0 0 1 0 0
FIVE	0 0 0 0 0 1 0 1	V	0 0 1 1 0 1 0 1	LESSER	0 1 1 0 0 1 0 1
SIX	0 0 0 0 0 1 1 0	W	0 0 1 1 0 1 1 0	LIMIT	0 1 1 0 0 1 1 0
SEVEN	0 0 0 0 0 1 1 1	X	0 0 1 1 0 1 1 1	LOW	0 1 1 0 0 1 1 1
EIGHT	0 0 0 0 1 0 0 0	Y	0 0 1 1 1 0 0 0	LOWER	0 1 1 0 1 0 0 0
NINE	0 0 0 0 1 0 0 1	Z	0 0 1 1 1 0 0 1	MARK	0 1 1 0 1 0 0 1
TEN	0 0 0 0 1 0 1 0	AGAIN	0 0 1 1 1 0 1 0	METER	0 1 1 0 1 0 1 0
ELEVEN	0 0 0 0 1 0 1 1	AMPERE	0 0 1 1 1 0 1 1	MILE	0 1 1 0 1 0 1 1
TWELVE	0 0 0 0 1 1 0 0	AND	0 0 1 1 1 1 0 0	MILLI	0 1 1 0 1 1 0 0
THIRTEEN	0 0 0 0 1 1 0 1	AT	0 0 1 1 1 1 0 1	MINUS	0 1 1 0 1 1 0 1
FOURTEEN	0 0 0 0 1 1 1 0	CANCEL	0 0 1 1 1 1 1 0	MINUTE	0 1 1 0 1 1 1 0
FIFTEEN	0 0 0 0 1 1 1 1	CASE	0 0 1 1 1 1 1 1	NEAR	0 1 1 0 1 1 1 1
SIXTEEN	0 0 0 1 0 0 0 0	CENT	0 1 0 0 0 0 0 0	NUMBER	0 1 1 1 0 0 0 0
SEVENTEEN	0 0 0 1 0 0 0 1	400 Hz TONE	0 1 0 0 0 0 0 1	OF	0 1 1 1 0 0 0 1
EIGHTEEN	0 0 0 1 0 0 1 0	80 Hz TONE	0 1 0 0 0 0 1 0	OFF	0 1 1 1 0 0 1 0
NINETEEN	0 0 0 1 0 0 1 1	20 ms SILENCE	0 1 0 0 0 0 1 1	ON	0 1 1 1 0 0 1 1
TWENTY	0 0 0 1 0 1 0 0	40 ms SILENCE	0 1 0 0 0 1 0 0	OUT	0 1 1 1 0 1 0 0
THIRTY	0 0 0 1 0 1 0 1	80 ms SILENCE	0 1 0 0 0 1 0 1	OVER	0 1 1 1 0 1 0 1
FORTY	0 0 0 1 0 1 1 0	160 ms SILENCE	0 1 0 0 0 1 1 0	PARENTHESIS	0 1 1 1 0 1 1 0
FIFTY	0 0 0 1 0 1 1 1	320 ms SILENCE	0 1 0 0 0 1 1 1	PERCENT	0 1 1 1 0 1 1 1
SIXTY	0 0 0 1 1 0 0 0	CENTI	0 1 0 0 1 0 0 0	PLEASE	0 1 1 1 1 0 0 0
SEVENTY	0 0 0 1 1 0 0 1	CHECK	0 1 0 0 1 0 0 1	PLUS	0 1 1 1 1 0 0 1
EIGHTY	0 0 0 1 1 0 1 0	COMMA	0 1 0 0 1 0 1 0	POINT	0 1 1 1 1 0 1 0
NINETY	0 0 0 1 1 0 1 1	CONTROL	0 1 0 0 1 0 1 1	POUND	0 1 1 1 1 0 1 1
HUNDRED	0 0 0 1 1 1 0 0	DANGER	0 1 0 0 1 1 0 0	PULSES	0 1 1 1 1 1 0 0
THOUSAND	0 0 0 1 1 1 0 1	DEGREE	0 1 0 0 1 1 0 1	RATE	0 1 1 1 1 1 0 1
MILLION	0 0 0 1 1 1 1 0	DOLLAR	0 1 0 0 1 1 1 0	RE	0 1 1 1 1 1 1 0
ZERO	0 0 0 1 1 1 1 1	DOWN	0 1 0 0 1 1 1 1	READY	0 1 1 1 1 1 1 1
A	0 0 1 0 0 0 0 0	EQUAL	0 1 0 1 0 0 0 0	RIGHT	1 0 0 0 0 0 0 0
B	0 0 1 0 0 0 0 1	ERROR	0 1 0 1 0 0 0 1	SS	1 0 0 0 0 0 0 1
C	0 0 1 0 0 0 1 0	FEET	0 1 0 1 0 0 1 0	SECOND	1 0 0 0 0 0 1 0
D	0 0 1 0 0 0 1 1	FLOW	0 1 0 1 0 0 1 1	SET	1 0 0 0 0 0 1 1
E	0 0 1 0 0 1 0 0	FUEL	0 1 0 1 0 1 0 0	SPACE	1 0 0 0 0 1 0 0
F	0 0 1 0 0 1 0 1	GALLON	0 1 0 1 0 1 0 1	SPEED	1 0 0 0 0 1 0 1
G	0 0 1 0 0 1 1 0	GO	0 1 0 1 0 1 1 0	STAR	1 0 0 0 0 1 1 0
H	0 0 1 0 0 1 1 1	GRAM	0 1 0 1 0 1 1 1	START	1 0 0 0 0 1 1 1
I	0 0 1 0 1 0 0 0	GREAT	0 1 0 1 1 0 0 0	STOP	1 0 0 0 1 0 0 0
J	0 0 1 0 1 0 0 1	GREATER	0 1 0 1 1 0 0 1	THAN	1 0 0 0 1 0 0 1
K	0 0 1 0 1 0 1 0	HAVE	0 1 0 1 1 0 1 0	THE	1 0 0 0 1 0 1 0
L	0 0 1 0 1 0 1 1	HIGH	0 1 0 1 1 0 1 1	TIME	1 0 0 0 1 0 1 1
M	0 0 1 0 1 1 0 0	HIGHER	0 1 0 1 1 1 0 0	TRY	1 0 0 0 1 1 0 0
N	0 0 1 0 1 1 0 1	HOUR	0 1 0 1 1 1 0 1	UP	1 0 0 0 1 1 0 1
O	0 0 1 0 1 1 1 0	IN	0 1 0 1 1 1 1 0	VOLT	1 0 0 0 1 1 1 0
P	0 0 1 0 1 1 1 1	INCHES	0 1 0 1 1 1 1 1	WEIGHT	1 0 0 0 1 1 1 1

Note: Address $8F_H$ is the last legal address in this word list. Exceeding address $8F_H$ will produce pieces of unintelligible, invalid speech data.

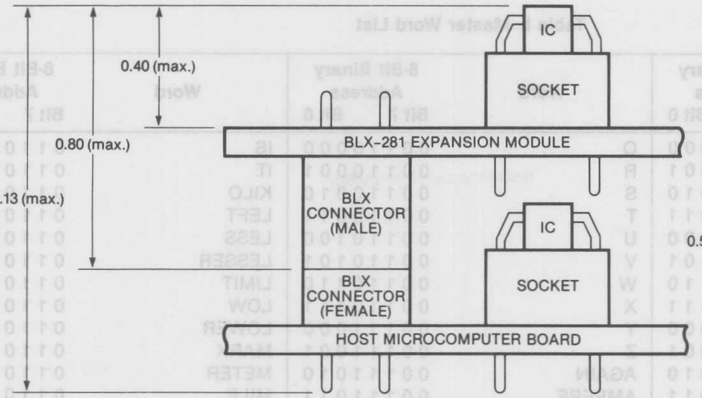


Figure 2. BLX-281 Expansion Module Mounting Clearances (inches)

Specifications

Word Size

Data — 8 bits

I/O Addressing

Function	Type of Operation	BLX Connector Port Address
Data Transfer	Write	X0-XF
Interrupt Clear	Read	X0-XF

Note: The port addresses are determined on the host BLC microcomputer. Refer to the Hardware Reference Manual for your host BLC microcomputer to determine the first digit (X) of the connector port address.

Vocabulary — See Table I

Interrupts — One interrupt request at end of speech sequence

Interfaces — BLX Bus — All signals TTL compatible

Speaker Port — ½W audio signal into 4-8Ω

Speaker Port Connector — Standard miniature phone-jack

Physical

Height: 2.85 in. (7.24 cm)
Width: 3.70 in. (9.40 cm)
Depth
BLX-281 Module
0.80 in. (2.04 cm)
BLX-281 Module + Host Board
1.13 in. (2.86 cm)
Weight: 1.7 oz. (48 gm)

Electrical

+5 VDC ± 5% @ 385 mA
+12 VDC ± 5% @ 150 mA

Environmental

Operating Temperature: 0°C to 55°C
Relative Humidity: 0% to 90%, non-condensing

Ordering Information

BLX-281 Speech Synthesis Expansion Module

Documentation

420306414-001 BLX-281 Speech Synthesis Expansion Module User's Manual

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National Semiconductor

DIGITALKER™ Speech Synthesis

DT1000 DIGITALKER™ Speech Synthesis Evaluation Board

General Description

The DIGITALKER™ (DT1000) speech synthesis evaluation board is an extremely easy to use device for understanding the operation and application of the DIGITALKER chip set in an end product.

The DT1000 contains all components required to output speech upon demand: a speech processor chip (SPC), 2 MAXI-ROMs® containing 138 individual words, linear filter, audio amplifier, keyboard, and a COPS™ microcontroller complete with stored data programmed to provide the various functions on the board. The only external hardware required for complete operation are a single 7V–11V power supply, a speaker of your choice for size and quality, and this instruction sheet.

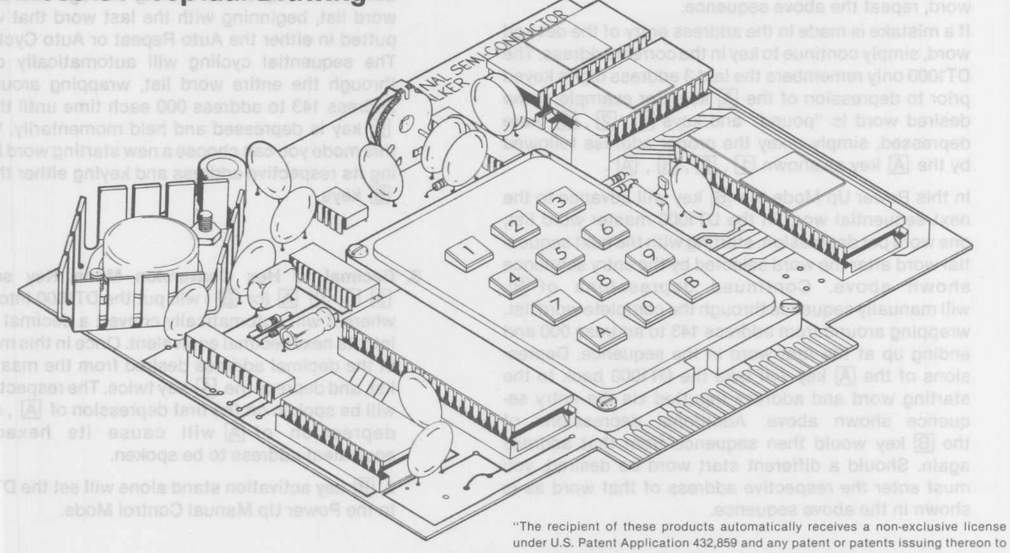
The 2 speech MAXI-ROMs employed on the board contain a brief introductory phrase, 138 separate and individual words consisting of numbers and letters of the alphabet, assorted useful nouns, verbs and tones; and 5 different individual silence durations. (In constructing a phrase, different silence durations between different words significantly affect the overall quality of the phrase.)

A COPS program is provided which permits the user to: 1) sequentially output each word automatically; 2) repeat any desired word; 3) build and store several short phrases for outputting when desired; 4) output a "canned" phrase which permits insertions and changing of a word in the phrase; 5) play a simple game which requires some interaction between the keyboard and the user; and 6) output hex equivalent decimal number inputs.

Features

- Only a single 7V–11V power supply and inexpensive loudspeaker required for total operation
- 138 individually addressable words, applicable to many products
- Programmed COPS processor permits 6 individual program modes
- Demonstrates the extreme flexibility and ease of application of the DIGITALKER chip set
- 1/2 watt audio amplifier on-board
- Edge connector facilitates tying in to external processor system (3M Company connector part number #3415)

DT1000 Conceptual Drawing



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V_{DD} Supply Voltage 12V

Electrical Characteristics $T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}*	Supply Voltage	$V_{SS} = 0V$	7.0		11.0	V
I_{DD}	Supply Current	$V_{DD} = 11V$			0.6	A
	Amplifier Output	$V_{DD} = 11V, 8\Omega$	0.55			W
		$V_{DD} = 9V, 8\Omega$	0.50			W

*** Important!** V_{DD} must be regulated!

All pin connections, except for speaker out, and power supply, are TTL compatible.

Functional Description

INSTRUCTIONS FOR USE

In any case, plus 7V to 11V direct current and ground must be brought to the respective pins on the edge connector of the DT1000 board. See *Figure 1.*

BASIC MODE OPERATIONS

1. **Power Up Mode.** At power up, the DT1000 will say "This is DIGITALKER". You can make it repeat this phrase by depressing $\boxed{A}$. Further depressions of $\boxed{A}$ will repeat the same phrase until a new word address is entered. From the DT1000 master word list (Table I) select the 3-digit address of the next word desired. The new word can be outputted simply by keying in its 3-digit address and ending with an $\boxed{A}$ key depression. For example, the word "pound" will be spoken as a result of key sequence $\boxed{1}$, $\boxed{2}$, $\boxed{3}$, $\boxed{A}$. Additional depressions of A will repeat the word "pound". To output a new word, repeat the above sequence.

   If a mistake is made in the address entry of the desired word, simply continue to key in the correct address. The DT1000 only remembers the last 3 address digits keyed prior to depression of the $\boxed{A}$ key. For example, if the desired word is "pound" and keys $\boxed{1}$, $\boxed{2}$, $\boxed{2}$ were depressed, simply rekey the proper address followed by the $\boxed{A}$ key as shown $\boxed{1}$, $\boxed{2}$, $\boxed{3}$, $\boxed{A}$.

   In this Power Up Mode the $\boxed{B}$ key will advance to the next sequential word in the DT1000 master word list, one word per depression, starting with the next sequential word after the word selected by the entry sequence shown above. Continued depressions of $\boxed{B}$ will manually sequence through the complete word list, wrapping around from address 143 to address 000 and ending up at the first word in the sequence. Depressions of the $\boxed{A}$ key will take the DT1000 back to the starting word and address inputted via the entry sequence shown above. Additional depressions of the $\boxed{B}$ key would then sequence from that address again. Should a different start word be desired, you must enter the respective address of that word as is shown in the above sequence.

The DT1000 has 144 legal address locations, these are shown in the Master Word List as being addresses 000 through 143. If an address of 144 through 199 is inadvertently keyed in, a response of "Please Try Again" will be outputted. Addresses 200 and up will put the DT1000 into various operating modes as explained in paragraphs 2 through 7.

2. **Auto Repeat/Auto Cycle Mode.** The Auto Repeat/Cycle Mode is entered by depressing $\boxed{2}$ $\boxed{0}$ $\boxed{0}$ and either the $\boxed{A}$ or $\boxed{B}$ key. An additional depression of $\boxed{A}$ will start an automatic repeating cycle of some word and address, until the $\boxed{A}$ key is depressed and held momentarily. Depression of the $\boxed{B}$ key will start the automatic sequential cycling through the complete word list, beginning with the last word that was outputted in either the Auto Repeat or Auto Cycle Mode. The sequential cycling will automatically continue through the entire word list, wrapping around from address 143 to address 000 each time until the $\boxed{A}$ or $\boxed{B}$ key is depressed and held momentarily. When in this mode you can choose a new starting word by entering its respective address and keying either the $\boxed{A}$ or $\boxed{B}$ keys.

3. **Decimal to Hex Conversion Mode.** Key sequence $\boxed{3}$ $\boxed{0}$ $\boxed{0}$ $\boxed{A}$ (or $\boxed{B}$) will put the DT1000 into a mode where it will automatically convert a decimal address into its hexadecimal equivalent. Once in this mode, key in the decimal address desired from the master word list, and depress the $\boxed{A}$ key twice. The respective word will be spoken on the first depression of $\boxed{A}$, a further depression of $\boxed{A}$ will cause its hexadecimal equivalent address to be spoken.

   A $\boxed{B}$ key activation stand alone will set the DT1000 into the Power Up Manual Control Mode.

Functional Description (Continued)

4. **Phrase Construct Mode.** In this mode, it is possible to string respective word addresses together to create up to 3 phrases or short sentences and play them back upon demand. The phrase modes are [4] [0] [0], [5] [0] [0], and [6] [0] [0]. The 400 mode will store up to twelve word addresses, the 500 and 600 modes will store up to six addresses each. Initial phrase construction should begin with key sequence [4] [0] [0] [B] where the [B] depression clears out any addresses previously stored. (In either the [4] [0] [0], [5] [0] [0], [6] [0] [0] sequence, the B key will "clear" out any previous addresses stored in those respective modes.) You are then ready to string addresses together to construct a phrase. To construct the phrase, simply enter each address of the words desired in the phrase and in the sequence in which the words are to be outputted. Each word address keyed in must be followed by two depressions of the [B] key. The first depression of the [B] key will speak the word at that respective address to give you a chance to "hear" the word before its address is "loaded" into the DT1000 RAM. A second depression of the [B] key will store that address into the DT1000 RAM and that word is then in position in the desired phrase. If upon the first depression of the [B] key the word outputted is not the desired word, simply key in the correct address and depress the [B] key again, and again finally to store into the RAM. In the construction of a phrase a "beep" will occur during the addressing of the last possible address that will fit into that particular phrase mode. (If additional addresses are still keyed in, they will replace the first addresses loaded in that same phrase.)

   An example of constructing a phrase is as follows for the desired word sequence "To start the time set the meter and go", key sequence: [4] [0] [0] [B] / [0] [0] [2] [B] [B] / [1] [3] [5] [B] [B] / [1] [3] [8] [B] [B] / [1] [3] [9] [B] [B] / [1] [3] [1] [B] [B] / [1] [3] [8] [B] [B] / [1] [0] [6] [B] [B] / [0] [6] [0] [B] [B] / [0] [8] [6] [B] [B] /. To output this same phrase, depress the [A] key. The above phrase should automatically be spoken from the DT1000. Additional keyings of [A] will output the same phrase until it is cleared out by a [4] [0] [0] [B] sequence.

   Registers 500 and 600 can be loaded in exactly the same way as shown above, except that the [5] [0] [0] [B] and/or the [6] [0] [0] [B] keys must be addressed to load those respective registers. Remember that registers 500 and 600 are each only 6 addresses long.

   If you chose to construct the exact phrase as shown above, you may have noticed that the spoken output was rather a mechanical output. This is primarily due to the fact that the words were butted against each other. In normal human speech, the brain puts durations of silence between the words to make the sentence flow smoothly. Since several durations of silence are provided in the Master Word List, the actual quality of the same phrase can be significantly improved by adding durations of silence (also assigned addresses) between the words. As one thinks about how the phrase is actually spoken, one might assume the approximate duration of silence between each word, and insert the closest duration of silence from the word list. It is found that some experimentation in this area can significantly enhance the quality of the desired phrase. A hint in this area would be that for words beginning with the letters K, T, P, B, D, and G insert 80 milliseconds silence prior to the words, and for words ending in the same letters as above, 40 milliseconds silence following the word is recommended. It is also possible in this mode to make any singular word plural by the addition of "SS" (Address 129) to the word. In this case no silence should be inserted between the word and the "SS".

4A. **Phrase Output Mode.** As stated in (4) any phrase can be outputted by being in the 400, 500 or 600 modes and depressing the [A] key. It is also possible to output all 3 phrases in any sequence. To "string" these phrases together, simply key in the phrase sequence desired concluded with two depressions of the [A] key. Key sequence [4] [5] [6] [A] [A] would output phrases at 400-500 and 600 respectively. (This would indicate that a sentence 24 addresses long might be constructed.) Any phrase sequence might actually be chosen, 546, 645, etc. For an interesting effect the same phrase could be outputted twice or even three times such as 455, 444, 664, etc.

5. **Canned Phrase Mode.** Key sequence [7] [0] [0] [A] (or [B]) will output a fixed phrase "The time is _ P.M.". This gives you the ability to insert the desired word(s) in the blank location. In this case "twelve OH one" might be appropriate. While in the [7] [0] [0] [A] mode simply key in the respective addresses of the words desired, inserting silences if required, exactly the same as constructing a phrase in the 400-500 or 600 modes. To output the completed phrase, simply depress the [A] key. To insert a new word sequence into the blank, key [7] [0] [0] [B] to erase the original contents. Then enter the new word addresses as required.

   This mode demonstrates how a talking clock or a trip computer might work. Changing data can be inserted at the required time as a part of a fixed message.

6. **Reaction Timer Game.** Key sequence [8] [0] [0] [A] (or [B]) enters you into a simple game which could conceptually be a real product. In this mode, the DT1000 speaks ten random numbers from zero to nine, with a pause between each number output. The game is to hit the respective key as fast as possible after the number has been called out. After the tenth and last number has been depressed, a tone is outputted and the total reaction time is spoken as "seven point three two five seconds". Obviously, the game is to have the lowest possible total reaction time. *Note that it is necessary to eventually hit the correct key for the number called out.* If the wrong key is depressed, the DT1000 will not output another number until the correct key is depressed–meanwhile, time is accruing. It should also be noted that the random pauses between word outputs is not part of total elapsed time.

   To continue playing the game, keying the [A] key will output a new set of numbers. To exit the game mode, depress the [B] key.

7. **Back to Power Up Mode.** Key sequence [9] [0] [0] [A] (or [B]) will put the DT1000 back into the Power Up Mode. Refer to mode (1.) explained in the earlier section of this data sheet for all operations covered by this mode.

Functional Description (Continued)

GENERAL COMMENTS

1. The DT1000 is always in one of the modes. To exit a mode, simply key in the control code of the next desired mode.
2. "SS" (located at address 129) can make singular words plural.
3. "Centi", "milli", "re" are prefixes to make words like "centimeter", "reset", etc. Some prefixes do not blend well directly with some words such as "milli ampere". In these cases, insert an appropriate amount of silence between the words.
4. High output volume can be obtained by supplying 11V to power supply input (pin 50).

SPEECH QUALITY

The actual speech quality of the DT1000 is affected by many factors. Certainly the quality is affected most significantly by the actual speaker and baffle chosen to output the final speech data. Although the DT1000 will drive most any size of "common" PM speakers, care ought to be made in the actual selection of the speaker, AND its respective baffle or enclosure. An unbaffled speaker will not give a true response, small speakers typically do not reproduce low frequencies. Truly, the most desirable combination for best quality would be a medium size speaker 6 inches to 12 inches in diameter, and housed in a solid wood enclosed baffle.

One can actually "experiment" with the quality by trying various speaker and baffle combinations.

APPLICATION WITH EXTERNAL PROCESSOR

The DT1000 is designed so that it is possible to access only the DIGITALKER portion of the board. *Important: it is necessary to remove the COP402 from the DT1000 in this mode.* The DIGITALKER portion is defined as the speech processor chip (SPC) and the speech ROM(s) which contain the actual vocabulary (see Table I). The inputs required to connect the DIGITALKER (and the vocabulary of the DT1000 board) to an external processor have been made available on the pin edge connector (refer to Figure 3).

The following describes the function of all speech processor chip (SPC) inputs and outputs, and all other inputs and outputs required for operation in this external processor mode. Note: in the following descriptions and Table I, a low represents a logic zero (0.4V nominal) and a high represents a logic one (2.4V nominal).

CONNECTION REQUIREMENTS FOR EXTERNAL PROCESSOR APPLICATIONS

Edge Connector Pin Number	Function
8	**Chip Select ($\overline{CS}$).** The SPC is selected when $\overline{CS}$ is low. It is only necessary to have $\overline{CS}$ low during a command to the SPC. It is not necessary to hold $\overline{CS}$ low for the duration of the speech data.
	Data Bus (SW1–SW8). This is an 8-bit parallel binary data bus which accepts the binary address of the desired word. The binary addresses are available from Table I and are the same as the decimal address from the word list. Unused inputs must be connected to ground when used with external logic.
3	SW1 (LSB)
43	SW2
45	SW3
40	SW4
13	SW5
9	SW6
16	SW7
11	SW8 (MSB)
34	**Command Select (CMS).** This line is used to specify the two commands to the SPC.
37	**Write Strobe ($\overline{WR}$).** This line latches the starting address (A0–A7) into a register. On the rising edge of the $\overline{WR}$, the SPC starts execution of the command specified by CMS. The command sequence is shown in the timing waveform section. If a command to start a new speech sequence is issued during a speech sequence, the new speech sequence will be started immediately.
50	**Power Supply Voltage (V_{DD}).** Plus 7V to 11V maximum, direct current, to SPC, filter and amplifier sections. **Important!** V_{DD} *must* be regulated!
47	**Ground (V_{SS}).**
7	**Interrupt Output (INTR).** This signal goes high at the completion of any speech sequence. It is reset by the next valid command. It is also reset at power up.
10	**Speaker Output.** 4Ω–8Ω 1/2W at V_{DD}, 11.0V

CMS Command	Function
0	Reset interrupt and start speech sequence
1	Reset interrupt only

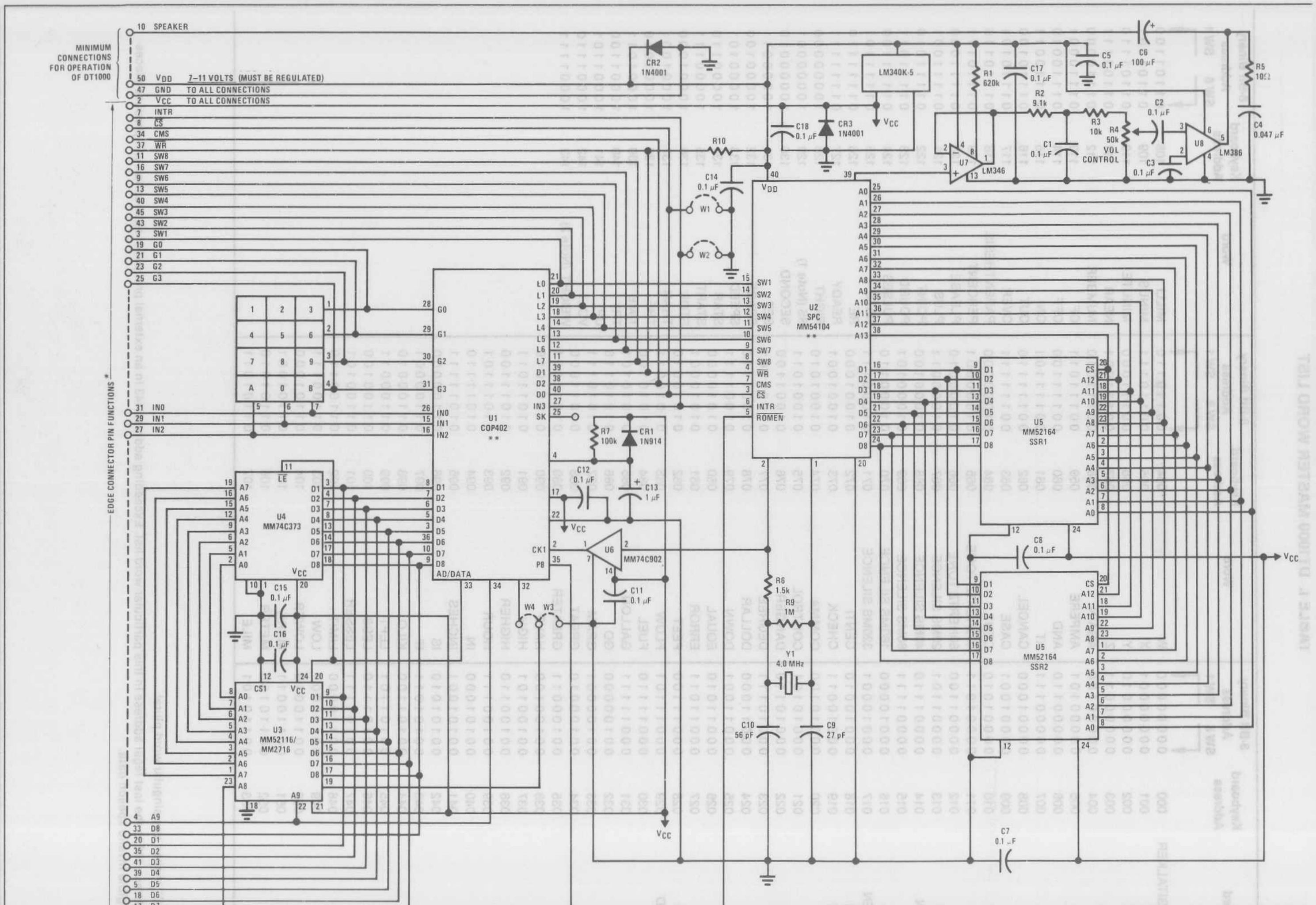
Functional Description (Continued)

TABLE I. DT1000 MASTER WORD LIST

Word	Keyboard Address	8-Bit Binary Address SW 8 SW 1	Word	Keyboard Address	8-Bit Binary Address SW 8 SW 1	Word	Keyboard Address	8-Bit Binary Address SW 8 SW 1
THIS IS DIGITALKER	000	00000000	W	054	00110110	MILLI	108	01101100
ONE	001	00000001	X	055	00110111	MINUS	109	01101101
TWO	002	00000010	Y	056	00111000	MINUTE	110	01101110
THREE	003	00000011	Z	057	00111001	NEAR	111	01101111
FOUR	004	00000100	AGAIN	058	00111010	NUMBER	112	01110000
FIVE	005	00000101	AMPERE	059	00111011	OF	113	01110001
SIX	006	00000110	AND	060	00111100	OFF	114	01110010
SEVEN	007	00000111	AT	061	00111101	ON	115	01110011
EIGHT	008	00001000	CANCEL	062	00111110	OUT	116	01110100
NINE	009	00001001	CASE	063	00111111	OVER	117	01110101
TEN	010	00001010	CENT	064	01000000	PARENTHESIS	118	01110110
ELEVEN	011	00001011	400HERTZ TONE	065	01000001	PERCENT	119	01110111
TWELVE	012	00001100	80HERTZ TONE	066	01000010	PLEASE	120	01111000
THIRTEEN	013	00001101	20MS SILENCE	067	01000011	PLUS	121	01111001
FOURTEEN	014	00001110	40MS SILENCE	068	01000100	POINT	122	01111010
FIFTEEN	015	00001111	80MS SILENCE	069	01000101	POUND	123	01111011
SIXTEEN	016	00010000	160MS SILENCE	070	01000110	PULSES	124	01111100
SEVENTEEN	017	00010001	320MS SILENCE	071	01000111	RATE	125	01111101
EIGHTEEN	018	00010010	CENTI	072	01001000	RE	126	01111110
NINETEEN	019	00010011	CHECK	073	01001001	READY	127	01111111
TWENTY	020	00010100	COMMA	074	01001010	RIGHT	128	10000000
THIRTY	021	00010101	CONTROL	075	01001011	SS (Note 1)	129	10000001
FORTY	022	00010110	DANGER	076	01001100	SECOND	130	10000010
FIFTY	023	00010111	DEGREE	077	01001101	SET	131	10000011
SIXTY	024	00011000	DOLLAR	078	01001110	SPACE	132	10000100
SEVENTY	025	00011001	DOWN	079	01001111	SPEED	133	10000101
EIGHTY	026	00011010	EQUAL	080	01010000	STAR	134	10000110
NINETY	027	00011011	ERROR	081	01010001	START	135	10000111
HUNDRED	028	00011100	FEET	082	01010010	STOP	136	10001000
THOUSAND	029	00011101	FLOW	083	01010011	THAN	137	10001001
MILLION	030	00011110	FUEL	084	01010100	THE	138	10001010
ZERO	031	00011111	GALLON	085	01010101	TIME	139	10001011
A	032	00100000	GO	086	01010110	TRY	140	10001100
B	033	00100001	GRAM	087	01010111	UP	141	10001101
C	034	00100010	GREAT	088	01011000	VOLT	142	10001110
D	035	00100011	GREATER	089	01011001	WEIGHT (Note 2)	143	10001111
E	036	00100100	HAVE	090	01011010			
F	037	00100101	HIGH	091	01011011			
G	038	00100110	HIGHER	092	01011100			
H	039	00100111	HOUR	093	01011101			
I	040	00101000	IN	094	01011110			
J	041	00101001	INCHES	095	01011111			
K	042	00101010	IS	096	01100000			
L	043	00101011	IT	097	01100001			
M	044	00101100	KILO	098	01100010			
N	045	00101101	LEFT	099	01100011			
O	046	00101110	LESS	100	01100100			
P	047	00101111	LESSER	101	01100101			
Q	048	00110000	LIMIT	102	01100110			
R	049	00110001	LOW	103	01100111			
S	050	00110010	LOWER	104	01101000			
T	051	00110011	MARK	105	01101001			
U	052	00110100	METER	106	01101010			
V	053	00110101	MILE	107	01101011			

Note 1: "SS" makes any singular word plural.

Note 2: Address 143 is the last legal address in this particular word list. Exceeding address 143 in an external processor application will produce pieces of unintelligible invalid speech data.



* Even numbered edge connector pins are the top side of the DT1000 board, odd numbered pi bottom side. 50-pin edge connector part number: 3M Company #3415.

** The COP402 device must be removed from the socket for external processor applications.

FIGURE 1. DT1000 DIGITALKER™ Evaluation Board Circuit Diagram

AC Electrical Characteristics

(For Use in External Processor Application) $T_A = 0°C$ to $70°C$, $V_{DD} = 7V–11V$, $V_{SS} = 0V$, unless otherwise specified.

Symbol	Parameter	Min	Max	Units
t_{aw}	CMS Valid to Write Strobe	350		ns
t_{csw}	Chip Select ON to Write Strobe	310		ns
t_{dw}	Data Bus Valid to Write Strobe	50		ns
t_{wa}	CMS Hold Time after Write Strobe	50		ns
t_{wd}	Data Bus Hold Time after Write Strobe	100		ns
t_{ww}	Write Strobe Width (50% Point)	430		ns
t_{wss}	Write Strobe to Speech Output Delay		410	μs

Note: Rise and fall times (10% to 90%) of MICROBUS™ signals should be 50 ns maximum.

Timing Waveforms (Required in external processor applications)

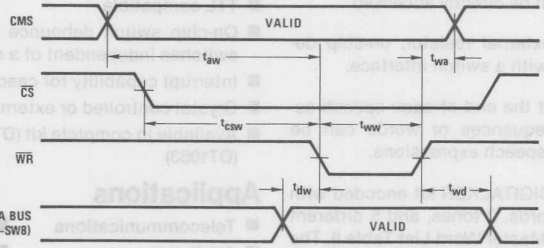
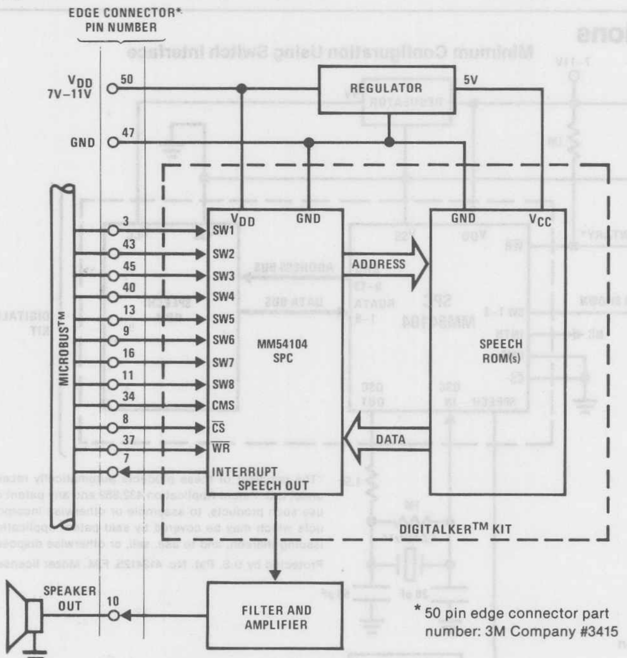


FIGURE 2. Command Sequence

Typical Application



* 50 pin edge connector part number: 3M Company #3415

Note: COP402 must be removed from DT1000 in this configuration.

FIGURE 3. DIGITALKER™ Connections to External MICROBUS™ Processor

National Semiconductor

DIGITALKER™ Speech Synthesis

DT1050/DT1053 DIGITALKER™ Standard Vocabulary Kit

General Description

The DIGITALKER™ is a speech synthesis system consisting of several N-channel MOS integrated circuits. It contains a speech processor chip (SPC) and speech ROM and when used with external filter, amplifier, and speaker, produces a system which generates high quality speech including the natural inflection and emphasis of the original speech. Male, female, and children's voices can be synthesized.

The SPC communicates with the speech ROM, which contains the compressed speech data as well as the frequency and amplitude data required for speech output. Up to 128k bits of speech data can be directly accessed.

With the addition of an external resistor, on-chip debounce is provided for use with a switch interface.

An interrupt is generated at the end of each speech sequence so that several sequences or words can be cascaded to form different speech expressions.

The DT1050 is a standard DIGITALKER kit encoded with 137 separate and useful words, 2 tones, and 5 different silence durations. (See the Master Word List Table I). The words and tones have been assigned discrete addresses, making it possible to output single words or words concatenated into phrases or even sentences.

The "voice" output of the DT1050 is a highly intelligible male voice. The vocabulary is chosen so that it is applicable to many products and markets.

Features

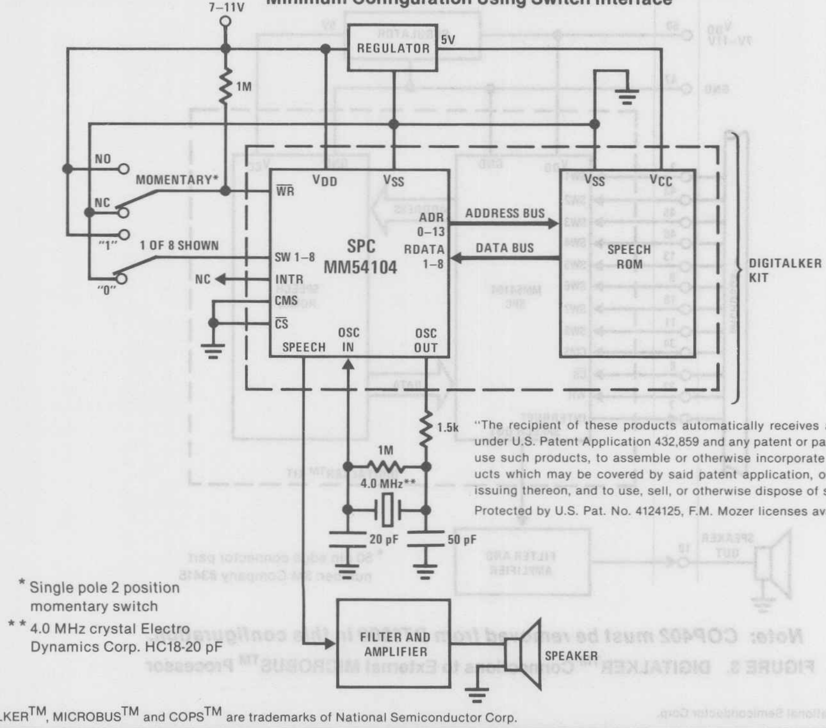
- COPS™ and MICROBUS™ compatible
- Designed to be easily interfaced to other popular microprocessors
- 144 addressable expressions, including numbers
- Natural inflection and emphasis of original speech
- Addresses 128k of ROM directly
- TTL compatible
- On-chip switch debounce for interfacing to manual switches independent of a microprocessor
- Interrupt capability for cascading words or phrases
- Crystal controlled or externally driven oscillator
- Available in complete kit (DT1050) or speech ROM only (DT1053)

Applications

- Telecommunications
- Appliance
- Automotive
- Teaching aids
- Consumer products
- Clocks
- Language translation
- Annunciators

Typical Applications

Minimum Configuration Using Switch Interface



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* Single pole 2 position momentary switch

** 4.0 MHz crystal Electro Dynamics Corp. HC18-20 pF

Absolute Maximum Ratings*

Storage Temperature Range	−65°C to +150°C	Voltage at Any Pin	12V
Operating Temperature Range	0°C to 70°C	Operating Voltage Range, V_{DD}-V_{SS}	7V to 11V
V_{DD}-V_{SS}	12V	Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics* $T_A = 0°C$ to $70°C$, $V_{DD} = 7V–11V$, $V_{SS} = 0V$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Voltage		−0.3		0.8	V
V_{IH}	Input High Voltage		2.0		V_{DD}	V
V_{OL}	Output Low Voltage	$I_{OL} = 1.6$ mA			0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -100\ \mu A$	2.4		5.0	V
V_{ILX}	Clock Input Low Voltage		−0.3		1.2	V
V_{IHX}	Clock Input High Voltage		5.5		V_{DD}	V
I_{DD}	Power Supply Current				45	mA
I_{IL}	Input Leakage				±10	μA
I_{ILX}	Clock Input Leakage				±10	μA
V_S	Silence Voltage			$0.45\,V_{DD}$		V
V_{OUT}	Peak to Peak Speech Output	$V_{DD} = 11V$		2.0		V
R_{EXT}	External Load on Speech Output	R_{EXT} Connected Between Speech Output and V_{SS}	50			kΩ

AC Electrical Characteristics* $T_A = 0°C$ to $70°C$, $V_{DD} = 7V–11V$, $V_{SS} = 0V$, unless otherwise specified.

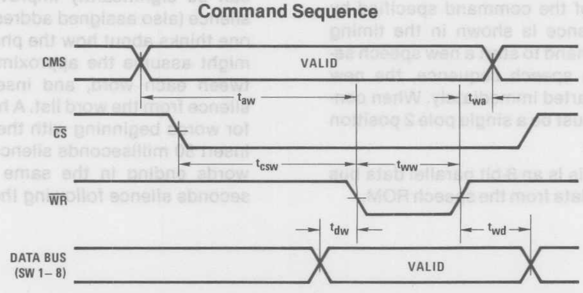
Symbol	Parameter	Min	Max	Units
t_{aw}	CMS Valid to Write Strobe	350		ns
t_{csw}	Chip Select ON to Write Strobe	310		ns
t_{dw}	Data Bus Valid to Write Strobe	50		ns
t_{wa}	CMS Hold Time after Write Strobe	50		ns
t_{wd}	Data Bus Hold Time after Write Strobe	100		ns
t_{ww}	Write Strobe Width (50% Point)	430		ns
t_{red}	ROMEN ON to Valid ROM Data		2	μs
t_{wss}	Write Strobe to Speech Output Delay		410	μs
f_t	External Clock Frequency	3.92	4.08	MHz

Note: Rise and fall times (10% to 90%) of MICROBUS signals should be 50 ns maximum.

*SPC characteristics only. ROM characteristics covered by separate data sheet for MM52164.

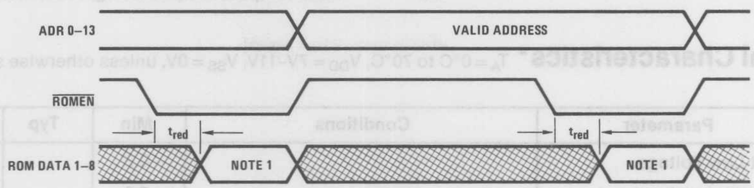
Timing Waveforms

Command Sequence



Timing Waveforms (Continued)

ROM Data Timing



Note 1: ROM Data 1-8 can go valid any time after ADR 0-13 changes, however it must be valid within the t_{red} spec and remain valid until $\overline{ROMEN}$ goes high.

Functional Description

The following describes the function of all SPC input and output pins.

Note: In the following descriptions, a low represents a logic 0 (0.4V nominal), and a high represents a logic 1 (2.4V nominal).

INPUT SIGNALS

Chip Select ($\overline{CS}$): The SPC is selected when $\overline{CS}$ is low. It is only necessary to have $\overline{CS}$ low during a command to the SPC. It is not necessary to hold $\overline{CS}$ low for the duration of the speech data.

Data Bus (SW 1-8): This is an 8-bit parallel data bus which contains the starting address of the speech data.

Data bus inputs SW 1–SW 8 accept an 8-bit binary address which is the address of the word which is to be "spoken" from the DIGITALKER output. See the Master Word List (Table I) for the complete listing of words and their respective addresses. If the entire word list is not used, unused inputs must be connected to V_{SS}.

Command Select (CMS): This line specifies the two commands to the SPC.

CMS	Function
0	Reset interrupt and start speech sequence
1	Reset interrupt only

Write Strobe ($\overline{WR}$): This line latches the starting address (SW 1–SW 8) into a register. On the rising edge of the $\overline{WR}$, the SPC starts execution of the command specified by CMS. The command sequence is shown in the timing waveform section. If a command to start a new speech sequence is issued during a speech sequence, the new speech sequence will be started immediately. When connecting $\overline{WR}$ to a switch, it must be a single pole 2 position switch as shown on page 1.

ROM Data (RDATA 1-8): This is an 8-bit parallel data bus which contains the speech data from the speech ROM.

OUTPUT SIGNALS

Interrupt (INTR): This signal goes high at the completion of any speech sequence. It is reset by the next valid command. It is also reset at power up.

ROM Address (ADR 0–ADR 13): This is a 14-bit parallel bus that supplies the address of the speech data to the speech ROM.

ROM Enable ($\overline{ROMEN}$): For low power applications, this line can be used to drive a transistor that switches the supply for static speech ROMs. See ROM data timing.

Speech Output (Speech Out): This is the analog output that represents the speech data. See frequency response section.

INPUT/OUTPUT SIGNALS

Clock Input/Output (OSC IN, OSC OUT): These two pins connect the main timing reference (crystal) to the SPC.

PHRASE QUALITY

In normal human speech, the brain puts durations of silence between the words to make the sentence flow smoothly. Since several durations of silence are provided in the Master Word List, the actual quality of any phrase can be significantly improved by adding durations of silence (also assigned addresses) between the words. As one thinks about how the phrase is actually spoken, one might assume the approximate duration of silence between each word, and insert the closest duration of silence from the word list. A hint in this area would be that for words beginning with the letters, K, T, P, B, D, and G insert 80 milliseconds silence prior to the words, and for words ending in the same letters as above, 40 milliseconds silence following the word is recommended.

Functional Description (Continued)

TABLE I. DT1050 MASTER WORD LIST*

Word	8-Bit Binary Address SW8 … SW1		8-Bit Binary Address SW8 … SW1		8-Bit Binary Address SW8 … SW1
THIS IS DIGITALKER	00000000	Q	00110000	IS	01100000
ONE	00000001	R	00110001	IT	01100001
TWO	00000010	S	00110010	KILO	01100010
THREE	00000011	T	00110011	LEFT	01100011
FOUR	00000100	U	00110100	LESS	01100100
FIVE	00000101	V	00110101	LESSER	01100101
SIX	00000110	W	00110110	LIMIT	01100110
SEVEN	00000111	X	00110111	LOW	01100111
EIGHT	00001000	Y	00111000	LOWER	01101000
NINE	00001001	Z	00111001	MARK	01101001
TEN	00001010	AGAIN	00111010	METER	01101010
ELEVEN	00001011	AMPERE	00111011	MILE	01101011
TWELVE	00001100	AND	00111100	MILLI	01101100
THIRTEEN	00001101	AT	00111101	MINUS	01101101
FOURTEEN	00001110	CANCEL	00111110	MINUTE	01101110
FIFTEEN	00001111	CASE	00111111	NEAR	01101111
SIXTEEN	00010000	CENT	01000000	NUMBER	01110000
SEVENTEEN	00010001	400HERTZ TONE	01000001	OF	01110001
EIGHTEEN	00010010	80HERTZ TONE	01000010	OFF	01110010
NINETEEN	00010011	20MS SILENCE	01000011	ON	01110011
TWENTY	00010100	40MS SILENCE	01000100	OUT	01110100
THIRTY	00010101	80MS SILENCE	01000101	OVER	01110101
FORTY	00010110	160MS SILENCE	01000110	PARENTHESIS	01110110
FIFTY	00010111	320MS SILENCE	01000111	PERCENT	01110111
SIXTY	00011000	CENTI	01001000	PLEASE	01111000
SEVENTY	00011001	CHECK	01001001	PLUS	01111001
EIGHTY	00011010	COMMA	01001010	POINT	01111010
NINETY	00011011	CONTROL	01001011	POUND	01111011
HUNDRED	00011100	DANGER	01001100	PULSES	01111100
THOUSAND	00011101	DEGREE	01001101	RATE	01111101
MILLION	00011110	DOLLAR	01001110	RE	01111110
ZERO	00011111	DOWN	01001111	READY	01111111
A	00100000	EQUAL	01010000	RIGHT	10000000
B	00100001	ERROR	01010001	SS (Note 1)	10000001
C	00100010	FEET	01010010	SECOND	10000010
D	00100011	FLOW	01010011	SET	10000011
E	00100100	FUEL	01010100	SPACE	10000100
F	00100101	GALLON	01010101	SPEED	10000101
G	00100110	GO	01010110	STAR	10000110
H	00100111	GRAM	01010111	START	10000111
I	00101000	GREAT	01011000	STOP	10001000
J	00101001	GREATER	01011001	THAN	10001001
K	00101010	HAVE	01011010	THE	10001010
L	00101011	HIGH	01011011	TIME	10001011
M	00101100	HIGHER	01011100	TRY	10001100
N	00101101	HOUR	01011101	UP	10001101
O	00101110	IN	01011110	VOLT	10001110
P	00101111	INCHES	01011111	WEIGHT (Note 2)	10001111

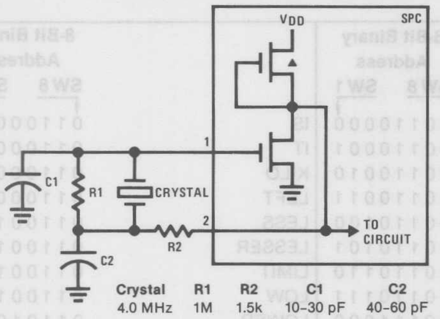
* DT1050 is a complete kit including MM54104 SPC; DT1053 is SSR1 and SSR2 speech ROMs only.

Note 1: "SS" makes any singular word plural

Note 2: Address 143 is the last legal address in this particular word list. Exceeding address 143 will produce pieces of unintelligible invalid speech data.

Crystal Circuit Information

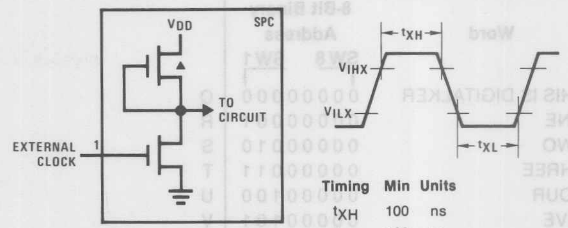
Typical Crystal Oscillator Network



Crystal	R1	R2	C1	C2
4.0 MHz	1M	1.5k	10–30 pF	40–60 pF

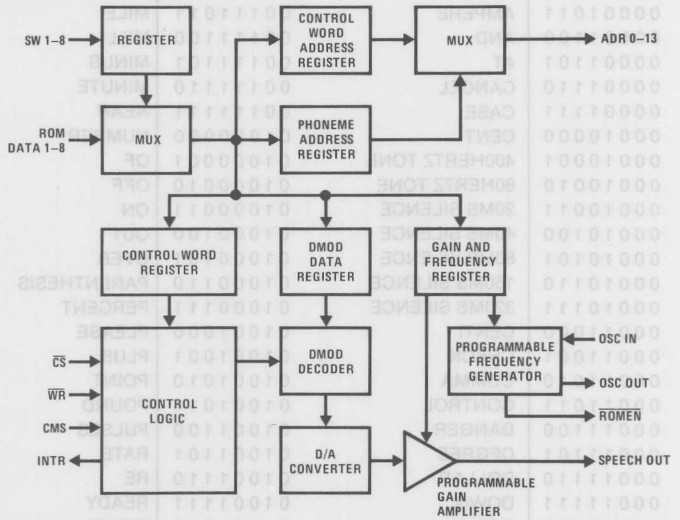
(4.0 MHz crystal manufactured by Electro Dynamics Corp. P/N HC18-20 pF)

External Clock Input (4.0 MHz)

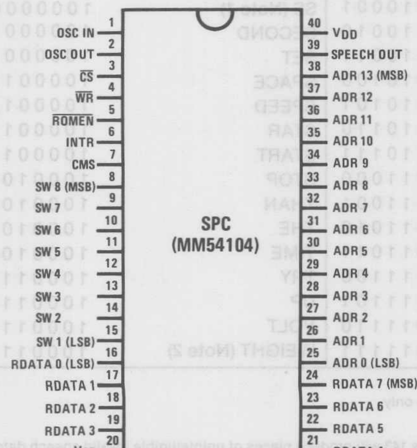


Timing	Min	Units
t_{XH}	100	ns
t_{XL}	100	ns

SPC Block and Connection Diagrams

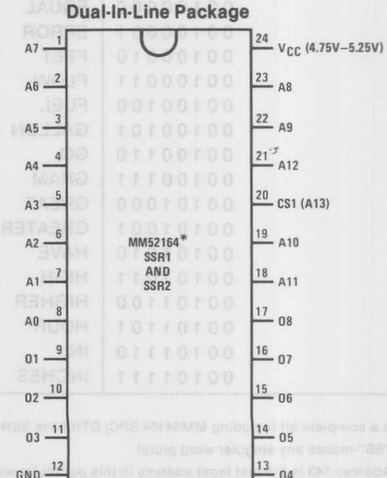


Dual-In-Line Package



TOP VIEW

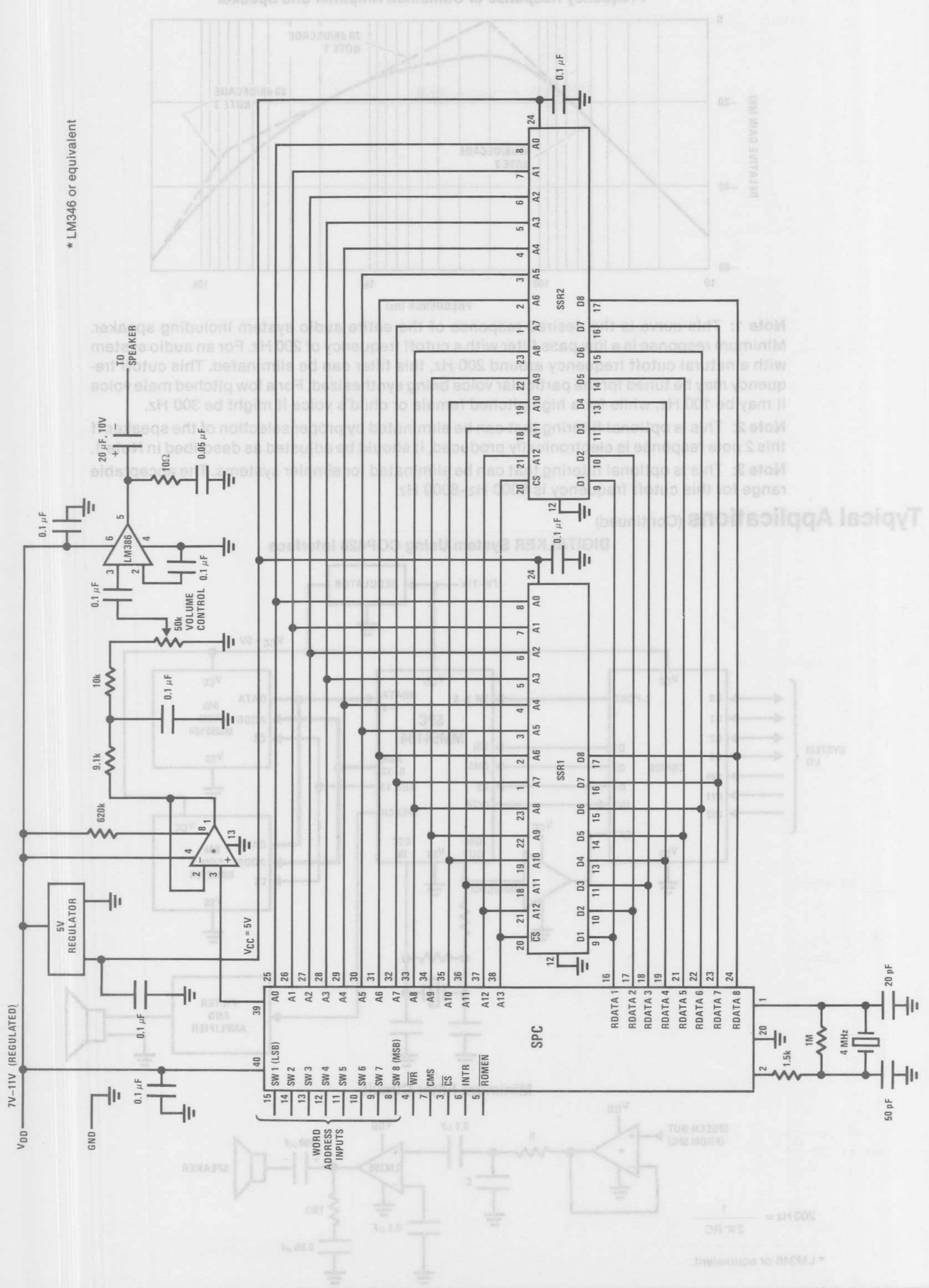
Dual-In-Line Package



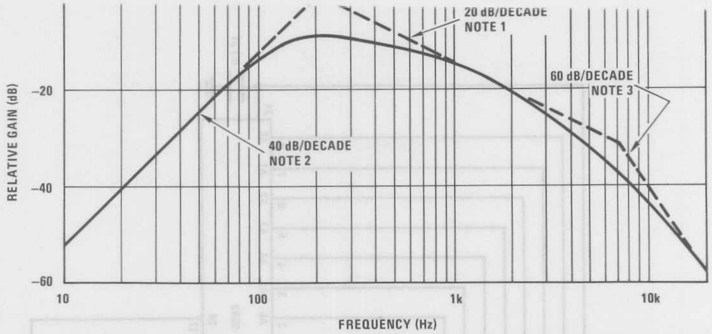
TOP VIEW

* For specific ROM device information, see MM52164 data sheet.

Recommended Schematic Diagram



* LM346 or equivalent



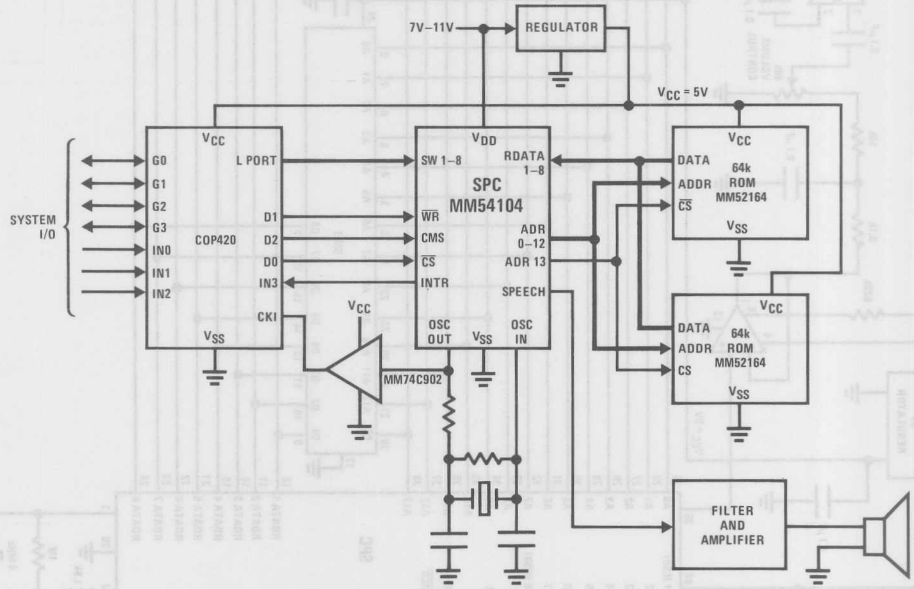
Note 1: This curve is the desired response of the entire audio system including speaker. Minimum response is a low pass filter with a cutoff frequency of 200 Hz. For an audio system with a natural cutoff frequency around 200 Hz, this filter can be eliminated. This cutoff frequency may be tuned for the particular voice being synthesized. For a low pitched male voice it may be 100 Hz, while for a high pitched female or child's voice it might be 300 Hz.

Note 2: This is optional filtering that can be eliminated by proper selection of the speaker. If this 2 pole response is electronically produced, it should be adjusted as described in Note 1.

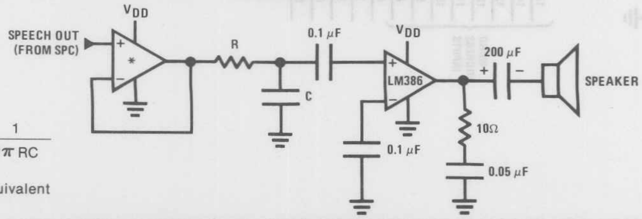
Note 3: This is optional filtering that can be eliminated for simpler systems. The acceptable range for this cutoff frequency is 6000 Hz–8000 Hz.

Typical Applications (Continued)

DIGITALKER System Using COP420 Interface



Minimum Filter Circuit

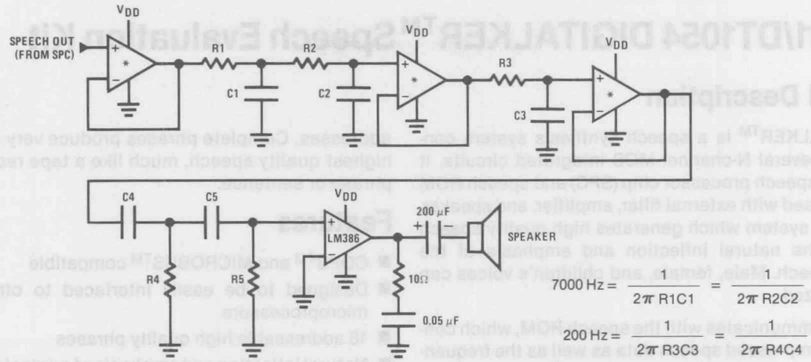


$$200\ \text{Hz} = \frac{1}{2\pi RC}$$

* LM346 or equivalent

Typical Applications (Continued)

Filter Circuit to Produce Maximum Frequency Response

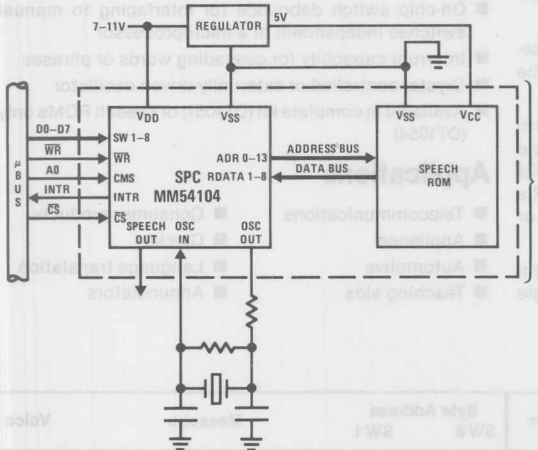


$$7000\ \text{Hz} = \frac{1}{2\pi\ R1C1} = \frac{1}{2\pi\ R2C2}$$

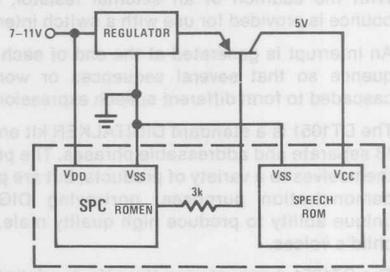
$$200\ \text{Hz} = \frac{1}{2\pi\ R3C3} = \frac{1}{2\pi\ R4C4} = \frac{1}{2\pi\ R5C5}$$

*LM346 or equivalent

DIGITALKER System Utilizing MICROBUS™ Interface



Low Power Configuration Using Static ROM



National Semiconductor

DT1051/DT1054 DIGITALKER™ Speech Evaluation Kit

General Description

The DIGITALKER™ is a speech synthesis system consisting of several N-channel MOS integrated circuits. It contains a speech processor chip (SPC) and speech ROM and when used with external filter, amplifier, and speaker, produces a system which generates high quality speech including the natural inflection and emphasis of the original speech. Male, female, and children's voices can be synthesized.

The SPC communicates with the speech ROM, which contains the compressed speech data as well as the frequency and amplitude data required for speech output. Up to 128k bits of speech data can be directly accessed.

With the addition of an external resistor, on-chip debounce is provided for use with a switch interface.

An interrupt is generated at the end of each speech sequence so that several sequences or words can be cascaded to form different speech expressions.

The DT1051 is a standard DIGITALKER kit encoded with 18 separate and addressable phrases. The phrases lend themselves to a variety of products, but are primarily for demonstration purposes, portraying DIGITALKER's unique ability to produce high quality male, female, or child's voices.

The DT1051 demonstrates the effects of digitizing complete phrases as opposed to individual words at single addresses. Complete phrases produce very natural and highest quality speech, much like a tape recording of a phrase or sentence.

Features

- COPS™ and MICROBUS™ compatible
- Designed to be easily interfaced to other popular microprocessors
- 18 addressable high quality phrases
- Natural inflection and emphasis of original speech
- Addresses 128k of ROM directly
- TTL compatible
- On-chip switch debounce for interfacing to manual switches independent of a microprocessor
- Interrupt capability for cascading words or phrases
- Crystal controlled or externally driven oscillator
- Available in complete kit (DT1051) or speech ROMs only (DT1054)

Applications

- Telecommunications
- Appliance
- Automotive
- Teaching aids
- Consumer products
- Clocks
- Language translation
- Annunciators

DT1051 Vocabulary*

Byte Address SW 8 … SW 1	Message	Voice	Byte Address SW 8 … SW 1	Message	Voice
00000000	BASSON MUSIC	N/A	00001001	CHECK OIL LEVEL	MALE
00000001	THIS IS NS DIGITALKER	FEMALE	00001010	CHECK COOLANT LEVEL	MALE
00000010	THE TIME IS 8:43 PM	FEMALE	00001011	CHECK FUEL LEVEL	MALE
00000011	EMERGENCY, CALL 911	FEMALE	00001100	DOOR OPEN	MALE
00000100	SELECT TEMPERATURE	FEMALE	00001101	DEFROST	MALE
00000101	SELECT COOKING TIME	FEMALE	00001110	GOING UP	MALE
00000110	THE NUMBER YOU REACHED HAS BEEN CHANGED, PLEASE CALL 408 737-5000	MALE	00001111	FIRST FLOOR	MALE
00000111	WARNING THE BRAKE FLUID IS LOW	MALE	00010000	PLEASE CALL YOUR OFFICE	MALE
00001000	PLEASE FASTEN YOUR SEATBELT	MALE	00010001	I'M CUTE, AREN'T I?	CHILD
				END OF VOCABULARY	

* DT1051 is a complete kit including MM54104 SPC; DT1054 is SSR3 and SSR4 speech ROMs only.

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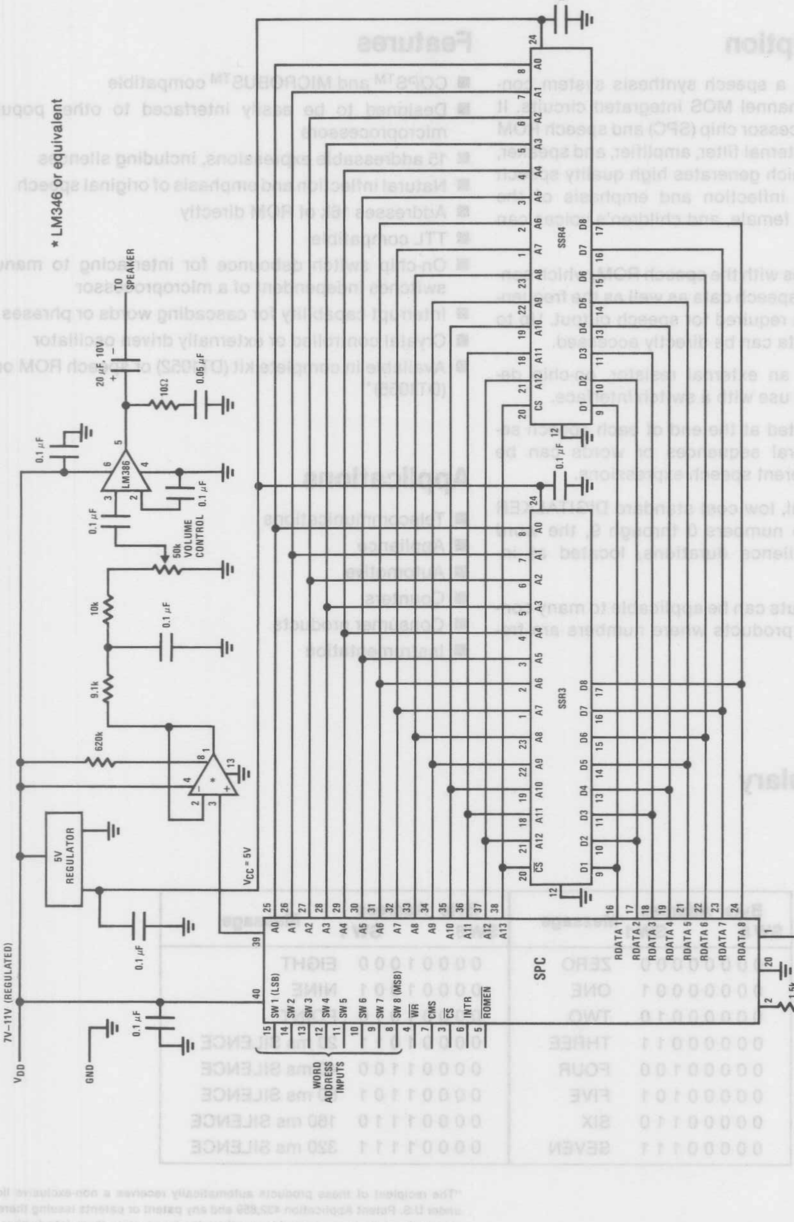
Protected by U.S. Pat. No. 4124125, F.M. Mozer licenses available.

Recommended Schematic Diagram



Refer to MM54104 data sheet for complete specifications on electrical and timing characteristics.

National Semiconductor

DIGITALKER™ Speech Synthesis

DT1052/DT1055 DIGITALKER™ Basic Numbers Kit

General Description

The DIGITALKER™ is a speech synthesis system consisting of several N-channel MOS integrated circuits. It contains a speech processor chip (SPC) and speech ROM and when used with external filter, amplifier, and speaker, produces a system which generates high quality speech including the natural inflection and emphasis of the original speech. Male, female, and children's voices can be synthesized.

The SPC communicates with the speech ROM, which contains the compressed speech data as well as the frequency and amplitude data required for speech output. Up to 128k bits of speech data can be directly accessed.

With the addition of an external resistor, on-chip debounce is provided for use with a switch interface.

An interrupt is generated at the end of each speech sequence so that several sequences or words can be cascaded to form different speech expressions.

The DT1052 is a useful, low cost standard DIGITALKER kit, encoded with the numbers 0 through 9, the word point, and several silence durations, located at individual addresses.

These numerical outputs can be applicable to many consumer and industrial products where numbers are frequently displayed.

Features

- COPS™ and MICROBUS™ compatible
- Designed to be easily interfaced to other popular microprocessors
- 15 addressable expressions, including silences
- Natural inflection and emphasis of original speech
- Addresses 16k of ROM directly
- TTL compatible
- On-chip switch debounce for interfacing to manual switches independent of a microprocessor
- Interrupt capability for cascading words or phrases
- Crystal controlled or externally driven oscillator
- Available in complete kit (DT1052) or speech ROM only (DT1055)*

Applications

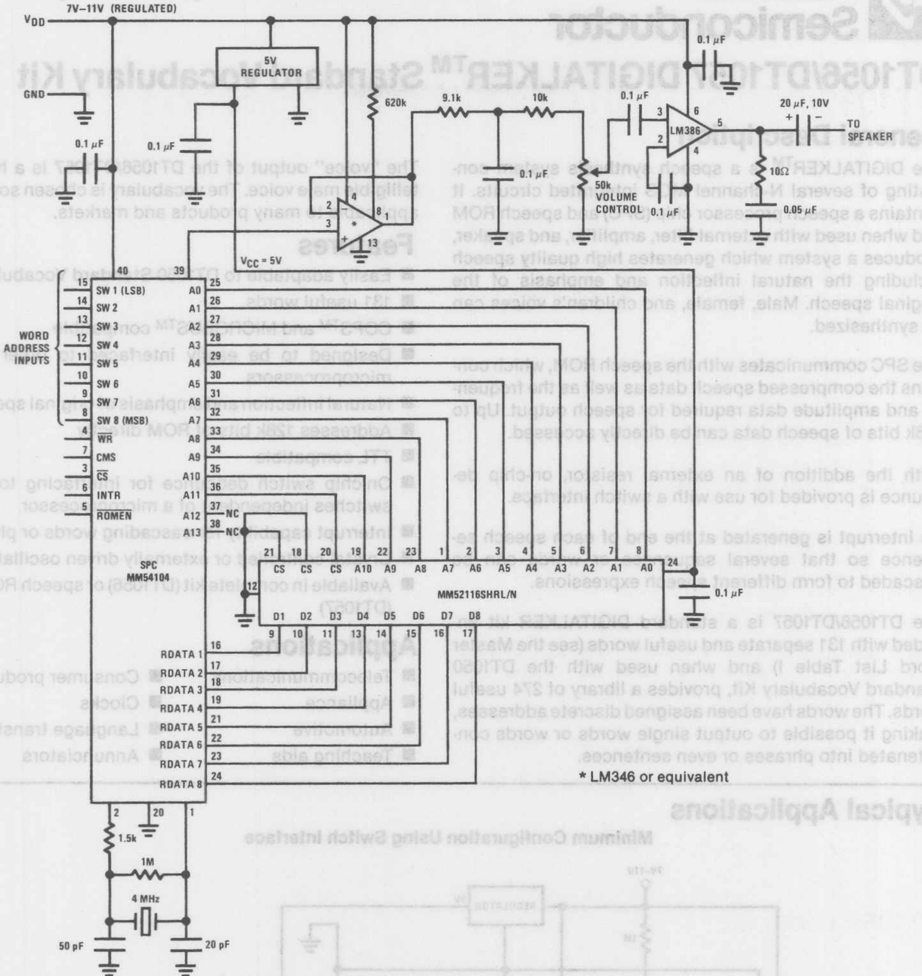
- Telecommunications
- Appliance
- Automotive
- Counters
- Consumer products
- Instrumentation

DT1052 Vocabulary

Byte Address SW 8 … SW 1	Message	Byte Address SW 8 … SW 1	Message
0 0 0 0 0 0 0 0	ZERO	0 0 0 0 1 0 0 0	EIGHT
0 0 0 0 0 0 0 1	ONE	0 0 0 0 1 0 0 1	NINE
0 0 0 0 0 0 1 0	TWO	0 0 0 0 1 0 1 0	POINT
0 0 0 0 0 0 1 1	THREE	0 0 0 0 1 0 1 1	20 ms SILENCE
0 0 0 0 0 1 0 0	FOUR	0 0 0 0 1 1 0 0	40 ms SILENCE
0 0 0 0 0 1 0 1	FIVE	0 0 0 0 1 1 0 1	80 ms SILENCE
0 0 0 0 0 1 1 0	SIX	0 0 0 0 1 1 1 0	160 ms SILENCE
0 0 0 0 0 1 1 1	SEVEN	0 0 0 0 1 1 1 1	320 ms SILENCE

* DT1052 is a complete kit including MM54104 SPC; DT1055 is MM52116SHRL speech ROM only.

Recommended Schematic Diagram



* LM346 or equivalent

Refer to MM54104 and MM52116 data sheets for complete specifications on electrical and timing characteristics.

National Semiconductor

DIGITALKER™ Speech Synthesis

DT1056/DT1057 DIGITALKER™ Standard Vocabulary Kit

General Description

The DIGITALKER™ is a speech synthesis system consisting of several N-channel MOS integrated circuits. It contains a speech processor chip (SPC) and speech ROM and when used with external filter, amplifier, and speaker, produces a system which generates high quality speech including the natural inflection and emphasis of the original speech. Male, female, and children's voices can be synthesized.

The SPC communicates with the speech ROM, which contains the compressed speech data as well as the frequency and amplitude data required for speech output. Up to 128k bits of speech data can be directly accessed.

With the addition of an external resistor, on-chip debounce is provided for use with a switch interface.

An interrupt is generated at the end of each speech sequence so that several sequences or words can be cascaded to form different speech expressions.

The DT1056/DT1057 is a standard DIGITALKER kit encoded with 131 separate and useful words (see the Master Word List Table I) and when used with the DT1050 Standard Vocabulary Kit, provides a library of 274 useful words. The words have been assigned discrete addresses, making it possible to output single words or words concatenated into phrases or even sentences.

The "voice" output of the DT1056/DT1057 is a highly intelligible male voice. The vocabulary is chosen so that it is applicable to many products and markets.

Features

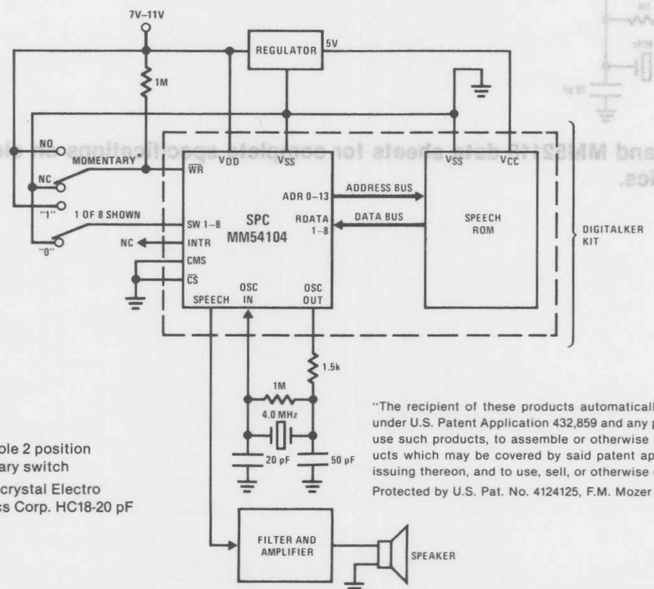
- Easily adaptable to DT1050 Standard Vocabulary Kit
- 131 useful words
- COPS™ and MICROBUS™ compatible
- Designed to be easily interfaced to other popular microprocessors
- Natural inflection and emphasis of original speech
- Addresses 128k bits of ROM directly
- TTL compatible
- On-chip switch debounce for interfacing to manual switches independent of a microprocessor
- Interrupt capability for cascading words or phrases
- Crystal controlled or externally driven oscillator
- Available in complete kit (DT1056) or speech ROMs only (DT1057)

Applications

- Telecommunications
- Appliance
- Automotive
- Teaching aids
- Consumer products
- Clocks
- Language translation
- Annunciators

Typical Applications

Minimum Configuration Using Switch Interface



*Single pole 2 position momentary switch

**4.0 MHz crystal Electro Dynamics Corp. HC18-20 pF

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Absolute Maximum Ratings*

Storage Temperature Range	− 65°C to + 150°C	Voltage at Any Pin	12V
Operating Temperature Range	0°C to 70°C	Operating Voltage Range, V_{DD}-V_{SS}	7V to 11V
V_{DD}-V_{SS}	12V	Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics* $T_A = 0°C$ to $70°C$, $V_{DD} = 7V$–$11V$, $V_{SS} = 0V$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Voltage		− 0.3		0.8	V
V_{IH}	Input High Voltage		2.0		V_{DD}	V
V_{OL}	Output Low Voltage	$I_{OL} = 1.6$ mA			0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -100\ \mu A$	2.4		5.0	V
V_{ILX}	Clock Input Low Voltage		− 0.3		1.2	V
V_{IHX}	Clock Input High Voltage		5.5		V_{DD}	V
I_{DD}	Power Supply Current				45	mA
I_{IL}	Input Leakage				± 10	μA
I_{ILX}	Clock Input Leakage				± 10	μA
V_S	Silence Voltage			0.45 V_{DD}		V
V_{OUT}	Peak to Peak Speech Output	$V_{DD} = 11V$		2.0		V
R_{EXT}	External Load on Speech Output	R_{EXT} Connected Between Speech Output and V_{SS}	50			kΩ

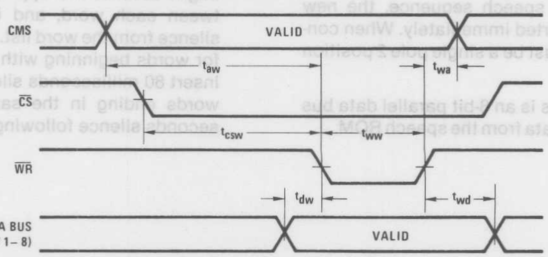
AC Electrical Characteristics* $T_A = 0°C$ to $70°C$, $V_{DD} = 7V$–$11V$, $V_{SS} = 0V$, unless otherwise specified.

Symbol	Parameter	Min	Max	Units
t_{aw}	CMS Valid to Write Strobe	350		ns
t_{csw}	Chip Select ON to Write Strobe	310		ns
t_{dw}	Data Bus Valid to Write Strobe	50		ns
t_{wa}	CMS Hold Time after Write Strobe	50		ns
t_{wd}	Data Bus Hold Time after Write Strobe	100		ns
t_{ww}	Write Strobe Width (50% Point)	430		ns
t_{red}	$\overline{\text{ROMEN}}$ ON to Valid ROM Data		2	μs
t_{wss}	Write Strobe to Speech Output Delay		410	μs
f_t	External Clock Frequency	3.92	4.08	MHz

Note: Rise and fall times (10% to 90%) of MICROBUS signals should be 50 ns maximum.
*SPC characteristics only. ROM characteristics covered by separate data sheet for MM52164.

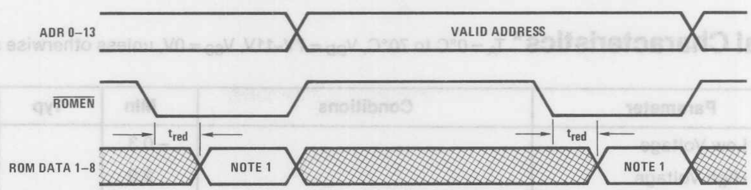
Timing Waveforms

Command Sequence



Timing Waveforms (Continued)

ROM Data Timing



Note 1: ROM Data 1-8 can go valid any time after ADR 0-13 changes, however it must be valid within the t_{red} spec and remain valid until $\overline{ROMEN}$ goes high.

Functional Description

The following describes the function of all SPC input and output pins.

Note: In the following descriptions, a low represents a logic 0 (0.4V nominal), and a high represents a logic 1 (2.4V nominal).

INPUT SIGNALS

Chip Select ($\overline{CS}$): The SPC is selected when $\overline{CS}$ is low. It is only necessary to have $\overline{CS}$ low during a command to the SPC. It is not necessary to hold $\overline{CS}$ low for the duration of the speech data.

Data Bus (SW 1-8): This is an 8-bit parallel data bus which contains the starting address of the speech data.

Data bus inputs SW 1–SW 8 accept an 8-bit binary address which is the address of the word which is to be "spoken" from the DIGITALKER output. See the Master Word List (Table I) for the complete listing of words and their respective addresses. If the entire word list is not used, unused inputs must be connected to V_{SS}.

Command Select (CMS): This line specifies the two commands to the SPC.

CMS	Function
0	Reset interrupt and start speech sequence
1	Reset interrupt only

Write Strobe ($\overline{WR}$): This line latches the starting address (SW 1–SW 8) into a register. On the rising edge of the $\overline{WR}$, the SPC starts execution of the command specified by CMS. The command sequence is shown in the timing waveform section. If a command to start a new speech sequence is issued during a speech sequence, the new speech sequence will be started immediately. When connecting $\overline{WR}$ to a switch, it must be a single pole 2 position switch as shown on page 1.

ROM Data (RDATA 1-8): This is an 8-bit parallel data bus which contains the speech data from the speech ROM.

OUTPUT SIGNALS

Interrupt (INTR): This signal goes high at the completion of any speech sequence. It is reset by the next valid command. It is also reset at power up.

ROM Address (ADR 0-ADR 13): This is a 14-bit parallel bus that supplies the address of the speech data to the speech ROM.

ROM Enable ($\overline{ROMEN}$): For low power applications, this line can be used to drive a transistor that switches the supply for static speech ROMs. See ROM Data Timing.

Speech Output (Speech Out): This is the analog output that represents the speech data. See frequency response section.

INPUT/OUTPUT SIGNALS

Clock Input/Output (OSC IN, OSC OUT): These two pins connect the main timing reference (crystal) to the SPC.

PHRASE QUALITY

In normal human speech, the brain puts durations of silence between the words to make the sentence flow smoothly. Since several durations of silence are provided in the Master Word List, the actual quality of any phrase can be significantly improved by adding durations of silence (also assigned addresses) between the words. As one thinks about how the phrase is actually spoken, one might assume the approximate duration of silence between each word, and insert the closest duration of silence from the word list. A hint in this area would be that for words beginning with the letters, K, T, P, B, D, and G insert 80 milliseconds silence prior to the words, and for words ending in the same letters as above, 40 milliseconds silence following the word is recommended.

Functional Description (Continued)

TABLE I. DT1056/DT1057* MASTER WORD LIST

Word	8-Bit Binary Address SW8 … SW1	Word	8-Bit Binary Address SW8 … SW1	Word	8-Bit Binary Address SW8 … SW1
ABORT	00000000	FARAD	00101100	PER	01011000
ADD	00000001	FAST	00101101	PICO	01011001
ADJUST	00000010	FASTER	00101110	PLACE	01011010
ALARM	00000011	FIFTH	00101111	PRESS	01011011
ALERT	00000100	FIRE	00110000	PRESSURE	01011100
ALL	00000101	FIRST	00110001	QUARTER	01011101
ASK	00000110	FLOOR	00110010	RANGE	01011110
ASSISTANCE	00000111	FORWARD	00110011	REACH	01011111
ATTENTION	00001000	FROM	00110100	RECEIVE	01100000
BRAKE	00001001	GAS	00110101	RECORD	01100001
BUTTON	00001010	GET	00110110	REPLACE	01100010
BUY	00001011	GOING	00110111	REVERSE	01100011
CALL	00001100	HALF	00111000	ROOM	01100100
CAUTION	00001101	HELLO	00111001	SAFE	01100101
CHANGE	00001110	HELP	00111010	SECURE	01100110
CIRCUIT	00001111	HERTZ	00111011	SELECT	01100111
CLEAR	00010000	HOLD	00111100	SEND	01101000
CLOSE	00010001	INCORRECT	00111101	SERVICE	01101001
COMPLETE	00010010	INCREASE	00111110	SIDE	01101010
CONNECT	00010011	INTRUDER	00111111	SLOW	01101011
CONTINUE	00010100	JUST	01000000	SLOWER	01101100
COPY	00010101	KEY	01000001	SMOKE	01101101
CORRECT	00010110	LEVEL	01000010	SOUTH	01101110
DATE	00010111	LOAD	01000011	STATION	01101111
DAY	00011000	LOCK	01000100	SWITCH	01110000
DECREASE	00011001	MEG	01000101	SYSTEM	01110001
DEPOSIT	00011010	MEGA	01000110	TEST	01110010
DIAL	00011011	MICRO	01000111	TH (NOTE 2)	01110011
DIVIDE	00011100	MORE	01001000	THANK	01110100
DOOR	00011101	MOVE	01001001	THIRD	01110101
EAST	00011110	NANO	01001010	THIS	01110110
ED (NOTE 1)	00011111	NEED	01001011	TOTAL	01110111
ED (NOTE 1)	00100000	NEXT	01001100	TURN	01111000
ED (NOTE 1)	00100001	NO	01001101	USE	01111001
ED (NOTE 1)	00100010	NORMAL	01001110	UTH (NOTE 3)	01111010
EMERGENCY	00100011	NORTH	01001111	WAITING	01111011
END	00100100	NOT	01010000	WARNING	01111100
ENTER	00100101	NOTICE	01010001	WATER	01111101
ENTRY	00100110	OHMS	01010010	WEST	01111110
ER	00100111	ONWARD	01010011	SWITCH	01111111
EVACUATE	00101000	OPEN	01010100	WINDOW	10000000
EXIT	00101001	OPERATOR	01010101	YES	10000001
FAIL	00101010	OR	01010110	ZONE	10000010
FAILURE	00101011	PASS	01010111		

*DT1056 is a complete kit including MM54104 SPC; DT1057 is SSR5 and SSR6 speech ROMs only.

Note 1: "ED" is a suffix that can be used to make any present tense word become a past tense word. The way we say "ED," however, does vary from one word to the next. For that reason, we have offered 4 different "ED" sounds. It is suggested that each "ED" be tested with the desired word for best quality results. Address 31 "ED" or 32 "ED" should be used with words ending in "T" or "D," such as exit or load. Address 34 "ED" should be used with words ending with soft sounds such as ask. Address 33 "ED" should be used with all other words.

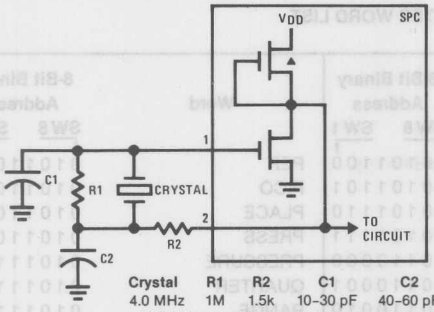
Note 2: "TH" is a suffix that can be added to words like six, seven, eight to form adjective words like sixth, seventh, eighth.

Note 3: "UTH" is a suffix that can be added to words like twenty, thirty, forty to form adjective words like thirtieth, fortieth, etc.

Note 4: Address 130 is the last legal address in this particular word list. Exceeding address 130 will produce pieces of unintelligible invalid speech data.

Crystal Circuit Information

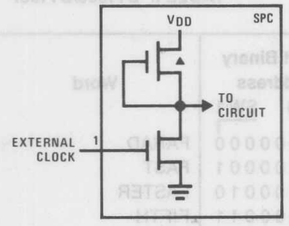
Typical Crystal Oscillator Network

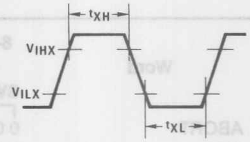


Crystal	R1	R2	C1	C2
4.0 MHz	1M	1.5k	10–30 pF	40–60 pF

(4.0 MHz crystal manufactured by Electro Dynamics Corp. P/N HC18-20 pF)

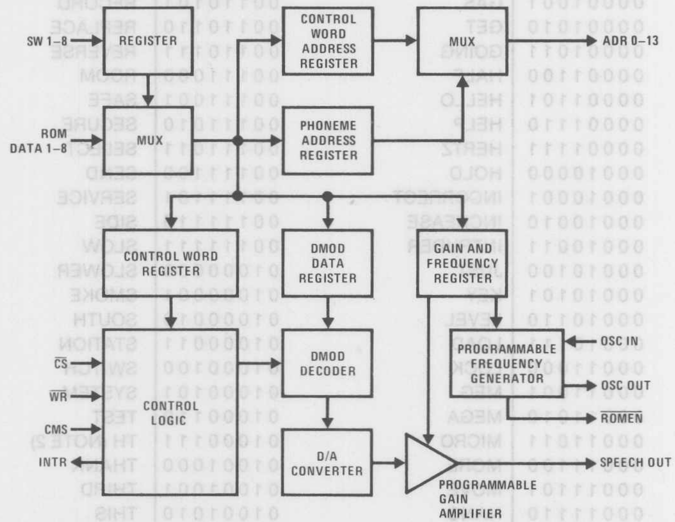
External Clock Input (4.0 MHz)



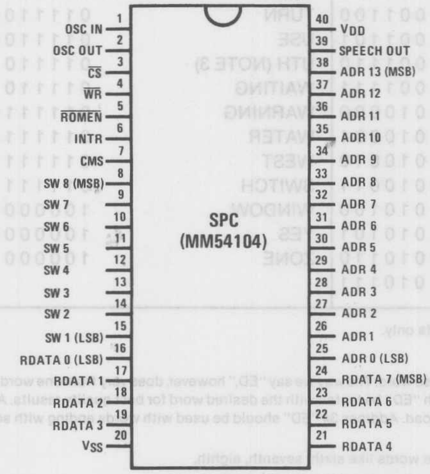


Timing	Min	Units
t_{XH}	100	ns
t_{XL}	100	ns

SPC Block and Connection Diagrams

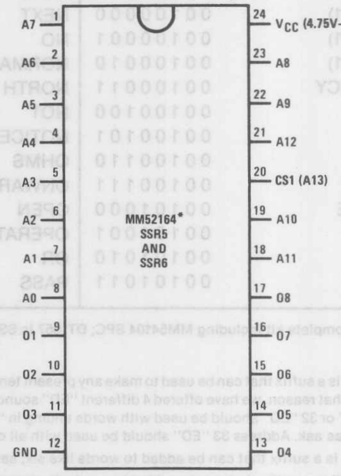


Dual-In-Line Package



TOP VIEW

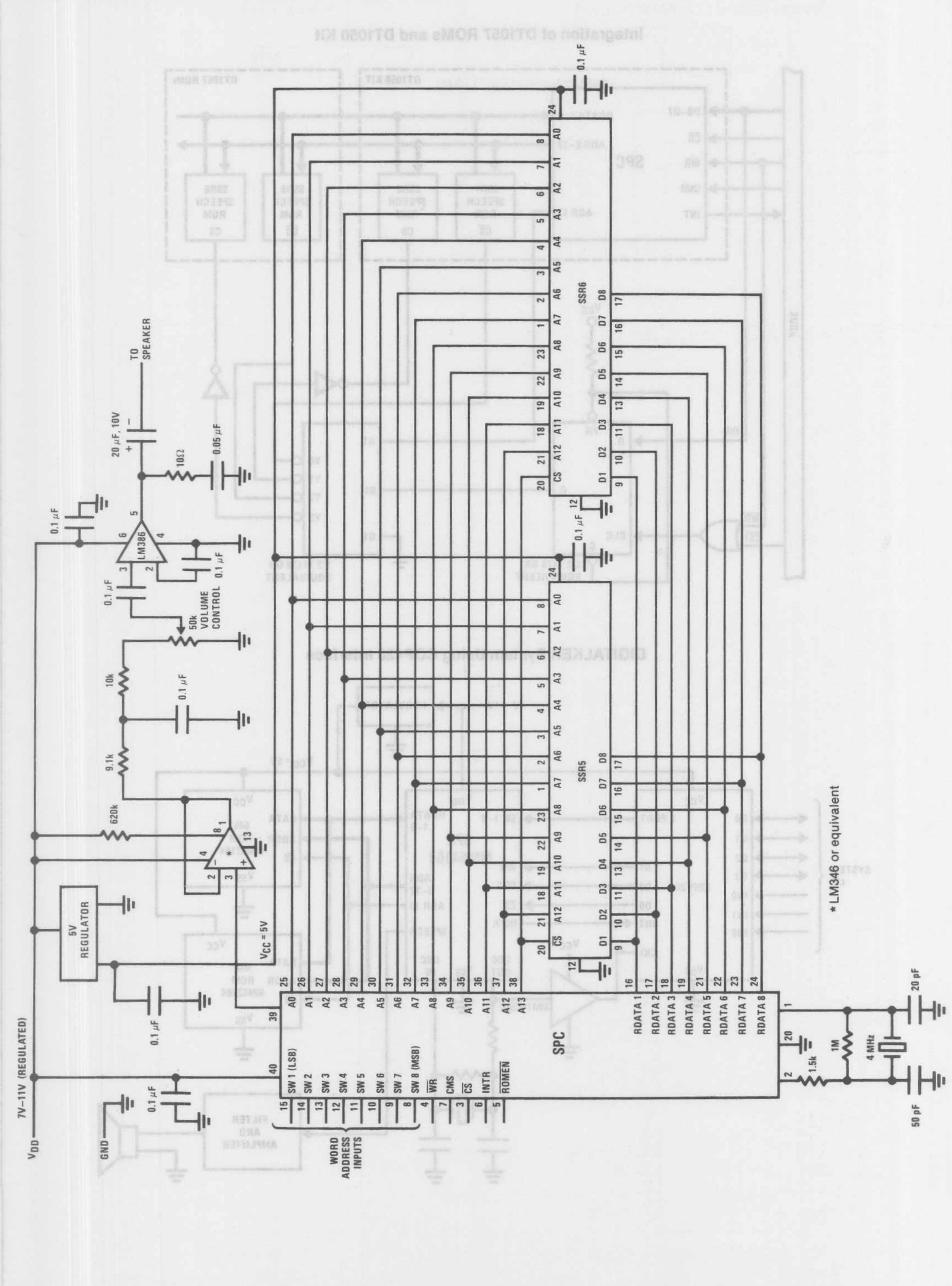
Dual-In-Line Package



TOP VIEW

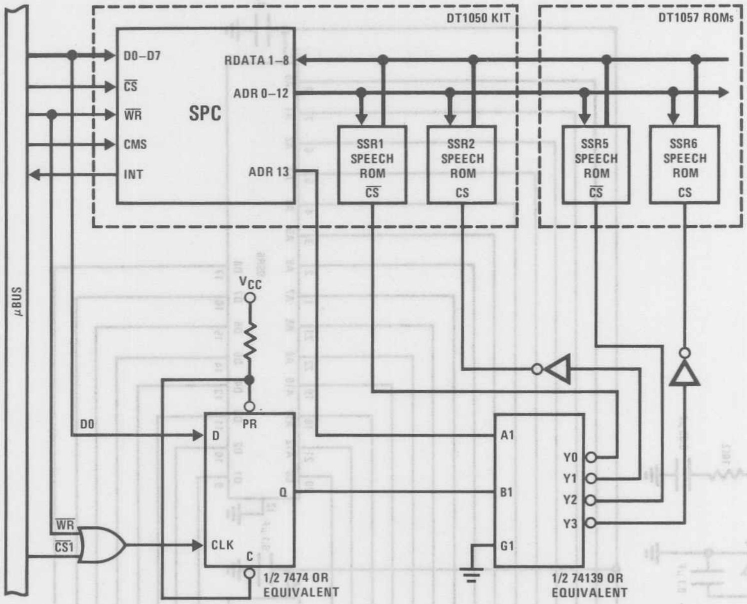
*For specific ROM device information, see MM52164 data sheet.

Recommended Schematic Diagram

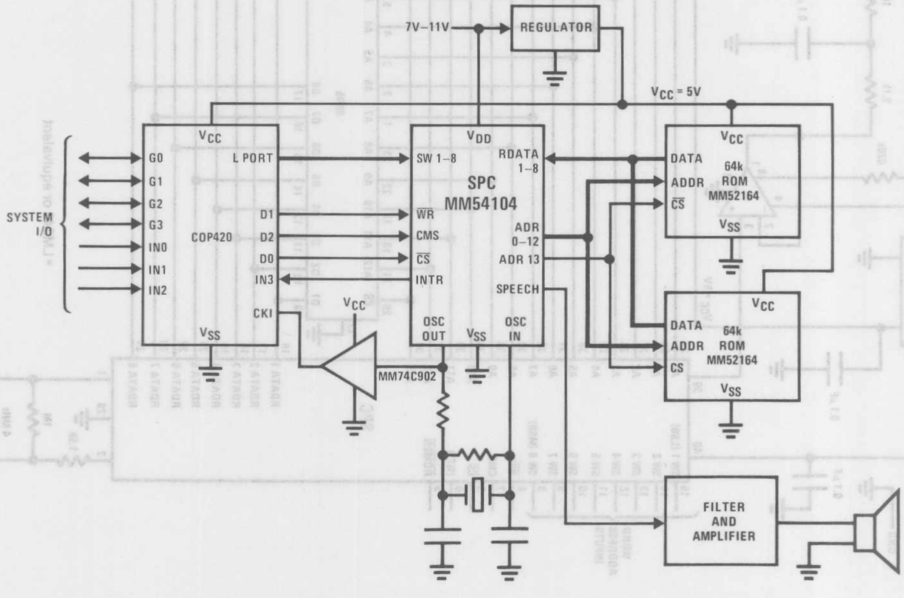


* LM346 or equivalent

Integration of DT1057 ROMs and DT1050 Kit

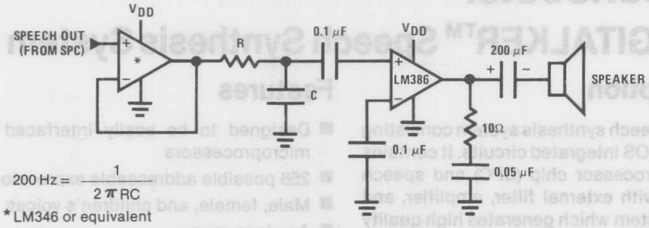


DIGITALKER System Using COP420 Interface



Typical Applications (Continued)

Minimum Filter Circuit

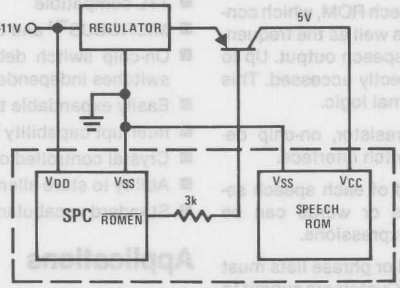


$$200\ \text{Hz} = \frac{1}{2\pi RC}$$

*LM346 or equivalent

See MM54104 data sheet for additional filter information.

Low Power Configuration Using Static ROM



National Semiconductor

DIGITALKER™ Speech Synthesis

MM54104 DIGITALKER™ Speech Synthesis System

General Description

The DIGITALKER is a speech synthesis system consisting of multiple N-channel MOS integrated circuits. It contains an MM54104 speech processor chip (SPC) and speech ROM and when used with external filter, amplifier, and speaker, produces a system which generates high quality speech including the natural inflection and emphasis of the original speech. Male, female, and children's voices can be synthesized.

The SPC communicates with the speech ROM, which contains the compressed speech data as well as the frequency and amplitude data required for speech output. Up to 128k bits of speech data can be directly accessed. This can be expanded with minimal external logic.

With the addition of an external resistor, on-chip debounce is provided for use with a switch interface.

An interrupt is generated at the end of each speech sequence so that several sequences or words can be cascaded to form different speech expressions.

Encoding (digitizing) of custom word or phrase lists must be done by National Semiconductor. Customers submit to the factory high quality recorded magnetic reel to reel tapes containing the words or phrases to be encoded. National Semiconductor will sell kits consisting of the SPC and ROM(s) containing the digitized word or phrases.

Features

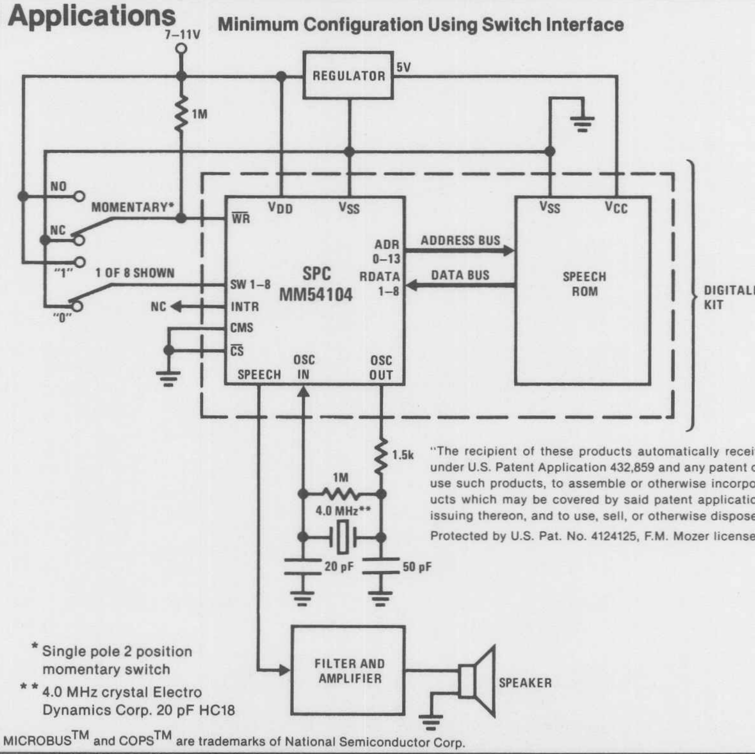
- Designed to be easily interfaced to most popular microprocessors
- 256 possible addressable expressions
- Male, female, and children's voices
- Any language
- Natural inflection and emphasis of original speech
- Addresses 128k of ROM directly
- TTL compatible
- MICROBUS™ and COPS™ compatible
- On-chip switch debounce for interfacing to manual switches independent of a microprocessor
- Easily expandable to greater than 128k ROM
- Interrupt capability for cascading words or phrases
- Crystal controlled or externally driven oscillator
- Ability to store silence durations for timing sequences
- Standard vocabulary sets available

Applications

- Telecommunications
- Appliance
- Automotive
- Teaching aids
- Consumer products
- Clocks
- Language translation
- Annunciators

Typical Applications

Minimum Configuration Using Switch Interface



"The recipient of these products automatically receives a non-exclusive license under U.S. Patent Application 432,859 and any patent or patents issuing thereon to use such products, to assemble or otherwise incorporate them into further products which may be covered by said patent application, or any patent or patents issuing thereon, and to use, sell, or otherwise dispose of such products".

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* Single pole 2 position momentary switch

** 4.0 MHz crystal Electro Dynamics Corp. 20 pF HC18

Absolute Maximum Ratings

Storage Temperature Range	$-65°C$ to $+150°C$
Operating Temperature Range	$-40°C$ to $85°C$
V_{DD}-V_{SS}	12V
Voltage at Any Pin	12V
Operating Voltage Range, V_{DD}-V_{SS}	7V to 11V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics $T_A = 0°C$ to $70°C$, $V_{DD} = 7V$–$11V$, $V_{SS} = 0V$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Voltage		−0.3		0.8	V
V_{IL}	Input Low Voltage	$T_A = -40°C$ to $85°C$	−0.3		0.6	V
V_{IH}	Input High Voltage		2.0		V_{DD}	V
V_{IH}	Input High Voltage	$T_A = -40°C$ to $85°C$	2.2		V_{DD}	V
V_{OL}	Output Low Voltage	$I_{OL} = 1.6$ mA			0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -100\ \mu A$	2.4		5.0	V
V_{ILX}	Clock Input Low Voltage		−0.3		1.2	V
V_{IHX}	Clock Input High Voltage		5.5		V_{DD}	V
V_{OLX}	Clock Output Low Voltage	Typical Crystal Configuration and 10M Load on Pin 2			1.2	V
V_{OHX}	Clock Output High Voltage	Typical Crystal Configuration and 10M Load on Pin 2	5.5		V_{DD}	V
I_{DD}	Power Supply Current				45	mA
I_{DD}	Power Supply Current	$T_A = -40°C$ to $85°C$			50	mA
I_{IL}	Input Leakage				±10	μA
I_{ILX}	Clock Input Leakage				±10	μA
V_S	Silence Voltage			$0.45\ V_{DD}$		V
V_{OUT}	Peak to Peak Speech Output	$V_{DD} = 11V$		2.0		V
R_{EXT}	External Load on Speech Output	R_{EXT} Connected Between Speech Output and V_{SS}	50			kΩ

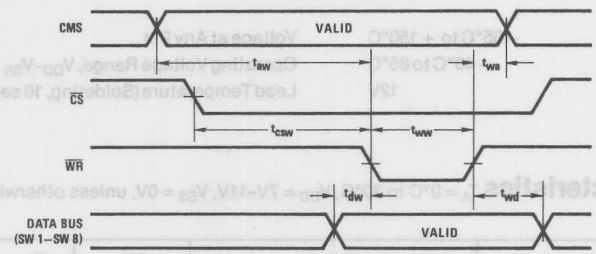
AC Electrical Characteristics $T_A = 0°C$ to $70°C$, $V_{DD} = 7V$–$11V$, $V_{SS} = 0V$, unless otherwise specified.

Symbol	Parameter	Min	Max	Units
t_{aw}	CMS Valid to Write Strobe	350		ns
t_{csw}	Chip Select ON to Write Strobe	310		ns
t_{dw}	Data Bus Valid to Write Strobe	50		ns
t_{wa}	CMS Hold Time after Write Strobe	50		ns
t_{wd}	Data Bus Hold Time after Write Strobe	100		ns
t_{ww}	Write Strobe Width (50% Point)	430		ns
t_{red}	$\overline{\text{ROMEN}}$ ON to Valid ROM Data		2	μs
t_{wss}	Write Strobe to Speech Output Delay		410	μs
f_t	External Clock Frequency	3.92	4.08	MHz

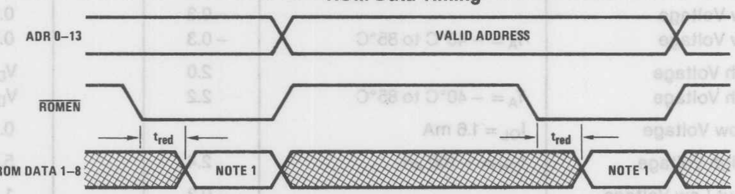
Note: Rise and fall times (10% to 90%) of MICROBUS signals should be 50 ns maximum.

Timing Waveforms

Command Sequence



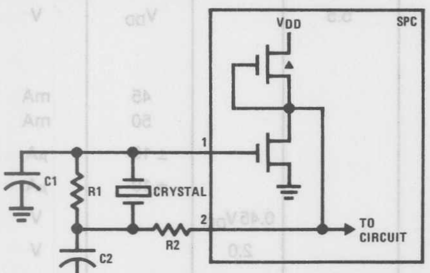
ROM Data Timing



Note 1: ROM data 1-8 can go valid any time after ADR 0-13 changes, however it must be valid within the t_{red} specifications and remain valid until ROMEN goes high.

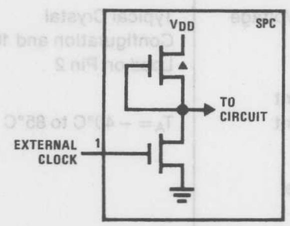
Crystal Circuit Information

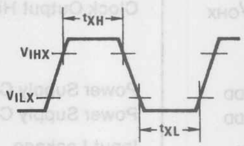
Typical Crystal Oscillator Network



Crystal	R1	R2	C1	C2
4.0 MHz	1M	1.5k	10–30 pF	40–60 pF

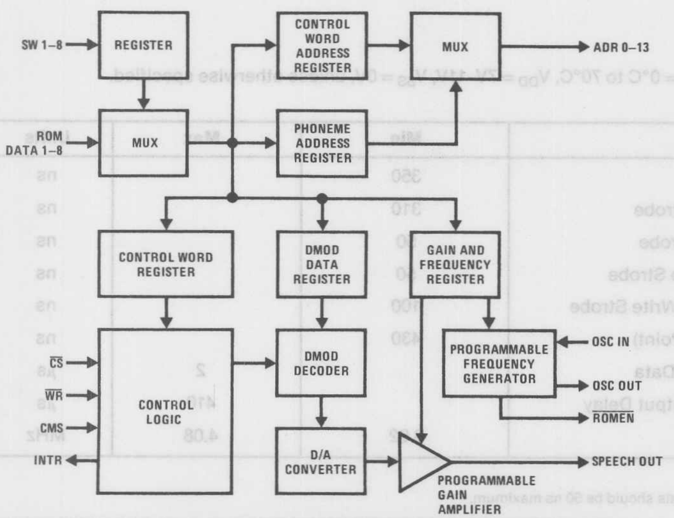
External Clock Input (4.0 MHz)



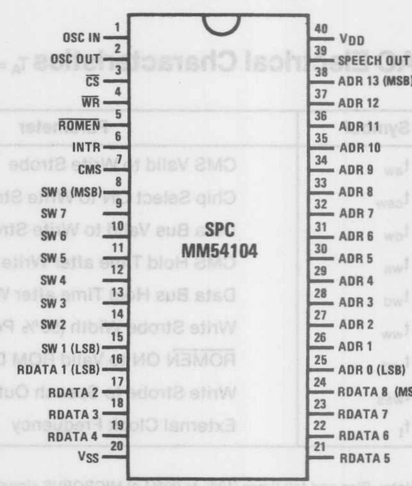


Timing	Min	Units
t_{XH}	100	ns
t_{XL}	100	ns

Block and Connection Diagrams



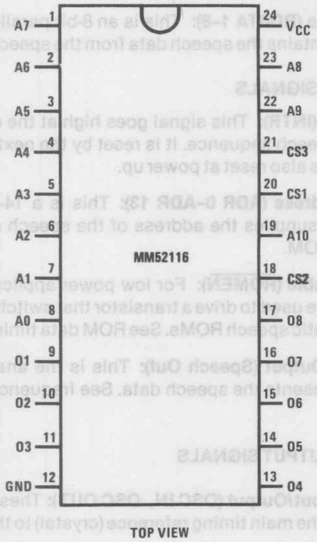
Dual-In-Line Package



TOP VIEW

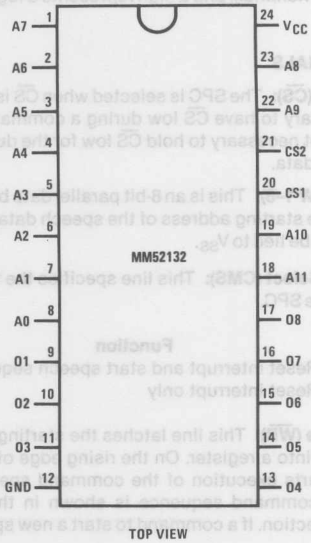
Connection Diagrams (Continued) (V_{CC} = 4.75V–5.25V)

Dual-In-Line Package



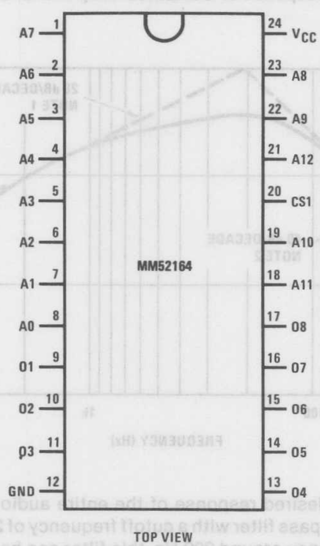
16k

Dual-In-Line Package



32k

Dual-In-Line Package



64k

For specific ROM device information, see MM52116, MM52132, or MM52164 data sheets.

Note: In the following descriptions, a low represents a logic 0 (0.4V nominal), and a high represents a logic 1 (2.4V nominal).

INPUT SIGNALS

Chip Select ($\overline{CS}$): The SPC is selected when $\overline{CS}$ is low. It is only necessary to have $\overline{CS}$ low during a command to the SPC. It is not necessary to hold $\overline{CS}$ low for the duration of the speech data.

Data Bus (SW 1-8): This is an 8-bit parallel data bus which contains the starting address of the speech data. Unused inputs must be tied to V_{SS}.

Command Select (CMS): This line specifies the two commands to the SPC.

CMS	Function
0	Reset interrupt and start speech sequence
1	Reset interrupt only

Write Strobe ($\overline{WR}$): This line latches the starting address (SW1-SW8) into a register. On the rising edge of the $\overline{WR}$, the SPC starts execution of the command specified by CMS. The command sequence is shown in the timing waveform section. If a command to start a new speech se- ... switch as shown on page 1.

ROM Data (RDATA 1-8): This is an 8-bit parallel data bus which contains the speech data from the speech ROM.

OUTPUT SIGNALS

Interrupt (INTR): This signal goes high at the completion of any speech sequence. It is reset by the next valid command. It is also reset at power up.

ROM Address (ADR 0-ADR 13): This is a 14-bit parallel bus that supplies the address of the speech data to the speech ROM.

ROM Enable ($\overline{ROMEN}$): For low power applications, this line can be used to drive a transistor that switches the supply for static speech ROMs. See ROM data timing.

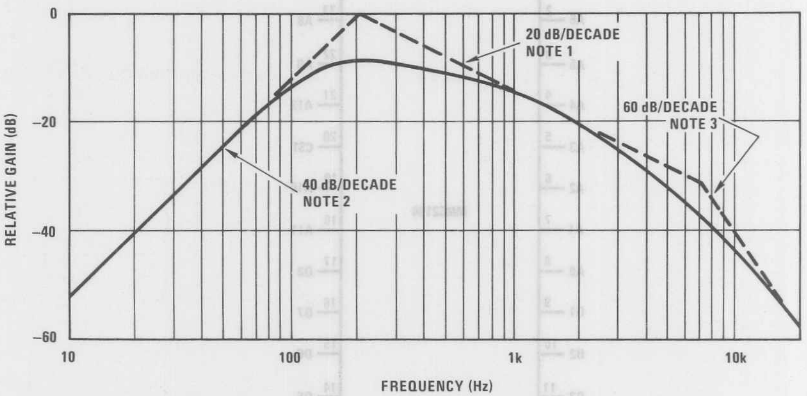
Speech Output (Speech Out): This is the analog output that represents the speech data. See frequency response section.

INPUT/OUTPUT SIGNALS

Clock Input/Output (OSC IN, OSC OUT): These two pins connect the main timing reference (crystal) to the SPC.

Applications Information

Frequency Response of Combined Amplifier and Speaker



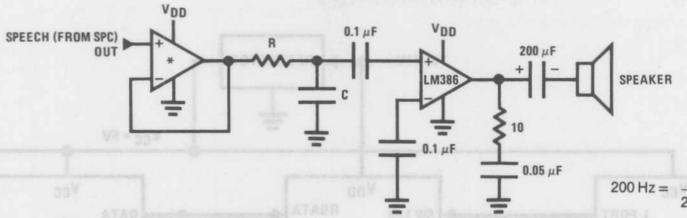
Note 1: This curve is the desired response of the entire audio system including speaker. Minimum response is a low pass filter with a cutoff frequency of 200 Hz. For an audio system with a natural cutoff frequency around 200 Hz, this filter can be eliminated. This cutoff frequency may be tuned for the particular voice being synthesized. For a low pitched male voice it may be 100 Hz, while for a high pitched female or child's voice it might be 300 Hz.

Note 2: This is optional filtering that can be eliminated by proper selection of the speaker. If this 2 pole response is electronically produced, it should be adjusted as described in Note 1.

Note 3: This is optional filtering that can be eliminated for simpler systems. The acceptable range for this cutoff frequency is 6000 Hz-8000 Hz.

Typical Applications (Continued)

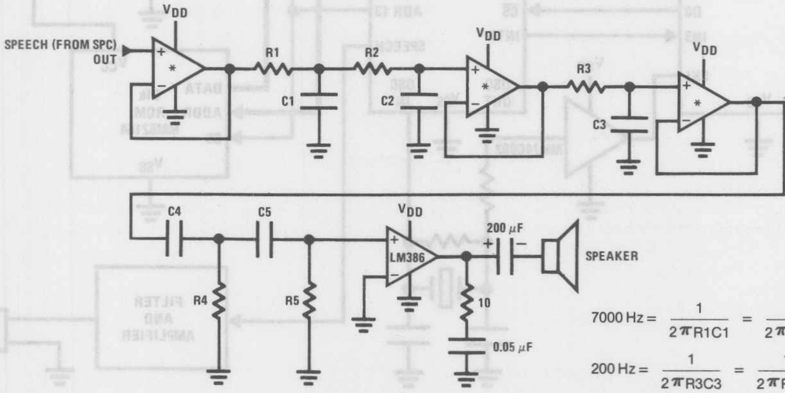
Minimum Filter Circuit



$$200\ \text{Hz} = \frac{1}{2\pi RC}$$

* LM346 or equivalent

Filter Circuit to Produce Maximum Frequency Response

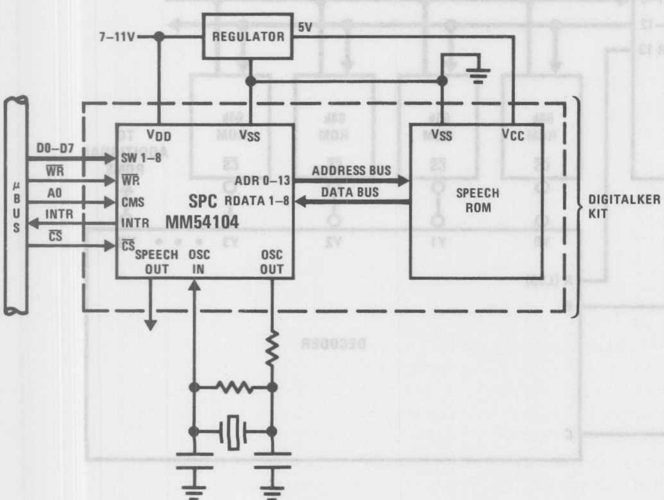


$$7000\ \text{Hz} = \frac{1}{2\pi R1C1} = \frac{1}{2\pi R2C2}$$

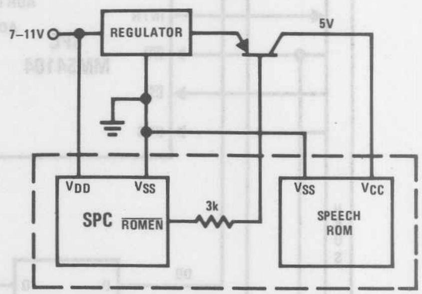
$$200\ \text{Hz} = \frac{1}{2\pi R3C3} = \frac{1}{2\pi R4C4} = \frac{1}{2\pi R5C5}$$

* LM346 or equivalent

DIGITALKER™ System Utilizing MICROBUS™ Interface

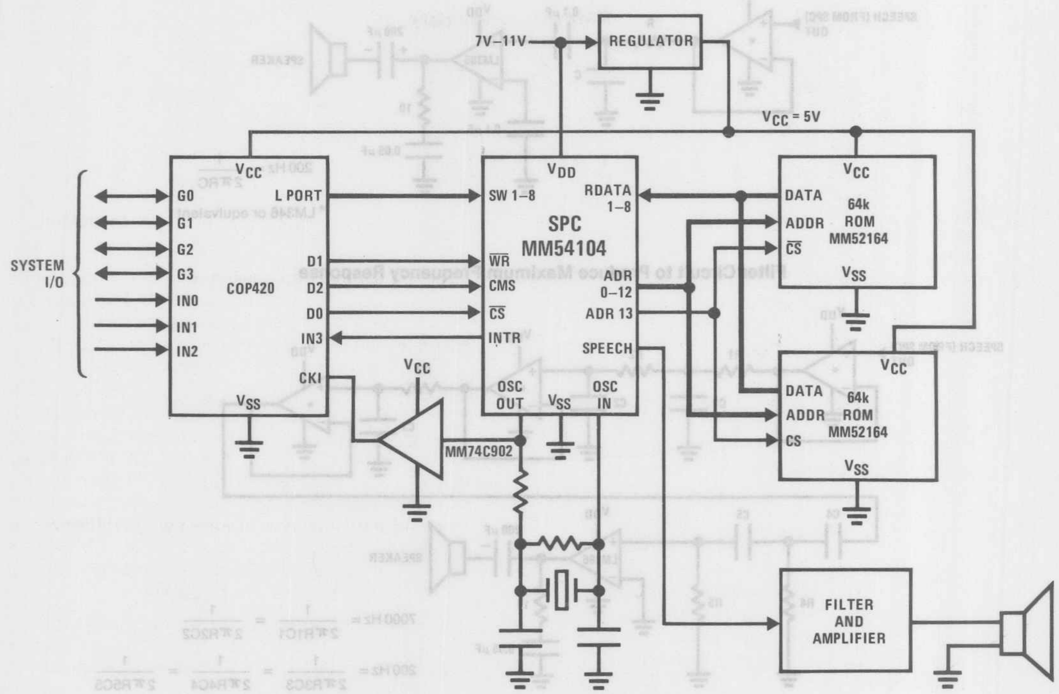


Low Power Configuration Using Static ROM

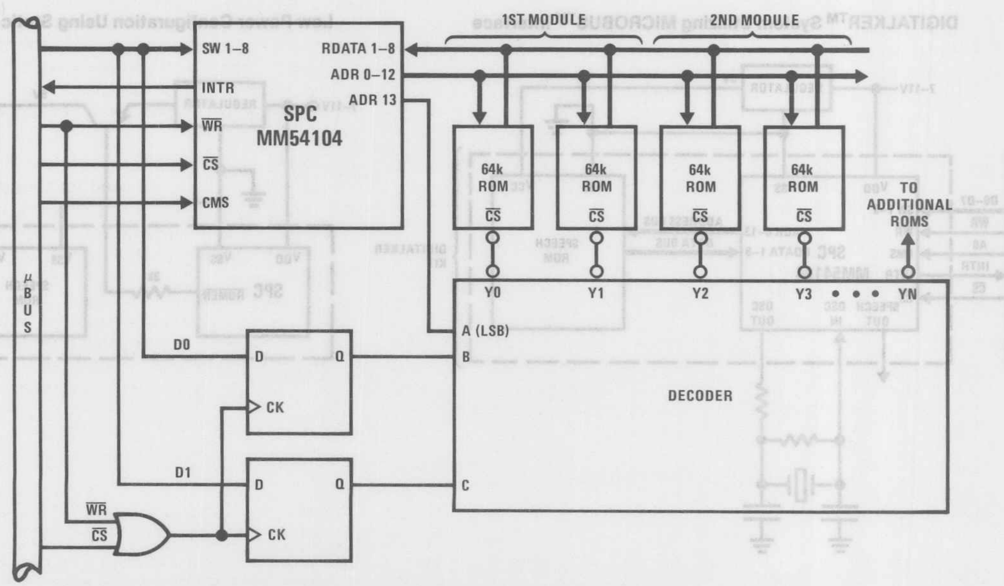


Typical Applications (Continued)

DIGITALKER™ System Using COP420 Interface



Speech ROM Expansion for Requirements Greater Than 128k Bits



Circuit for Evaluation of Custom Vocabulary EPROM Prototype Set

National Semiconductor
Linear Brief 54
Fred Wickersham
June 1981

EPROM PROTOTYPE

In the process of developing a product with a "custom" generated vocabulary, it may be necessary to develop special circuitry for listening to and evaluating your prototype synthesized vocabulary prior to committing to read only memory (ROM) production.

The prototype set will normally be supplied by National Semiconductor in the form of 2716 EPROM (Intel pinout) sets. The SPC (speech processor chip, part number MM54104) communication with EPROM sets *does* require some external hardware considerations which may not be necessary in the final ROM application, especially in multiple EPROM-equivalent ROM situations. (For example, four 16k-bit 2716 EPROMs equal one 64k-bit ROM.)

Shown on next page is a recommended circuit which shows proper interface between 2716 EPROMs and the SPC. The circuit covers vocabularies from the minimum system of one 2716 (16k bits) to larger vocabularies of eight 2716s (128k bits). It is also true, that in an application requiring only one 2716, the MM74LS138 decoder device can be eliminated by connecting pin 20 of the 2716 to V_{SS} (ground). The remaining unused pins 36, 37 and 38 of the SPC can be left unconnected in this case.

UNUSED SPC INPUTS

In any DIGITALKER™ design, an applications suggestion is in the area of unused input pins of the SPC. It should be understood that the number of different expressions and coincident addresses, as designated by the custom vocabulary, determines how many of the SW word address pins (pins 8–15) on the SPC are utilized. Vocabularies of less than 128 addresses will not use SW 8; vocabularies of less than 64 addresses will not use SW 7 or SW 8, and etc. These unused SW pins must be tied to V_{SS} (ground) to simplify the application. In fact, *any* unused *input* to the SPC must be tied to V_{SS}.

FILTERING

Use of the DIGITALKER is quite straightforward, however, a point on application that must be covered in this brief concerns the frequency response of the output speech. The ultimate quality of the DIGITALKER will strongly depend upon the filter, amplifier and speaker choices made by the user. For that reason, it is important to understand the output characteristics of the device.

Because the synthesized speech data is derived from a differentiated and sampled input signal, it is necessary to pass the output waveform of the MM54104 through a low-pass filter with a cutoff frequency of approximately 200 Hz and an attenuation characteristic of 20 dB/decade. This compensates for the high frequency pre-emphasis used in the synthesis technique. If the system of interest has a natural rolloff near 200 Hz, this low-pass filter can be eliminated. The important item is that the entire audio system should have a cutoff frequency of approximately 200 Hz. The placement of the cutoff frequency may be adjusted for the particular type of voice being synthesized. A low pitched man's voice might sound better with a 100 Hz cutoff point while women's and children's voices may show improvements with a 300 Hz cutoff.

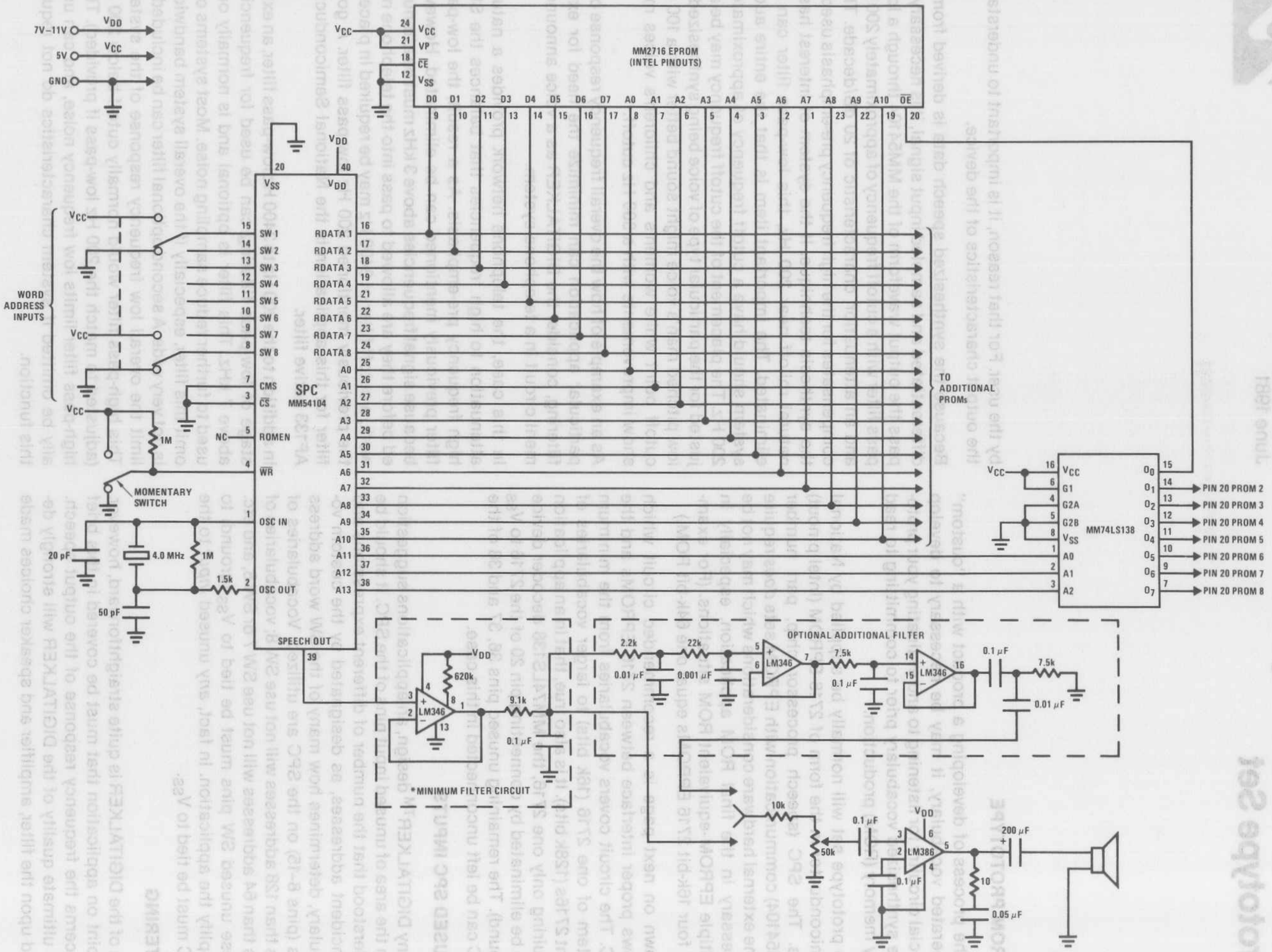
As an example of how the overall frequency response of a particular application can minimize the need for extra filtering, consider the DIGITALKER as a voice announcement circuit in a telephone system.

In this case, the telephone network provides a natural attenuation to high frequencies that balances the SPC high frequency pre-emphasis. As a result, the low-pass filter previously mentioned can be eliminated. However, because signal frequencies above 3 kHz must be attenuated before they are allowed to pass into the telephone network, a cutoff filter of 3400 Hz may be required in place of the previously mentioned 200 Hz low-pass filter. A good filter for this application is the National Semiconductor AF133 active filter.

In addition to the 200 Hz to 3400 Hz low-pass filter, an extra stage of low-pass filtering can be used for frequencies above 7 kHz. This filter is optional and is normally only used to further reduce sampling noise. Most systems can omit this filter, especially if the overall system bandwidth is not very wide. A second optional filter can be included to limit the overall low frequency response of the system. This high-pass filter would normally cutoff below 200 Hz (adjusted to match the 200 Hz low-pass if provided). This high-pass filter limits low frequency noise, and can usually be omitted if system characteristics do not require this function.

LB-54 Circuit for Evaluation of Custom Vocabulary EPROM Prototype Set

Recommended Circuit for Evaluating up to 8 Custom Encoded EPROMs (2716)



Note: All unused inputs to SPC must be tied to ground (V_{SS}).

* Recommended filter requirements. See text and MM54104 data sheet for complete filter application suggestions

Speech Synthesis

National Semiconductor
Application Note 252
Jim Smith
Dave Weinrich

INTRODUCTION

Electronic speech circuits offer a new dimension of sophistication to many modern machines. As annunciators in trains, elevators, office buildings, autos, airplanes, terminals, toys and games, etc., electronic speech circuits provide a more direct and natural announcement than bells, buzzers or lights. With electronic voice signals, complex directions can be clearly given in any language and with a minimum of effort.

In the past, electronic announcement systems required elaborate tape mechanisms. These systems were expensive and troublesome, so their use was limited to the small number of applications that required speech announcements (e.g., telephone announcement systems). The first all-electronic systems used analog to digital conversion techniques to convert actual voice into digital signals. These digital speech signals were then stored as PCM or delta modulation signals in semiconductor memories. The major problem with this arrangement was the massive memory required for a moderate amount of announcement time. One second of digital speech, in this configuration, required from 16k to 100k bits of memory.

The latest solution to electronic speech is known as speech synthesis. This technique provides a dramatic reduction in the memory required for one second of speech. Memory requirements range from 400 bits to 2000 bits per second depending on the desired speech attributes and overall quality. The synthesizer technique takes advantage of the fact that speech signals are highly redundant and predictable. By coding only the slowly varing coefficients of speech or by dramatic compression of digitized speech, significant bandwidth reductions in the digitized signal can be realized. These techniques, coupled with LSI semiconductor technology, make true voice synthesis practical.

The National Semiconductor speech processor chip (SPC) provides the complete speech synthesis reproduction circuitry needed to generate high quality and natural speech (male, female or a child's voice), electronic tones or music. A complete chip set is called the DIGITALKER™. It consists of the speech processor chip and a speech ROM. The applications for this chip set are endless, but to name a few:

- Voice interactive computer terminals
- Automotive, nautical and aeronautical instrumentation annunciators
- Voice-back units for banking, weather and time announcements, answering machines, etc.
- Elevators, trains, subway systems, etc.
- Consumer appliances, toys and games
- Warning systems for fire and police emergency

All of these applications benefit from the lower overall cost, high reliability, excellent performance and fast control response afforded by the National Semiconductor DIGITALKER™ system. The remainder of this note will be devoted to a description of the MM54104 SPC, the technique used to synthesize speech and finally a review of the major DIGITALKER™ applications.

SPEECH SYNTHESIS

The basic phonological element of speech is the phoneme. The phoneme represents a simple sound that by itself cannot distinguish different words. Phonemes, together with speaker inflection, volume, emphasis, etc. are the fundamental building blocks of speech. The overall quality of any speech synthesizer, therefore, is directly controlled by its ability to faithfully reproduce all of the necessary speech attributes and not just phoneme reproduction.

The common American English language consists of approximately 38 to 40 phonemes—14–16 vowel sounds and 24 consonant sounds. Each phoneme is generated with either a voiced sound, as in "eye", or an unvoiced sound like the sh in "shy". This difference between a voiced and unvoiced sound is very important because the unvoiced sounds are generally fewer in number and less dependent upon the physiological characteristics of the speaker. A speech synthesizer, it turns out, can exploit this important difference. Finally, normal speech rates are approximately 10 to 15 phonemes per second (including silence intervals). Since 38-40 phonemes can be coded using 6 bits, the normal bit rate for phoneme reproduction is approximately 60 to 90 bits per second. This bit rate, however, contains only phoneme information which is only one of the many important speech attributes.

Since phoneme reproduction is a basic element in any speech synthesizer, an understanding of phoneme construction would be useful. Speech synthesis models use two driving functions, an impulse source for voiced sounds and a noise source (hiss noise) for unvoiced sounds. Each of these driving signals are filtered into specific frequency bands or formants by time-varying filters. The net result, for any particular set of valid filter coefficients, is a formant sound. In the human vocal tract system, the driving function consists of the lungs as the energy source, and the vocal cords for generating a voiced sound. The driving function for an unvoiced sound relies on the noise generated as air rushes through the vocal chambers and not on vocal cord vibrations. The formants are then generated by the resonant chambers of the throat, mouth and nasal cavities. By controlling the physical nature of these chambers with mouth position, tongue position and throat orifice size, a speaker can control the formants to generate a phoneme. It should be noted, however, that formants are identified by distinctive frequency bands. The unvoiced sounds do not generate these distinctive bands and therefore do not necessarily require the "normal" formants for a faithful reproduction. These sounds are characterized by a noise or hiss with very little resonance. This unvoiced resonance is normally identified as a fricative formant (e.g., the "sh" sound) and is characterized by an unusually large content of high frequencies.

DIGITALKER™ is a trademark of National Semiconductor Corp.

for voiced sounds and one formant filter for unvoiced sounds. An additional resonance, called nasal resonance, may be included but no dynamic formant function is usually associated with the nasal resonator. For the synthesis of a normal English vowel using a male voice, the three basic formants would fall into the approximate frequency bands of 200 Hz to 800 Hz, 900 Hz to 2300 Hz and 2400 Hz to 3000 Hz. The fricative formant is typically a pulse of high frequency noise in the band from approximately 2500 Hz to 8000 Hz, with the higher frequency fricatives like "th" usually much lower in relative amplitude when compared to the "sh" fricative sound.

The basic formant synthesizer requires formant filter coefficient data, amplitude control data and driving function control data. This minimum system could synthesize speech, but would not control inflection or emphasis. Its quality, therefore, can be very disappointing. Normal memory requirements for a minimal system are approximately 400 bits for one second of speech.

A second approach to speech synthesis does not automatically break speech into its minimum phonological elements. Instead, the speech waveform is sampled, digitized and compressed by the elimination of symmetrical redundancy and silent intervals, the use of adaptive delta modulation, and the adjustment of phase information in the digitized speech. In this way, speech elements can be synthesized as phonemes, phoneme groups, words or even whole phrases. Also, the attributes of the original speaker can be maintained if the synthesized elements are not broken down incorrectly (i.e., inflection can modify the sound of a phoneme if it occurs at the end of a word or phrase rather than at the beginning).

sounds are compressed. Unvoiced sounds, however, are compared to the available sounds and synthesized by substitution. This approach is successful because unvoiced sounds have very few speaker defined characteristics. As a result, a relatively small set of unvoiced sounds can be used repeatedly.

This speech compression technique offers excellent quality at a low data rate. The synthesis of a male voice, using English, will usually require an average of 1000 bits per word. Because the technique can be applied to any voice frequency signal, it is also capable of synthesizing women's and children's voices, music and tones. This flexibility, plus the realistic quality of the synthesized speech, make this technique very attractive.

THE NSC SPEECH PROCESSOR CHIP (SPC)

The National Semiconductor speech synthesis system consists of the SPC device plus the speech memory (ROM) required to assemble a complete DIGITALKER™ kit. To this kit a customer must add a clock input signal or the necessary oscillator components, an audio filter and amplifier and the control circuit function. This would represent the minimum configuration shown in *Figure 1.* The maximum amount of directly addressable speech memory accessible by the SPC is 128k bits, but external page addressing by the control circuit function can increase this ROM field as required.

The SPC utilizes the speech compression synthesis technique. As mentioned earlier, this technique reduces the amount of memory needed to store electronic speech by removing the excess or redundant data from the

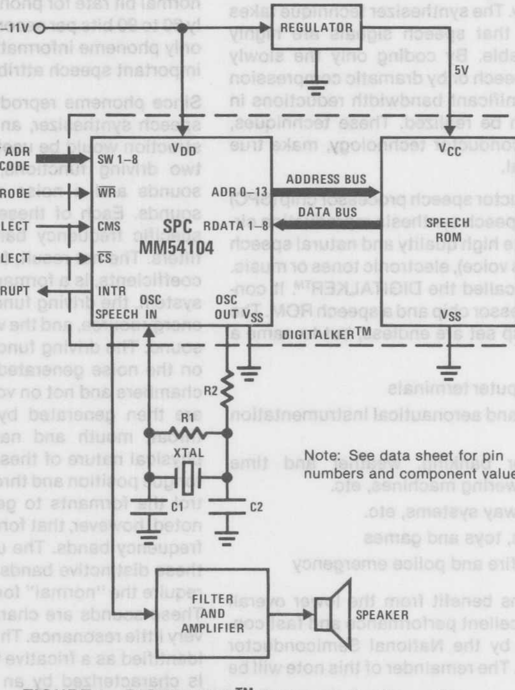


FIGURE 1. DIGITALKER™ Minimum Configuration

speech signal. The four main techniques to perform that task are:

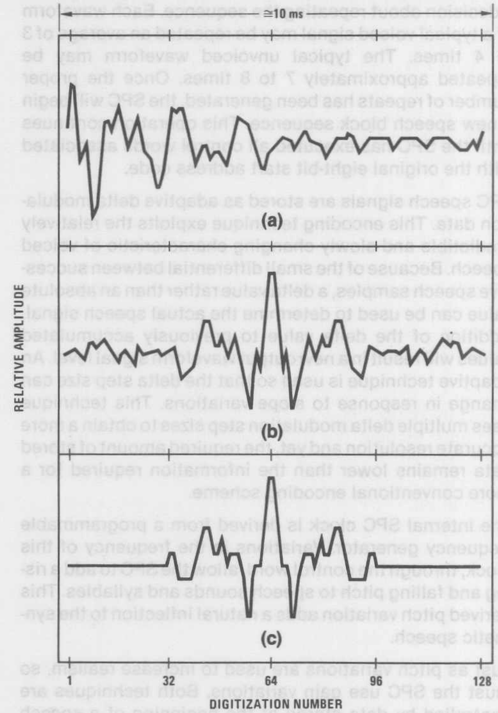
1. Elimination of redundant pitch periods
2. Adaptive delta modulation coding to minimize bandwidth and memory requirements
3. Phase angle adjustments to create mirror image symmetry
4. Replacing the low level portion of a pitch period with silence (half-period zeroing)

National Semiconductor uses an elaborate computer program to analyze a high fidelity tape recording and generate a ROM pattern that will faithfully synthesize the original voice message.

Figure 2 contains a block diagram of the MM54104 SPC. The eight-bit start address bus allows up to 256 separately defined sounds or expressions to be stored in the speech ROM. The control interface to the start address port can take the form of decoding logic, a MICROBUS™ port or mechanical switches.

When the $\overline{WR}$ goes high, the start address code is loaded into the control word address register. The SPC uses this control address to fetch the control word from ROM for the first block of speech data. The control word contains waveform information, repeat information and the address of the speech data. This address is loaded into the phoneme address register and is used to fetch the speech data used to recreate the speech waveform. Before the synthesis takes place, the waveform data must be decoded to provide information such as male or female, voiced or unvoiced, half-period zeroed or not half-period zeroed and silence.

The unsynthesized waveform for a typical voiced pitch period might look like the signal shown in *Figure 3a.* In the process of converting this signal to a synthetic form, several operations are performed. First, the phase delay of the signal can be adjusted to create a symmetrical waveform about the center of the pitch period as shown in *Figure 3b.* The next step will replace the low level beginning and ending quarters of the waveform with silence *(Figure 3c).* The result is a compression factor of 4 to 1 on the original voice data. Now, delta modulation is applied and the results are shown in *Figure 3c.* Synthesis of the waveform starts with a period of silence (no speech data required), a quarter period of adaptive delta modulation-generated speech followed by the same speech data



(a) Original Speech Waveform
(b) Phase Angle Adjusted to Create Mirror Symmetry
(c) Half-Period Zeroed and Delta Modulated

FIGURE 3. SPC Waveforms (After Mozer [2])

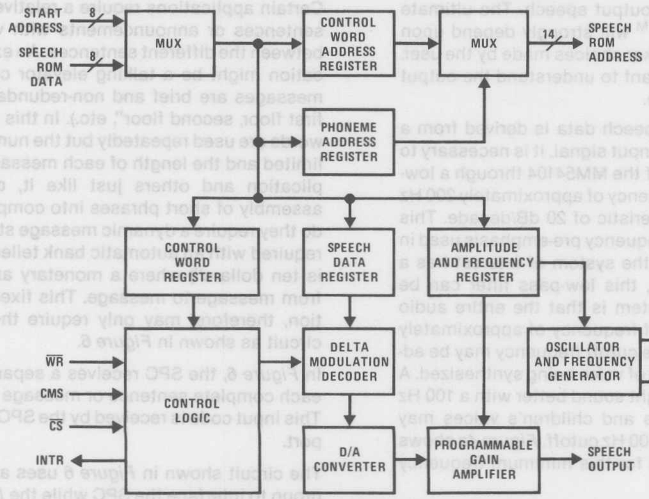


FIGURE 2. MM54104 Block Diagram

MICROBUS™ is a trademark of National Semiconductor Corp.

fetched in reverse. Finally, the SPC will finish the last quarter cycle of the speech block period with silence. This phase modified speech data sounds the same as the original speech.

At the end of a waveform or speech block, the SPC makes a decision about repeating the sequence. Each waveform of a typical voiced signal may be repeated an average of 3 to 4 times. The typical unvoiced waveform may be repeated approximately 7 to 8 times. Once the proper number of repeats has been generated, the SPC will begin a new speech block sequence. This operation continues until the SPC has executed all control words associated with the original eight-bit start address code.

SPC speech signals are stored as adaptive delta modulation data. This encoding technique exploits the relatively predictible and slowly changing characteristic of voiced speech. Because of the small differential between successive speech samples, a delta value rather than an absolute value can be used to determine the actual speech signal. Addition of the delta value to previously accumulated values will result in a new output waveform signal level. An adaptive technique is used so that the delta step size can change in response to slope variations. This technique uses multiple delta modulation step sizes to obtain a more accurate resolution and yet, the required amount of stored data remains lower than the information required for a more conventional encoding scheme.

The internal SPC clock is derived from a programmable frequency generator. Variations in the frequency of this clock, through the control word, allow the SPC to add a rising and falling pitch to speech sounds and syllables. This derived pitch variation adds a natural inflection to the synthetic speech.

Just as pitch variations are used to increase realism, so must the SPC use gain variations. Both techniques are controlled by data stored at the beginning of a speech block and the programmable oscillator and output amplifier circuit blocks of the SPC.

Use of the DIGITALKER™ is quite straightforward and will be outlined in the next section. However, a point on application that must be covered in this note concerns the frequency response of the output speech. The ultimate quality of the DIGITALKER™ will strongly depend upon the filter, amplifier and speaker choices made by the user. For that reason, it is important to understand the output characteristics of the device.

Because the synthesized speech data is derived from a differentiated and sampled input signal, it is necessary to pass the output waveform of the MM54104 through a low-pass filter with a cutoff frequency of approximately 200 Hz and an attenuation characteristic of 20 dB/decade. This compensates for the high frequency pre-emphasis used in the synthesis technique. If the system of interest has a natural rolloff near 200 Hz, this low-pass filter can be eliminated. The important item is that the entire audio system should have a cutoff frequency of approximately 200 Hz. The placement of the cutoff frequency may be adjusted for the particular type of voice being synthesized. A low pitched man's voice might sound better with a 100 Hz cutoff point while women's and children's voices may show improvements with a 300 Hz cutoff. *Figure 4a* shows a filter and amplifier circuit for this minimum frequency response characteristic.

As an example of how the overall frequency response of a particular application can minimize the need for extra filtering, consider the DIGITALKER™ as a voice announcement circuit in a telephone system.

In this case, the telephone network provides a natural attenuation to high frequencies that balances the SPC high frequency pre-emphasis. As a result, the low-pass filter previously mentioned can be eliminated. However, because signal frequencies above 3 kHz must be attenuated before they are allowed to pass into the telephone network, a cutoff filter of 3400 Hz may be required in place of the previously mentioned 200 Hz low-pass filter. A good filter for this application is the National Semiconductor AF133 active filter.

In addition to the 200 Hz to 3400 Hz low-pass filter, an extra stage of filtering can be used for frequencies above 7 kHz. This filter is optional and is normally only used to further reduce sampling noise. Most systems can omit this filter, especially if the overall system bandwidth is not very wide. A second optional filter can be included to limit the overall low frequency response of the system. This high-pass filter would normally cutoff below 200 Hz (adjusted to match the 200 Hz low-pass if provided). This high-pass filter limits low frequency noise, and can usually be omitted if system characteristics do not require this function. A circuit having the full frequency response characteristic is shown in *Figure 4b*. *Figure 5* shows the recommended overall speech synthesis system frequency response.

APPLICATIONS

While the variety of synthetic speech applications are numerous, the actual implementation in any single application is usually limited to one of the following three techniques:

(a) Single channel, hardware control logic

(b) Single channel, software control logic

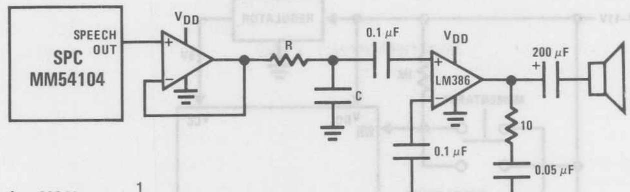
(c) Multichannel, hardware or software control logic

Each of these circuit approaches for the SPC will be discussed in this section. Particular emphasis will be placed on items (b) and (c), however, because of the broad application possibilities for these two techniques.

Certain applications require a relatively small number of sentences or announcements with very little similarity between the different sentences. An example of this application might be a talking elevator controller where the messages are brief and non-redundant (e.g., "going up, first floor, second floor", etc.). In this application, certain words are used repeatedly but the number of messages is limited and the length of each message is short. This application and others just like it, do not require the assembly of short phrases into complete sentences, nor do they require a dynamic message structure as would be required with an automatic bank teller (e.g., "your change is ten dollars") where a monetary amount may change from message to message. This fixed message application, therefore, may only require the minimum control circuit as shown in *Figure 6*.

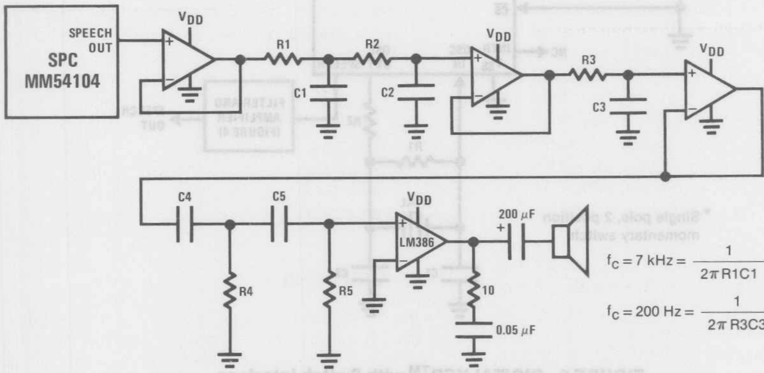
In *Figure 6*, the SPC receives a separate coded input for each complete sentence or message that is synthesized. This input code is received by the SPC through the SW 1–8 port.

The circuit shown in *Figure 6* uses a mechanical switch group to interface the SPC while the *Figure 7* circuit uses a hardware logic controller to input the coded message control data.



$$f_C = 200\text{ Hz} = \frac{1}{2\pi RC}$$

(a) Minimum Low-Pass Filter/Amplifier



$$f_C = 7\text{ kHz} = \frac{1}{2\pi R1C1} = \frac{1}{2\pi R2C2}$$

$$f_C = 200\text{ Hz} = \frac{1}{2\pi R3C3} = \frac{1}{2\pi R4C4} = \frac{1}{2\pi R5C5}$$

(b) Maximum Filter Response Configuration

FIGURE 4. SPC Filter and Amplifier

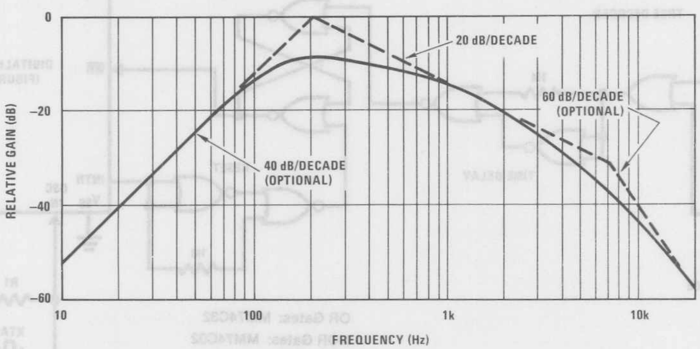


FIGURE 5. Recommended Frequency Response of Entire Audio System for MM54104 SPC

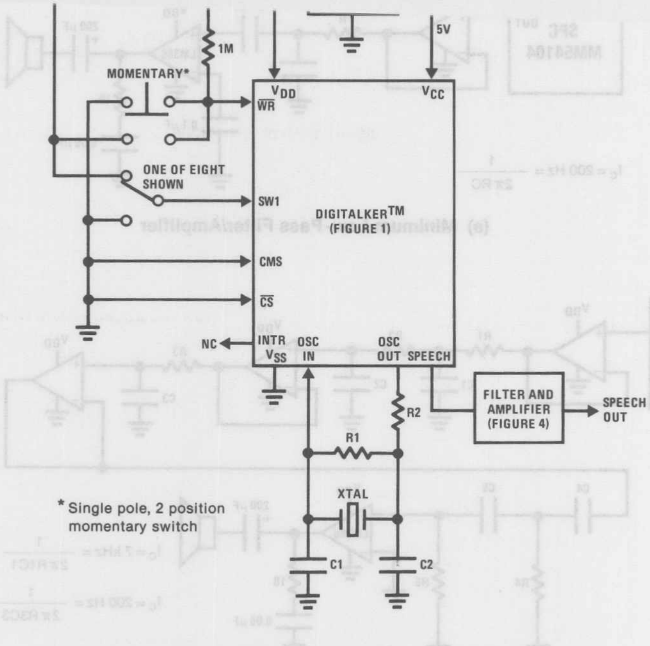


FIGURE 6. DIGITALKER^{TM} with Switch Interface

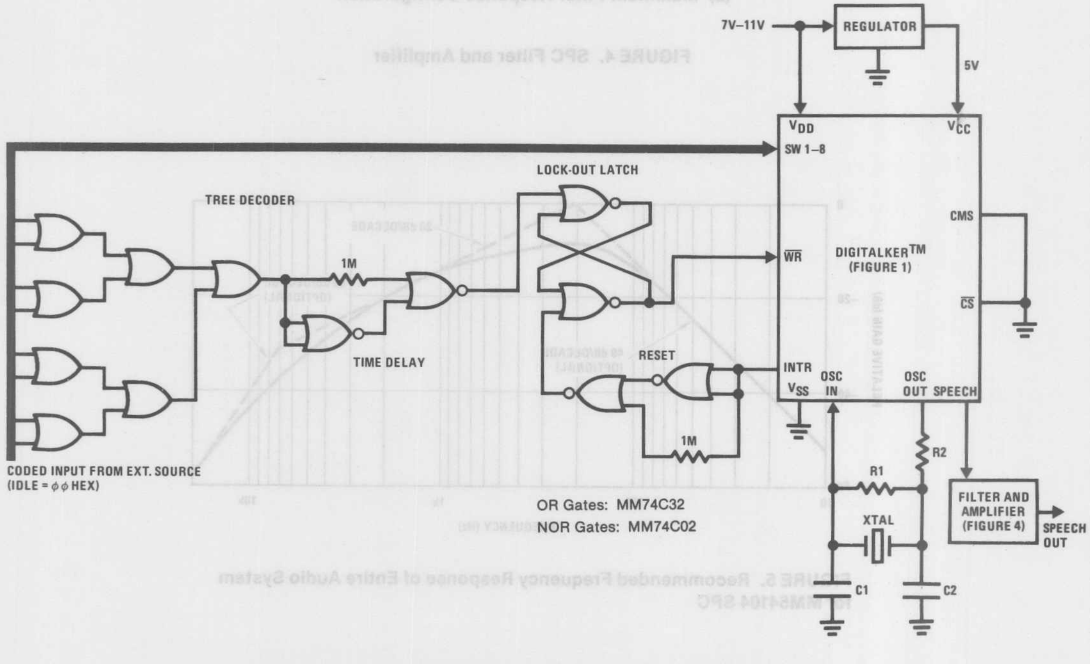


FIGURE 7. DIGITALKER^{TM} with Logic Control Interface

After the proper message address is established on the SW 1-8 port, a momentary pulse must be applied to the $\overline{WR}$ line. If this signal is applied with a momentary action switch, as shown in *Figure 6,* then an external pull-up resistor should be used to pull the $\overline{WR}$ line up to logic high and complete the on-chip switch debounce circuitry. The suggested value of this resistance is one megohm. The $\overline{WR}$ input signal will latch the coded message address into the SPC on the rising edge of $\overline{WR}$ and initiate the synthetic speech message. Since each complete message uses a unique address code of the SW 1-8 port, no further control action is required after this point. The SPC will synthesize the requested message and return to the idle state. If a new input command signal is received, either during or after a message is synthesized, the SPC will immediately abort the current message and begin the new one. The circuit in *Figure 7* shows a lock-out circuit to prevent the aborting of a current message so that messages must be completed before a new message can be initiated.

In *Figure 7,* a message is initiated whenever a valid code word is applied to the eight-bit SW 1-8 port of the SPC. The valid code is detected by the combinational logic decoder and timed to insure all transitions have died. Once the valid code is timed, an S-R latch is set and a $\overline{WR}$ rising edge is generated to start the SPC. This latch circuit also prevents retriggering of the SPC until after the present speech message is completed. Once the synthesized message has ended, the SPC will set the INTR line to the logic one state and a reset pulse will be generated to reset the lock-out latch. A new speech message can now be started by momentarily applying an idle address code followed by a valid code on the SW 1-8 input port.

The SPC will directly address up to 128k bits of speech memory. *Figure 8a* shows a typical speech ROM configuration of 128k using two 64k ROMs. The types of ROMs used have mask programmable chip selects, therefore, no extra decode logic is required for memory requirements of less than 128k. Although this memory size is usually sufficient for most applications, certain systems may require added speech ROM addressing. The circuit in *Figure 8b* shows how the speech ROM of an SPC kit can be expanded in 128k bit pages or modules. Each page is arranged to contain a complete portion of the entire speech library for a particular system. Each single speech data block, as addressed via the start address port of the SPC, must be contained within one ROM page. No page boundaries can be crossed during the synthesis of a speech expression.

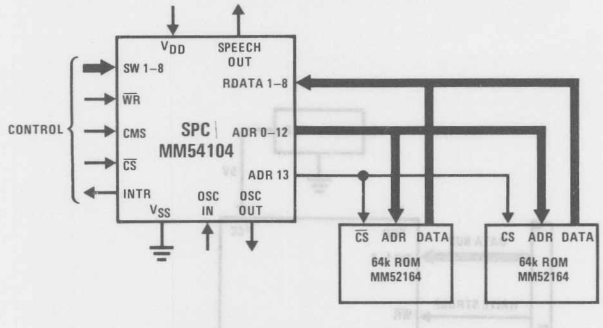


FIGURE 8a. Typical Speech ROM Configuration

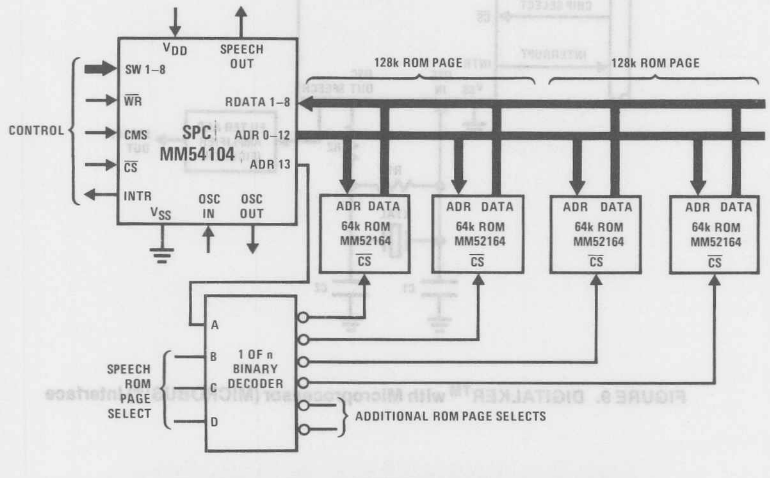


FIGURE 8b. Speech ROM Expansion Configuration

While the simple control schemes discussed so far can be used in many applications, a far more important group of applications will take advantage of the SPC's ability to construct sentences from a group of words, sounds and phrases. This type of application uses an intelligent controller or a microprocessor to string together a group of synthesized phrases to form a complete sentence. The electronic bank teller, previously mentioned, is a good example of this application. The microprocessor controls the stringing of SPC code addresses and applies them, one at a time, to the SW 1–8 port of the SPC. Handshake timing between the microprocessor and the SPC is provided with the INTR line. This microprocessor interface arrangement is known as MICROBUS™ and the configuration is shown in *Figure 9*.

The use of a microprocessor controller expands the versatility of the SPC tremendously. Messages that are composed of numerical responses or fixed phrases in random sequence can be easily constructed from a library speech memory. In addition, various tones or warnings can be synthesized and added before, during, or after an announcement to identify the urgency of each message. For example, an automobile message may state that "oil pressure is low". Alone, that message may only mean that pressure has dropped but no immediate hazard exists. If, however, pressure has dropped below a critical value, the message could be compounded to say "warning, oil pressure is low, pull over and stop the engine". In this latter case, phrases of high urgency are added to the initial message to increase its level of importance. Of course, the second message is not completely separate from the first but is, instead, an expansion of the first. This technique allows fewer input address codes to initiate a larger number of messages without assigning a separate address code for each message and for each of its derivatives. This would be particularly important to an electronic bank teller since a large number of monetary amounts must be synthesized for a relatively small number of finished sentences.

When preparing a speech ROM for an SPC that will synthesize whole sentences from groups of phrases, it is important to note the desired inflections. The SPC has the ability to synthesize all of the important speech attributes including pitch and gain variations, emphasis, inflection, etc. This leads to very high quality life-like synthetic speech if the stringing of phrases does not result in an artificial emphasis or inflection. It is important to choose phrases carefully and to record them with the attribute required for a realistic sentence string. The stringing of phonemes should be avoided whenever possible because the natural inflection is usually lost in such an arrangement.

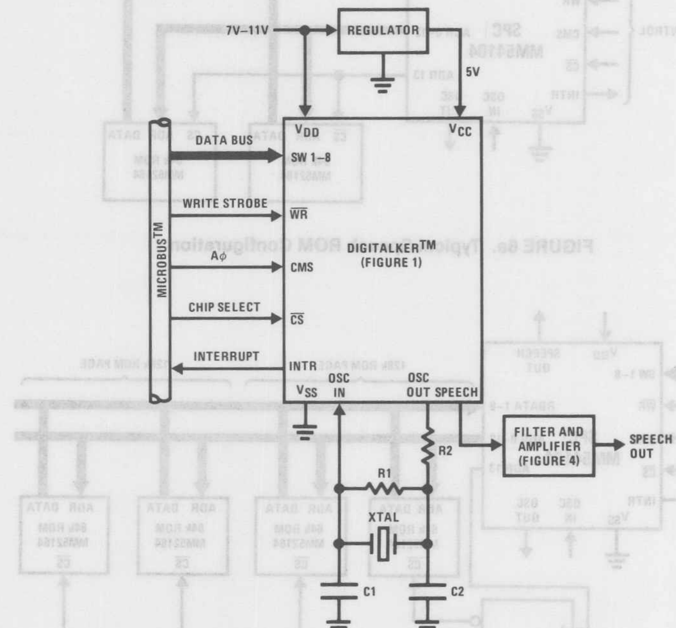


FIGURE 9. DIGITALKER™ with Microprocessor (MICROBUS™) Interface

A low cost intelligent controller for the SPC is one of the COP400 series of microcontrollers. *Figure 10* shows one possible arrangement of an SPC system and a COP420. The COP provides all of the advantages associated with a MICROBUS™ interface at a relatively low cost. Because of its limited I/O structure, the COP's serial I/O port is expanded as required to obtain the desired number of input lines.

The final application technique to be covered is the multichannel configuration. The previous arrangements used an SPC and a dedicated set of speech ROMs to provide a single channel of synthetic speech. Appliances, autos, toys and games, terminals, etc. would probably use a single channel SPC arrangement. But an entirely different group of products could take advantage of a multiple channel approach to reduce the ROM requirements. This group of products includes multiple elevator controllers, electronic bank tellers, multiple pupil learning centers, voice response telephone answering equipment, telephone switching system call announcement centers, etc. In this application, each channel would use a separate SPC and amplifier circuit, but several channels would share a common controller and speech library ROM. A typical configuration is shown in *Figure 11*.

The library ROM of *Figure 11* is shared over eight SPC channels. Each SPC channel is scanned once in 16 μs as

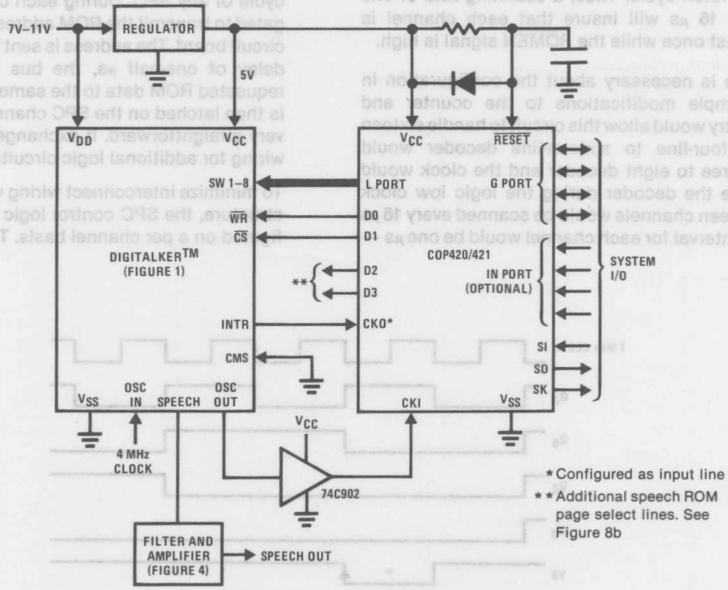


FIGURE 10. DIGITALKER™ with COP420/COP421 Interface

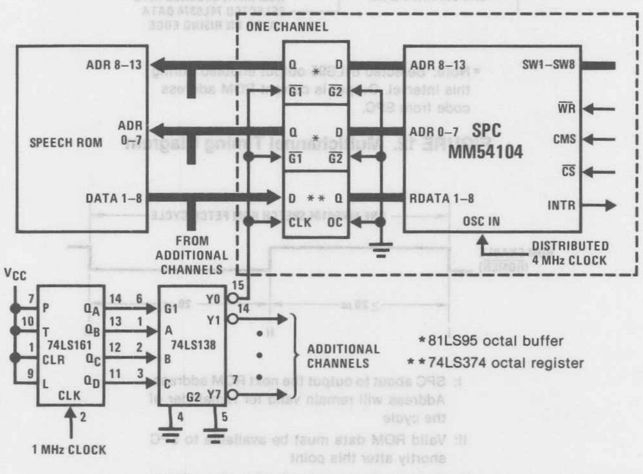


FIGURE 11. Multichannel Speech Synthesizer

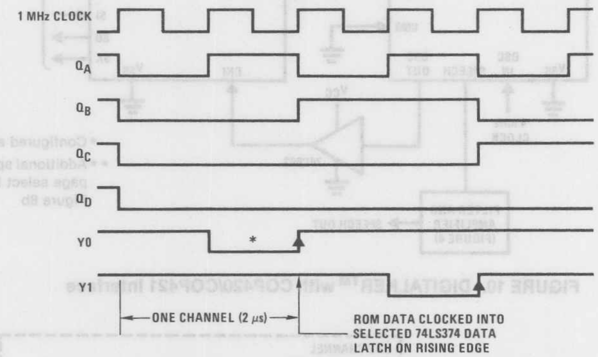
one μs, the data from the ROM is clocked into the channel's octal data latch, the output of which is connected to the SPC ROM data input port. The remaining 1 μs of each channel cycle is provided for bus settling time.

When the speech library ROM is shared over many channels, the actual number of shared channels is controlled by the MM54104 SPC memory cycle timing. Because the channel scanning is asynchronous to the SPC cycle timing, it is necessary for each channel to be scanned at least once during the high interval of the $\overline{\text{ROMEN}}$ signal. As shown in *Figure 13,* this signal is high for at least 20 μs of each memory fetch cycle. Thus, a scanning rate of one channel every 16 μs will insure that each channel is scanned at least once while the $\overline{\text{ROMEN}}$ signal is high.

One final note is necessary about the configuration in *Figure 11.* Simple modifications to the counter and decoder circuitry would allow this circuit to handle sixteen channels. A four-line to sixteen-line decoder would replace the three to eight decoder and the clock would directly enable the decoder during the logic low clock period. All sixteen channels would be scanned every 16 μs and the scan interval for each channel would be one μs — scheme reduces the number of wires speech ROM and each SPC channel. By multiplexing address and data over the same parallel bus, fewer wires are needed. This approach is particularly attractive when each SPC channel is located on an individual circuit card. A telephone central office or PABX announcement system is a typical example of a channel per card arrangement. *Figure 14* represents that type of system.

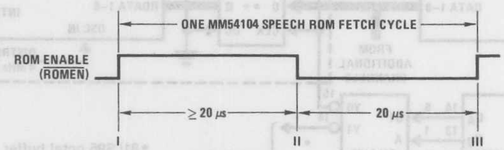
As shown in *Figure 15,* each channel of the unified bus approach is scanned for one μs. As many as sixteen channels, therefore, can be scanned during the $\overline{\text{ROMEN}}$ high cycle of any SPC. During each channel scan, the bus is gated to transmit the ROM address to latches on the ROM circuit board. The address is sent in two bytes. After a brief delay of one-half μs, the bus is gated to return the requested ROM data to the same SPC channel. This data is then latched on the SPC channel card. This scheme is very straightforward. It exchanges reduced interconnect wiring for additional logic circuits.

To minimize interconnect wiring when using a unified bus structure, the SPC control logic would probably be configured on a per channel basis. The COP microcontroller,



*Note: Selected 81LS95 output enabled during this interval. Output is current ROM address code from SPC.

FIGURE 12. Multichannel Timing Diagram



I: SPC about to output the next ROM address. Address will remain valid for remainder of the cycle

II: Valid ROM data must be available to SPC shortly after this point

III: Cycle ends, new cycle begins immediately

FIGURE 13. MM54104 SPC Speech Memory Cycle Timing

once again, is a logical choice for this function. The COP controller initiates and assembles a group of fixed messages. Because of general similarities between the various messages, phrase strings are used to construct each finished message. Also, the circuit in *Figure 14* allows one message to contain a non-fixed message—a telephone number. The COP controller reads a group of program switches or receives a down-loaded number from the switching system's central processor. It then inserts this number into the appropriate place during the synthesis of the following typical message—"The number you are calling has been changed. The new number is 555-3434". The ROM library in this case contains the phrases required for message construction and the data needed to synthesize the name of each decimal digit. The library could also contain the names of the teen digit pairs, and the words "hundred" and "thousand". These would be used to synthesize the words "thirteen hundred" or "two thousand", etc.

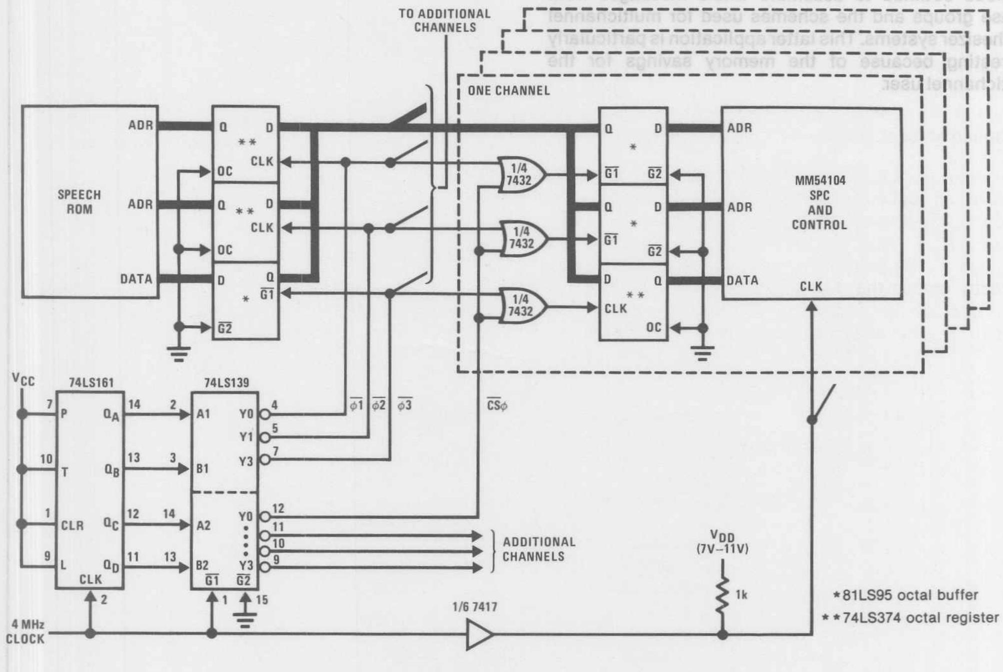


FIGURE 14. Multichannel Synthesizer with Unified Bus

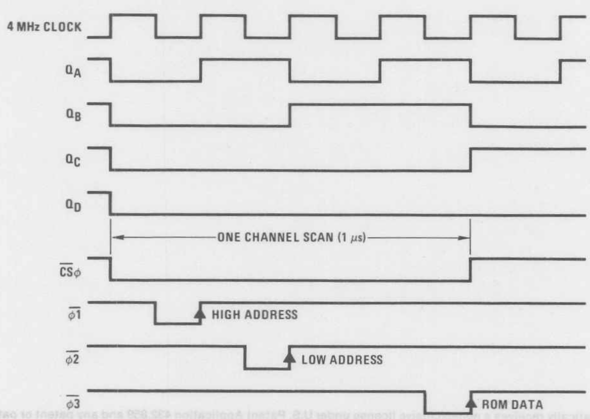


FIGURE 15. Multichannel (Unified Bus) Timing Diagram

AN-252 Speech Synthesis

SUMMARY

This application note describes some of the versatility and flexibility of the National Semiconductor DIGITALKER™ System. This system provides low cost speech and tone synthesis for products ranging from consumer items to computers. It provides a reliable alternative to mechanical systems (i.e., tape decks) without sacrificing voice quality. Also described in this note are a few of the most popular circuit arrangements possible with the DIGITALKER™. Of particular interest are the methods outlined to assemble whole messages from phrase groups and the schemes used for multichannel synthesizer systems. This latter application is particularly interesting because of the memory savings for the multichannel user.

REFERENCES

1. Morris, Dennis E. and Weinrich, David W., *A New Speech Synthesis Chip Set,* IEEE International Conference on Acoustics, Speech and Signal Processing, 1980.
2. Mozer, Forrest, *Method and Apparatus for Speech Synthesizing,* Pending US Patent.
3. Weinrich, David W., *A Speech Synthesis Chip Set Using Compression Techniques,* Electronics, April 10, 1980.

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Section 14

Appendices/ Physical Dimensions

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Section Contents

For additional information on Linear Products, see National Semiconductor's Linear Applications Handbook.

I. RELIABILITY vs. QUALITY

The words "reliability" and "quality" are often used interchangeably, as though they connoted identical facets of a product's merit. But reliability and quality are different, and IC users must understand the essential difference between the two concepts in order to properly evaluate which of National's extended screening programs, A+ or B+ will offer the most cost effective product improvement for his application.

QUALITY

The concept of QUALITY gives us information about the population of faulty IC devices among good devices, and generally relates to the number of faulty devices that arrive at a user's plant. Looked at in another way, quality then relates to the number of faulty IC's that escape detection at the IC vendor's plant.

At National, it is the charter of the Quality Control (QC) Operation to continually monitor and reduce the number of faulty IC's that escape detection. QC does this by testing the outgoing parts on an Acceptance Quality Level (AQL) basis.[1] The tighter the AQL testing, the more difficult it becomes for a defective part to escape detection, thus the quality of the shipped product increases.

RELIABILITY

The concept of RELIABILITY, on the other hand, refers to how well a part that is initially good will withstand its environment. *Reliability cannot be tested into a device.* Reliability is principally a function of device design, die size, power dissipation, assembly methods and material, etc. Still there are tests and procedures that an IC vendor can implement which will subject the IC to stress in excess of what it will endure in actual use, which will eliminate marginal, short-life parts.

On this basis, it is easily seen that it is possible that high quality IC's may, in fact, have low reliability, while low quality IC's may have high reliability. The object of extended screening programs is: (1) to enhance the quality by reducing the population of faulty devices among good devices and by so doing, eliminate the costly requirement of incoming tests by the user, and (2) provide maximum long term reliability minimizing equipment down-time, costly repairs and maintenance.

II. QUALITY SAVES YOU MONEY

When an IC vendor specifies 100% final testing of his parts then, in theory, every shipped part should be a good part. However, in any population of mass-produced items there does exist a small percentage of defective parts.

One of the best ways to reduce the number of such faulty parts is, simply, to retest the parts prior to shipment. Thus, if there is a one percent chance that a bad part will escape detection initially, retesting the parts reduces that probability to only 0.01 percent. This is exactly what tightening of the outgoing AQL level achieves.

WHAT IS AQL?

A good example of savings which can be achieved by taking advantage of tighter AQL[1] inspection levels is illustrated as follows:

> Assume a system uses 100 devices of a certain type which are procured to a 1% AQL level, and no incoming inspection/testing is done by the user. Statistically it can be shown that the number of systems that will require rework will be 80% of all systems manufactured! If enough devices are purchased to manufacture 100 systems (10,000 devices) and the cost to trouble shoot and repair each system is $30.00, the total cost of repair will be $2,400 (80% of 100 systems at $30.00 each).

Thus, the need for some preliminary component screening prior to system assembly becomes obvious. However, if the same devices are procured to a 0.14% AQL level, which is seven times tighter than originally assumed, it can be shown that the number of systems requiring rework is reduced by a factor of four, *without the need for incoming inspection.*

Thus, on a 100 system basis, 20 systems will require repair at $30.00 per system, or a total of $600.00. A savings of $1,800 is realized, and the user need not invest in expensive capital equipment, procedures, and paper work.

On a "savings per device" basis, this is a savings of 18¢ per device. Indeed, *Quality saves you money!*

This is the value added by the A+ and B+ Linear programs.

III. RELIABILITY SAVES YOU MONEY

With the increased population of integrated circuits in modern electronics systems has come an increased concern with IC failures. And rightly so, for at least two major reasons. First, the effect of component reliability on system reliability can be quite dramatic. For example, suppose that you, as a system manufacturer, were to choose an IC that is 99% reliable. You would find that if your system used only 70 such IC's the overall reliablility of the system's IC portion would be only 50%.

In other words, one out of every two systems in the field would fail. The result? A system that is very costly to produce, costly to maintain, and probably very difficult to sell.

Second, whether the system is large or small you cannot afford unnecessary maintenance costs. Not only have labor, repair and rework costs risen – and promise to continue to rise – but also, field replacement may be prohibitively expensive or impossible. If you ship a system that contains a marginally performing IC, and that IC later fails in the field, the cost of repair and replacement may be literally hundreds of times more than the cost of the failed IC itself.

(1) AQL testing is not to be confused with "in process" or electrical parameter testing in the normal product flow. All National products are 100% tested for electrical data sheet parameters.

IV. IMPROVING THE RELIABILITY OF SHIPPED PARTS

As was previously mentioned, reliability, in the true sense cannot be tested into a product. The most important factors that affect reliability are design, construction, materials and the assembly method. However, many of these can be examined and monitored by testing. As a matter of routine, National frequently performs 1000 hour burn-in life test and accelerated life tests to continually guarantee the quality and reliability of the linear product which is being shipped to customers. For example, the quality of the die attach for voltage regulators can be monitored by observing the thermal characteristics associated with "pulse loading" the regulator. This is a technique which National Linear pioneered over 10 years ago and still performs on a 100% basis on three terminal regulators at no additional cost to the user. Many such tests, including destructive and non-destructive wire bond pull tests are a matter of routine with National.

Further, in any test of reliability, the weaker parts will fail first. Stress tests will accelerate, or shorten the time of failure of the weak parts. Because the stress test causes weak parts to fail prior to shipment, the population of shipped parts will in fact demonstrate a higher reliability.

One of, if not the most effective screening procedures in the Semiconductor industry, is the use of a burn-in to stress and accelerate the failure of weak parts.

Thus, burn-in screen plus the tightened AQL outgoing testing, is the key to the A+ Linear Program.

QUALITY AND RELIABILITY PROGRAMS FOR MOLDED LINEAR PRODUCTS

One concern, with regard to quality and reliability in molded plastic products, is the problem of thermal intermittents. This problem first came to light in 1970 and plagued all semiconductor manufacturers. Since that time considerable efforts have been focused on improving lead bonding and lead frames to make them stronger and more reliable as well as improvements in the package molding material itself.

To better understand the problems a brief discussion of thermal intermittents is in order.

Because wires and bonds are completely imbedded in plastic, molded integrated circuits are extremely rugged devices. They can survive mechanical shock and vibration conditions which would literally tear the bonds and wires to pieces in a cavity type package. However, the non-cavity construction does present a unique problem. Sould a bond fracture or a wire break for some reason, the broken bond will remain in contact as long as the surrounding encapsulant continues to exert a compressive force on the bond. However, as the temperature increases, the compressive forces tend to relax due to the thermal mismatches between the lead frame, die, wires and the plastic.

Ultimately, if a high enough temperature is reached, the broken bond will separate, causing an electrical discontinuity. The phenomenon is frequently reversible, that is, as temperature decreases, electrical continuity is restored. This type of discontinuity is commonly referred to as a THERMAL INTERMITTENT OPEN. If electrical continuity does not return when the package temperature returns to ambient, then a permanent open has occurred.

If such defects occur during the manufacturing cycle of the device, and are not screened out by the manufacturer's testing sequence or by some screening test imposed by the user, they will show up as infant mortality failures in the user's equipment. If they occur during the user's equipment manufacturing cycle (due to solder heat exposure, for example) they will also show up as infant mortality failure.

The best way to screen for this phenomenon is to perform temperature cycling and "Hot Rail" testing after the device has been manufactured. The temperature cycling will stress the package mechanically to force the intermittent to occur if such a failure exists. The "Hot Rail" testing is performed to determine the functionality of the device at 100°C to ensure there are no open bonds at the worst case condition.

NATIONAL'S B+ LINEAR PROGRAM GETS IT ALL TOGETHER

We have stated that the B+ program improves both the quality and reliability of National's molded integrated circuits, and pointed out the difference between those two concepts. Now, how do we bring them together? The answer is in the B+ program processing, which is a continuum of stress and double testing. With the exception of the final QC inspection, which is a tightened sample program, *all steps of the B+ process are performed on 100% of the parts.* The following flow chart shows how we do it, step by step.

EPOXY B PROCESSING FOR ALL MOLDED PARTS –
At National, all molded semiconductors, including IC's have been built by this process for some time. All processing steps, inspections and QC monitoring are designed to provide highly reliable products. (Reliability reports are available that give, in detail, the background of Epoxy B, the reason for its selection at National and reliability data that proves its success.)

SIX HOUR, 150°C BAKE –
This stress places the die bond and all wire bonds into a combined tensile and shear stress mode, and helps eliminate marginal bonds and electrical connections.

FIVE TEMPERATURE CYCLES (0°C to 100°C)
Exercising the circuits over a 100°C temperature range further stresses the bonds and eliminates marginal bonds missed during the bake.

ELECTRICAL TESTING
These room-temperature functional and parametric tests are the normal final tests through which all National products pass.

HIGH TEMPERATURE (100°C) FUNCTIONAL ELECTRICAL TEST –
A high temperature test such as this with voltages applied places the die under the most severe stress possible. The test is actually performed at 100°C – 30°C higher than the commercial ambient limit. *All devices are thoroughly exercised at the 100°C ambient.* (Even though Epoxy B processing has virtually eliminated thermal intermittents, we perform this test to ensure against even the remote possibility of such a problem.)

100% DC FUNCTIONAL AND PARAMETRIC TESTS –
This is the second time that room-temperature functional and parametric tests are performed to National data sheet electrical limits.

TIGHTER-THAN-NORMAL QC INSPECTION PLANS –
Most vendors sample inspect outgoing parts to a 0.65% (or in some cases a 1%) AQL. When you specify the B+ program, however, not only do we sample your parts to a 0.28% AQL for all data sheet dc parameters, but they receive a 0.14% AQL for functionality as well. (Functional failures – not parameter shifts – cause most system failures.) Thus, the five to seven-times tightening of the AQL procedure gives a substantially higher quality to your B+ parts. And you can rely on the integrity of your received IC's without incoming tests at your facility.

SHIP PARTS

Here are the QC Procedures used in our B+ test program:

TEST	TEMPERATURE	AQL
Electrical Functionality	25°C	0.14%
Parametric, dc	25°C	0.28%
Major Mechanical	25°C	0.25%
Minor Mechanical	25°C	1%

NATIONAL'S A+ LINEAR PROGRAM – THE ULTIMATE IN QUALITY AND RELIABILITY

National has combined the successful B+ program with the Military/Aerospace processing specifications and provides the A+ program as the best cost-effective approach to maximum quality and reliability on molded devices. The following flow chart shows how we do it step by step. *The major difference between B+ and the A+ is the burn-in associated with the A+ program.*

SEM –
Randomly selected wafers are taken from production regularly and subjected to SEM analysis.

EPOXY B SEAL –
At National, all molded semiconductors, including IC's have been built by this process for some time. All processing steps, inspections and QC monitoring are designed to provide highly reliable products.

SIX HOUR, 150°C BAKE –
This stress places the die bond and all wire bonds into a combined tensile and shear stress mode, and helps eliminate marginal bonds and electrical connections.

FIVE TEMPERATURE CYCLES (0°C to 100°C) –
Exercising the circuits over 100°C temperature range further stresses the bonds and eliminates any marginal bonds missed during the bake.

ELECTRICAL TESTING
These room-temperature functional and parametric tests are the normal final tests through which all National products pass.

BURN-IN TEST –
Devices are stressed at maximum operating conditions to eliminate marginal devices. Test is performed per MIL-STD-883A, Method 1015.1.

HIGH TEMPERATURE (100°C) FUNCTIONAL ELECTRICAL TEST –
A high temperature test with voltages applied places the die under the most severe stress possible. The test is actually performed at 100°C – 30°C higher than the commercial ambient limit. *All devices are thoroughly exercised at the 100°C ambient.*

100% DC FUNCTIONAL AND PARAMETRIC TESTS –
This is the second time that room-temperature functional and parametric tests are performed to National data sheet electrical limits.

TIGHTER-THAN-NORMAL QC INSPECTION PLANS –
Most vendors sample inspect outgoing parts to a 0.65% (or in some cases a 1%) AQL. When you specify the A+ program, however, not only do we sample your parts to a 0.28% AQL for all data sheet dc parameters, but they receive 0.14% AQL for functionality as well. (Functional failures – not parameter shifts beyond spec – cause most system failures.) Thus, the five- to seven-times tightening of the sampling AQL procedure gives a substantially higher quality to your A+ parts. And you can rely on the integrity of your received IC's without incoming tests at your facility.

SHIP PARTS

Here is the QC procedure used in our A+ test program:

TEST	TEMPERATURE	AQL*
Electrical Functionality	25°C	0.14%
Parametric, dc	25°C	0.28%
Major Mechanical	25°C	0.25%
Minor Mechanical	25°C	1%

* Note: New AQL's will be in effect June '82. Consult your local Sales Office.

QUALITY AND RELIABILITY PROGRAM FOR HERMETIC PACKAGED LINEAR PRODUCT

An improved quality and reliability program, similar to that which is available for molded products, is also available for commercial temperature range hermetic packages.

There is one major difference between the molded A+ program and the hermetic package A+ program. Since there is no material in contact with the wire bonds in a hermetic package, the need for "Hot Rail" functional testing at 100°C is of no benefit and therefore not included. The devices are electrically tested (100%), then burned-in and then 100% electrically tested again. If a bond failure were to occur during burn-in, there is no material in contact with the bond (such as plastic in the case of molded products) that would tend to restore the bond when the device cooled. The result is that a weak bonding wire, once broken causing an "open" will remain open and be caught at the second 100% electrical screening.

The A+ hermetic package program flow chart is shown below.

NATIONAL'S A+ PROGRAM FLOW CHART FOR HERMETIC PACKAGES

National has extended the successful B+ and A+ molded product programs to hermetic packages. We believe this to be the best practical approach to maximum quality and reliability for commercial devices. The following flow chart explains this program step by step.

SEM –
Randomly selected wafers are taken from production regularly and subjected to SEM analysis.

ASSEMBLY AND SEAL –
All processing steps, inspections, and QC monitoring are designed to provide highly reliable products. MIL-STD-883 is the guideline by which all linear products are manufactured.

SIX HOUR, 150°C BAKE –
This stress places the die bond and all wire bonds into a combined tensile and shear stress mode, and helps eliminate marginal bonds and electrical connections.

FIVE TEMPERATURE CYCLES (0°C to 100°C) –
Exercising the circuits over 100°C temperature range further stresses the bonds and eliminates any marginal bonds missed during the bake.

ELECTRICAL TESTING –
Every device will be 100% tested at 25°C for functional and dc parameters.

BURN-IN –
Devices are stressed at maximum operating conditions to eliminate marginal devices. Test is performed per MIL-STD-883A method 1015.1.

DC FUNCTIONAL AND PARAMETRIC TESTS
These room temperature functional and parametric tests are the normal, final tests through which all National products pass. This is the second time 100% electrical testing is performed.

TIGHTER-THAN-NORMAL QC INSPECTION PLANS –
Most vendors sample inspect outgoing parts to a 0.65% (or in some cases a 1%) AQL. When you specify the A+ program, however, not only do we sample your parts to a 0.28% AQL for all data sheet dc parameters, but they receive 0.14% AQL for functionality as well. (Functional failures – not parameter shifts beyond spec – cause most system failures.) Thus, the five- to seven-times tightening of the sampling procedure gives the highest quality to your A+ parts. And you can rely on the integrity of your received IC's without incoming tests at your facility.

SHIP PARTS

Here are the QC Sampling plans used in our A+ test program:

TEST	TEMPERATURE	AQL*
Electrical Functionality	25°C	0.14%
Parametric, dc	25°C	0.28%
Major Mechanical	25°C	0.25%
Minor Mechanical	25°C	1%

* Note: New AQL's will be in effect June '82. Consult your local Sales Office.

PROCESS FLOW	MOLDED N PACKAGE		HERMETIC H AND J PACKAGE
DESCRIPTION	A+	B+	A+
100% High Temperature Storage – 6 Hours @ 150°C	X	X	X
100% Temperature Cycling, 5 Cycles – 0° to 100°C	X	X	X
100% Burn-in per MIL-STD-883A, Method 1015.1	X		X
100% High Temperature Test for Functionality at 100%	X	X	
100% DC Functional parametric Tests at Room Temperature	X	X	X
Tightened QC Inspection Plan	X	X	X

Q.C. SAMPLE PLAN

TEST	TEMPERATURE	AQL
Electrical Functionality	25°C	0.14%
Parametric, dc	25°C	0.28%
Major Mechanical	25°C	0.25%
Minor Mechanical	25°C	1%

A synopsis of the A+ and B+ programs is shown on the preceding page. Also shown below is a listing of some of the most popular devices which are processed to this program and are readily available.

For more information about this, or other National Linear programs, please contact your local representative.

LF13331	LM1458	LM307	LM324	LM3900	LM723C
LF13741	LM1496	LM308	LM3301	LM393	LM725C
LF347	LM2900	LM3080	LM3302	LM4250C	LM733
LF351	LM2901	LM310	LM339	LM555C	LM741C
LF353	LM2902	LM311	LM3401	LM556	LM747C
LF355	LM2903	LM318	LM346	LM566	LM748C
LF356	LM2904	LM319	LM348	LM567	
LF357	LM301A		LM358	LM709C	
			LM360		
			LM361		

SUMMARY

The B+ program, although offering improved Reliability attendent with additional stress testing, is primarily aimed at enhancing the quality of incoming devices and thus eliminating the need for incoming testing by the user. This program offers significant cost savings to the user and eliminates the need for the investment in expensive capital equipment to perform this testing. For all general, but relatively non-critical circuits, the B+ program is the most cost-effective.

The A+ program incorporates not only the quality inherent with B+ program, but also adds burn-in for the ultimate in Reliability testing. The A+ program is recommended as the most cost-effective program for components which the user deems to be the most critical in his system.

Both programs, A+ and B+, incorporate high temperature stress, double testing, and very tight out-going AQL QC proceedures.

ORDER INFORMATION

Any of the devices listed molded or hermetic package, may be ordered to the A+ program simply by adding the term A+ behind the device number, with a slash (/) in between.

Examples:
LM348N/A+
LF356H/A+
LM1458J/A+

Likewise, any molded (N package) product may be ordered to the B+ program by adding the term B+ behind the device number.

Examples:
LF351N/B+
LM741CN/B+

For devices not listed, contact your local National Semiconductor Sales office for information on availability and ordering information.

National Semiconductor

MIL-STD-883

Mil-Standard-883 is a Test Methods and Procedures Document for Microelectronic Circuits. It was derived from MIL-S-19500, MIL-STD-750, and MIL-STD-202C for transistors and diodes at about the time that National Semiconductor Corporation was entering the military microelectronics market. As a result, our standard quality control operations are written around MIL-STD-883. The bonding control, visual inspections, and post seal screening requirements set forth by 883 (as well as added control procedures beyond the requirements of 883) have been part of National's quality control procedures almost from the start. Our Quality Assurance Procedures Manual is available upon request.

We offer a complete line of linear/883 (Class B) products as standard, off-the-shelf items. Special Linear/883 data sheets have been prepared to reflect this capability. They show process flow, electrical parameters, end of test criteria, and test circuits. We save you the problem of specifying test and inspection procedures, and offer significant cost savings by having an off-the-shelf, "to the letter" 883 program. In addition, we will test any of our integrated circuits to any class of MIL-STD-883.

MIL-M-38510

MIL-M-38510 specifies the general requirements for supplying microcircuits. These are; product assurance, which includes screening and quality conformance inspection; design and construction; marking; and workmanship. The screening and quality conformance inspection are conducted in accordance with MIL-STD-883.

Screening

All microcircuits delivered in accordance with MIL-M-38510 must have been subjected to, and passed all the screening tests detailed in Method 5004 of MIL-STD-883 for the type of microcircuit and product assurance level.

The device electrical and package requirements of MIL-M-38510 are detailed by a device specification referred to as a slash sheet. Each slash sheet defines the microcircuit electrical performance and mechanical requirements. Each device listed on a slash sheet is referred to as a slash number and the group of the microcircuits contained on a slash sheet is defined as a family of devices. The device may be Class B or C as defined by MIL-STD-883, Method 5004 and 5005. Three lead finishes are allowed by the slash sheet, pot solder dip, bright tin plate, and gold plate.

The MIL-M-38510 specs for standard linear devices require 100% DC testing at 25°C, −55°C and +125°C. AC testing is performed at +25°C. The electrical parameters specified are tighter than the normal data sheet guaranteed limits. Additionally, MIL-M-38510 requires device traceability, extensive documentation and closely matched maintenance.

Quality Conformance

Quality conformance inspection is conducted in accordance with the applicable requirements of Group A, (electrical test), Group B and C, (environmental test) of Method 5005, MIL-STD-883. These tests are conducted on a sample basis with Group A performed on each sublot, Group B on each lot, and Group C as specified (usually every three months).

To supply devices to MIL-M-38510, the IC manufacturer must qualify the devices he plans to supply to the detail specifications. Qualification consists of notifying the qualifying activity of one's intent to qualify to MIL-M-38510. After passing comprehensive audits of facilities and documentation systems, the IC manufacturer will subject the device to and demonstrate that they satisfy all of the Group A, B, and C requirements of Method 5005 of MIL-STD-883 for the specified classes and types of IC. The qualification tests shall be monitored by the qualifying agency. Finally the IC manufacturer shall prepare and submit qualification test data to the qualifying agency. Groups A, B, and C inspections then shall be performed at intervals no greater than three months.

The purpose of qualification testing is to assure that the device and lot quality conform to certain standard limits. In effect, lot qualification tests tend to ensure that once a particular device type is demonstrated to be acceptable, it's production, including materials, processing, and testing will continue to be acceptable. These limits are specified in MIL-STD-883 in terms of LTPD's (Lot Tolerance Percent Defective) for the various qualification test sub-groups. Qualification testing is performed on a sample of devices which are chosen at random from a lot of devices that has satisfactorily completed the screening of Method 5004 must be performed on each device, i.e. on a 100% basis as opposed to qualification testing (Method 5005) which occurs on a random sample basis.

In summary, the entire purpose of MIL-M-38510 and MIL-STD-883 is to provide the military, through its contractors with standard devices.

We at National Semiconductor have supplied and are supplying devices to the MIL-M-38510 specifications. To order a MIL-M-38510 microcircuit, specify the following:

For example; to specify an LM741 in a DIP processed to the requirements of MIL-M-38510, Class B, with gold plated leads, specify M-38510/10101BCC.

MM38510/	XXX	XX	X	X	X
Specifies the General Requirements of MIL-M-38510	Slash Sheet No.	Device Type	Device Class	Case Outline	Lead Finish

Device No.	Function	National Direct Replacement
FAIRCHILD		
μA101AHM	General Purpose Op Amp	LM101AH
μA102HM	Voltage Follower	LM102H
μA107HM	General Purpose Op Amp	LM107H
μA108AHM	Super Beta Op Amp	LM108AH
μA108HM	Super Beta Op Amp	LM108H
μA110HM	Voltage Comparator	LM110H
μA111HM	Voltage Comparator	LM111H
μA111RM	Voltage Comparator	LM111J-8
μA201AHM	General Purpose Op Amp	LM201AH
μA201AT	General Purpose Op Amp	LM201AN
μA207HM	General Purpose Op Amp	LM207H
μA208AHM	Super Beta Op Amp	LM208AH
μA208HM	Super Beta Op Amp	LM208H
μA301AHC	General Purpose Op Amp	LM301AH
μA301ATC	General Purpose Op Amp	LM301AN
μA302HC	Voltage Follower	LM302H
μA307HC	General Purpose Op Amp	LM307H
μA307TC	General Purpose Op Amp	LM307N
μA308AHC	Super Beta Op Amp	LM308AH
μA308HC	Super Beta Op Amp	LM308H
μA309KC	5 Volt Regulator	LM309KC
μA310HC	Voltage Follower	LM310H
μA311HC	Voltage Comparator	LM311H
μA311R	Voltage Comparator	LM311J-8
μA311TC	Voltage Comparator	LM311N
μA324PC	Quad Op Amp	LM324N
μA339APC	Quad Comparator	LM339AN
μA339PC	Quad Comparator	LM339N
μA376TC	Voltage Regulator	LM376N
μA555HC	Single Timing Circuit	LM555CH
μA555HM	Single Timing Circuit	LM555H
μA555TC	Single Timing Circuit	LM555CN
μA556PC	Dual Timing Circuit	LM556CN
μA709AHM	High Performance Op Amp	LM709AH
μA709HC	High Performance Op Amp	LM709CH
μA709HM	High Performance Op Amp	LM709H
μA709PC	High Performance Op Amp	LM709CN
μA709TC	High Performance Op Amp	LM709CN-8
μA710HC	High Speed Differential Comparator	LM710CH
μA710HM	High Speed Differential Comparator	LM710H
μA710PC	High Speed Differential Comparator	LM710CN
μA711HC	Dual Comparator	LM711CH
μA711HM	Dual Comparator	LM711H
μA711PC	Dual Comparator	LM711CN
μA723DC	Precision Voltage Regulator	LM723CJ
μA723DM	Precision Voltage Regulator	LM723J
μA723HC	Precision Voltage Regulator	LM723CH
μA723HM	Precision Voltage Regulator	LM723H
μA723PC	Precision Voltage Regulator	LM723CN
μA725AHM	Instrumentation Op Amp	LM725AH
μA725HC	Instrumentation Op Amp	LM725CH
μA725HM	Instrumentation Op Amp	LM725H
μA733HC	Differential Video	LM733CH
μA733HM	Differential Video	LM733H
μA741AHM	Frequency Compensated Op Amp	LM741AH
μA741DC	Frequency Compensated Op Amp	LM741CJ-14
μA741EHC	Frequency Compensated Op Amp	LM741EH
μA741HC	Frequency Compensated Op Amp	LM741CH
μA741HM	Frequency Compensated Op Amp	LM741H
μA741PC	Frequency Compensated Op Amp	LM741CN-14
μA741RC	Frequency Compensated Op Amp	LM741CJ
μA741TC	Frequency Compensated Op Amp	LM741CN
μA746PC	Chroma Demodulator	LM746N
μA747AHM	Dual Frequency Compensated Op Amp	LM747AH
μA747EHC	Dual Frequency Compensated Op Amp	LM747EH
μA747HC	Dual Frequency Compensated Op Amp	LM747CH
μA747HM	Dual Frequency Compensated Op Amp	LM747H
μA747PC	Dual Frequency Compensated Op Amp	LM747CN
μA748HC	Op Amp	LM748CH
μA748HM	Op Amp	LM748H
μA748TC	Op Amp	LM748CN
μA760HC	High Speed Differential Comparator	LM760CH
μA796HC	3-Terminal Positive Voltage Regulator	LM1496H
μA796PC	3-Terminal Positive Voltage Regulator	LM1496M
μA798HM	Dual Op Amp	LM358H
μA1558HM	Dual Internally Compensated Op Amp	LM1558H

Device No.	Function	National Direct Replacement
FAIRCHILD (Continued)		
μA2901PC	Dual Internally Compensated Op Amp	LM2901N
μA3046DC	Transistor Array	LM3046N
μA3064PC	TV Automatic Fine-Tuning Circuit	LM3064N
μA3075PC	FM IF Limiter/Detector/Audio Preamplifier	LM3075N
μA3086PC	Transistor Array	LM3086N
μA3301P	Quad Single Supply Amplifier	LM3301N
μA3302P	Quad Comparator	LM3302N
μA3401P	Quad Single Supply Amplifier	LM3401N
μAF111HM	Voltage Comparator	LF111H
μAF211HM	Voltage Comparator	LF211H
μAF311HC	Voltage Comparator	LF311H
MOTOROLA		
LF155AH	Monolithic JFET Op Amp	LF155AH
LF155H	Monolithic JFET Op Amp	LF155H
LF156AH	Monolithic JFET Op Amp	LF156AH
LF156H	Monolithic JFET Op Amp	LF156H
LF157AH	Monolithic JFET Op Amp	LF157AH
LF157H	Monolithic JFET Op Amp	LF157H
LF355AH	Monolithic JFET Op Amp	LF355AH
LF355H	Monolithic JFET Op Amp	LF355H
LF355N	Monolithic JFET Op Amp	LF355N
LF356AH	Monolithic JFET Op Amp	LF356AH
LF356H	Monolithic JFET Op Amp	LF356H
LF356N	Monolithic JFET Op Amp	LF356N
LM117H	3-Terminal Adj. Positive Regulator	LM117H
LM117K	3-Terminal Adj. Positive Regulator	LM117K
LM123K	Positive Voltage Regulator	LM123K
LM317H	3-Terminal Adj. Positive Regulator	LM317H
LM317K	3-Terminal Adj. Positive Regulator	LM317K
LM317T	3-Terminal Adj. Positive Regulator	LM317T
MC1303P	Dual Stereo Preamplifier	LM1303N
MC1310P	FM Stereo Demodulator	LM1310N
MC1408L6	8-Bit Multiplying D/A Converter	LM1408J-6
MC1408L7	8-Bit Multiplying D/A Converter	LM1408J-7
MC1408L8	8-Bit Multiplying D/A Converter	LM1408J-8
MC1408P6	8-Bit Multiplying D/A Converter	LM1408N-6
MC1408P7	8-Bit Multiplying D/A Converter	LM1408N-7
MC1408P8	8-Bit Multiplying D/A Converter	LM1408N-8
MC1414L	Dual Differential Comparator	LM1414J
MC1414P	Dual Differential Comparator	LM1414N
MC1496G	Balanced Modulator-Demodulator	LM1496H
MC1496P	Balanced Modulator-Demodulator	LM1496N
MC1508L8	8-Bit Multiplying D/A Converter	LM1508D-8
MC1514L	Dual Differential Comparator	LM1514J
MC1596G	Blanced Modulator-Demodulator	LM1596H
MC1710AG	Differential Comparator	LM710AH
MC1710CG	Differential Comparator	LM710CH
MC1710CP	Differential Comparator	LM710CN
MC1710G	Differential Comparator	LM710H
MC1711CG	Dual Differential Comparator	LM711CH
MC1711CP	Dual Differential Comparator	LM711CN
MC1711G	Dual Differential Comparator	LM711H
MC1723CL	Adj. Positive or Negative Volt. Regulator	LM723CJ
MC1723CP	Adj. Positive or Negative Volt. Regulator	LM723CN
MC1723L	Adj. Positive or Negative Volt. Regulator	LM723J
MC1733CG	Differential Video Amp	LM733CH
MC1733CP	Differential Video Amp	LM733CN
MC1733G	Differential Video Amp	LM733H
MC1741CG	General Purpose Op Amp	LM741CH
MC1741CL	General Purpose Op Amp	LM741CJ-14
MC1741CP1	General Purpose Op Amp	LM741CN
MC1741CP2	Generla Purpose Op Amp	LM741CN-14
MC1741G	General Purpose Op Amp	LM741H
MC1741L	General Purpose Op Amp	LM741J-14
MC1741U	General Purpose Op Amp	LM741J
MC1747CG	Dual MC1741 Op Amp	LM747CH
MC1747CL	Dual MC1741 Op Amp	LM747CJ
MC1747CP2	Dual MC1741 Op Amp	LM747CN
MC1747G	Dual MC1741 Op Amp	LM747H
MC1747L	Dual MC1741 Op Amp	LM747J
MC1748CG	General Purpose Op Amp	LM748CH
MC1748CP1	General Purpose Op Amp	LM748CN
MC1748CU	General Purpose Op Amp	LM748CJ
MC1748G	General Purpose Op Amp	LM748H

MOTOROLA (Continued)

MC1748U	General Purpose Op Amp	LM748J
MC2901P	Quad Comparator	LM2901N
MC2902P	Quad Op Amp	LM2902N
MC3301P	Quad Op Amp	LM3301N
MC3302P	Quad Comparator	LM3302N
MC3401P	Quad Op Amp	LM3401N
MC34001AP		LF411CN
MC34022BP		LF412ACN
MC78XXCK	Positive Voltage Regulator	LM78XXCK
MC78XXCT	Positive Voltage Regulator	LM78XXCT
MC78LXXACG	Positive Voltage Regulator	LM78LXXACH
MC78LXXACP	Positive Voltage Regulator	LM78LXXACZ
MC78LXXCG	Positive Voltage Regulator	LM78LXXCH
MC78LXXCP	Positive Voltage Regulator	LM78LXXCZ
MC79XXCK	Negative Voltage Regulator	LM79XXCK
MC79XXCT	Negative Voltage Regulator	LM79XXCT
MC79LXXACP	Negative Voltage Regulator	LM79LXXACZ
MC79LXXCP	Negative Voltage Regulator	LM79LXXCZ
MLM101AG	Gen. Purpose Adj. Op Amp	LM101AH
MLM101AU	Gen. Purpose Adj. Op Amp	LM101AJ
MLM107G	General Purpose Op Amp	LM107H
MLM107U	General Purpose Op Amp	LM107J
MLM108AG	Precision Op Amp	LM108AH
MLM108AU	Precision Op Amp	LM108AJ
MLM109G	Positive Voltage Regulator	LM109H
MLM110G	Unity Gain Op Amp	LM110H
MLM110U	Unity Gain Op Amp	LM110J-8
MLM111G	Voltage Comparator	LM111H
MLM111L	Voltage Comparator	LM111J
MLM111U	Voltage Comparator	LM111J-8
MLM124L	Quad Op Amp	LM124J
MLM124P	Quad Op Amp	LM124N
MLM139AL	Quad Comparator	LM139AJ
MLM139L	Quad Comparator	LM139J
MLM158G	Dual Op Amp	LM158H
MLM201AG	General Purpose Op Amp	LM201AH
MLM201API	General Purpose Op Amp	LM201AN
MLM207G	General Purpose Op Amp	LM207H
MLM207U	General Purpose Op Amp	LM207J
MLM208AG	Precision Op Amp	LM208AH
MLM208AL	Precision Op Amp	LM208AJ
MLM208AU	Precision Op Amp	LM208AJ-8
MLM208G	Precision Op Amp	LM208H
MLM208L	Precision Op Amp	LM208J
MLM208U	Precision Op Amp	LM208J-8
MLM209G	Positive Voltage Regulator	LM209H
MLM211G	Voltage Comparator	LM211H
MLM211L	Voltage Comparator	LM211J
MLM211U	Voltage Comparator	LM211J-8
MLM224L	Quad Op Amp	LM224J
MLM239AL	Quad Comparator	LM239AJ
MLM239L	Quad Comparator	LM239J
MLM258G	Dual Op Amp	LM258H
MLM301AG	General Purpose Op Amp	LM301AH
MLM301API	General Purpose Op Amp	LM301AN
MLM307G	General Purpose Op Amp	LM307H
MLM307PI	General Purpose Op Amp	LM307N
MLM307U	General Purpose Op Amp	LM307J
MLM308AG	Precision Op Amp	LM308AH
MLM308AL	Precision Op Amp	LM308AJ
MLM308API	Precision Op Amp	LM308AN
MLM308AU	Precision Op Amp	LM308AJ-8
MLM308G	Precision Op Amp	LM308H
MLM308L	Precision Op Amp	LM308J
MLM308PI	Precision Op Amp	LM308N
MLM308U	Precision Op Amp	LM308J-8
MLM309G	Positive Voltage Regulator	LM309H
MLM309K	Positive Voltage Regulator	LM309K
MLM310G	Unity Gain Op Amp	LM310H
MLM310PI	Unity Gain Op Amp	LM310N
MLM310U	Unity Gain Op Amp	LM310J-8
MLM311G	Voltage Comparator	LM311H
MLM311L	Voltage Comparator	LM311J
MLM311PI	Voltage Comparator	LM311N
MLM311U	Voltage Comparator	LM311J-8
MLM324L	Quad Op Amp	LM324J
MLM324P	Quad Op Amp	LM324N

MOTOROLA (Continued)

MLM339AL	Quad Comparator	LM339AJ
MLM339AP	Quad Comparator	LM339AN
MLM339L	Quad Comparator	LM339J
MLM339P	Quad Comparator	LM339N
MLM358G	Dual Op Amp	LM358H
MLM358PI	Dual Op Amp	LM358N
MLM565CP	Phase Locked Loop	LM565CN

PMI

OP-15FG		LF411ACH
OP-15GP		LF411CN
OP-15FP		LF411ACN
OP-15CH		LF411CH
PM108AJ	Operational Amplifier	LM108AH
PM108J	Operational Amplifier	LM108H
PM155AJ	JFET Input Op Amp	LF155AH
PM155J	JFET Input Op Amp	LF155H
PM156AJ	JFET Input Op Amp	LF156AH
PM156J	JFET Input Op Amp	LF156H
PM157AJ	JFET Input Op Amp	LF157AH
PM157J	JFET Input Op Amp	LF157H
PM208AJ	Operational Amplifier	LM208AH
PM208J	Operational Amplifier	LM208H
PM255J	JFET Input Op Amp	LF255H
PM256J	JFET Input Op Amp	LF256H
PM257J	JFET Input Op Amp	LF257H
PM308AJ	Operational Amplifier	LM308AH
PM308J	Operational Amplifier	LM308H
PM355AJ	JFET Input Op Amp	LF355AH
PM355J	JFET Input Op Amp	LF355H
PM356AJ	JFET Input Op Amp	LF356AH
PM356J	JFET Input Op Amp	LF356H
PM357AJ	JFET Input Op Amp	LF357AH
PM357J	JFET Input Op Amp	LF357H
PM725CJ	Operational Amplifier	LM725CH
PM725J	Operational Amplifier	LM725H
PM741CJ	Compensated Op Amp	LM741CH
PM741J	Compensated Op Amp	LM741H
PM747CJ	Dual Compensated Op Amp	LM747CH
PM747J	Dual Compensated Op Amp	LM747H
PM1558J	Dual Compensated Op Amp	LM1558H

SIGNETICS

µA709AT	Operational Amplifier	LM709AH
µA709CN	Operational Amplifier	LM709CN-8
µA709CN-14	Operational Amplifier	LM709CN
µA709CT	Operational Amplifier	LM709CH
µA709T	Operational Amplifier	LM709H
µA710CN-14	Differential Voltage Comparator	LM710CN
µA710CT	Differential Voltage Comparator	LM710CH
µA710T	Differential Voltage Comparator	LM710H
µA711CN	Dual Voltage Comparator	LM711CN
µA711CT	Dual Voltage Comparator	LM711CH
µA711K	Dual Voltage Comparator	LM711H
µA723CF	Precision Voltage Regulator	LM723CJ
µA723CL	Precision Voltage Regulator	LM723CH
µA723CN	Precision Voltage Regulator	LN723CN
µA723F	Precision Voltage Regulator	LM723J
µA723L	Precision Voltage Regulator	LM723H
µA733CN	Differential Video Amp	LM733CN
µA733CT	Differential Video Amp	LM733CH
µA733F	Differential Video Amp	LM733H
µA741CF	General Purpose Op Amp	LM741CJ-14
µA741CN	General Purpose Op Amp	LM741CN
µA741CN-14	General Purpose Op Amp	LM741CN-14
µA741CT	General Purpose Op Amp	LM741CH
µA741F	General Purpose Op Amp	LM741J-14
µA741T	General Purpose Op Amp	LM741H
µA747CN	Dual Op Amp	LM747CN
µA748CF	General Purpose Op Amp	LM748CJ
µA748CN	General Purpose Op Amp	LM748CN
µA748CT	General Purpose Op Amp	LM748CH
µA748F	General Purpose Op Amp	LM748J-14
µA748T	General Purpose Op Amp	LM748H
78XXCU	3-Terminal Positive Voltage Regulator	LM78XXCT
78XXDA	3-Terminal Positive Voltage Regulator	LM78XXCK
78LXXACS	3-Terminal Positive Voltage Regulator	LM78XXACZ

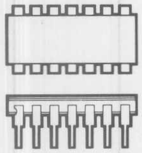
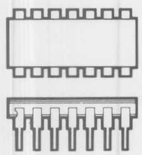
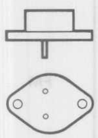
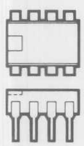
Device No.	Function	National Direct Replacement
SIGNETICS (Continued)		
78LXXADB	3-Terminal Positive Voltage Regulator	LM78LXXACH
78LXXCDB	3-Terminal Positive Voltage Regulator	LM78LXXCH
78LXXCS	3-Terminal Positive Voltage Regulator	LM78LXXCZ
79XXCU	3-Terminal Negative Voltage Regulator	LM79XXCT
79XXDA	3-Terminal Negative Voltage Regulator	LM79XXCK
LF155AT	Hi Performance JFET Input Op Amp	LF155AH
LF155T	Hi Performance JFET Input Op Amp	LF155H
LF156AT	Hi Performance JFET Input Op Amp	LF156AH
LF156T	Hi Performance JFET Input Op Amp	LF156H
LF157AT	Hi Performance JFET Input Op Amp	LF157AH
LF157T	Hi Performance JFET Input Op Amp	LF157H
LF255T	Hi Performance JFET Input Op Amp	LF255H
LF256T	Hi Performance JFET Input Op Amp	LF256H
LF257T	Hi Performance JFET Input Op Amp	LF257H
LF355AT	Hi Performance JFET Input Op Amp	LF355AH
LF355T	Hi Performance JFET Input Op Amp	LF355H
LF356AT	Hi Performance JFET Input Op Amp	LF356AH
LF356T	Hi Performance JFET Input Op Amp	LF356H
LF357AT	Hi Performance JFET Input Op Amp	LF357AH
LF357T	Hi Performance JFET Input Op Amp	LF357H
LM101AF	High Performance Amplifier	LM101AJ-14
LM101AT	High Performance Amplifier	LM101AH
LM107F	General Purpose Op Amp	LM107J-14
LM107T	General Purpose Op Amp	LM107H
LM108AF	Precision Op Amp	LM108AJ
LM108AT	Precision Op Amp	LM108AH
LM108F	Precision Op Amp	LM108J
LM108T	Precision Op Amp	LM108H
LM109DB	5 Volt Regulator	LM109H
LM111F	Voltage Comparator	LM111J
LM111T	Voltage Comparator	LM111H
LM119F	Dual Voltage Comparator	LM119J
LM119K	Dual Voltage Comparator	LM119H
LM124AF	Gen Purpose Single Supply Op Amp	LM124AJ
LM124F	Gen Purpose Single Supply Op Amp	LM124J
LM124N	Gen Purpose Single Supply Op Amp	LM124N
LM139AF	Quad Voltage Comparator	LM139AJ
LM139F	Quad Voltage Comparator	LM139J
LM193AT	Low Power Dual Voltage Comparator	LM193AH
LM193T	Low Power Dual Voltage Comparator	LM193H
LM201AF	High Performance Amplifier	LM201AJ-14
LM201AN	High Performance Amplifier	LM201AN
LM207F	General Purpose Op Amp	LM207J-14
LM207T	General Purpose Op Amp	LM207H
LM208AF	General Purpose Op Amp	LM208AJ
LM208AT	Precision Operational Amp	LM208AH
LM208F	Precision Operational Amp	LM208J
LM208T	Precision Operational Amp	LM208H
LM209DB	5 Volt Regulator	LM209H
LM211F	Voltage Comparator	LM211J
LM211T	Voltage Comparator	LM211H
LM219F	Dual Voltage Comparator	LM219J
LM219K	Dual Voltage Comparator	LM219H
LM224AF	Gen Purpose Single Supply Op Amp	LM224AJ
LM224AN	Gen Purpose Single Supply Op Amp	LM224AN
LM224F	Gen Purpose Single Supply Op Amp	LM224J
LM239AF	Quad Voltage Comparator	LM239AJ
LM239F	Quad Voltage Comparator	LM239J
LM258T	Gen Purpose Single Supply Op Amp	LM258H
LM293T	Low Power Dual Voltage Comparator	LM293H
LM301AF	High Performance Amplifier	LM301AJ-14
LM301AN	High Performance Amplifier	LM301AN
LM301AT	High Performance Amplifier	LM301H
LM307F	General Purpose Op Amp	LM307J-14
LM307N	General Purpose Op Amp	LM307N
LM307T	General Purpose Op Amp	LM307H
LM308AF	Precision Op Amp	LM308AJ
LM308AN	Precision Op Amp	LM308AN
LM308AT	Precision Op Amp	LM308AH
LM308F	Precision Op Amp	LM308J
LM308N	Precision Op Amp	LM308N
LM308T	Precision Op Amp	LM308H
LM309DA	5 Volt Regulator	LM309K
LM309DB	5 Volt Regulator	LM309H
LM311F	Voltage Comparator	LM311J
LM311N	Voltage Comparator	LM311N
LM311N-14	Voltage Comparator	LM311N-14

Device No.	Function	National Direct Replacement
SIGNETICS (Continued)		
LM311T	Voltage Comparator	LM311H
LM319F	Dual Voltage Comparator	LM319J
LM319K	Dual Voltage Comparator	LM319H
LM319N	Dual Voltage Comparator	LM319N
LM324AF	Gen Purpose Single Supply Op Amp	LM324AJ
LM324AN	Gen Purpose Single Supply Op Amp	LM324AN
LM324F	Gen Purpose Single Supply Op Amp	LM324J
LM324N	Gen Purpose Single Supply Op Amp	LM324N
LM339AF	Quad Voltage Comparator	LM339AJ
LM339AN	Quad Voltage Comparator	LM339AN
LM339F	Quad Voltage Comparator	LM339J
LM339N	Quad Voltage Comparator	LM339N
LM340XXDA	3-Terminal Positive Voltage Regulator	LM340KXX
LM340XXLL	3-Terminal Positive Voltage Regulator	LM340TXX
LM381AN	Dual Low Noise Preamplifier	LM381AN
LM381N	Dual Low Noise Preamplifier	LM381N
LM382N	Dual Low Noise Preamplifier	LM382N
LM387N	Dual Low Noise Preamplifier	LM387N
LM393AN	Low Power Dual Voltage Comparator	LM393AN
LM393AT	Low Power Dual Voltage Comparator	LM393AH
LM393N	Low Power Dual Voltage Comparator	LM393N
LM393T	Low Power Dual Voltage Comparator	LM393H
LM2901F	Quad Voltage Comparator	LM2901J
LM2901N	Quad Voltage Comparator	LM2901N
LM2903N	Low Power Dual Voltage Comparator	LM2903N
MC1408-7F	8-Bit Multiplying D/A Converter	LM1407J-7
MC1408-8F	8-Bit Multiplying D/A Converter	LM1408J-8
MC1408-7N	8-Bit Multiplying D/A Converter	LM1408N-7
MC1408-8N	8-Bit Multiplying D/A Converter	LM1408N-8
MC1496K	Balanced Modulator Demodulator	LM1496H
MC1496N	Balanced Modulator Demodulator	LM1496N
MC1596K	Balanced Modulator Demodulator	LM1596H
MC3302N	Quad Voltage Comparator	LM3302N
NE555T	Timer	LM555CH
NE555N	Timer	LM555CN
NE556N	Dual Timer	LM556CN
NE556F	Dual Timer	LM556J
NE565K	Phase Locked Loop	LM565CH
NE565N	Phase Locked Loop	LM565CN
NE566N	Function Generator	LM566CN
NE567T	Tone Decoder/Phase Locked Loop	LM567CH
NE567N	Tone Decoder/Phase Locked Loop	LM567CN
SE555T	Timer	LM555H
SE565K	Phase Locked Loop	LM565H
SE567T	Tone Decoder/Phase Locked Loop	LM567H
TBA120N	FM IF Amp & Demodulator	TBA120T
TBA120S-2	8-Stage Amp w/Balanced Demodulator	TBA120S II
TBA120S-3	8-Stage Amp w/Balanced Demodulator	TBA120S III
TBA120S-4	8-Stage Amp w/Balanced Demodulator	TBA120S IV
TBA120S-5	8-Stage Amp w/Balanced Demodulator	TBA120S V
TBA120SN	8-Stage w/Balanced Demodulator	TBA120SQ
TBA120S-2N	8-Stage w/Balanced Demodulator	TBA120SQ II
TBA120S-3N	8-Stage w/Balanced Demodulator	TBA120SQ III
TBA120S-4N	8-Stage w/Balanced Demodulator	TBA120SQ IV
TBA120S-5N	8-Stage w/Balanced Demodulator	TBA120SQ V
TBA120U	FM IF Amp & Demodulator	TBA120U
TBA120UN	FM IF Amp & Demodulator	TBA120UQ
TEXAS INSTRUMENTS		
μA709CN	Op Amp	LM709CN
μA709CP	Op Amp	LM709CN-8
μA711CN	Dual Comparator	LM711CN
μA723CJ	Voltage Regulator	LM723CJ
μA723CN	Voltage Regulator	LM723CN
μA723MJ	Voltage Regulator	LM723J
μA733CN	Video Amp	LM733CN
μA741CJ	Compensated Op Amp	LM741CJ-14
μA741CJ	Compensated Op Amp	LM741CN-14
μA741CJG	Compensated Op Amp	LM741CJ
μA741CP	Compensated Op Amp	LM741CN
μA741MJ	Compensated Op Amp	LM741J-14
μA741MJG	Compensated Op Amp	LM741J
μA748CJG	Op Amp	LM748CJ
μA748CN	Op Amp	LM748CN
μA748MJ	Op Amp	LM748J-14
μA748MJG	Op Amp	LM748J

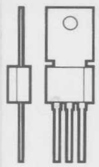
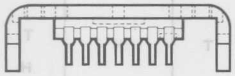
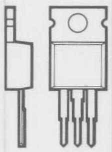
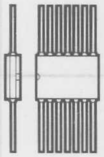
Device No.	Function	National Direct Replacement
TEXAS INSTRUMENTS (Continued)		
μA78XXCKC	Positive Voltage Regulator	LM78XXCT
μA78LXXACL	Positive Voltage Regulator	LM78LXXACZ
μA78LXXCLP	Positive Voltage Regulator	LM78LXXCZ
μA78MXXCKD	Positive Voltage Regulator	LM78MXXCP
μA79XXCKC	Negative Voltage Regulator	LM79XXCT
μA79MXXCKD	Negative Voltage Regulator	LM79MXXCP
LF356P	JFET Input Op Amp	LF356N
LM101AJ	Improved Op Amp	LM101AJ-14
LM101AJG	Improved Op Amp	LM101AJ
LM107J	Compensated Op Amp	LM107J-14
LM107JG	Compensated Op Amp	LM107J
LM111J	Voltage Comparator	LM111J
LM111JG	Voltage Comparator	LM111J-8
LM118JG	High Slew Rate Op Amp	LM118J
LM124J	Quad Op Amp	LM124J
LM124N	Quad Op Amp	LM1$24N
LM139J	Quad Comparator	LM139J
LM201AJ	Improved Op Amp	LM201AJ-14
LM201AJG	Improved Op Amp	LM201AJ
LM201AN	Improved Op Amp	LM201AN
LM207J	Compensated Op Amp	LM207J-14
LM207JG	Compensated Op Amp	LM207J
LM218JG	High Slew Rate Op Amp	LM218J-8
LM224J	Quad Op Amp	LM224J
LM239J	Quad Comparator	LM239J
LM301AJ	Improved Op Amp	LM301AJ-14
LM301AJG	Improved Op Amp	LM301AJ
LM301AN	Improved Op Amp	LM301AN
LM307J	Compensated Op Amp	LM307J-14

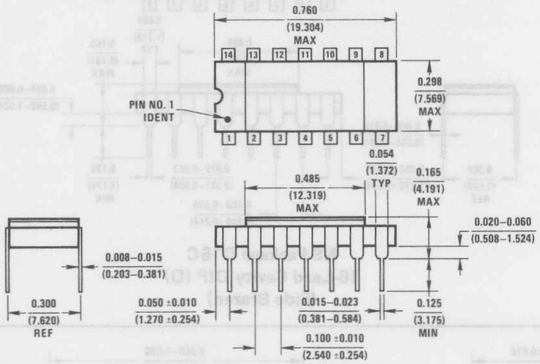
Device No.	Function	National Direct Replacement
TEXAS INSTRUMENTS (Continued)		
LM307JG	Compensated Op Amp	LM307J
LM307N	Compensated Op Amp	LM307N
LM311J	Voltage Comparator	LM311J
LM311JG	Voltage Comparator	LM311J-8
LM311N	Voltage Comparator	LM311N-14
LM311P	Voltage Comparator	LM311N
LM317KC	3-Terminal Adjustable Regulator	LM317T
LM318JG	High Slew Rate Op Amp	LM318J-8
LM318P	High Slew Rate Op Amp	LM318N
LM324J	Quad Op Amp	LM324J
LM324N	Quad Op Amp	LM324N
LM339J	Quad Comparator	LM339J
LM339N	Quad Comparator	LM339N
LM358P	Dual Op Amp	LM358N
LM376P	Positive Voltage Regulator	LM376N
LM393P	Dual Comparator	LM393N
LM2901N	Quad Comparator	LM2901N
LM2902J	Quad Op Amp	LM2902J
LM2902N	Quad Op Amp	LM2902N
LM2903P	Dual Comparator	LM2903N
LM2904P	Dual Op Amp	LM2904N
MC1558JG	Dual Compensated Op Amp	LM1558J
NE555CJG	Timer	LM555CJ
SE555JG	Timer	LM555J
TL081ACN	Single Low Cost Bi-Fet Op Amp	LF351AN
TL081CN	Single Low Cost Bi-Fet Op Amp	LF351N
TL087CP		LF411ACN
TL287CP		LF412CN
TL710CN	Comparator	LM710CN

National Semiconductor

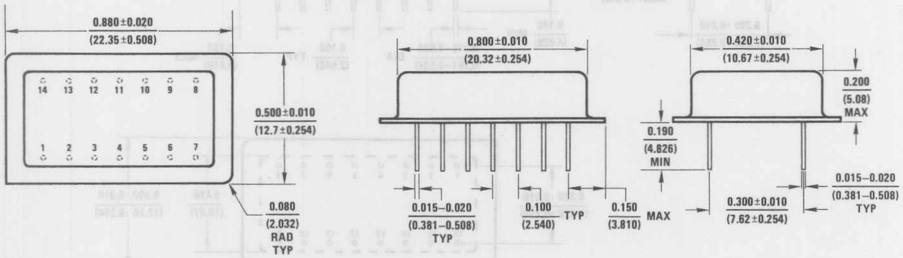
		NSC	Signetics	Fairchild	Motorola	TI	RCA	Silicon General	AMD	Raytheon
	14/16 Lead Glass/Metal DIP	D	I	D	L		D	D	D	D, M
	TO-99, TO-100, TO-5	H	T, K, L, DB	H	G	L	S*, V1**	T	H	T, H
	8, 14 and 16-Lead Low-Temperature Ceramic DIP	J	F	R, D	U	J				DC, DD
	TO-3 (Steel)	K			KS			K		K
	TO-3 (Aluminum)	KC	DA	K	K	K		K		LK, TK
	8, 14 and 16-Lead Plastic DIP	N	V, A, B	T, P	P	P, N	E	M, N	PC	N, DN, DP, MP

*With dual-in-line formed leads.
**With radially formed leads.

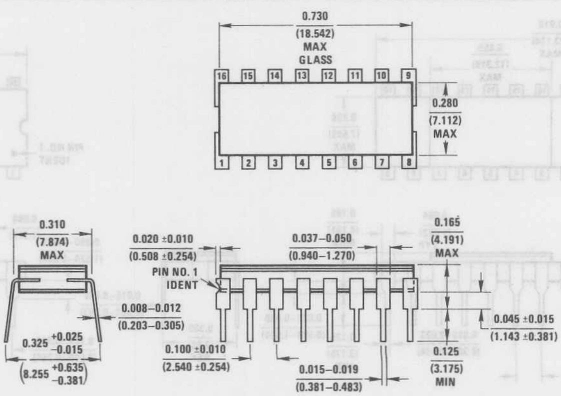
		NSC	Signetics	Fairchild	Motorola	TI	RCA	Silicon General	AMD	Raytheon
	TO-202 (D-40, Durawatt)	P				KD				
	"SGS" Type Power DIP	S		BP						
	TO-220	T	U	U		KC				
	Low Temperature Glass Hermetic Flat Pack	W		F	F	W			FM	
	TO-92 (Plastic)	Z	S	W	P	LP				



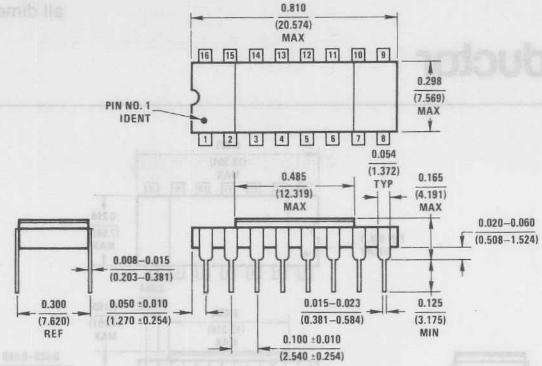
NS Package D14E
14-Lead Cavity DIP (D)
(Side Brazed)



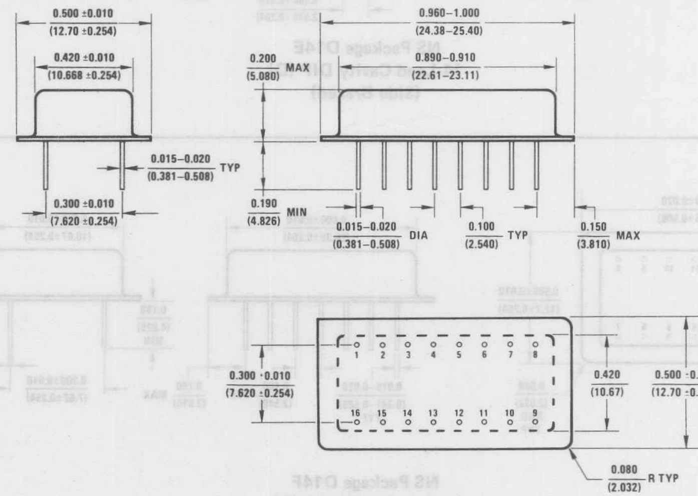
NS Package D14F
14-Lead Metal DIP (D)



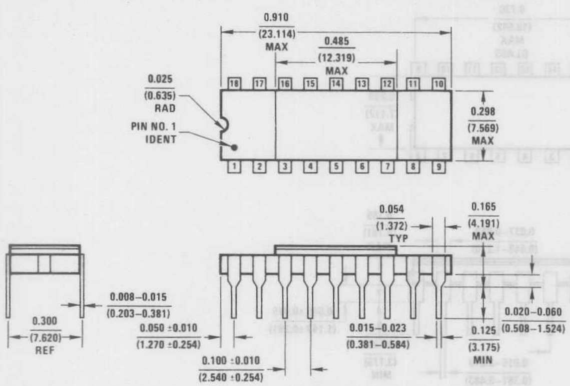
NS Package D16A
16-Lead Cavity DIP (D)



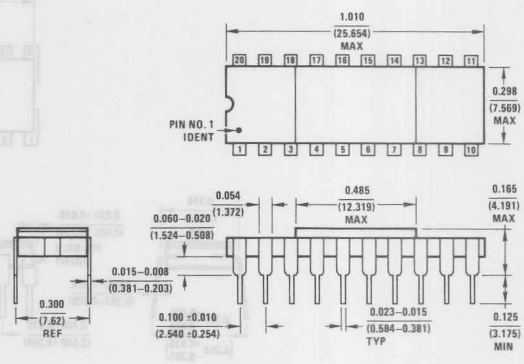
NS Package D16C
16-Lead Cavity DIP (D)
(Side Brazed)



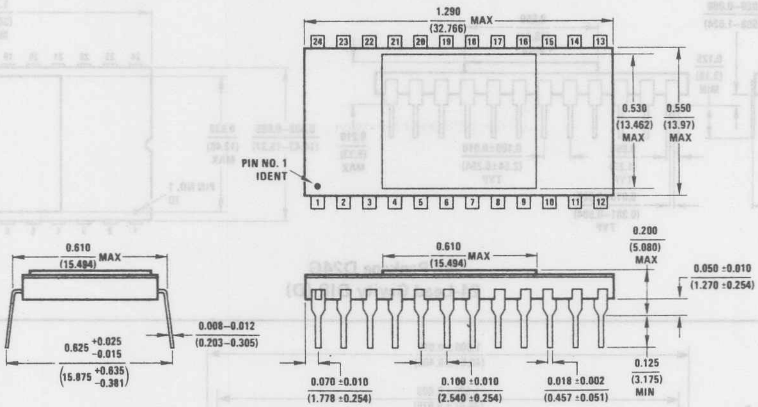
NS Package D16D
16-Lead Metal DIP (D)



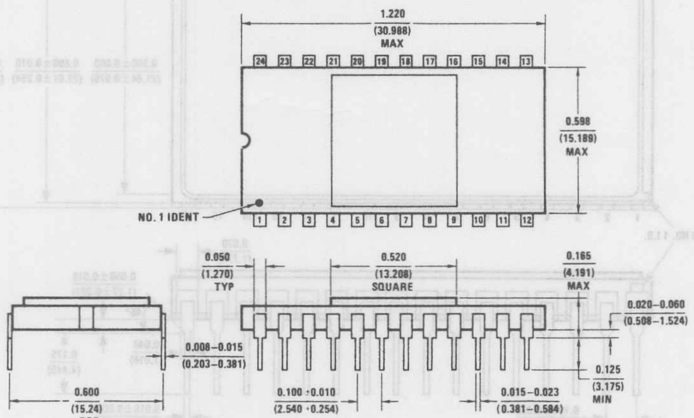
NS Package D18A
18-Lead Cavity DIP (D)
(Side Brazed)



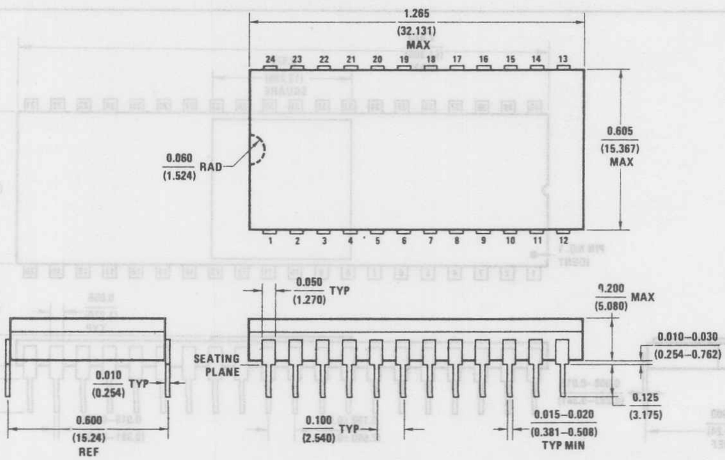
NS Package D20A
20-Lead Cavity DIP (D)



NS Package D24A
24-Lead Cavity DIP (D)

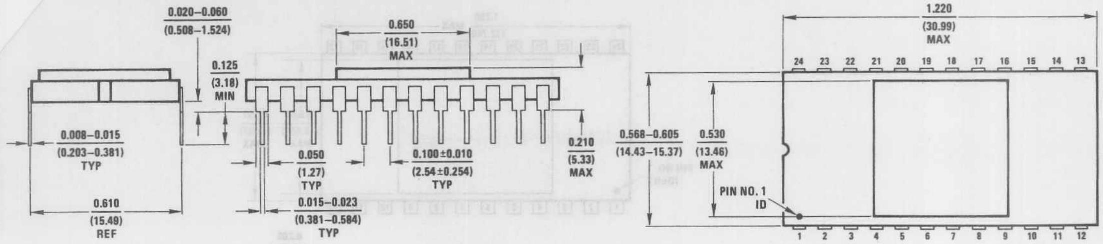


NS Package D24C
24-Lead Cavity DIP (D)

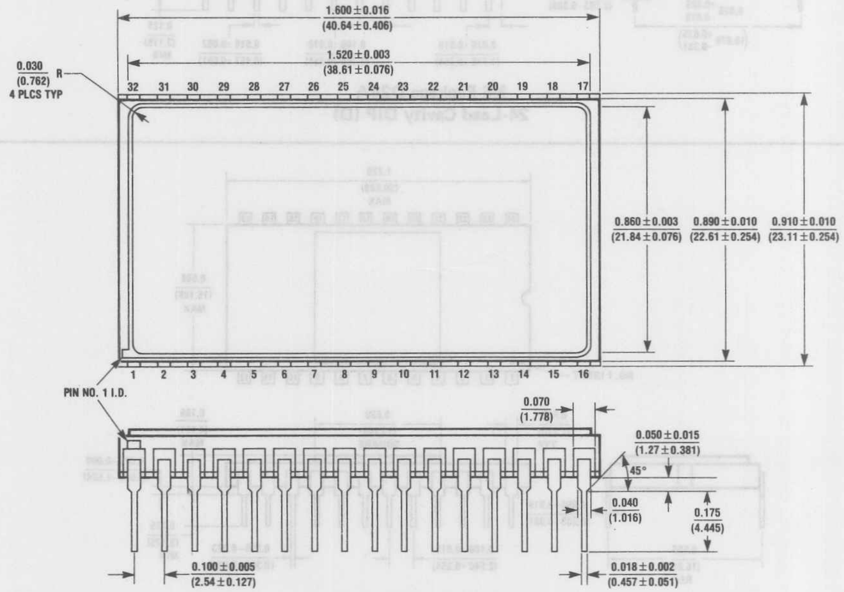


NS Package D24D
24-Lead Cavity DIP (D)

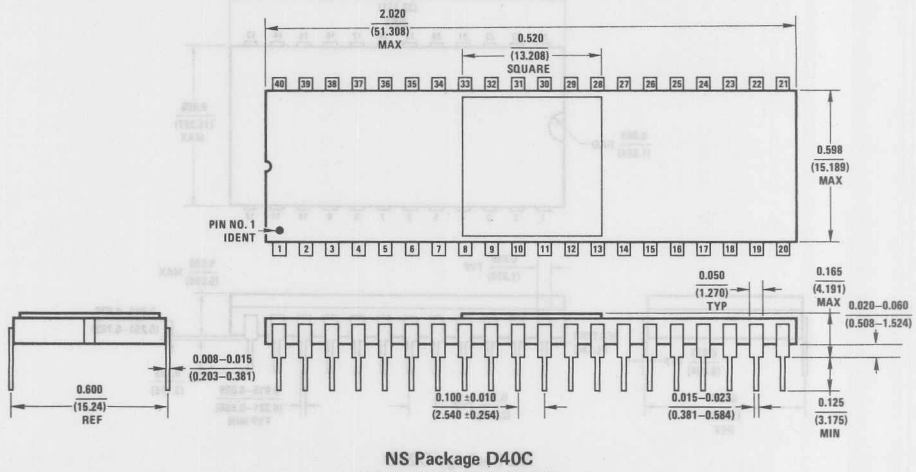
14



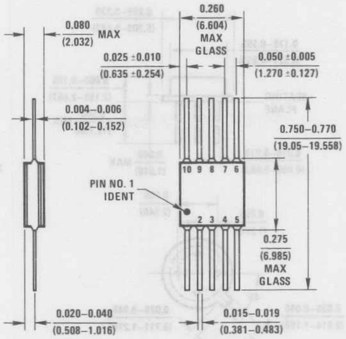
NS Package D24G
24-Lead Cavity DIP (D)



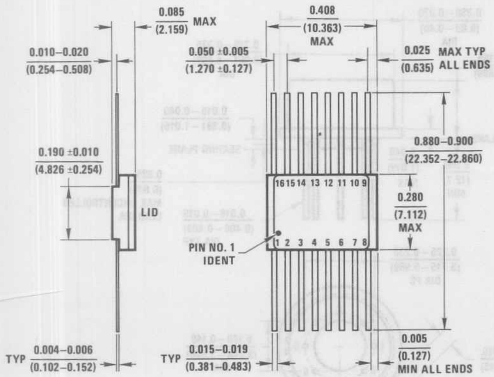
NS Package D32B
32-Lead Cavity DIP (D)
(Hybrid Side Blazed)



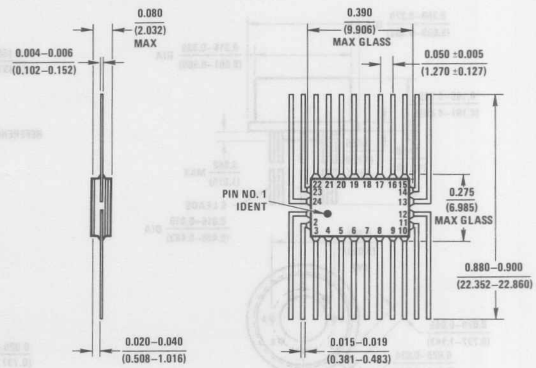
NS Package D40C
40-Lead Cavity DIP (D)



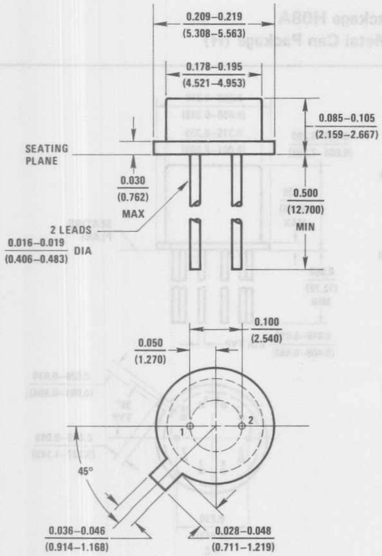
NS Package F10A
10-Lead Flat Package (F)



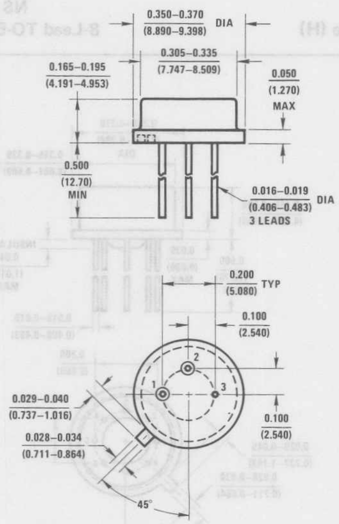
NS Package F16B
16-Lead Flat Package (F)



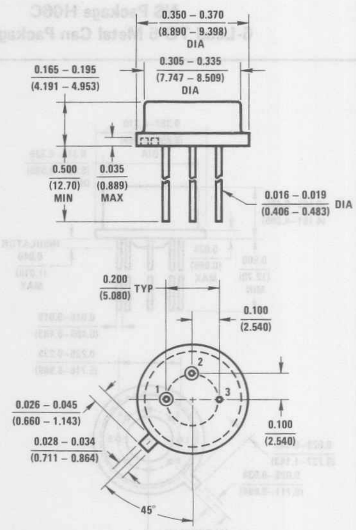
NS Package F24A
24-Lead Flat Package (F)



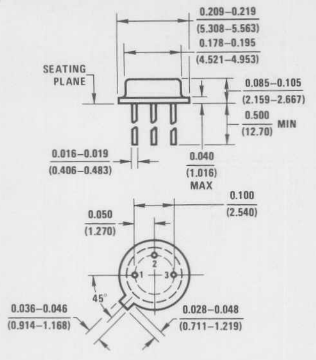
NS Package H02A
2-Lead TO-46 Metal Can Package (H)



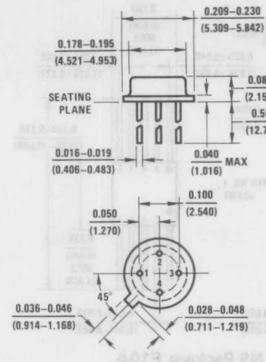
NS Package H03A
3-Lead TO-39 Metal Can Package (H)



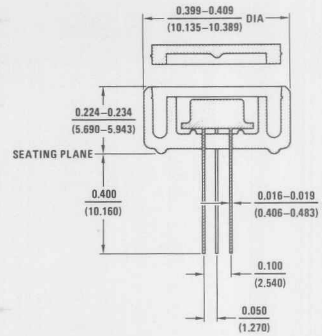
NS Package H03B
3-Lead TO-5 Metal Can Package (H)



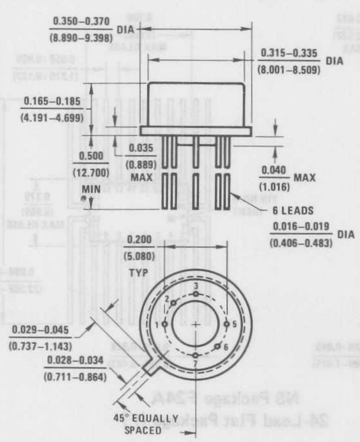
NS Package H03H
3-Lead TO-46 Metal Can Package (H)



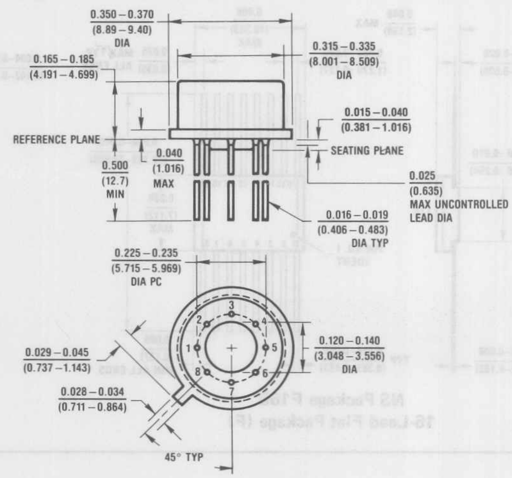
NS Package H04A
4-Lead TO-46 Metal Can Package (H)



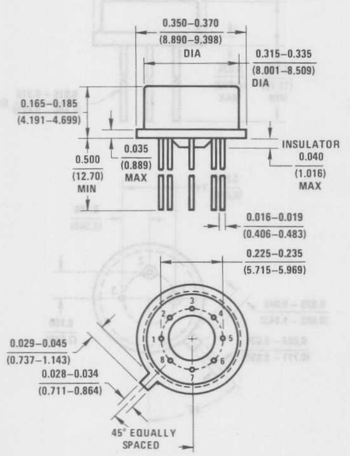
NS Package H04D
Thermal Shield for H04A



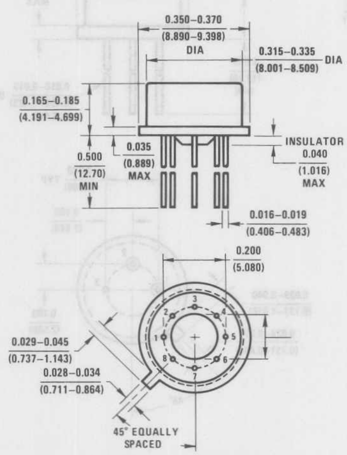
NS Package H06C
6-Lead TO-5 Metal Can Package (H)



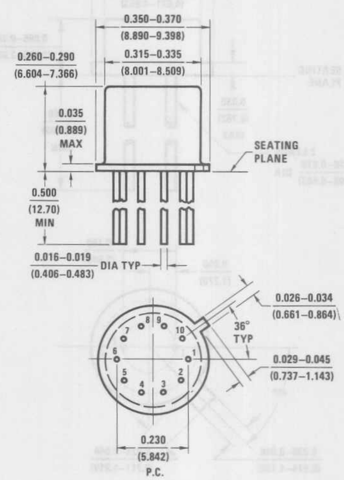
NS Package H08A
8-Lead TO-5 Metal Can Package (H)



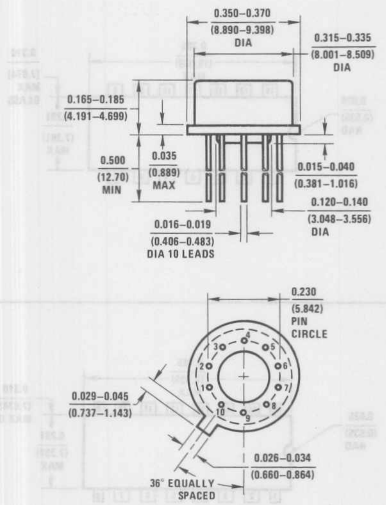
NS Package H08B
8-Lead TO-5 Metal Can Package (H)



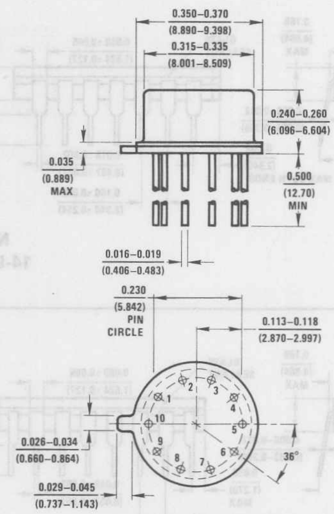
NS Package H08C
8-Lead TO-5 Metal Can Package (H)



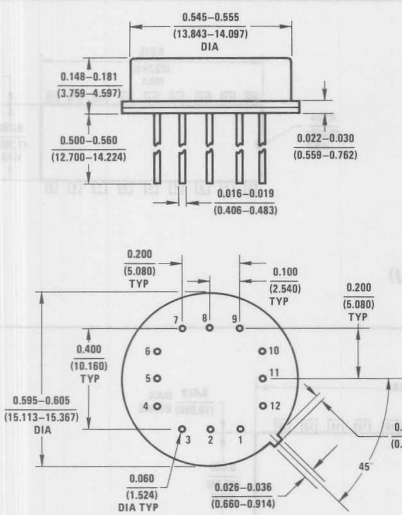
NS Package H10B
10-Lead TO-5 Metal Can Package (H)



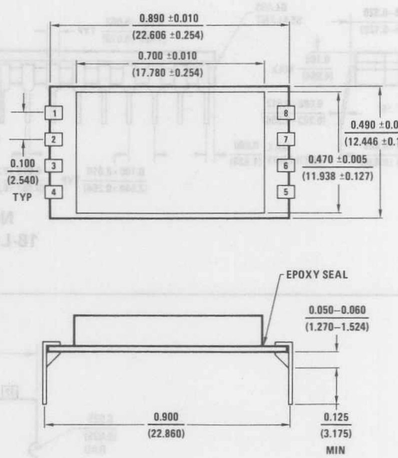
NS Package H10C
10-Lead TO-5 Metal Can Package (H)



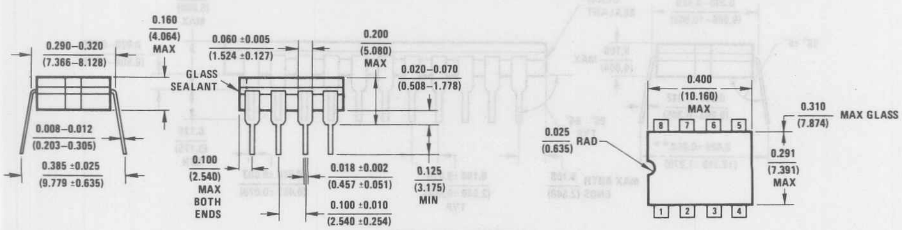
NS Package H10D
10-Lead TO-5 Metal Can Package (H)



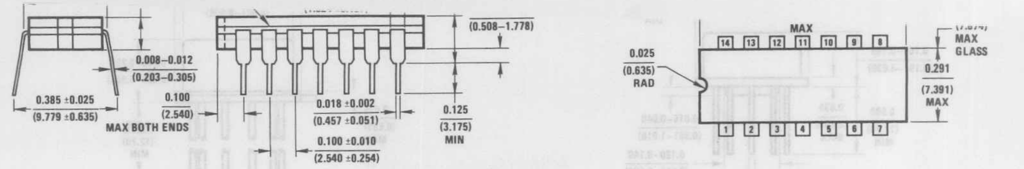
NS Package H12B
12-Lead TO-8 Metal Can Package (H)



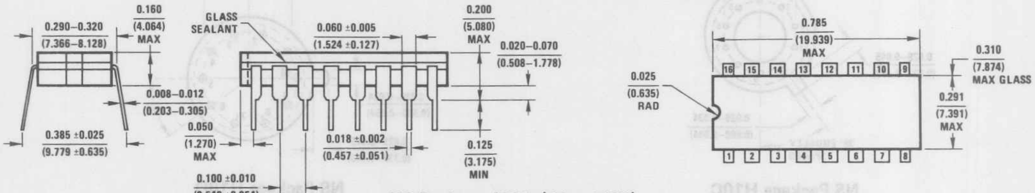
NS Package HY08A
8-Lead Cavity DIP (J) (Hybrid)



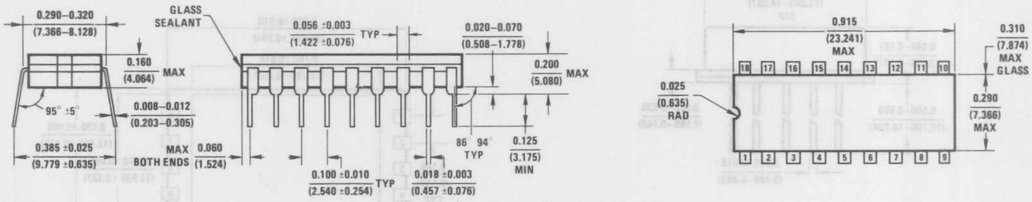
NS Package J08A
8-Lead Cavity DIP (J)



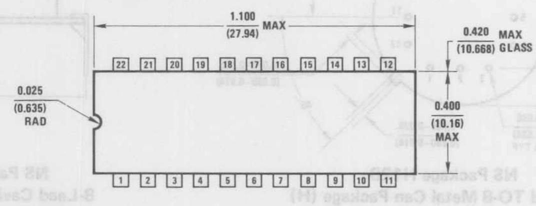
NS Package J14A
14-Lead Cavity DIP (J)

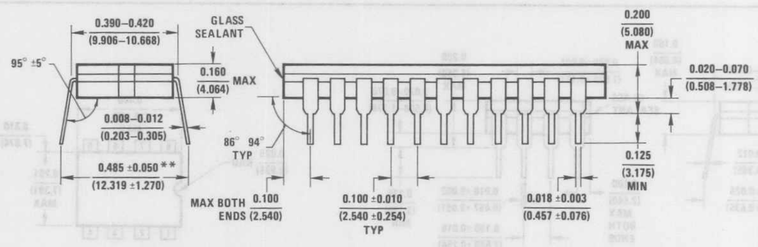


NS Package J16A (Also J16S)
16-Lead Cavity DIP (J)

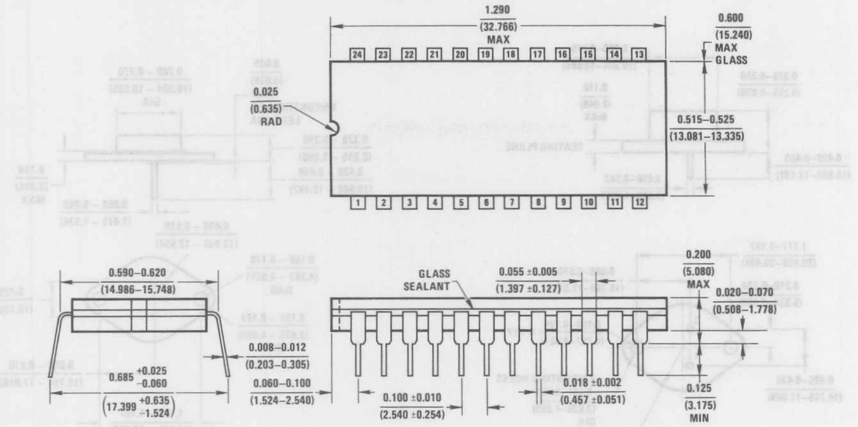


NS Package J18A
18-Lead Cavity DIP (J)

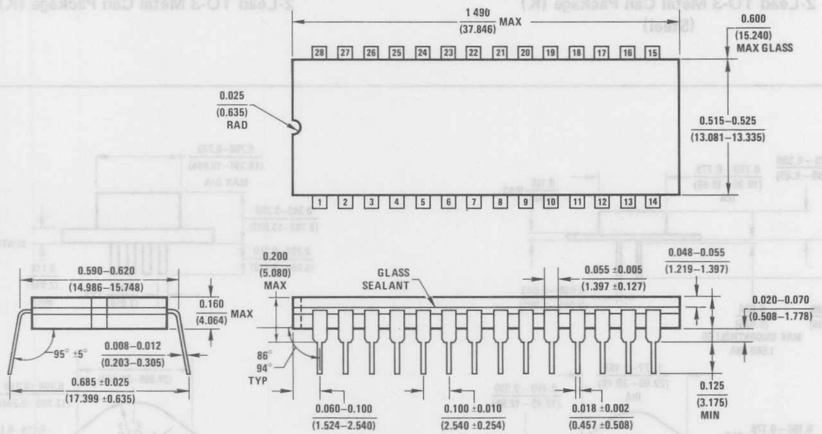




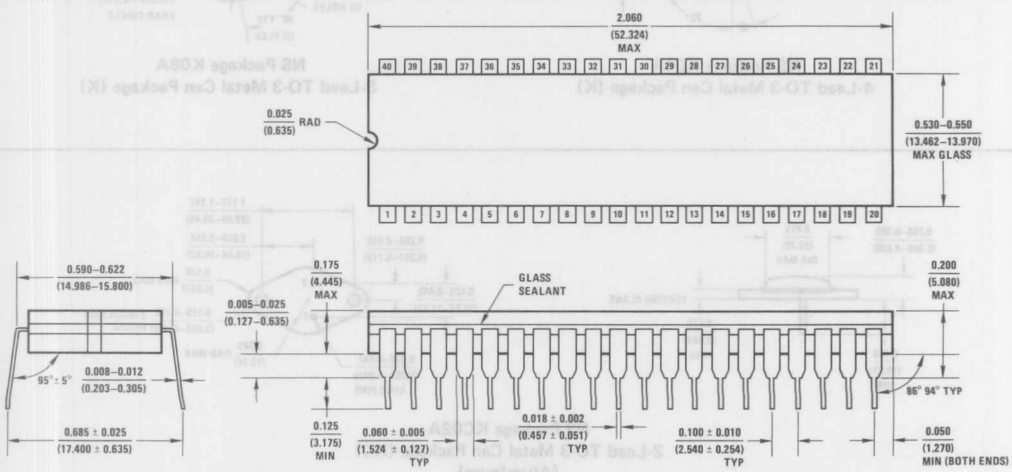
NS Package J22A
22-Lead Cavity DIP (J)



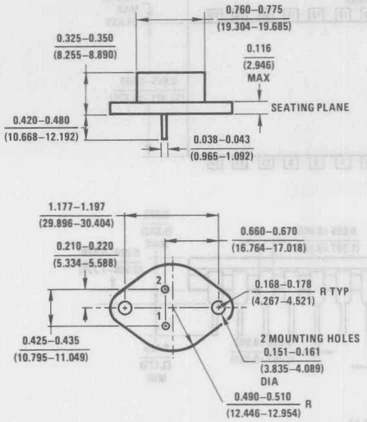
NS Package J24A
24-Lead Cavity DIP (J)



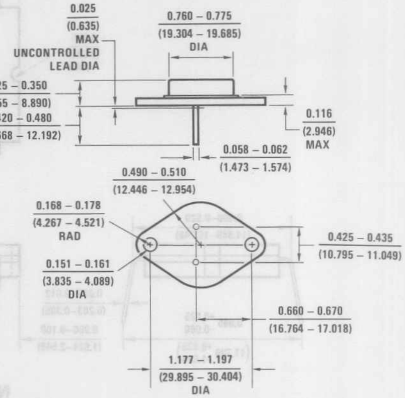
NS Package J28A
28-Lead Cavity Dip (J)



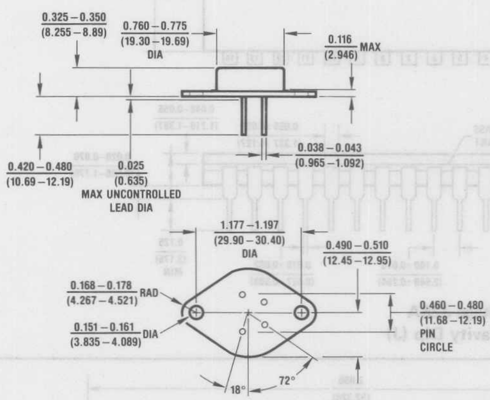
NS Package J40A
40-Lead Cavity DIP (J)



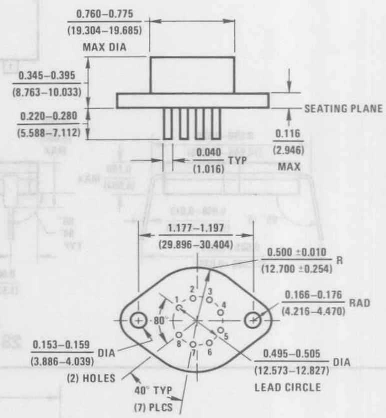
NS Package K02A
2-Lead TO-3 Metal Can Package (K)
(Steel)



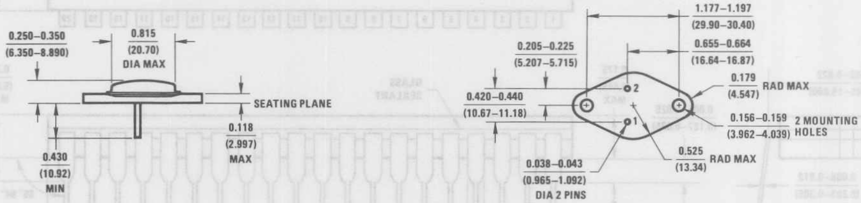
NS Package K02B
2-Lead TO-3 Metal Can Package (K)



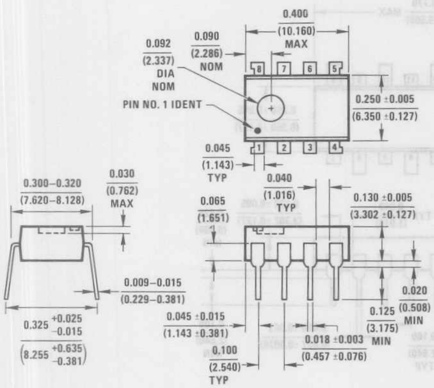
NS Package K04A
4-Lead TO-3 Metal Can Package (K)



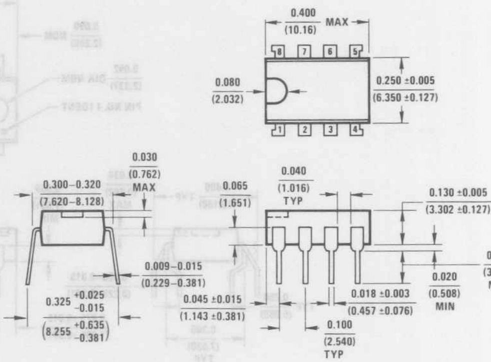
NS Package K08A
8-Lead TO-3 Metal Can Package (K)



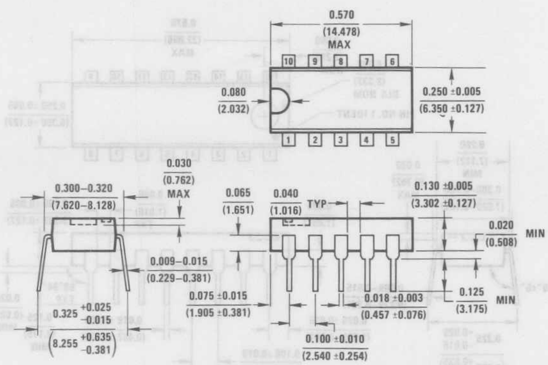
NS Package KC02A
2-Lead TO-3 Metal Can Package (KC)
(Aluminum)



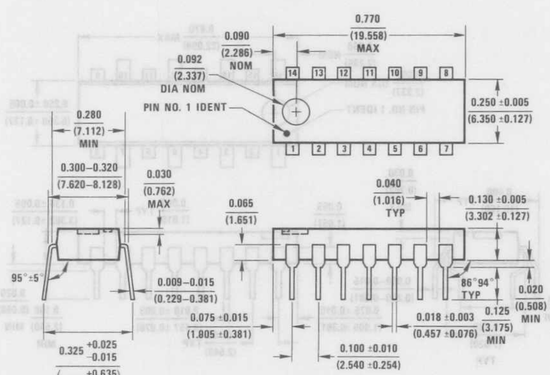
NS Package N08A
8-Lead Molded Mini-DIP (N)



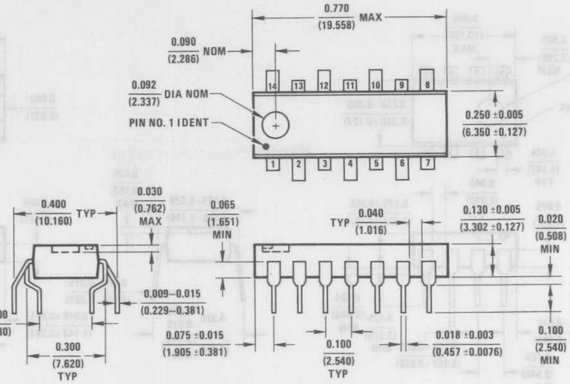
NS Package N08B
8-Lead Molded Mini-DIP (N)



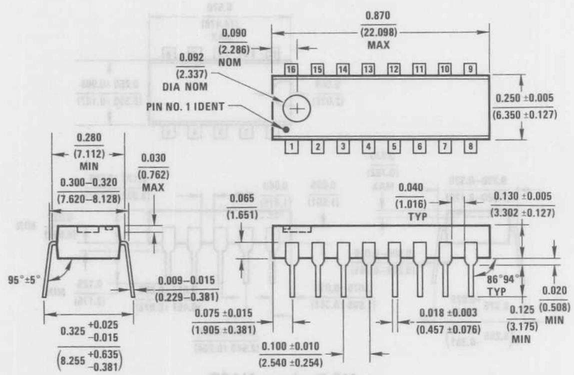
NS Package N10B
10-Lead Molded DIP (N)



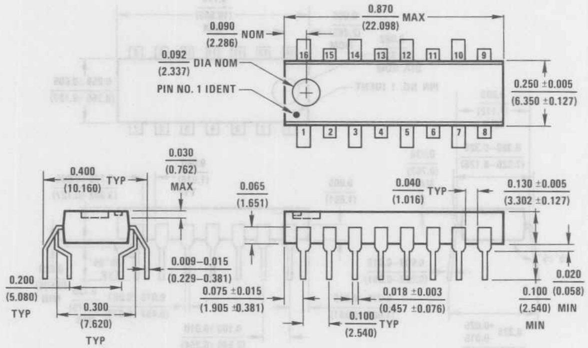
NS Package N14A
14-Lead Molded DIP (N)



NS Package N14C
14-Lead Molded DIP (N-01)
(Staggered Leads)

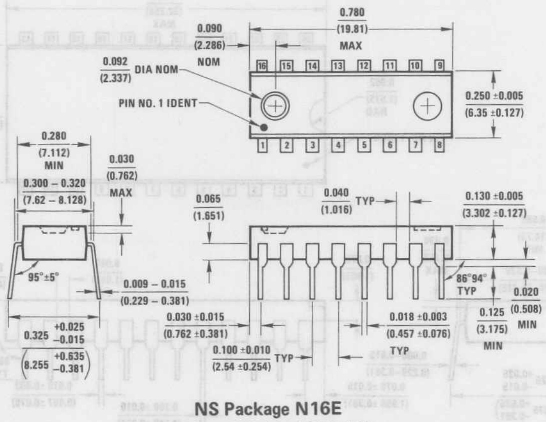


NS Package N16A
16-Lead Molded DIP (N)

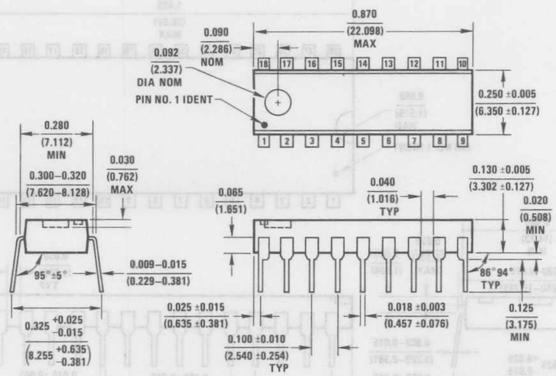


NS Package N16C
16-Lead Molded DIP (N-01)
(Staggered Leads)

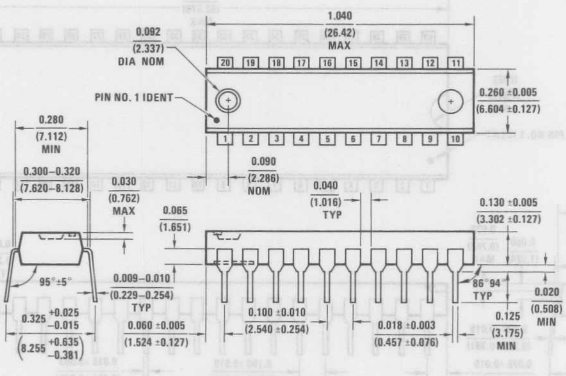
14



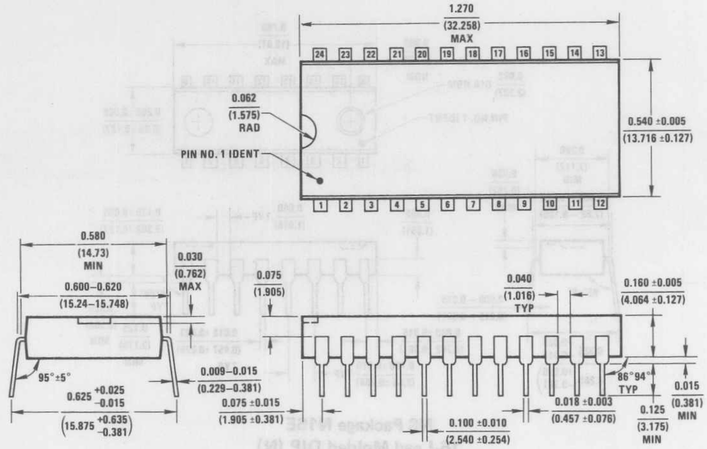
NS Package N16E
16-Lead Molded DIP (N)



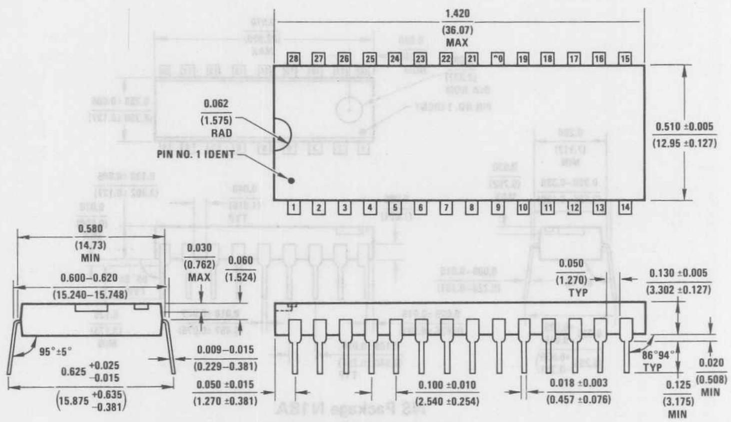
NS Package N18A
18-Lead Molded DIP (N)



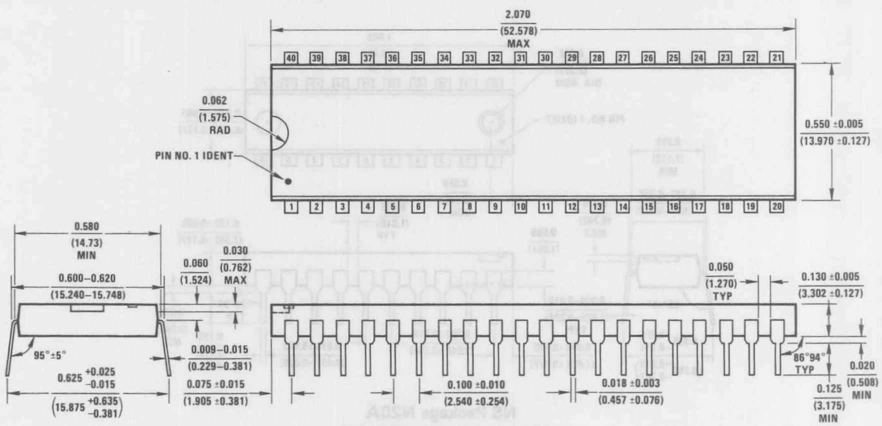
NS Package N20A
20-Lead Molded DIP (N)



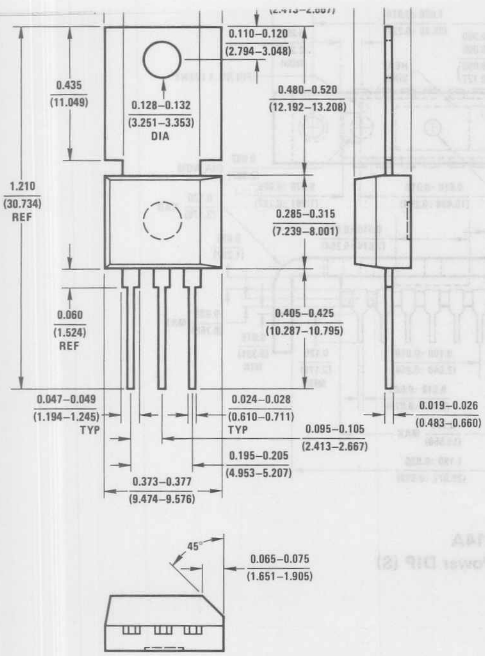
NS Package N24A
24-Lead Molded DIP (N)



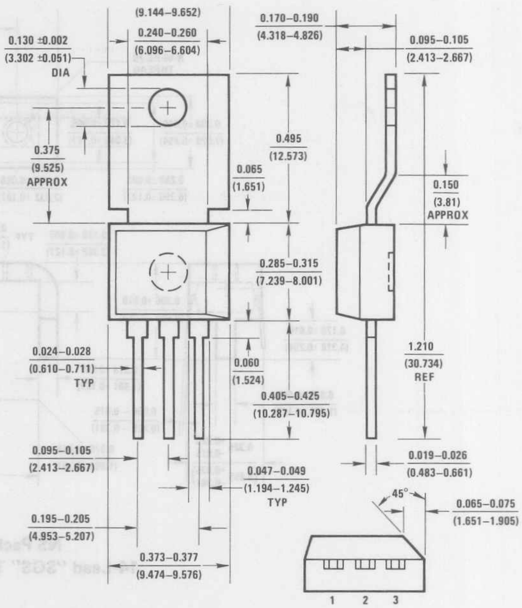
NS Package N28A
28-Lead Molded DIP (N)



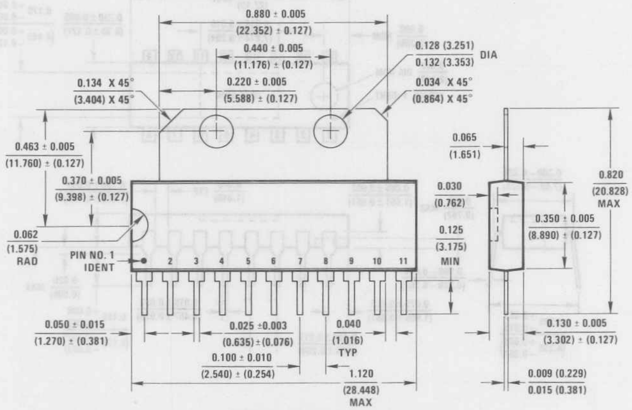
NS Package N40A
40-Lead Molded DIP (N)



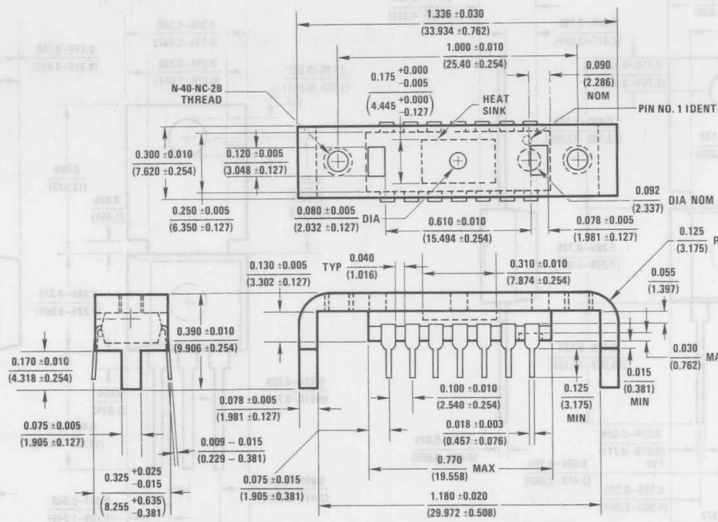
NS Package P03A
3-Lead TO-202 Power Package (P)



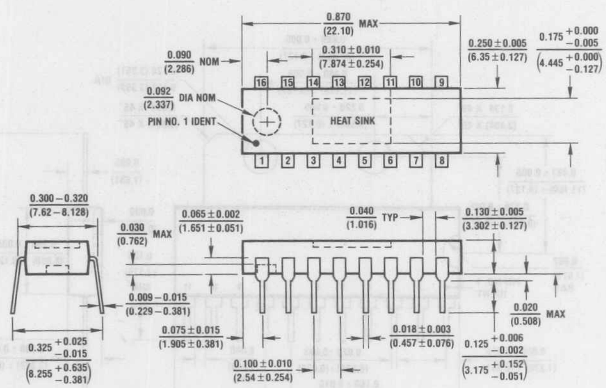
NS Package P03E
Tab Formed 3-Lead
TO-202 Power Package (P)



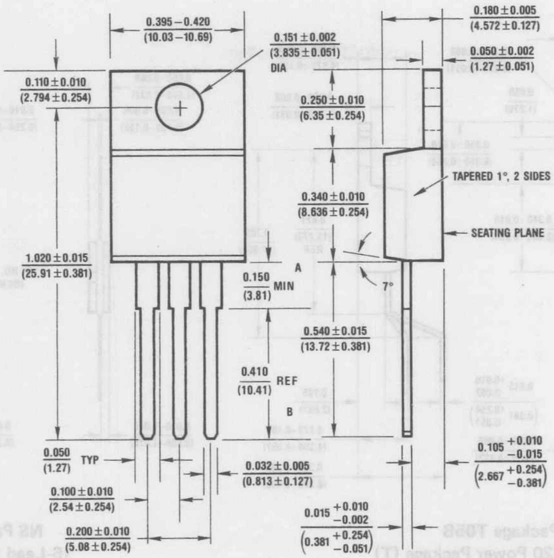
NS Package P11A
11-Lead Single-In-Line Package (P)



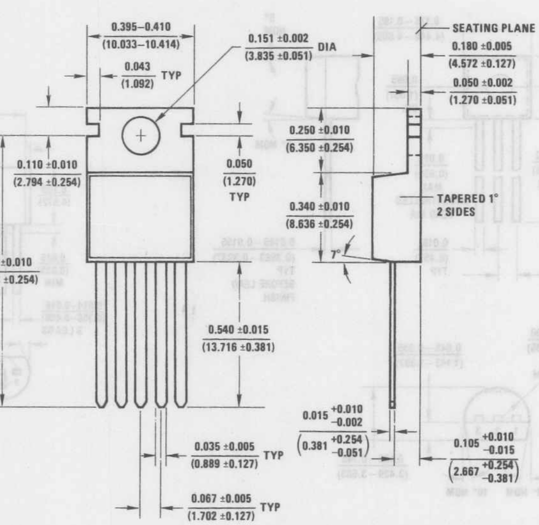
NS Package S14A
14-Lead "SGS" Type Power DIP (S)



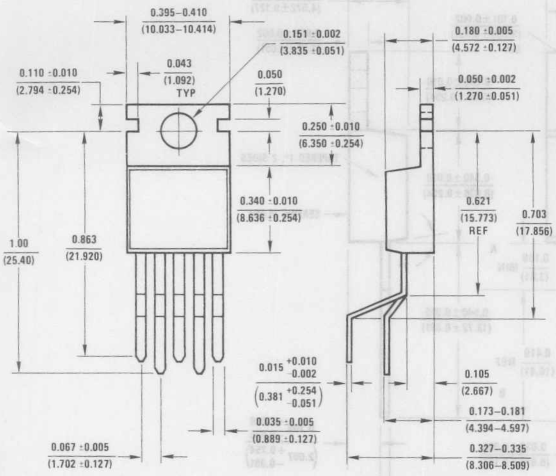
NS Package S16A
16-Lead Power DIP (S)



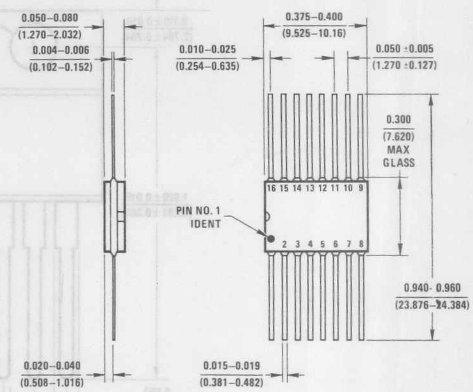
NS Package T03B
3-Lead TO-220 Power Package (T)



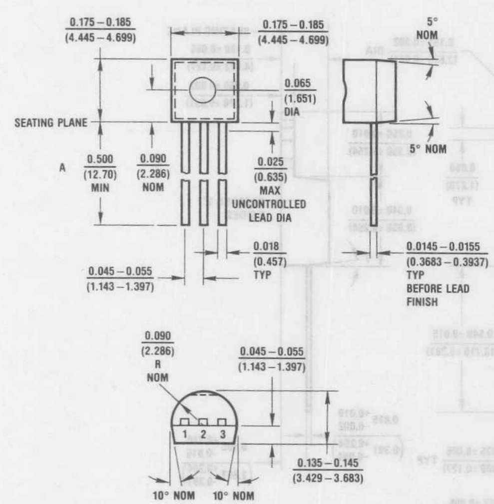
NS Package T05A
5-Lead TO-220 Power Package (T)



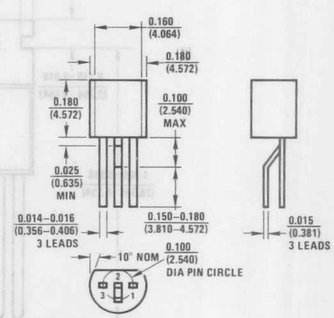
NS Package T05B
5-Lead TO-220 Power Package (T)



NS Package W16A
16-Lead Flat Package (W)



NS Package Z03A
3-Lead TO-92 Plastic Package (Z)



NS Package Z03D
3-Lead TO-92 Plastic Package (Z)